EE3450 Hw1 - Question 2

總分 14/14

Chapter 1 Computer Abstraction and Technology

0 分，共 0 分

Email Address *

zxc36mn999947@gmail.com

Name *

陳彥文

Student ID *

106061242

Question 2 (1.6)

14 分，共 14 分

Section 1.6

Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). The implementations are respectively P1 with a clock rate of 2.5 GHz and CPIs of 1, 1, 3, and 4, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2. Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 30% class B, 40% class C, and 20% class D.

✓ Which implementation is faster? * 2/2

- ○ P1
- ◉ P2 ✓

✓ What is the global CPI for P1 implementation? * 3/3

- ○ 1.4
- ◉ 2.4 ✓
- ○ 3.4

✓ What is the global CPI for P2 implementation? * 3/3

- ◉ 2 ✓
- ○ 3
- ○ 4

✓ Find the total clock cycles required in P1 cases.(Unit: 10^6 cycles) * 3/3

2.4 ✓

✓ Find the total clock cycles required in P2 cases.(Unit: 10^6 cycles) * 3/3

2 ✓