Department of Computer Science
National Tsing Hua University
CS4100 Computer Architecture
Spring, 2019
Homework 5
Deadline: 6/25 23:59

1. (60%) Suppose a cache receives the following 64-bit memory addresses for accessing 64-bit double words: (Note: Memory addresses are to the bytes.)
   0x018, 0x5a0, 0x158, 0x018, 0x010, 0x5f8, 0x2c0, 0x5f0, 0x070, 0x5f0, 0x5a8, 0x160
   (a) For each of these references, identify the tag, the index, and the block offset, given a direct-mapped cache with 8 one-doubleword blocks. Also, list whether each reference is a hit or a miss, assuming the cache is initially empty. If it is a miss, indicate the type of the miss, e.g. compulsory, conflict, or capacity. What is the hit rate?
   (b) Repeat (a) for a direct-mapped cache with two-doubleword blocks and a total size of four blocks.
   (c) Repeat (a) for a 2-way associative cache with four sets.

2. (40%) The following data constitute a stream of virtual byte addresses generated by a processor.
   0x123d, 0x08b3, 0x365c, 0x8716, 0xbee6, 0x3140, 0xc040
   Assume 8 KB pages, a four-entry fully associative TLB, and approximate LRU replacement. If pages must be brought in from disk, they can be placed anywhere in page frames 0 to 15. The initial TLB and page table states are as below.

TLB

Valid	Tag	Physical Page No.	Reference
1	0x5	11	0
1	0x7	4	1
1	0x3	6	0
0	0x4	9	1

Page Table

Index	Valid	Physical Page or in Disk
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9
5	1	11
6	0	Disk
7	1	4
8	0	Disk
…	…	…

   For each access shown above, list whether the access is a hit or miss in the TLB, whether the access is a page fault, the updated state of the TLB, and the corresponding physical address (give the last 12 bits).