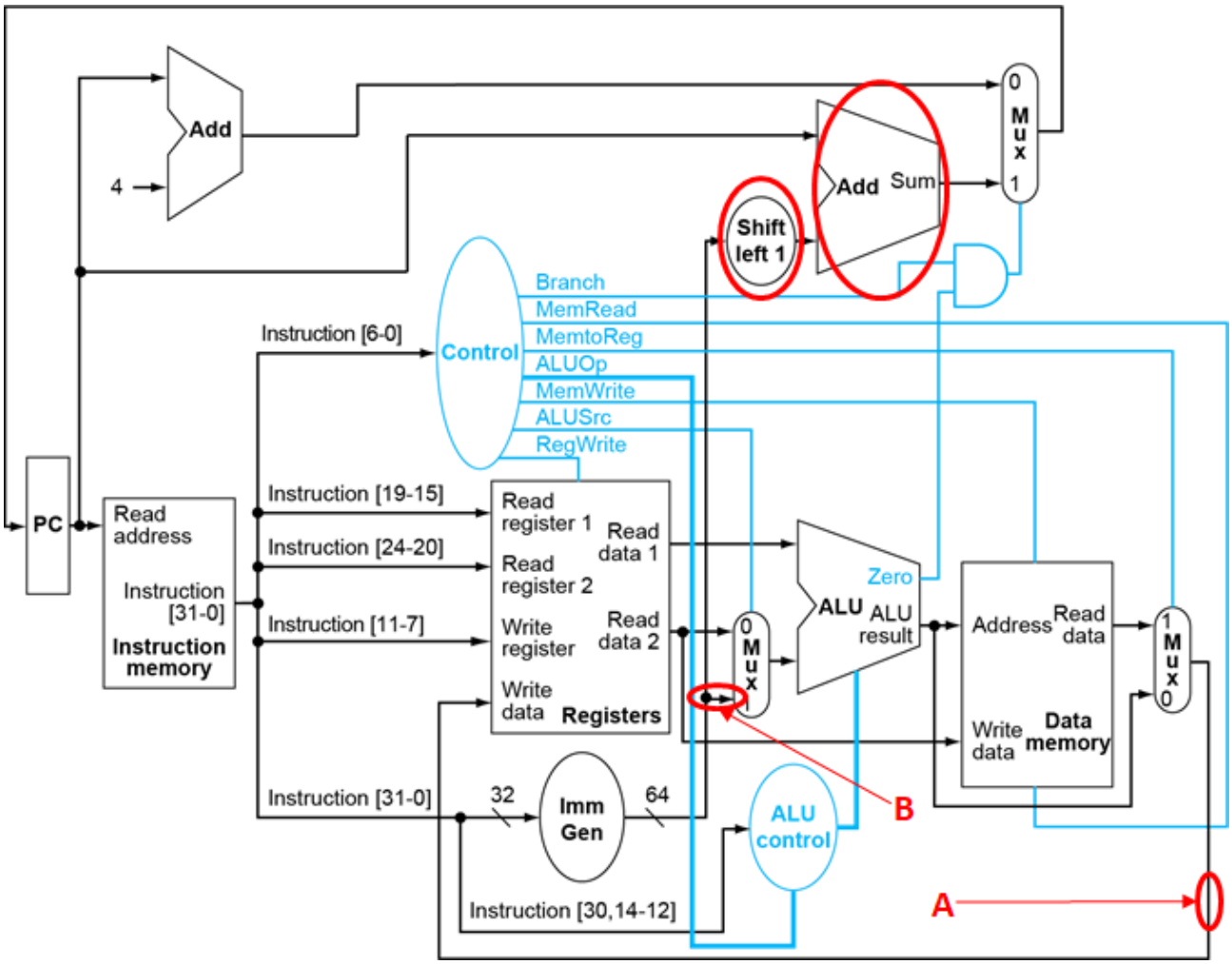
Department of Computer Science
National Tsing Hua University
CS4100 Computer Architecture
Spring, 2019
Homework 4
Deadline: 2019/05/27 18:00

1. (40%) Consider the single-cycle 64-bit RISC-V CPU shown below (Fig. 4.17). Suppose at a certain clock cycle, the following instruction is fetched: 1100 0010 0101 0001 1000 0000 1110 0011, which is stored starting at the memory location of $990087000080A0C0_{16}$.



Assume that the processor's registers have the following values at the beginning of the cycle in which the above instruction word is fetched:

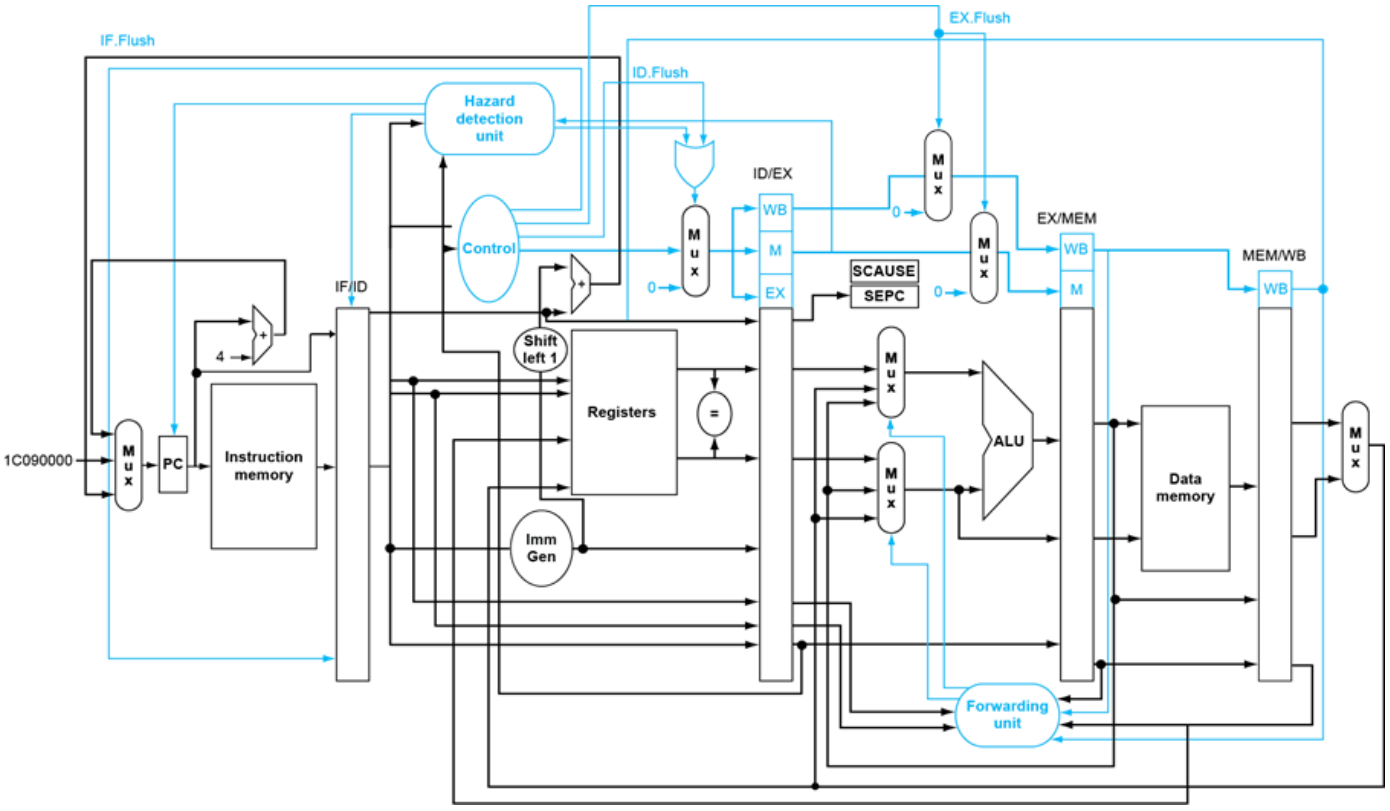
x0	x1	x2	x3	x4	x5	x6	x8	x12	x31
0	-1	2	-3	-4	-3	6	8	2	-16

(a) What is the output of the Imm Gen for this instruction word in decimal?

(b) What is the output of the ALU that is circled at the top right in hexadecimal?
(c) What are the values of all the control signals, including “Zero”, for this instruction?
(d) What is the new PC address after this instruction is executed? Highlight the path through which this value is determined.
(e) What are the contents of the above registers after this instruction is executed?
(f) Explain the purpose of the Shift left 1 that is in circle.
(g) Which instructions among add, sub, slt, sd, ld, and beq will fail if the path labeled A has been cut?
(h) Which instructions among add, sub, slt, sd, ld, and beq will fail if the path labeled B has been cut?
(i) If the control signal MemtoReg is stuck on 1, what instruction may fail?
(j) To execute this instruction, which of the following components act as a combinational circuit: PC, Instruction memory, Registers, ALU, Data memory? Give you reasons.

2. (50%) Consider the following sequence of instructions, which is to be executed on the RISC-V 5-stage pipelined datapath:

```
80:   ld    x4,4(x3)
84:   add   x1,x0,x4
88:   ld    x1,0(x1)
92:   beq   x4,x1,Loop
96:   sd    x2,0(x4)
```



(a) If there is no forwarding or hazard detection and the branch outcome is determined in the MEM stage, insert NOP instructions to ensure correct execution.

(b) Assume there is full forwarding with hazard detection but no stalling. Suppose the branch outcome is determined in the ID stage. Indicate hazards, if any, and add NOP instructions to eliminate them.

(c) Under the conditions of (b), without NOP, highlight the paths and indicate the values on the paths (similar to Fig. 4.60 in the textbook p.34) based on the pipeline shown in Fig. 4.63, when add of the above code is at the MEM stage.

(d) For the execution in (c), which data on the highlighted paths are in error due to no-stalling that eventually leads to incorrect execution of the code?

(e) Repeat (c), assuming full forwarding with hazard detection as well as stalling.

3. (10%) Assume the logic blocks needed to implement the datapath shown in Question 2 above have the following latencies: (Delays for other components are ignored.)

I-Mem	Add	Mux	ALU	Regs	D-Mem	Imm Gen	Shift-left	=
400 ps	100 ps	40 ps	120 ps	200 ps	350 ps	20 ps	10 ps	30 ps

Compute the required delay time for each stage of the datapath and determine the minimum cycle time of the computer.