NATIONAL TSING HUA UNIVERSITY
DEPARTMENT OF COMPUTER SCIENCE
CS 4100: Computer Architecture
Fall 2003, Mid-term Examination

1. (20%) Consider a program running on a 1-GHz processor with the following measurements:

Instruction type	Execution cycle	Number of instructions
Integer arithmetic and logic	2	350,000
Floating-point arithmetic	10	50,000
Load/store	5	300,000
Branch/jump	3	200,000
Others	2	100,000

   (a) What is the execution time of the program on the processor?
   (b) What is the maximum speedup if we enhance the performance of the floating-point unit in the processor?
   (c) Explain (b) in terms of the Amdahl's Law. Use the parameters: *f* as the faction of the program that can be enhanced and *s* as the ratio of improvement in the floating-point unit.

2. (10%) The following table shows the publication record of three universities, A, B, and C.

Journals	Number of papers published			Ratio relative to C		
	A	B	C	A	B	C
SCI	10	100	200	0.05	0.5	1
EI	1000	100	20	50	5	1

   (a) What is the performance ranking of universities A, B, and C using the arithmetic mean of the ratios relative to C?
   (b) Repeat (a) using the arithmetic mean of the ratios relative to B.
   (c) What kind of mean we should use to get a consistent ranking regardless of the reference?

3. (10%) Show the minimal sequence of instructions for the C statement:
   `x[1] = x[2] + c;`
   Assume that `c` corresponds to register `$t0` and the array `x` has a base address of 0x200.

4. (10%) The MIPS code segment on the right below implements the first few statements in the C recursive procedure on the left. What the values of A, B, and C?

```
int fact (int n)
{ if (n < 1) return (1);
  else return (n*fact(n-1));
}
```

```
fact: sub  $sp,$sp,  A
      sw     B
      sw     C
      slt    $t0,$a0,1
      beq    $t0,$0,L1
      .....
```

5. (10%) Complete the following table for Booth's multiplication of two signed 4-bit numbers: $0010_2 \times 1110_2$.

Iteration	Multiplicand	Product
0	0010	0000 1110 0
1		
…		

6. (10%) (a) Write the 32-bit IEEE 754 floating-point number representation of -28.625. (b) Which number represents a larger IEEE 754 floating-point number: 0x738E9BD0 or 0x058AB913?

7. (30%) Suppose we want to add the MIPS instruction `lh` (load halfword, opcode=0x21) to the single-cycle CPU shown in Figure 1. Assume that the data memory always supplies a word on a read. Therefore, we have to pick the lower two bytes (halfword) from the supplied word.
   (a) Modify Figure 1 to implement this instruction. Please show the extra control signals.
   (b) Can we reuse the "sign extend" unit in Figure 1 for (a)? Explain your reasons.
   (c) Modify the single-cycle controller shown in Figure 2 for (a).

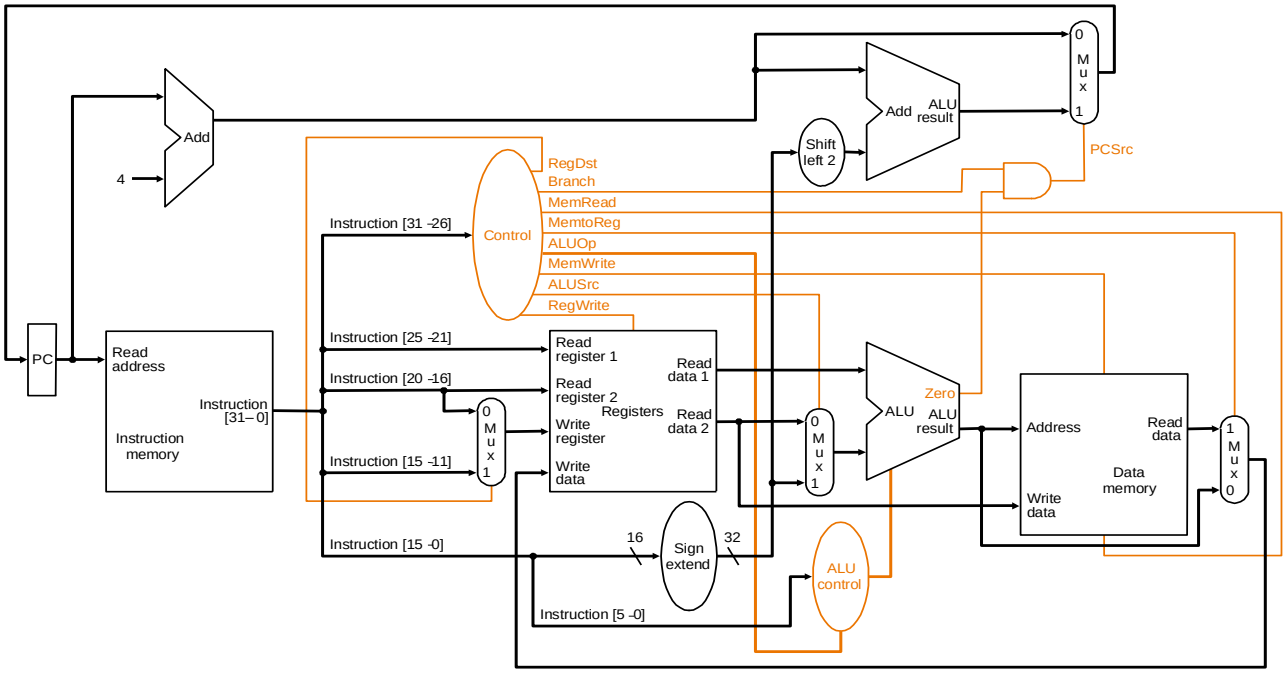

Figure 1

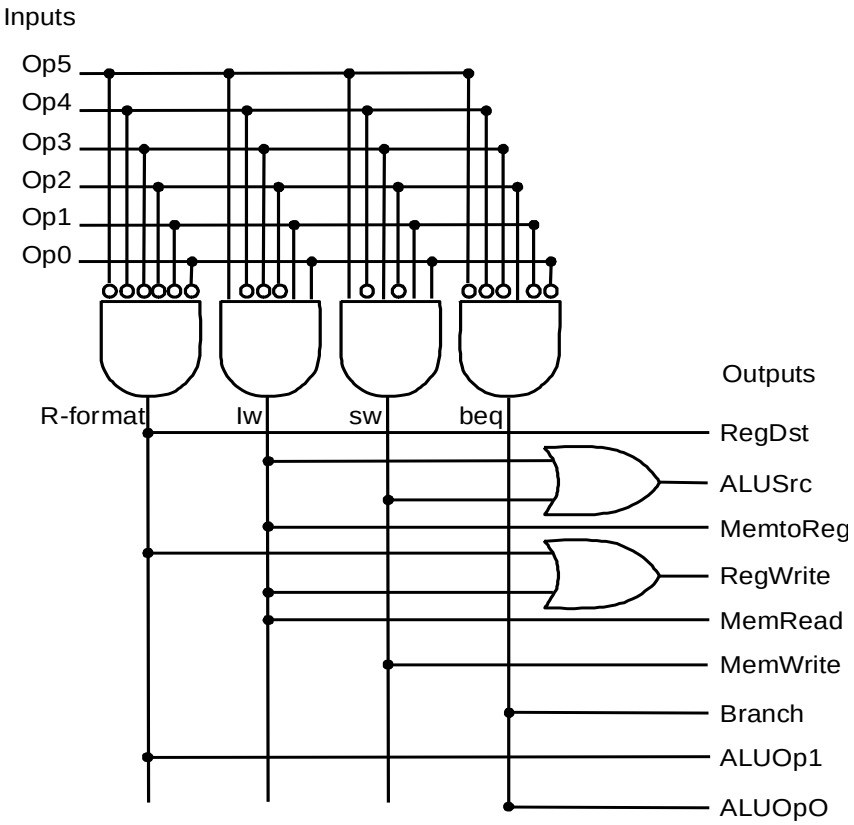

Figure 2