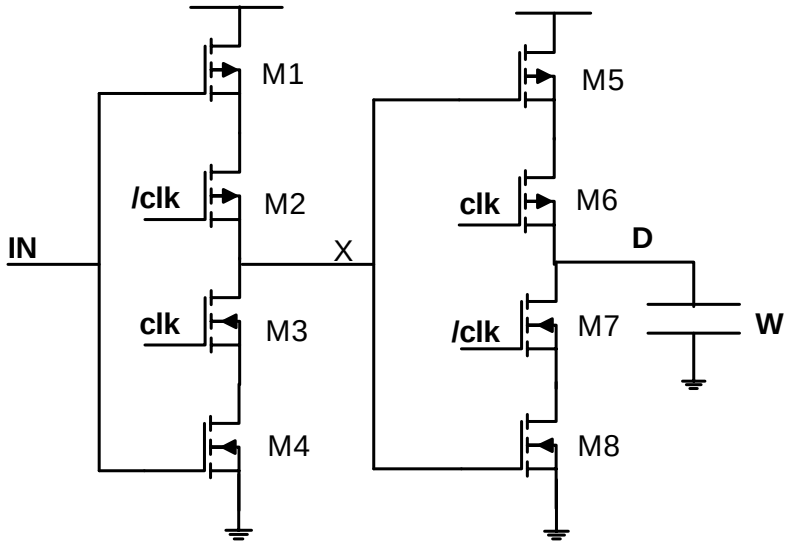
Sequential Logic (Solutions)

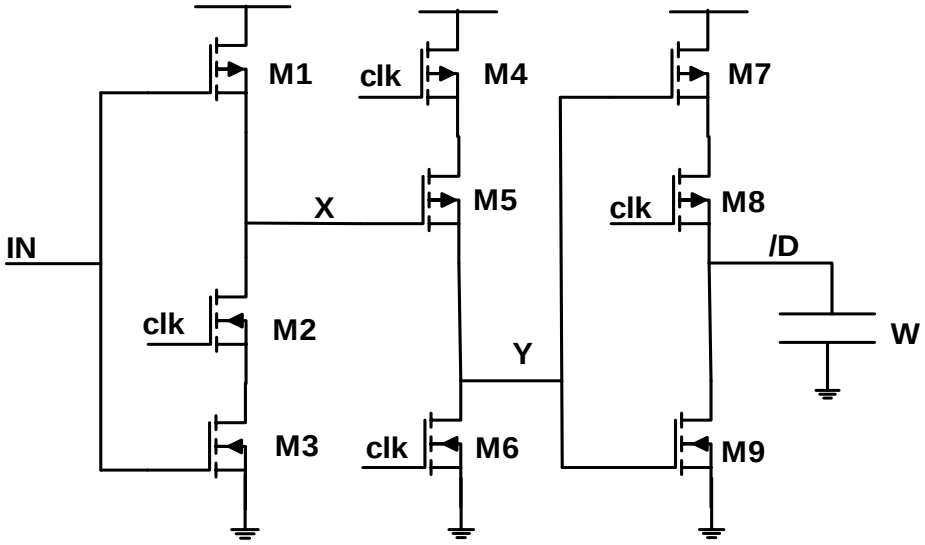
Solution1:

Part (i)
(a) Schematic for –ve edge triggered C^2MOS FF:



C^2MOS Flip-Flop

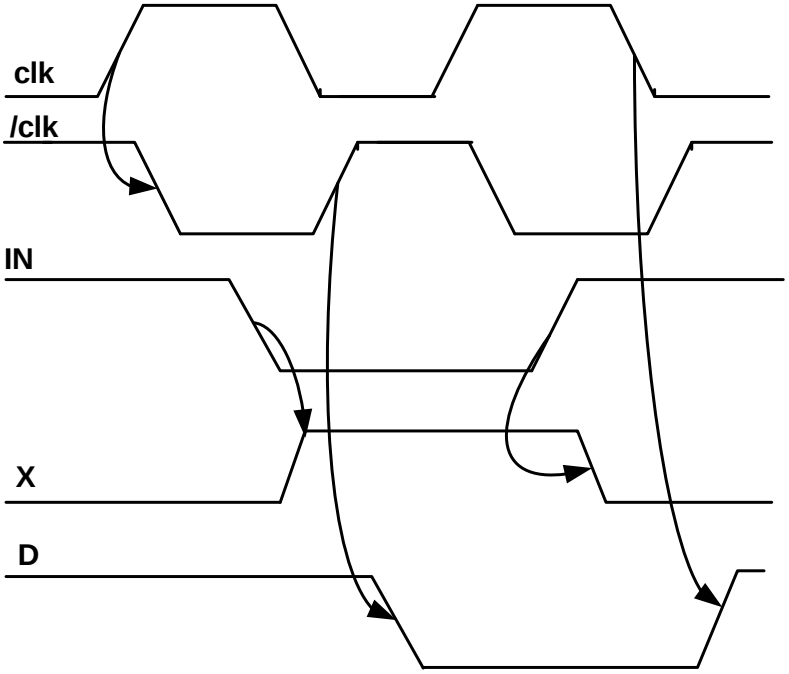
(b) Schematic for –ve edge triggered TSPC FF:



TSPC Flip-Flop

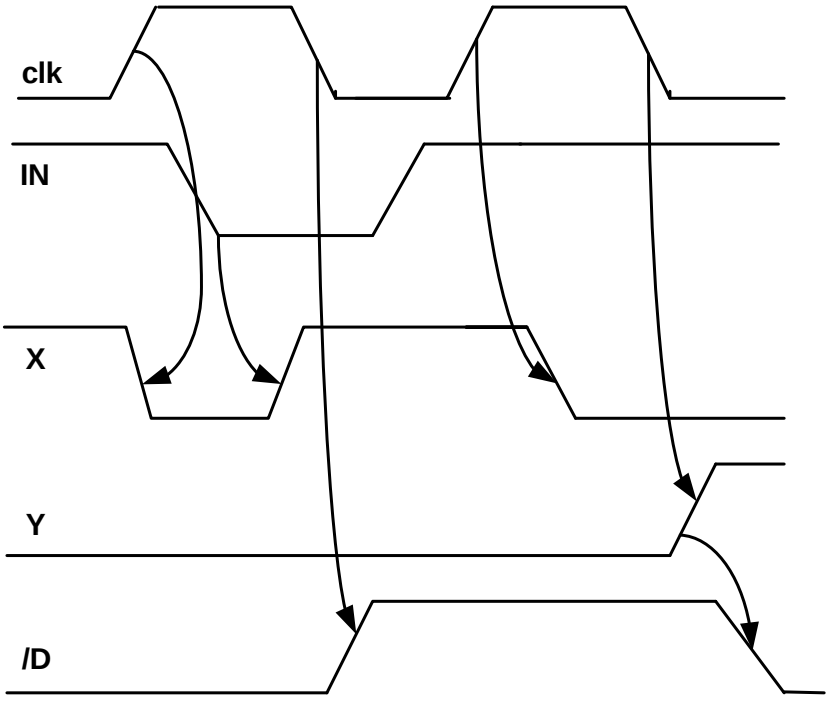
Part(ii) Timing diagrams

C^2MOS



C^2MOS Timing

TSPC

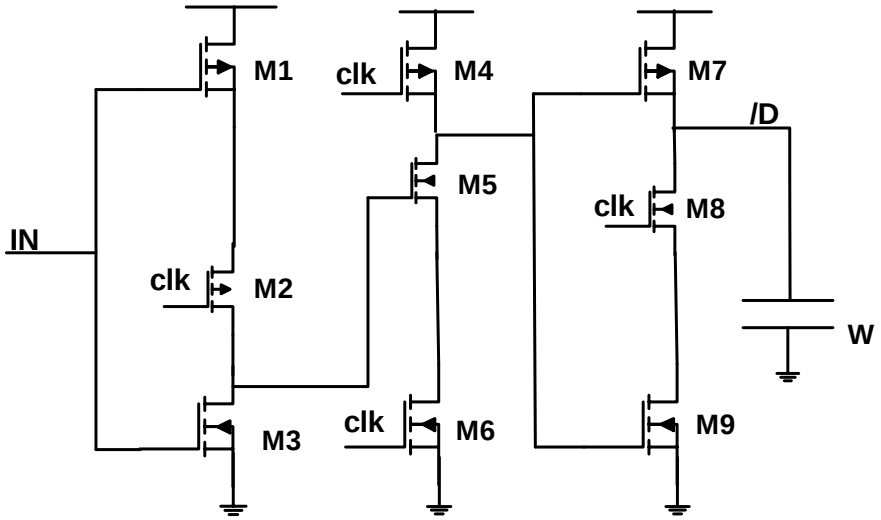


TSPC Timing

(iii) Converting –ve edge triggered to +ve edge triggered Flip-Flop

C^2MOS can be converter by simply interchanging the clk and /clk transistors. That is: For the +ve edge triggered Flip-Flop M2 and M7 should have clk signals while M3 and M6 should have /clk signal.

TSPC +ve edge triggered Flip-flop is shown below:



Positive edge triggered TSPC Flip-Flop

(iv) C^2MOS Sizing: Assume we size the flip flop for a stage ratio of 2. We will follow the same principle for transistor sizing as we did for the combinational logic tutorial. Hence, we first map the circuit to equivalent inverters and then size the master and stage sections. Sizing is done starting from the output Q terminal working our way back to the primary input. For this problem we also assume $\mu_n/\mu_p = 2.5$.

First, we size the slave section (transistors M5, M6, M7, M8).

The equivalent inverter driving the output load of W micron gate capacitance is designed for a stage ratio of 2. Hence, looking in into the input of the inverter, Wp + Wn of equivalent inverter = W/2.

Now, the ratio of the mobility is 2.5. So, for equal rise and fall times, we have Wp = 2.5Wn

Thus 3.5Wn = W/2. So Wn = W/7, Wp = 2.5W/7.

Now, these transistor sizes, pertaining to the inverter, need to be mapped to the slave section transistors. M5 and M6, are 2 p-MOS transistors in series, while M7 and M8 are 2 n-MOS transistors in series. So, they need to sized up by a factor of 2.

Thus we have M5 = M6 = 5W/7
And M7 = M8 = 2W/7

Now we need to size the transistors of the master section. The equivalent inverter representing the master section again drives an output load at node X equal to Wp(M5) + Wn(M8) = 5W/7 + 2W/7 = W.

Using the above technique as we used for the slave section we obtain identical sizes for the master section transistors:

M1 = M2 = 5W/7
M3 = M4 = 2W/7

This flip-flop needs both clk and /clk signals using a local inverter. The local inverter generating /clk signal drives transistors M2 and M7 and has a total output load of 5W/7 + 2W/7 = W

So for a stage ratio of 2, the clock inverter should be designed for Wp(clk) + Wn(clk) = W/2.

Hence Wp(clk) = 2.5W/7 and Wn(clk) = W/7

Thus the total transistor width on the clock network = (M2+M3+M6+M7+local inverter) = 2W + W/2 = 2.5W
Total transistor width on data network = (M1+M4+M5+M8) = 2W

The total delay (Clk→ Q) is the equivalent of 2 inverter delays.

The total transistor width on each network acts as a measure of the capacitance needed to be switched and can be used to estimate dynamic power (dominant component) when the data and clock activity factors are provided. This is a qualitative approach but is very handy when comparing different designs as will be apparent when we do the same for the TSPC flip flop in the next section.

TSPC sizing: The TSPC flip-flop can be visualized as a chain of 3 cascaded inverter stages. We design the inverters for a stage ratio of 2 and a $\mu_n/\mu_p = 2.5$. We start from the inverter at the output and work our way to the input. The output inverter has a sizing of:

Wp = 2.5W/7 and Wn = W/7 (same reasoning as for C^2MOS).

Thus, the inverter sizing can be mapped to the transistors (M7, M8, M9) as follows:

M7 and M8 are 2 p-MOS transistors in series and thus have the sizing 5W/7 each.
M9 remains equal to W/7.

The inverter for the middle stage, driving node Y, sees a load of: M7 + M9 = 6W/7

Thus the middle inverter stage is designed for a stage ratio of 2 such that the:

Wp(inv) + Wn(inv) = 3W/7

Since Wp(inv) = 2.5Wn(inv), we have 3.5Wn(inv) = 3W/7.

Hence, Wn(inv) = 3W/24.5 and Wp(inv) = 7.5W/24.5

Now these sizes need to be mapped to the transistors M4, M5, M6.
M4 and M5 are 2 series connected p-MOS and so each is sized as 2Wp(inv) = 15W/24.5
M6 remains at 3W/24.5

Now we need to size the input stage of the TSPC flip-flop.

The input inverter drives a load of M5 equal to 15W/24.5 hence the inverter should be sized for a total width of 7.5W/24.5 (stage ratio of 2)

Thus the Wp(inv) for this stage is (7.5*2.5)W/(24.5*3.5) and Wn(inv) = 7.5W/(24.5*3.5)

However, following the reasoning as before we observe that the 2 n-MOS transistors M2 and M3 are in series.

Thus M2 and M3 are each sized as M2 = M3 = 15W/(24.5*3.5) = 15W/85.75
While M1 size remains unchanged at M1 = (7.5*2.5)W/(24.5*3.5) = 18.75W/85.75

Now we can sum the clock and data transistor widths as follows:

Clock transistors: M2+M4+M6+M8 = 15W/85.75 + 15W/24.5+ 3W/24.5 + 5W/7 = 1.62W

Data transistors: M1+M3+M5+M7+M9 = 0.218W + 0.175W + 0.612W + 0.714W + 0.148W = 1.86W

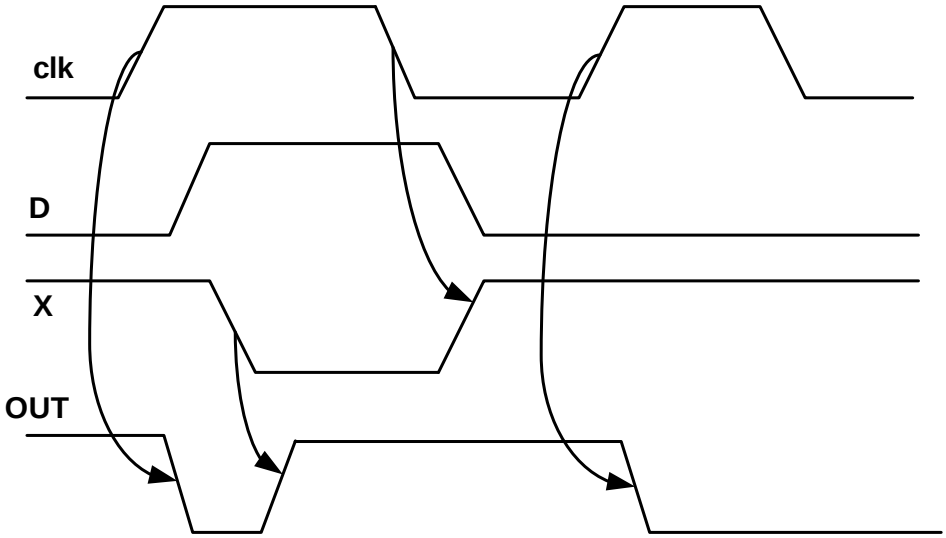
The equivalent delay can be quantified as equal to 3 inversion delays.

Hence, we can infer that the total power consumption of TSPC FF is less (less clock width, clock has higher switching activity) and better for a low power application, but offers poorer performance. Also, it needs to be noted that for TSPC we do not need clk and /clk signals and that it outputs the inverted data while C^2MOS needs for clk and /clk signals and outputs the true version of the input data.

Solution 2: Part (i) The circuit shown in the figure has 2 stages. The first stage is a dynamic gate implementing the logic function F = /(A.B) that is A NAND B.

The next stage is an inverting stage. So the overall logic function implemented is F = A.B and the two stages together implement a positive level sensitive latch. Thus, this is an example of a logic embedded latch.

Timing diagram:



(ii) The sizing strategy is the same as in problem 1 and that introduced in the combinational logic tutorials. We can visualize the gate as being 2 equivalent inverters cascaded back to back driving a load of W microns. We assume a stage ratio of 2 and mobility ratio of 2.5 as before. Following the same line approach as before we have:

The equivalent output inverter driving the net OUT and load of W should have a Wp(inv) = 2.5W/7 and Wn(inv) = W/7.

This leads us to size M5 = Wp(inv) = 2.5W/7, and
M6 = M7 = 2Wn(inv) = 2W/7

Now we design the input stage inverter (representing the equivalent of M1, M2, M3, M4). This inverter drives node X and sees a total load of M5 + M7 = 4.5W/7

Thus, the input stage inverter designed for a stage ratio of 2 should have:

Wp(inv) + Wn(inv) = 4.5W/(7*2)

Since Wp(inv) = 2.5Wn(inv) we have, Wp(inv) = (4.5*2.5)W/(14*3.5) = 0.229W
Wn(inv) = 0.092W

Now we map these inverter sizes to the transistors M1, M2, M3, M4

M1 remains that same as Wp(inv) = 0.229W

M2 = M3 = M3 = 3*Wn(inv) = 0.276W

Problem 3.

We consider the 2 following cases for the problem. Case 1 when there is no pipelining, and Case 2 when there is pipelining.

Case 1:

When there is no pipelining the worst case delay is:

T_{max}: T_{reg} + T_A+ T_B = (4 + 20 + 65)ps = 89ps (neglecting set-up time for the 2^{nd} register)

Thus the maximum frequency of operation = $f_{max} = 1/T_{max}$ = 11.2MHz

Assuming total power = dynamic power = CV^2f we have for 5V, 11.2MHz operation:

Power: (2*Reg + Mod A + Mod B) = (2*0.2 + 30 + 112)*5^2*11.2 (MHz*pF*V^2) = 39.8mW

Case 2:

Now we introduce a register stage between Modules A and B.

The new worst case delay is given by:

T_{max}: T_{reg} + T_B = (4+65)ps = 69ps. With a corresponding $f_{max} = 1/T_{max}$ = 14.5MHz

This results in an overall speedup by a factor of 89/69 = 1.27 (approx).

We can now do two things: (a) either operate the system at this higher frequency (there is extra latency and clock power) or (b) drop the voltage, get back to the same performance as in Case (i) and save power at iso-performance.

As per the requirements of the problem, we follow the second approach.

From the graph in the text book (pg. 247) we observe that to slow down the system by a factor of 1.27 we need to drop the supply voltage from 5V to 3.75V.

So, $V_{dd(new)}$ = 3.75V

Hence in the pipelined case at the new operating supply voltage with 3 stages of registers the power consumption is:

Power = (3*Reg + Mod A + Mod B) = (3*0.2 + 30 + 112)*3.75^2*11.2 (MHz*pF*V^2) = 22.5mW. This results in a total power savings by 44% (approx)