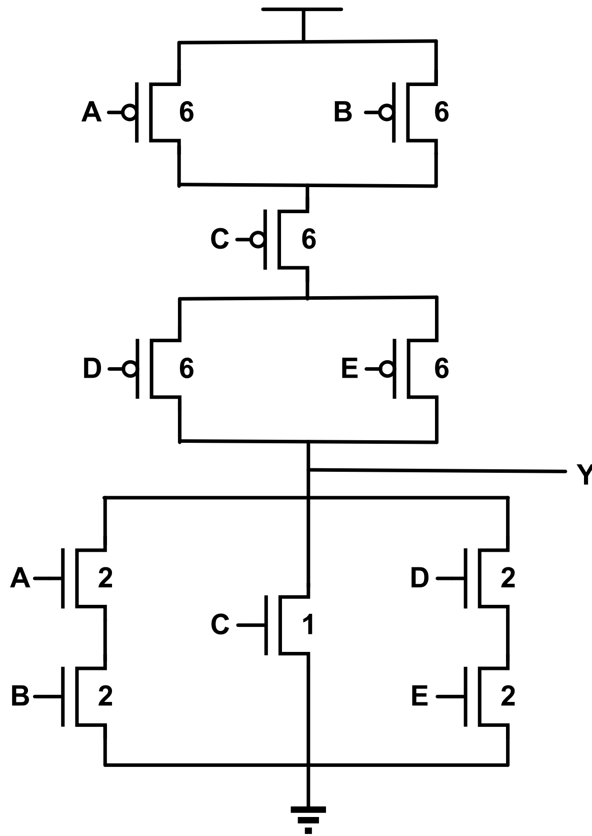
2018 VLSI midterm solution

1.

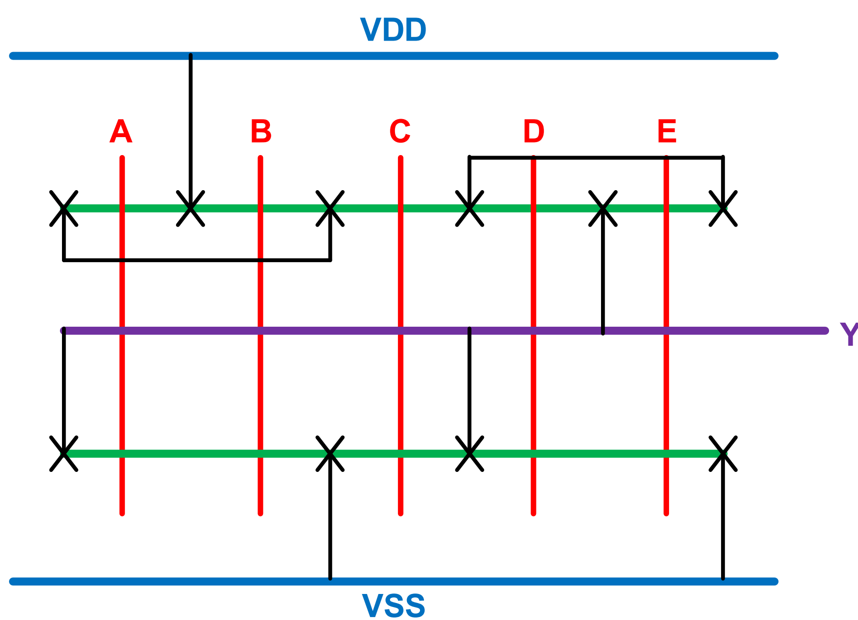
(a)

參考解答:



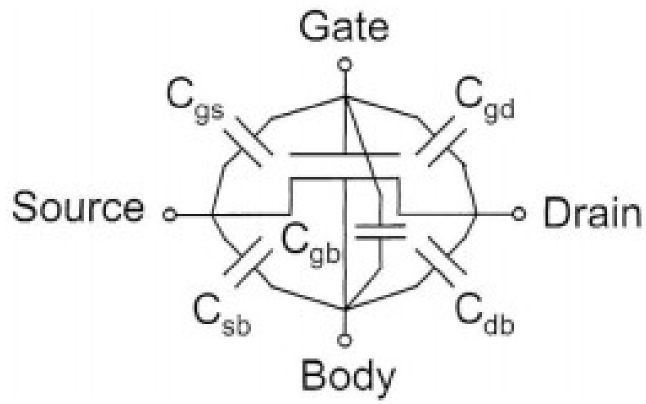
(b)

參考解答: (接線要與(a)小題相符)

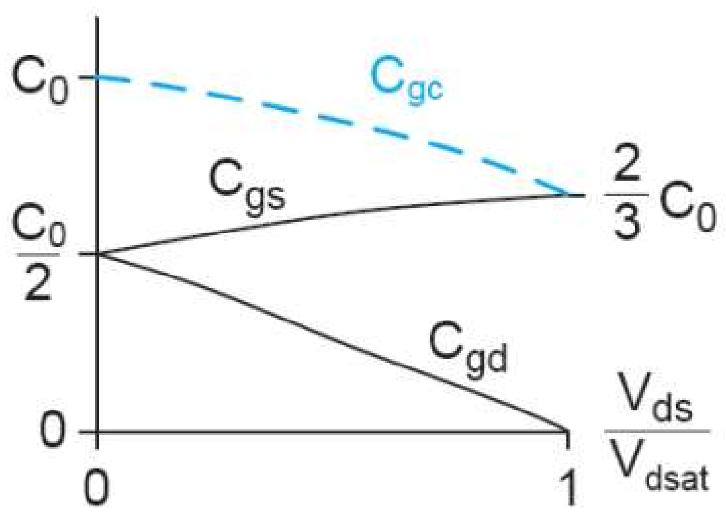


2.

(a)

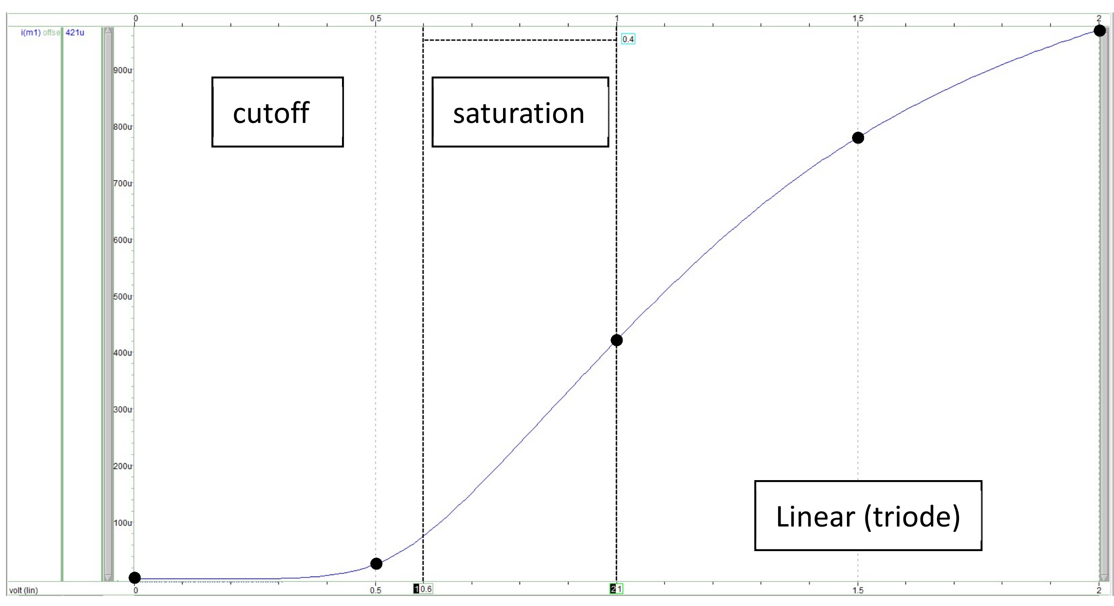


(b)



3.

(a)



(b)

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat}\left(= V_{gs} - V_t\right) & \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat}\left(= V_{gs} - V_t\right) & \text{saturation} \end{cases}$$

4.

(a)

$$D = N\left(\frac{128}{8}\right)^{\frac{1}{N}} + N$$

N	1	2	3	4
F	16	4	2.52	2
D	17	10	10.56	12

N = 2

(b)

$f_i = 4$

D = 10

5.

(a)

$t_{pdr} = (9+4h)RC$

$t_{pdf} = 3C*R/3 + 3C*2R/3 + (9+4h)RC = (12+4h)RC$

$t_{pd} = (t_{pdr} + t_{pdf})/2 = (21/2+4h)RC$

(b)

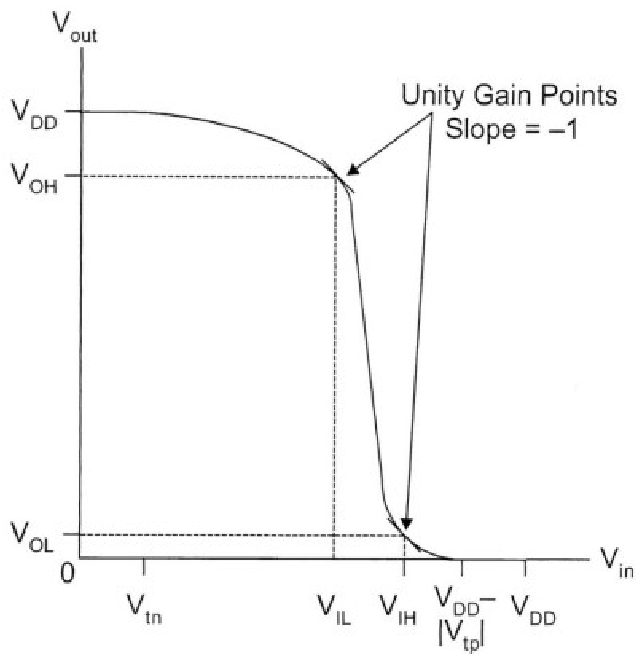
$t_{cdr} = (9+4h)C*R/3 = (3+4h/3)RC$

$t_{cdf} = (9+4h)RC$

$t_{cd} = (t_{cdr} + t_{cdf})/2 = (6+8h/3)RC$

6.

(a)

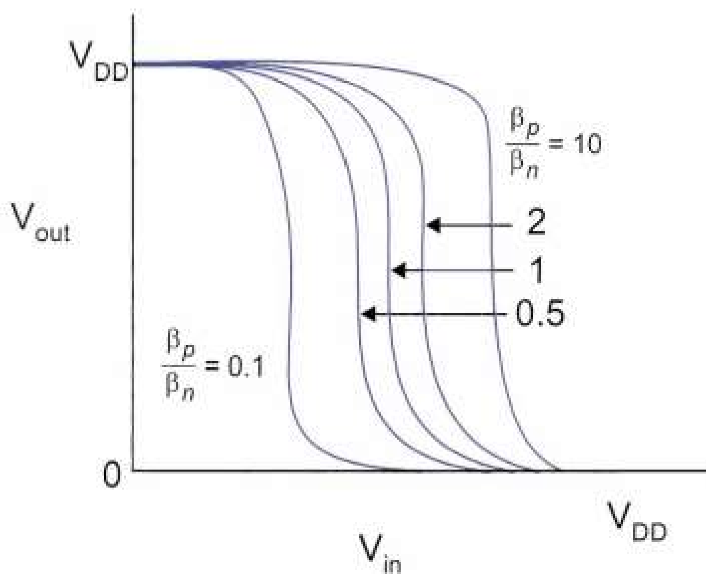


(b)

$NM_H = V_{OH} - V_{IH}$

$NM_L = V_{IL} - V_{OL}$

(c)



$\beta \uparrow 1 \rightarrow V_{IH} \uparrow \rightarrow NM_H \downarrow$

$\rightarrow V_{IL} \uparrow \rightarrow NM_L \uparrow$

$\beta \downarrow 1 \rightarrow V_{IH} \downarrow \rightarrow NM_H \uparrow$

$\rightarrow V_{IL} \downarrow \rightarrow NM_L \downarrow$

(d)

$$W_p / W_n = \mu_n / \mu_p = 4$$

7.

(a)

$$d = gh + p = 1 \times 1 + 1 = 2$$

$$f_{osc} = \frac{1}{2Nd'} = \frac{1}{2 \times 7 \times 2 \cdot 400 \cdot 150f} = 595.24MHz$$

(b) Multiply the length of PMOS and NMOS by $\sqrt{2}$.

8.

(a)

$$G = 1 \times \frac{4}{3} \times \frac{5}{3} \times 1 = \frac{20}{9}$$

$$B = 2 \times 2 = 4$$

$$H = \frac{60}{2} = 30$$

(b)

$$F = GBH = \frac{800}{3}$$

$$N = 4$$

$$P = \frac{3}{3} + \frac{6}{3} + \frac{6}{3} + \frac{3}{3} = 6$$

$$D = NF^{\frac{1}{N}} + P = 22.16$$

(c)

$$\hat{f} = F^{\frac{1}{N}} = 4.04$$

$$C_{in} = \frac{g \times C_{out}}{\hat{f}}$$

$$C_{in,z} = \frac{\frac{3}{3} \times 60}{4.04} = 14.85$$

$$C_{in,y} = \frac{\frac{5}{3} \times 14.85}{4.04} = 6.13$$

$$C_{in,x} = \frac{\frac{4}{3} \times 6.13 \times 2}{4.04} = 4.04$$

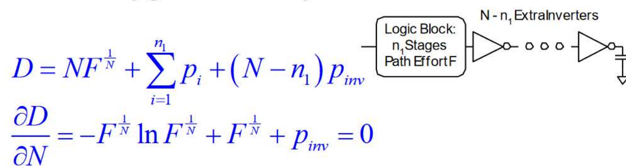
9.

(a)

$$\mathrm{D} = \mathrm{N}F^{\frac{1}{N}} + \sum_{i=1}^{n_1} p_i + (N - n_1)p_{inv}$$

(b)

- Consider adding inverters to end of path
  - How many give least delay?



$$D = NF^{\frac{1}{N}} + \sum_{i=1}^{n_1} p_i + (N - n_1) p_{inv}$$

$$\frac{\partial D}{\partial N} = -F^{\frac{1}{N}} \ln F^{\frac{1}{N}} + F^{\frac{1}{N}} + p_{inv} = 0$$

- Define best stage effort $\rho = F^{\frac{1}{N}}$

$$p_{inv} + \rho(1 - \ln \rho) = 0$$

- $p_{inv} + \rho(1 - \ln \rho) = 0$ has no closed-form solution
- Neglecting parasitics (p_{inv}=0), we define

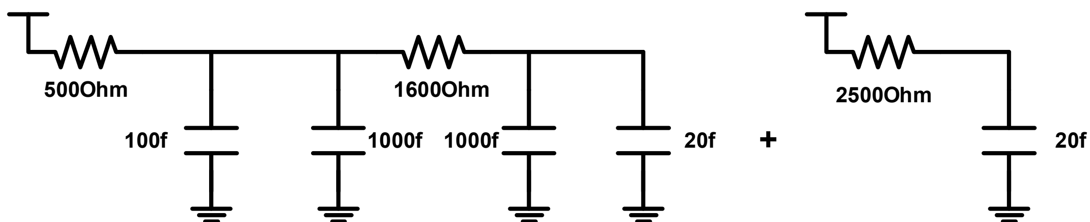
  ρ = 2.718 (e)
- For p_{inv}=1, solve numerically for ρ = 3.59

However, at $\rho = 3.59$, the corresponding number of stage is 5~6. N should be larger than 8. So we take total number of stages N=8, $\rho = 2.593$.

$$\mathrm{D} = 8 \cdot 2048^{\frac{1}{8}} + 8 \times 2 + 0 = 36.749$$

10.

(a)



$$t_{pd} = 500(100f + 1000f) + (500 + 1600)(1000f + 20f) + 2500 \cdot 20f$$
$$= 2.742 \quad (nsec)$$

(b)

$$t_{pd} = 50(1000f + 1000f) + (50 + 1600)(1000f + 20f) + 2500 \cdot 20f$$
$$= 1.833 \ \ (nsec)$$

11.

(a) 講義 2-18: Self-aligned silicide: to reduce the interconnection resistance of gate, source/drain

(b) 講義 2-28: Silicon-On-Insulator: higher speed device, no latch-up

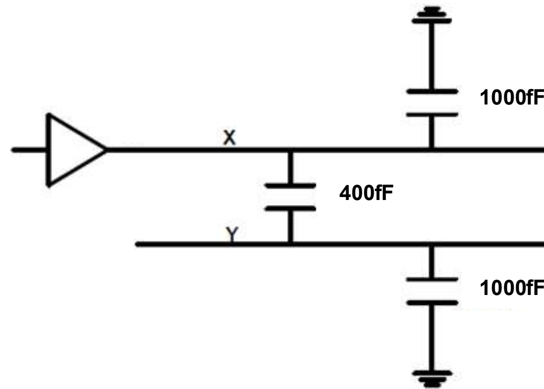
(c) 講義 2-18: Lightly Doped Drain: Reduce electrical field of drain junction & hot-electron damage, High sheet resistance

(d) 講義 2-29: High mobility device by adding a layer of SiGe

(e) 講義 2-16: Effective Oxide Thickness: can be reduced by High-K dielectric to reduce gate leakage

12.

(a)



$$\Delta V_Y = \Delta V_X \times \frac{400f}{1000f + 400f} = -0.714V$$

(b) shielding; increase the loading cap; put two wires away

13.

At 200MHz

$$\mathrm{P} = \alpha \mathrm{C} V^2 f = 0.1 \times (5 \times 10^6) \times (0.8 \times 2 \times 10^{-15}) \times 2.5^2 \times (200 \times 10^6)$$
$$+0.02 \times (45 \times 10^6) \times (0.2 \times 2 \times 10^{-15}) \times 2.5^2 \times (200 \times 10^6) = 1 + 0.45$$
$$= 1.45(W)$$

14. d j l a g b f k i h c e

15.

(a) 講義 3-11: at high Vds ↗, the carrier velocity is not proportional to lateral field. Ids decrease ↘

(b) 講義 4-15: paracitic BJT causing positive feedback, leading to VDD – GND shortage

(c) 講義 3-11: threshold voltage Vt is influence by Vbs (body-tosource voltage)

(d) 講義 2-62: wire attracts charge during plasma processing and builds up voltage

(e) 講義 3-16: when Vgs<Vt, weak inversion causes leakage current at subthreshold region

Drain-Induced Barrier Lowering(DIBL): Vt↘ by positive Vds at subthreshold region

16. F T F F T

F T T T T