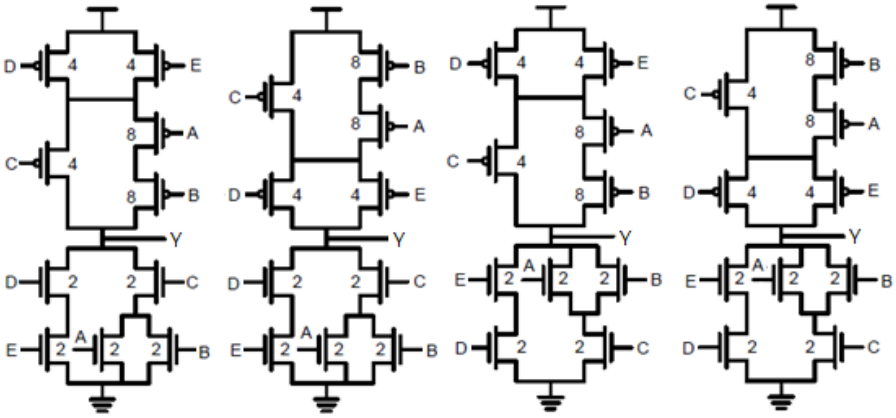
2017 VLSI midterm solution

1.

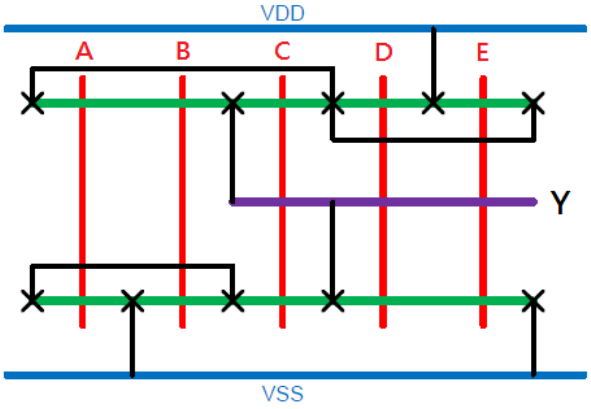
(a)

參考答案：



(b)

參考答案：（可分不同 diffusion，畫對就給分）



2.

(a)

Vout = 1→0.8(V)

(b) (1)Vout = 0.5→1(V)

(2)Vout = X→0.5→1(V)

(1)、(2)皆可

3.

(a)

$$D = N\left(\frac{256}{10}\right)^{\frac{1}{N}} + N$$

N	2	3	4	5	6
F	5.06	2.95	2.25	1.91	1.72
D	12.12	11.84	13.00	14.56	16.30

N = 3

(b)

f_i = 2.95

D = 11.84

4.

(a)

t_{pdf} = (6+4h)RC

t_{pdr} = 4C*R/2 + (6+4h)RC = (8+4h)RC

t_{pd} = (t_{pdf} + t_{pdr})/2 = (7+4h)RC

(b)

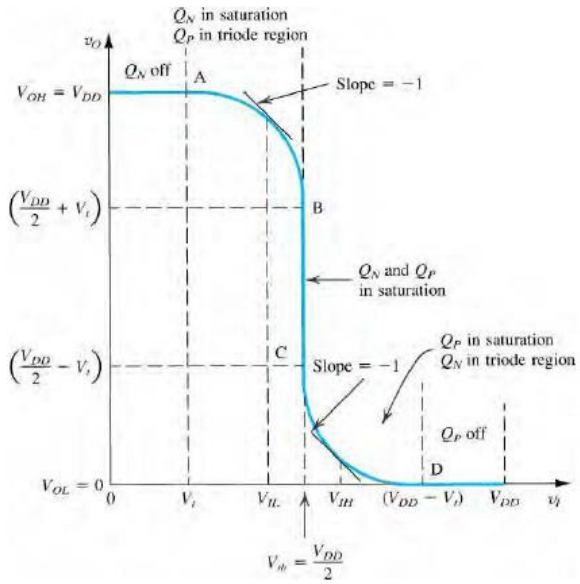
t_{cdf} = (3+2h)RC

t_{cdr} = (6+4h)RC

t_{cd} = (t_{cdf} + t_{cdr})/2 = (9/2+3h)RC

5.

(a)



(b)

$NM_H=V_{OH}-V_{IH}$

$NM_L=V_{IL}-V_{OL}$

(c)

$$W_p/W_n = \mu_n/\mu_p = 3$$

(d)

A>B>C

6.

(a)

$$d = gh + p = 2$$

$$f_{osc} = \frac{1}{2Nd'} = \frac{1}{2 \times 5 \times 2 \cdot 500 \cdot 100f} = 1GHz$$

(b)

Multiply the length of PMOS and NMOS by $\sqrt{2}$.

7.

(a)

$$G = 1 \times \frac{4}{3} \times \frac{5}{3} \times \frac{5}{3} = \frac{100}{27}$$

$$B = 2 \times 2 = 4$$

$$H = \frac{480}{4} = 120$$

(b)

$$F = GBH = \frac{48000}{27}$$

$$N = 4$$

$$P = 1 + 2 + 3 + 2 = 8$$

$$D = NF^{\frac{1}{N}} + P = 33.97$$

(c)

$f = F^{\frac{1}{N}} = 6.49$

$$\text{Cin} = \frac{\text{g} \times \text{Cout}}{\text{f}}$$

$$\text{z} = \frac{\frac{5}{3} \times 480}{6.49} = 123.27$$

$$\rightarrow \quad \text{y} = \frac{\frac{5}{3} \times 123.27}{6.49} = 31.66$$

$$\text{x} = \frac{\frac{4}{3} \times 31.66 \cdot 2}{6.49} = 13$$

8.

(a)

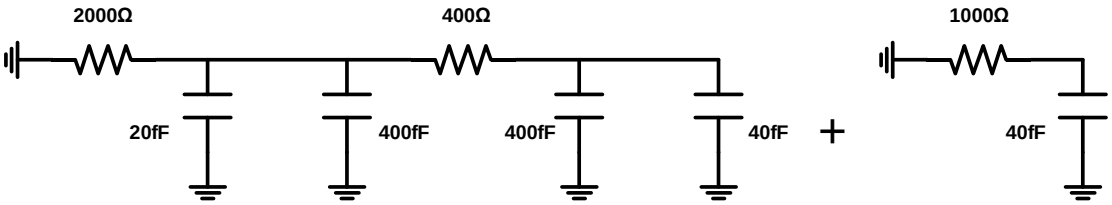
$$\text{D} = NF^{\frac{1}{N}} + \sum_{i=1}^{n1} p_i + (\text{N} - \text{n1})p_{inv}$$

(b)

$$\text{N} = 10 \rightarrow \text{D} = 10 \times \sqrt[10]{1024} + 30 = 50$$

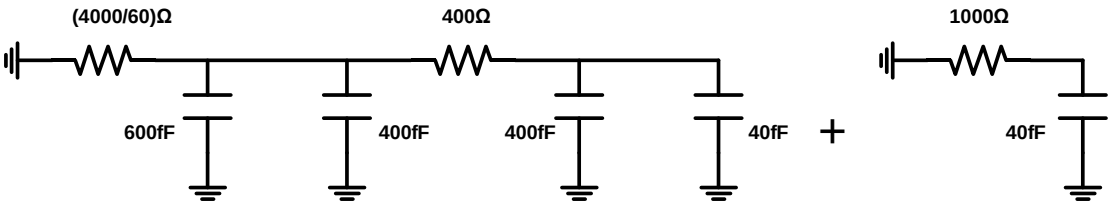
9.

(a)



$$t_{pd} = 2000 \times (20\text{f} + 400\text{f}) + (2000 + 400) \times (400\text{f} + 40\text{f}) + 1000 \times 40\text{f}$$
$$= 1.936\text{ns}$$

(b)



$$t_{pd} = \frac{4000}{60} \times (600\text{f} + 400\text{f}) + \left(\frac{4000}{60} + 400\right) \times (400\text{f} + 40\text{f}) + 1000 \times 40\text{f}$$
$$= 0.312\text{ns}$$

10.

(a) Lightly doped drain: Reduce electrical field of drain junction & hot-electron damage, High sheet resistance

(b) Structure planarization for further stack process.

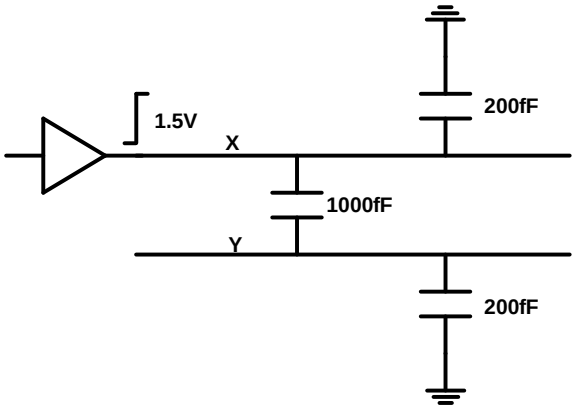
(c) 使用 high-K dielectric 可以降低 EOT，並降低 gate leakage

(d) 可以增加對 Gate 的控制能力，降低 leakage

(e) Shallow Trench Isolation: High density & better isolation, need Chemical Mechanical Polishing (CMP) to planarize the structure

11.

(a)



$$C_{wire} = 2000\mu\text{m} \times 0.1\,{}^{\text{fF}}/_{\mu\text{m}} = 200\text{fF}$$

$$C_{adl} = 2000\mu\text{m} \times 0.5\,{}^{\text{fF}}/_{\mu\text{m}} = 1000\text{fF}$$

$$\Delta V_Y = \frac{1000\text{fF}}{1000\text{fF} + 200\text{fF}} \times 1.5V = 1.25V$$

(b)
Shielding
Increase the loading cap
Put two wire away

12.
(a) Dynamic power (in W/MHz)

$$P = \alpha CV^2 f = [(0.1 \times 20 \times 10^6 \times 5 \times 2) + (0.02 \times 80 \times 10^6 \times 2 \times 2)] \times 1.5^2 \times 10^6 = 59.4\ (\mathrm{mW/MHz})$$

(b) Static power

$$P = I \times V = [(20 \times 10^6 \times 0.05 \times 10^{-9} \times 5) + (80 \times 10^6 \times 1 \times 10^{-9} \times 2)] \times 1.5 = 247.5\ (\mathrm{mW})$$

13.

l → c → i → f → g → j → a → k → d → h → b → e

14.
(a) 講義 2-62: wire attracts charge during plasma processing and builds up voltage
(b) 講義 4-12 : "Electron wind" causes movement of metal atoms along wires
(c) 講義 3-11: at high Vds ↗, depletion of S/D ↗ , effective L↘. Ids increase ↗
(d) 講義 3-11: threshold voltage Vt is influence by Vbs (body-tosource voltage)
(e) 講義 3-11: at high Vgs ↗, the carrier scatter more and mobility decrease. Ids decrease ↘
(f) 講義 4-15: paracitic BJT causes positive feedback leading to VDD – GND short
(g) 講義 4-13: Current through wire resistance generates heat
(h) 講義 4-19: Collisions with particles create electron-hole pairs in substrate
(i) 講義 4-14: Electric fields across channel impart high energies to some carriers
(j) 講義 3-11: at high Vds ↗, the carrier velocity is not proportional to lateral field. Ids decrease ↘

15.
T T T T F
T F T F F