1. Consider a NAND2 as shown in Fig. 1. Assume there are 3 sets of input with (i) A=B=0→1, (ii) A=1, B=0→1, (iii) B=1, A=0→1. **(10%)**
   (a) Link the transition thresholds of i), ii) and (iii) to the curves ①, ②, and ③. (2.5%)
   (b) Explain the root cause of the data-dependent voltage transfer curve. (2.5%)
   (c) Redesign and sketch a symmetric NAND2 to solve the data-dependent issue. (2.5%)
   (d) Redesign and sketch an asymmetric NAND2 to reduce the logical effort of A (g_A) to be 13/12, find g_B. (2.5%)

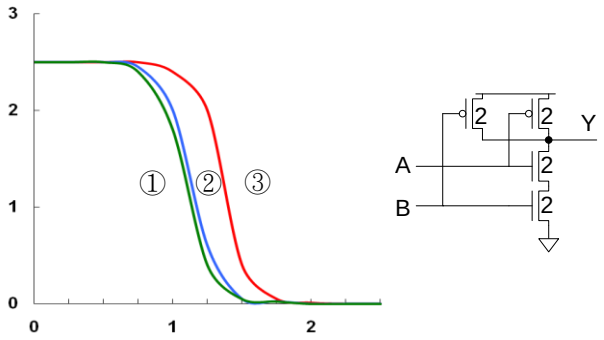

Fig. 1

2. Consider the inverter in Fig. 2 with a mobility ratio of N/P MOSs $\mu_n/\mu_p = 3$. **(5%)**
   (a) Find the best P for best noise margin performance. (2.5%)
   (b) Find the best P for least average delay. (2.5%)

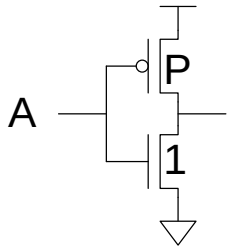

Fig. 2

3. Write down 2 possible issues of dynamic logic and explain. **(5%)**

4. Design a 16-input (k = 16) AND gate using static inverter and footed dynamic NOR gates as shown in Fig. 4. Assume $C_{in}/C_{unit\text{-}inv} = 2$ and the output loading H = 64. **(5%)**
   (a) Find the path delay (from evaluation clock edge to output). (2.5%)
   (b) Sketch and label the transistor widths. (assume precharge pMOS =1) (2.5%)

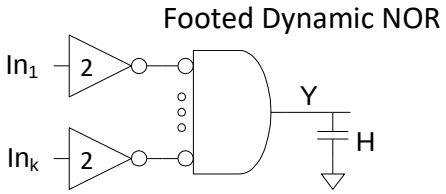

Fig. 4

5. Implement a latch starting from a simple tansmission gate as shown in Fig. 5. Adding the required circuit one-by-one for the following purposes **(10%)**
   (a) Level restoring. (2.5%)
   (b) Static latch. (2.5%)
   (c) Diffusion input. (2.5%)
   (d) Backdriving. (2.5%)

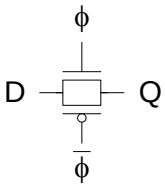

Fig. 5

6. Determine the maximum amount of borrowing time in the following sequencing styles with clock period = 10ns, $t_{setup} = t_{hold} = 2$ns. **(10%)**
   (a) Positive-triggered flip-flops. (2.5%)
   (b) Two-phase transparent latches with 1ns nonoverlap between phases. (2.5%)
   (c) Pulsed latched with 4ns pulse width. (2.5%)
   (d) Repeat (b) and (c) with a clock skew of 1ns. (2.5%)

7. A sequential circuit using flip-flop is shown in Fig. 7. Assume the period of clk T_c = 20ns, max data-to-q delay t_{pdq} = 4ns, min data-to-q delay t_{cdq} = 1.5ns, max clk-to-q delay t_{pcq} = 2ns, min clock-to-q delay t_{ccq} = 0.4ns, setup time = 1.5ns, hold time = 3ns, the clock skew = 0.5ns. **(10%)**
   (a) Find the max delay of combination logic t_{cd}. (2.5%)
   (b) Sketch the timing diagram of Clk, Q1, and D2 with notations for t_{pd} definition. (2.5%)
   (c) Find the min delay of combination logic t_{cd} with and without clock skew. (2.5%)
   (d) Sketch the timing diagram of Clk, Q1, and D2 with notations for t_{cd} definition. (2.5%)

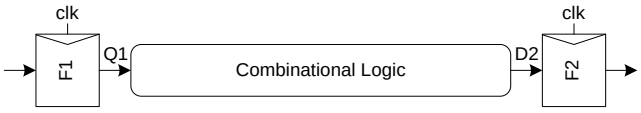

Fig. 7

8. Consider the 6T SRAM cell in Fig. 8. **(10%)**
   (a) Explain the read-disturb behavior (in read operation) and index the cell ratio design concern to overcome it. (2.5%)
   (b) Based on the design concern in (a), explain the pull-up ratio design concern to get a correct write operation. (2.5%)
   (c) Add bit-line conditioning circuit and explain the operation (2.5%)
   (d) Add sense amplifier circuit with isolation transistor and explain the operation. (2.5%)

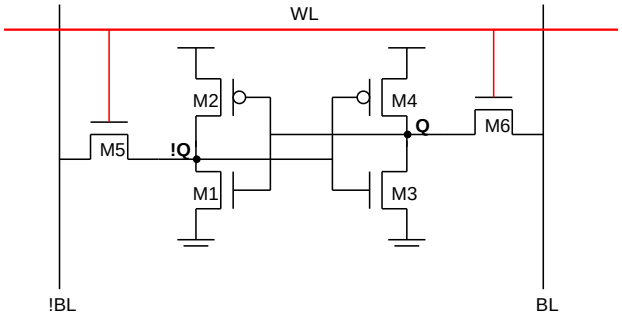

Fig. 8

9. Consider the ET FF as shown in Fig. 9. Explain the relative clock conditions (clk and clk!) to cause the problems (a)~(c). **(10%)**
   (a) Race. (2.5%)
   (b) Undefined state. (2.5%)
   (c) Dynamic storage. (2.5%)
   (d) How to modify the design to guarantee it is hold time issue free? (2.5%)

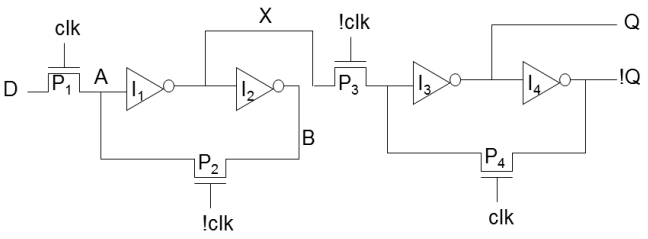

Fig. 9

10. Consider the DRAM cell in Fig. 10, assume the C_{cell} = 5fF and C_{bit} = 100fF. **(10%)**
   (a) Sketch the voltage waveform of "word", "X", and "bit" with stored values of "1" and "0". (2.5%)
   (b) Assume VDD=3.3V, find the ΔV on bit line of reading "1". (2.5%)
   (c) Explain the pros and cons of "open bitline" architecture. (2.5%)
   (d) Explain the pros and cons of "folded bitline" architecture. (2.5%)

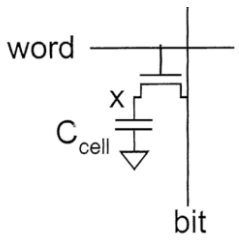

Fig. 10

11. To implement an adder for two 9-bit words. Assume t_{pg} = delay of 1-bit PG (propagate and generate) gate, t_{AO} = delay of AND-OR gate, t_{XOR} = delay of XOR gate **(10%)**
   (a) Sketch the carry-ripple adder using PG logics. (2.5%)

(b) Express the delay t_{ripple} in terms of t_{pg}, t_{AO}, and t_{XOR}. (2.5%)

(c) Sketch the block diagram of Carry-Skip adder with a 3-bit grouping. (2.5%)

(d) Express the delay tskip in terms of tpg, tAO, and tXOR. (2.5%)

12. Fig. 12 shows a PLA (programmable Logic Array) for your reference. **(5%)**

(a) Design and sketch a new PLA to implement $x = \bar{a}bc + \bar{b}\bar{c} + abc + a\bar{c}$ and $y = \bar{a}\bar{b}c + +ac + b\bar{c}$ (2.5%)

(b) Use ROM to implement the logic in (a), sketch the decoder and dot array. (2.5%)

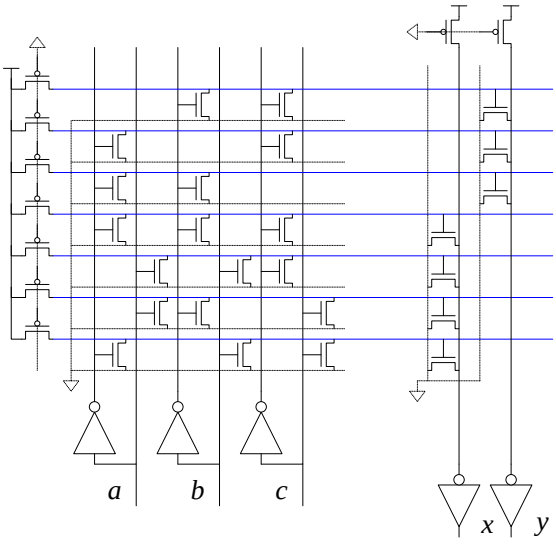

Fig. 12

13. Design a logic path in Fig. 13. **(5%)**

(a) Find the path parameters G, B, H. (1%)

(b) Find the minimum path delay. (2%)

(c) Find the size of the x, y, z to get the minimum path delay. (2%)

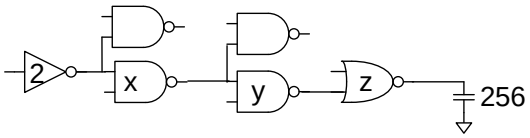

Fig. 13

14. Estimate the delay of a 10x unit inverter driving a 2x unit inverter at the end of the 4mm wire implemented in metal2 with 0.4um wide, $R_{\square}$ = 0.06Ω/□, and C_{wire} = 0.2 fF/μm. Assume the effective turn-on resistance of 1x unit inverter = 5kΩ, the C_{in} and $C_{parasitic}$ of 1x unit inverter all equal to 4fF. **(5%)**

(a) Find the t_{pd} with 1-segment pi-model. (2.5%)

(b) Find the t_{pd} with 100x unit inverter as a driver. (2.5%)

15. Answer the following questions. (T or F) **(10%)**

(a) Shmoo plots is a diagnose methodology by varying the operation supply and bias. (1%)

(b) *Linear feedback shift register* is used to generate a pseudo random code. (1%)

(c) Redundancy and error correction are implemented to improve the operation performance of memory. (1%)

(d) Clock jitter is due to the low frequency environment variation. (1%)

(e) *Drift* clock skew is due to process variation and can be solved by calibration. (1%)

(f) *H-Tree* type clock distribution is suffered at systematic skew between points closet and furthest to the driver. (1%)

(g) *Grid* type clock distribution is suffered at delay mismatch of local near points from different tree. (1%)

(h) *Design for test* = design circuit to increase fault coverage. (1%)

(i) Good test pattern means a good production yield. (1%)

(j) FIFO needs two pointers; and LIFO needs only one pointer instead. (1%)