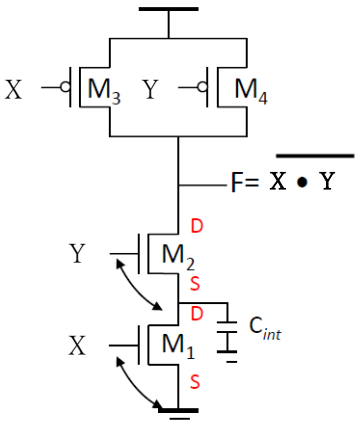
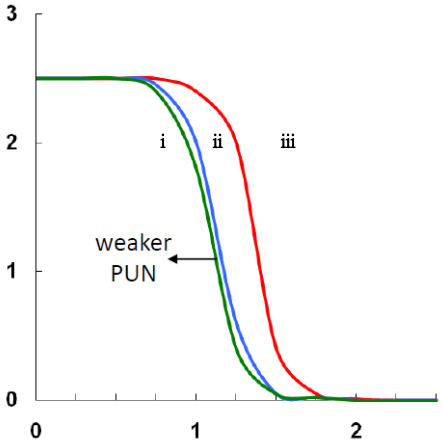
1.

(a)





(b)

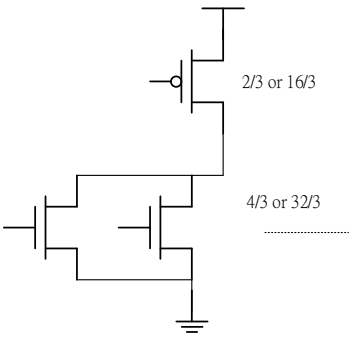
The threshold voltage of M2 is higher than M1 due to body effect

2.

(a)

D=50.2223

(b)

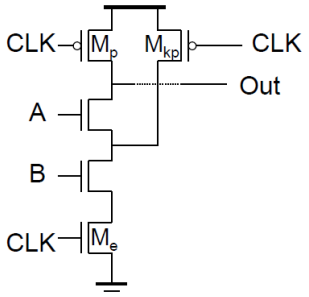


3.

(a)

$$V_{OUT} = \frac{40}{10 + 40} = 0.8$$

(b) precharge internal node



4.

(a) “Electron wind” causes movement of metal atoms along wires. Excessive electromigration leads to open circuits.

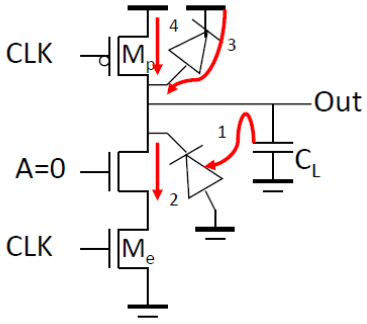
(b) Current through wire resistance generates heat.Self-heating limits AC current densities for reliability

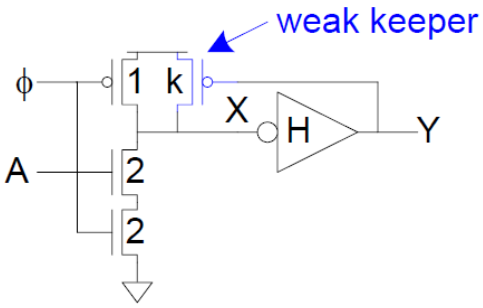
(c) Electric fields across channel impart high energies to some carriers.

(d) The inadvertent creation of a low-impedance path between the power supply rails of a MOSFET circuit, triggering a parasitic structure which disrupts proper functioning of the part, possibly even leading to its destruction due to overcurrent.

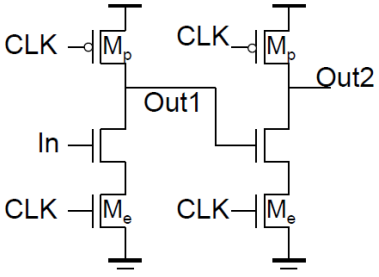
5.

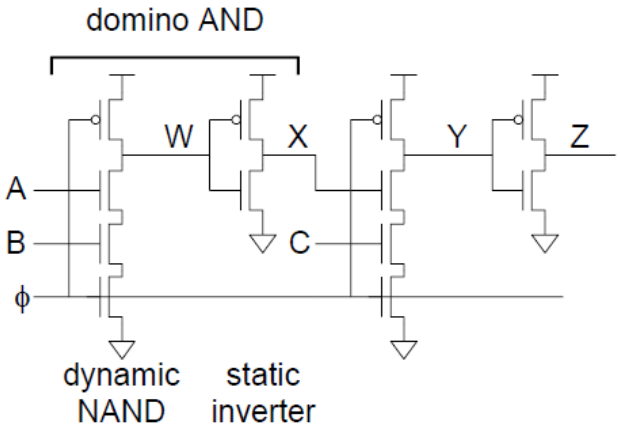
(a)Dynamic node floats high during evaluation





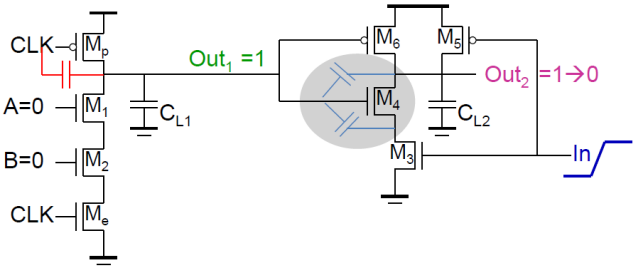
(b) Only a single 0 -> 1 transition allowed at the inputs during the evaluation period!





(c) Susceptible to crosstalk due to 1) high impedance of the output node and 2) backgate capacitive coupling

–Out2 capacitively couples with Out1 through the gate-source and gate-drain capacitances of M4



Dynamic NAND Static NAND

Add buffer at internal.

(d) Coupling between Out and CLK input of the precharge device due to the gate-drain capacitance. So voltage of Out can rise above VDD. The fast rising (and falling edges) of the clock couple to Out.

Solution: add loading at output.

6.

(a)

Max delay $\mathrm{T_{pd}} \leq \mathrm{T_c} - \max(\mathrm{t}_{pdq}, \mathrm{t}_{pcq} + \mathrm{T_{setup}} - \mathrm{t}_{pw} + t_{skew}) = 14\mathrm{n}$

(b)

Without skew:

$$\mathrm{t}_{cd} \geq T_{hold} - t_{ccq} + t_{pw} = 3.2n$$

With skew:

$3.7n$

7.

(a) no time borrowing

(b)7n

(c)3n

(d)2 phase:6.5n,pulse latch:2.5n

8.

(a)9ns

(b)5ns

(c)2.5n

(d)non-overlap 2 phase clk

9.

(a) 參見講義 Chapter 7-32 頁

(b) 參見講義 Chapter 7-36 頁

(c) 參見講義 Chapter 7-28 頁

(d) Speed : (b)>(a)>(c)

10.

(a)F

(b)F

(c)F

(d)T

(e)T

(f)T

(g)T

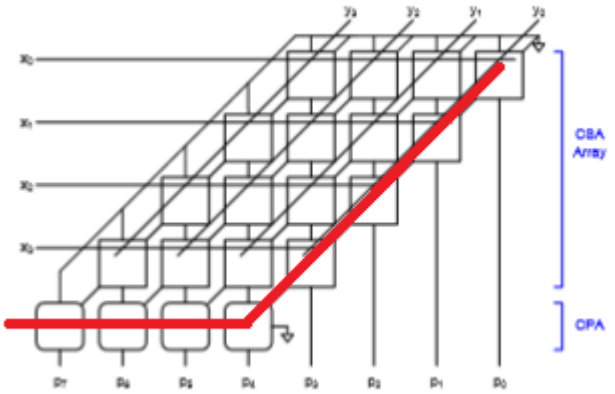
(h)

True→ Arithmetic Shifter: Rt shift sign extends

False→ Barrel Shifter: Shifts number left or right and fills with lost bits

(i)F

(j)



11.

(a)M1&M3 > M5&M6 (參見講義 Chapter 8-8 頁)

(b)M5&M6 > M2&M4(參見講義 Chapter 8-9 頁)

12.

(a)Read 0 : $\frac{C_{cell}\times 0+C_{bl}\times\frac{V_{DD}}{2}}{C_{cell}+C_{bl}}=\frac{50f\times 0+1p\times 1.65}{50f+1p}=1.57\text{V}$

Read 1 : $\frac{C_{cell}\times V_{DD}+C_{bl}\times\frac{V_{DD}}{2}}{C_{cell}+C_{bl}}=\frac{50f\times 0+1p\times 1.65}{50f+1p}=1.73\text{V}$

(b)to select column or reduce column circuits area.

(c)

Sense amplifier: It's invented to provide faster sensing by responding to a small voltage swing.

Isolation transistors: To Cut off large bitline capacitance when sense amplifier works.

(d)

(1)redundancy cell.

(2)ECC.

(3)built-in self-test (BIST)

(e)x=a$\bar{b}\bar{c}$+$\bar{a}b\bar{c}$+$\bar{a}\bar{b}$c+abc

y=ab+ac+bc

13.

(a) Open bitlines: use another subarray as reference

–Higher density

–Noise affect one array more than the other appears as differential noise.

(b) Folded bitlines: take the neighbor cell in the same subarray as reference

–Noise appears as common mode

–Larger layout area

14.

(a)F

(b)F

(c)T

(d)T

(e)F

(f)T

(g)F

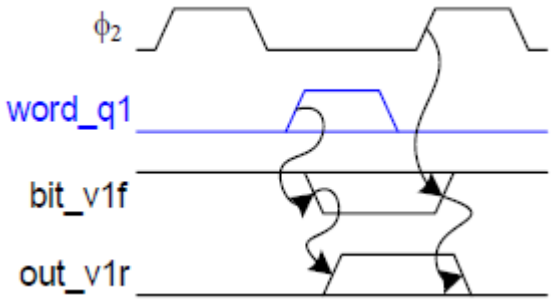
(h)T

(i)F

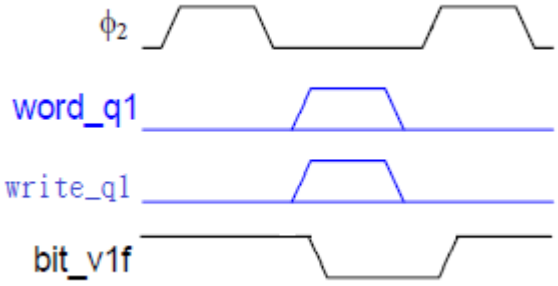
(j)F

15.

(a)



(b) If data_s1=1



16.

(a) F=GBH = $(1\times\frac{4}{3}\times\frac{5}{3}\times\frac{5}{3})$ (2×2) $(\frac{256}{1})=\frac{102400}{27}$

N=4，P=1+2+3+2=8

D=N$F^{\frac{1}{N}}$ +P=39.39

(b)f= $(\frac{102400}{27})^{\frac{1}{4}}$ =7.848，$C_{in}=\frac{g\times C_{out}}{f}$

$$\rightarrow\begin{cases} z=\frac{\frac{5}{3}\times256}{7.848}=54.366 \\ y=\frac{\frac{5}{3}\times54.37}{7.848}=11.546 \\ x=\frac{\frac{4}{3}\times2\times11.546}{7.848}=3.922 \end{cases}$$

17.

(a) D=N$F^{\frac{1}{N}}$ +N= D=N$(\frac{512}{1})^{\frac{1}{N}}$ +N=N$(512)^{\frac{1}{N}}$ +N

N	1	2	3	4	5	6	7
D	513	47.255	27	23.027	22.411	22.971	24.066

Ans.: N=5

(b)

$f=512^{\frac{1}{5}}=3.482$，$D=22.411$