1. Consider a NAND2 logic $F = \overline{X \bullet Y}$ with Y as the inner input. **(5%)**
   (a) Find the transition-threshold ordering of the following cases: (i) X, Y: 0→1, (ii) X = 1, Y: 0→1, (iii) Y = 1, X: 0→1. (2.5%)
   (b) Explain the root cause of the data-dependent voltage transfer curve. (2.5%)

2. Design a 32-input (k = 32) AND gate using inverter and pseudo-nMOS NOR gates as shown in Fig. 2. Choose pull-up device size to be 2/3 and the output loading H = 128. **(5%)**
   (a) Find the path delay. (2.5%)
   (b) Sketch and label the transistor widths. (2.5%)

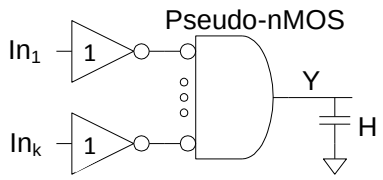

Fig. 2

3. Consider a dynamic logic (NADN2) as shown in Fig. 3. Assume the $C_a = C_b = 10fF$, $C_L = 40fF$, $C_{gs}(C_{gd})$ of $M_p = 5fF$, and $V_{DD} = 1V$. **(5%)**
   (a) In precharge, assume all the charge on C_a and C_b are 0. Find the voltage V_{out} in evaluation with B = 0, A = 0→1. (2.5%)
   (b) Provide an add-on circuit to solve the issue in (a). (2.5%)

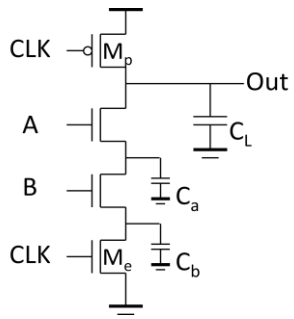

Fig. 3

4. Explain the mechanism of the following reliability issues. **(10%)**
   (a) Electromigration. (2.5%)
   (b) Self-heating. (2.5%)
   (c) Hot carrier. (2.5%)
   (d) Latchup. (2.5%)

5. Explain the following issues and solution of dynamic logic. **(10%)**
   (a) Leakage. (2.5%)
   (b) Cascading gates. (2.5%)
   (c) Backgate coupling. (2.5%)
   (d) Clock feedthrough. (2.5%)

6. A sequential circuit using pulse latch is shown in Fig. 6. Assume the period of clk = 20ns, max data-to-q delay t_{pdq} = 6ns, min data-to-q delay t_{cdq} = 4ns, max clk-to-q delay t_{pcq} = 5ns, min clock-to-q delay t_{ccq} = 3ns, setup time = 2.4ns, hold time = 4.2ns, the clock skew = 0.5ns. **(5%)**
   (a) With pulse width t_{pw} = 2ns, find the max delay of combination logic t_{pd}. (2.5%)
   (b) Find the min delay of combination logic t_{cd} with and without clock skew. (2.5%)

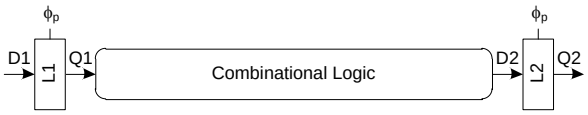

Fig. 6

7. Determine the maximum amount of borrowing time in the following sequencing styles with clock period = 20ns, $t_{setup} = t_{hold}$ = 2ns. **(10%)**
   (a) Positive-triggered Flip-flops. (2.5%)
   (b) Two-phase transparent latches with 1ns nonoverlap between phases. (2.5%)
   (c) Pulsed latched with 5ns pulse width. (2.5%)
   (d) Repeat (b) and (c) with a clock skew of 0.5ns. (2.5%)

8. Consider the MUX type ET FF in Fig. 8. Assume the propagation delays of $I_{1\sim6}$ =2ns and $T_{1\sim4}$ = 3ns respectively. The delay between clk and !clk is 2.5ns. **(5%)**
   (a) Find the setup time. (2.5%)
   (b) Find the t_{pcq}. (2.5%)
   (c) Find the hold time. (2.5%)
   (d) How to modify the design to guarantee it is hold time issue free? (2.5%)

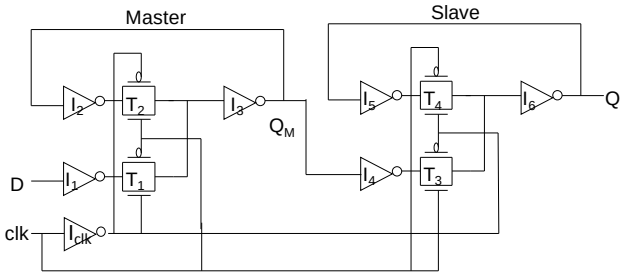

Fig. 8

9. Using two 9-bit words input with a 3-bit grouping as an example, sketch and explain the operation of the following types of adder. **(10%)**
   (a) Carry-Lookahead. (2.5%)
   (b) Carry-Select. (2.5%)
   (c) Carry-Skip. (2.5%)
   (d) Order these adders in term of speed. (2.5%)

10. Answer the following questions about Datapath Subsystems. (T or F) **(10%)**
   (a) *One-zero detection* is used to check the magnitude equality of two inputs. (1%)
   (b) Logic levels, fan-in and grouping are the 3 design-tradeoff corner parameters of tree adder. (1%)
   (c) *Parity check* is commonly used to do the data error-detection and correction.
   (d) *Linear feedback shift register* is used to generate pseudo random code. (1%)
   (e) The critical path of a multi-bit adder is usually the carry propagation. (1%)
   (f) *Booth encoding* is used to solve the x3 operation in multi-bit multiplier. (1%)
   (g) *Gray code* is used to reduce dynamic power and glitch of decoder. (1%)
   (h) If we shift "Right" a word 1011 to get 1101, it is an Arithmetic shifter operation. (1%)
   (i) M×N-bit multiplication will produce M N-bit partial products. (1%)
   (j) If carry generation is the slowest path in the CSA cell in Fig. 10. Identify the critical path of this multiplier. (1%)

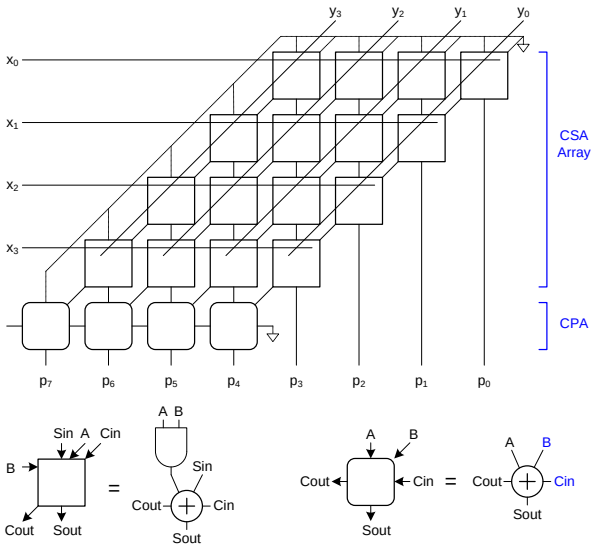

Fig. 10

11. Consider the 6T SRAM cell in Fig. 11. **(5%)**
   (a) Explain the transistor sizing requirement for read stability. (2.5%)
   (b) Explain the transistor sizing requirement for write stability. (2.5%)

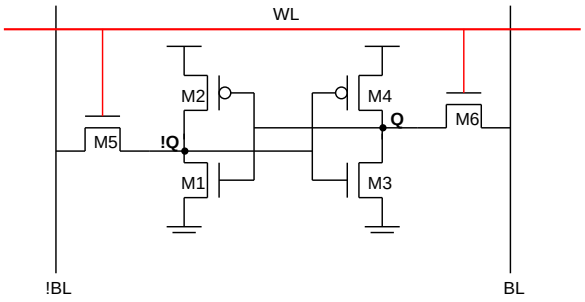

Fig. 11

12. Answer the following about Memory: **(10%)**
    (a) For a 1T DRAM cell, assume the bit line is precharged to $V_{DD}/2$, the cell capacitance is 50fF, and the bit line capacitance is 1pF. Find the data 0 and 1 voltage level on bit line during readout with V_{DD} = 3.3V. (2%)
    (b) Explain the purpose of "column multiplexing". (2%)
    (c) Explain the purpose of sense amplifier and isolation transistor. (2%)
    (d) Write down two common methods to improve the yield of memory. (2%)
    (e) Write the Boolean function of x, y in Fig. 12. (2%)

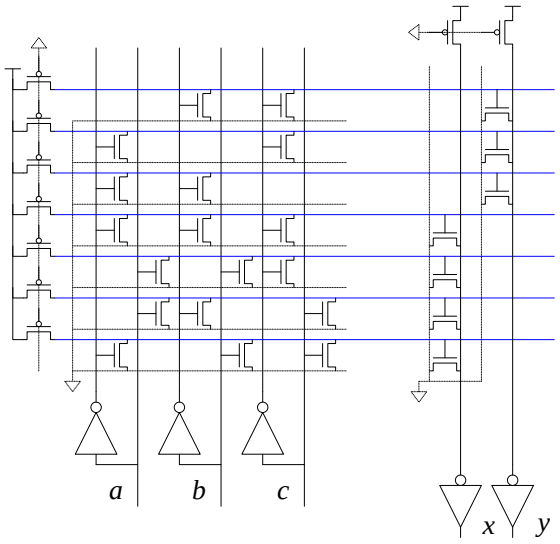

Fig. 12

13. Explain the implementation, pros, and cons of the following bitline design of DRAM. **(5%)**
    (a) *Open bitline*. (2.5%)
    (b) *Folded bitline* (2.5%)

14. Answer the following questions. (T or F) **(10%)**
    (a) *Drift* clock skew is due to process variation and can be solved by one-time calibration. (1%)
    (b) *Random* skew is caused by time-dependent environmental variations. (1%)
    (c) H-Tree type clock distribution is suffered at random skew between points closet and furthest to the driver. (1%)
    (d) JTAG is development for components test on PCB to verify solder joints. (1%)
    (e) Electron-beam (ebeam), u-Probe, and Focused Ion Beam (FIB) are all debugging methods without mechanical contacts. (1%)
    (f) DRAM is not compatible to standard CMOS process technology due to special capacitor structure. (1%)
    (g) Fault coverage is a measure of manufacturing yield. (1%)
    (h) The RLC effect of I/O pads will affect the power quality and signal settling behavior as well. (1%)
    (i) Schmitt trigger is used to filter out the noise of output pin. (1%)
    (j) Bypassing capacitors are used to stabilize voltage and normally implemented with identical capacitances in parallel. (1%)

15. Sketch the timing diagrams of ϕ_1, ϕ_2, word_q1, birt_v1f, and out_v1r to explain the SRAM operations in Fig. 15. **(5%)**
    (a) Read operation. (2.5%)
    (b) Write operation. (2.5%)

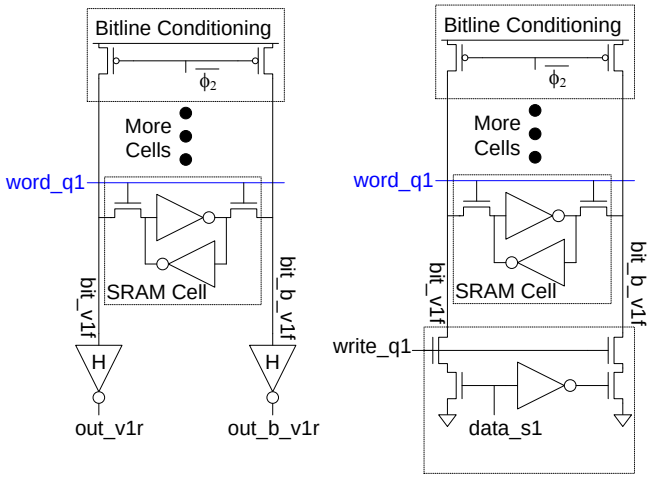

Fig. 15

16. A logic path as shown in Fig. 16. **(5%)**
    (a) Find the minimum path delay. (2.5%)
    (b) Find the size of the x, y, z to get the minimum path delay. (2.5%)

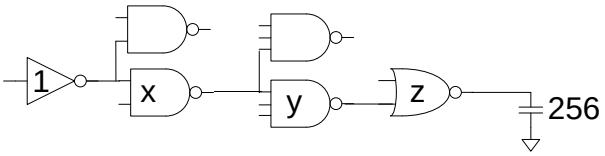

Fig. 16

17. Design a tapered buffer to drive a 512-unit loading (relative to C_{in} of unit inverter) as shown in Fig. 17. **(5%)**
    (a) Design stage number N to get the minimum delay. (2.5%)
    (b) With the N in (a), find the stage effort delay f_i and the total path delay D. (2.5%)

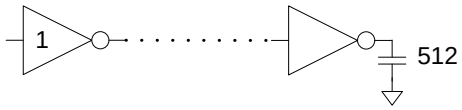

Fig. 17