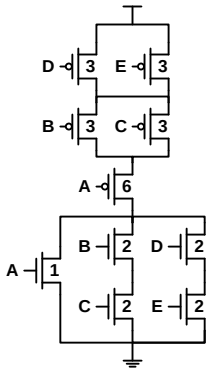
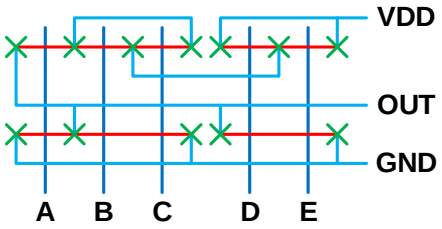
1. (a)



有多種答案，畫對任一種都算對，不用標示 size

(b) $g_a=\frac{6+1}{3}=\frac{7}{3}$ $g_c=\frac{3+2}{3}=\frac{5}{3}$ $g_d=\frac{3+2}{3}=\frac{5}{3}$

(c)



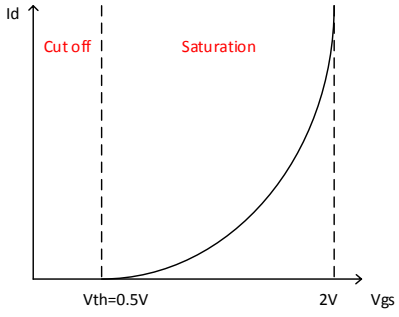
有多種答案，畫對任一種都算對，並要正確標示 A~E,VDD,GND,Y(out)
若需使用到 metal2 則需明顯標示。

(d) (2.5%) (no partial)

$$P_{max}=\frac{6+6+2+2+1}{3}=\frac{17}{3}$$

$$P_{min}=\frac{6+2+2+1}{3}=\frac{11}{3}$$

2. (a)

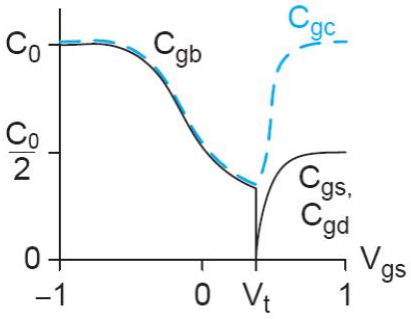


(b) at saturation: $I_D=\frac{1}{2}u_nC_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2$

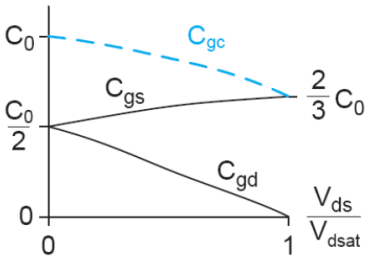
at linear： $I_D=\frac{1}{2}u_nC_{ox}\frac{W}{L}(2(V_{GS}-V_{TH})V_{DS}-{V_{DS}}^2)$

at cut off： $I_D=0$

3. (a)



(b)



4. **(a)** d=gh+p=2

$d' = d \times R \times C = 2 \times 5k \times 10f$

$$f_{osc} = \frac{1}{2Nd'} = \frac{1}{2 \times 5 \times 2 \times 5k \times 10f} = 1.0\text{GHz or } 10^9 Hz$$

(b) Unit inverter g_{avg}=1

Skewed inverter g_{avg} =1

$$f_{osc} = \frac{1}{2Nd'} = \frac{1}{5 \times 2 \times 5k \times 10f} = 1.0\text{GHz or } 10^9\text{Hz}$$

5. (a) 當 V_{DS} 電壓上升，Drain 端空乏區變大，使得有效 Channel length 縮短，讓 I_{DS} 上升。

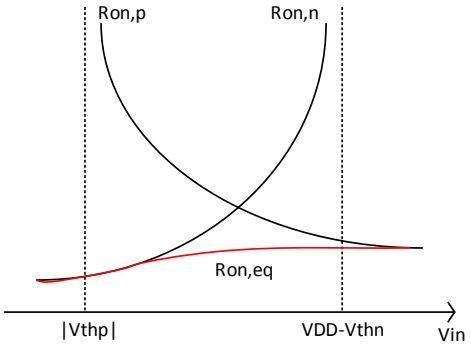
(b) 因半導體中 Carrier 有其最大速度極限，使得當 V_{DS} 增加時，其速度並不會正比於電場大小，此時可以稱之為 Velocity Saturation，也造成 I_{DS} 因此達到飽和。

(c) CMOS 具有寄生 BJT 與阻值，當電流流經 Substrate 使得寄生 BJT 間產生正回授 Loop 造成 VDD-GND 的大電流產生。

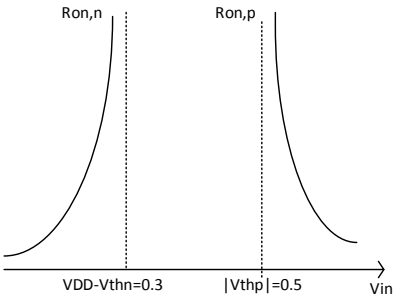
(d) 當 Body 與 Source 電壓不一致時，造成 Threshold 電壓改變。

(e) 當 Channel 電場過大，在 Carrier 上產生高能量，並撞擊矽原子產生電子電洞對，產生漏電流。

6. (a)



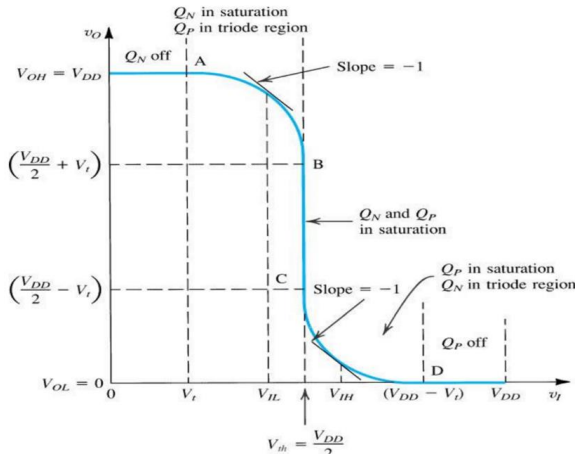
(b)



Ron 在小於 0.3V 與大於 0.5V 時，會隨著 vin 變動而有巨幅改變，在 0.3V~0.5V 時，MOS turn off ，為 high impedance

7. (a) (W/L)p = (6um/0.18um)

(b)



(c) NM_H = VOH-VIH

NM_L = VIL – VOL

(d) NM_H C>B>A

NM_L A>B>C

8. **(a)** $D = NF^{\frac{1}{N}} + \sum_{i=1}^{n1} Pi + (N-n_1)P_{inv}$

(b) Pinv+ρ(1−lnρ)=0, Pinv=1, ρ=3.59

D = (10×3.59) + (4×3) + (6×1) = 53.9

9. **(a)** if N=3, f=6.35, D=3×6.35+3=22.05

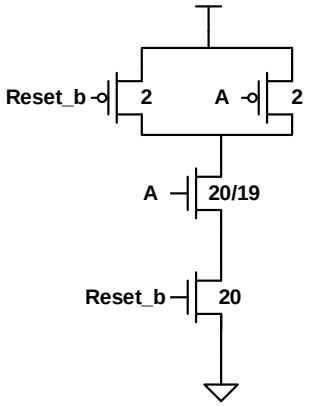
if N=4, f=4, D=4×4+4=20

if N=5, f=3.03, D=5×3.03+5=20.16

N=4 has the minimum delay

(b) f=4, D=4×4+4=20

10.



(a) Pull down path: resistance = $1 - \frac{1}{20} = \frac{19}{20}$; size_A = $\frac{20}{19}$

Pull up path unchanged: sizes = 2

(b) $g_A = \frac{2+\frac{20}{19}}{3} = \frac{58}{57}, g_B = \frac{2+20}{3} = \frac{22}{3}$

11.

C_{wire} = 500fF

C_{adj} = 200fF

R_{wire}= 0.6x (1mm/0.5um) = 1.2K

(a) C_{eff} = 200*2+500 = 900fF

0.5k x (50f+450f)+ (0.5k+1.2k) x 450f = 1.015ns

(b) C_{eff} = 200*1+500 = 700fF

0.5k x (50f+350f) + (0.5k+1.2k)x350f = 795ps

(c) ΔV_Y = 1.8x (200f/700f)= 0.514V

(d) Shielding , Increase the loading Cap , Put two wire away

12. **(a)** $H = \frac{300}{3} = 100$

$$F = GBH = \left(1 \times \frac{4}{3} \times \frac{5}{3} \times \frac{5}{3}\right)(2 \times 2)\left(\frac{300}{3}\right) = \frac{40000}{27}$$

$$N = 4, \qquad P = 1 + 2 + 3 + 2 = 8$$

$$D = NF^{\frac{1}{N}} + P = 32.82$$

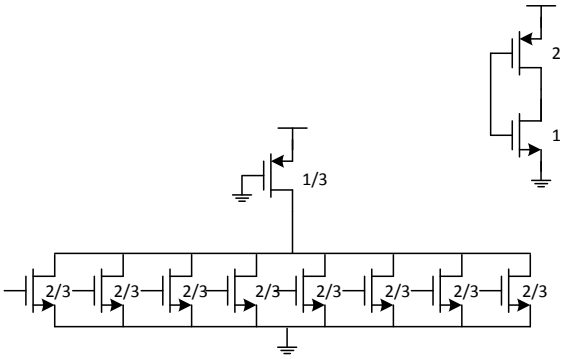
(b) $f = \left(\frac{40000}{27}\right)^{\frac{1}{4}} = 6.204$

$$Cin = \frac{g \times Cout}{f}$$

$$\Rightarrow \begin{cases} z = \dfrac{5/3 \times 300}{6.204} = 80.59 \\ y = \dfrac{5/3 \times 80.59}{6.204} = 21.65 \\ x = \dfrac{4/3 \times 21.65 \times 2}{6.204} = 9.305 \end{cases}$$

13.

(a)



$$gu = \frac{2}{3}, gd = \frac{2}{9}, g_{avg} = \frac{4}{9}$$

$$pu = \frac{17}{3}, pd = \frac{17}{9}, p_{avg} = \frac{34}{9}$$

$$G = 1 \times \frac{4}{9} = \frac{4}{9}$$

$$H = \frac{64}{1} = 64$$

$$F = GBH = \frac{4}{9} \times 1 \times 64 = \frac{256}{9}$$

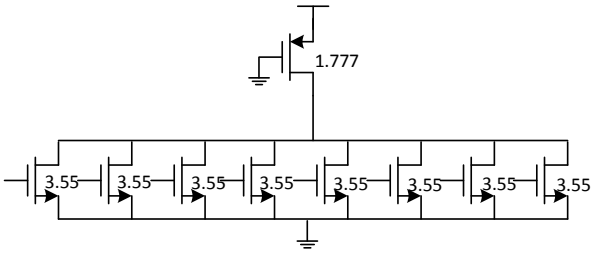
$$D = NF^{\frac{1}{N}} + P = 2 \times \sqrt{\frac{256}{9}} + \frac{34}{9} = 35.777$$

(b) $f = \sqrt{\frac{256}{9}} = \frac{16}{3}$

$$x = \frac{C_{out} \times g_{in}}{f} = \frac{64 \times \frac{4}{9}}{\frac{16}{3}} = 5.3333$$

$$\text{PMOS: } 5.333 \times \frac{\frac{1}{3}}{\frac{1}{3}+\frac{2}{3}} = 1.7777$$

$$\text{NMOS: } 5.333 \times \frac{\frac{2}{3}}{\frac{1}{3}+\frac{2}{3}} = 3.5555$$



14.

Sizing:

MNOS=> 3 unit

PMOS=> 2 unit

(a)

T_{pdr} = (9+5h)RC

T_{pdf} = (3C*R/3)+(3C*2R/3)+R*(9+5h)C = (12+5h)RC

T_{pd} = (10.5+5h)RC

(b)

T_{cdr} = R/3 *(9+5h)C = (9+5h)RC/3

T_{cdf} = (9+5h)RC

T_{cd} = (18+10h)RC/3

15.

(a) 使用 high-K dielectric 可以降低 EOT，並降低 gate leakage

(b) 使用 low-K dielectric 可以降低導線寄生電容

(c) 增加導電度，降低阻值

(d) 可以增加對 Gate 的控制能力，降低 leakage

(e) High speed & 避免 Latch up 產生

16. FTTFT TTTFT