1. Consider the design of a CMOS compound gate computing $F = \overline{A+(B \bullet C)+(D \bullet E)}$. **(10%)**
   (a) Sketch transistor-level schematic. (2.5%)
   (b) Find g_A, g_C, g_D. (2.5%)
   (c) Sketch the stick diagram. (2.5%)
   (d) Find the maximum and minimum p with different layout style. (2.5%)

2. For DC characteristic of nMOS with V_{tn}=0.5V **(5%)**
   (a) Sketch the I-V curves at V_{GS} = 0~2V and identify the operation regions. (2.5%)
   (b) Write down the corresponding ideal I-V equations. (2.5%)

3. Assume an nMOS with V_{tn} = 0.5V and C_0 = C_{ox}WL. **(5%)**
   (a) Sketch the gate capacitance (Cgd, Cgs, Cgb) in terms of C_0 @ Vds = 1V for Vgs = -1V~1V. (2.5%)
   (b) Sketch the gate capacitance (Cgd, Cgs) in terms of C_0 for Vds/Vdsat = 0~1. (2.5%)

4. A ring oscillator composed of N-stages identical inverters is as shown in Fig. 4. Assume the effective resistance of an unit inverter (P:2, N:1) is 5kΩ and parasitic capacitance is 10fF. **(5%)**
   (a) N = 5, find the oscillated frequency. (2.5%)
   (b) Use skewed inverter and find the oscillated frequency. (2.5%)

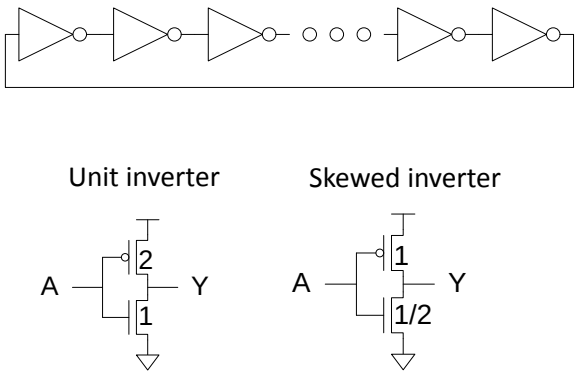

Fig. 4

5. Explain the following terminologies and its root cause: (**10%**)
   (a) Channel length modulation effect. (2%)
   (b) Velocity saturation. (2%)
   (c) Latchup. (2%)
   (d) Body effect. (2%)
   (e) Hot carriers. (2%)

6. A transmission gate as shown in Fig. 6 with V_{DD} = 1.4V and $|V_{tp}| = V_{tn}$ = 0.5V. **(5%)**
   (a) Sketch the transfer curve of Ron with V_{in} = 0 ~ V_{DD} (2.5%)
   (b) Sketch the curve with V_{DD} = 0.8V, observe and comments the possible issue. (2.5%)

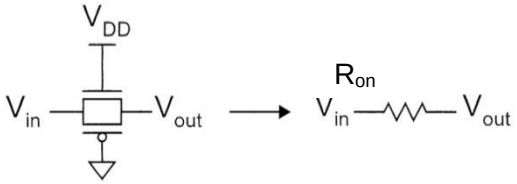

Fig. 6

7. Fig.7 shows the transfer curves of CMOS inverter with μ_n/μ_p = 3 and $V_{tn} = |V_{tp}|$ = 0.5V **(10%)**
   (a) For "B" curve, find (W/L)p with (W/L)n = 2um/0.18um. (2.5%)
   (b) Based on "B" curve, sketch and identify V_{IL}, V_{IH}, V_{OL}, and V_{OH} . (2.5%)
   (c) Define NM_H and NM_L. (2.5%)
   (d) Rank the noise margins (NM_H and NM_L) of A, B, and C. (2.5%)

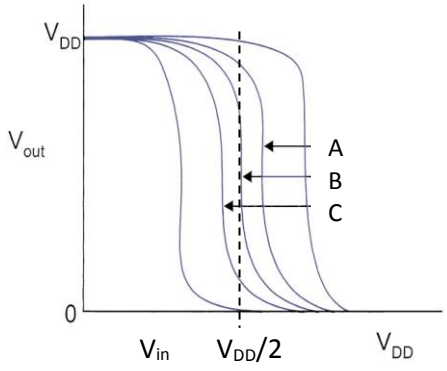

Fig. 7

8. The logic block shown in Fig. 8 has n_1 stages and a path effort of F = 128. Consider adding N-n_1 inverter to the end. Assume the i-th parasitic of logic block is p_i and the parasitic of inverter p_{inv} = 1. (**5%**)
   (a) Express path delay D in terms of N, F, p_i, n_1 and p_{inv}. (2.5%)
   (b) N = 10, n_1 = 4, p_i = 3, find the best stage effort ρ and the least delay D. (2.5%)

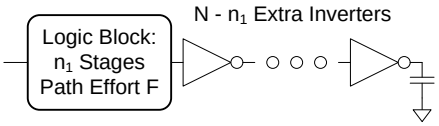

Fig. 8

9. Design a tapered buffer to drive a 256-unit loading (relative to C_{in} of unit inverter) as shown in Fig. 9. **(5%)**
   (a) Design stage number N to get the minimum delay. (2.5%)
   (b) Find the minimum stage effort delay f_i and the total path delay D. (2.5%)

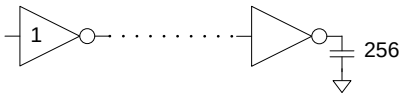

Fig. 9

10. Design the asymmetric gate in Fig. 10. **(5%)**
    (a) Choose the nMOS size of reset_B as 20 units, design and sketch the transistor sizes to get the rising and falling effective resistance equal to unit inverter. (2.5%)
    (b) Find g_A and g_B. (2.5%)

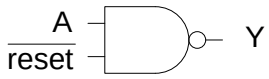

Fig. 10

11. Two adjacent wires X and Y are in a pair of 1mm lines with capacitances of 0.5 fF/μm to ground and 0.2 fF/μm to its neighbor. The wire width is 0.5um with a sheet resistance of 0.6Ω/□. Each line is driven by an inverter with a 0.5kΩ effective resistance and 50fF parasitic capacitance. Use one-segment pi-model for wire and Elmore delay model to find the propagation delay of X wire with the following conditions. **(10%)**
    (a) X=0→1.8V, Y=1.8V→0. (2.5%)
    (b) X=1.8V→0, Y=0. (2.5%)
    (c) If Y is floating, find the cross talk value ΔV_Y when X = 1.8V→0. (2.5%)
    (d) List 2 ways to reduce the cross talk. (2.5%)

12. A logic path as shown in Fig. 12. **(5%)**
    (a) Find the minimum path delay. (2.5%)
    (b) Find the size of the x, y, z to get the minimum path delay. (2.5%)

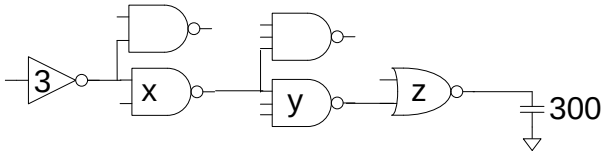

Fig. 12

13. Design an 8-input (k=8) AND gate using inverter and pseudo-nMOS NOR gates as shown in Fig. 13. Choose pull-up device size to be 1/3 and the output loading H = 64. **(5%)**
    (a) Find the path delay. (2.5%)
    (b) Sketch and label the transistor widths. (2.5%)

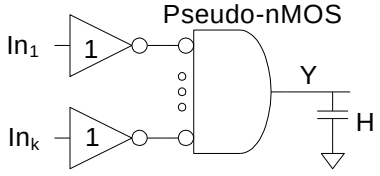

Fig. 13

14. Consider a NAND3 driving h copies of NAND3 as shown in Fig. 14. **(5%)**
    (a) Find the propagation delay. (2.5%)
    (b) Find the contamination delay. (2.5%)

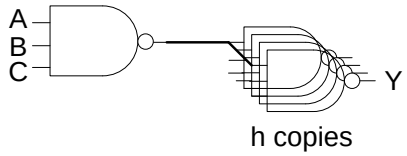

Fig. 14

15. Explain the following terminologies and its purpose: (**10%**)
    (a) High-K dielectric. (2%)
    (b) Low-K dielectric. (2%)
    (c) Copper interconnect. (2%)
    (d) FinFET. (2%)
    (e) SOI. (2%)

16. Answer the following questions with TRUE or FALSE: **(10%)**
    (a) Metal-insulator-metal capacitor is more popular in advanced technology for its low cost. (1%)
    (b) The delay of logic gate is proportional to product of logical effort and fanout. (1%)
    (c) Electromigration is caused by electron wind of AC current. (1%)
    (d) The dimension precision of source/drain implantation is higher than well. (1%)
    (e) Multiple threshold voltage devices use same oxide thickness for manufacturing concern. (1%)
    (f) The pitch of M1 is smaller than M6. (1%)
    (g) CMP is used to planarize the structure for multi-layer inter- connects stacking. (1%)
    (h) Salicide is used to reduce the S/D and gate resistance. (1%)
    (i) DRC is for design issue and LVS is for manufacturing issue. (1%)
    (j) For a multiple input logic, the slower input should be connected to outer node to get smaller delay. (1%)