1. Explain the following terminology and solution of dynamic logic. **(10%)**
   (a) Leakage. (2.5%)
   (b) Charge sharing. (2.5%)
   (c) Backgate coupling. (2.5%)
   (d) Clock feedthrough. (2.5%)

2. Consider the design of a CMOS single-bit full adder, assume the inputs are A, B and C_{in} (Carry-in) **(5%)**
   (a) Write the Boolean expressions of sum S and carry out C_{out}. (2.5%)
   (b) Write the Boolean expression of *Generate* (*G*) and *Propagate* (*P*) signals. (2.5%)

3. Consider the dynamic logics as shown in Fig. 3 **(5%)**
   (a) Write down the Boolean equations. (2.5%)
   (b) Find the logical efforts g_d and p_d for each (2.5%)

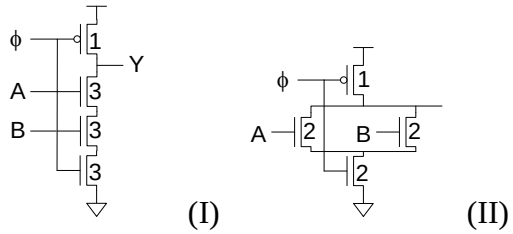

Fig. 3

4. A sequential circuit using flip-flop is shown in Fig. 4. Assume the period of clk = 10ns, max data-to-q delay t_{pdq} = 4ns, min data-to-q delay t_{cdq} = 1.5ns, max clk-to-q delay t_{pcq} = 2ns, min clock-to-q delay t_{ccq} = 0.5ns, setup time = 0.8ns, hold time = 1.2ns, the clock skew = 2ns. **(5%)**
   (a) Find the max delay of combination logic t_{pd}. (2.5%)
   (b) Find the min delay of combination logic t_{cd} with and without clock skew. (2.5%)

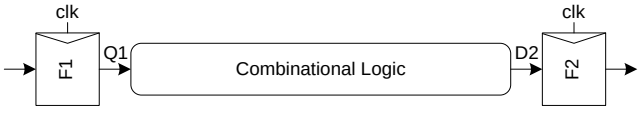

Fig. 4

5. Consider the MUX type ET FF as shown in Fig. 5. Assume the propagation delays of I_x and T_x are 1ns and 2ns respectively. The delay between clk and !clk is 0. **(5%)**
   (a) Find the setup time. (2.5%)
   (b) Find the propagation clock-to-q-delay t_{pcq}. (2.5%)

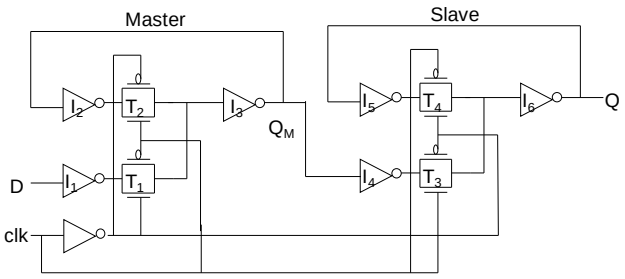

Fig. 5

6. Consider the sequential circuit as shown in Fig. 6. Assume period of $\phi_1 = \phi_2$ = 12ns, $t_{ccq1} = t_{ccq2}$ = 0.5ns, $t_{pcq1} = t_{pcq2}$ = 1.5ns, t_{hold} = 1.2ns and the clock skew = 1ns. **(5%)**
   (a) Assume the minimum delay $t_{cd1} = t_{cd2}$ = 0.6ns, design $t_{nonoverlap}$ to meet the hold time requirement. (2.5%)
   (b) Find the maximum delay t_{pd} with and without clock skew. (2.5%)

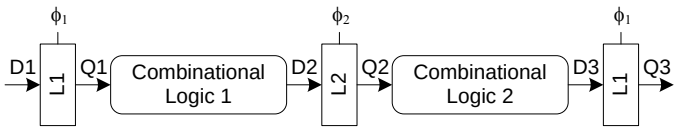

Fig. 6

7. Sketch the block diagram and result of addition of four 3-bit words (101, 010, 100, 011) with the following 2 types of adder. **(5%)**
   (a) Carry-Save Adder (CSA). (2.5%)
   (b) Carry-Propagation Adder (CPA). (2.5%)

8. Sketch the block diagram of the following shift register (SR) with flip-flop and MUX. **(5%)**
   (a) 4-bits serial-in-parallel-out SR. (2.5%)
   (b) 4-bits parallel-in-serial-out SR. (2.5%)

9. Consider the ET FF as shown in Fig. 9. Explain the relative clock conditions (clk and clk!) to cause the problems (a)~(c). **(10%)**
   (a) Race. (2.5%)
   (b) Undefined state. (2.5%)
   (c) Dynamic storage. (2.5%)
   (d) How to modify the design to guarantee it is hold time issue free? (2.5%)

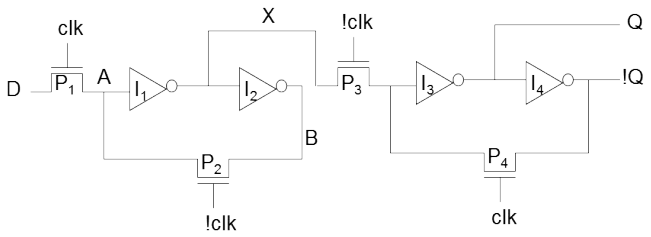

Fig. 9

10. Consider the ROM as shown in Fig. 10 with code Word[n] = [Y5Y4Y3Y2Y1Y0]. **(5%)**
   (a) Write the ROM code Word3~Word0. (2.5%)
   (b) Sketch the logic implementation of 2:4 DEC. (2.5%)

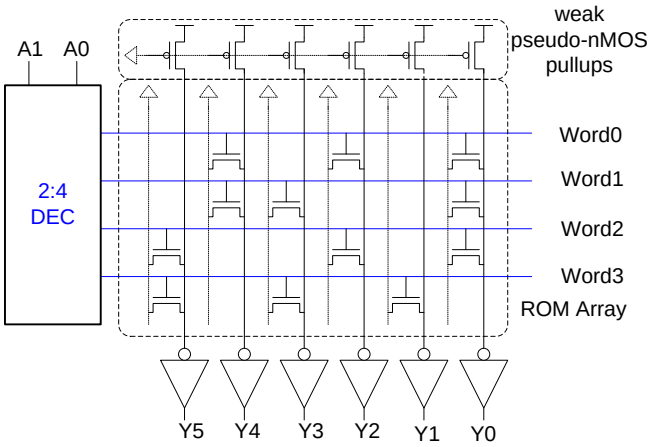

Fig. 10

11. Explain the implementation, pros, and cons of the following bitline design of DRAM. **(5%)**
   (a) *Open bitline*. (2.5%)
   (b) *Folded bitline* (2.5%)

12. Answer the following about Memory: **(10%)**
   (a) Explain the purpose of "bitline conditioning" in SRAM. (2%)
   (b) Explain the purpose of "sense amplifier". (2%)
   (c) Explain the purpose of "column multiplexing". (2%)
   (d) Write down two common methods to improve the yield of memory. (2%)
   (e) List two types of nonvolatile memory. (2%)

13. Consider the 6T SRAM cell in Fig. 13. **(5%)**
   (a) Explain the read-disturb behavior (in read operation) and index the cell ratio design concern to overcome it. (2.5%)
   (b) Based on the design concern in (a), explain the pull-up ratio design concern to get a correct write operation. (2.5%)

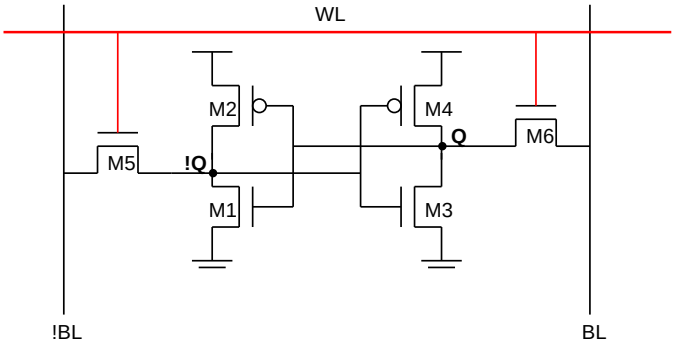

Fig. 13

14. Consider the DRAM cell in Fig. 14 with C_{cell} = 50fF and C_{bit} = 500fF. **(5%)**
   (a) Explain the read operation of DRAM. (2.5%)
   (b) Find the voltage difference $|\Delta V_x|$ (read"1" or read"0") with V_{DD} = 1.8V. (2.5%)

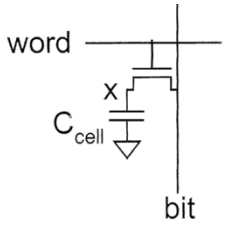

Fig. 14

15. Answer the following questions with TRUE or FALSE: **(20%)**
    (a) Latch is edge triggered and Flip-flop is level triggered. (1%)
    (b) Sequential logic using 2-phase latch is skew tolerant. (1%)
    (c) DRAM is compatible to standard CMOS process technology. (1%)
    (d) Multi-level decoder for memory is used to match smaller cell pitch. (1%)
    (e) Clock jitter due to high-frequency power noise cannot be calibrated. (1%)
    (f) *Drift* clock skew is due to process variation and can be solved by one-time calibration. (1%)
    (g) *Random* skew is caused by time-dependent environmental variations. (1%)
    (h) *Gray code* is a common skill for low power and jitter free decoder design. (1%)
    (i) Clock skew can be reduced by careful clock distribution, skew tolerant design and plenty of metal wire routing. (1%)
    (j) *Grid* type type clock distribution is suffered at systematic skew between points closet and furthest to the driver. (1%)
    (k) *H-Tree* clock distribution is suffered at delay mismatch of local near points from different tree. (1%)
    (l) *Design for test* = design circuit to increase fault observability and controllability. (1%)
    (m) *Boundary Scan test* used to decrease the probe contacts at wafer test stage. (1%)
    (n) *PRSG* is usually implemented for built-in-self-test pattern generation.
    (o) Fault coverage is a measure of goodness of a set of test vectors. (1%)
    (p) JTAG is a testing protocol for board level verification. (1%)
    (q) The RLC effect of I/O pads will affect the power quality and signal settling behavior as well. (1%)
    (r) The design consideration of output pad is noise reduction instead of driving capability. (1%)
    (s) Schmitt trigger is used to filter out the noise of output pin. (1%)
    (t) Bypassing capacitors are used to stabilize voltage and normally implemented with identical capacitances in parallel. (1%)

16. Answer the following questions with TRUE or FALSE: **(10%) (Bonus!)**
    (a) Metal-insulator-metal capacitor is more popular in advanced technology for its low cost. (1%)
    (b) The delay of logic gate is proportional to product of logical effort and fanout. (1%)
    (c) Electromigration is caused by electron wind of AC current. (1%)
    (d) The dimension precision of source/drain implantation is higher than well. (1%)
    (e) Multiple threshold voltage devices use same oxide thickness for manufacturing concern. (1%)
    (f) The pitch of M1 is smaller than M6. (1%)
    (g) CMP is used to planarize the structure for multi-layer inter- connects stacking. (1%)
    (h) Salicide is used to reduce the S/D and gate resistance. (1%)
    (i) DRC is for design issue and LVS is for manufacturing issue. (1%)
    (j) For a multiple input logic, the slower input should be connected to outer node to get smaller delay. (1%)