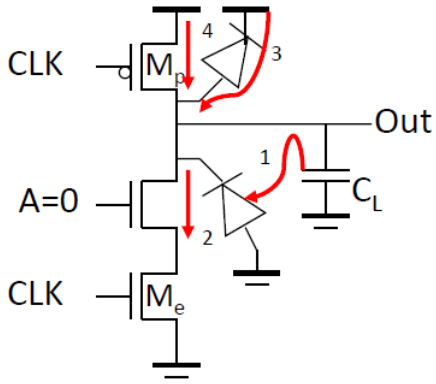
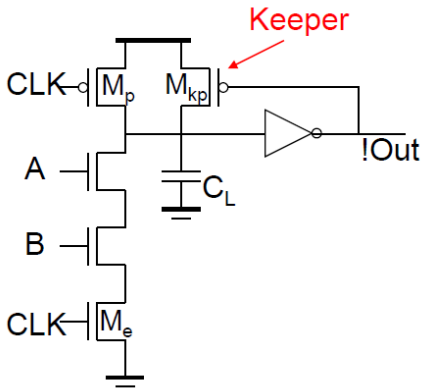
1. (A)MOS has leakage current when operating in subthreshold. Output settles to an intermediate voltage determined by a resistive divider of the pull-up and pull-down networks.



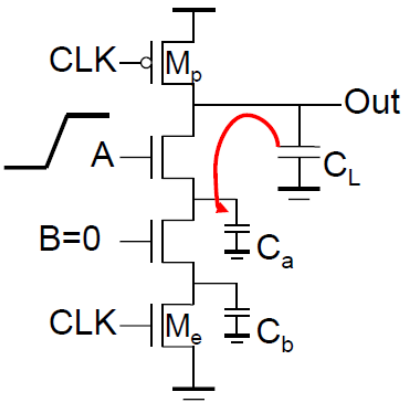
Leakage sources

Solution:

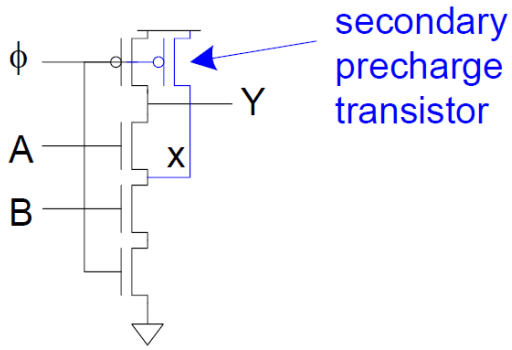
Keeper compensates for the charge lost due to the pull-down leakage paths.



(B)Charge stored originally on CL is redistributed (shared) over CL and CA leading to static power consumption by downstream gates and possible circuit malfunction.

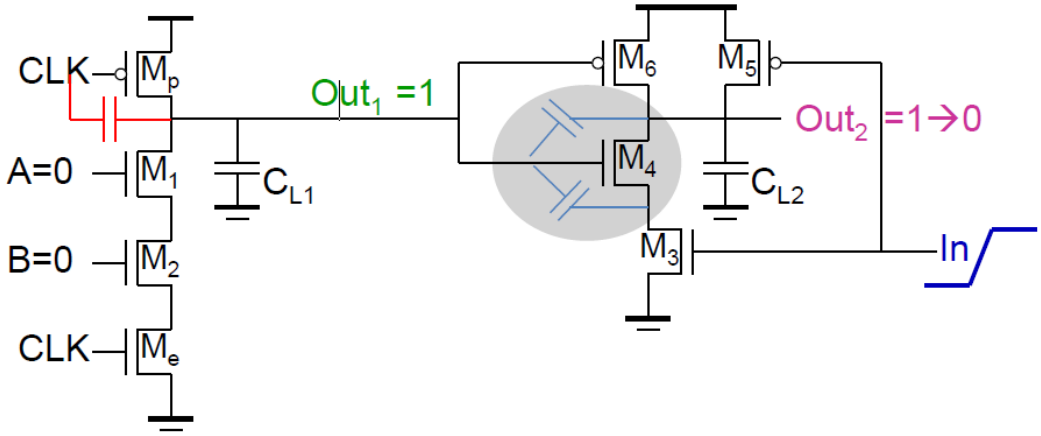


Solution: add secondary pre-charge transistors : typically need to pre-charge every other node, Big load capacitance CY helps as well.



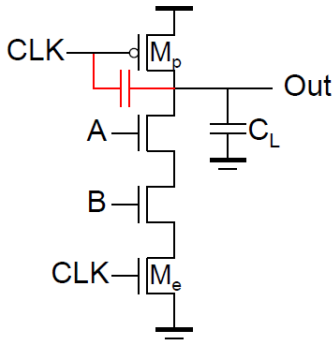
(C)Susceptible to crosstalk due to 1) high impedance of the output node and 2) backgate capacitive coupling

–Out2 capacitively couples with Out1 through the gate-source and gate-drain capacitances of M4



Solution: add loading CL1

(D) Coupling between Out and CLK input of the precharge device due to the gate-drain capacitance. So voltage of Out can rise above VDD. The fast rising (and falling edges) of the clock couple to Out.



Solution: add loading at CLK

2.

(a) $\mathrm{S} = \mathrm{A} \oplus \mathrm{B} \oplus \mathrm{C}_{in}$ $\mathrm{C}_{out} = AB + B\mathrm{C}_{in} + A\mathrm{C}_{in}$

(b) $\mathrm{G} = A \cdot B$ $\mathrm{P} = \mathrm{A} \oplus \mathrm{B}$

3.

(a) (I) $\mathrm{Y} = \overline{A \cdot B}$ (II) $\mathrm{Y} = \overline{A + B}$

(b) (I) $\mathrm{g}_d = 1,\ \mathrm{p}_d = \frac{4}{3}$ (II) $\mathrm{g}_d = \frac{2}{3},\ \mathrm{p}_d = \frac{5}{3}$

4.

(a) (寫其中一種即可)

Without skew: $\mathrm{T_{pd}} \leq \mathrm{T_c} - (\mathrm{T_{setup}} + \mathrm{T_{pcq}}) = 10\mathrm{ns} - (0.8\mathrm{ns} + 2\mathrm{ns}) = 7.2\mathrm{ns}.$

With skew: 5.2ns

(b) (兩種都要寫)

Without skew: $\mathrm{T_{cd}} \geq \mathrm{T_{hold}} - \mathrm{T_{ccq}} = 1.2\mathrm{ns} - 0.5\mathrm{ns} = 0.7\mathrm{ns}$.

With skew:2.7ns

5.

(a)

setup time $= 3\mathrm{I}_X + 1\mathrm{T}_X = 3 \times 1 + 2 = 5ns.$

(b)

$\mathrm{T_{pcq}} = 1\mathrm{I}_X + 1\mathrm{T}_X = 1 + 2 = 3ns.$

6.

(a) (寫其中一種即可)

Without skew:

$\mathrm{t}_{cd} \geq T_{hold} - t_{ccq} - t_{nonoverlap}.$

$0.6ns \geq 1.2ns - 0.5ns - t_{nonoverlap} \rightarrow t_{nonoverlap} \geq 0.1ns.$

With skew:

$\mathrm{t}_{cd} \geq T_{hold} - t_{ccq} - t_{nonoverlap} + t_{skew}.$

$0.6ns \geq 1.2ns - 0.5ns - t_{nonoverlap} + 1ns \rightarrow t_{nonoverlap} \geq 1.1ns.$

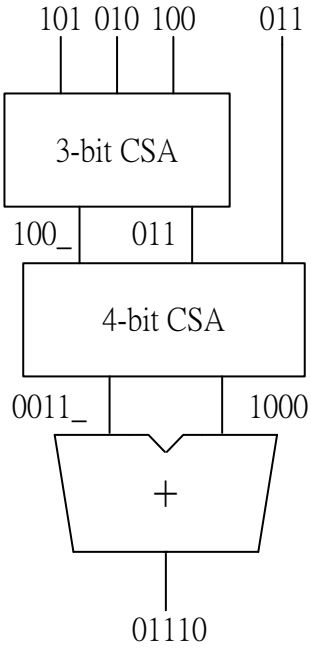
(b) (兩種都要寫)

With and without skew (skew-tolerant):

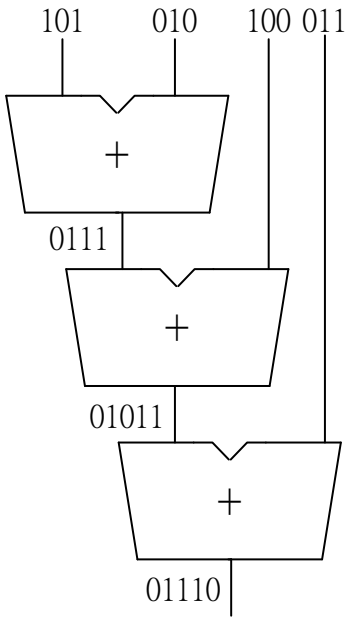
$\mathrm{t}_{pd} \leq T_C - (t_{pdq1} + t_{pdq2}) = 12ns - 2 \times 1.5ns = 9ns.$

7.

(a)

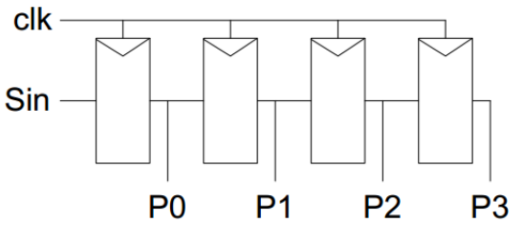

101 010 100
011
3-bit CSA
100_
011
4-bit CSA
0011_
1000
+
01110

(B)

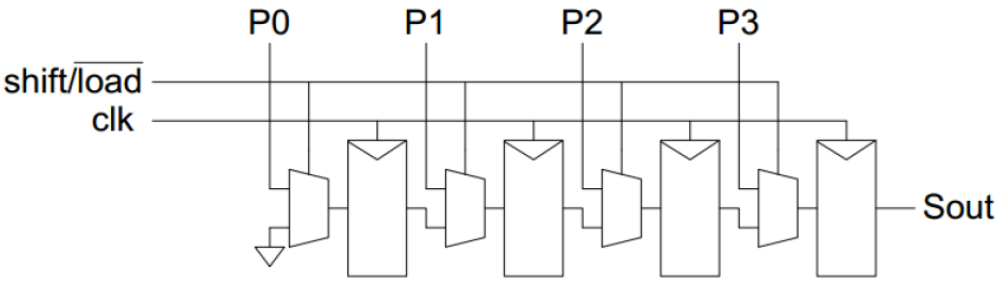

101
010
100 011
+
0111
+
01011
+
01110

8.

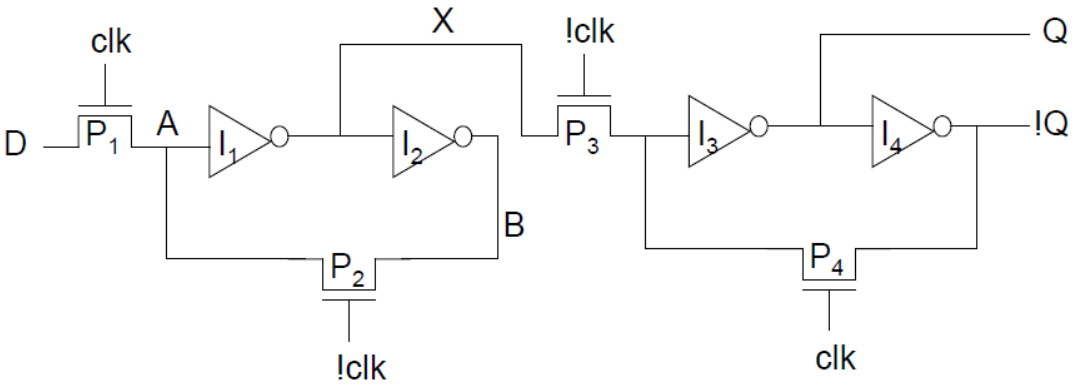
(a)



(b)



9.

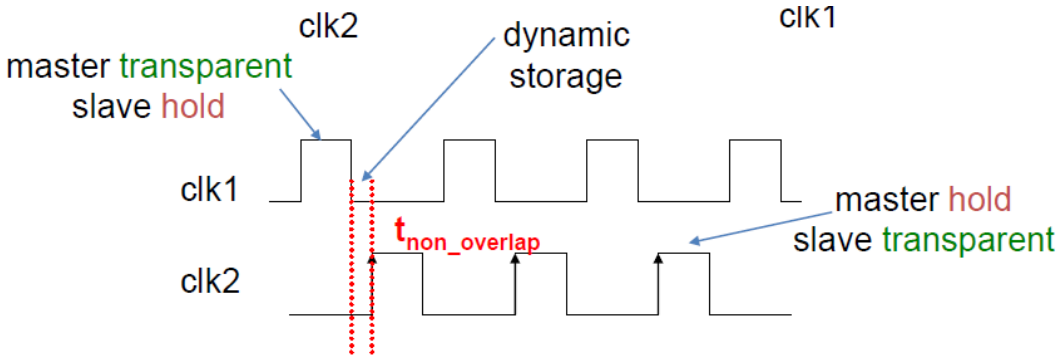


(a) direct path from D to Q during the short time when both clk and !clk are high (1-1 overlap)

(b) both B and D are driving A when clk and !clk are both high

(c) when clk and !clk are both low (0-0 overlap)

(d) An easy way to guarantee hold times is to use 2-phase latches with big nonoverlap times



10.

(a)

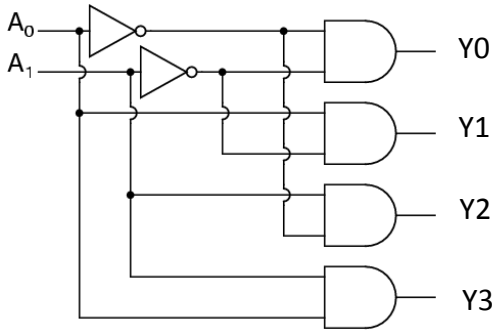
Word0=[010101]

Word1=[011001]

Word2=[100101]

Word3=[101010]

(b)



11.

(a) Open bitlines: use another subarray as reference

–Higher density

–Noise affect one array more than the other appears as differential noise.

(b) Folded bitlines: take the neighbor cell in the same subarry as reference

–Noise appears as common mode

–Larger layout area

12.

(a)

For read purpose: Precharge both bitlines high

• Then turn on wordline

• One of the two bitlines will be pulled down by the cell

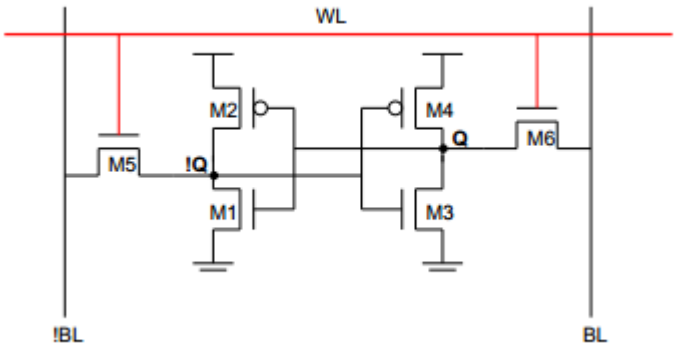
(b) *Sense amplifiers* are triggered on small voltage swing to reduce read time.

(c) *Add dummy lines:*The dummy lines are placed at the edge because photolithography and etch problems occur most often near the edge of large repetitive structure.

*ECC:*Error-detecting and correcting codes are commonly used to recover from soft errors that spontaneously flipa bit store in one of the cell.

*BIST:*Built-in self-test that place multiplexers in the address and data paths to take over the memory during test mode.

13.



(a)

Read stability

If !Q=0,voltage will bump up by resistive voltage division while word-line open.

M1>M5

(b) in write 1 operation, M6 must overpower M4 pull up MOS.

14.

1. The sense amplifiers are disconnected.
2. The bit-lines are precharged to exactly equal voltages that are in between high and low logic levels (e.g., 0.5 V if the two levels are 0 and 1 V). The bit-lines are physically symmetrical to keep the capacitance equal, and therefore at this time their voltages are equal.
3. The precharge circuit is switched off. Because the bit-lines are relatively long, they have enough capacitance to maintain the precharged voltage for a brief time. This is an example of dynamic logic.
4. The desired row's word-line is then driven high to connect a cell's storage capacitor to its bit-line. This causes the transistor to conduct, transferring charge from the storage cell to the connected bit-line (if the stored value is 1) or from the connected bit-line to the storage cell (if the stored value is 0). Since the capacitance of the bit-line is typically much higher than the capacitance of the storage cell, the voltage on the bit-line increases very slightly if the storage cell's capacitor is discharged and decreases very slightly if the storage cell is charged (e.g., 0.54 V and 0.45 V in the two cases). As the other bit-line holds 0.50 V there is a small voltage difference between the two twisted bit-lines.

(b) $\Delta \mathrm{Vx} = \frac{1.8}{2} \times \frac{50f}{50f+500f} = 0.08V$

15.

FTFTT

FFTTT

TTFTT

TTFFF

16.

FTFTF

TTTFF