1. Consider the design of a CMOS compound AND-OR-INVERT (AOI22) gate computing $F = \overline{(A \bullet B) + (C + D)}$. **(10%)**
   (a) Sketch transistor-level schematic. (2.5%)
   (b) Find g_A, g_C. (2.5%)
   (c) Sketch the stick diagram. (2.5%)
   (d) Find maximum and minimum p. (2.5%)

2. For a MOSFET device structure. **(5%)**
   (a) Sketch all the parasitic capacitance. (2.5%)
   (b) Sketch the transfer curve of gate cap. Cg versus V_{ds}/V_{dsat}. (2.5%)

3. Using pseudo-nMOS logic to implement NAND3 with relative pMOS size as 1/3 and design nMOS sizes to get an effective pulling low current as unit current compared to unit inverter. **(5%)**
   (c) Find logical effort g_u, g_d, and g_{avg}. (2.5%)
   (d) Find parasitic delay p_u, p_d, and p_{avg}. (2.5%)

4. Supposed and V_{tn} = 0.5V, find V_{out1} and V_{out2} in Fig. 4 by neglecting the body effect for: **(5%)**
   (a) V_{DD} = 1V, V_{in} = 0→0.5V. (2.5%)
   (b) V_{DD} = 1.2V, V_{in} = 0.5V→1V. (2.5%)

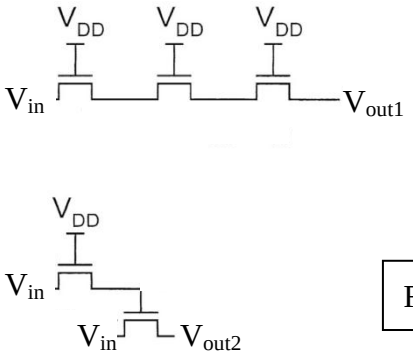

Fig. 4

5. Sketch a NOR4 CMOS static logic. **(5%)**
   (a) Choose the transistor widths to achieve effective rise and fall resistances equal to a unit inverter. (2.5%)
   (b) Sketch the stick diagram with smallest output parasitic capacitance. (2.5%)

6. Consider a NOR2 driving h copies of NAND2 as shown in Fig. 5. **(5%)**
   (a) Find the propagation delay. (2.5%)
   (b) Find the contamination delay. (2.5%)

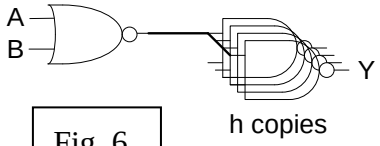

Fig. 6

7. Sketch on Fig. 7 and define the following terminologies based on unity-gain point. **(10%)**
   (a) V_{IL}, V_{IH}, V_{OL}, V_{OH}. (2%)
   (b) Define NM_H and NM_L. (2%)
   (c) Explain the trend of noise margin varied with β (μ_n/μ_p) ratio design. (2%)
   (d) If μ_n/μ_p = 4, how to design the ratio of W_p/W_n and make $NM_H = NM_L$. (2%)
   (e) Sketch and identify the operation regions of MOS for Vin = 0 → V_{DD}. (2%)

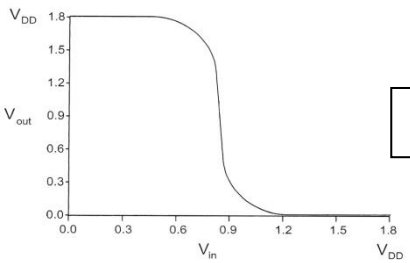

Fig. 7

8. Design a tapered buffer to drive a 256-unit loading (relative to C_{in} of unit inverter) as shown in Fig. 8. **(5%)**
   (a) Design stage number N and the minimum delay D. (2.5%)
   (b) Find the minimum stage effort delay f_i and the size of each stage. (2.5%)

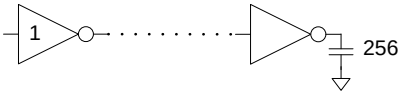

Fig. 8

9. There are 2 adjacent wires X and Y. Each wire in a pair of 0.5mm lines has capacitance of 0.6 fF/μm to ground and 0.4 fF/μm to its neighbor. The wire resistance is 0.3Ω/μm. Each line is

driven by an inverter with a 1kΩ effective resistance and 40fF parasitic capacitance. Use L-model to find the propagation delay of X wire with the following conditions. **(10%)**

(a) X=0→1, Y=1→0. (2.5%)
(b) X=1→0, Y=0. (2.5%)
(c) If Y is floating, find the cross talk value ΔV_Y when X = 1→0. (2.5%)
(d) List 2 ways to reduce the cross talk. (2.5%)

10. Design the asymmetric gate as shown in Fig. 10. **(5%)**
    (a) Choose the nMOS size of reset_B as 8 units, design and sketch the transistor sizes to get the rising and falling effective resistance equal to unit inverter. (2.5%)
    (b) Find g_A and g_B. (2.5%)

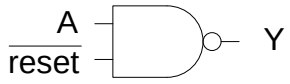

Fig. 10

11. Consider the design of 2-input NAND gate. **(5%)**
    (a) Design the optimized size of nMOS and pMOS size to get best noise margin. Find the logical effort g_{avg} and p. (2.5%)
    (b) Design the optimized size of nMOS and pMOS size to get the least delay. Find the logical effort g_{avg} and p. (2.5%)

12. A logic path as shown in Fig. 12. **(5%)**
    (a) Find the minimum path delay. (2.5%)
    (b) Find the size of the x, y, z to get the minimum path delay. (2.5%)

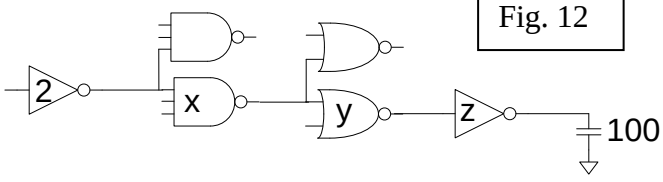

Fig. 12

13. Explain the following terminologies and its root cause: (**10%**)
    (a) Hot carrier. (2%)
    (b) Velocity saturation. (2%)
    (c) Latchup. (2%)
    (d) Mobility degradation. (2%)
    (e) Electromigration. (2%)

14. Design a 3-input LO-skew NAND gate. Size the devices so that the pull-down is x2 as strong as the pull-up. **(5%)**
    (a) Sketch and label the transistor widths. (2.5%)
    (b) Estimate the rising, falling and average logical efforts. (2.5%)

15. Design a 16-input (k=16) AND gat using inverter and pseudo-nMOS NOR gates as shown in Fig. 14. Choose pull-up device size to be 2/3 and the output loading H = 64. **(5%)**
    (a) Find the path delay. (2.5%)
    (b) Sketch and label the transistor widths. (2.5%)

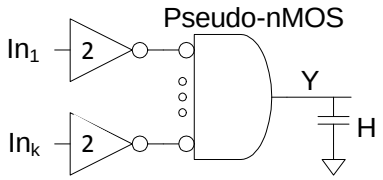

Fig. 14

16. Please give the correct order of the following steps in IC design flow (a) Chip verification (b) Ttransistors sizing and pre-sim (c) Choose device technology (d) Chip spec definition (e) Mask formation (f) Design rule check (g) Post simulation (h) Layout (i) Architecture define (j) Chip assembly (k) Parasitic extraction (l) Layout vs. schematic check **(5%)**.

17. Answer the following questions about MOS characteristics with TRUE or FALSE: **(10%)**
    (a) The critical path means the fastest one in logic gate. (1%)
    (b) The delay of logic gate is proportional to product of logical effort and parasitic. (1%)
    (c) Velocity saturation becomes worse at pMOS. (1%)
    (d) Mobility degradation is due to the strong lateral electric field in channel. (1%)
    (e) High-K gate dielectric can increase channel charge and reduce coupling effect. (1%)
    (f) Tunneling becomes worse at thinner gate oxide and higher Vgs. (1%)
    (g) Junction leakage is smaller than OFF channel leakage at modern technology. (1%)
    (h) Multiple threshold voltage devices need different oxide thickness and can't be implemented in single chip. (1%)
    (i) The finite output resistance of MOS at Saturation region is proportional to channel length. (1%)
    (j) FinFET is used to increase the ability of gate control in advanced transistor. (1%)
    (k) Poly layer is implemented before source /drain implant for better alignment. (1%)
    (l) Salicide is used to reduce the S/D and gate resistance. (1%)
    (m) Copper interconnect development is mainly due to its low resistance and thickness. (1%)
    (n) CMP is used to planarize the inter-layer isolation structure for multi-layer inter-connects stacking. (1%)
    (o) LDD is used to reduce hot carrier effect. (1%)