1. Consider the dynamic logics as shown in Fig. 1 **(10%)**
   (a) Write down the Boolean equations. (4%)
   (b) Find the logical efforts g_d and p_d for each (6%)

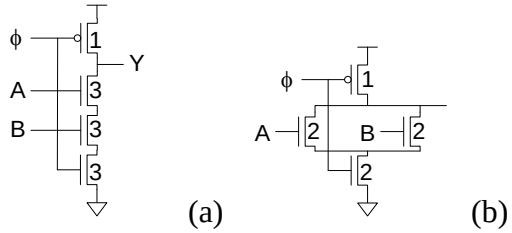

Fig. 1

2. Explain the following terminology and solution of dynamic logic. **(10%)**
   (a) Leakage. (2.5%)
   (b) Backgate coupling. (2.5%)
   (c) Clock feedthrough. (2.5%)
   (d) Charge sharing. (2.5%)

3. A sequential circuit using flip-flop is shown in Fig. 3. Assume the period of clk = 20ns, max clock-to-q delay t_{pcq} = 2ns, min clock-to-q delay t_{ccq} = 0.5ns, max data-to-q delay t_{dcq} = 2ns, min data-to-q delay t_{ccq} = 1.5ns, setup time = 1.2ns, and hold time = 2.8ns. **(10%)**
   (a) Find the max delay of combination logic t_{pd}. (2%)
   (b) Sketch the timing diagram of "clk", "Q1", and "D2" to illustrate the max delay. (2%)
   (c) Find the min delay of combination logic t_{cd}. (2%)
   (d) Sketch the timing diagram of "clk", "Q1", and "D2" to illustrate the min delay. (2%)
   (e) Add clock skew on (d) and find the min delay. (2%)

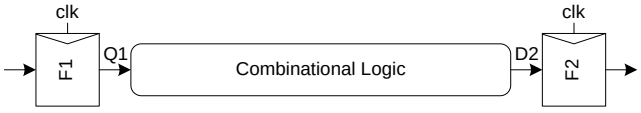

Fig. 3

4. Consider the ET FF as shown in Fig. 4. Explain the relative clock conditions (clk and clk!) to cause the problems (a)~(c). **(10%)**
   (a) Race. (2.5%)
   (b) Undefined state. (2.5%)
   (c) Dynamic storage. (2.5%)
   (d) How to modify the design to guarantee it is hold time issue free? (2.5%)

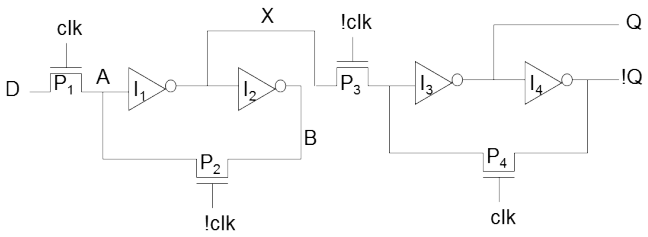

Fig. 4

5. Write down the Boolean equation of carry behaviors in full adder. **(5%)**
   (a) Generate (G). (2.5%)
   (b) Propagate (P). (2.5%)

6. Explain the design concept of the following 3 types of adder. **(10%)**
   (a) Carry-Lookahead. (2%)
   (b) Carry-Select. (2%)
   (c) Carry-Skip. (2%)
   (d) Order in speed of these 3 adders. (2%)
   (e) Pick one type of adder and sketch the block diagram. (2%)

7. Sketch the block diagram of the following design with flip-flop and MUX. **(5%)**
   (a) 4-bits serial-in-parallel-out shift register. (2.5%)
   (b) 4-bits parallel-in-serial-out shift register. (2.5%)

8. Explain the implementation, pros, and cons of the following bitlines design of DRAM. **(5%)**
   (a) *Open bitlines*. (2.5%)
   (b) *Folded bitlines* (2.5%)

9. Sketch the block diagram and Boolean equation of addition of four 3-bit words (111, 001, 100, 101) with the following 2 types of adder. **(10%)**
   (a) Carry-Save Adder (CSA). (5%)
   (b) Carry-Propagation Adder (CPA). (5%)

10. Consider the 4-bits array multiplier as shown in Fig. 10. For CSA block, the C_{in}-to-C_{out} delay = 2ns. For CPA block, C_{in}-to-C_{out} delay = 6ns. **(5%)**
   (a) With S_{in}-to-S_{out} delay = 3ns, find the total delay of the critical path. (2.5%)
   (b) With S_{in}-to-S_{out} delay = 1.5ns, find the total delay of the critical path. (2.5%)

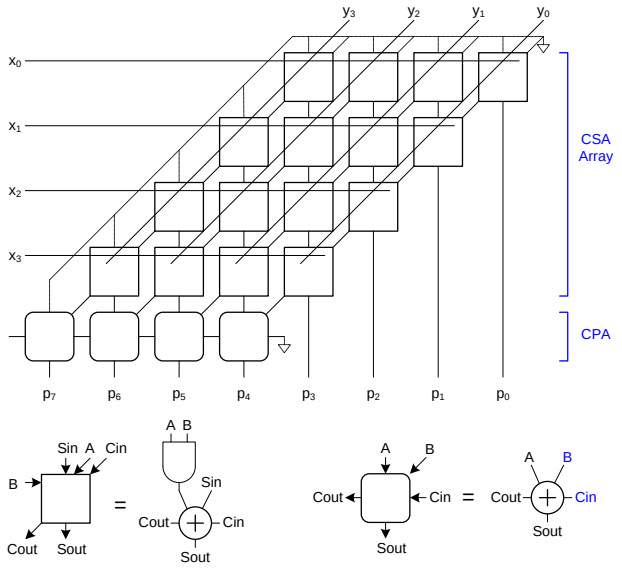

Fig. 10

11. Assume the bit line of a 1T DRAM cell is pre-charged to $V_{DD}/2$, the cell capacitance is 200fF, and the bit line capacitance is 0.6pF. **(5%)**
   (a) Find the data 0 and 1 voltage level on bit line during readout with VDD = 1V. (2.5%)
   (b) List two approaches to double the signal swing. (2.5%)

12. Consider the 6T SRAM cell in Fig. 12. **(5%)**
   (a) Explain the read-disturb behavior (in read operation) and index the cell ratio design concern to overcome it. (2.5%)
   (b) Based on the design concern in (a), explain the pull-up ratio design concern to get a correct write operation. (2.5%)

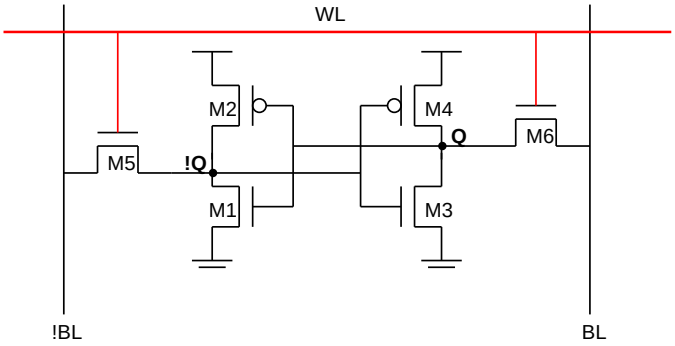

Fig. 12

13. Answer the following about Memory: **(10%)**
   (a) Explain the purpose of "bitline conditioning" in SRAM. (2%)
   (b) Explain the purpose of "column multiplexing" in SRAM. (2%)
   (c) Write down two common methods to improve the yield of memory. (2%)
   (d) List two types of nonvolatile memory. (2%)
   (e) Explain the purpose of content address memory (CAM). (2%)

14. Design a tapered buffer to drive a 512-unit loading (relative to C_{in} of unit inverter) as shown in Fig. 14. **(5%)**
   (a) Design stage number *N* to get the minimum delay. (2.5%)
   (b) Find the minimum stage effort delay f_i and the total path delay *D*. (2.5%)

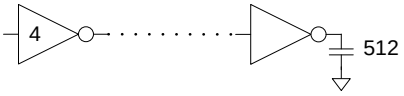

Fig. 14

15. There are 2 adjacent wires X and Y. Each wire in a pair of 2mm lines has capacitance of 0.8 fF/μm to ground and 0.4 fF/μm to its neighbor. The wire resistance is 0.2Ω/μm. Each line is driven by an inverter with a 1kΩ effective resistance and 40fF parasitic capacitance. Use L-model to find the propagation delay of X wire with the following conditions. **(5%)**
    (a) X=1→0, Y=0→1. (2.5%)
    (b) If Y is floating, find the cross talk value ΔV_Y when X = 1→0. (2.5%)

16. A logic path as shown in Fig. 16. **(5%)**
    (a) Find the minimum path delay. (2.5%)
    (b) Find the size of the x, y, z to get the minimum path delay. (2.5%)

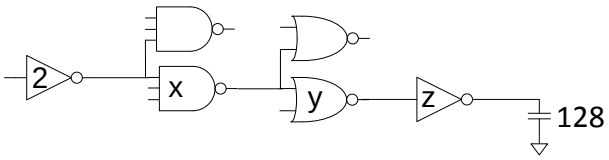

Fig. 16

17. Consider a NAND2 driving h copies of NAND2 as shown in Fig. 17. **(5%)**
    (a) Find the propagation delay. (2.5%)
    (b) Find the contamination delay. (2.5%)

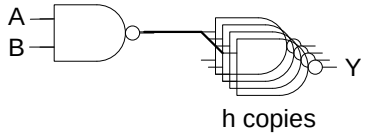

Fig. 17

18. Answer the following questions with TRUE or FALSE: **(10%)**
    (a) Flip-flop is edge triggered and Latch is level triggered. (1%)
    (b) Sequential logic using 2-phase latch is skew tolerant. (1%)
    (c) Clock jitter is due to the low frequency environment variation and cannot be calibrated. (1%)
    (d) *Drift* clock skew is due to process variation and can be solved by one-time calibration. (1%)
    (e) Clock skew can be reduced by careful clock distribution, skew tolerant design and plenty of metal wire routing. (1%)
    (f) *Grid* type clock distribution is suffered at systematic skew between points closet and furthest to the driver. (1%)
    (g) *H-Tree* type clock distribution is suffered at delay mismatch of local near points from different tree. (1%)
    (h) *Design for test* = design circuit to increase fault observability and controllability. (1%)
    (i) *Boundary Scan test* can be used to verify solder joints on PCB. (1%)
    (j) The RLC effect of I/O pads and pins should be included in circuit simulation to increase the accuracy. (1%)