1. Consider the design of a CMOS compound AND-OR-INVERT (AOI22) gate computing $F = \overline{(A \bullet B) + (C + D) \bullet E}$. **(10%)**
   (a) Sketch transistor-level schematic. (2.5%)
   (b) Find $g_A$, $g_C$, $g_E$. (2.5%)
   (c) Sketch the stick diagram. (2.5%)
   (d) Find maximum and minimum p. (2.5%)

2. Using pseudo-nMOS logic to implement NAND3 with relative pMOS size as 2/3 and design nMOS sizes to get an effective pulling low current as unit current compared to unit inverter. (5%)
   (a) Find logical effort $g_u$, $g_d$, and $g_{avg}$. (2.5%)
   (b) Find parasitic delay $p_u$, $p_d$, and $p_{avg}$.. (2.5%)

3. Supposed $V_{DD} = 1.2V$ and $|V_{tp}| = V_{tn} = 0.5V$, find $V_{out} = (?)V \rightarrow (?)V$ in Fig. 3 by neglecting the body effect for: (5%)
   (a) $V_{in} = 1.2 \rightarrow 0.3V$. (2.5%)
   (b) $V_{in} = 0V \rightarrow 0.9V$. (2.5%)

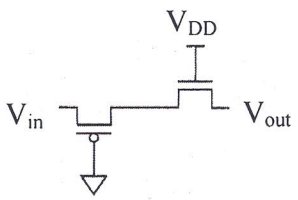


Fig. 3

4. Sketch a NOR3 CMOS static logic. (5%)
   (a) Choose the transistor widths to achieve effective rise and fall resistances equal to a unit inverter. (2.5%)
   (b) Sketch the stick diagram with smallest output parasitic capacitance. (2.5%)

5. Consider a NAND3 driving h copies of NAND2 as shown in Fig. 5, (5%)
   (c) Find the propagation delay. (2.5%)
   (d) Find the contamination delay. (2.5%)

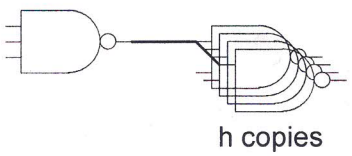


Fig. 5

6. Sketch on Fig. 6 and define the following terminologies based on unity-gain point. **(10%)**
   (a) $V_{IL}$, $V_{IH}$, $V_{OL}$, $V_{OH}$. (2%)
   (b) Define $NM_H$ and $NM_L$. (2%)
   (c) Explain the trend of noise margin with high-skewed and low-skewed design. (2%)
   (d) If $\mu_n/\mu_p = 3$, how to design the ratio of $W_p/W_n$ and make $NM_H = NM_L$. (2%)
   (e) What are the $NM_H$ and $NM_L$ of dynamic inverter? (2%)

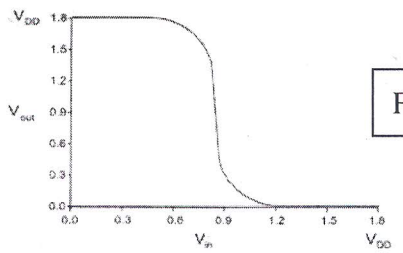


Fig. 6

7. Design a tapered buffer to drive a 128-unit loading (relative to $C_{in}$ of unitinverter) as shown in Fig. 6. (5%)
   (f) Design stage number N to get the minimum delay. (2.5%)
   (g) Find the minimum stage effort delay $f_i$ and the total path delay D. (2.5%)

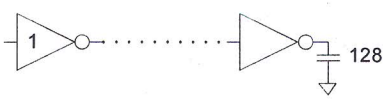


Fig. 6

8. There are 2 adjacent wires X and Y. Each wire in a pair of 0.5mm lines has capacitance of 0.4 fF/μm to ground and 0.2 fF/μm to its neighbor. The wire resistance is 0.2Ω/μm. Each line is driven by an inverter with a 1kΩ effective resistance and 10fF parasitic capacitance. Use L-model to find the propagation delay of X line with the following conditions. **(10%)**
   (a) X=0→1, Y=1→0. (2.5%)
   (b) X=1→0, Y=1. (2.5%)
   (c) If Y is floating, find the cross talk value $\Delta V_Y$ when X = 0→1. (2.5%)
   (d) List 2 ways to reduce the cross talk. (2.5%)

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9. A ring oscillator composed of N-stages identical inverters is as shown in Fig. 9. Assume the effective resistance of an unit inverter (P:2, N:1) is 0.5kΩ and parasitic capacitance is 5fF. (5%)
   (a) N = 7, find the oscillated frequency. (2.5%)
   (b) Use skewed inverter and find the oscillated frequency. (2.5%)

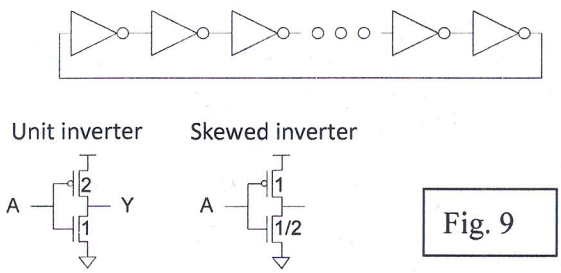


Fig. 9

10. Consider the design of 3-input NAND gate. (5%)
   (a) Design the optimized size of nMOS and pMOS size to get best noise margin. Find the logical effort $g_{avg}$ and p. (2.5%)
   (b) Design the optimized size of nMOS and pMOS size to get the least delay. Find the logical effort $g_{avg}$ and p. (2.5%)

11. Explain the following non-ideal effects about dynamic logic and propose the solutions. **(10%)**
   (a) Clock feedthrough. (2%)
   (b) Leakage. (2%)
   (c) Charge sharing. (2%)
   (d) Backgate coupling. (2%)
   (e) Error due to Cascading gates. (2%)

12. A logic path as shown in Fig. 12. (5%)
   (a) Find the minimum path delay. (2.5%)
   (b) Find the size of the x, y, z to get the minimum path delay. (2.5%)

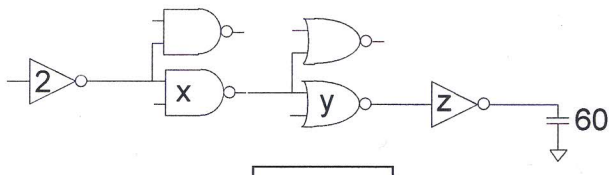


Fig. 12

13. Explain the following terminologies and its root cause: **(10%)**
   (a) Latchup. (2%)
   (b) Hot carriers. (2%)
   (c) Electromigration. (2%)
   (d) Self-heating. (2%)
   (e) Soft errors. (2%)

14. A pass transistor logic is implemented as shown in Fig. 12 with $V_{DD}$ = 1.2V, $|V_{tp}| = |V_{tn}|$ = 0.5V, The inverter $M_1(M_2)$ has $V_{IL}$ = 0.2V and $V_{IH}$ = 1.0V. Ignore the body effect. (5%)
   (a) Sketch the schematic of adding a restorer to solve the voltage drop at $V_x$. (2.5%)
   (b) Assume $R_{on}(M_n)$ = 100ohms, design the minimum $R_{on}$ of restorer to avoid logic 1 fail at $V_{out}$. (2.5%)

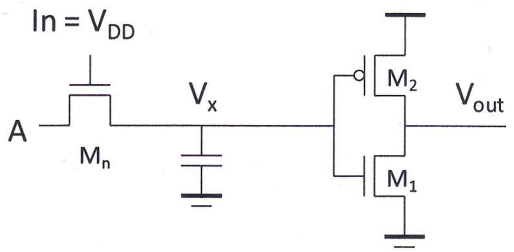


Fig. 12

15. A 100M transistor chip with 20M logic and 80M memory transistors, the switching activity factors of logic and memory are 0.1 and 0.05 respectively. The average width of logic and memory are 0.6um and 0.2um, and the $C_g$ = 2fF/um. With operating frequency as 1GHz and $V_{DD}$=0.8V, find the dynamic power consumption. (5%)

16. Answer the following questions about MOS characteristics with TRUE or FALSE: **(15%)**
   (a) $C_g$ (gate capacitance) at Saturation is larger than that at Linear region. (1%)
   (b) Source/Drain junction capacitance is proportional to length. (1%)

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(c) Velocity saturation becomes worse at pMOS. (1%)
(d) Mobility degradation is due to the strong lateral electric field in channel. (1%)
(e) Tunneling becomes worse at thinner gate oxide and higher Vgs. (1%)
(f) Junction leakage is smaller than OFF channel leakage at modern technology. (1%)
(g) The finite output resistance of MOS at Saturation region is proportional to channel length. (1%)
(f) High-K gate dielectric can increase channel charge and reduce coupling effect. (1%)
(g) FinFET is used to increase the ability of gate control in advanced transistor. (1%)
(h) Silicon-on-Insulator (SOI) can increase device speed, but with worse latchup issue. (1%)
(i) Multiple threshold voltage devices need different oxide thickness and can't be implemented in single chip. (1%)
(j) Copper interconnect development is mainly due to its low resistance and thickness. (1%)
(k) CMP is used to planarize the inter-layer isolation structure for multi-layer inter-connects stacking. (1%)
(l) Salicide is used to reduce the S/D and gate resistance. (1%)
(m) LDD is used to reduce S/D junction leakage to substrate. (1%)
(n) MIM capacitor can be implemented in logic process with better matching and higher density compared to MOM. (1%)
(o) DRC is for design issue and LVS is for manufacturing issue. (1%)

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