1. Consider the MUX type ET FF as shown in Fig. 1. Assume the propagation delays of $I_x$ and $T_x$ are 2ns and 4ns respectively. The delay between clk and !clk is 0 (5%)
   (a) Find the setup time. (2.5%)
   (b) Find the propagation clock-to-q-delay $t_{pcq}$. (2.5%)

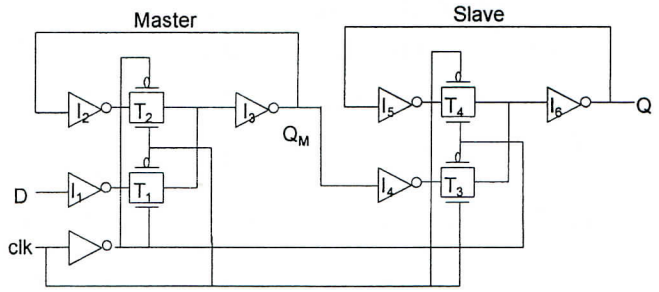


Fig. 1

2. Use Fig. 1. to state the condition and explain the following problems from clock skew of clk and clk!. (5%)
   (a) Race. (2.5%)
   (b) Dynamic Storage. (2.5%)

3. Design a 2-phase clock generator with NAND and INV gates. (5%)
   (a) Sketch the schematic. (3%)
   (b) Identify the added delay chain in your schematic to program the non-overlapped interval. (2%)

4. A sequential circuit using pulse latch is shown in Fig. 4. Assume the period of clk = 10ns, max data-to-q delay $t_{pdq}$ = 4ns, max clk-to-q delay $t_{pcq}$ = 2ns, setup time = 0.5ns. (5%)
   (a) With pulse width $t_{pw}$ = 4ns, find the max delay of combination logic $t_{pd}$. (2.5%)
   (b) With pulse width $t_{pw}$ = 2ns, find the max delay of combination logic $t_{pd}$. (2.5%)

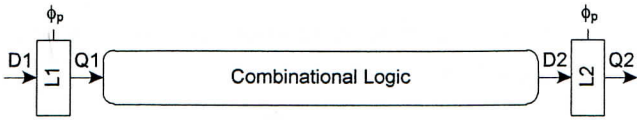


Fig. 4

5. Consider the sequential circuit as shown in Fig. 5. Assume period of $\phi_1 = \phi_2$ = 20ns, $t_{ccq1} = t_{ccq2}$ = 1ns, $t_{pcq1} = t_{pcq2}$ = 6ns, $t_{hold}$ = 4ns and the clock skew = 2ns. (5%)
   (a) Assume the minimum delay $t_{cd1} = t_{cd2}$ = 1ns, design $t_{nonoverlap}$ to meet the hold time requirement. (2.5%)
   (b) Find the maximum delay $t_{pd}$ with and without clock skew. (2.5%)

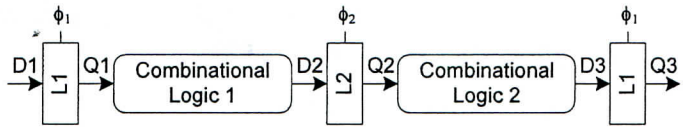


Fig. 5

6. Consider the design and condition in question 5, assume the minimum clk-to-q-delay $t_{ccq}$ is 1.5ns, the minimum delay of combination logic $t_{cd}$ = 4ns, and pulse width $t_{pw}$ = 2ns. (5%)
   (a) Find the hold time. (2.5%)
   (b) Redesign the latch with a hold time = 1ns, find the maximum tolerant clock skew. (2.5%)

7. Consider a full adder with inputs A and B; carry-in $C_{in}$, sum S, and carry-out $C_{out}$. (5%)
   (a) Write the Boolean expressions of sum S and carry-out $C_{out}$. (2.5%)
   (b) Write the Boolean expressions of sum S and carry-out $C_{out}$ in term of G (Generate), P (Propogate) and carry-in ($C_{in}$). (2.5%)

8. Explain the design concept of the following 3 types of adder. (10%)
   (a) Carry-Lookahead. (2%)
   (b) Carry-Select. (2%)
   (c) Carry-Skip. (2%)
   (d) Order in speed of these 3 adders. (2%)
   (e) Pick one type of adder and sketch the block diagram. (2%)

9. Sketch the block diagram and Boolean equation of addition of four 3-bit words (011, 101, 100, 110) with the following 2 types of adder. (10%)
   (a) Carry-Save Adder. (5%)
   (b) Carry-Propagation Adder. (5%)

10. The 4-bits array multiplier as shown in Fig. 11 is implemented by adders with $C_{in}$-$C_{out}$ delay = 4ns, $S_{in}$-$S_{out}$ delay = 5ns. (5%)
    (a) Find the critical path and delay in Fig. 11.1. (2.5%)
    (b) Sketch the circuit of Fig. 11.2 with the adder in Fig. 11.3 and necessary supporting combination logic. (2.5%)

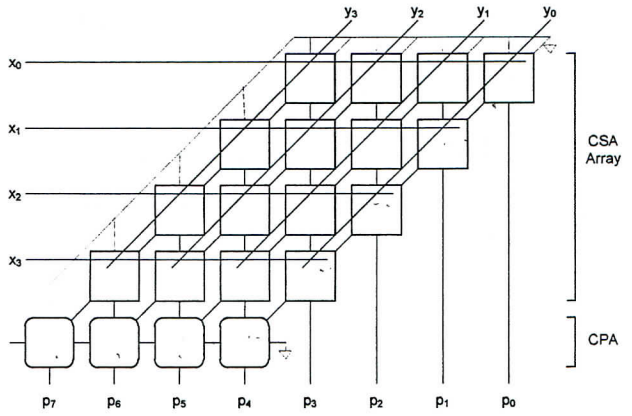


Fig. 11.1

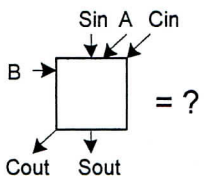


Fig. 11.2

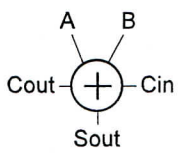


Fig. 11.3

11. Find the output patterns of the following shift functions with input pattern 10011. (5%)
    (c) Logical shift "Left" 2 bits. (2.5%)
    (d) Arithmetic shift "Right" 2 bits. (2.5%)

12. Consider the 6T SRAM cell in Fig. 12. (5%)
    (a) Explain the read-disturb behavior (in read operation) and index the cell ratio design concern to overcome it. (2.5%)
    (b) Based on the design concern in (a), explain the pull-up ratio design concern to get a correct write operation. (2.5%)

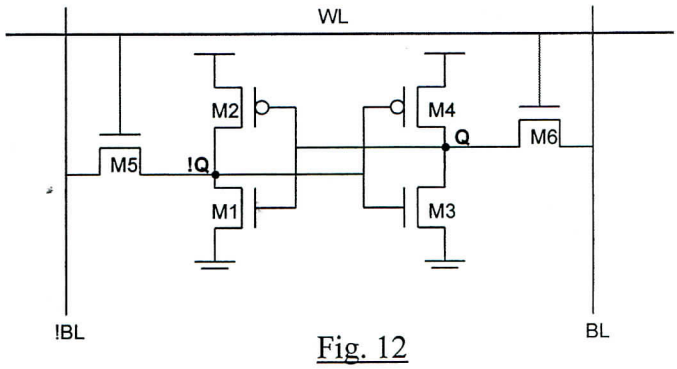


Fig. 12

13. Explain the functions and purposes of the following peripheral blocks of SRAM. (5%)
    (a) *Bit-line conditioning*. (2.5%)
    (b) *Sense amplifier*. (2.5%)

14. Assume the bit line of a 1T DRAM cell is pre-charged to $V_{DD}/2$, the cell capacitance is 50fF, and the bit line capacitance is 1pF. (5%)
    (a) Find the data 0 and 1 voltage level on bit line during readout with VDD = 1.8V. (2.5%)
    (b) List two approaches to double the signal swing. (2.5%)

15. Answer the following about Memory: (10%)
    (a) Explain the purpose of "*Twisted bitline*" in SRAM. (2%)
    (b) Explain the purpose of "equalization" in bitline conditioning of SRAM. (2%)
    (c) Explain the purpose of isolation transistor in sense amplifier. (2%)

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(d) Write down two common methods to improve the yield of memory. (2%)

(e) What's the 6x4 code in the ROM as shown in Fig. 15. (2%)

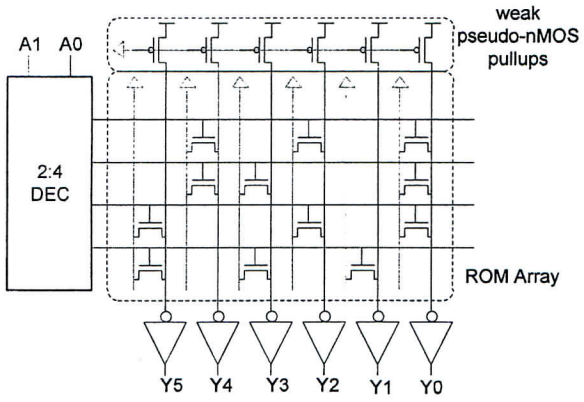


Fig. 15

16. Design a tapered buffer to drive a 256-unit loading (relative to $C_{in}$ of unit inverter) as shown in Fig. 16. (5%)
    (a) Design stage number $N$ to get the minimum delay. (2.5%)
    (b) Find the minimum stage effort delay $f_i$ and the total path delay $D$. (2.5%)

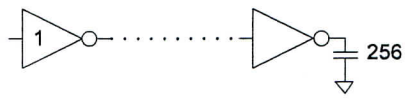


Fig. 16

17. Using pseudo-nMOS logic to implement NOR-5 with a relative pMOS size as 2/3 and design nMOS sizes to get an effective pulling low current as unity compared to unit inverter. (5%)
    (a) Find logical effort $g_u$, $g_d$, and $g_{avg}$. (2.5%)
    (b) Find parasitic delay $p_u$, $p_d$, and $p_{avg}$. (2.5%)

18. Sketch the transistor-level schematic of the gate computing $F = \overline{(A \bullet B) + (C \bullet D)}$: (5%)
    (c) Find logical effort $g_A$ and $g_C$. (2.5%)
    (d) Find parasitic delay p. (2.5%)

19. There are 2 adjacent wires X and Y. Each wire in a pair of 1mm lines has capacitance of 0.3 fF/μm to ground and 0.6 fF/μm to its neighbor. The wire resistance is 0.2Ω/μm. Each line is driven by an inverter with a 1kΩ effective resistance and 20fF parasitic capacitance. Use L-model to find the propagation delay of X line with the following conditions. (5%)
    (a) X = 0→1, Y = 0. (2.5%)
    (b) If Y is floating, find the cross talk value $\Delta V_Y$ when X = 1→0. (2.5%)

20. Answer the following questions with TRUE or FALSE: (10%)
    (a) Sequential logic using flip-flop is skew tolerant. (1%)
    (b) Time borrowing range of 2-phase latch depends on period and hold time. (1%)
    (c) Latch is edge triggered and Flip-flop is level triggered. (1%)
    (d) Minimum delay of sequential logic depends on hold time. (1%)
    (e) *Drift* is kind of skew that can be removed by careful layout. (1%)
    (f) *Random* skew is caused by time-dependent environmental variations. (1%)
    (g) *Gray code* is a common skill for low power and jitter free decoder design. (1%)
    (h) Clock distribution with H-Tree results in higher systematic skew. (1%)
    (i) Wide clock wire is segmented to be narrower to avoid conductance effect. (1%)
    (j) *Boundary Scan test* is used to decrease the probe contacts at wafer test stage. (1%)

21. Answer the following questions with TRUE or FALSE: (10%)
    (a) *Design for test* means to design circuit with fault observability and controllability. (1%)
    (b) The soft error in Memory can be solved by redundancy and ECC. (1%)

(c) SRAM and DRAM are nonvolatile and ROMs are volatile memory. (1%)

(d) Compare to single-level decoder, multi-level decoder can be implemented to match smaller memory cell pitch with better glitch performance. (1%)

(e) The read operation of DRAM is single ended and need following refresh. (1%)

(f) PRSG is usually implemented for built-in-self-test pattern generation. (1%)

(g) Bi-directional I/O is used for analog signal's input and output. (1%)

(h) Cost, form factor, heat removal, and little delay/distortion are all functions of package. (1%)

(i) Bypassing capacitors are used to stabilize voltage and normally implemented with identical capacitances in parallel. (1%)

(j) Schimitt trigger is used to filter out noise of output. (1%)