2011 VLSI Final Exam Solution

2012/1/12

1.

(a)

t_{su}=10ns

(b)

t_{pcq}=6ns

2.

(a.) 2.5%

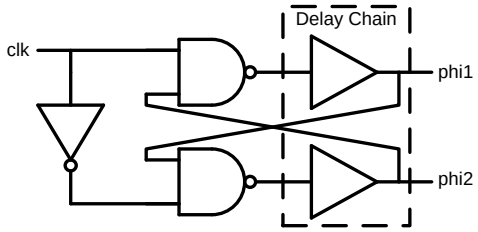
Race condition – direct path from D to Q during the short time when both clk and !clk are high (1-1 overlap)

(b.) 2.5%

Dynamic storage – when clk and !clk are both low (0-0 overlap)

3.

(a.) 3%



(b.) 2% Delay chain 為 buffer (2N 個 inverter)

4.

(a)

$$t_{pd} \leq T_c - \max(t_{pdq}, t_{pcq} + t_{setup} - t_{pw})$$
$$= 10n - \max(4n, 2n + 0.5n - 4n)$$
$$= 10n - 4n$$
$$= 6n\ (s)$$

(b)

$$t_{pd} \leq T_c - \max(t_{pdq}, t_{pcq} + t_{setup} - t_{pw})$$
$$= 10n - \max(4n, 2n + 0.5n - 2n)$$
$$= 10n - 4n$$
$$= 6n\ (s)$$

5.

(a)

$T_{nonoverlap} \geq 4ns$

(b)

$T_{pd} \leq 8ns$

(skew tolerance)

6.

(a)

$t_{pw} = 2ns$

$$t_{nonoverlap} = \frac{T_c}{2} - t_{pw} = 10n - 2n = 8n$$

$$t_{cd1}, t_{cd2} \geq t_{hold} - t_{ccq} - t_{nonoverlap} + t_{skew}$$

$$t_{hold} \geq t_{ccq} + t_{nonoverlap} - t_{skew} + t_{cd1}, t_{cd2}$$

$$t_{hold} \leq 1.5n + 8n - 2n + 4n = 11.5n(s)$$

(b)

$$t_{cd1}, t_{cd2} \geq t_{hold} - t_{ccq} - t_{nonoverlap} + t_{skew}$$

$$t_{skew} \leq t_{cd1}, t_{cd2} - t_{hold} + t_{ccq} + t_{nonoverlap}$$

$$= 4n - 1n + 1.5n + 8n = 12.5n(s)$$

7.

(a)

$S = A \oplus B \oplus C_{in}$

$C_{out} = AB + BC_{in} + C_{in}A$

(b)

$S = P \oplus C_{in}$

$C_{out} = G + PC_{in}$

8.

(a) 參見講義 Chapter 7-32 頁

(b) 參見講義 Chapter 7-36 頁

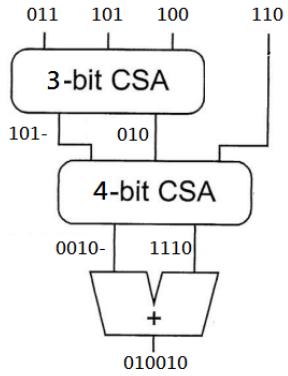
(c) 參見講義 Chapter 7-28 頁

(d) Speed: (b)>(a)>(c)

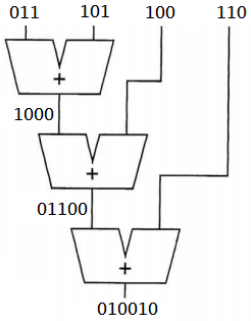
(e) 參見講義 Chapter 7-28、32、36 頁，畫出任一即給分

9.

(a)5%

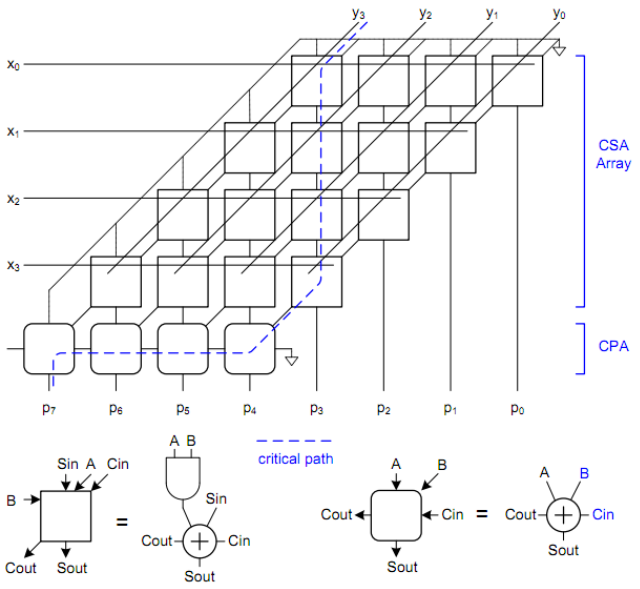


(b)5%



10.

(a)(b)



1.5% 2.5%

Delay=$4(C_{in}-C_{out})+4(S_{in}-S_{out})=36ns$(1%)

11.

(a)01100 (2.5%)
(b)11100 (2.5%)

12.

(a)
Assuming !Q=0 and Q=1. During read operation, there will be a voltage divider at !Q, which causes the !Q voltage increasing. Therefore, the ratio of M1/M5 and M3/M6 should be much larger than 1.
(b)
During write operation, M4(M2) and M6(M5) are fighting. To make sure of correct write operation, M6(M5) >> M4(M2).

13.

(a)
precharge bitline to V_{DD}
(b)
sense small voltage difference between two bitlines

14.

(a)V0=0.8571≒0.86
V1=0.9429≒0.94 (1.5% → 2.5%)
(b)
1. Double the C_{cell}.(use trench)
2. Halve the $C_{bitline}$.(reduce the cell number in one line)
3. Double the VDD. (any two get 2.5%)

15.

(a)
Try to couple noise equally onto bit and bit_b, and hence reduce the noise effect.
(b)
Equalize bitlines to minimize voltage difference between bit and bit_b when using sense amplifier.
(c)
To cut off large bitline capacitance.

(d)

(1)redundancy cell.

(2)ECC.

(3)built in selft test (BIST).

(e)

010101

011001

100101

101010

16.

(a)

N=4

(b)

fi=4

D=20

17.

(a)

$$g_u = \frac{4/3}{1} = \frac{4}{3}$$

$$g_d = \frac{4/3}{3} = \frac{4}{9}$$

$$g_{avg} = \frac{4/3 + 4/9}{2} = \frac{8}{9}$$

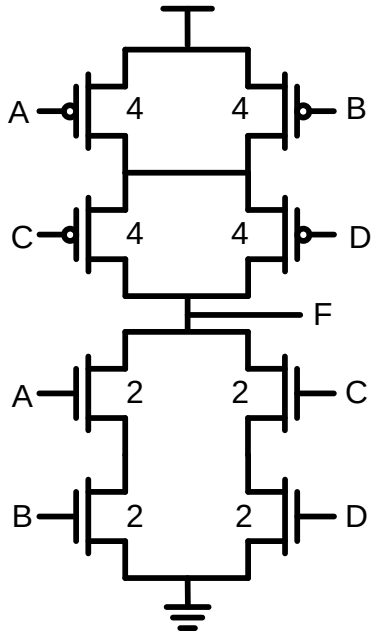
(b)

$$p_u = \frac{4 \times 5/3 + 2/3}{1} = \frac{22}{3}$$

$$p_g = \frac{4 \times 5/3 + 2/3}{3} = \frac{22}{9}$$

$$p_{avg} = \frac{22/3 + 22/9}{2} = \frac{44}{9}$$

18.



(a)2.5% (no partial)

$$g_A = \frac{4+2}{3} = 2$$

$$g_C = \frac{4+2}{3} = 2$$

(b)2.5% (no partial)

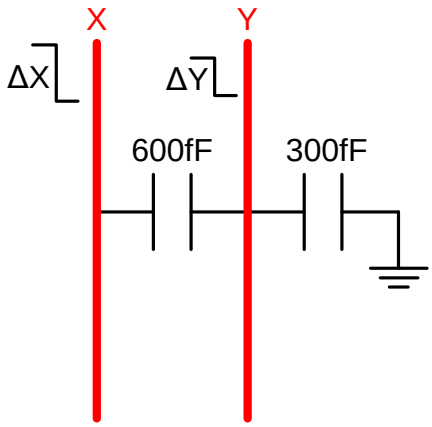
$$p = \frac{4+4+2+2}{3} = 4$$

19.

$R_{inv} = 1k\Omega$
$C_{inv} = 20fF$
$R = 0.2(\Omega/\mu m) \times 1mm = 200\Omega$
$C_{adj} = 0.6(fF/\mu m) \times 1mm = 600fF$
$C_{gnd} = 0.3(fF/\mu m) \times 1mm = 300fF$
(a)
X=0→1, Y=0
$C_{eff} = C_{adj} + C_{gnd} = 900fF$
$T_{pd} = R_{inv} \times C_{inv} + (R + R_{inv}) \times C_{eff} = \mathbf{1.1}\boldsymbol{ns}$

(b)

Y is floating, X=1→0



$$\Delta Y = \Delta X \times \left(\frac{C_{adj}}{C_{adj} + C_{gnd}}\right) = 1 \times \frac{2}{3} = \mathbf{\frac{2}{3}}$$

20.

FFFTFFTFTF (1%per1)

21.

TTFFTTFTFF (1%per1)