$F = \overline{(A+B)\bullet(C+D)}$. (5%)

(a) Sketch the transistor-level schematic. (2.5%)

(b) Sketch the stick diagram. (2.5%)

2. Sketch the transistor-level schematic of the AOI21 gate computing $F = \overline{A \bullet B + C}$: (5%)

(a) Find logical effort g_A, g_B, and g_C. (2.5%)

(b) Find parasitic delay p. (2.5%)

3. Consider the transfer characteristics of CMOS inverter is as shown in Fig. 3. Assume the mobility ratio $\mu_n/\mu_p = 3$, $Vt_n = |Vt_p| = 0.5V$, and the size of nMOS $(W/L)_n = 2um/0.18um$. (5%)

(a) Find the $(W/L)_p$ of curve B. (2.5%)

(b) Rank the noise margins (NM_H and NM_L) of A, B, and C. (2.5%)

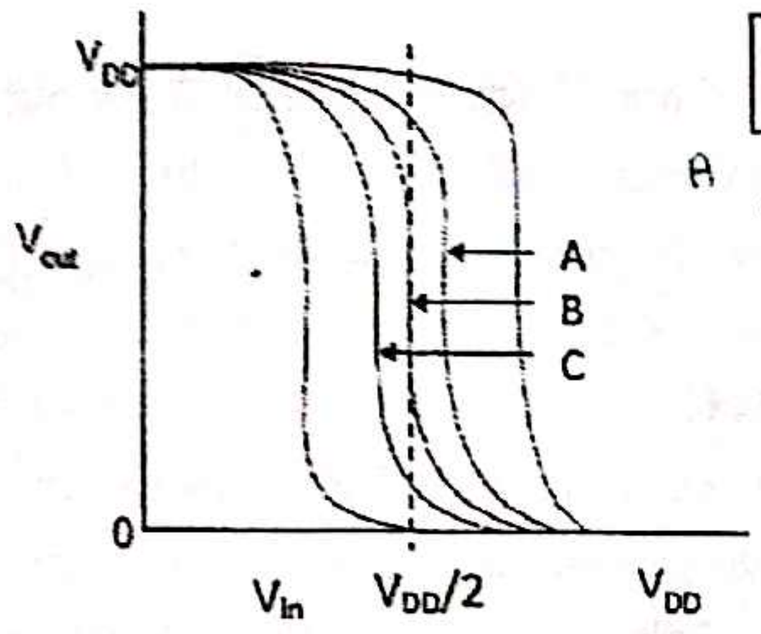

Fig. 3

4. The DC transfer characteristic of inverter is shown as Fig. 4. Please fill the correlated operation regions of nMOS and pMOS into the Table I. (5%)

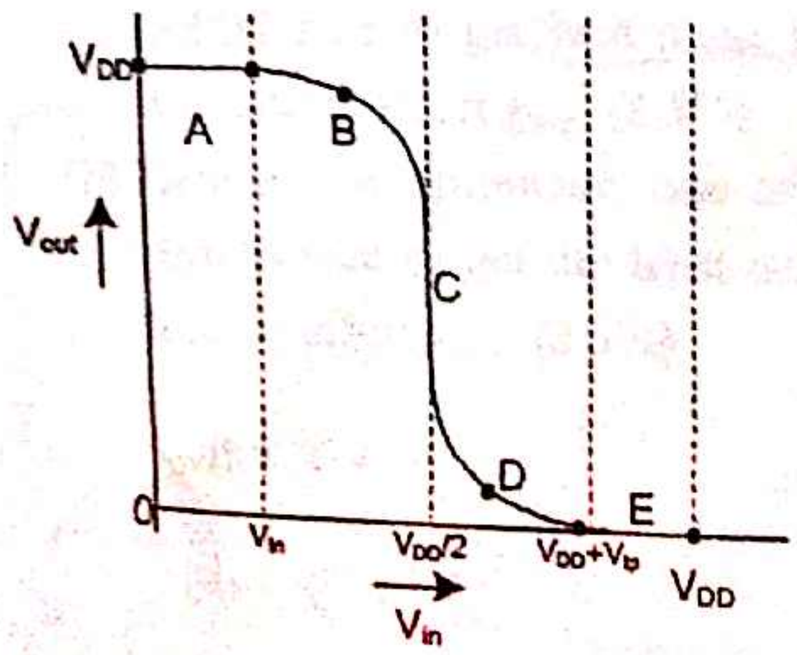

Fig. 4

Region	nMOS	pMOS
A		
B		
C		
D		
E		

5. Please give the correct order of the following steps in IC design flow (a) Layout vs. Schematic check, (b) Size Transistors and Pre-sim (c) Layout (d) Chip Spec Definition (e) (f) Design Rule Check (g) Post simulation (h) Mask Formation (i) Choose Device Technology (j) Architecture define (k) Chip Assembly (l) Parasitic Extraction (m) Chip Verification (5%).

6. Assume there are 7 masks for CMOS inverter manufacturing as (i) diffusion (ii) poly (iii) n+ (iv) p+ (v) well (vi) metal (vii) contact. (5%)

(a) Find the correct order of masks in the process. (2.5%)

(b) Sketch the cross-section of the devices nMOS and pMOS. (2.5%)

7. Suppose $V_{DD} = 1.5V$ and $V_{tn} = 0.5V$. Neglect the body effect; Find V_{out1} and V_{out2} in Fig. 7. (5%)

(a) $V_{in} = 0 \rightarrow 1.2V$. (2.5%)

(b) $V_{in} = 0 \rightarrow 0.9V$. (2.5%)

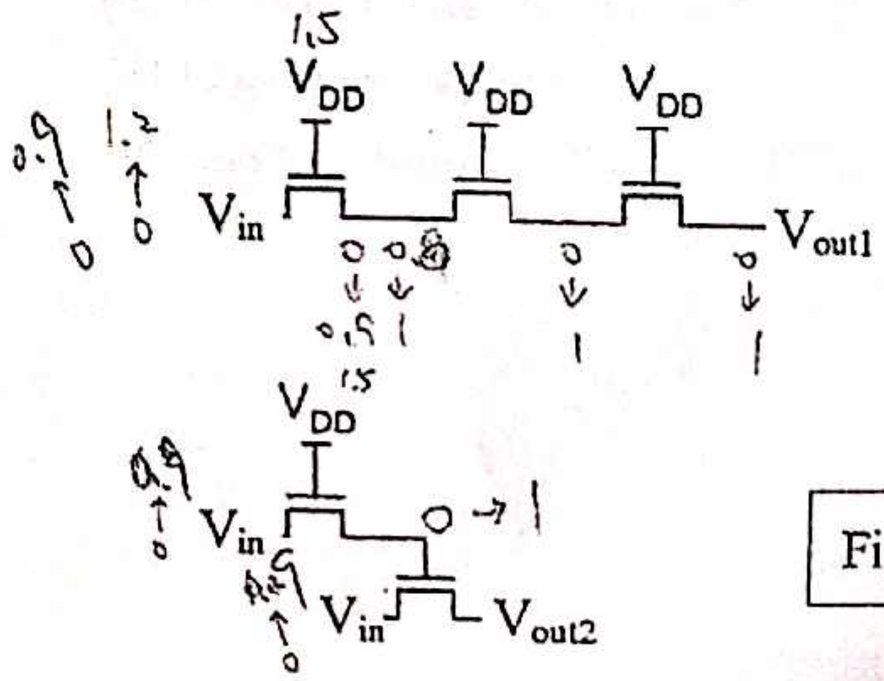

Fig. 7

8. Sketch the stick diagram of CMOS NAND2 with "**smallest**" output parasitic diffusion capacitance. (5%)

9. A ring oscillator composed of N-stages identical inverters is as shown in Fig. 9. Assume the effective resistance of an unit inverter (P:2, N:1) is 1kΩ and parasitic capacitance is 10fF. (5%)
   (a) N = 9, find the oscillated frequency. (2.5%)
   (b) Use skewed inverter and find the oscillated frequency. (2.5%)

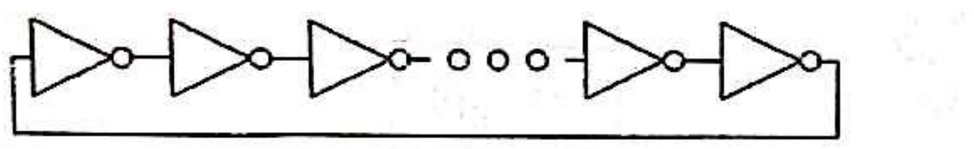

Fig. 9

10. There are 2 adjacent wires X and Y. Each wire in a pair of 1mm lines has capacitance of 0.3 fF/μm to ground and 0.2 fF/μm to its neighbor. The wire resistance is 0.1Ω/μm. Each line is driven by an inverter with a 1kΩ effective resistance and 10fF parasitic capacitance. Use L-model to find the propagation delay of X line with the following conditions. (5%)
   (a) X=0→1, Y=0→1. (2.5%)
   (b) X=1→0, Y=0→1. (2.5%)

11. Consider the design of 3-input NOR gate. (5%)
   (a) Design the optimized size of nMOS and pMOS size to get best noise margin. Find the logical effort g_{avg}. (2.5%)
   (b) Design the optimized size of nMOS and pMOS size to get the least delay. Find the logical effort g_{avg}. (2.5%)

12. Sketch a 2-input (A, B) Hi-Skew NAND gate. Size the devices so that the pull-up is x3 as strong as the pull-down. (5%)
   (a) Estimate the rising, falling and average logical efforts. (2.5%)
   (b) To favor input A by resizing the nMOS to 5/6 as asymmetric gate. By keeping pMOSs unchanged, design the nMOS of input B and find the rising and falling logical efforts. (2.5%)

13. The logic block shown in Fig. 13 has n_1 stages and a path effort of F. Consider adding N-n_1 inverter to the end. Assume the i-th parasitic of logic block is p_i and the parasitic of inverter p_{inv} = 1. **(10%)**
   (a) Express path delay D in terms of N, F, p_i, n_1 and p_{inv}. (5%)
   (b) Find the best stage effort $\rho = F^{1/N}$ to get the least delay D. (5%)

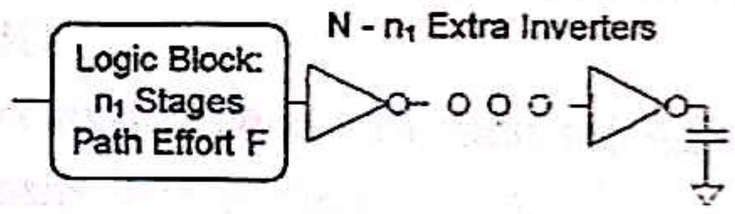

Fig. 13

14. Explain the following terminologies and its purpose about processing technology: **(10%)**
   (a) Salicide. (2%)
   (b) Chemical mechanical polishing. (2%)
   (c) High-K dielectric material. (2%)
   (d) Lightly doped drain. (2%)
   (e) Shallow trench isolation. (2%)

15. Design a 8-input (k=8) AND gat using inverter and pseudo-nMOS NOR gates as shown in Fig. 15. Choose pull-up device size to be 2/3 and the output loading H = 64. **(10%)**

(a) Find the path delay. (5%)

(b) Sketch and label the transistor widths. (5%)

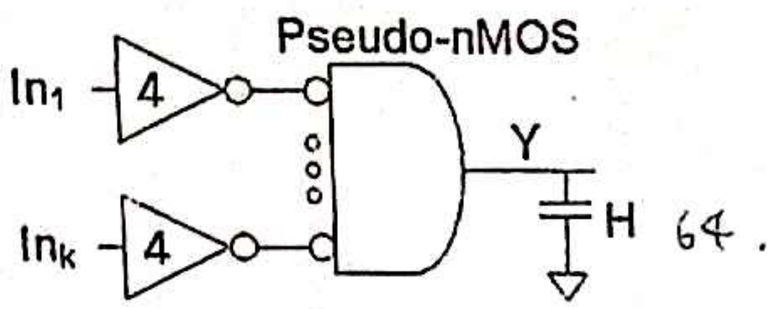

Fig. 15

16. An example logic path is shown as Fig. 16. Design the logic gates to get least path delay from A → C and B→D. **(10%)**

(a) Find the MOS size w, x, y, and z. (5%)

(b) Find the delay from A → D. (5%)

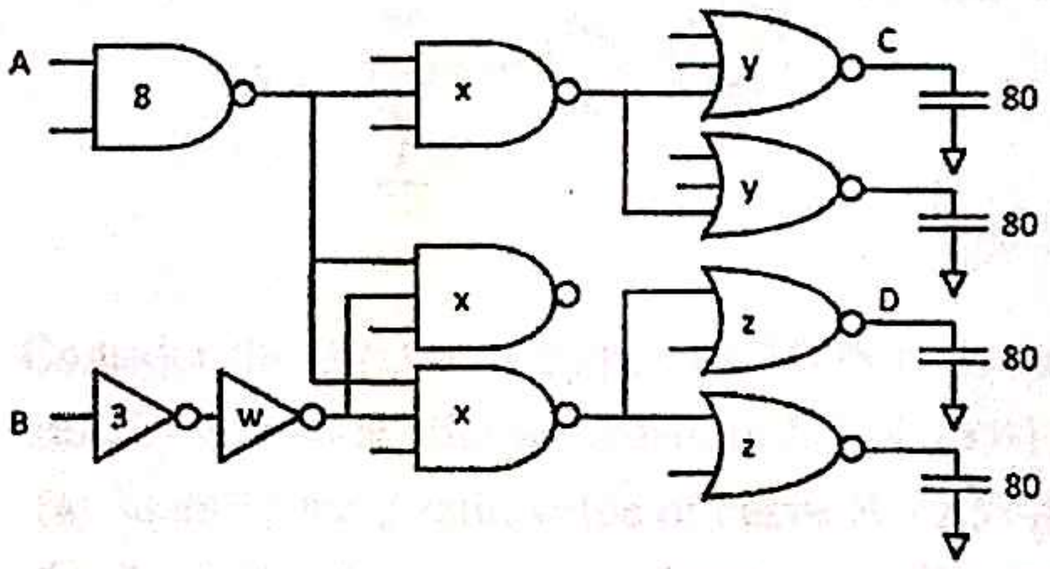

Fig. 16

17. Answer the following questions with TRUE or FALSE: **(10%)**

(a) Copper interconnection is proposed to improve conductivity and routing density. (1%)

(b) FinFET and GAA are proposed to reduce device parasitic and improve speed. (1%)

(c) MOM is better than MIM because it doesn't need extra processing layer. (1%)

(d) Antenna rule violation can be solved by adding protection diode or limiting the maximum metal area connected to gate. (1%)

(e) Stained silicon can be used to increase carrier mobility. (1%)

(f) Velocity saturation becomes worse with shorter channel length and higher V_{DD}. (1%)

(g) Mobility degradation is due to the carrier scattering and reduce channel leakage. (1%)

(h) Electro migration will limit the AC current density in your design. (1%)

(i) Latchup effect can be solved by adding protection diodes around I/O. (1%)

(j) The soft error in Memory can be solved by redundancy and ECC.