2010 VLSI: Final Examination (120%)

1. Consider a dynamic logic (NADN2) as shown in Fig. 1. Assume the $C_a = C_b = 10fF$, $C_L = 20fF$, $C_{gs}(C_{gd})$ of $M_p = 5fF$, and $V_{DD} = 1.8V$. (8%)
   (a) Identify nodes and explain the leakage issue in this circuit and provide the solution add-on circuit. (2%)
   (b) When CLK = 0, A = B = 0, assume all the charge on C_a and C_b are 0. Then, CLK = 0 → 1, find the voltage V_{out}. (2%)
   (c) Continue with (b), then B = 0, A = 0→1. Find the voltage V_{out}. (2%)
   (d) When cascading two identical dynamic NAND2 as shown in Fig. 1 together, explain the possible error issue and solution. (2%) (Hint: monotonic issue)

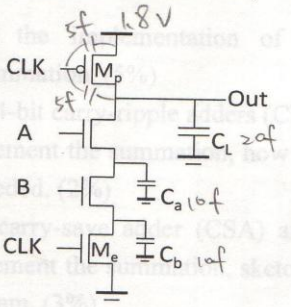


Fig. 1

2. Assign the correct relative timing definition of tA ~ tL in Fig. 2 based on table 1. (12%)

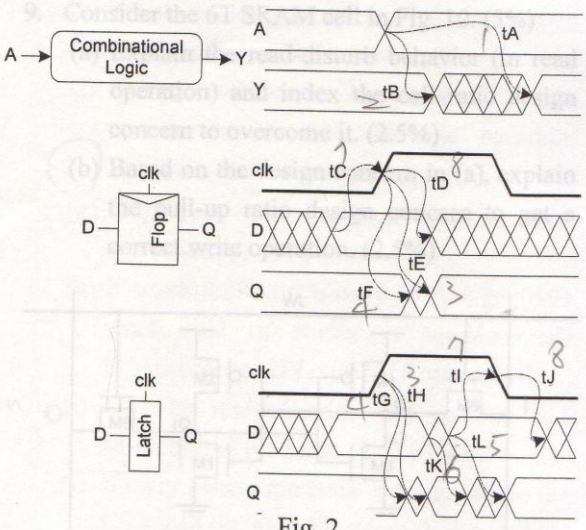


Fig. 2

1	t_{pd}	Logic Prop. Delay
2	t_{cd}	Logic Cont. Delay
3	t_{pcq}	Latch/Flop Clk-Q Prop Delay
4	t_{ccq}	Latch/Flop Clk-Q Cont. Delay
5	t_{pdq}	Latch D-Q Prop Delay
6	t_{pcq}	Latch D-Q Cont. Delay
7	t_{setup}	Latch/Flop Setup Time
8	t_{hold}	Latch/Flop Hold Time

Table. 1

3. A sequential circuit as shown in Fig. 3. Assume the period of clk = T, max clk-to-q delay of F1 = T_{preg}, min clk-to-q delay of F1 = T_{cdreg}, the maximum-delay of combinational logic = t_{plogic}, and the minimum delay = $t_{cdlogic}$. (5%)
   (a) Write the setup time equation. (2.5%)
   (b) Write the hold time equation. (2.5%)

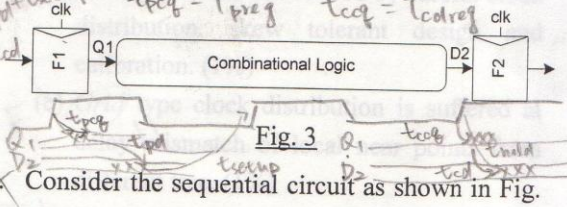


Fig. 3

4. Consider the sequential circuit as shown in Fig. 4. Assume period of $\phi_1 = \phi_2 = 100ns$, $t_{pdq1} = t_{pdq2} = 10ns$, $t_{ccq1} = t_{ccq2} = 6ns$, $t_{nonoverlap} = 5ns$ and the clock skew = 2ns. (5%)
   (a) Find the maximum delay $t_{pd} = t_{pd1} + t_{pd2}$ with and without clock skew. (2.5%)
   (b) Find the mnimum delay t_{cd} min(t_{cd1}, t_{cd2}) with and without clock skew. (2.5%)

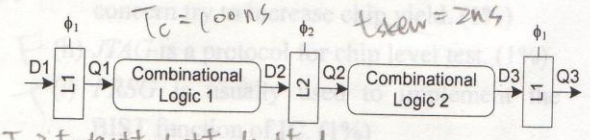
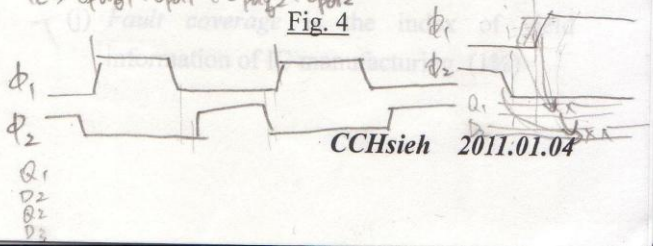


Fig. 4



CCHsieh 2011.01.04

5. Design a 2-phase clock generator. (5%)
   (a) Sketch the schematic. (3%)
   (b) Assume the schematic in (a) has 1ns non-overlap. Please insert a delay element in the schematic to achieve a 4ns non-overlap (2%)

6. Consider a full adder with inputs A and B; carry-in C_{in}, sum S, and carry-out C_{out}. (10%)
   (a) Write the Boolean expressions of sum S and carry-out C_{out} (4%)
   (b) Write the Boolean expression of *Generate* (*G*) and *Propagate* (*P*) signals. (4%)
   (c) Factor S in terms of A, B, C_{in} and C_{out}. Write the Boolean expressions of S. (2%)

7. Consider the implementation of four 4-bit words summation. (5%)
   (a) Use 4-bit carry-ripple adders (CRA) only to implement the summation, how many CRA is needed. (2%)
   (b) Use carry-save adder (CSA) and CRA to implement the summation, sketch the block diagram. (3%)

8. A pass transistor logic is implemented as shown in Fig. 8 with V_{DD} = 1.2V and $|V_{tp}| = |V_{tn}|$ = 0.5V. The inverter (M_1&M_2) has V_{IL} = 0.2V and V_{IH} = 1.0V. Ignore the body effect. (5%)
   (a) A = 0→1.2V, find V_x = ?, V_{out} = ?. (2%)
   (b) Adding a restorer to recover the level V_x to full swing, and assume $R_{on}(M_n)$ = 100ohms, design the minimum R_{on} of restorer to avoid logic 1 fail at V_{out}. (3%)

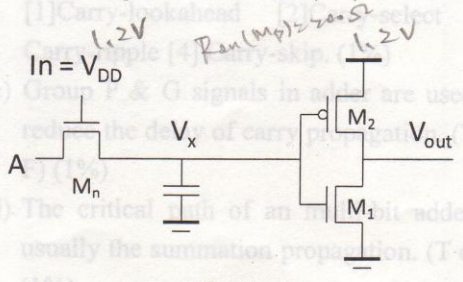


Fig. 8

9. Consider the 6T SRAM cell in Fig. 10. (5%)
   (a) Explain the read-disturb behavior (in read operation) and index the cell ratio design concern to overcome it. (2.5%)
   (b) Based on the design concern in (a), explain the pull-up ratio design concern to get a correct write operation. (2.5%)

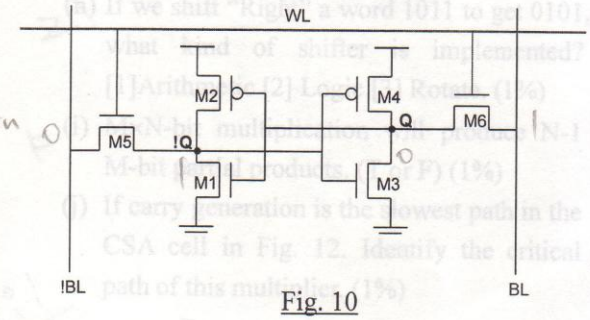


Fig. 10

10. Answer the following questions about Clock Distribution & Testing with TRUE or FALSE: (10%)
   (a) *Jitter* is due to process variation and can be solved by one-time calibration. (1%)
   (b) Clock skew can be reduced by careful clock distribution, skew tolerant design and calibration. (1%)
   (c) *Grid* type clock distribution is suffered at delay mismatch of local near points from different tree. (1%)
   (d) *Skew-tolerant domino logic* is proposed by replacing flip-flops with latches.
   (e) *Design for test* = design circuit to increase fault observability and controllability. (1%)
   (f) *Boundary Scan test* can be used to reduce the probe contacts at board-level test. (1%)
   (g) *Design for manufacturability* is the design concern try to increase chip yield. (1%)
   (h) *JTAG* is a protocol for chip level test. (1%)
   (i) *PRSG* is usually used to implement the BIST function of IC. (1%)
   (j) *Fault coverage* is the index of yield information of IC manufacturing. (1%)

11. Answer the following questions about Memory: (10%)
   (a) Explain the purpose and operation of bit line conditioning circuit and equalization transistor in SRAM. (2%)
   (b) Explain the purpose of sense amplifier and isolation transistor. (2%)
   (c) For a 1T DRAM cell, assume the bit line is precharged to $V_{DD}/2$, the cell capacitance is 100fF, and the bit line capacitance is 1pF. Find the data 0 and 1 voltage level on bit line during readout with V_{DD} = 3.3V. (2%)
   (d) Write down two common methods to improve the yield of memory. (2%)
   (e) What's the 4x4 code in the ROM as shown in Fig. 9. (2%)

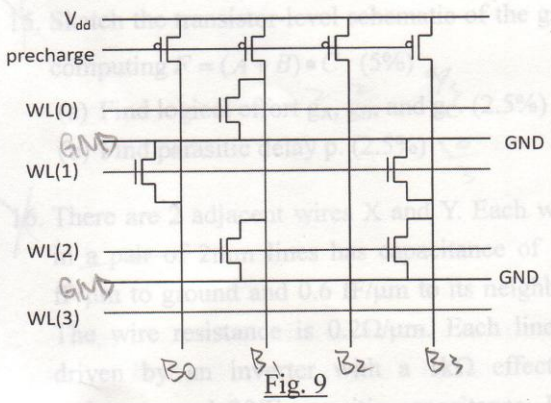


Fig. 9

12. Answer the following questions about Datapath Subsystems (10%)
   (a) Logic levels, fan-in and wiring track are the 3 design-tradeoff corner parameters of tree adder. (T or F) (1%)
   (b) Order the speed of the following adders: [1]Carry-lookahead [2]Carry-select [3] Carry-ripple [4] Carry-skip. (1%)
   (c) Group P & G signals in adder are used to reduce the delay of carry propagation. (T or F) (1%)
   (d) The critical path of an multi-bit adder is usually the summation propagation. (T or F) (1%)
   (e) *Booth encoding* is used to solve the glitch problem in decoder. (T or F) (1%)
   (f) *Subtraction* can be implemented by 2's complement as the following equation: $A - B = A + \overline{B} + 1$ (T or F) (1%)
   (g) *Gray code* is a common skill for error correction. (T or F) (1%)
   (h) If we shift "Right" a word 1011 to get 0101, what kind of shifter is implemented? [1]Arithmetic [2] Logic [3] Rotate. (1%)
   (i) M×N-bit multiplication will produce N-1 M-bit partial products. (T or F) (1%)
   (j) If carry generation is the slowest path in the CSA cell in Fig. 12. Identify the critical path of this multiplier. (1%)

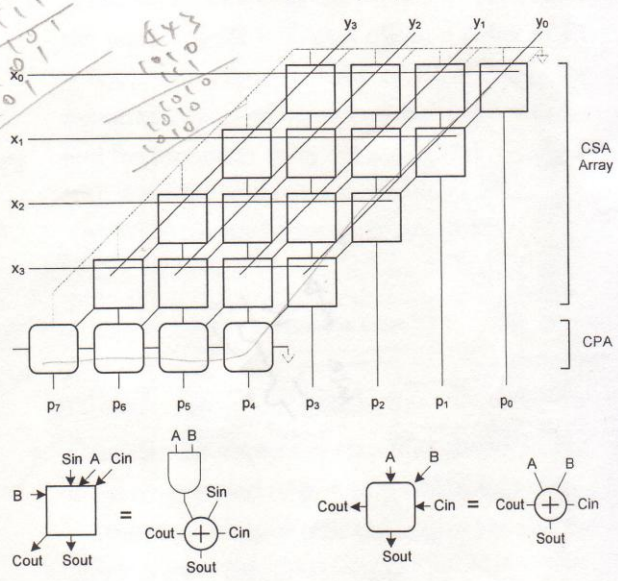


Fig. 12

13. An output pad contains a chain of successively larger inverters to drive the off-chip 40pF loading capacitance. If the first inverter in the chain has an input capacitance of 10fF, (5%)
   (a) Find the optimized stage number N of inverters. (2.5%)
   (b) Find the smallest delay D_F = ? FO4 inverter delay (2.5%)

14. A ring oscillator composed of N-stages identical inverter is as shown in Fig. 9. Assume the effective resistance of an unit inverter (P:2, N:1) is 200Ω and parasitic capacitance is 5fF. (5%)
    (a) N = 5, find the oscillated frequency. (2.5%)
    (b) Use skewed inverter and find the oscillated frequency. (2.5%)

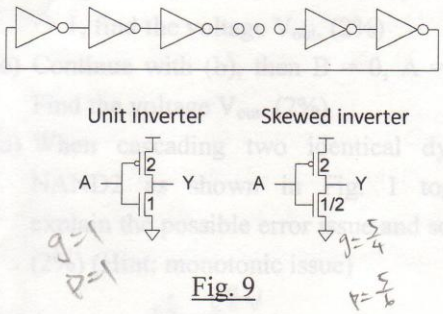


Fig. 9

15. Sketch the transistor-level schematic of the gate computing $F = \overline{(A+B)\bullet C}$: (5%)
    (a) Find logical effort g_A, g_B, and g_C. (2.5%)
    (b) Find parasitic delay p. (2.5%)

16. There are 2 adjacent wires X and Y. Each wire in a pair of 2mm lines has capacitance of 0.4 fF/μm to ground and 0.6 fF/μm to its neighbor. The wire resistance is 0.2Ω/μm. Each line is driven by an inverter with a 1kΩ effective resistance and 20fF parasitic capacitance. Use L-model to find the propagation delay of X line with the following conditions. (5%)
    (a) X=0→1, Y=0. (2.5%)
    (b) X=0→1, Y=1→0. (2.5%)

17. Design a 6-input (k=6) AND gate using inverter and pseudo-nMOS NOR gates as shown in Fig. 17. Choose pull-up device size to be 2/3 and the output loading H = 60. (**10%**)
    (a) Find the path delay. (5%)
    (b) Sketch and label the transistor widths. (5%)

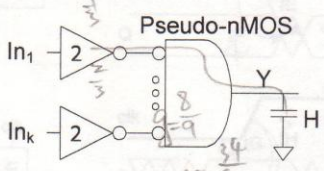


Fig. 17