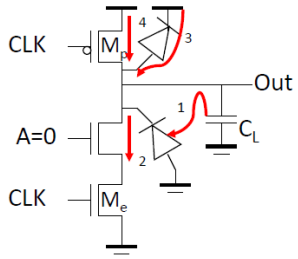
2010 VLSI Final Examination Solution

1.

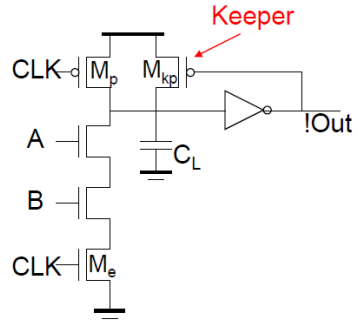
(a) 2%



Leakage sources → 0.5%

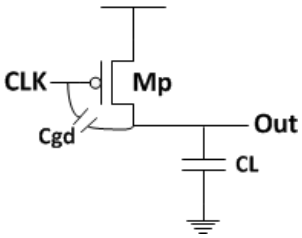
Due to charge leakage, output settles to an output settles to an intermediate voltage determined by a resistive divider of the pull-up and pull-down networks. Once the output drops below the switching threshold of the fan-out logic gate, the output is interpreted as a low voltage. (0.5%)

Solution: (1%)



Keeper compensates for the charge lost due to the pull-down leakage paths.

(b) 2%



$1.8 \times (20 + 5) = (Vx - 1.8) \times 5 + 20Vx$

$\rightarrow 25Vx = 54 \therefore Vx = 2.16V$

Ans: 2.16V

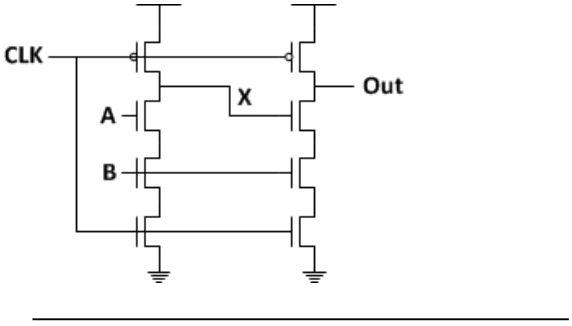
(c) 2%

$2.16 \times 20 = Vy \times (20 + 10)$

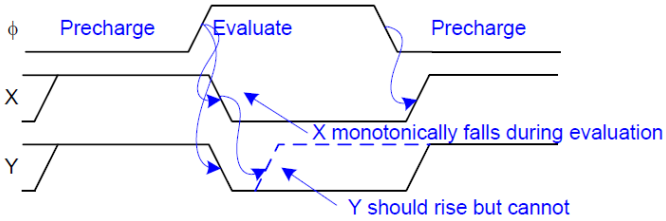
→ Vy = 1.44V

Ans: 1.44V

(d) 2%

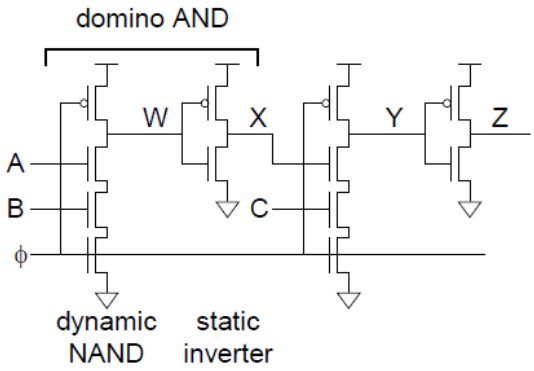


A,B=1



Dynamic gates require monotonically rising inputs during evaluation. (1%)

Solution:



(1%)

2.

Tpd(1)	**A**
Tcd(2)	**B**
Tpcq(3)	**E,H**
Tccq(4)	**F,G**
Tpdq(5)	**L**
Tcdq(6)	**K**
Tsetup(7)	**C,I**

Thold(8)	D,J

A➔1	**G➔4**
B➔2	**H➔3**
C➔7	**I➔7**
D➔8	**L➔8**
E➔3	**K➔6**
F➔4	**L➔5**

一格一分

3.

(a) 2.5%

$T_{\text{setup}} \leq \text{T} - \text{T}_{\text{preq}} - \text{t}_{\text{plogic}}$

(b) 2.5%

$T_{\text{hold}} \leq \text{T}_{\text{cdreq}} + \text{t}_{\text{cdlogic}}$

4.

(a) 2.5%(1.5% for only one correct)

With and without skew (skew-tolerant):

$t_{pd} \leq T_C - (t_{pdq1} + t_{pdq2}) = 100ns - 2 \times 10ns = 80ns$

(b) 2.5% (1.5% for only one correct)

Without skew:

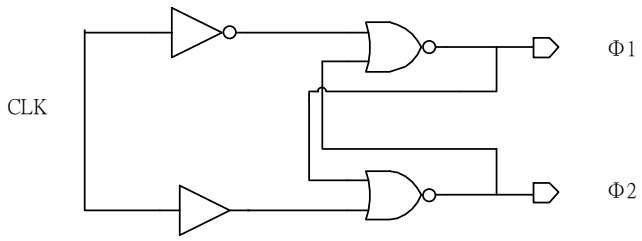
$t_{cd} \geq T_{hold} - t_{ccq} - t_{nonoverlap} = T_{hold} - 6ns - 5ns = T_{hold} - 11ns$

With skew:

$t_{cd} \geq T_{hold} - t_{ccq} - t_{nonoverlap} + t_{skew} = T_{hold} - 6ns - 5ns + 2ns = T_{hold} - 9ns$

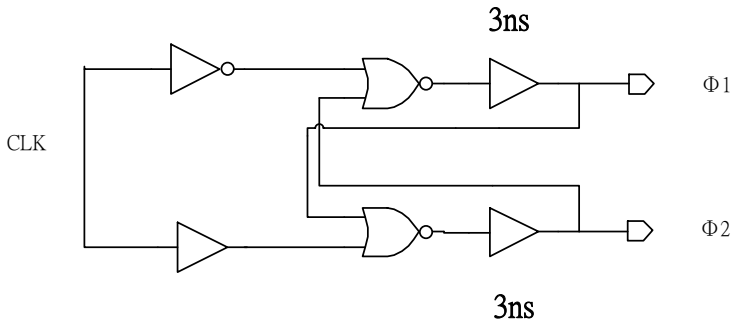
5.

(a)



3%

(b)



2%

6.

(a)

S=A⊕B⊕Cin 2%

Cout=MAJ(A,B,Cin)=AB+BC+CA=AB+Cin(A⊕B) 2%

(b)

G=AB 2%

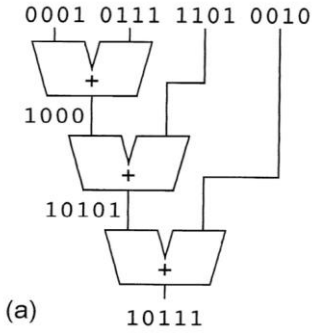
P=A⊕B 2%

(c)

S=ABCin+(A+B+Cin)(~Cout) 2%

7.

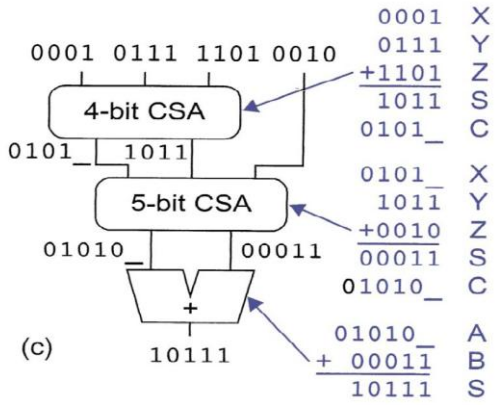
(a) 2%



Ans: 3

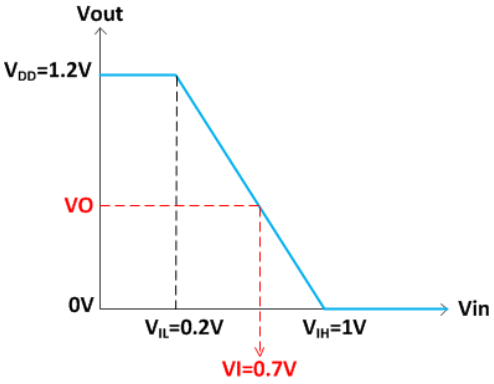
(b) 3%

Ans:



8.

(a) 2% (1% for each)



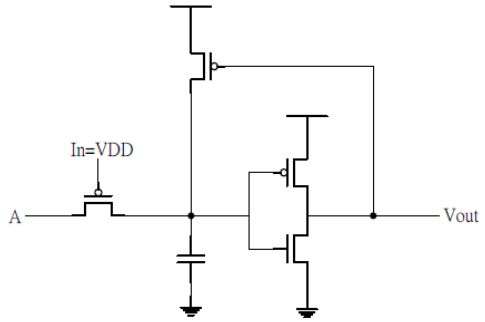
$$VO = (1 - 0.7) \times \frac{1.2 - 0}{1 - 0.2} = 0.45V$$

Ans:

Vx = 0 → 0.7V

Vout = 1.2 → 0.45V

(b) 3%



$$1.2 \times \frac{100}{100 + Ron} \leq 0.2 \rightarrow \text{Ron} \geq 500 \text{ (ohms)}$$

Ans: 500ohms

9.

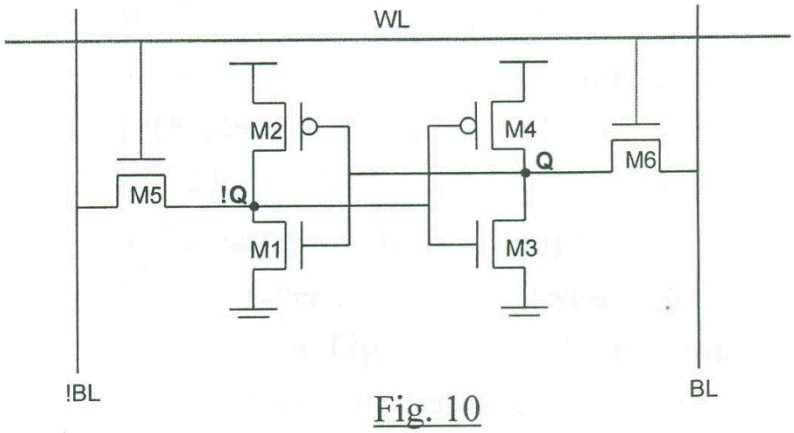


Fig. 10

(a)

Read disturb:

Assume Q=0, during the read operation:

∵ BL is precharged at VDD.

∴ Q will rise due to voltage devision.

$V_{rise} = \frac{R_{PD}}{R_{PD}+R_{PG}}$ 愈小愈好。

$\begin{cases} R_{PD} \propto \frac{1}{(\frac{W}{L})_{PD}} \\ R_{PG} \propto \frac{1}{(\frac{W}{L})_{PG}} \end{cases} \rightarrow \frac{(\frac{W}{L})_{PD}}{(\frac{W}{L})_{PD}} \uparrow \quad V_{rise} \downarrow$ 2.5%

(b)

Write:

寫入"0"時，pass-gate NMOS，要和 pull-up PMOS 競爭，PG 需較強，假設 mobility 一樣，$(\frac{W}{L})_{PG} > (\frac{W}{L})_{PU}$。 2.5%

10.

(a)F (b)T (c)F (d)T (e)T (f)T (g)T (h)F (i)T (j)F 1%each

11.

(a) 2%(1% for each)

Bitline conditioning: Precharge bitlines high before reads.

Equalization transistor: Equalize bitlines to minimize voltage difference when using sense amplifier.

(b) 2%(1% for each)

Sense amplifier: It's invented to provide faster sensing by responding to a small voltage swing.
Isolation transistors: To Cut off large bitline capacitance when sense amplifier works.

(c) 2%(1% for each)

$$\Delta V = \frac{VDD}{2}\frac{Ccell}{Ccell + Cbit} = 1.65 \times \frac{0.1}{1 + 0.1} = 0.15V$$

Ans:

Data 0: $1.65 - 0.15 = 1.5V$

Data 1: $1.65 + 0.15 = 1.8V$

(d) 2%(1% for each)

Add dummy lines: The dummy lines are placed at the edge because photolithography and etch problems occur most often near the edge of large repetitive structure.
ECC: Error-detecting and correcting codes are commonly used to recover from soft errors that spontaneously flip a bit store in one of the cell.
BIST: Built-in self-test that place multiplexers in the address and data paths to take over the memory during test mode.

(e) 2%(No partial)

Ans:

	B0	B1	B2	B3
WL0	1	0	1	1
WL1	0	1	1	0
WL2	1	0	1	0
WL3	1	1	1	1

(Exactly correct answers for ROM)

$B0 = \overline{WL(1)}$

$B1 = \overline{WL(0) + WL(2)}$

$B2 = 1$

$B3 = \overline{WL(1) + WL(2)}$

(These answers are also acceptable.)

12.

(a)

[False] 1%

∵Logic level、fan-out、wire track。

(b)

2➔1➔4➔3 1%

(c)

[True] 1%

(d)

[False] 1%

(e)

[False] 1%

(f)

[True] 1%

(g)

[False] 1%

(h)

[2] 1%

(i)

[False] 1%

(j)

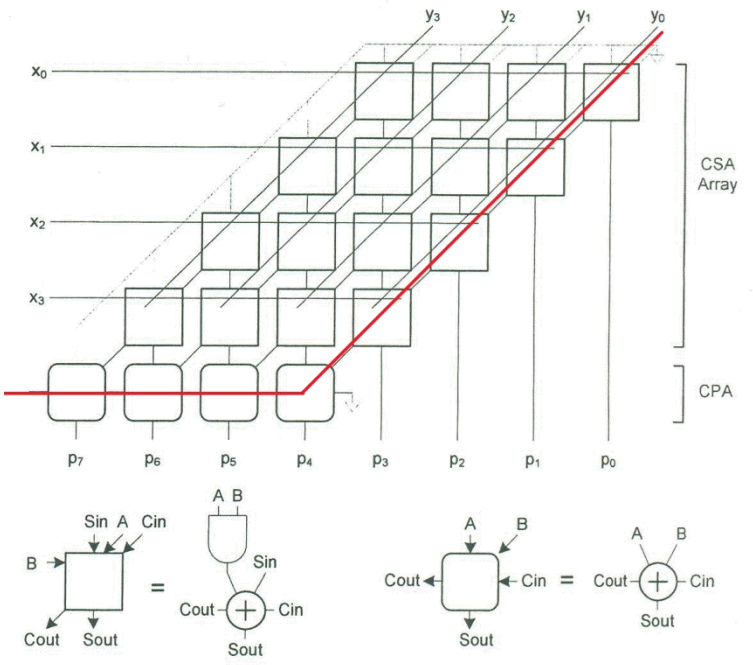


Fig. 12 1%

13.

G=1，B=1，H=40pF/10fF=4000

F=GBH=4000

(a) 2.5%

$D_F = N \times \sqrt[N]{F}$

N	D_F
4	31.81
5	26.27
6	23.91
7	22.89
8	22.56
9	22.62

(b) 2.5%

D_F=22.56/5=4.512FO_4

14.

(a) 2.5%

D_F=gh+p=2

$$f_{osc} = \frac{1}{2Nd} = \frac{1}{2 \times 5 \times 2 \times RC} = \frac{1}{2 \times 5 \times 2 \times 200 \times 5f} = 50GHz$$

(b) 2.5%

$$\begin{cases} g_u = \dfrac{2+\frac{1}{2}}{2+1} = \dfrac{5}{6} \\ g_d = \dfrac{2+\frac{1}{2}}{1+\frac{1}{2}} = \dfrac{5}{3} \end{cases}, g_{AVG} = \frac{g_u + g_d}{2} = \frac{5}{4}$$

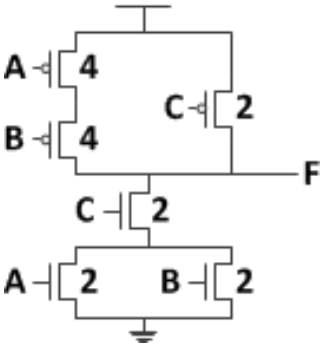
D_F=gh+p=5/4+5/4=5/2

$$f_{osc} = \frac{1}{2Nd} = \frac{1}{2 \times 5 \times \frac{5}{2} \times RC} = \frac{1}{2 \times 5 \times \frac{5}{2} \times 200 \times 5f} = 40GHz$$

15.

Ans:

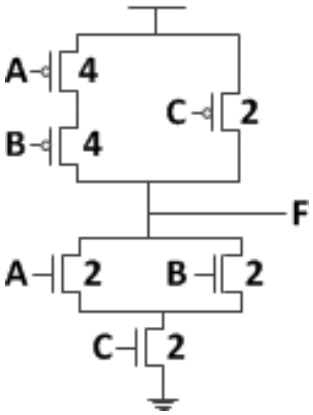
Method (1):

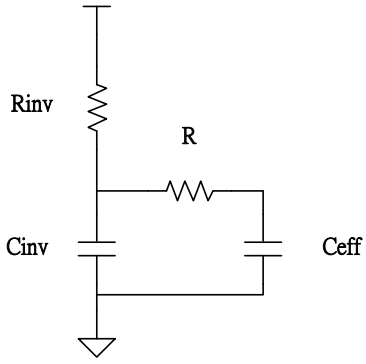


(a) $gA = \frac{4+2}{3} = 2, gB = \frac{4+2}{3} = 2, gC = \frac{2+2}{3} = \frac{4}{3}$ (2.5% No partial)

(b) $P = \frac{4+2+2}{3} = \frac{8}{3}$ (2.5%)

Method (2):





(a) $gA = \frac{4+2}{3} = 2, gB = \frac{4+2}{3} = 2, gC = \frac{2+2}{3} = \frac{4}{3}$ (2.5%)

(b) $P = \frac{4+2+2+2}{3} = \frac{10}{3}$ (2.5%)

16.

R_{inv}=1kΩ，C_{inv}=20fF，R=0.2X2000=400Ω

C_{adj}=0.6X2000=1.2pF，C_{gnd}=0.4X2000=0.8pF

(a) X=0➔1，Y=0

$C_{eff}=C_{gnd}+C_{adj}$

$T_{pd}=R_{inv}C_{inv}+(R+R_{inv})C_{eff}$=2820ps 2.5%

(b) X=0➔1，Y=1➔0

$T_{pd}=R_{inv}C_{inv}+(R+R_{inv})C_{eff}$=4500ps 2.5%

17.

(a) 5%(No partial)

Find gavg:

$$\text{gu} = \frac{\frac{4}{3}}{\frac{2}{3}+\frac{1}{3}} = \frac{4}{3}$$

$$\text{gd} = \frac{\frac{4}{3}}{2+1} = \frac{4}{9}$$

$$\text{gavg} = \frac{\frac{4}{3}+\frac{4}{9}}{2} = \frac{8}{9}$$

Find pavg:

$$\text{pu} = \frac{6\times\frac{4}{3}+\frac{2}{3}}{\frac{2}{3}+\frac{1}{3}} = \frac{26}{3}$$

$$\text{pd} = \frac{6\times\frac{4}{3}+\frac{2}{3}}{2+1} = \frac{26}{9}$$

$$\text{pavg} = \frac{\frac{26}{3}+\frac{26}{9}}{2} = \frac{52}{9}$$

Find path delay:

$$\text{G} = 1\times\frac{8}{9} = \frac{8}{9}$$

$$\text{F} = \text{GBH} = \frac{8}{9}\times 1\times\frac{60}{2} = \frac{80}{3}$$

$$\text{P} = 1+\frac{52}{9} = \frac{61}{9}$$

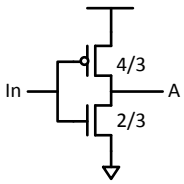
$$\text{N} = 2$$

$$\text{D} = 2\times\sqrt{\frac{80}{3}}+\frac{61}{9} = \frac{61+24\sqrt{15}}{9} = 17.106$$

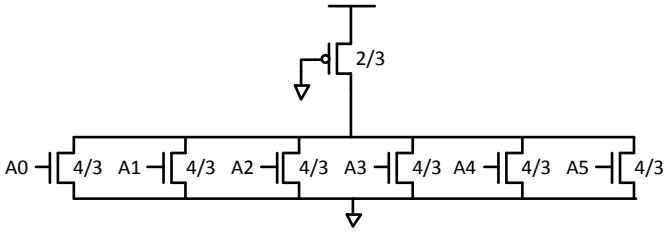
Ans: 17.106 (Time Unit)

(b) 5%

Ans 1:

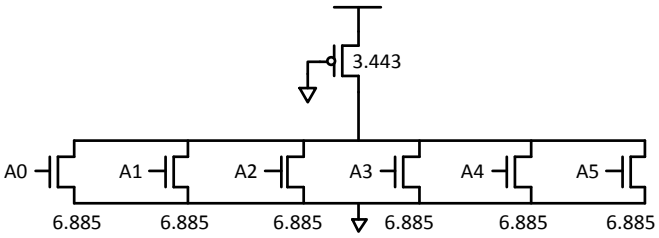


(0%)



Ans 2:

$$f = \sqrt{F} = \sqrt{\frac{80}{3}} = gh = \frac{8}{9} \times \frac{60}{x}$$



$$\rightarrow x = 10.328$$

$$\text{PMOS: } 10.328 \times \frac{\frac{2}{3}}{\frac{2}{3}+\frac{4}{3}} = 3.443$$

$$\text{NMOS: } 10.328 \times \frac{\frac{4}{3}}{\frac{2}{3}+\frac{4}{3}} = 6.885$$