1. Consider the design of a CMOS compound OR-AND-INVERT (OAI21) gate computing $F = \overline{(A+B)\bullet C}$. (5%)
   (a) Sketch the transistor-level schematic. (2.5%)
   (b) Sketch the stick diagram. (2.5%)

2. Sketch a transistor-level schematic for a single-stage CMOS logic gate for each of the following functions: (5%)
   (a) $Y = \overline{(AB+C)\bullet D}$ (2.5%)
   (b) $Y = \overline{AB+C\bullet(A+B)}$ (2.5%)

3. Suppose V_{DD} = 1.5V and $|V_{tp}| = V_{tn}$ = 0.5V. Neglect the body effect, determine V_{out} in Fig. 3 for: (5%)
   (a) V_{in} = 1.5→0.3V. (2.5%)
   (b) V_{in} = 1.5→0.9V. (2.5%)

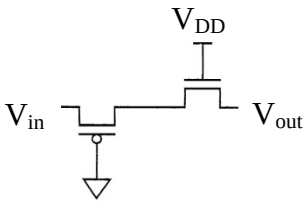

Fig. 3

4. Consider the β ratio as β_p/β_n of CMOS inverter transfer characteristics as shown in Fig. 4. (5%)
   (a) Identify the β ratio value of curve B. (2.5%)
   (b) Rank the β ratio order of curves A, B, and C. (2.5%)

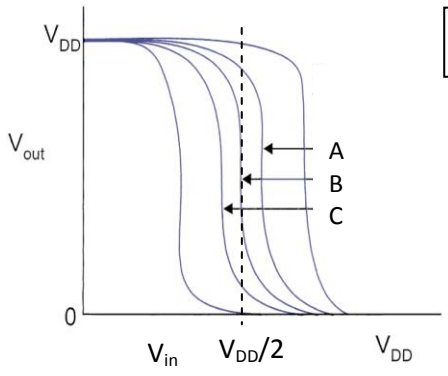

Fig. 4

5. The transfer characteristic of inverter is shown as Fig. 5. (5%)
   (a) Find the V_{IL}, V_{OL}, V_{IH}, and V_{OH}. (3%)
   (b) Find the NM_H and NM_L. (2%)

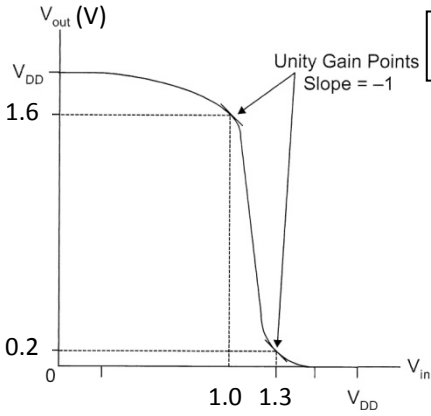

Fig. 5

6. Write down the 3 operation regions of MOS transistor and related ideal I-V equations. (5%)

7. Answer the following questions about MOS characteristics with TRUE or FALSE: (10%)
   (a) C_{gs} is larger than C_{gd} at Saturation. (1%)
   (b) C_g (gate capacitance) at Saturation is larger than that at Linear region. (1%)
   (c) Source/Drain junction capacitance is proportional to channel area. (1%)
   (d) Velocity saturation becomes worse with shorter channel length and lower V_{DD}. (1%)
   (e) Mobility degradation is due to the strong vertical electric field from V_{gs}. (1%)
   (f) The positive V_{sb} will increase V_t of nMOS. (Body effect) (1%)
   (g) Tunneling becomes worse at thinner gate oxide and lower VDD, and it causes gate leakage. (1%)
   (h) MOS ON current I_{dsat} is decreased with higher temperature T. (1%)
   (i) Junction leakage is worse than subthreshold leakage at modern technology. (1%)
   (j) The finite output resistance of MOS at Saturation region is proportional to channel length. (1%)

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8. Answer the following questions about MOS process enhancement with TRUE or FALSE: (10%)
   (a) Thinner gate oxide at advanced technology is used to decrease leakage current. (1%)
   (b) High-K gate dielectric can increase channel charge without thinning gate oxide. (1%)
   (c) FinFET is used to decrease the subthreshold leakage of advanced transistor. (1%)
   (d) Silicon-on-Insulator (SOI) can increase device speed, but with higher subthreshold leakage. (1%)
   (e) SOI is suffered to the floating body voltage (history effect). (1%)
   (f) Multiple threshold voltage devices need different oxide thickness and are used to provide speed tradeoff. (1%)
   (g) Copper interconnect development is mainly due to its low parasitic capacitance and thickness. (1%)
   (h) CMP is used to planarize the inter-layer isolation structure for multi-layer inter-connects stacking. (1%)
   (i) Salicide is used to reduce the S/D and gate resistance. (1%)
   (j) LDD is used to reduce S/D junction leakage. (1%)

9. Each wire in a pair of 2mm lines has capacitance of 0.2 fF/μm to ground and 0.1 fF/μm to its neighbor. The wire resistance is 0.1Ω/μm. Each line is driven by an inverter with a 1kΩ effective resistance and 5fF parasitic capacitance. Find the contamination and propagation delay. (5%)

10. A three-stage logic path is designed so that the effort borne by each stage is 14, 5, 8 delay units, respectively. (5%)
    (a) Find the optimized stage number N. (2.5%)
    (b) Find the smallest path delay D_F. (2.5%)

11. An output pad contains a chain of successively larger inverters to drive the off-chip 10pF loading capacitance. If the first inverter in the chain has an input capacitance of 20fF, (5%)
    (a) Find the optimized stage number N of inverters. (2.5%)
    (b) Find the smallest delay D_F = ? FO4 inverter delay (2.5%)

12. Design a 3-input LO-skew NOR gate. Size the devices so that the pull-down is x2 as strong as the pull-up. (5%)
    (a) Sketch and label the transistor widths. (2.5%)
    (b) Estimate the rising, falling and average logical efforts. (2.5%)

13. Design a pseudo-nMOS 3-input NOR gates. Choose pull-up device size to be 2/3. (5%)
    (a) Sketch and label the transistor widths. (2.5%)
    (b) Estimate the rising, falling and average logical efforts. (2.5%)

14. Design a 3-input footed dynamic NAND gate driving an electrical effort of 1. The pull-down transistors' widths are chosen to give unit resistance. Estimate the worst charge sharing noise as a fraction of V_{DD} assuming that diffusion capacitance on uncontacted nodes is about half of gate capacitance and on contacted node it equals gate capacitance. (5%)

15. As shown in Fig. 15, the input loading of A is 10 and output loading of Z is 160 units. (10%)
    (a) Sketch the logic by domino gates and footed dynamic circuits. (5%)
    (b) Find the path delay (A-Z) D_F. (5%)

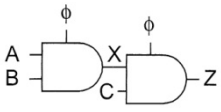

Fig. 15

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16. An example logic path is shown as Fig. 16. The input loading of A is 10 and output loading of B is 60. (10%)
    (a) Estimate the minimum delay of the path from A to B. (5%)
    (b) Find the transistor sizes (nMOS & pMOS) of each gate. (5%)

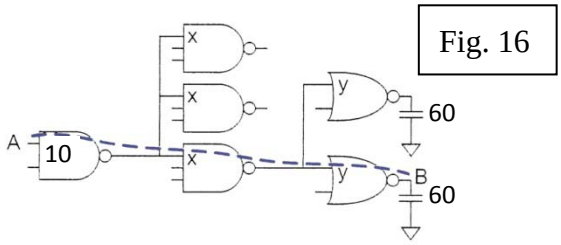

Fig. 16

17. Answer the following questions about circuit family property with TRUE or FALSE: (10%)
    (a) Pseudo-nMOS can improve the logical effort of static gates. (1%)
    (b) Dynamic circuit is used to decrease static power of pseudo-nMOS. (1%)
    (c) Secondary precharge devices are used to improve speed. (1%)
    (d) HI-skewed gate will favor the pull-down devices. (1%)
    (e) The best P/N ratio for logic gates is 2 to get the lowest average delay. (1%)
    (f) Domino logic is used to provide both true and complementary outputs. (1%)
    (g) Keepers in dynamic logic are used to restore the disturbed output level from leakage. (1%)
    (h) LO-skew inverter is favored in Domino logics. (1%)
    (i) For a multiple input logic, the slower input should be connected to outer node to get smaller delay. (1%)
    (j) Pass transistor logic is suffered from threshold drop and leakage as well. (1%)