2009 VLSI: Final Examination (124%)

1. Consider the design of a CMOS single-bit full adder, assume the inputs are A, B and C_{in} (Carry-in) (6%)
   (a) Write the Boolean expressions of sum S and carry out C_{out}. (2%)
   (b) Write the Boolean expression of *Generate* (*G*) and *Propagate* (*P*) signals. (2%)
   (c) Sketch the transistor-level schematic of this full adder. (2%)

2. For a 3 bits carry-ripple adder using the PG logic: (8%)
   (a) Write the Boolean expression of $G_{i:0}$ (in terms of $G_{i-1:0}$, G_i and P_i) (2%)
   (b) Write the Boolean expression of C_i in term of G_i, P_i and C_{i-1}.(2%)
   (c) Sketch the gate-level schematic of this 3 bits adder. (2%)
   (d) What is the critical path of this adder? (2%)

3. Answer the following questions about Datapath Subsystems with TRUE or FALSE: (10%)
   (a) Carry-lookahead is faster than Carry-select adder, and Carry-ripple is slowest. (1%)
   (b) Carry-in signal should be fed into the inner input of logic gates.
   (c) The critical path of an adder is the carry generation and propagation.
   (d) Logic levels, fanout and wiring track are the 3 design-tradeoff corner parameters of tree adder. (1%)
   (e) An *equality comparator* determines if ($A = B$), and can be implemented with XOR gates and 1's detector. (1%)
   (f) *Parity check* is commonly used to do the data error-detection and correction.
   (g) *Gray code* is better than *binary code* in decoder for no glitch and low power. (1%)
   (h) *Logical shifter* will shift the number to the left or right, and the empty spots are filled with bits shifted off the other end. (1%)
   (i) Carry-save adder accepts 3 inputs and produces 2 outputs, it is faster than the carry-propagate adder. (1%)
   (j) Subtraction can be implemented by 2's complement as the following equation: $A - B = A + \overline{B}$ (1%)

Using the following timing parameters for the questions 4-11:

	Setup time	Clk-to-Q delay	D-to-Q delay	Contamination delay	Hold time
Flip-flops	60ps	55ps	n/a	40ps	30ps
Latches	20ps	45ps	40ps	40ps	25ps

4. With clock skew = 0, for each of the following sequencing types, determine the maximum logic propagation delay available within 300ps clock cycle: (6%)
   (a) Flip-flops (2%)
   (b) Two-phase transparent latches (2%)
   (c) Pulsed latched with 70ps pulse width (2/%)

5. Repeat question 4, if the clock skew between any two elements is up to 40ps. (6%)
   (a) Flip-flops (2%)
   (b) Two-phase transparent latches (2%)
   (c) Pulsed latched with 70ps pulse width (2/%)

6. With clock skew = 0, for each of the following sequencing types, determine the minimum logic contamination delay in each clock cycle: (6%)
   (a) Flip-flops (2%)
   (b) Two-phase transparent latches with 60ps of nonoverlap between phases (2/%)
   (c) Pulsed latched with 80ps pulse width (2%)

7. Repeat question 6, if the clock skew between any two elements is up to 40ps. (6%)
   (a) Flip-flops (2%)
   (b) Two-phase transparent latches with 60ps of nonoverlap between phases (2/%)
   (c) Pulsed latched with 80ps pulse width (2%)

8. Suppose one cycle of logic is particularly critical and the next cycle is nearly empty. Determine the maximum amount of time the first cycle can borrow into the second for each of the following sequencing styles. (6%)
   (a) Flip-flops (2%)
   (b) Two-phase transparent latches with 50ps of nonoverlap between phases (2/%)
   (c) Pulsed latched with 70ps pulse width (2%)

9. Determine the maximum logic propagation delay available in a cycle for a traditional domino pipeline using a 400ps clock cycle. Assume the clock skew is 40ps. (5%)

10. Determine the maximum logic propagation delay in a cycle for a 4-phase skew-tolerant domino pipeline using a 600ps clock cycle with a 60ps skew. (5%)

11. How much time can one phase borrow into the next in question 10 if the clock has a 60% duty cycle. (5%)

12. Answer the following questions about Clock Distribution & Testing with TRUE or FALSE: (10%)
   (a) *Drift* clock skew is due to process variation and can be solved by one-time calibration. (1%)
   (b) Clock jitter is due to the high frequency environment variation and cannot be calibrated. (1%)
   (c) Clock skew can be reduced by careful clock distribution, skew tolerant design and smaller metal wire routing area. (1%)
   (d) *Grid* type clock distribution is suffered at random skew between points closet and furthest to the driver. (1%)
   (e) *H-Tree* type clock distribution is suffered at delay mismatch of local near points from different tree. (1%)
   (f) *Design for test* = design circuit to increase fault observability and controllability. (1%)
   (g) *Boundary Scan test* can be used to decrease the probe contacts at wafer test stage. (1%)
   (h) *Design for manufacturability* is the design concern try to increase chip yield. (1%)
   (i) *Built-in Self-Test* (BIST) can reduce the test cost and die area as well. (1%)
   (j) *Electron-beam* (ebeam), *Laser Voltage Probe* (LVP), and *Focused Ion Beam* (FIB) are all debugging methods without mechanical contacts. (1%)

13. For a 1T DRAM cell, assume the bitline is precharged to $V_{DD}/2$, the cell capacitance is 0.1pF, and the bit line capacitance is 5pF. Find the data 0 and data 1 voltage level on the bit line during readout with $V_{DD} = 3.3$V. (5%)

14. Answer the following questions about Memory with TRUE or FALSE: (10%)
   (a) SRAM and DRAM are nonvolatile and ROMs are volatile memory. (1%)
   (b) SRAM column circuit includes bitline conditioning, sense amplifier, and row decoders. (1%)
   (c) Bitline conditioning is used to precharge both bit and bit_b data to be V_{DD}. (1%)
   (d) Equalizer and twisting bitline can be used to reduce the noise coupling. (1%)
   (e) Compared to SRAM, DRAM has higher density and noise coupling immunity. (1%)
   (f) DRAM stores their content by a cross couple inverter. (1%)
   (g) The memory cell of programmable ROM is commonly a floating gate nMOS transistor. (1%)
   (h) Setup time issue is critical in shift register design. (1%)

(i) Isolation transistor in sense amplifier can speedup read/write operation at bit-line's precharging ~~high phase~~. (1%)

(j) Finite state machine can be implemented by ROM and its area is smaller than that by Programmable Logic Arrays. (PLA)

15. A three-stage logic path is designed so that the effort borne by each stage is 25, 6, 10 delay units, respectively. (5%)
    (a) Find the optimized stage number N. (2.5%)
    (b) Find the smallest path delay D_F. (2.5%)

16. An output pad contains a chain of successively larger inverters to drive the off-chip 20pF loading capacitance. If the first inverter in the chain has an input capacitance of 10fF, (5%)
    (a) Find the optimized stage number N of inverters. (2.5%)
    (b) Find the smallest delay D_F = ? FO4 inverter delay (2.5%)

17. Design a 3-input LO-skew NOR gate. Size the devices so that the pull-down is x4 as strong as the pull-up. (5%)
    (a) Sketch and label the transistor widths. (2.5%)
    (b) Estimate the rising, falling and average logical efforts. (2.5%)

18. Design a 4-input footed dynamic NAND gate driving an electrical effort of 1. The pull-down transistors' widths are chosen to give unit resistance. Estimate the worst charge sharing noise as a fraction of V_{DD} assuming that diffusion capacitance on uncontacted nodes is about half of gate capacitance and on contacted node it equals gate capacitance. (5%)

19. As shown in Fig. 19, the input loading of A is 20 and output loading of Z is 300 units. (5%)
    (a) Sketch the logic by domino gates and footed dynamic circuits. (2.5%)
    (b) Find the path delay (A-Z) D_F. (2.5%)

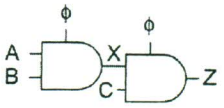

Fig. 19

20. An example logic path is shown as Fig. 20. The input loading of A is 5 and output loading of B is 80. (5%)
    (a) Estimate the minimum delay of the path from A to B. (2.5%)
    (b) Find the transistor sizes (nMOS & pMOS) of each gate. (2.5%)

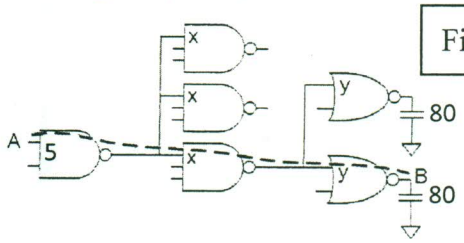

Fig. 20