EE3230 Lecture 8: Sequential Circuit Design

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Outline

- Sequencing Methods
- Max/Min Delay, Clock Skew, Timing Borrowing
- Sequencing Element Design

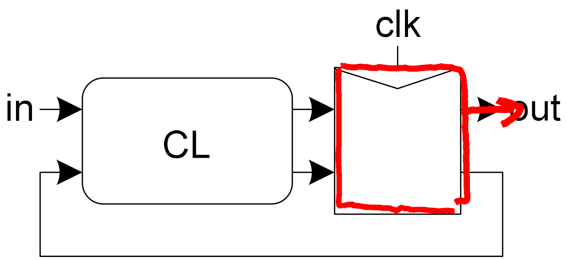
Outline

- **Sequencing Methods**
- Max/Min Delay, Clock Skew, Timing Borrowing
- Sequencing Element Design

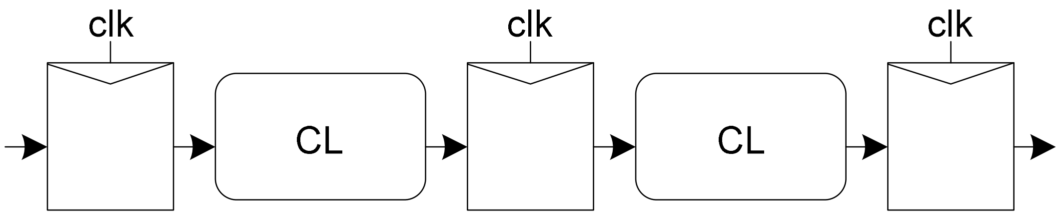
Sequencing

- Combinational logic
  - Outputs depend on current inputs

- Sequential logic
  - Outputs depend on current and previous inputs
  - Previous, current, and future separated
  - Memory elements required
    - Called states or tokens
  - Examples: **F**inite-**S**tate **M**achine (FSM), pipeline



Finite State Machine

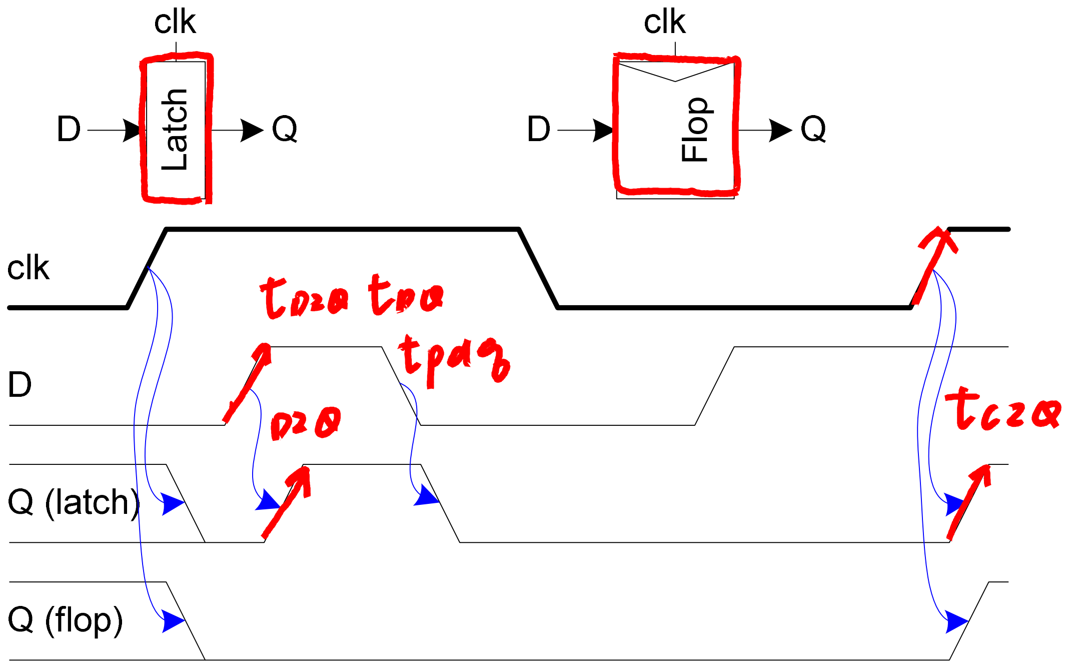


Pipeline

Sequencing Elements

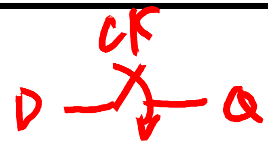
- **Latch:** level-sensitive
  - a.k.a. transparent latch, D latch, etc.
- **Flip-flop:** edge-triggered
  - a.k.a. master-slave flip-flop, D flip-flop, D register, etc.

- Timing diagram
  - Transparent
  - Opaque
  - Edge-triggered



Latch vs. Flip-Flops

- **Latch:** level-sensitive

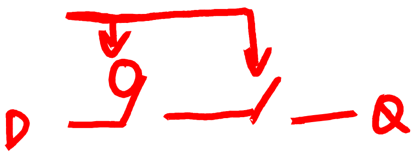


ON

  - Passes input D to Q when the clock is high – transparent mode
  - Input D sampled on the falling edge of the clock is held stable when clock is low – hold mode

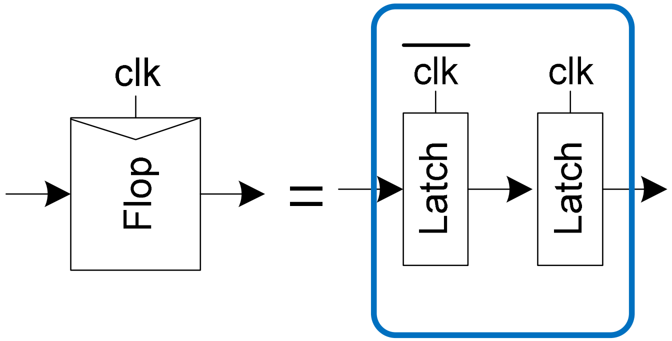
OFF

- **Flip-flop:** edge-triggered
  - Samples input D on a clock transition
  - Can be either positive edge-triggered or negative edge-triggered
  - Built using two latches (master-slave flip-flops)

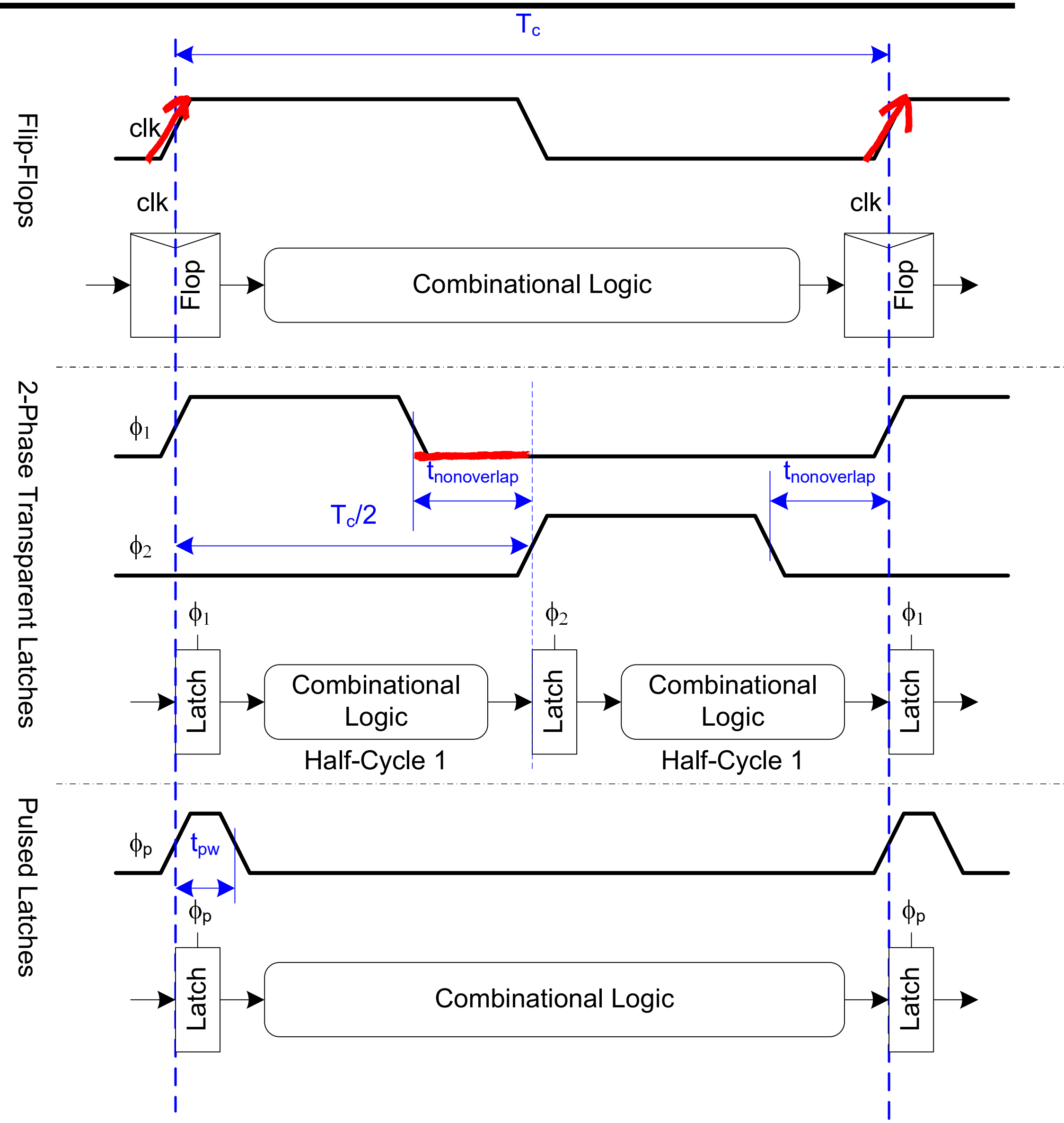


Sequencing Methods

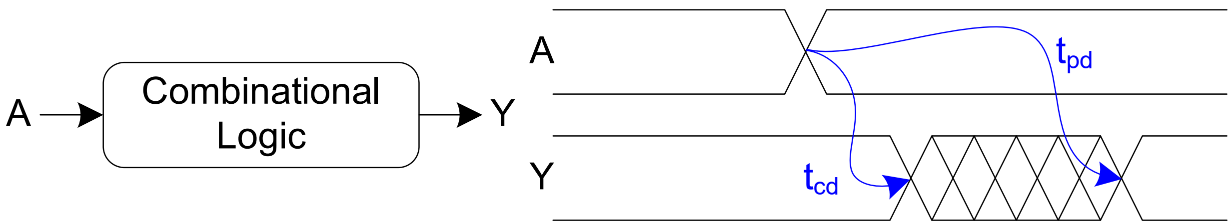
- Flip-flops



- 2-phase latches
- Pulsed latches

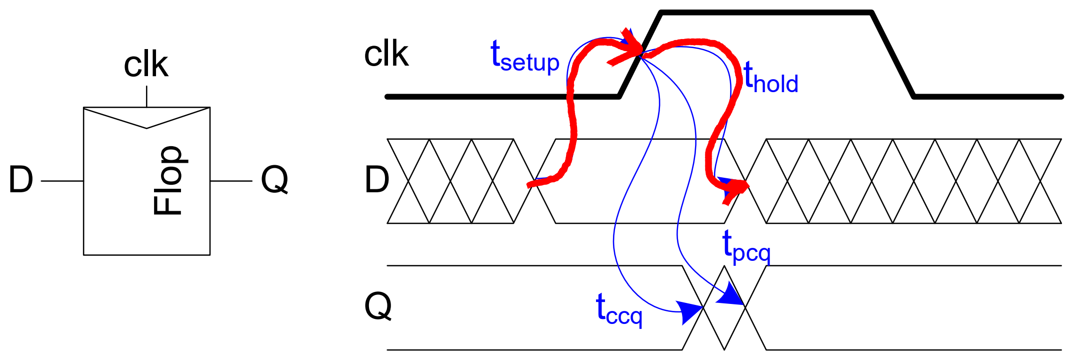


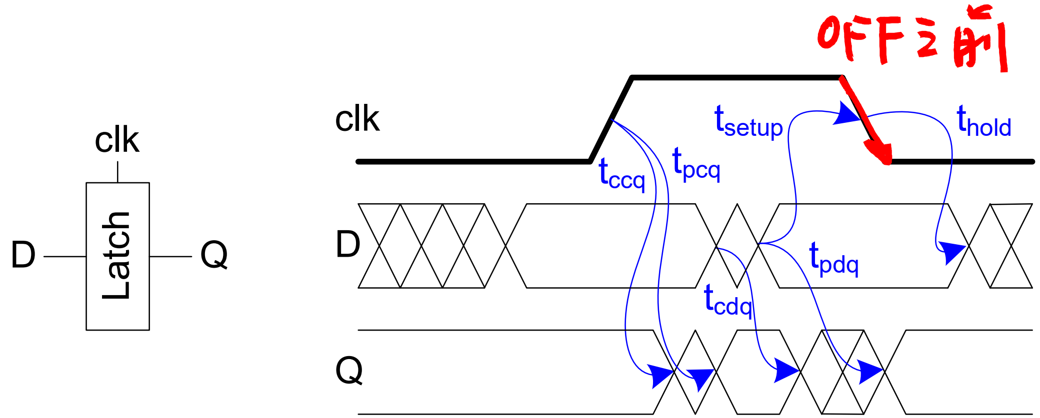
Timing Diagrams



t_{pd}	Logic Prop. Delay
t_{cd}	Logic Cont. Delay
t_{pcq}	Latch/Flop Clk-Q Prop Delay
t_{ccq}	Latch/Flop Clk-Q Cont. Delay
t_{pdq}	Latch D-Q Prop Delay
t_{cdq}	Latch D-Q Cont. Delay
t_{setup}	Latch/Flop Setup Time
t_{hold}	Latch/Flop Hold Time

* Contamination & Propagation delays





Sequencing Overhead

- Flip-flops are used to delay **fast tokens** so that they move through exactly one stage per cycle

- Inevitably add some delay to **slow tokens**
- Make circuits slower than just the logic delay
  - Called sequencing overhead
  - Some people call this clocking overhead
  - Inevitable side effect of maintaining sequence

Outline

- Sequencing Methods
- **Max/Min Delay, Clock Skew, Timing Borrowing**
- Sequencing Element Design

Max/Min Delay Constraints

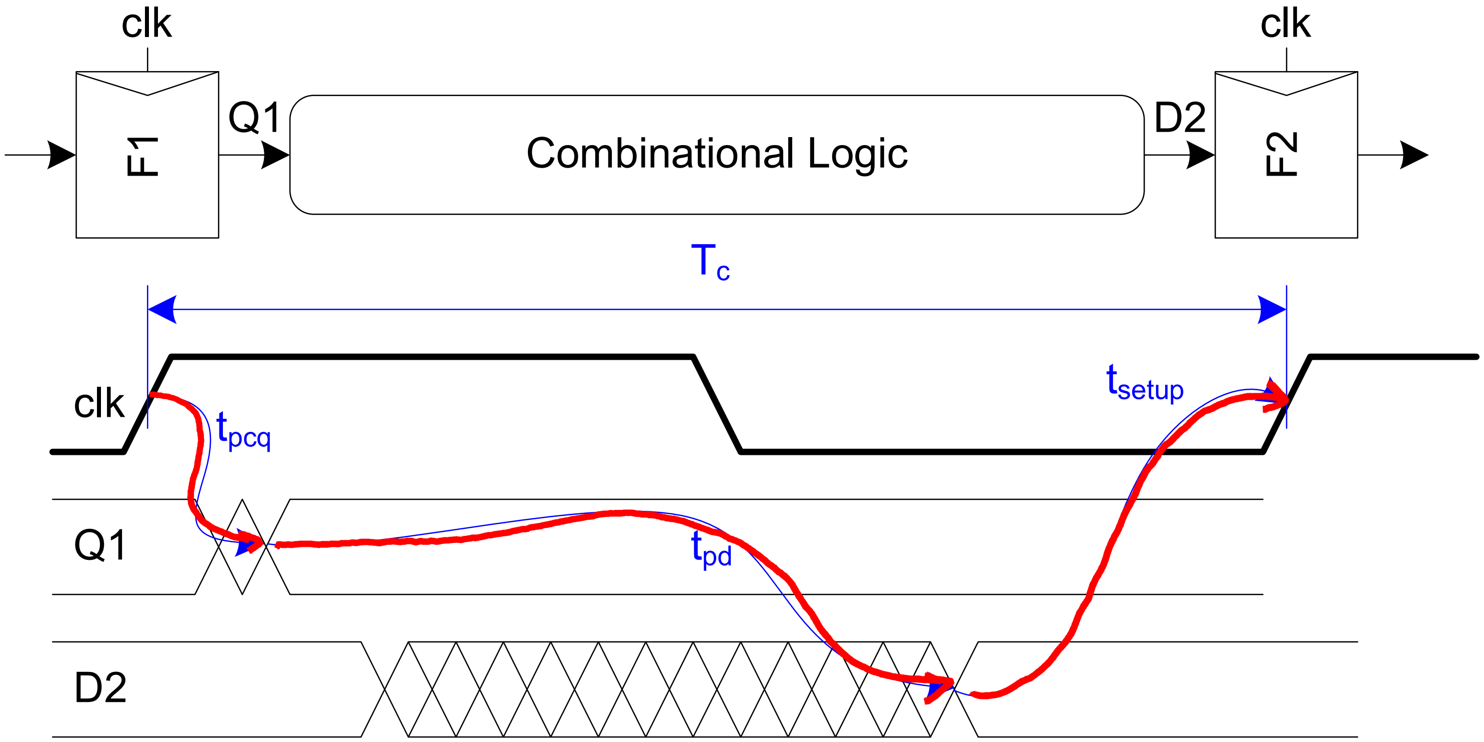
- Max delay constraint
  - Combinational logic delay cannot be too late, or the receiving element would miss its setup time and sample the wrong value → **setup time failure**

- Min delay constraint
  - Contamination delay of logic cannot be too small, or the data can incorrectly propagate through one clock edge and corrupt the state → **hold-time failure**, **race condition**
  - Redesign for slower logic

Max Delay: Flip-Flops

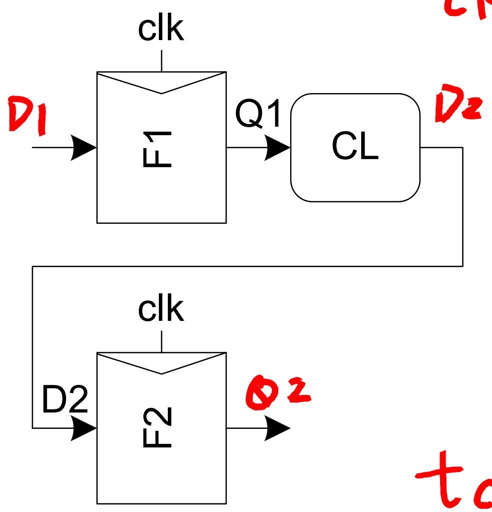
$$t_{pd} \le T_c - \underbrace{\left(t_{setup} + t_{pcq}\right)}_{\text{sequencing overhead}}$$

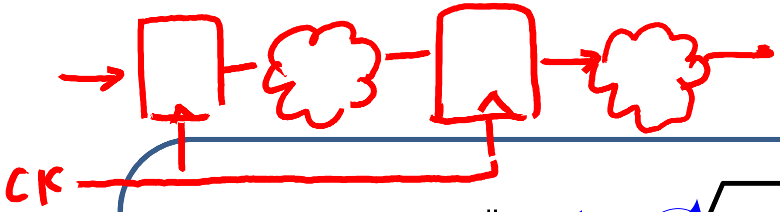
$t_{c2Q} + t_p + t_{setup} < T$

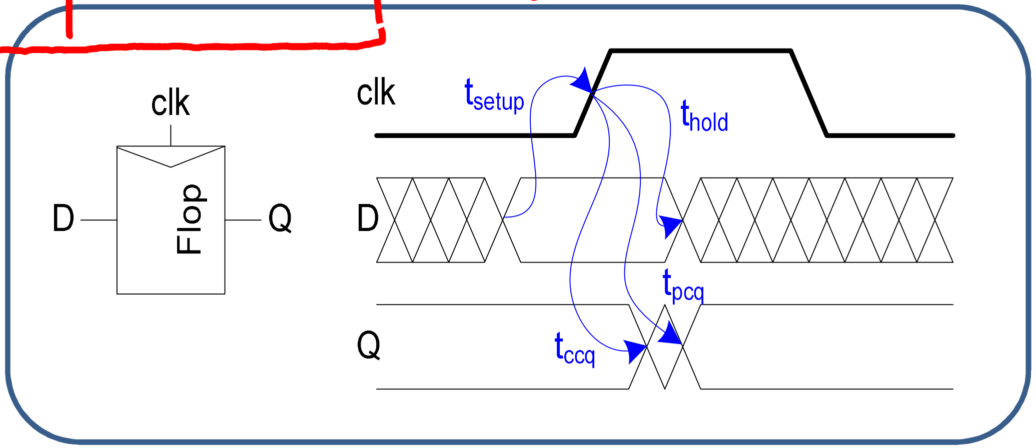


Min Delay: Flip-Flops

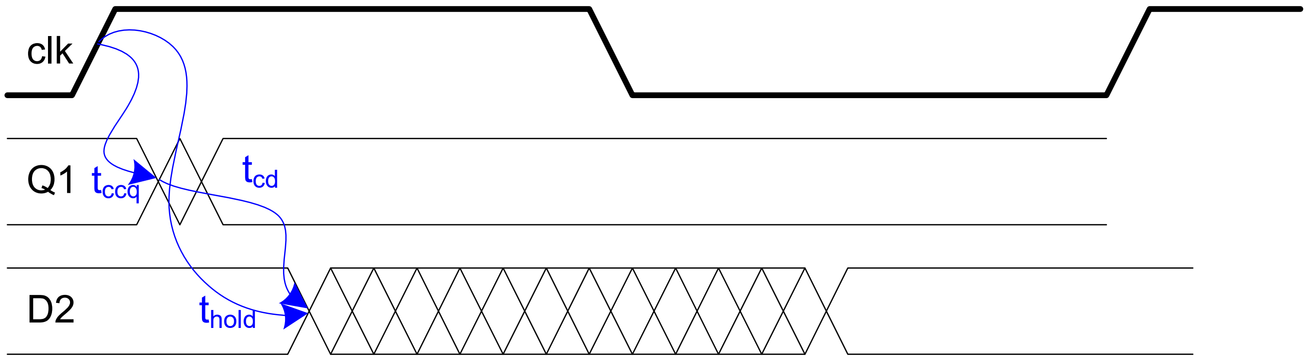
$$t_{cd} \geq t_{hold} - t_{ccq}$$







$t_{c2q} + t_p > t_{hold}$



Clock Skew

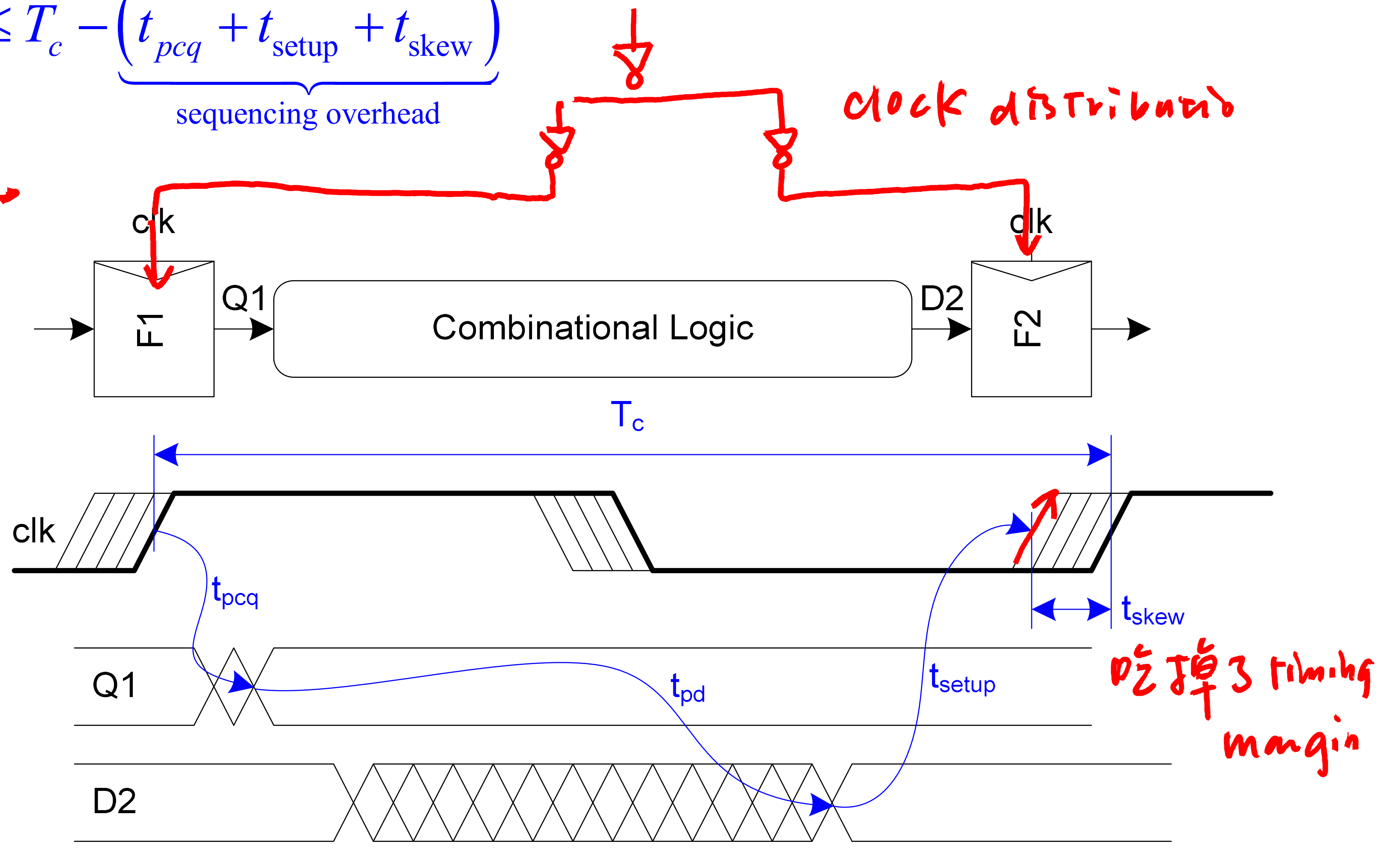
ideally

- We have assumed zero clock skew
- Clock signals have uncertainty in arrival time

Skew: Flip-Flops: Max Delay

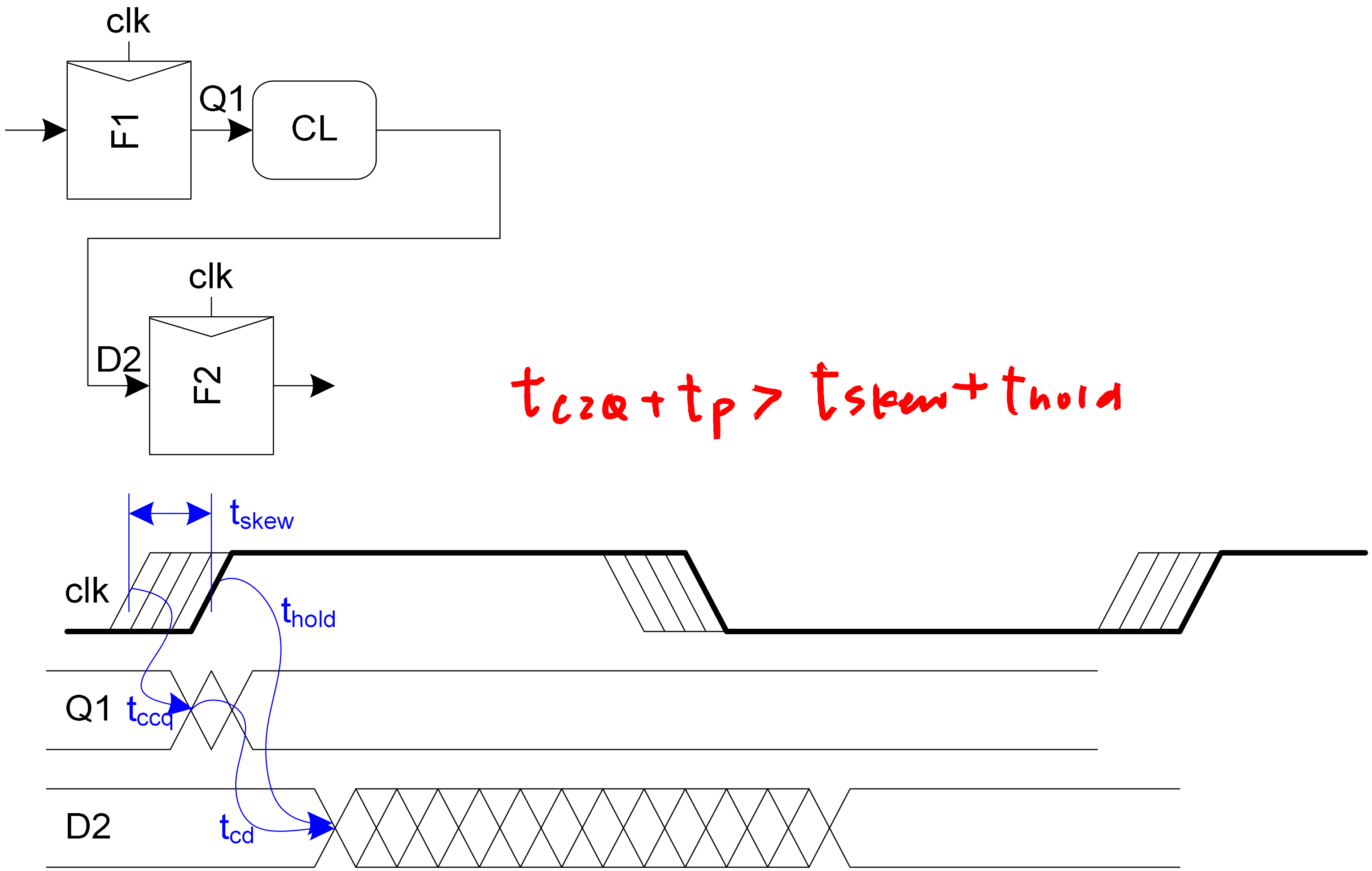
$$t_{pd} \le T_c - \Big(\underbrace{t_{pcq} + t_{\text{setup}} + t_{\text{skew}}}_{\text{sequencing overhead}}\Big)$$

CL →



Skew: Flip-Flops: Min Delay

$$t_{cd} \geq t_{\text{hold}} - t_{ccq} + t_{\text{skew}}$$



$t_{c2q} + t_p > t_{skew} + t_{hold}$

Max Delay: 2-Phase Latches

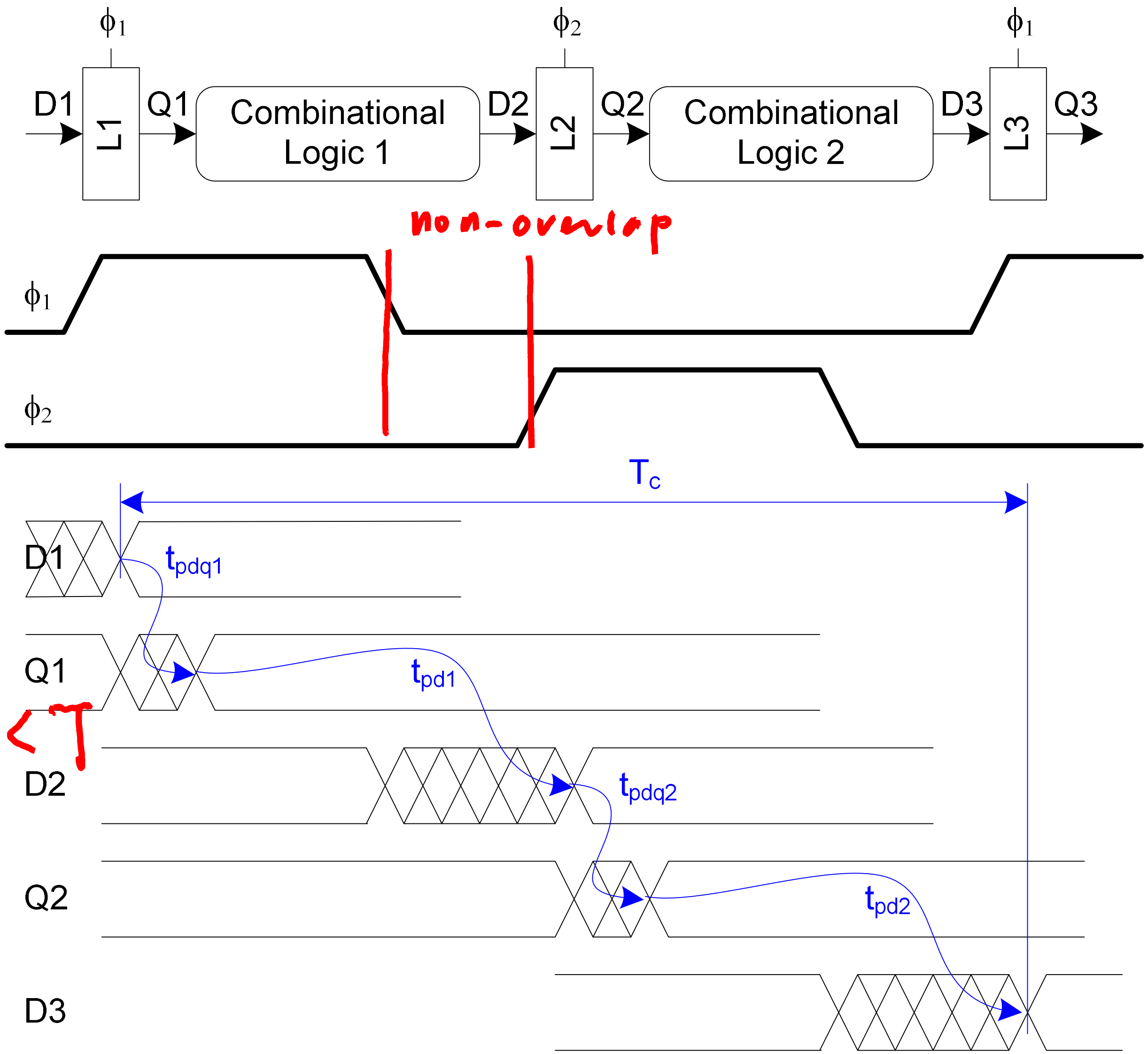
$$t_{pd} = t_{pd1} + t_{pd2}$$

$$\leq T_c - \underbrace{\left(2t_{pdq}\right)}_{\text{sequencing overhead}}$$

in average

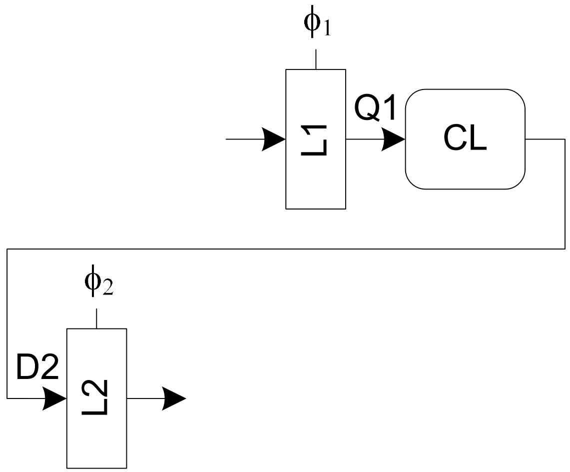
$t_{D1 \to D3} < T$

$t_{D2Q} + t_{P1} + t_{D2Q} + t_{P2} < T$



Min Delay: 2-Phase Latches

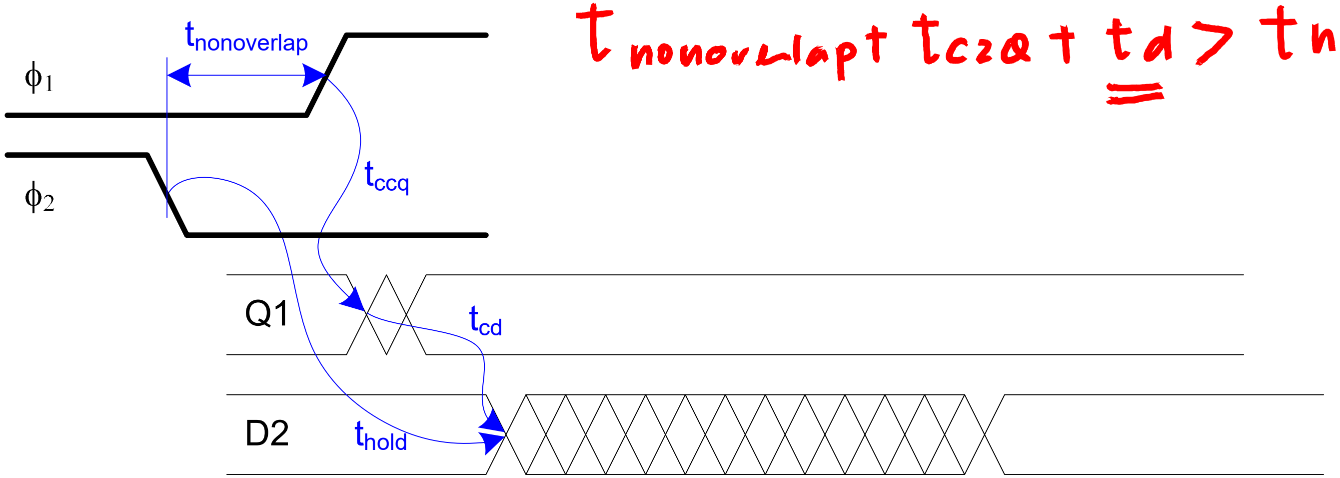
$t_{cd1}, t_{cd2} \geq t_{\text{hold}} - t_{ccq} - t_{\text{nonoverlap}}$



- Hold time error reduced by non-overlap compared to flip-flops

  → Internal race condition of flip-flops

$t_{nonoverlap} + t_{c2q} + \underline{\underline{t_{d}}} > t_{hold}$

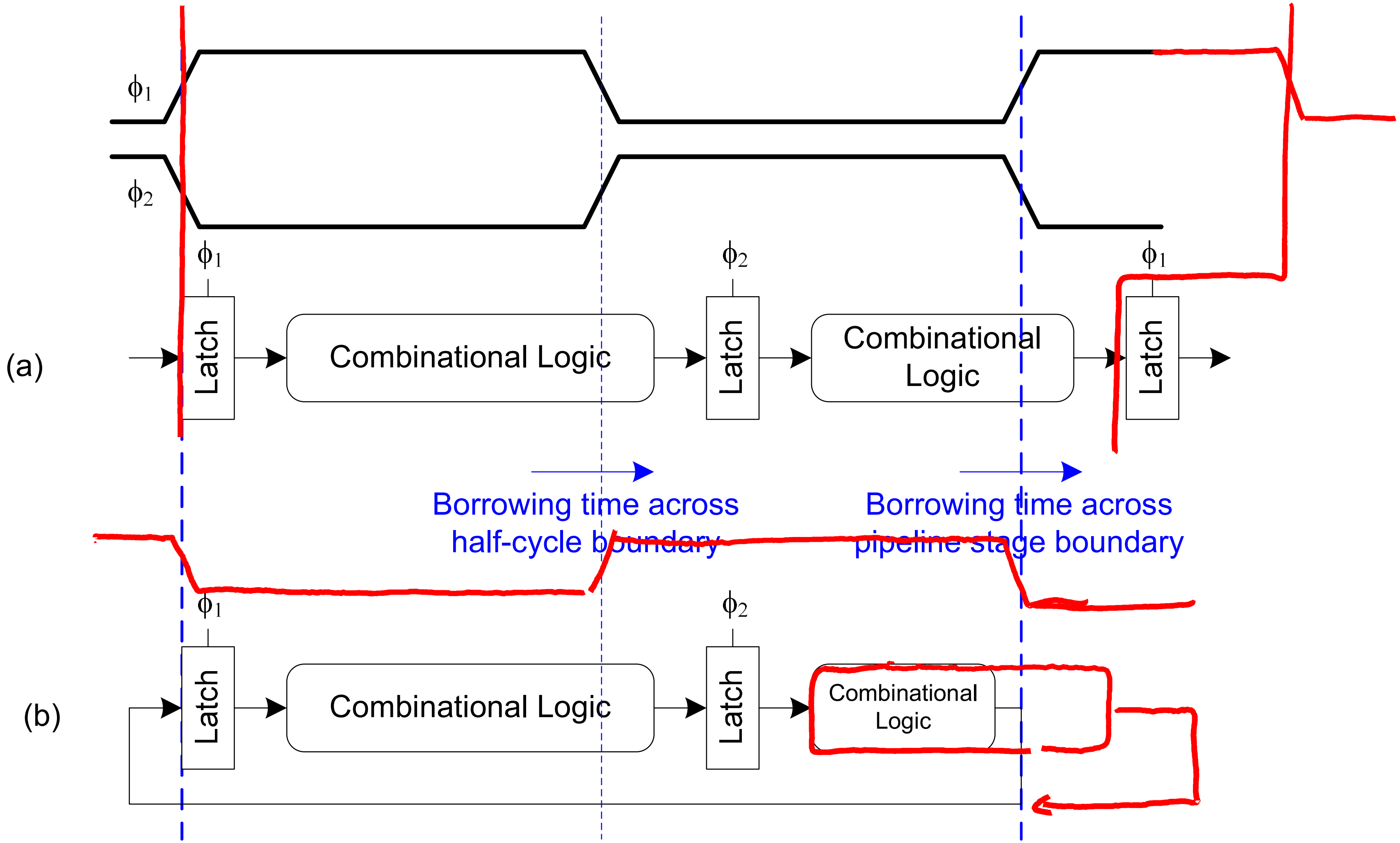


Timing Borrowing

- In flip-flop systems
  - Data launch on one rising edge
  - Must setup before next rising edge
  - If data arrive late → system fails
  - If data arrive early → system fails
  - **Flip-flop systems have hard edges**

- In latched-based systems
  - Data can pass through latches while transparent
  - Long logic delay can borrow time into next cycle
  - As long as each loop completes in time

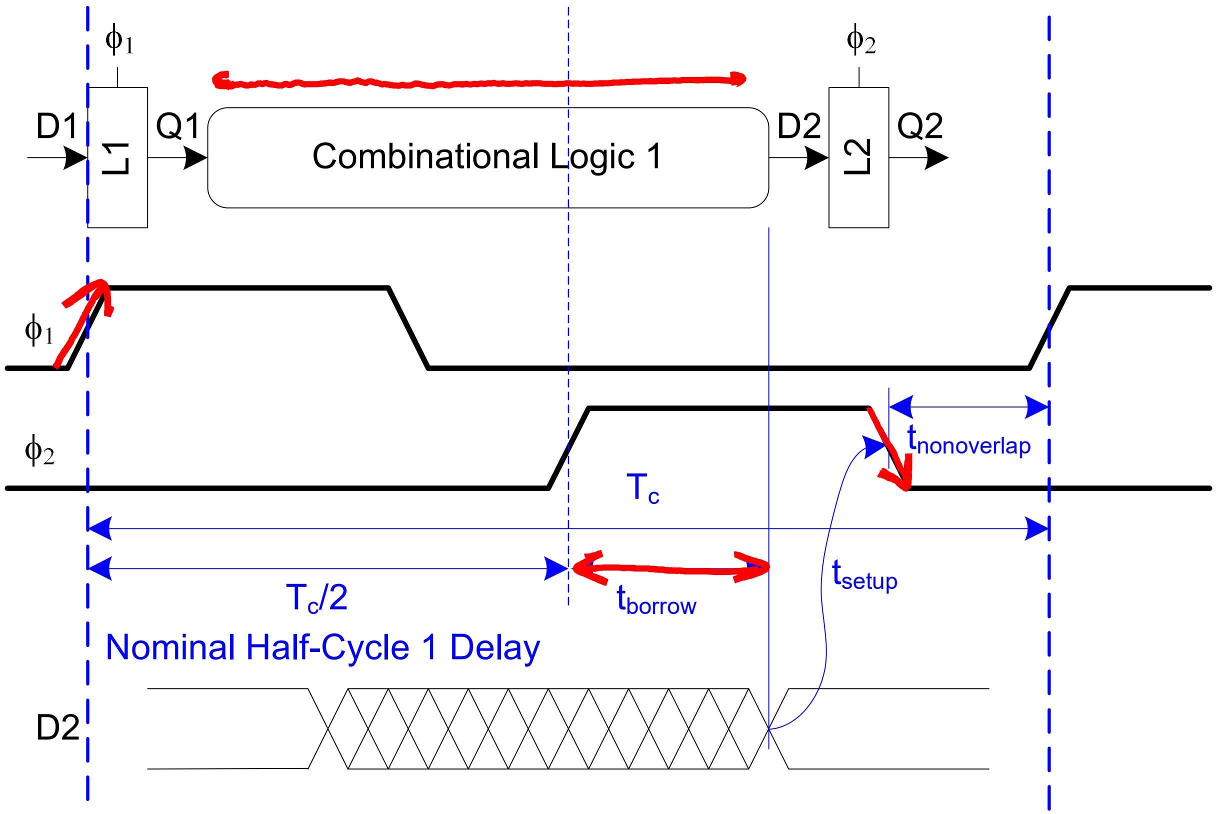
Time Borrowing Example



Loops may borrow time internally but must complete within the cycle

How Much Borrowing?

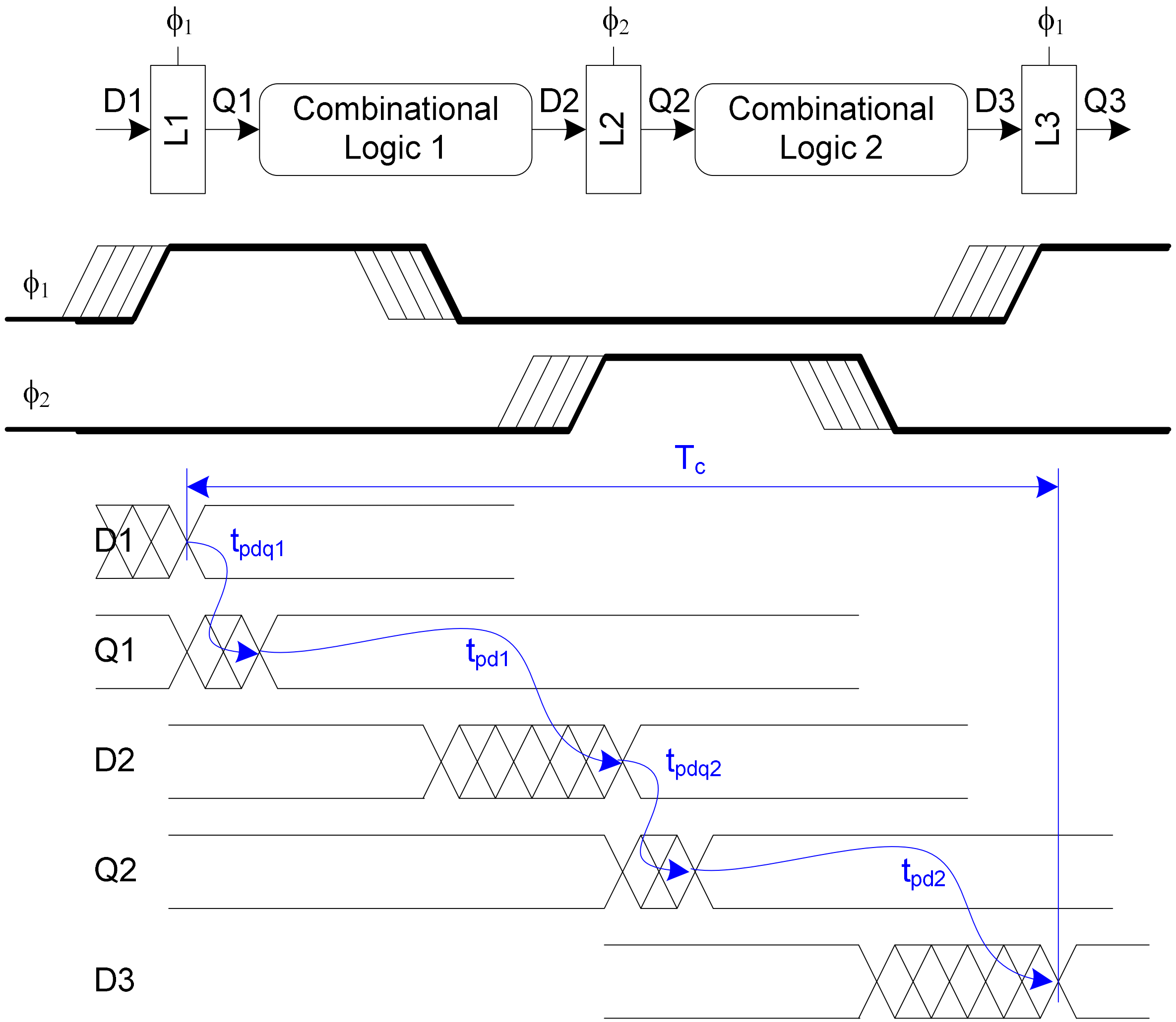
$$t_{\text{borrow}} \leq \frac{T_c}{2} - \left(t_{\text{setup}} + t_{\text{nonoverlap}}\right)$$



Skew: 2-Phase Latches: Max Delay

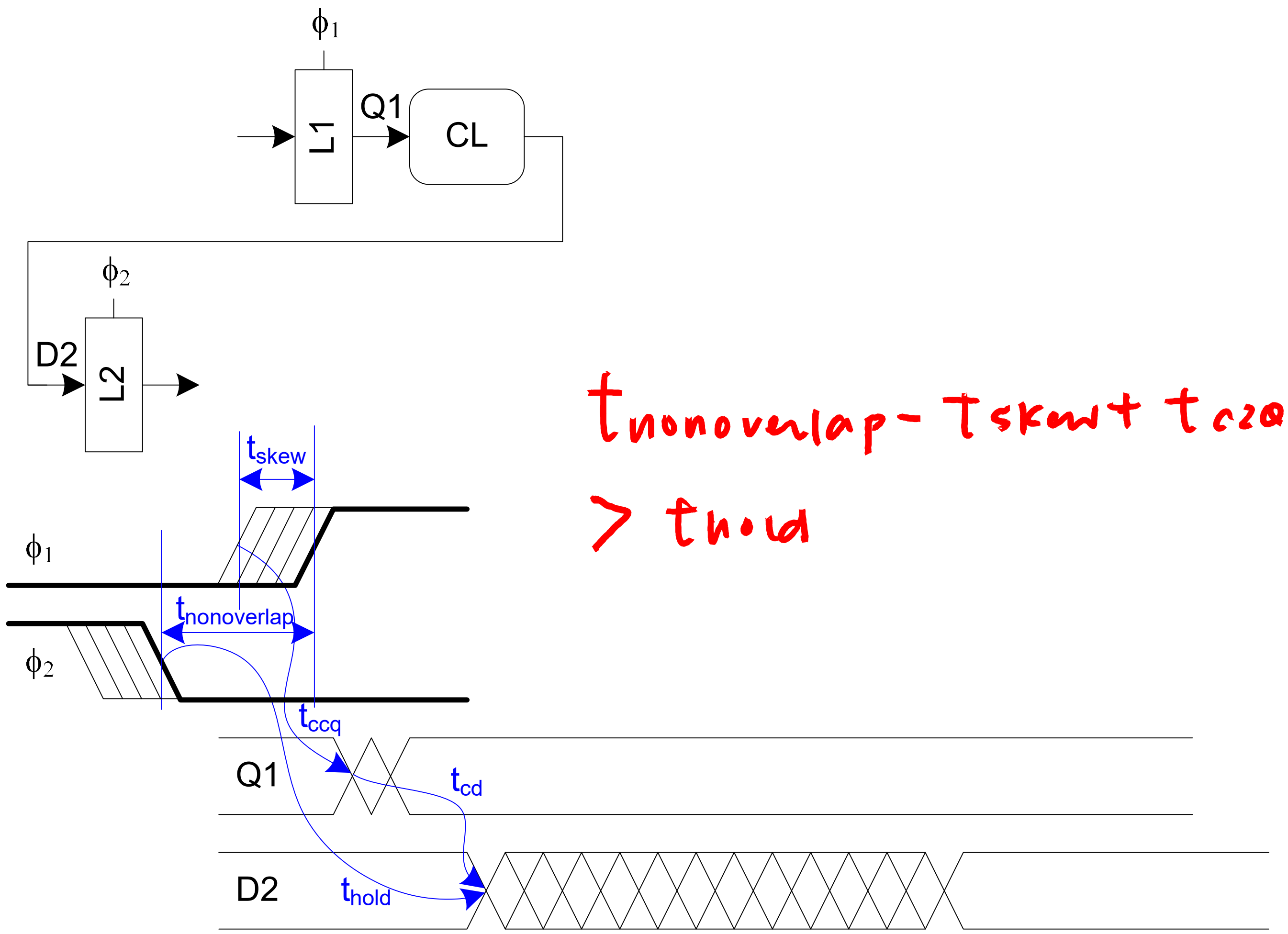
$$t_{pd} \leq T_c - \underbrace{\left(2t_{pdq}\right)}_{\text{sequencing overhead}}$$

- Latch-based designs are **skew-tolerant**



Skew: 2-Phase Latches: Min Delay

$$t_{cd1}, t_{cd2} \geq t_{\text{hold}} - t_{ccq} - t_{\text{nonoverlap}} + t_{\text{skew}}$$

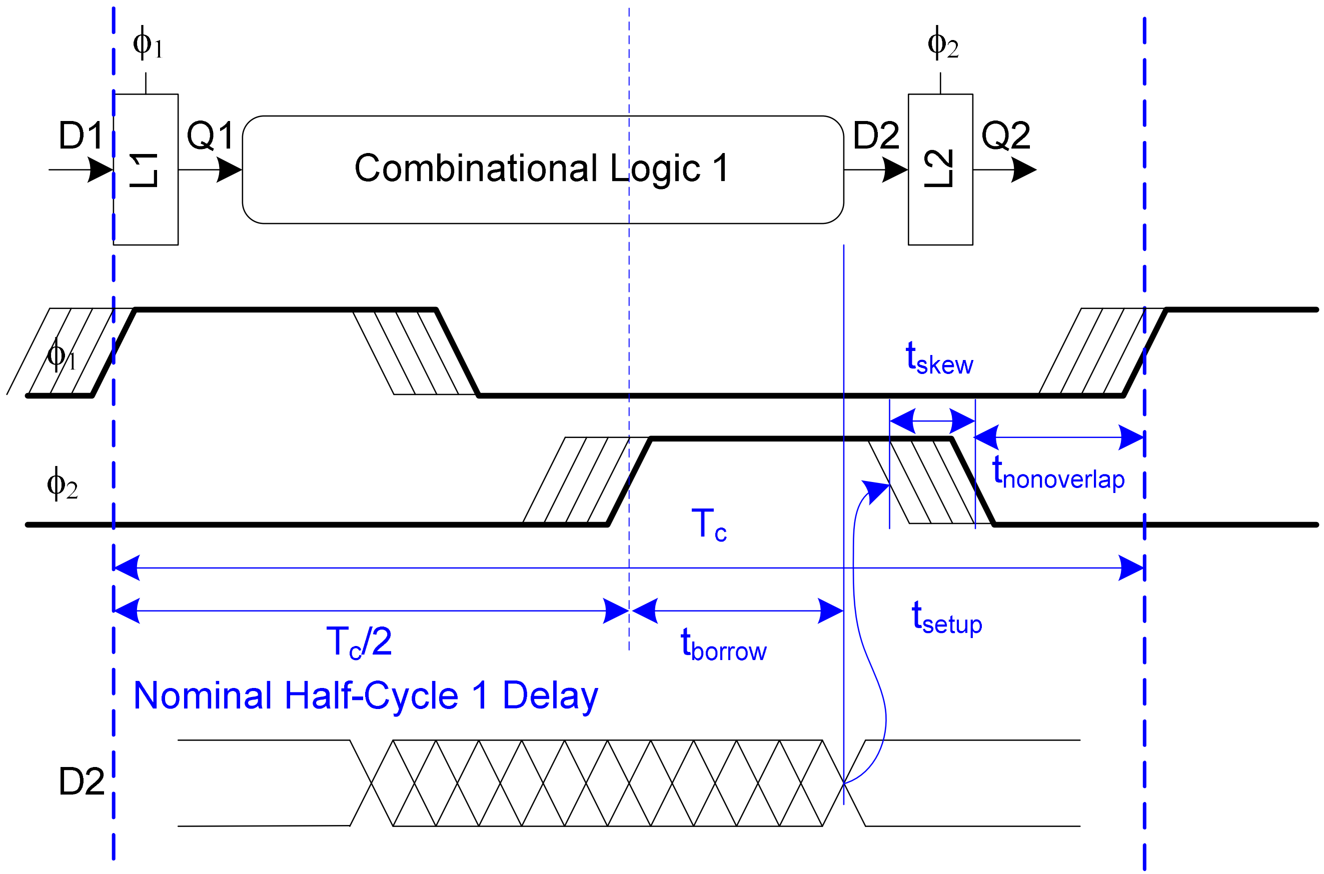


$t_{nonoverlap} - t_{skew} + t_{c2q} + \underline{\underline{t_p}}$

$> t_{hold}$

Skew: How Much Borrowing?

$$t_{\text{borrow}} \le \frac{T_c}{2} - \left(t_{\text{setup}} + t_{\text{nonoverlap}} \underline{+ t_{\text{skew}}}\right)$$ 讓你能借的時間變少



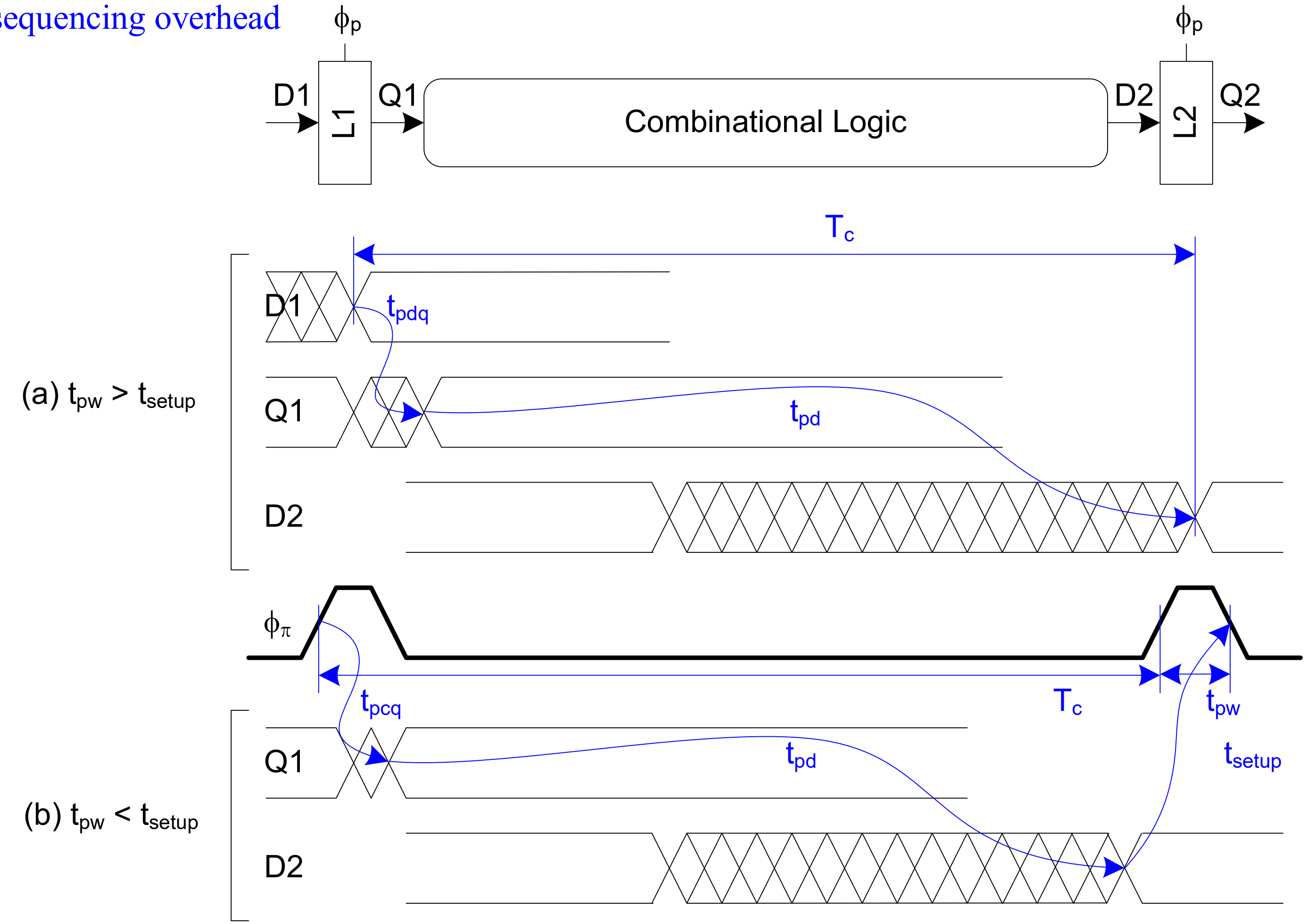
Clock Skew

- We have assumed zero clock skew
- Clock signals have uncertainty in arrival time
  → Negative impact on timing margin

  – Decrease setup time margin
    (effectively increase maximum delay)
  – Decrease hold time margin
    (effectively decrease contamination delay)
  – Decrease timing borrowing

Max Delay: Pulsed Latches

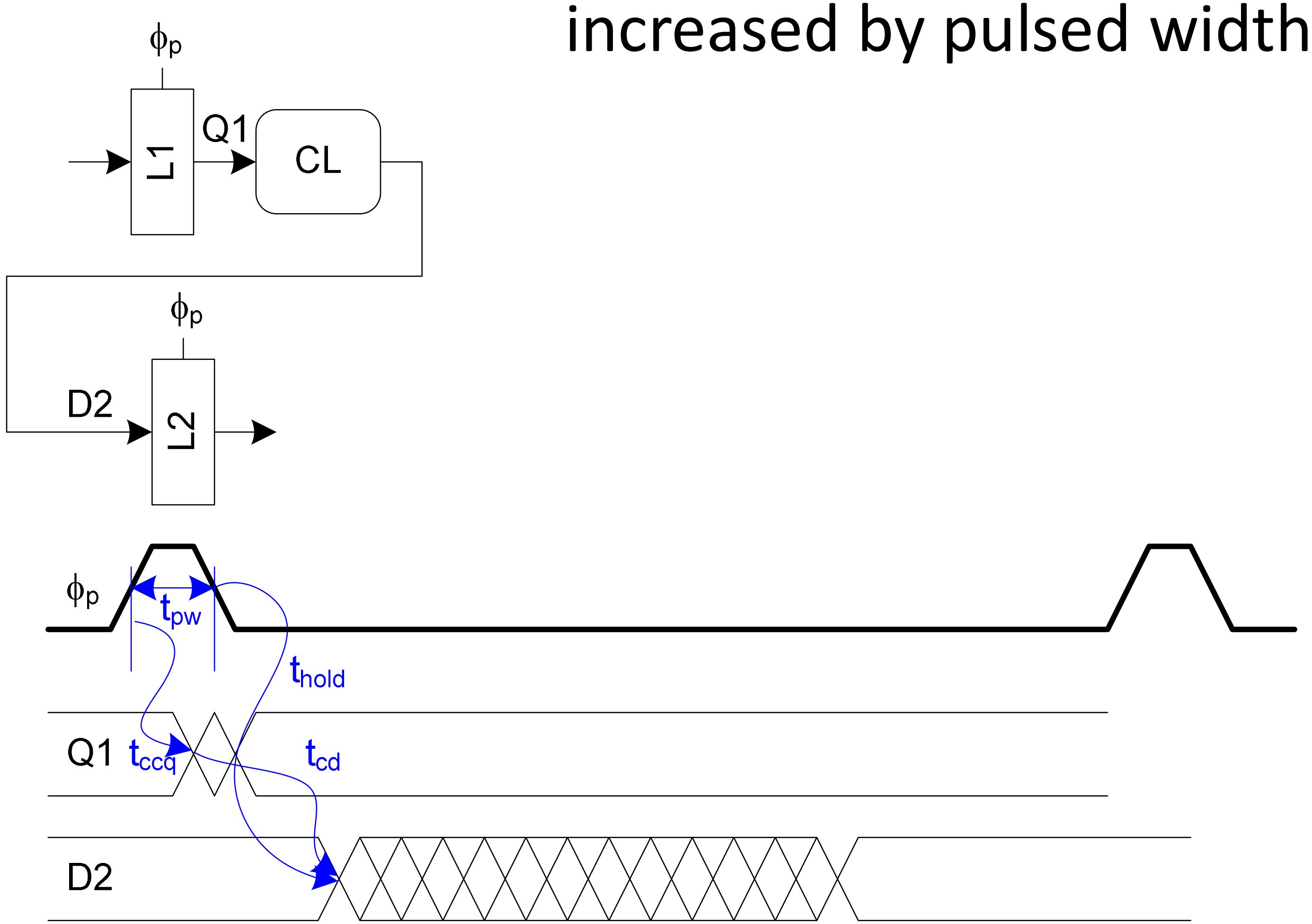
$$t_{pd} \leq T_c - \underbrace{\max\left(t_{pdq}, t_{pcq} + t_{setup} - t_{pw}\right)}_{\text{sequencing overhead}}$$



Min Delay: Pulsed Latches

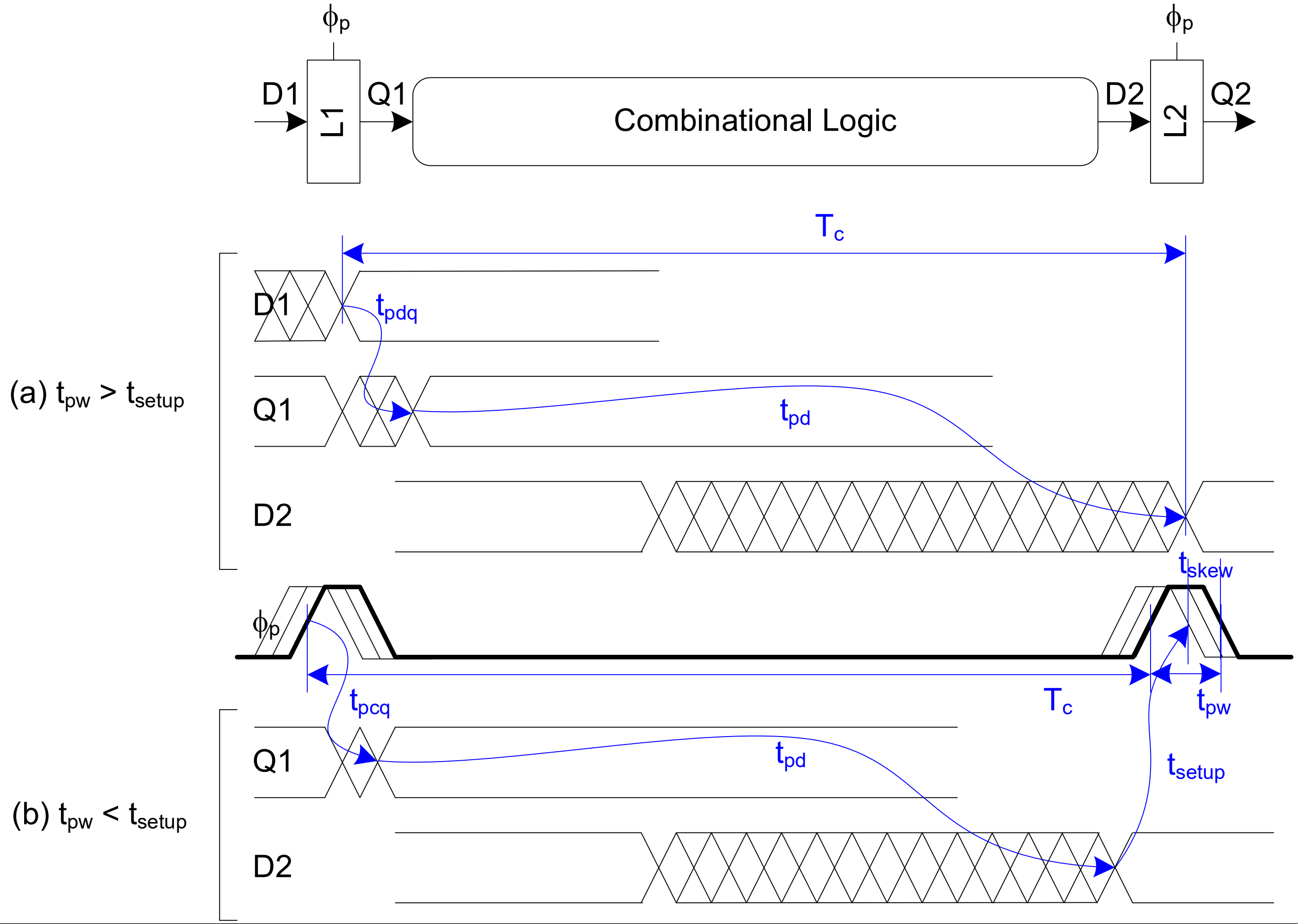
$$t_{cd} \geq t_{\text{hold}} - t_{ccq} + t_{pw}$$

- Hold-time error increased by pulsed width



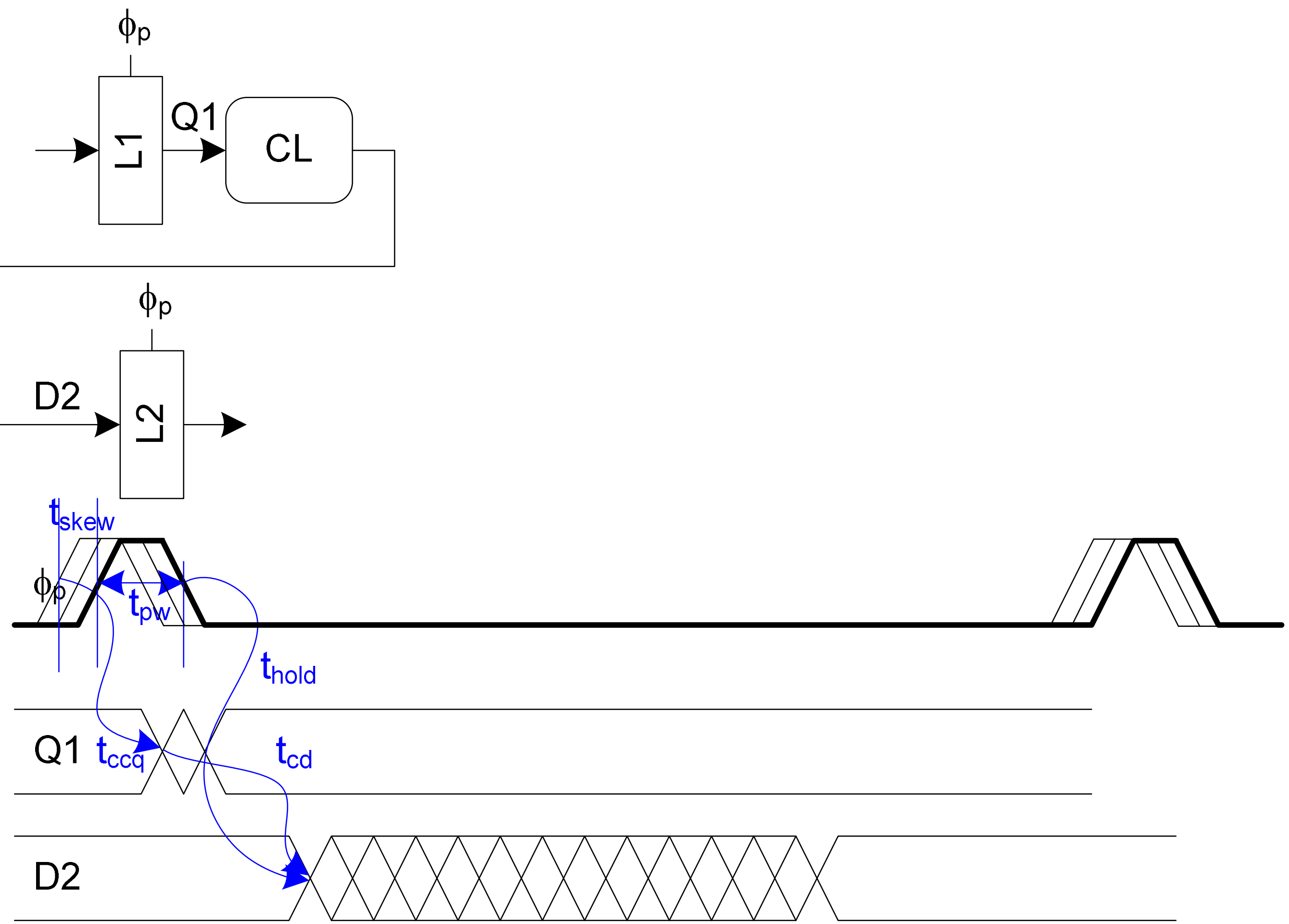
Skew: Pulsed Latches: Max Delay

$$t_{pd} \le T_c - \underbrace{\max\left(t_{pdq}, t_{pcq} + t_{\text{setup}} - t_{pw} + t_{\text{skew}}\right)}_{\text{sequencing overhead}}$$



Skew: Pulsed Latches: Min Delay

$$t_{cd} \geq t_{\text{hold}} + t_{pw} - t_{ccq} + t_{\text{skew}}$$



Outline

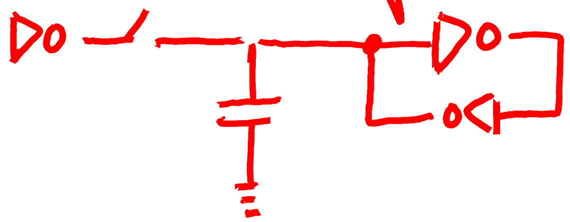
- Sequencing Methods
- Max/Min Delay, Clock Skew, Timing Borrowing
- **Sequencing Element Design**

Static vs. Dynamic Storage

- Static Storage
  - Preserve state as long as power is on
  - Use positive feedback (regeneration) with an internal connection between output and input
  - Useful when updates are infrequent

keeper

positive FB



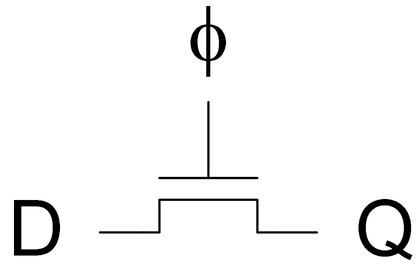
- Dynamic Storage
  - Store state on parasitic capacitors
  - Hold state only for short period of time (milli-seconds)
  - Require periodic refresh
  - Simpler design, higher speed, and lower power

metastable point

$v_{in} = V_{out} = 0.5\,V_{DD}$

Latch Design (I)

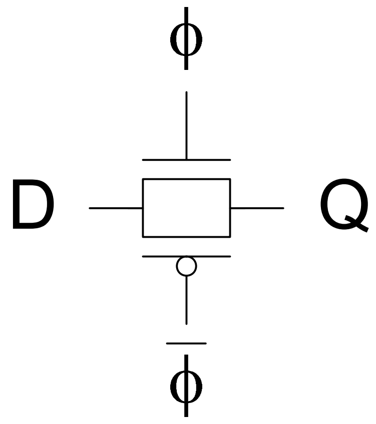
- Pass-transistor latch
- Pros:
  - Tiny
  - Low load on clock signal
- Cons:
  - Vth drop (not rail-to-rail)
  - Non-restoring
  - Back-driving
  - Output noise sensitivity
  - Dynamic (float when opaque)
  - Diffusion input



(used in 1970's)

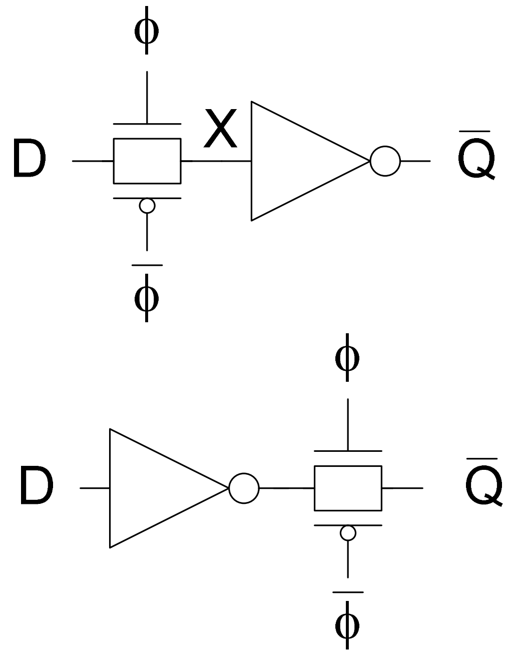
Latch Design (II)

- Transmission gate
- Pros:
  - No Vth drop
- Cons:
  - Inverted clock signal required



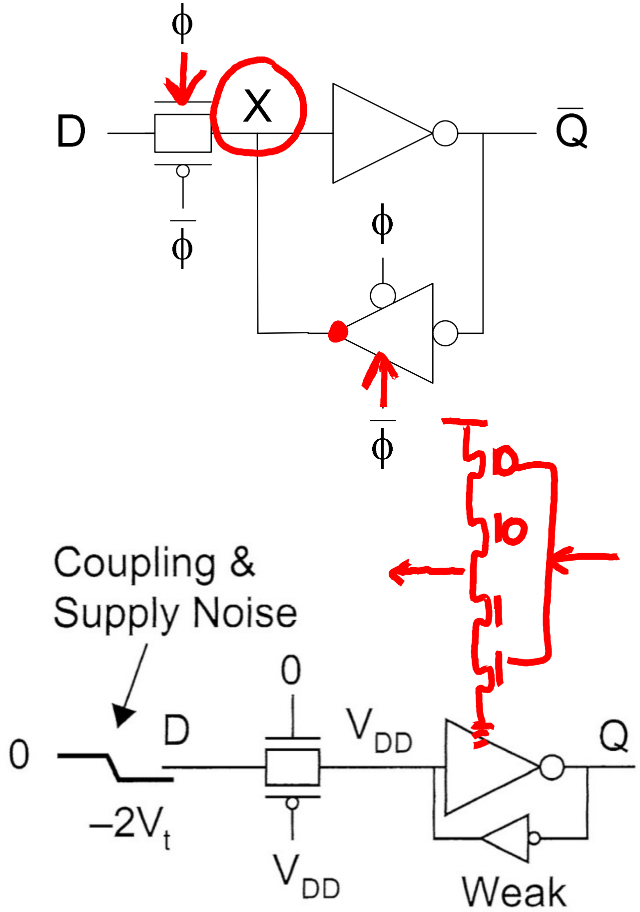
Latch Design (III)

- Buffered version
- Pros:
  - Restoring
  - No back-driving that fixes either one of the followings
    - Output noise sensitivity
    - Diffusion input
- Cons:
  - Inverted output



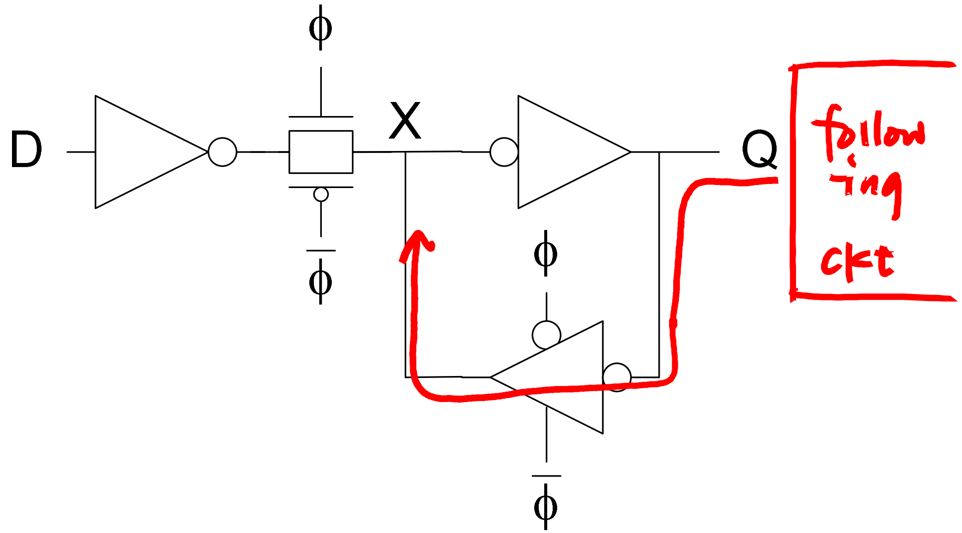
Latch Design (IV)

- Tristate feedback
- Pros:
  - Static
    - Static latches are now essential
- Cons:
  - Back-driving risk
  - Diffusion input
    - Noise can sneak through OFF transmission gate and destroy output



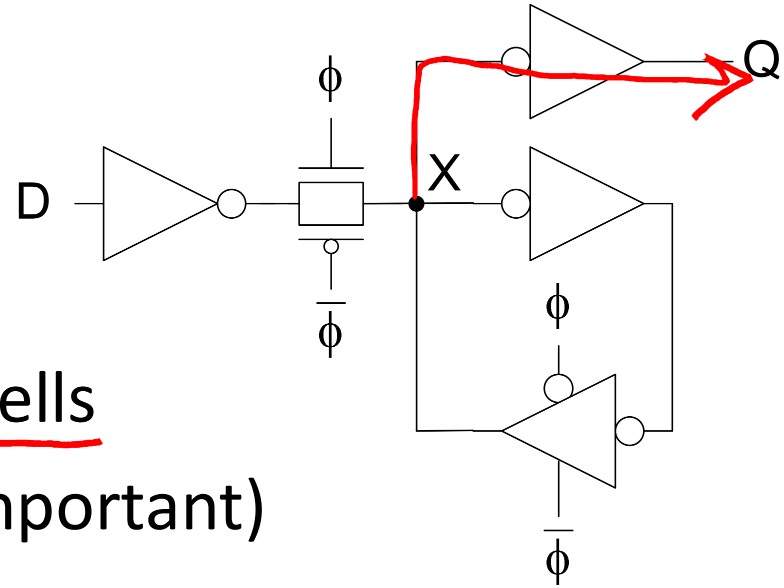
Latch Design (V)

- Buffered input with feedback
- Pros:
  - Fixes diffusion input
  - Non-inverting
- Cons:
  - Output noise back-driving



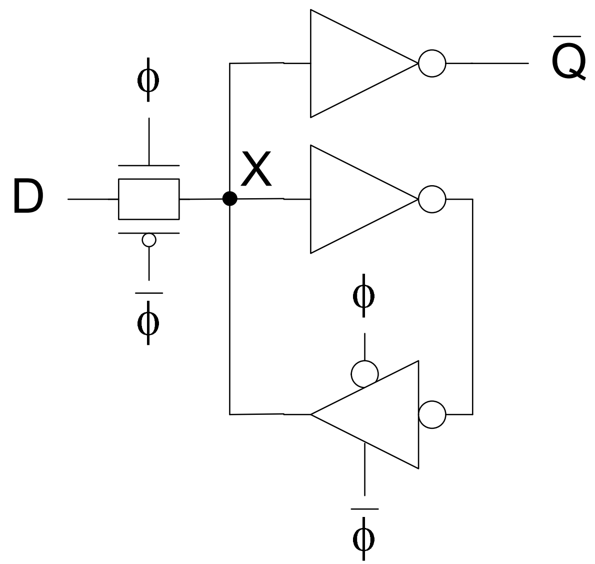
Latch Design (VI)

- Buffered output
  - No back-driving
- Widely used in standard cells
- Pros: very robust (most important)
- Cons:
  - Rather large
  - Rather slow (1.5 to 2 FO4 delays)
  - High clock loading



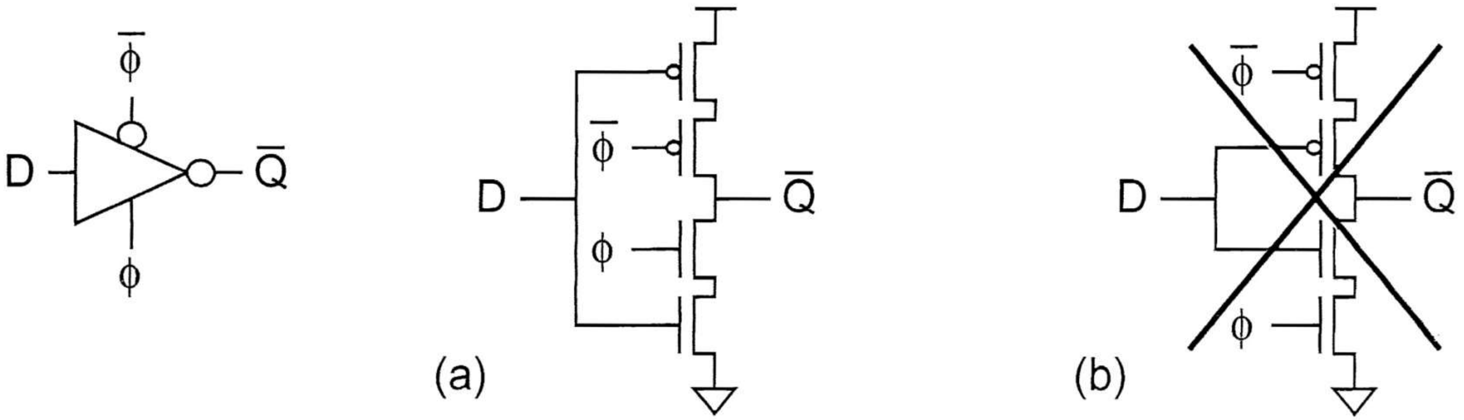
Latch Design (VII)

- Another alternative
  - Smaller and faster
  - Need to be careful with noise control



Clocked CMOS: C^2MOS

- C^2MOS latch
  - Smaller
  - Slower

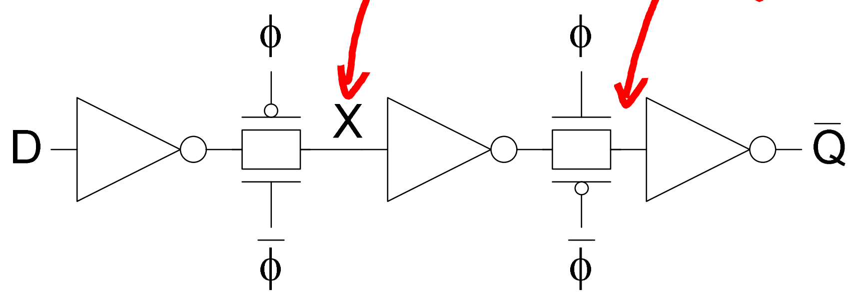


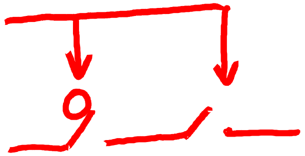
Bad design: toggling in D causes charge sharing noise when opaque

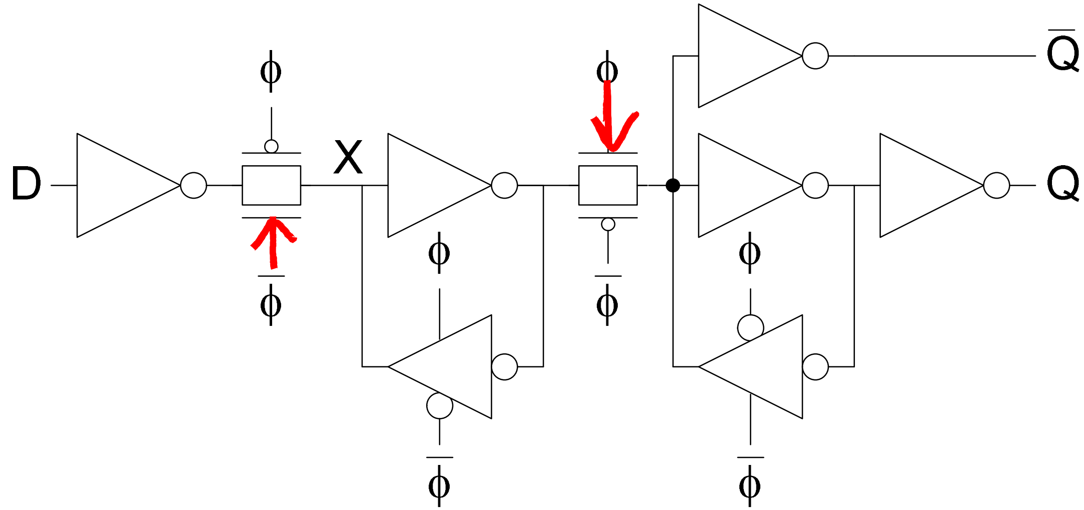
Flip-Flop Design

- Flip-flop is built as a pair of back-to-back latches

dynamic nodes

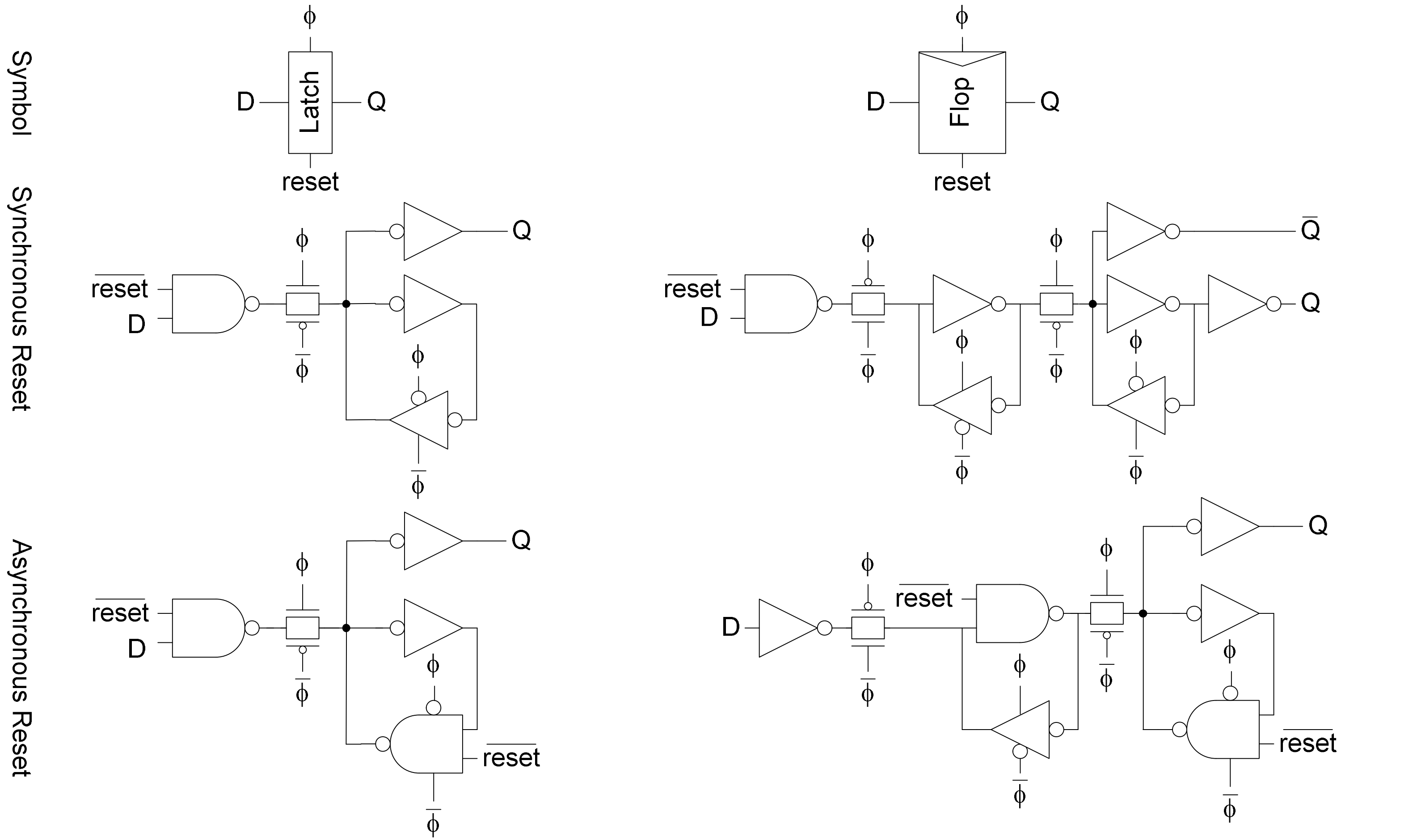






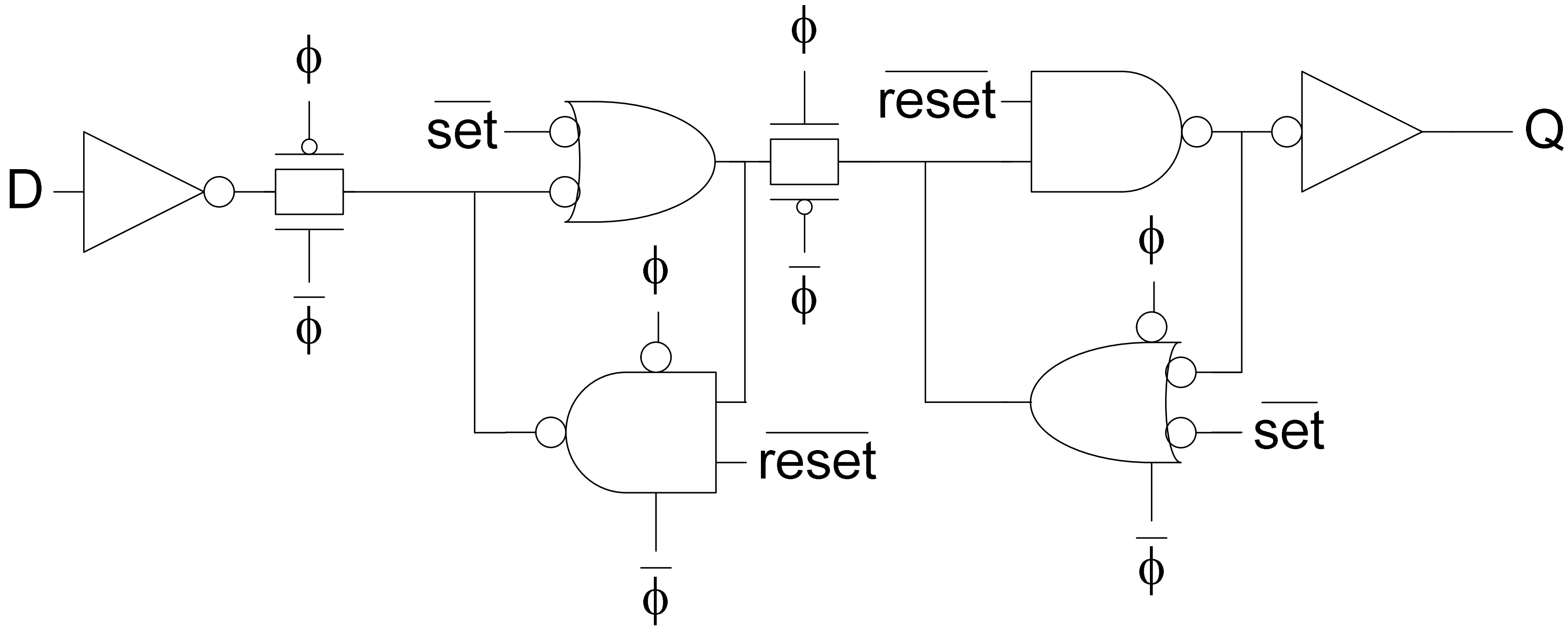
Reset

- Force output low when **reset** signal is asserted
- Synchronous vs. asynchronous



Set/Reset

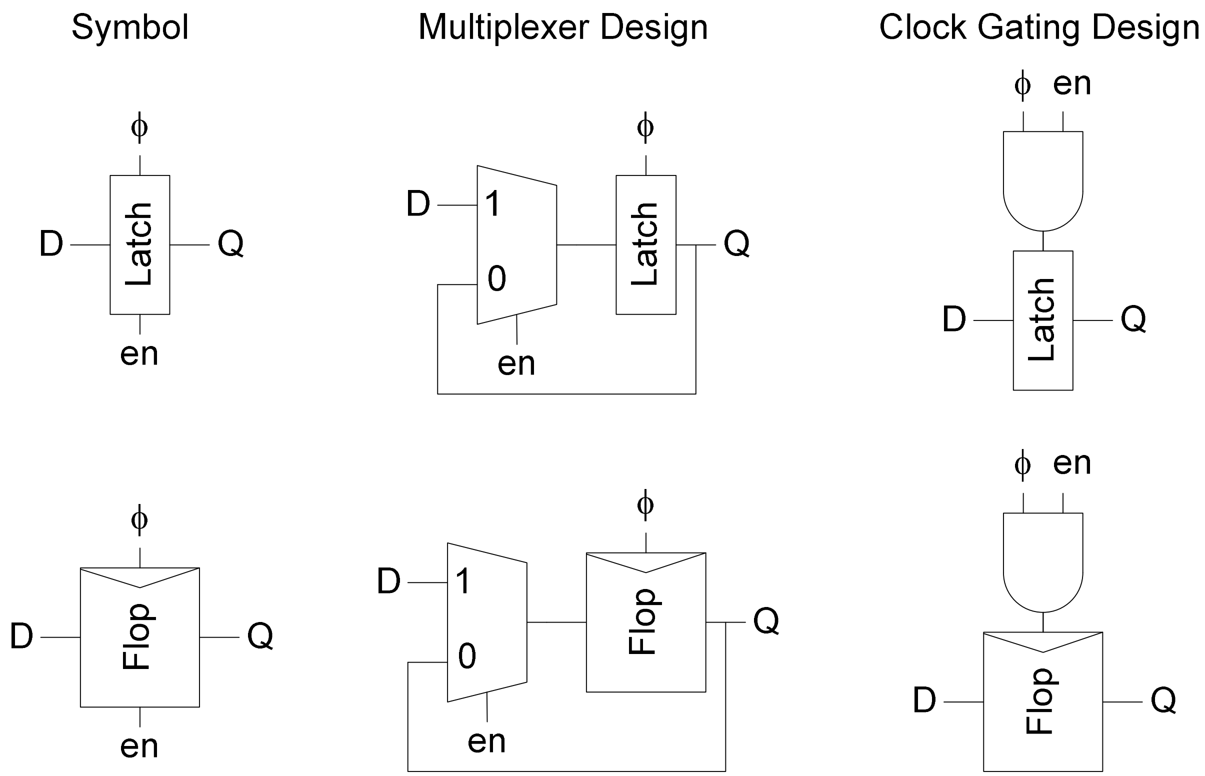
- Force output low when **reset** signal is asserted
- Force output high when **set** signal is asserted



- **Example:** flip-flop with asynchronous set and reset

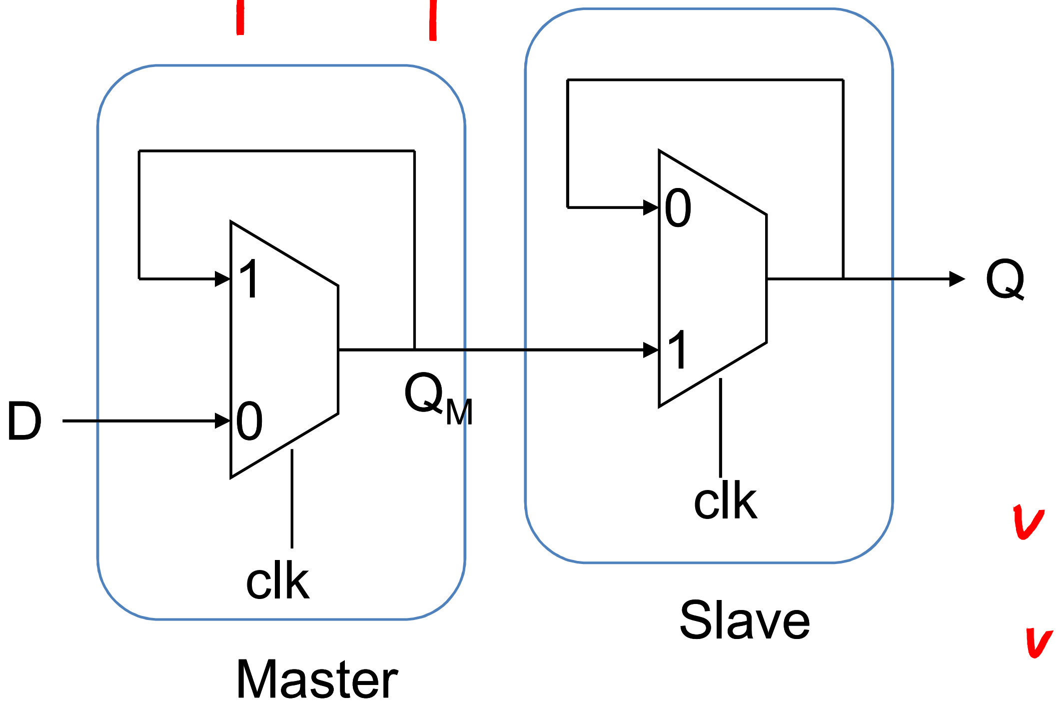
Enable

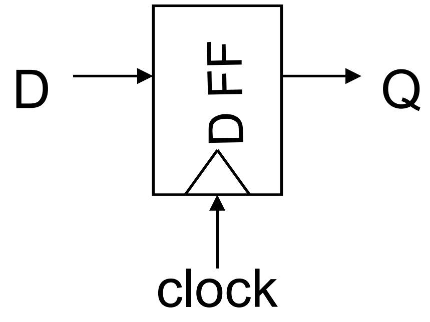
- Ignore clock when en = 0
  - MUX: increase D-to-Q delay
  - Clock gating: increase set-up time and skew



Sequencing Elements Characterization

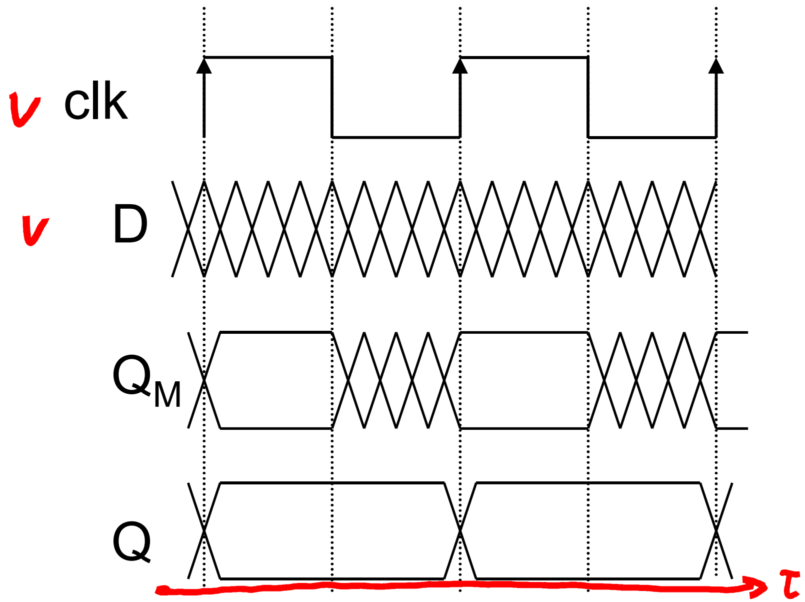
- Master-slave-based edge-triggered flip-flop



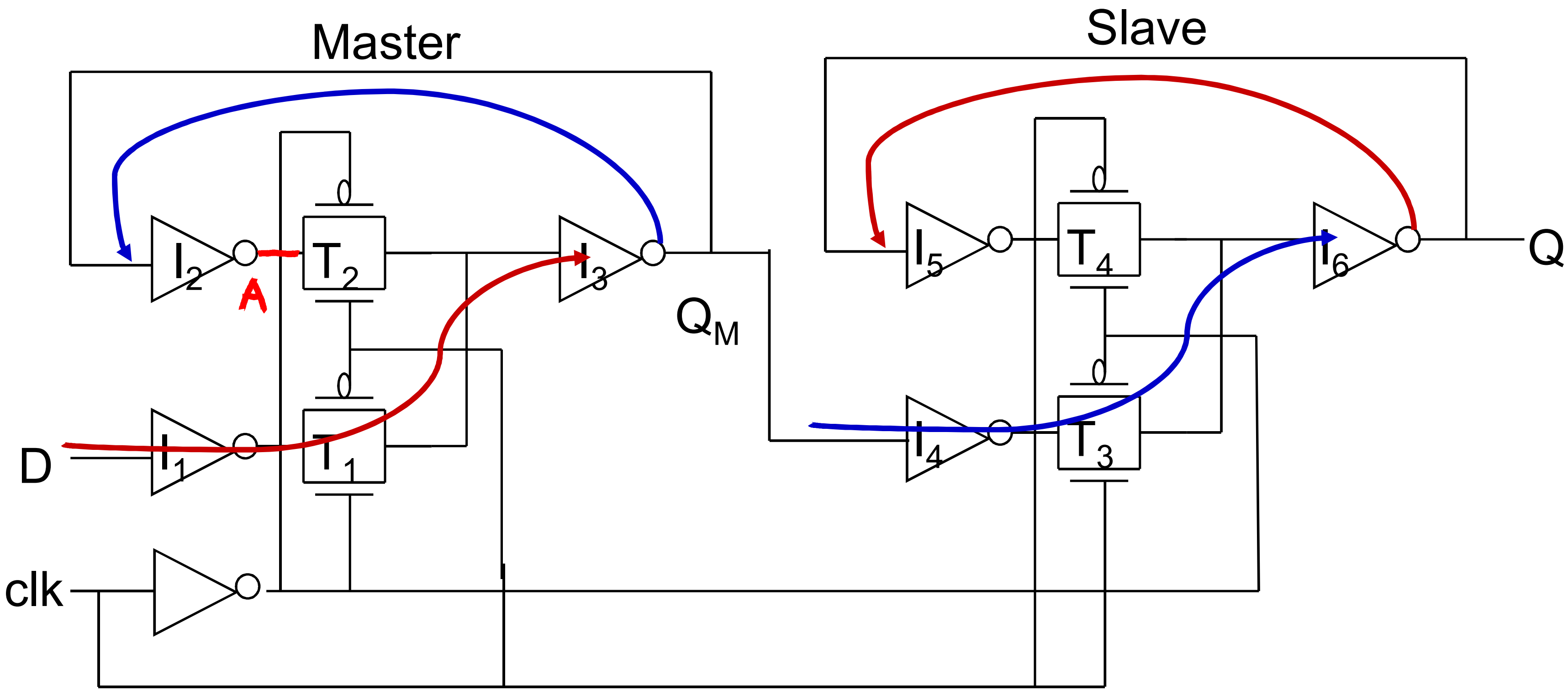


clk = 0 transparent hold

clk = 0→1 hold transparent



Implementation



Timing Properties

- Assume
  - Propagation delays are tpd_inv and tpd_tx
  - Contamination delay is 0
  - Inverter delay to clk is 0

- Setup time: time before rising edge of clk that D must be valid

$$t_{su} = 3 * t_{pd\_inv} + t_{pd\_tx}$$

- Propagation delay: time for D to reach Q

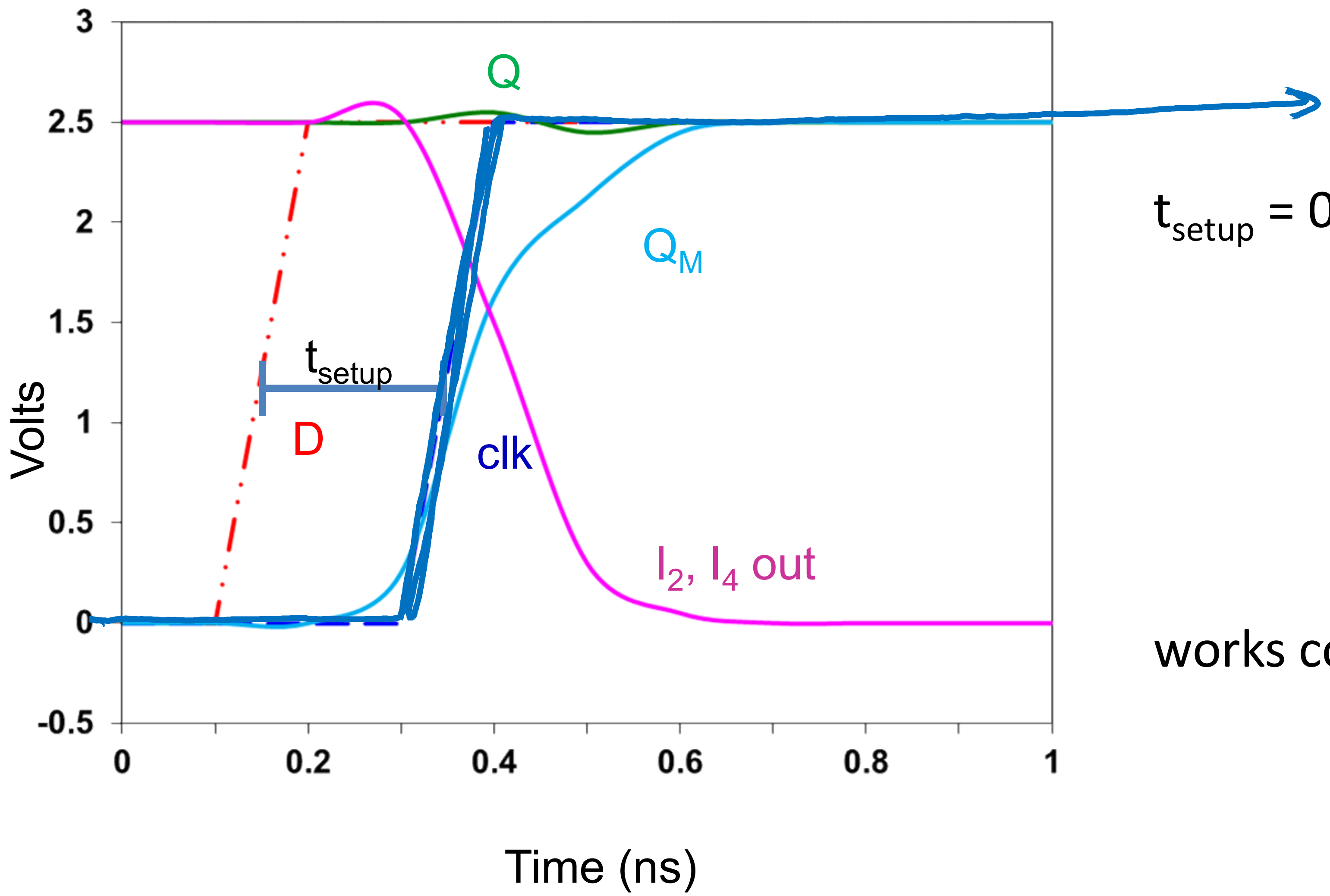
$$t_{c2q} = t_{pd\_inv} + t_{pd\_tx}$$

- Hold time: time D must be stable after rising edge of clk

$$t_{hold} = \text{zero}$$

  - Slow clock can cause both latches transparent and increase hold time

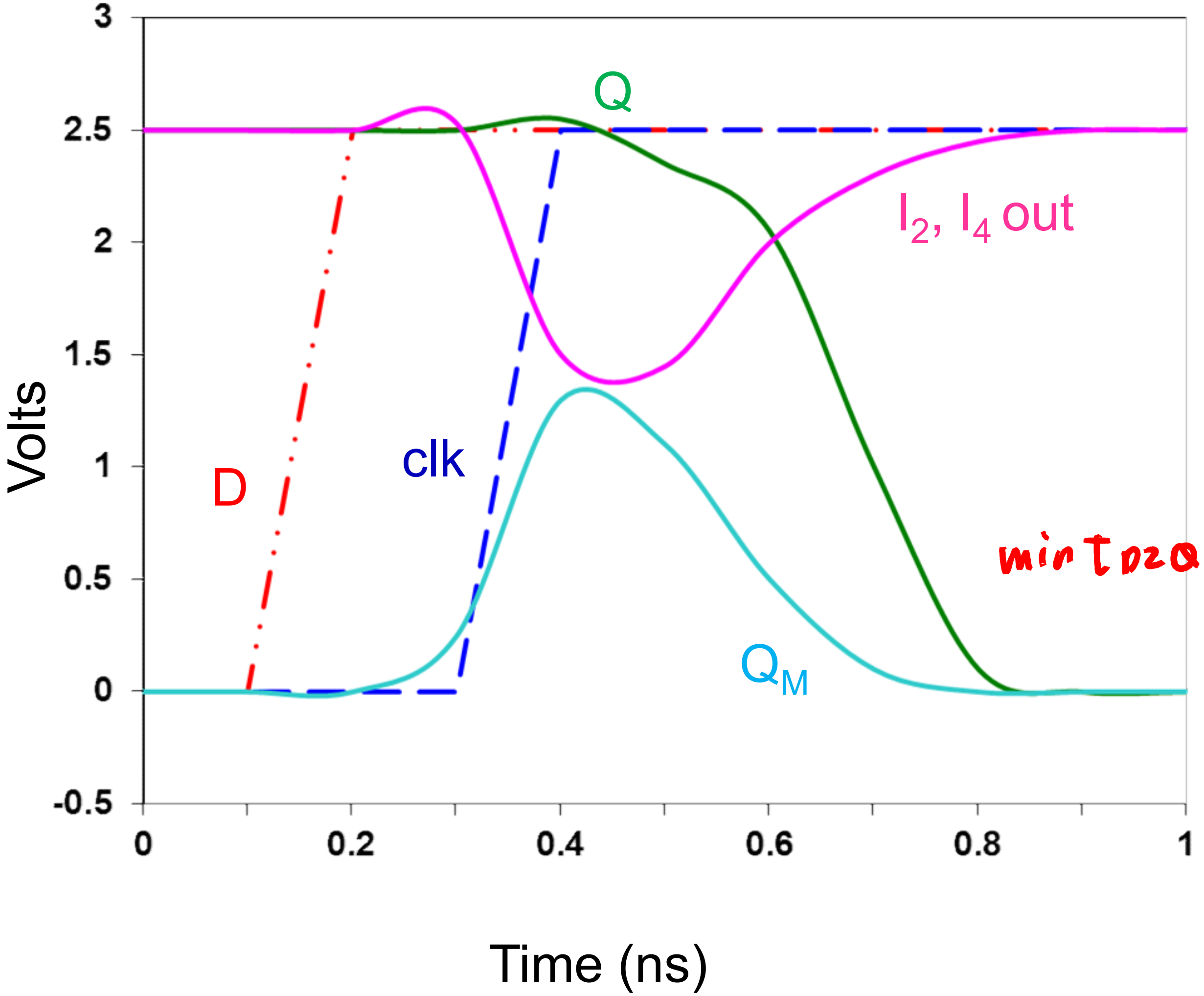
Setup Time Simulation (I)



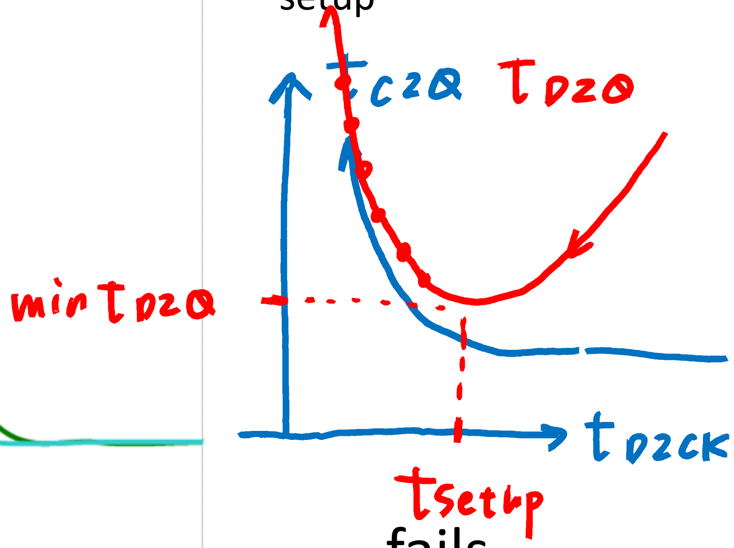
t_{setup} = 0.21 ns

works correctly

Setup Time Simulation (II)



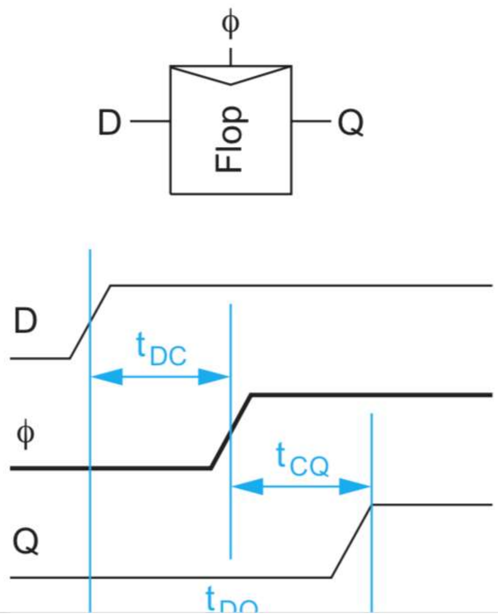
t_{setup} = 0.20 ns

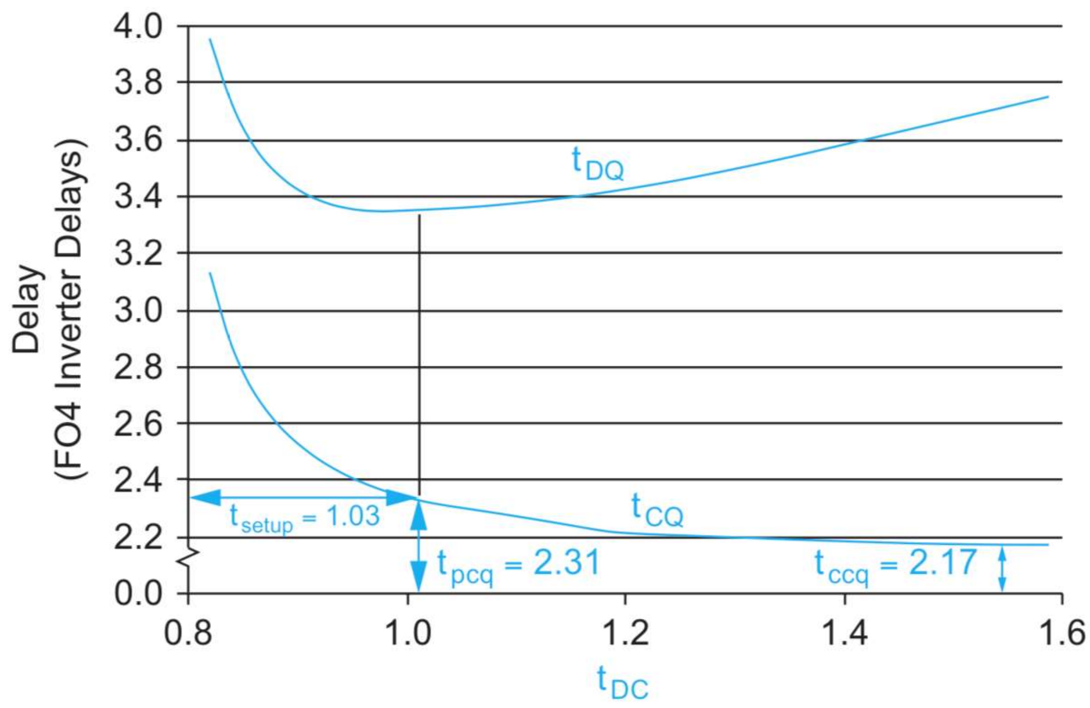


fails

Sequencing Element Characterization (I)

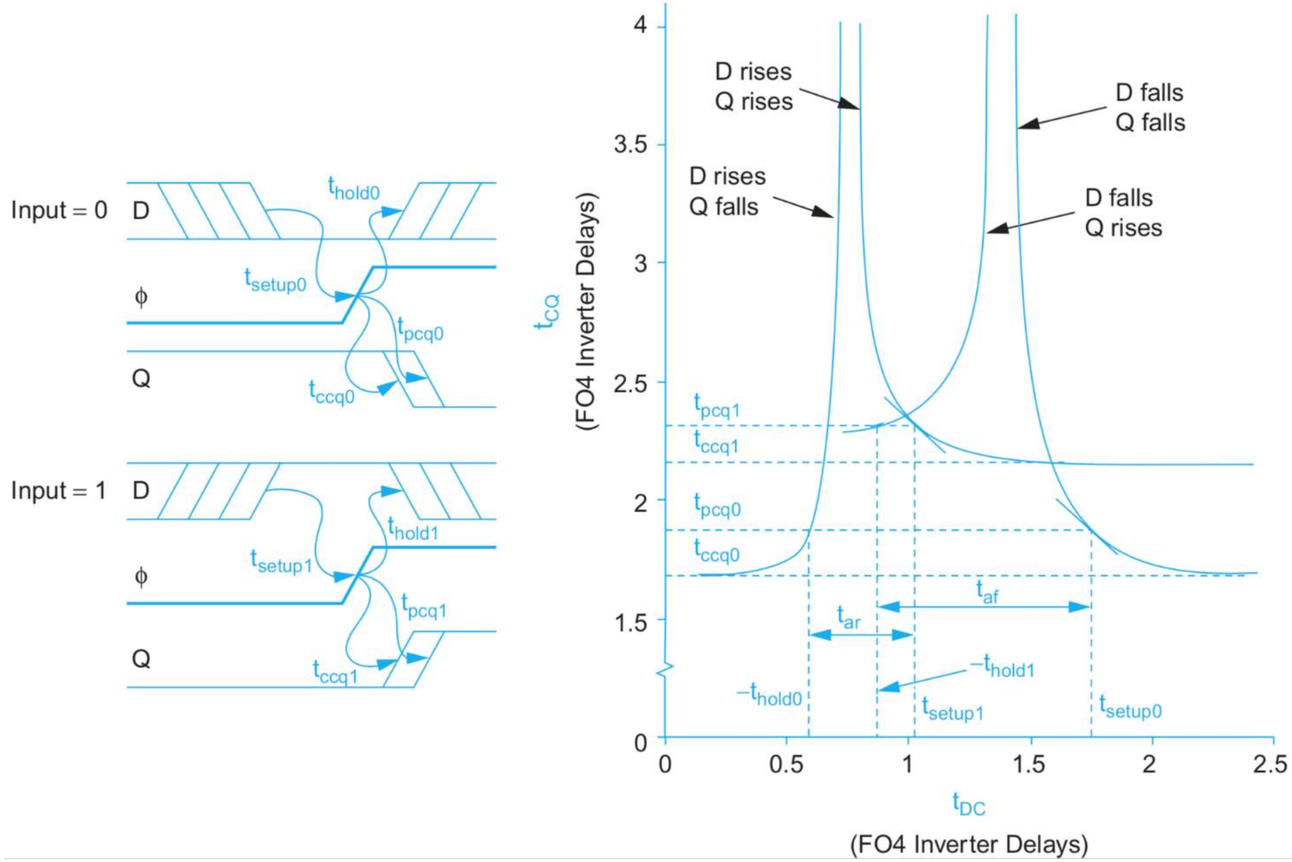
- **Flip flops**
- Setup time: minimize t_{D2Q}





Sequencing Element Characterization (II)

- Hold time: min. time from clock to D for $t_{C2Q} < t_{pcq}$
- Aperture width: the width of timing window around clock edge during which data must not transition



Sequencing Element Characterization (III)

- **Latches**
- Setup time: t_{D2Q} 5% greater than min. value