
ch15, ch1.5

EE3230 Lecture 2: CMOS Processing Technology

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Outline

- **CMOS Technology**
- Layout Design Rules
- CMOS Process Enhancements
- Manufacturing Issues

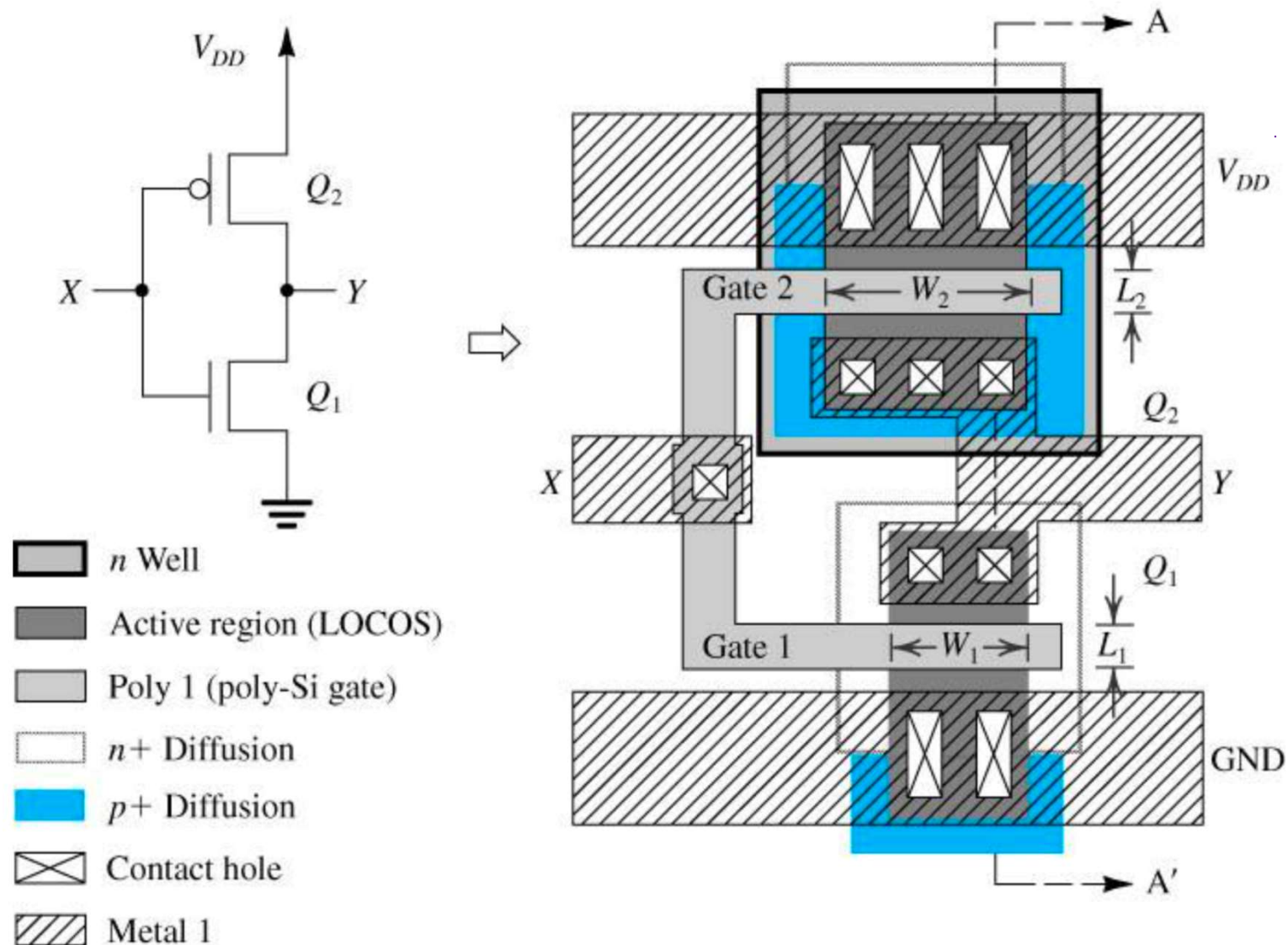
CMOS Technologies

- n-well process: p-substrate
- p-well process: n-substrate
- Twin-well process
 - Optimized for each transistor type
- Triple-well process (deep n-well)
 - Good isolation between analog and digital blocks
- BiCMOS process (SiGe)
- Silicon-on-insulator (SOI) process

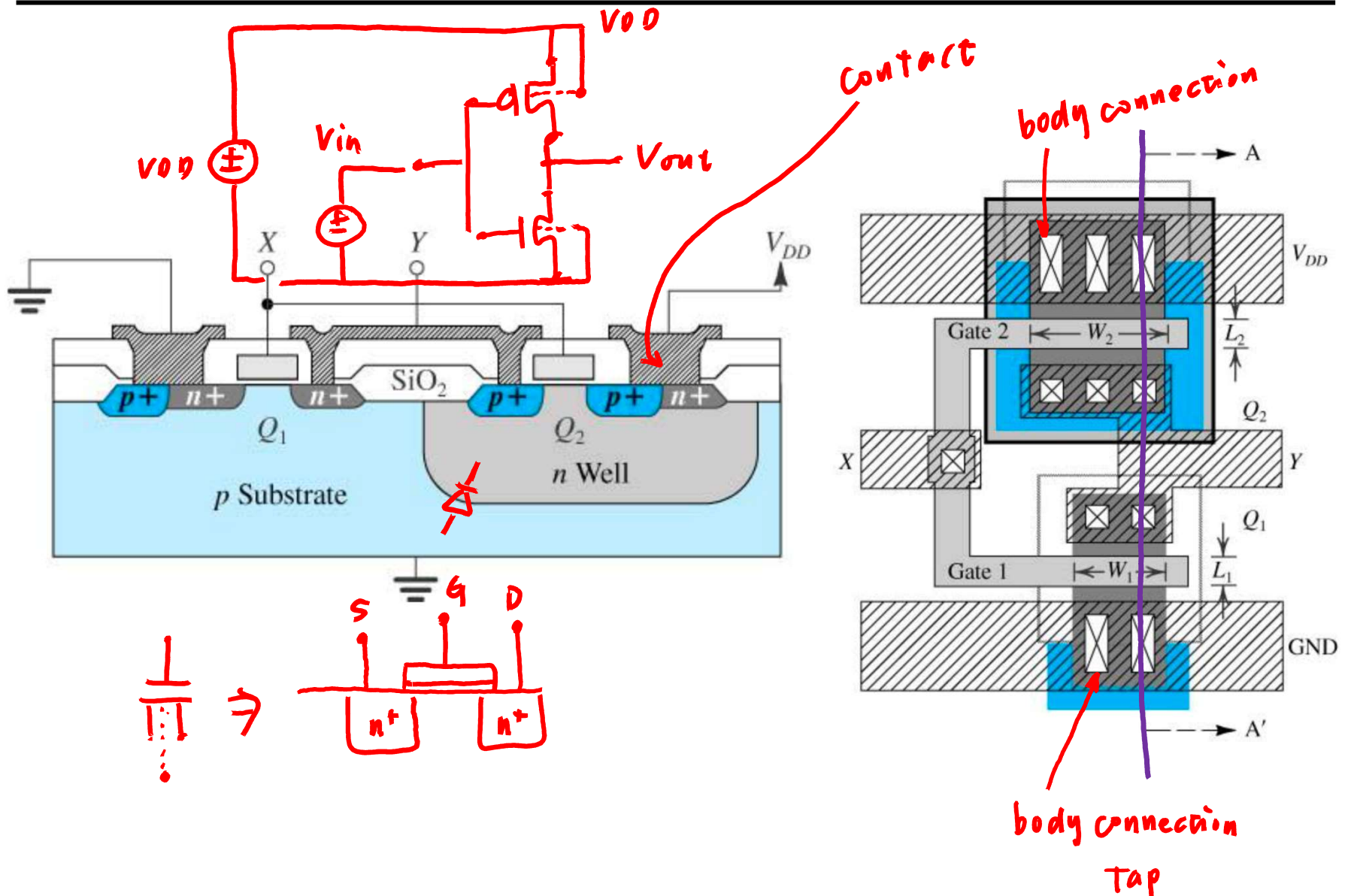
Process Steps

- Wafer formation
- Photolithography 光蝕刻
- Well and channel formation
- Isolation
- Gate oxide
- Gate & source/drain formation
- Contacts and metalization
- Passivation

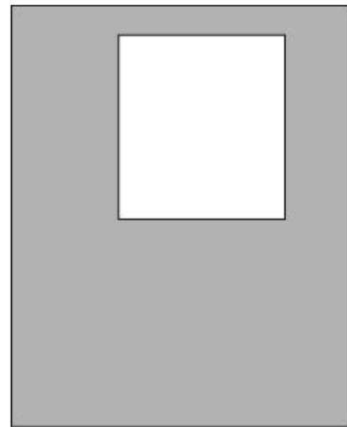
Schematic and Layout of CMOS Inverter



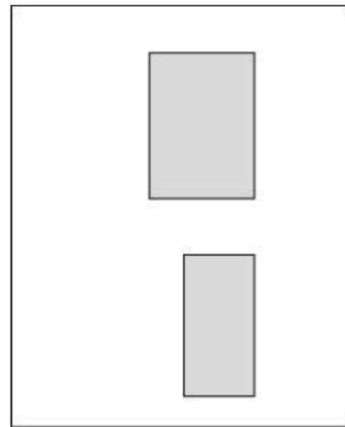
Cross Section of CMOS Inverter



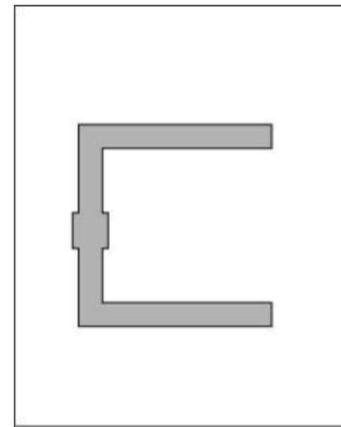
Photomasks of n-well CMOS Inverter



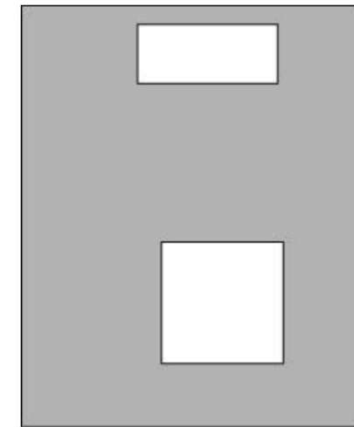
(a) n Well



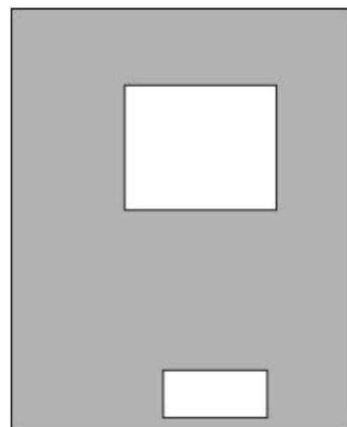
(b) Active region



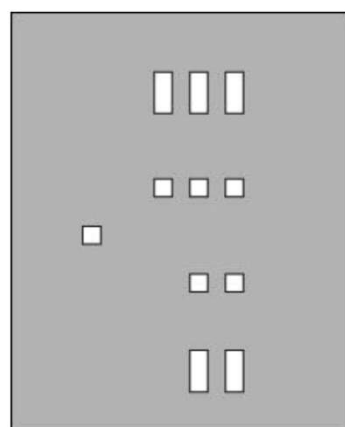
(c) Poly 1



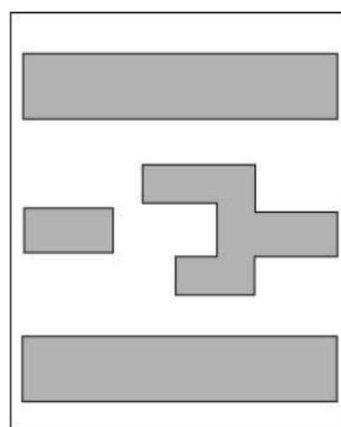
(d) $n+$ Diffusion



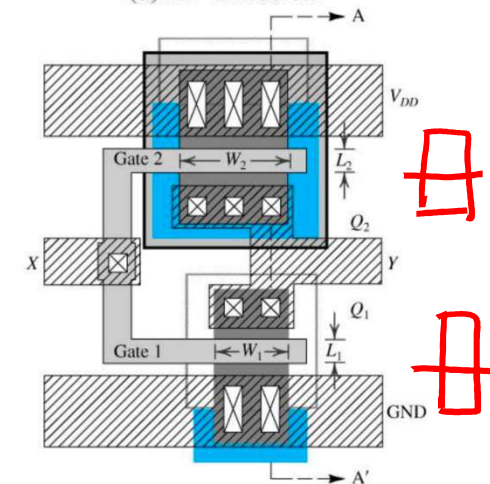
(e) $p+$ Diffusion



(f) Contact hole



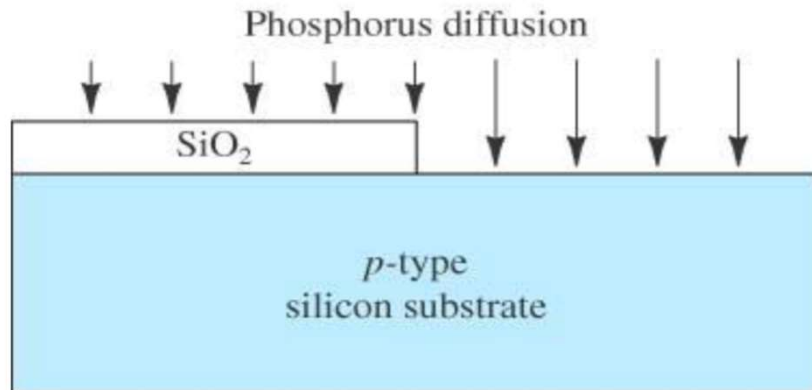
(g) Metal 1



n-well CMOS Process (I)

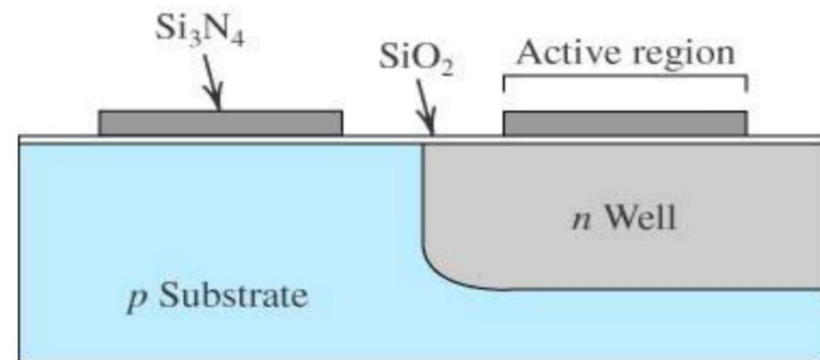
(a) (mask #1)

Define n-well diffusion



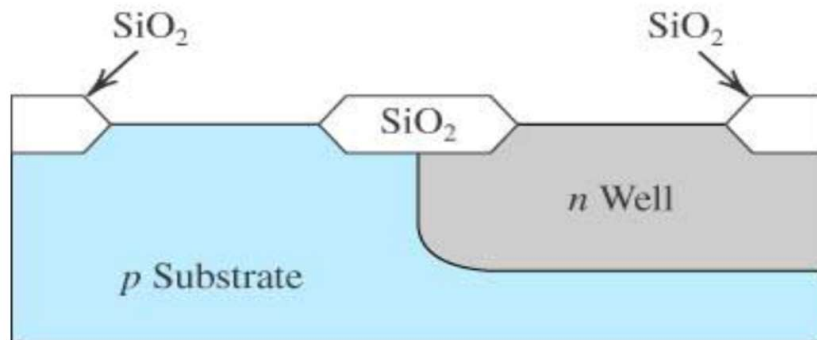
(b) (mask #2)

Define active regions (think oxide)



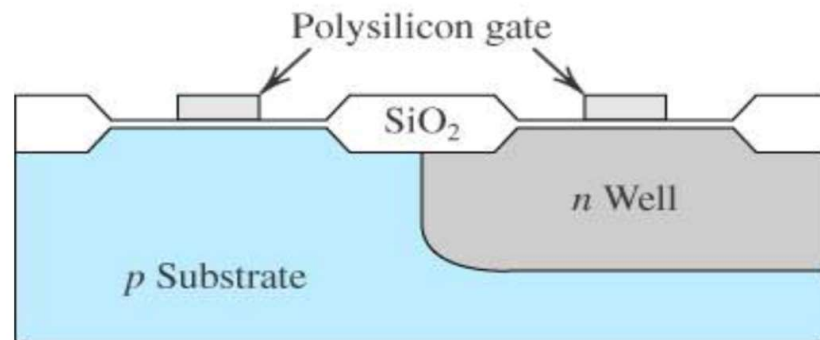
(c)

LOCOS oxidation(field oxide)



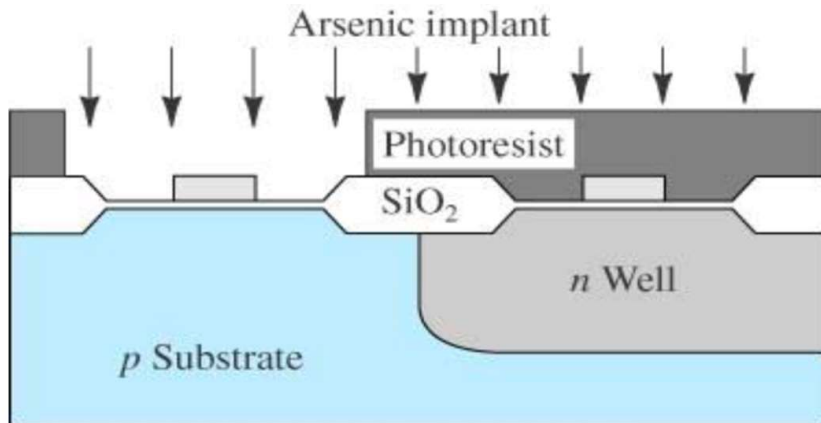
(d) (mask #3)

Polysilicon gate

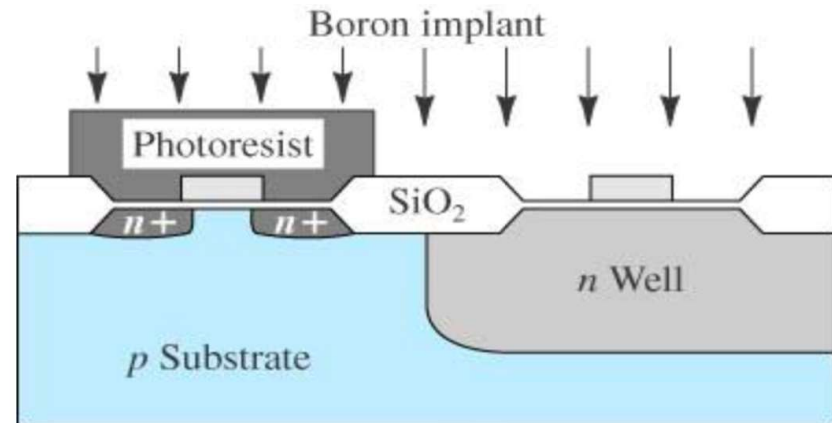


n-well CMOS Process (II)

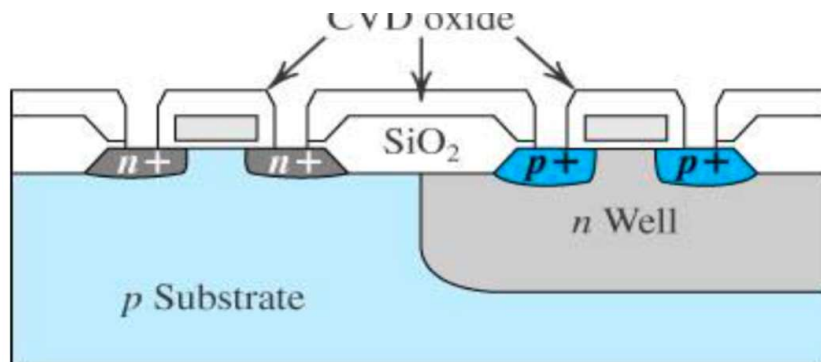
(e) (mask #4)
 n^+ diffusion



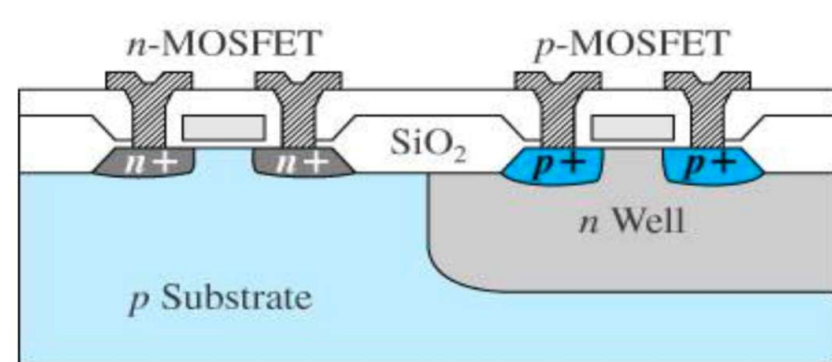
(f) (mask #5)
 p^+ diffusion



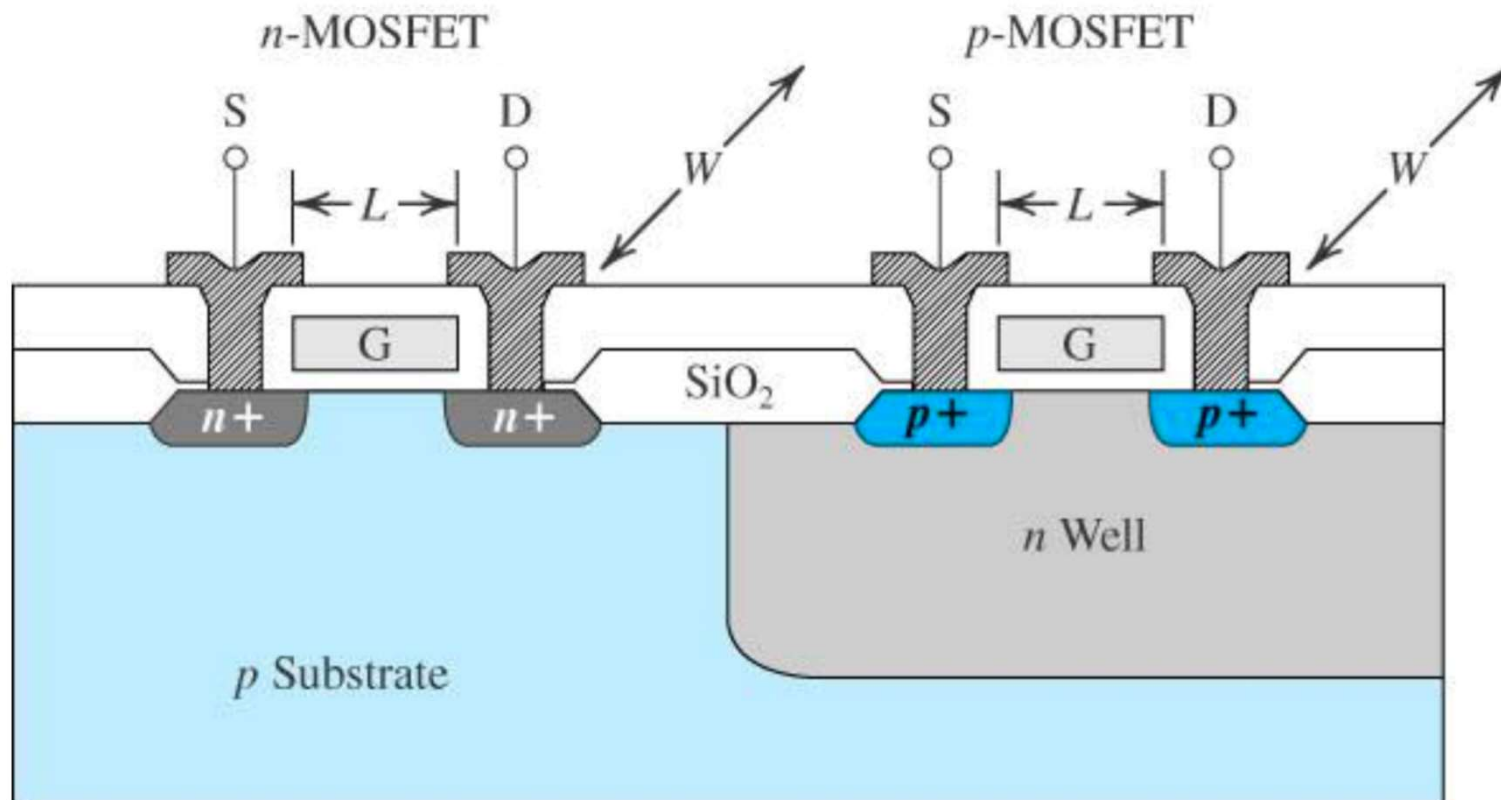
(g) (mask #6)
Contact holes



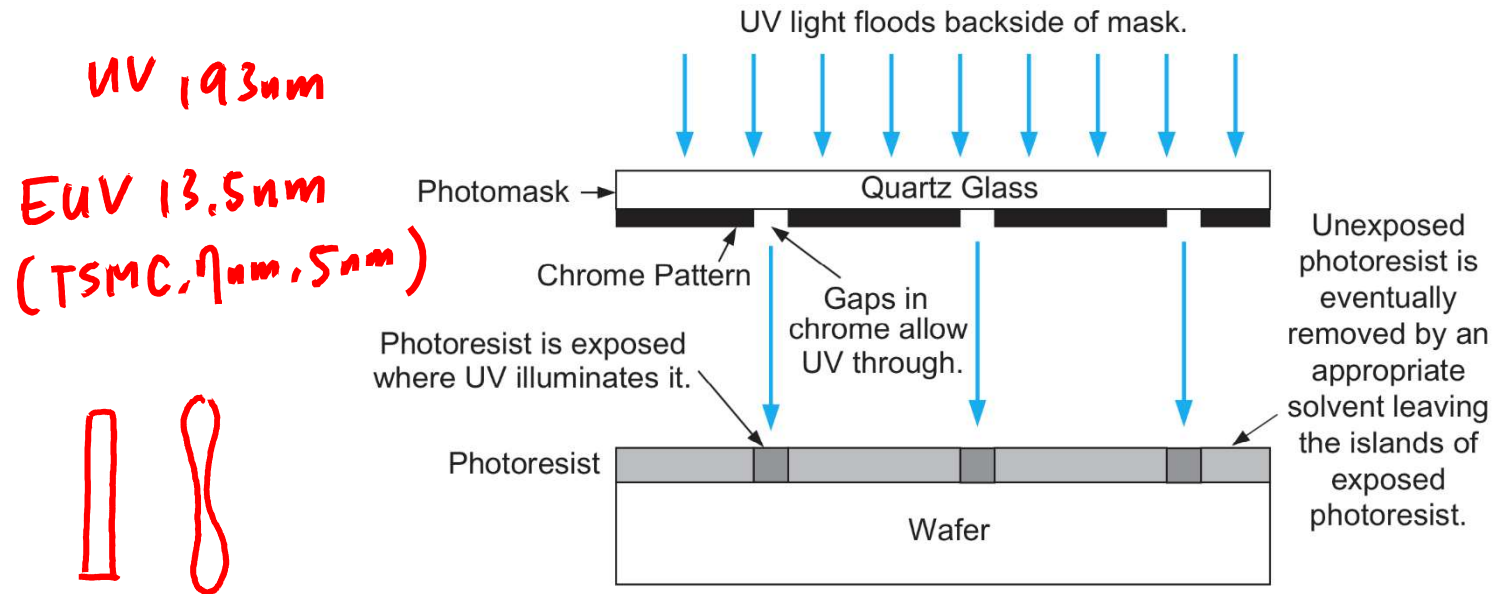
(h) (mask #7)
Metalization



Cross-Sectional Diagram of MOSFET

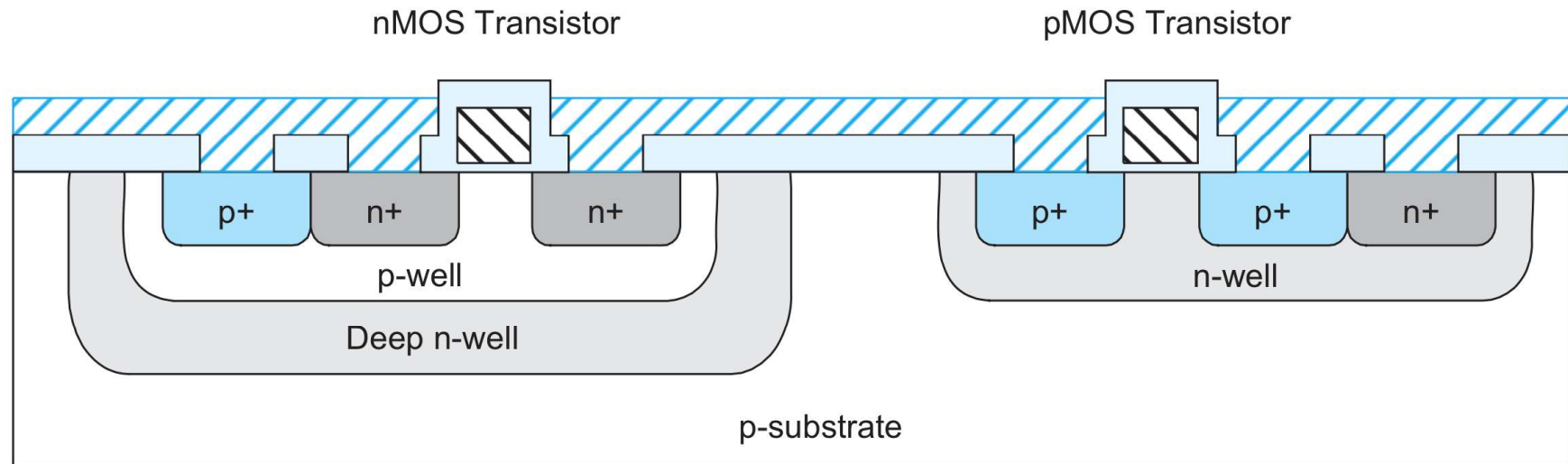


Photolithography



- Greek: *Photo*(light)+*lithos*(stone)+*graph*(picture)
 - Carving pictures into stone using light
- Resolution enhancement techniques
 - **Optimal proximity correction (OPC)**: local pre-distortion, **phase shift masks (PSM)**: light diffraction, **off-axis illumination: (OAI)**, contrast enhancement of repetitive pattern

Well and Channel Formation



Doping

- Vary portions of donor (n) and acceptor (p)

- Epitaxy: single-crystal film growth
- Deposition: chemical vapor deposition + drive-in
- Implantation: ion implantation + diffusion + annealing
(standard well and source/drain definition)

process variation



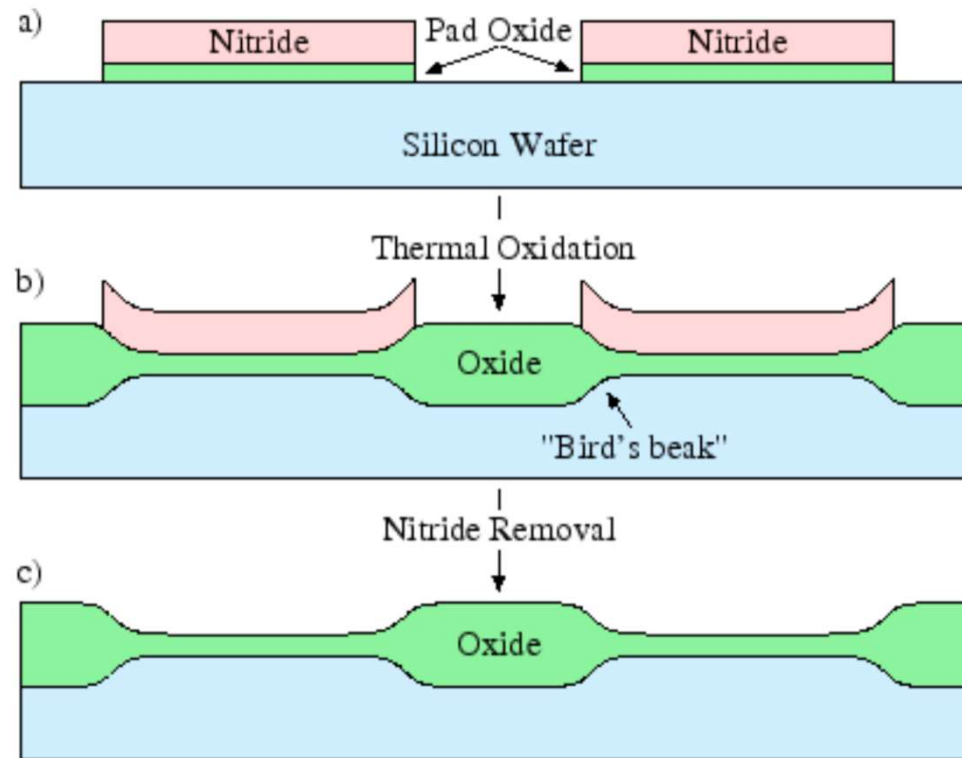
便分布均匀

Silicon Dioxide (SiO₂)

- Wet oxidation
 - Oxidizing atmosphere contains water vapor
temp: 900~1000°C, quick for thick field oxide
- Dry oxidation
 - Oxidizing atmosphere is pure oxygen
temp: ~1200°C, highly controlled thin gate oxide
- Atomic layer deposition
 - Thin chemical layer deposition for various requirement
(SiO₂, metal, dielectric)

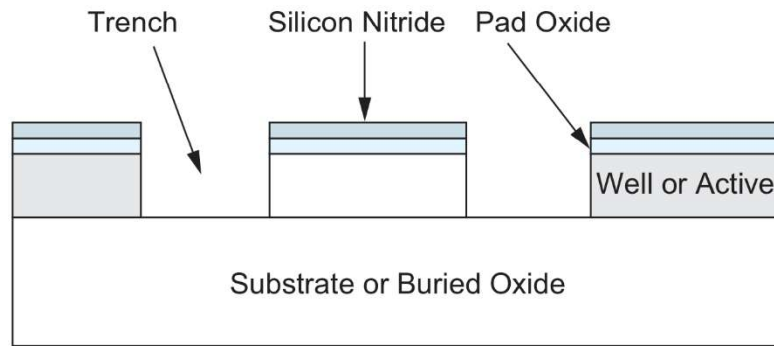
Isolation: LOCOS

field oxide

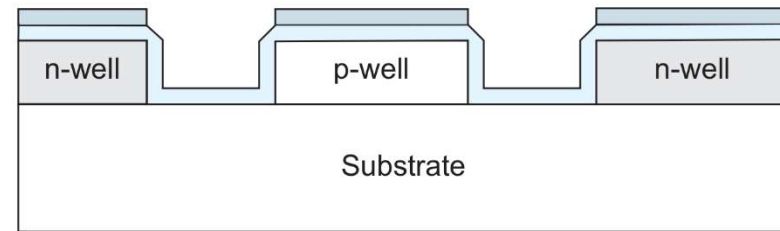


- Local Oxidation of Silicon (LOCOS)
 - Low density, high electrical field: bird's beak shape

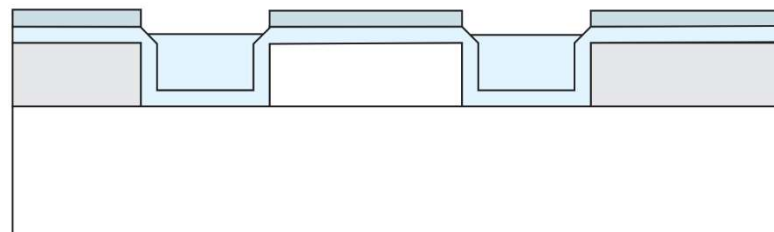
Isolation: STI



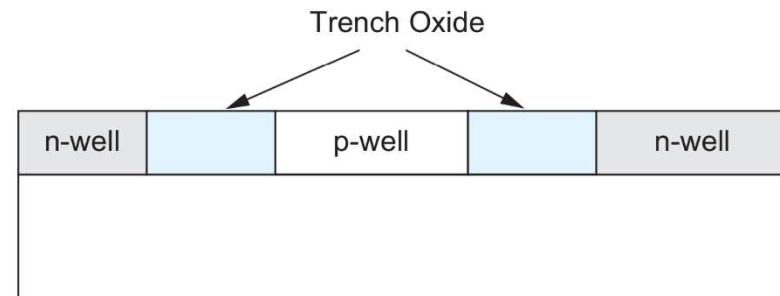
(a) Trench Etch



(b) Liner Oxidation



(c) Fill Trench with Dielectric



(d) CMP for Planarization

- Shallow Trench Isolation (STI)
 - High density and better isolation, need chemical mechanical polishing (CMP) to planarize the structure

Gate Oxide

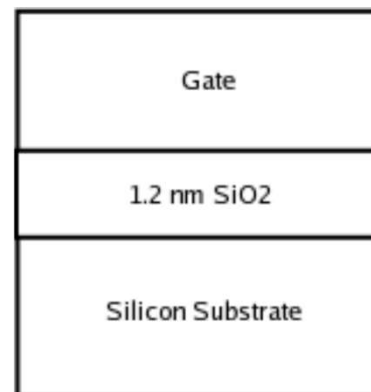
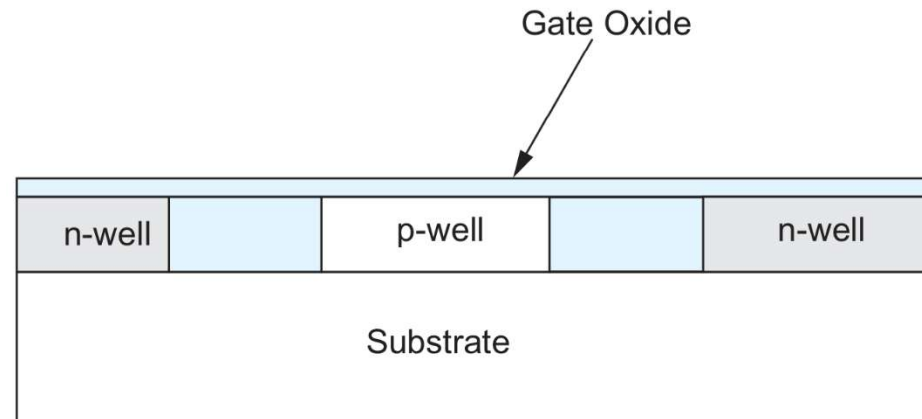
thin oxide

- Shorter gate length
→ thinner gate oxide

- Effective Oxide Thickness (EOT)
 - Decrease EOT using stack gate structure with high-k dielectric

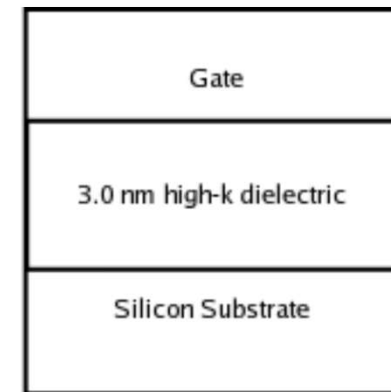
@ 60 nm EOT 10~15 Å

- Dual gate oxide for core and I/O



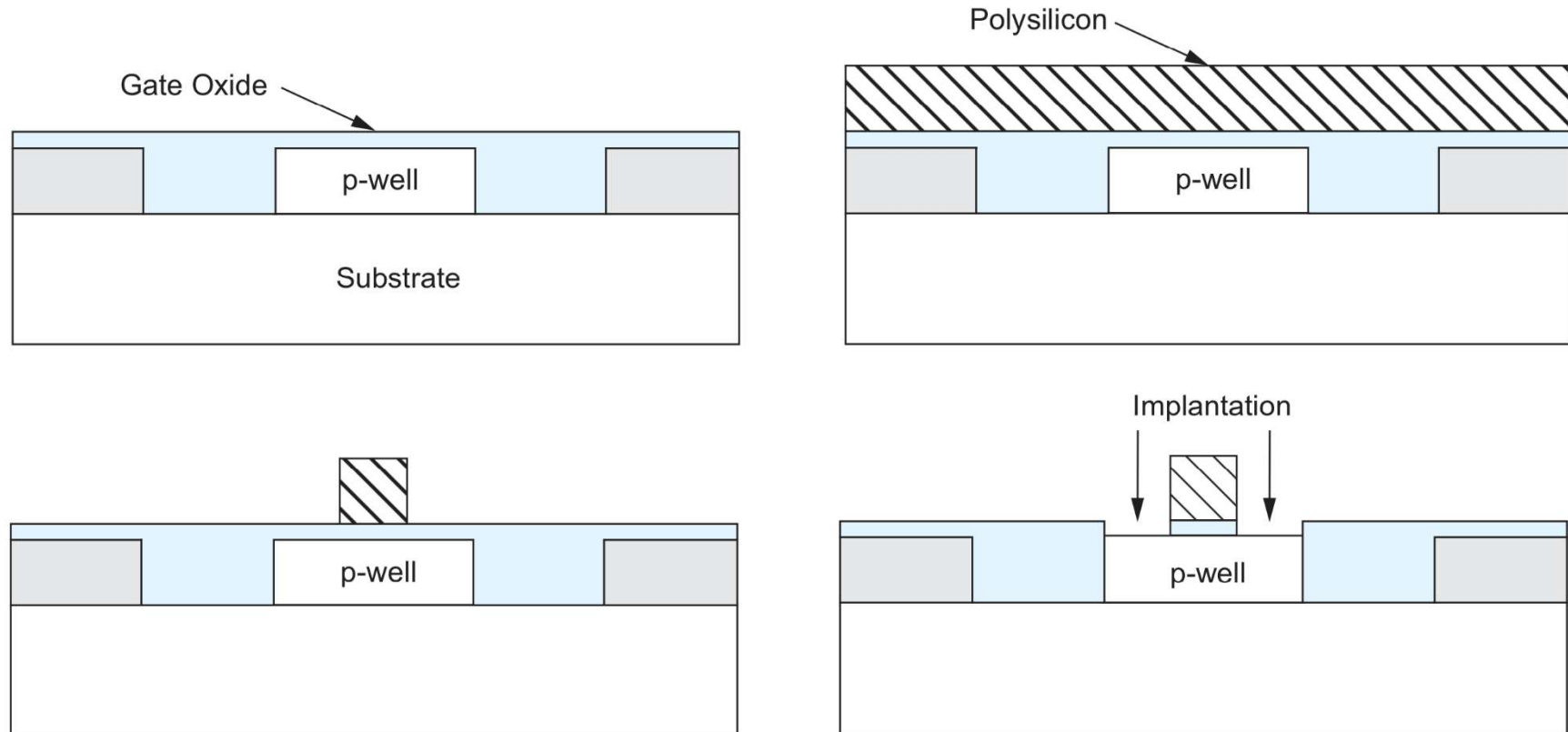
Existing 90 nm Process
Capacitance = 1 x
Leakage Current = 1 x

$$C = \frac{\kappa \epsilon_0 A}{t}$$



A potential high-k process
Capacitance = 1.6 x
Leakage Current = 0.01 x

Gate & Source/Drain Formation



- Self-aligned poly-silicon (poly) gate
- Lightly doped drain (LDD) structure

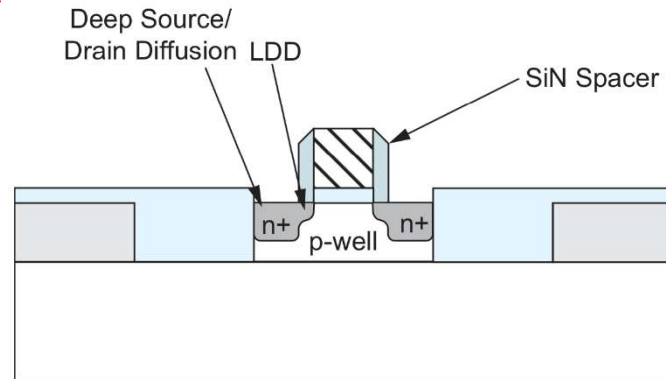
lightly-doped drain

LDD & Salicide

- LDD

short-channel effect

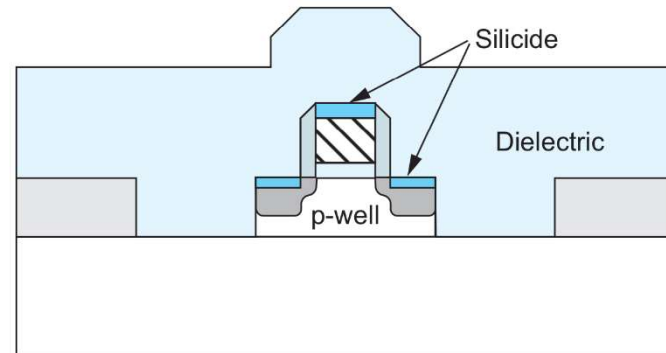
- Reduce electrical field of drain junction and hot-electron damage
- High sheet resistance



- Salicide:

self-aligned silicide

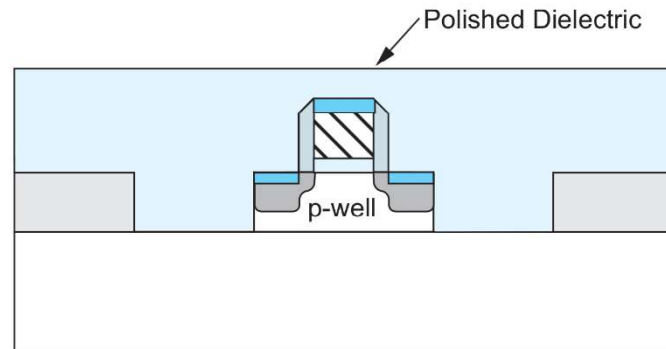
- Refractory metal to reduce interconnection resistance of gate, source/drain



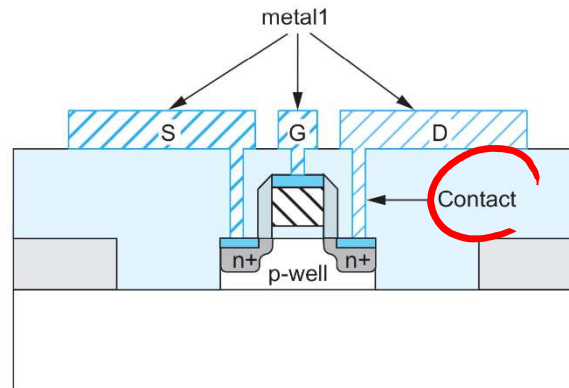
chemical mechanical planarization

- CMP

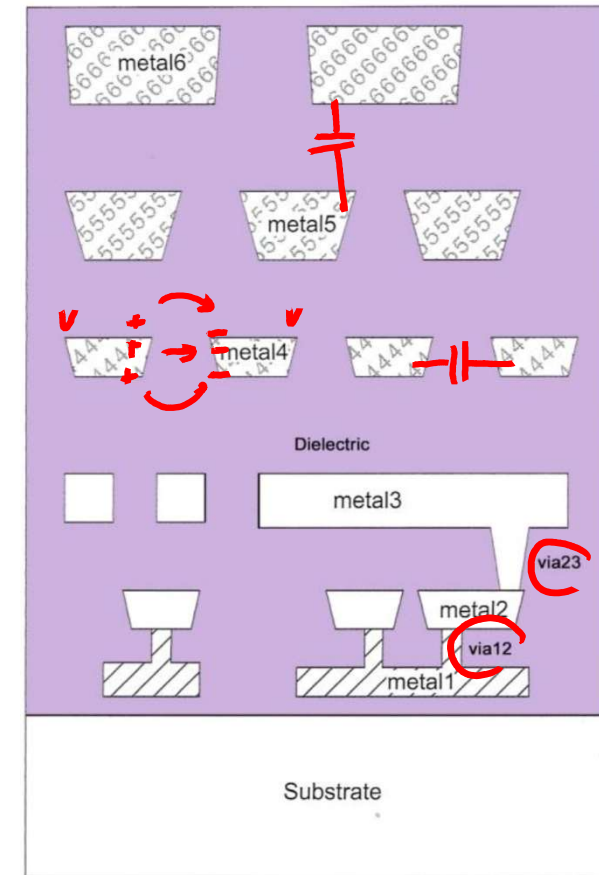
- Structure planarization for further stack process



Contacts and Metalization



- Contact
 - Poly-to-metal
 - diffusion-to-metal
- VIA
 - Metal-to-metal
- CMP
 - Structure planarization
 - for further stacking processes



Outline

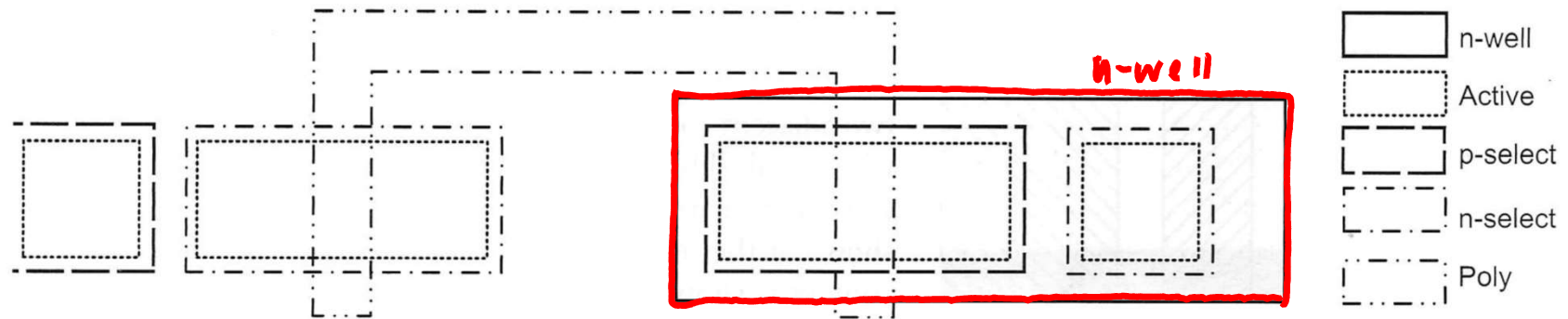
- CMOS Technology
- **Layout Design Rules** *DRC rules*
- CMOS Process Enhancements
- Manufacturing Issues

Layout Design Rules (I)

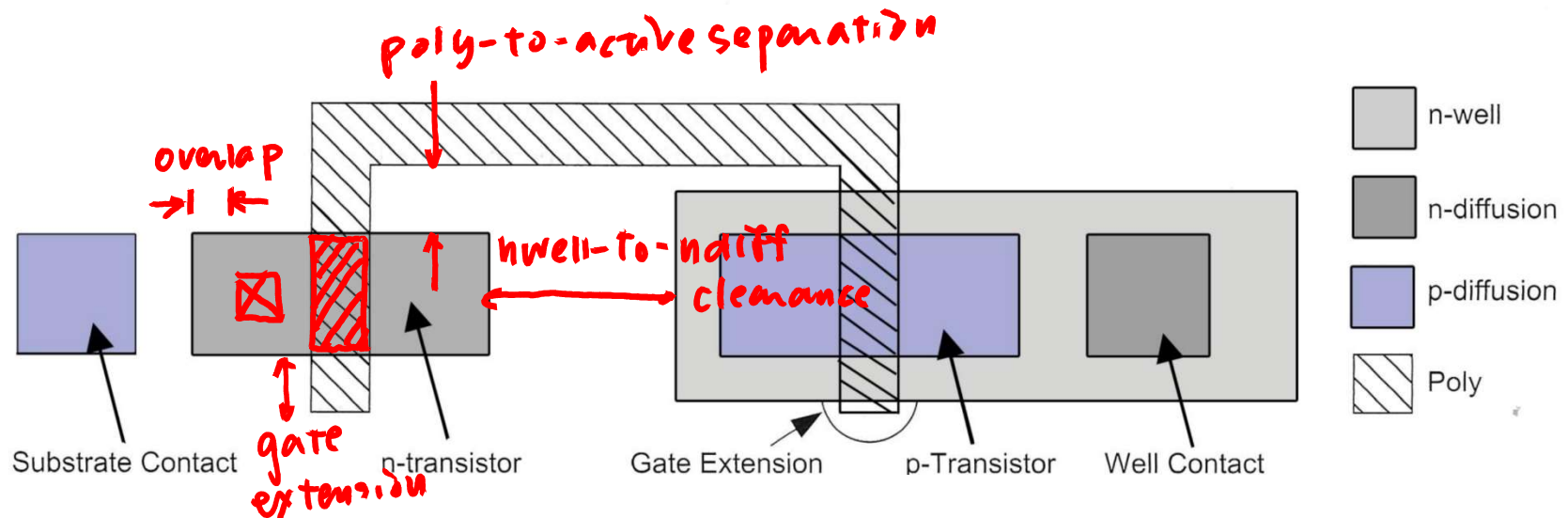
- Design rule: geometric constraint and tolerance for high probability of correct fabrication
 - Feature size, separations, and overlaps
- Well rule: isolation
- Transistor rule: channel quality
 - Poly, active region, n+/p+ implant
- Contact rule: single size for precise process control
- Metal and VIA rule: productivity and conductivity
 - Top metal with wider size, space and VIA rules

Layout Design Rules (II)

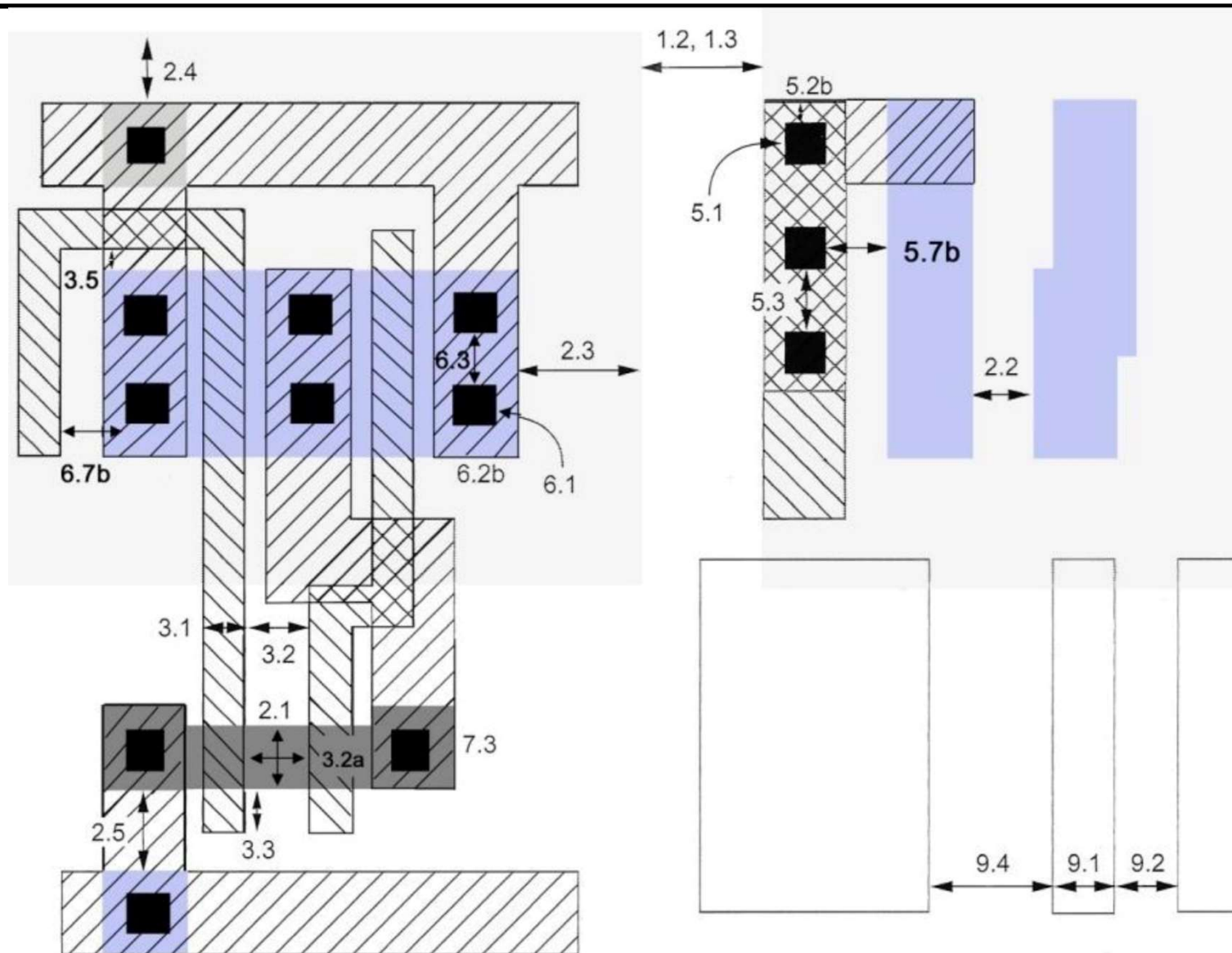
- N-well process transistors



(a)



Layout Design Rules (III)

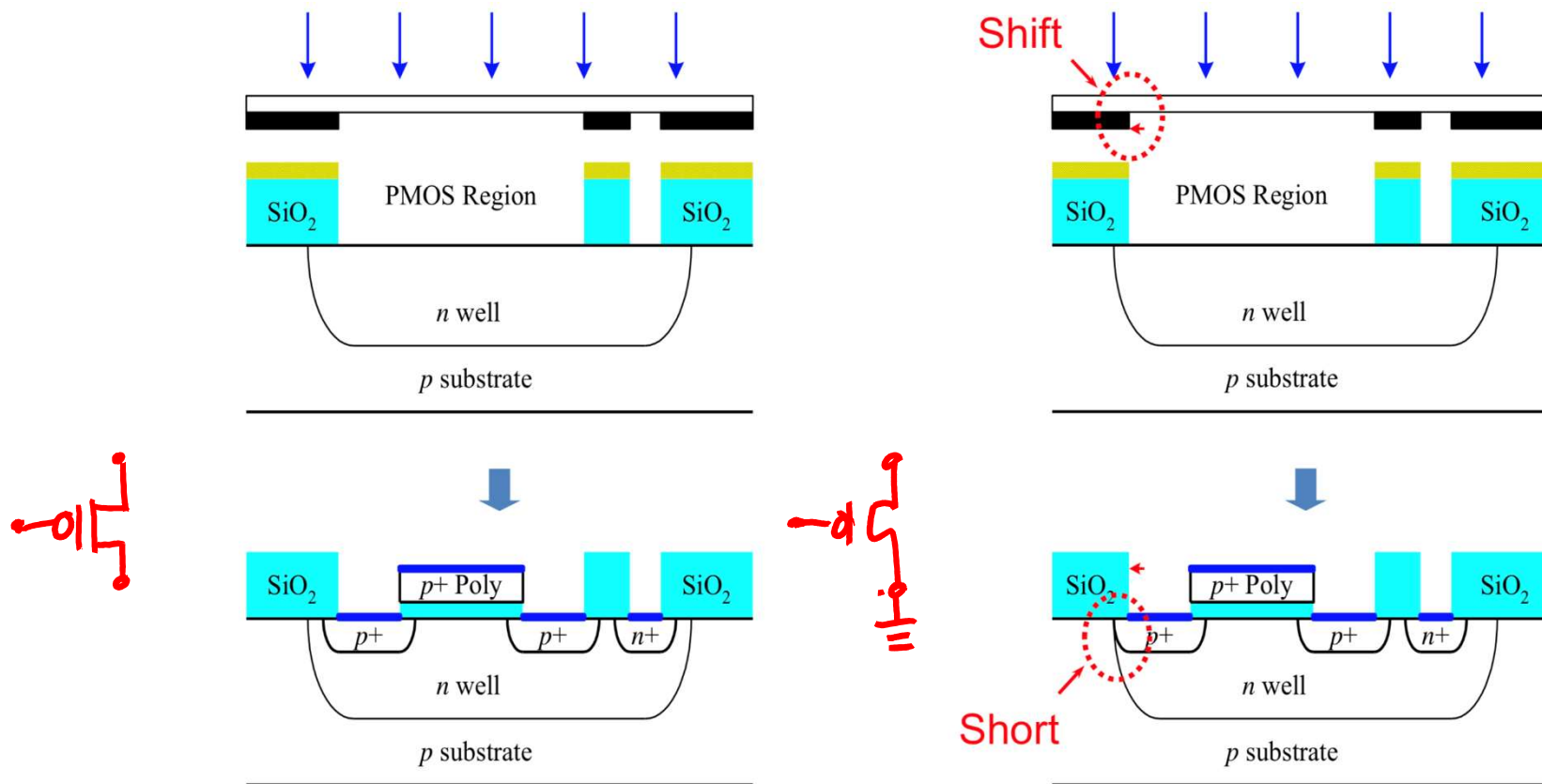


Layout Design Rules (IV)

Table 3.3 Micron design rules for 90nm process			
Layer	Rule	Description	90 nm rule (μm)
Well	1.1	Width	0.75
	1.2	Spacing to well at different potential	1.5
	1.3	Spacing to well at same potential	1.0
Active (diffusion)	2.1	Width	0.15
	2.2	Spacing to active	0.20
	2.3	Source/drain surround by well	0.25
	2.4	Substrate/well contact surround by well	0.25
	2.5	Spacing to active of opposite type	0.30
Poly	3.1	Width	0.09
	3.2	Spacing to poly over field oxide	0.15
	3.2a	Spacing to poly over active	0.15
	3.3	Gate extension beyond active	0.15
	3.4	Active extension beyond poly	0.15
	3.5	Spacing of poly to active	0.10
Select	4.1	Spacing from substrate/well contact to gate	0.25
	4.2	Overlap of active	0.20
	4.3	Overlap of substrate/well contact	0.10
	4.4	Spacing to select	0.30
Contact (to poly or active)	5.1, 6.1	Width (exact)	0.12
	5.2b, 6.2b	Overlap by poly or active	0.01
	5.3, 6.3	Spacing to contact	0.15
	5.4	Spacing to gate	0.10

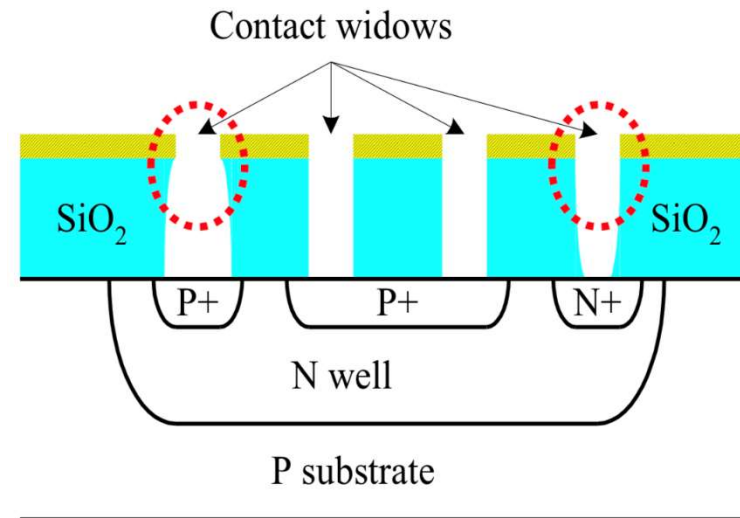
Design Rule Check (DRC) (I)

- To tolerate non-ideal effects and to guarantee successful device fabrication
- **Ex:** n-well and active region mask alignment error

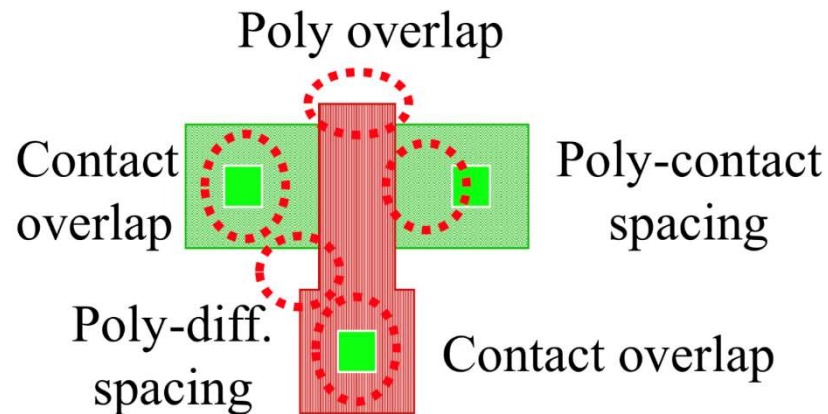


Design Rule Check (DRC) (II)

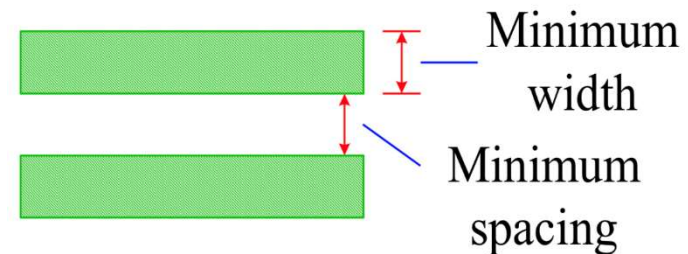
- Exposure and etching variation
- **Ex:** different contact windows
→ different contact resistance



alignment rules

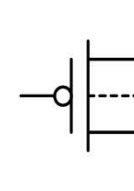
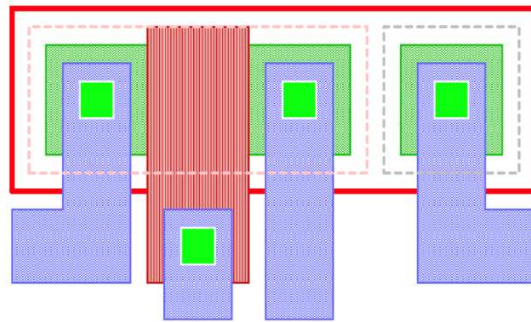


resolution rules

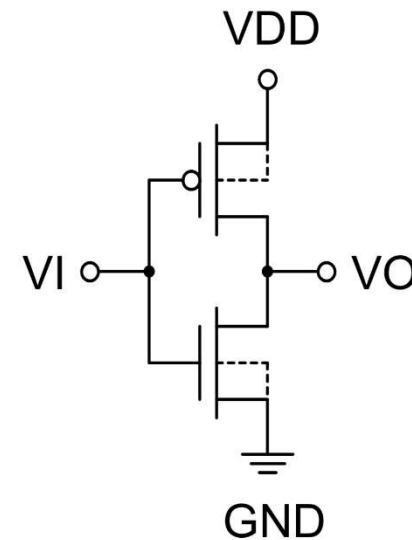
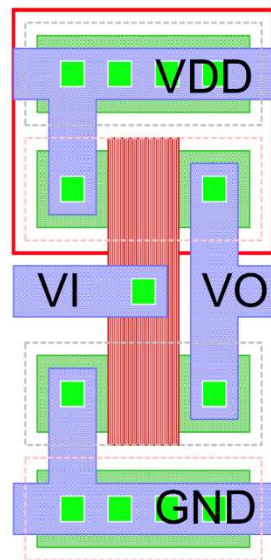


Layout vs. Schematic (LVS)

- To ensure layout is the same as *simulated* netlist
 - Check device parameters, interconnects, and I/O ports

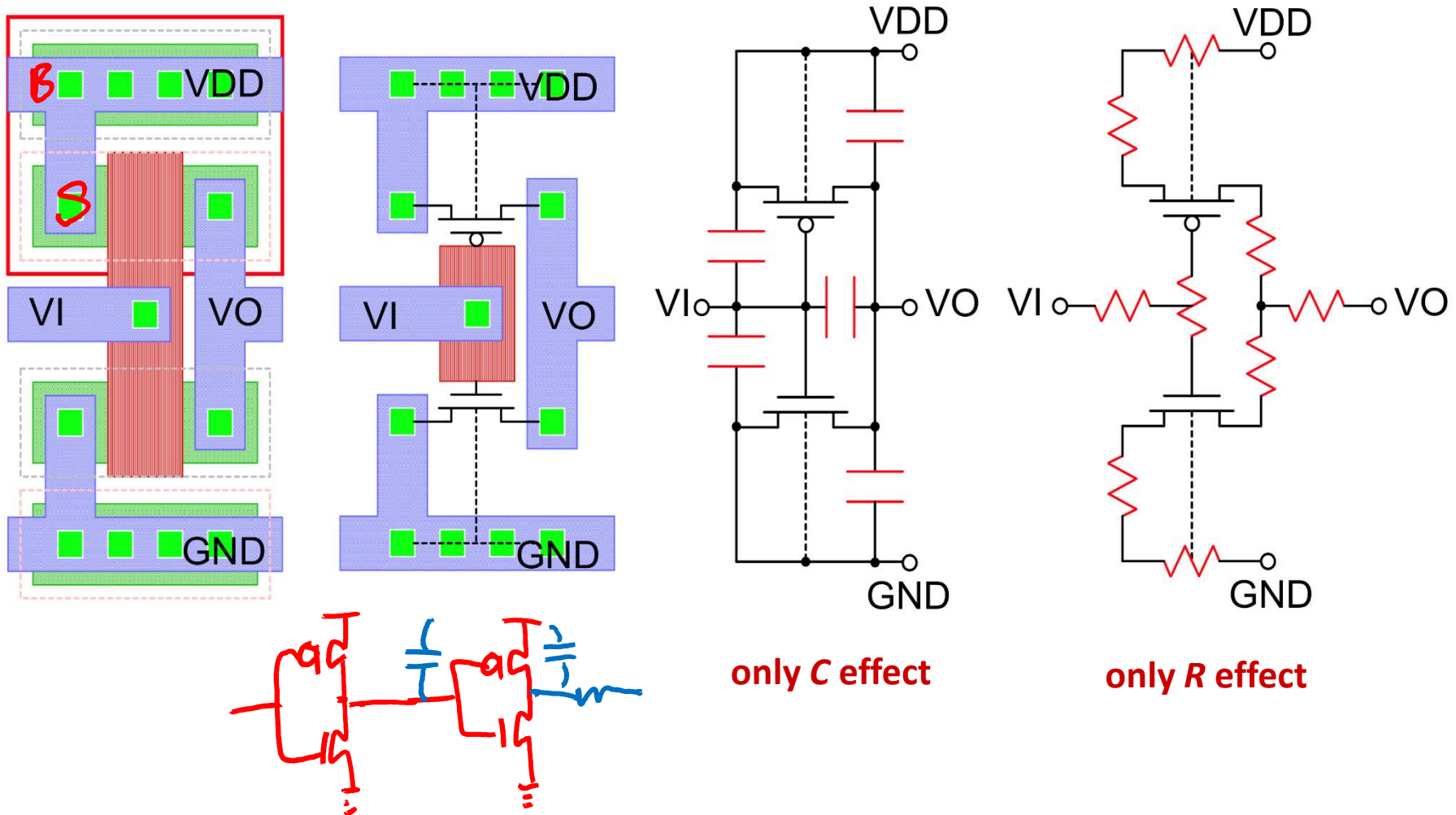


Model name
Channel width
Channel length



Parasitic Extraction (PEX)

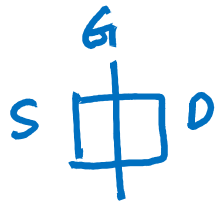
- Evaluate RC effects of interconnect (wires)



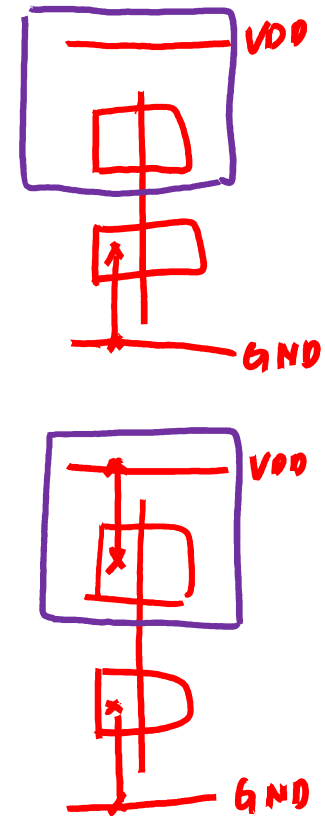
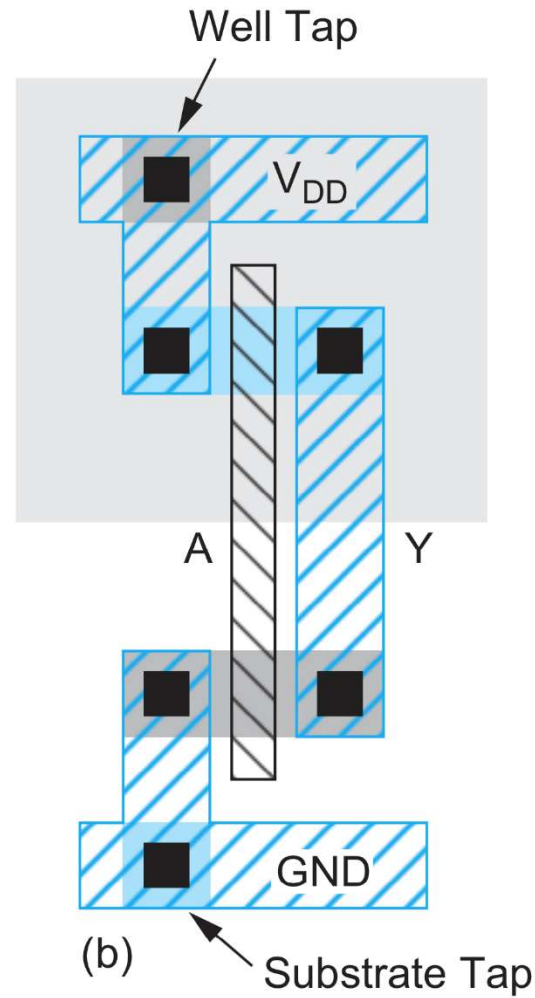
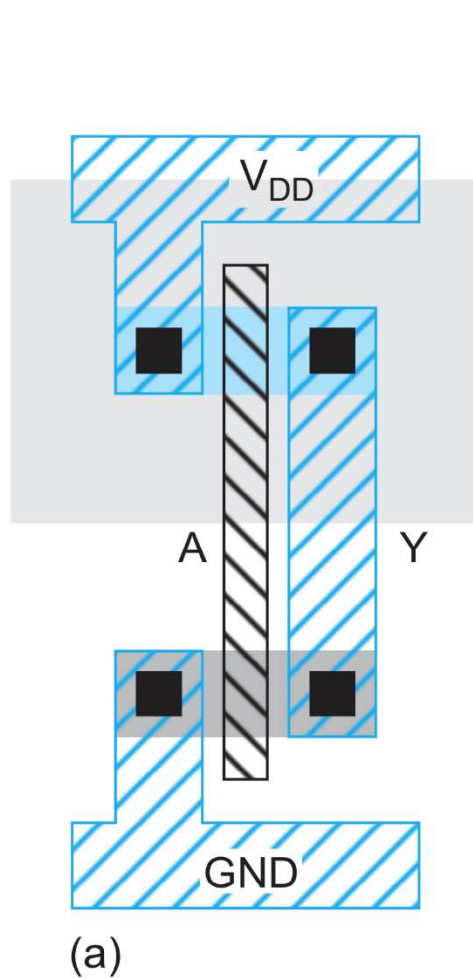
Gate Layout

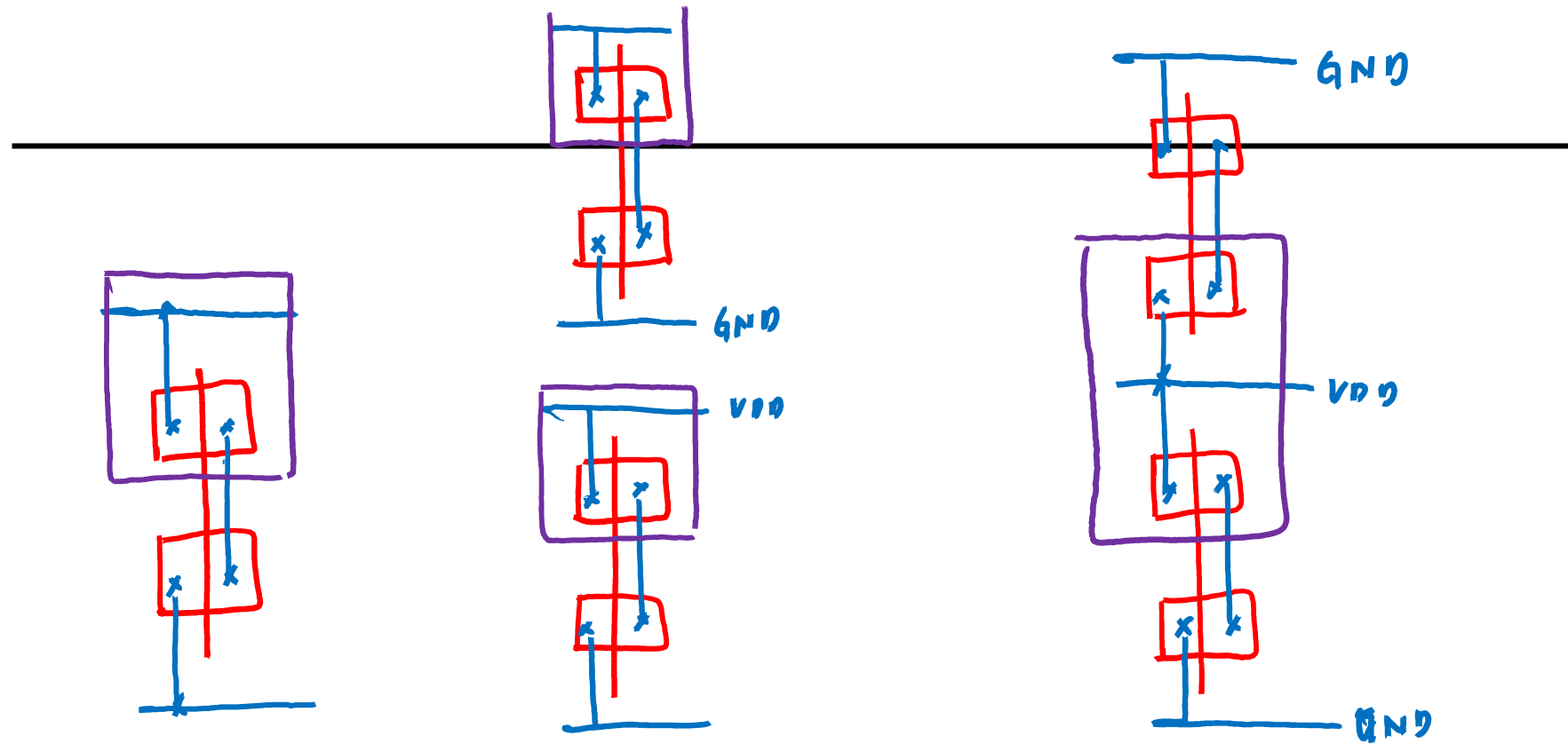
- Layout can be very time-consuming
 - Design gates to fit together nicely
 - Build a library of standard cells
- Standard cell design methodology
 - VDD and GND should abut (standard height)
 - Adjacent gates should satisfy design rules
 - NMOS at bottom and PMOS at top
 - All gates include well and substrate contacts

Example: Inverter



有时候会有
额外独立的
tap cell

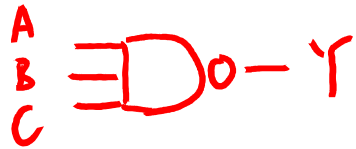




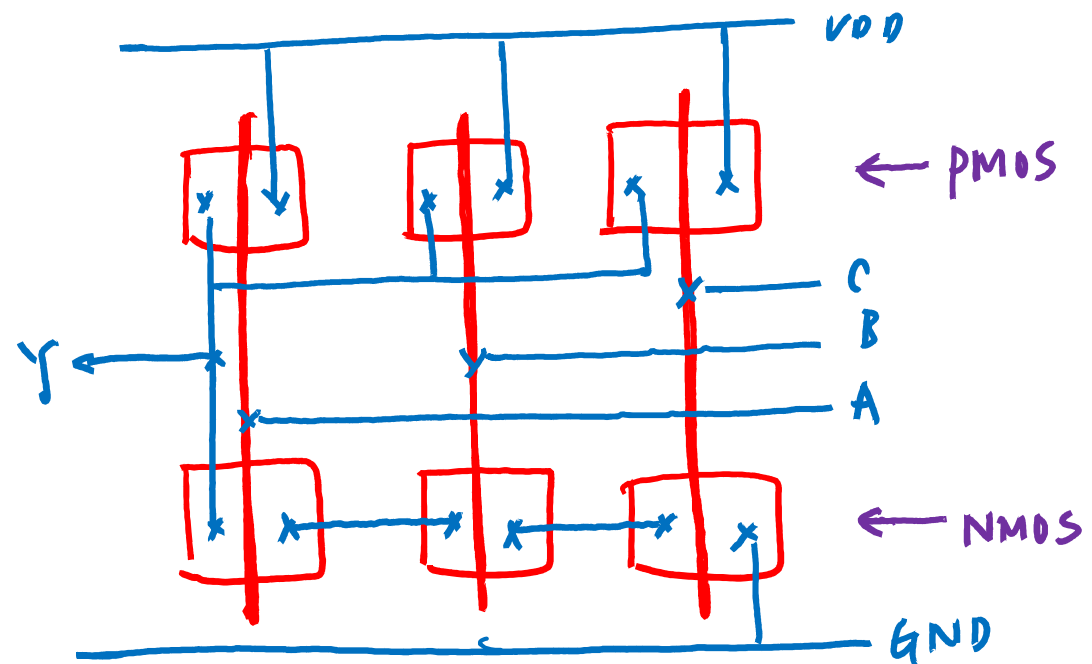
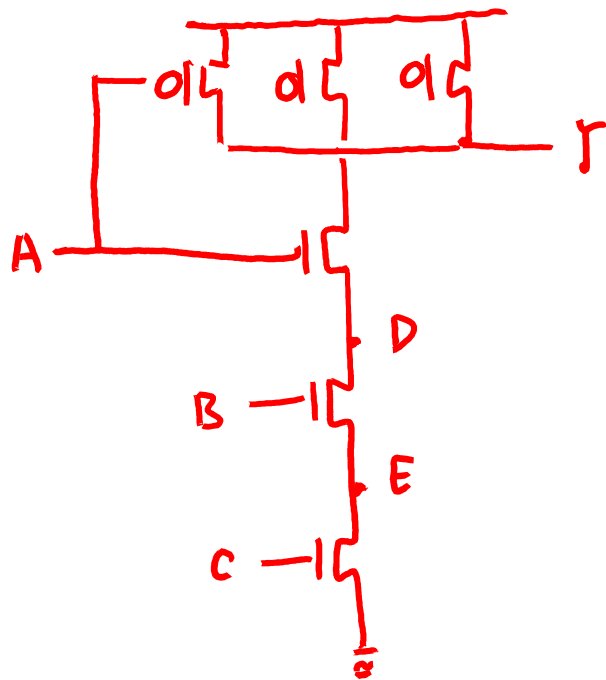
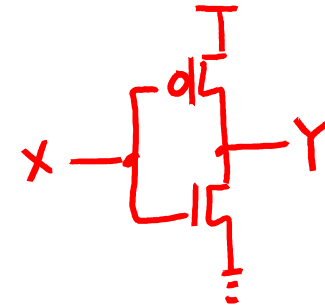
Example: NAND3

~~X → DO → Y~~

- 3-input NAND gate $Y = \overline{A \cdot B \cdot C}$

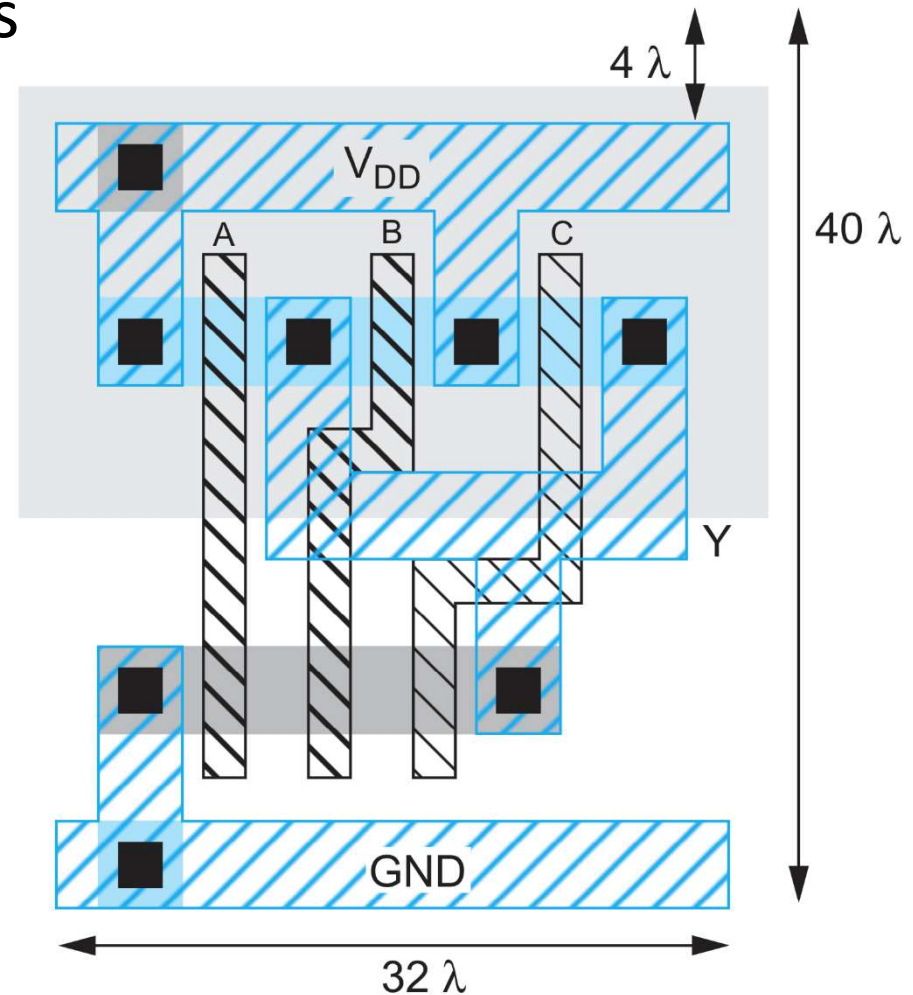


CMOS implementation



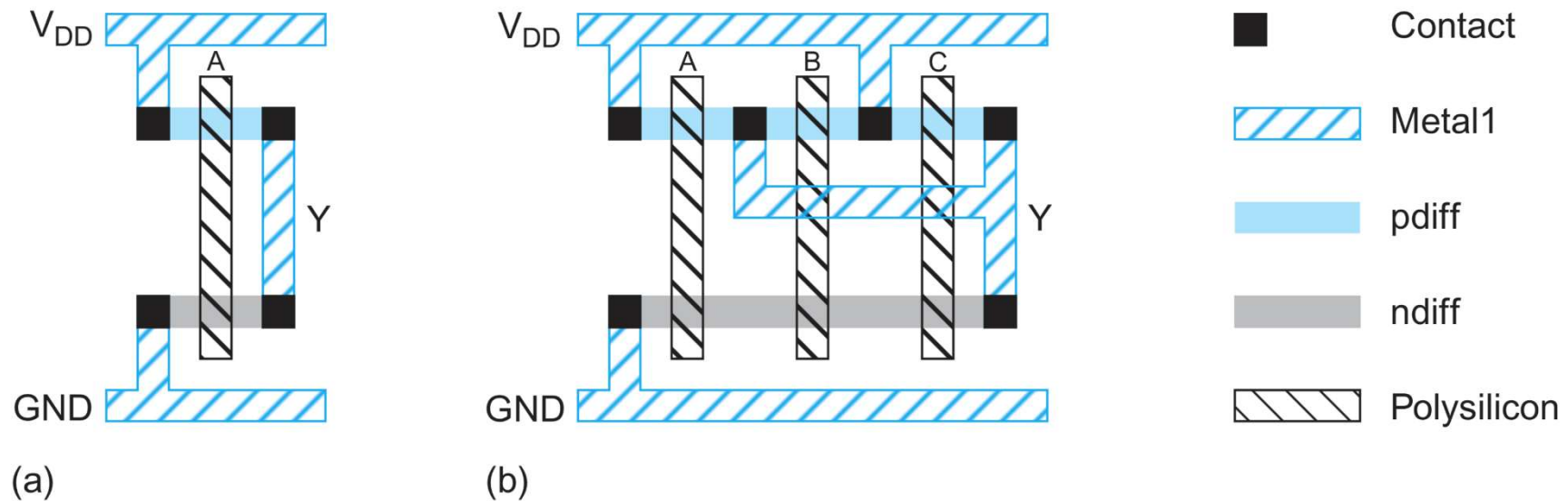
Example: NAND3

- Horizontal n-diffusion and p-diffusion stripes
- Vertical polysilicon gates
- M1 VDD rail at top
- M1 GND rail at bottom
- 32λ by 40λ

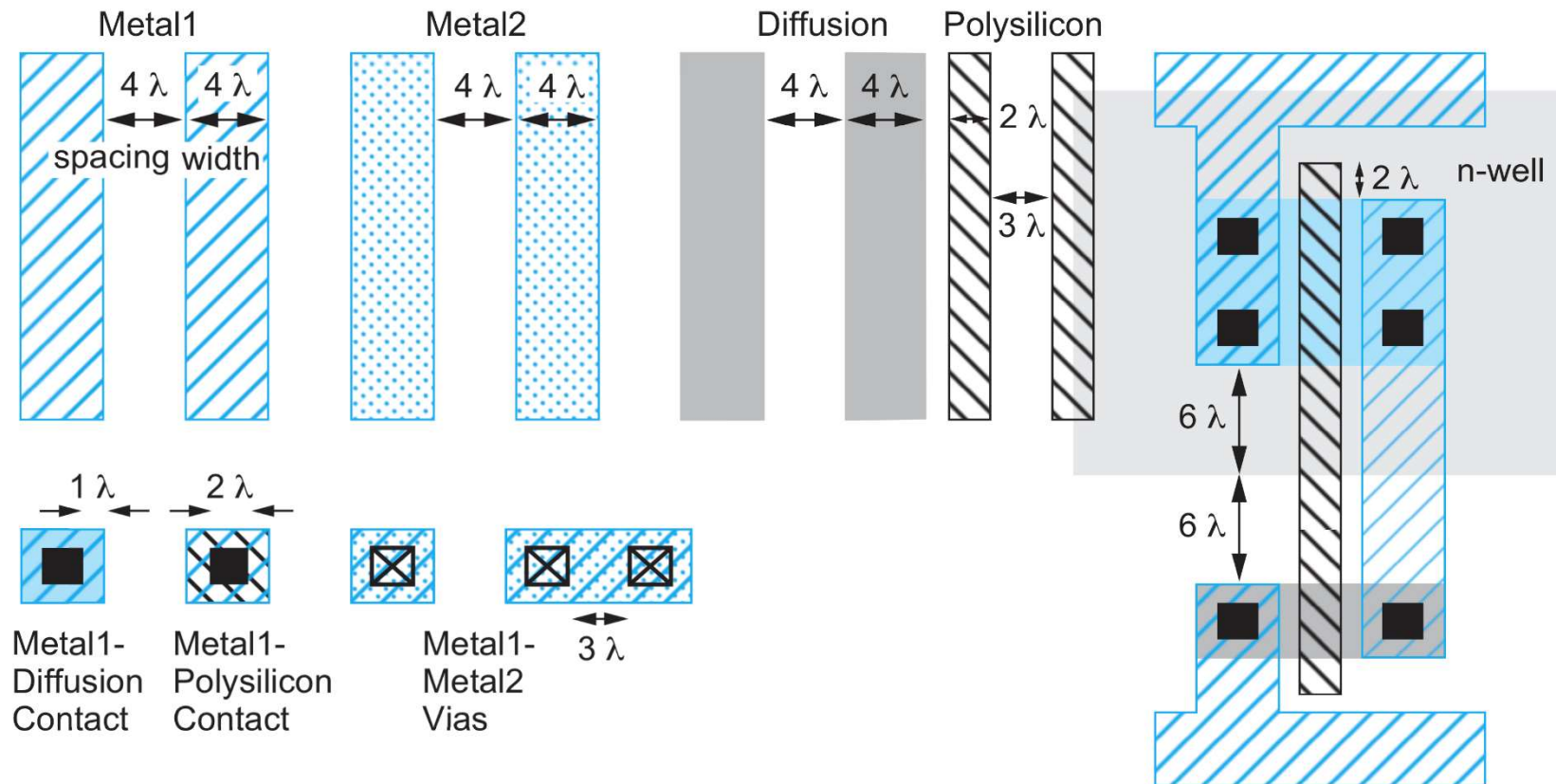


Stick Diagrams

- Help to plan layout quickly
 - Need not scale
 - Draw with color pencils or easy-to-erase markers



Simplified λ -Based Design Rules



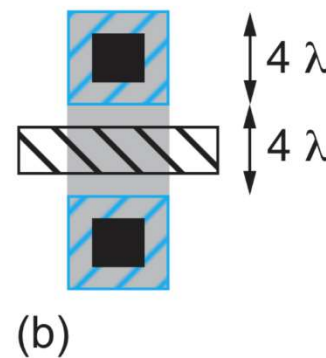
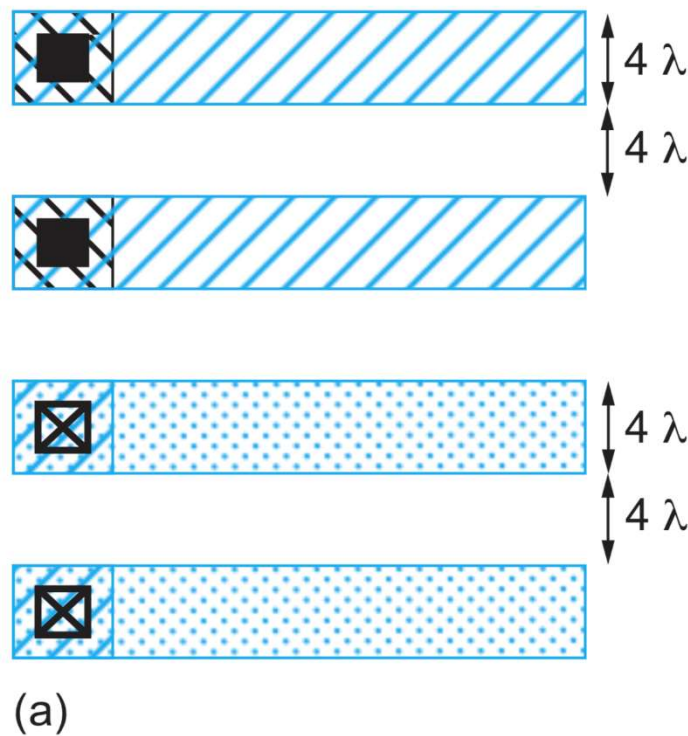
$180\text{nm} : \lambda = 90\text{nm}$

$90\text{nm} : \lambda = 45\text{nm}$

Wiring Tracks

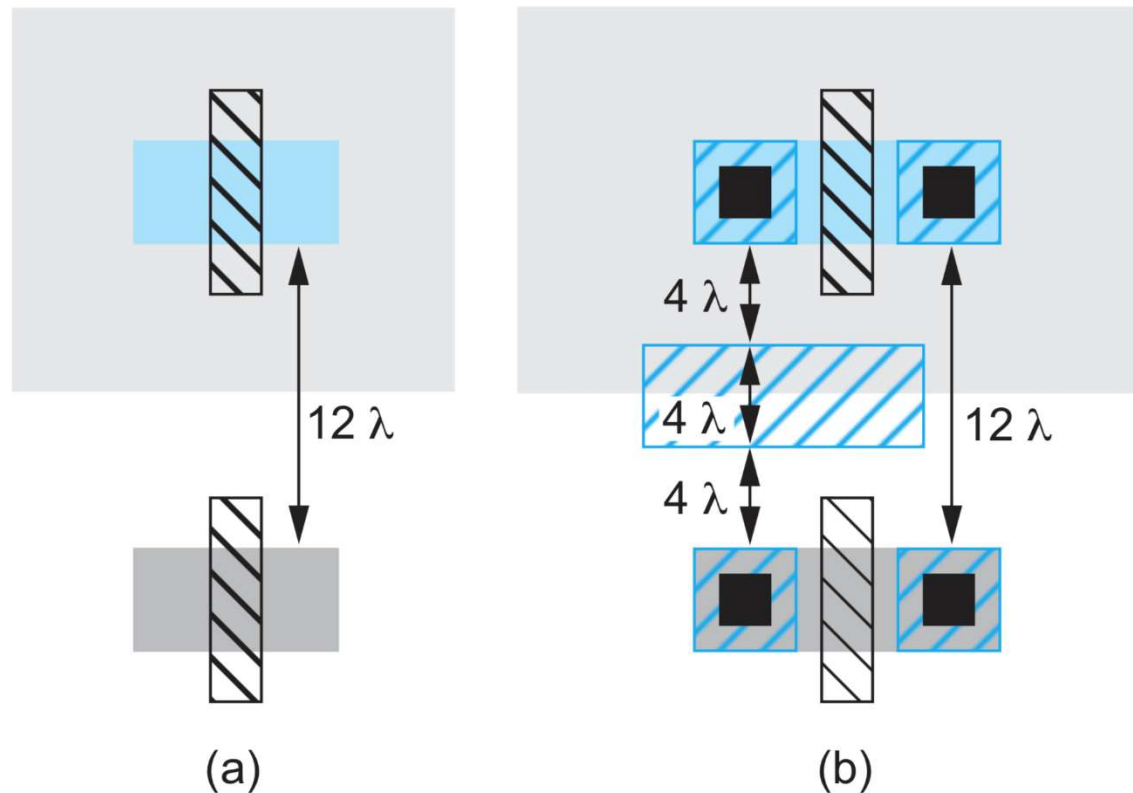
Layout dominated by wiring

- Space required by wires
 - 4λ for width and 4λ for spacing = 8λ pitch
- Transistors also consume one wiring track



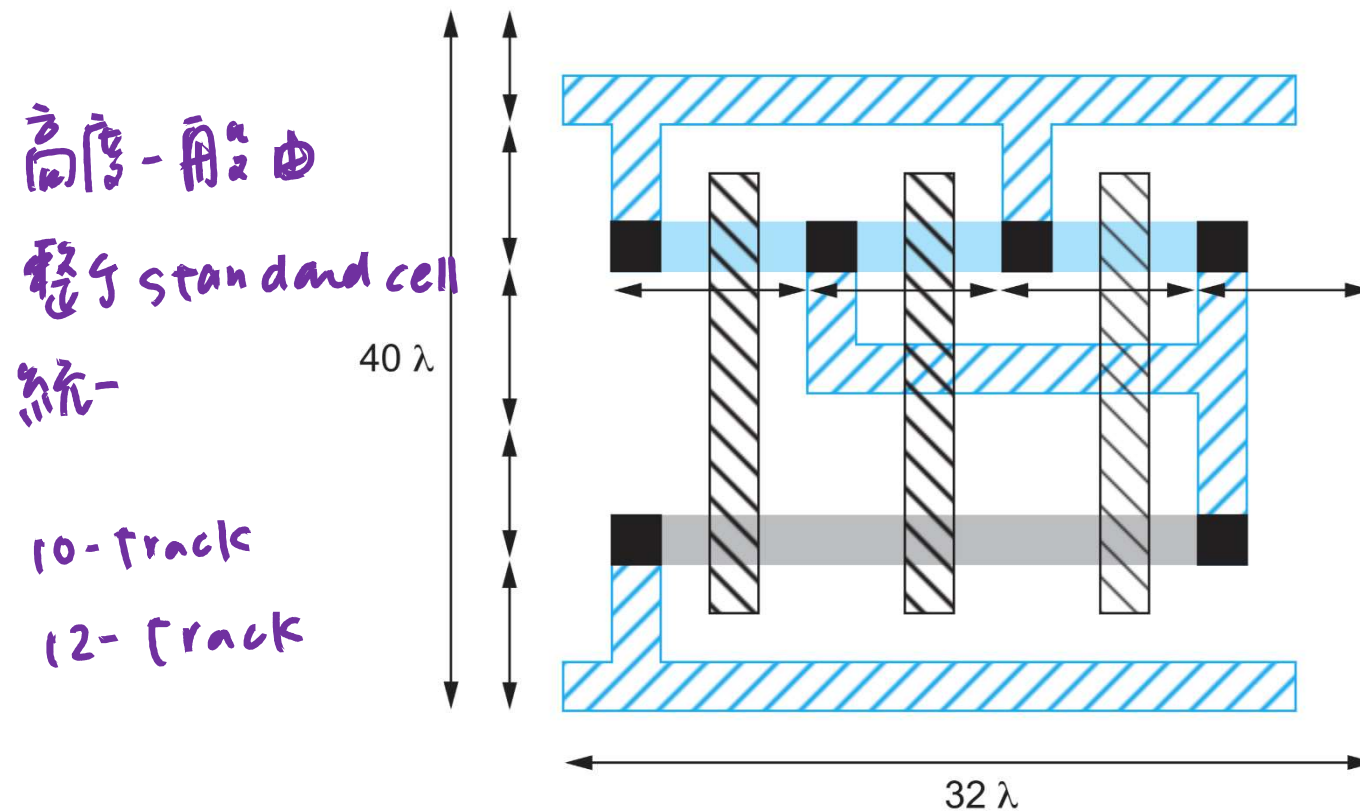
Well Spacing

- Wells must surround transistors by 6λ
 - Imply 12λ between opposite transistor flavors
 - Leave room for one wire track



Area Estimation

- Estimate area by counting wire tracks
 - Multiply by 8 to express in λ

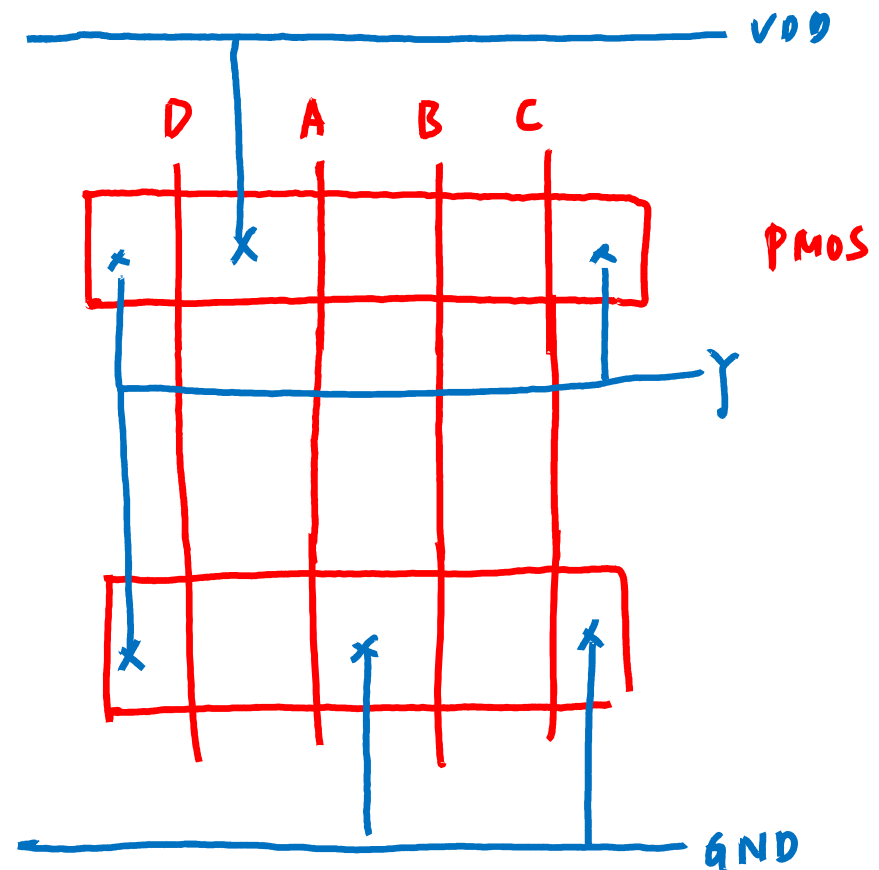
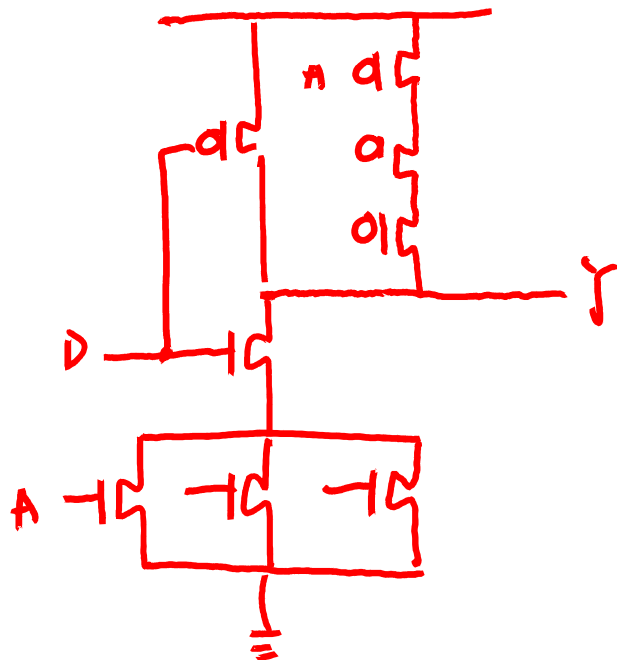


Example: O3AI (I) 3 input 先OR再AND再INV

- Sketch a stick diagram for O3AI and estimate area INV

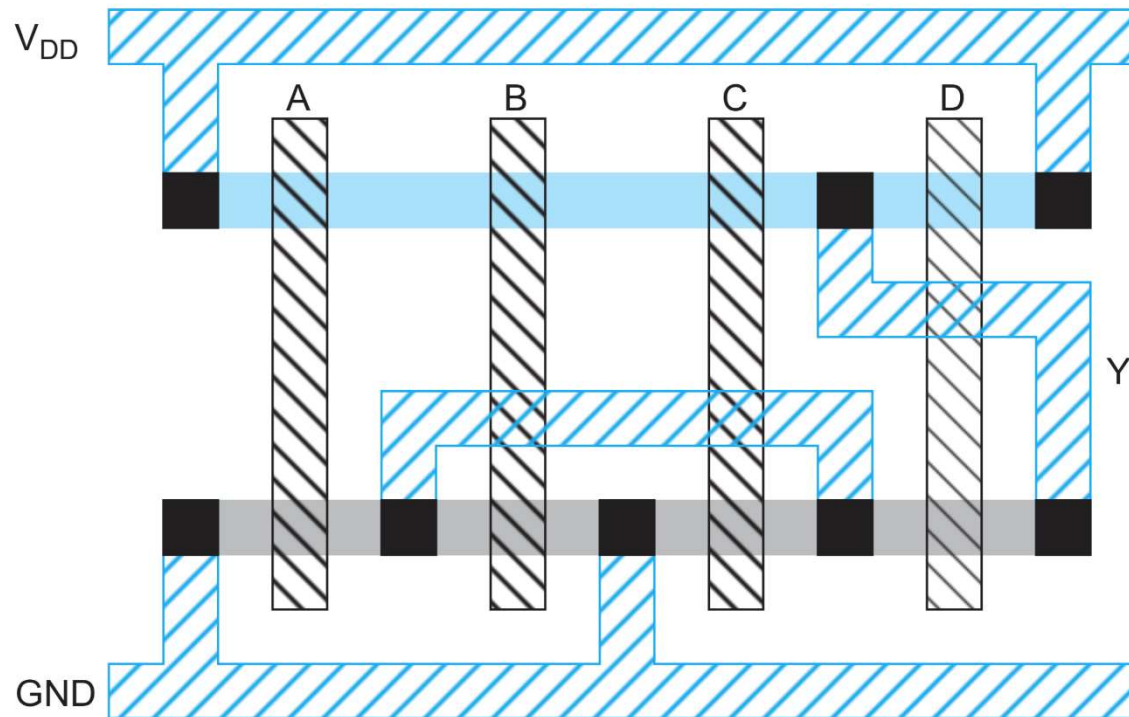
$$Y = \overline{(A + B + C) \cdot D}$$

CMOS implementation



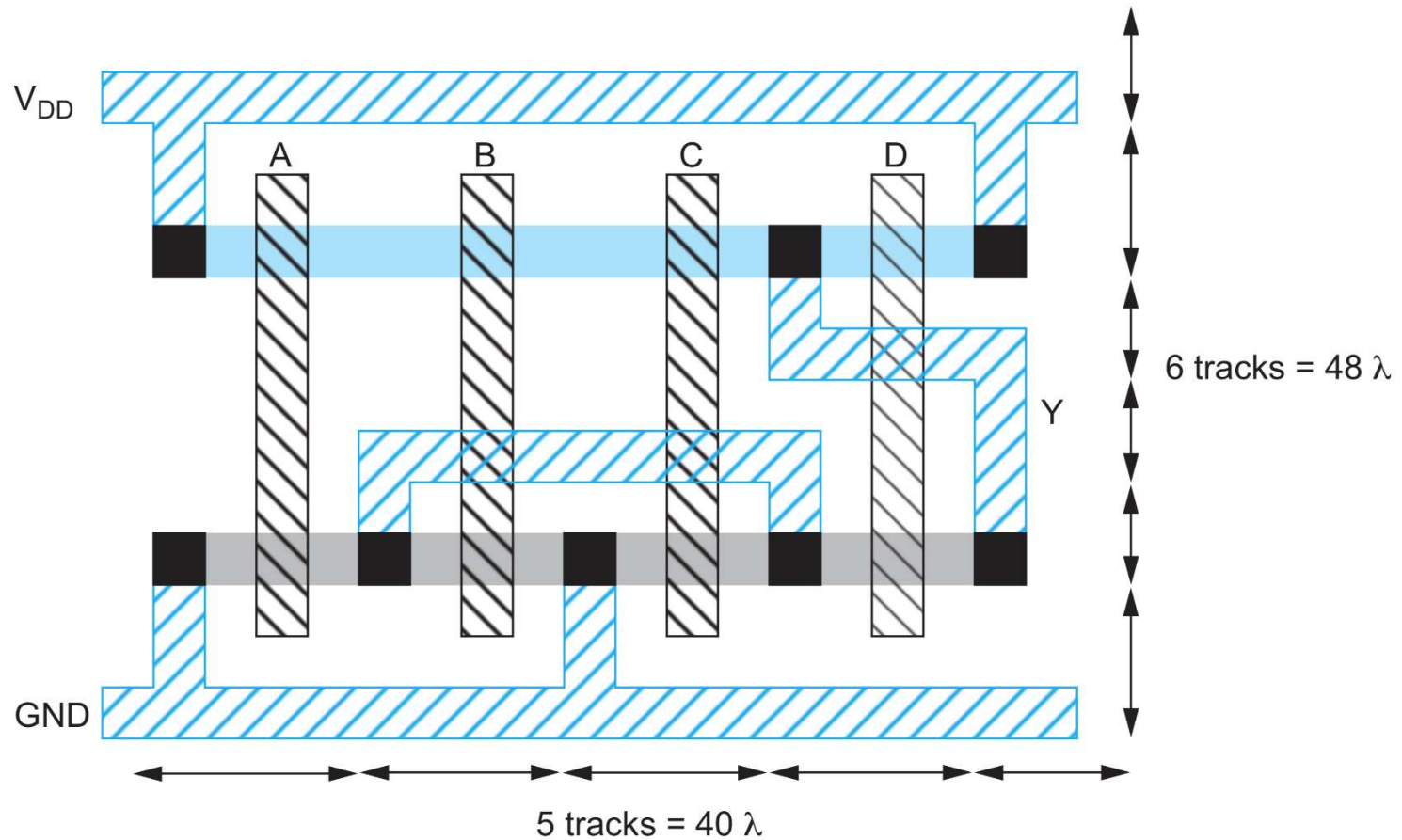
Example: O3AI (II)

- Sketch a stick diagram for O3AI and estimate area
 - $Y = \overline{(A + B + C)} \cdot D$



Example: O3AI (III)

- Sketch a stick diagram for O3AI and estimate area
 - $Y = \overline{(A + B + C) \cdot D}$



Outline

- CMOS Technology
- Layout Design Rules
- **CMOS Process Enhancements**
- Manufacturing Issues

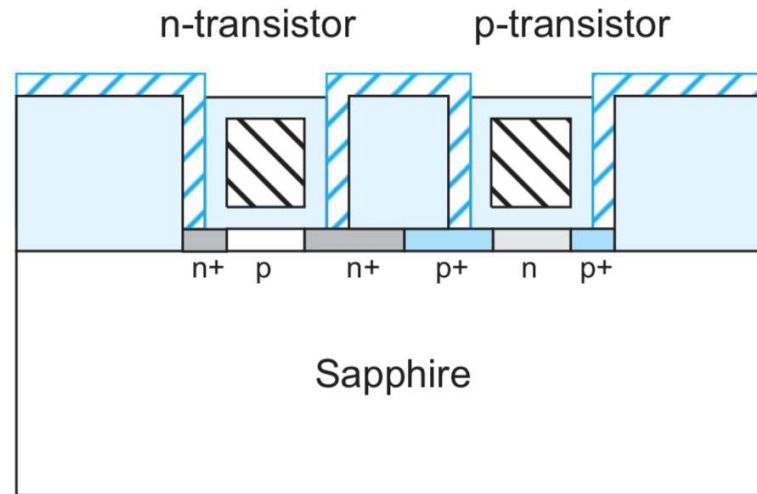
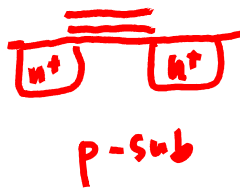
CMOS Process Enhancements

- Multiple threshold voltage and oxide thickness
 - Low core voltage for low power *core transistors*
 - High I/O voltage for interface compatibility *I/O transistors*
- Silicon on Insulator: higher speed
- High- k gate dielectric: thinner EOT
- Higher mobility: SiGe BJT, strained silicon
- Low-leakage transistor: finFET, gate-all-around (GAA)
- Plastic transistor: flexible electronic paper
- High-voltage transistor: LCD driver, power electronics
- Copper interconnect: high conductivity
- Low- k dielectric: low wire capacitance

Silicon on Insulator (SOI)

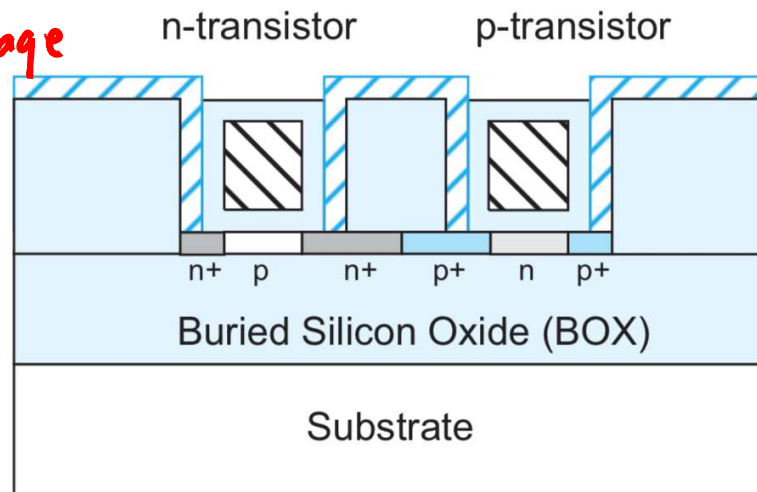
- Pros

- No capacitance between source/drain and body
→ higher speed
- No latch-up

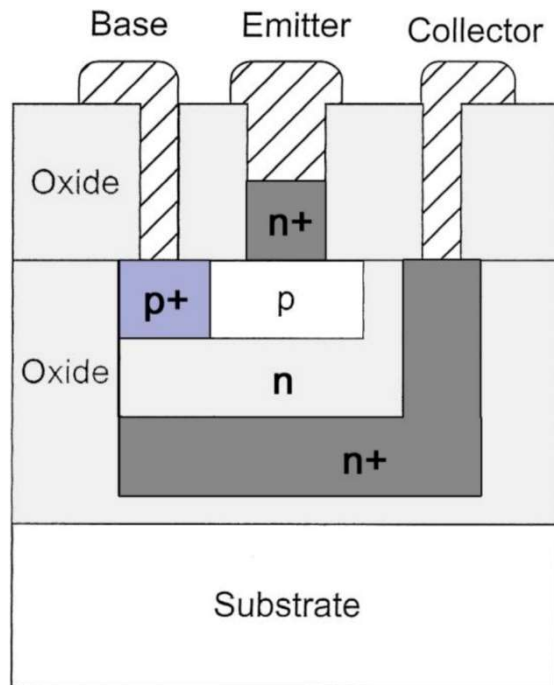


- Cons

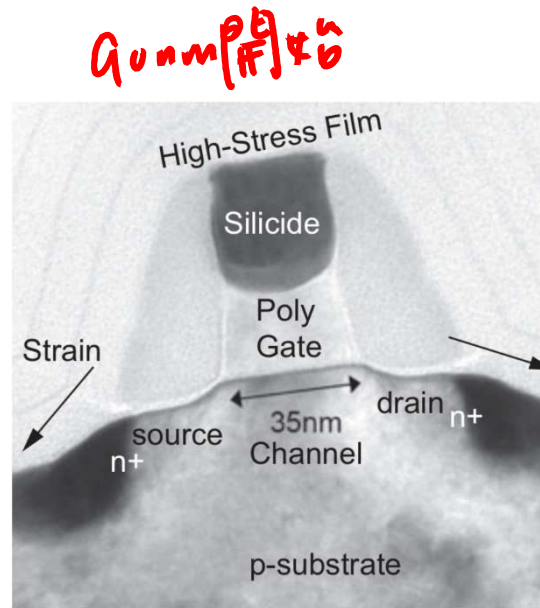
- Floating body *not well-defined body voltage*
→ history effect
- Self-heating effect
- Parasitic BJT
→ pass-gate leakage



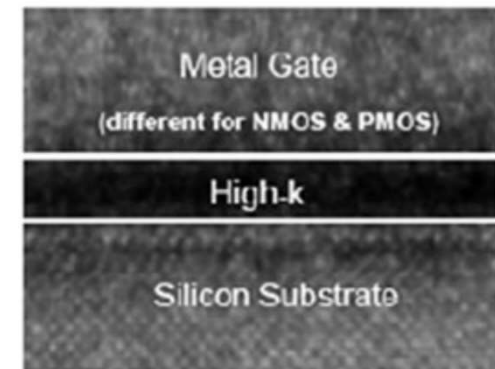
High- k and Higher Mobility



SiGe bipolar transistor



Strained Silicon

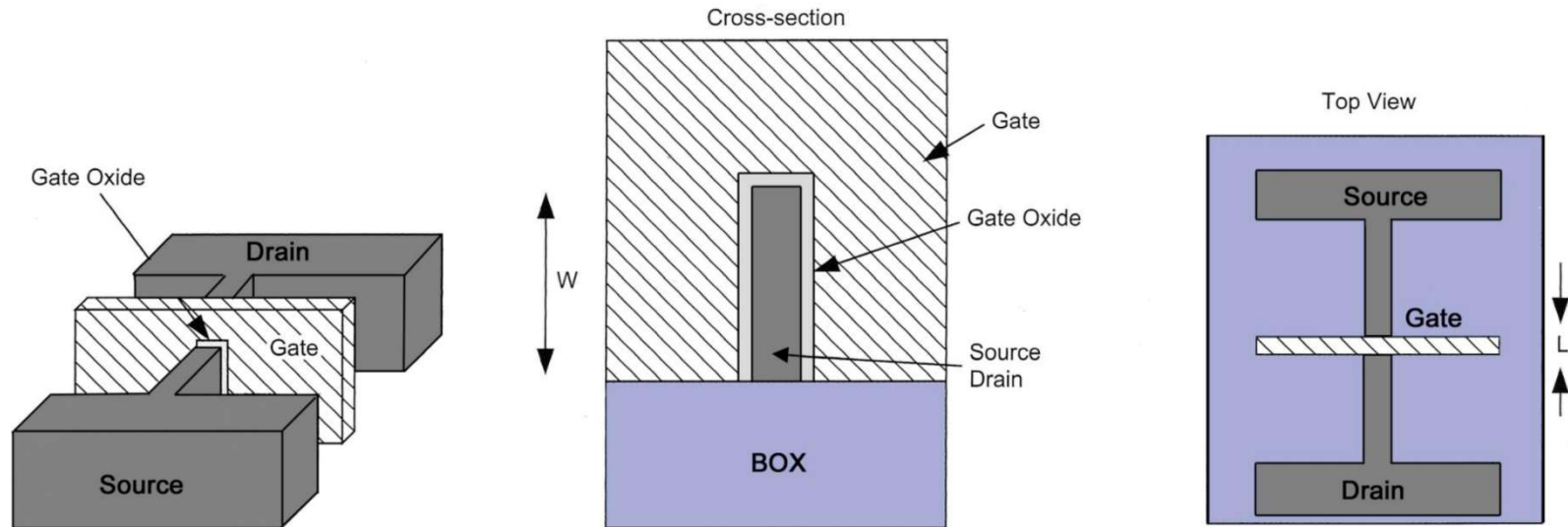


High- k + metal gate

Modern CMOS scaling is as much about material and structure innovation as dimensional scaling

Mark Bohr, "The new era of scaling in an SoC world," plenary session, ISSCC 2009

FinFET and GAA Structure



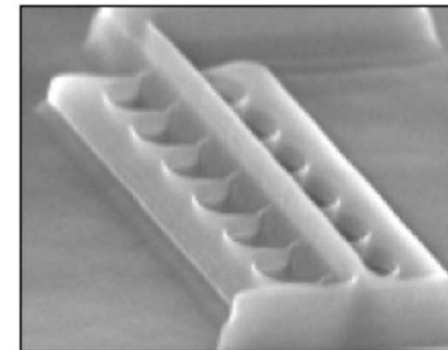
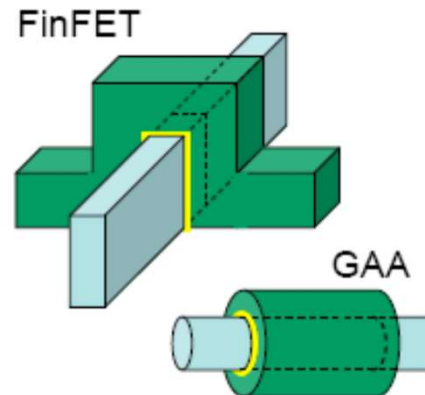
- Multi-gate FETs

- + Improved electrostatics

- ~~+ Steeper sub-threshold slope~~

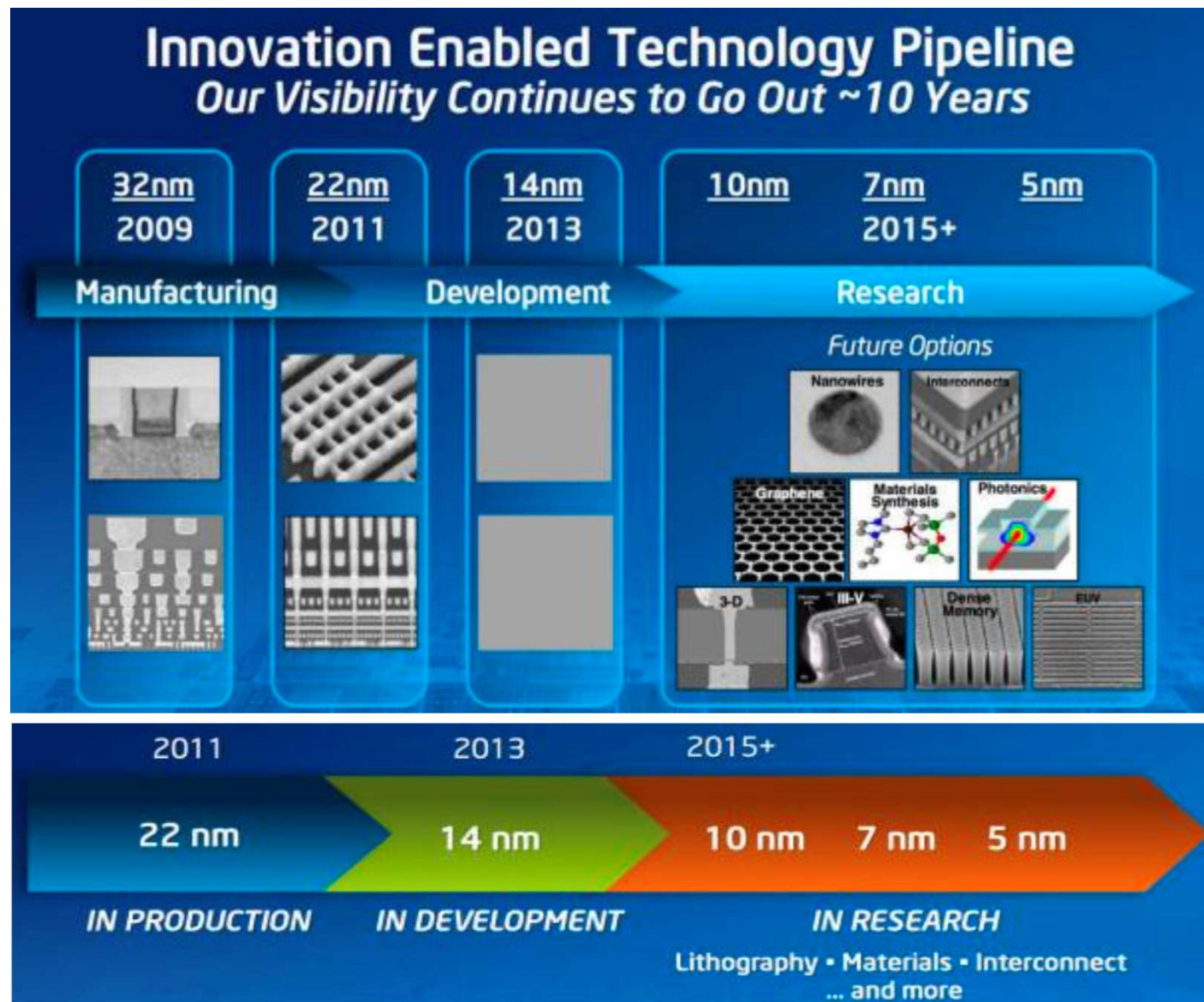
- ? Higher parasitic resistance

- ? Higher parasitic capacitance



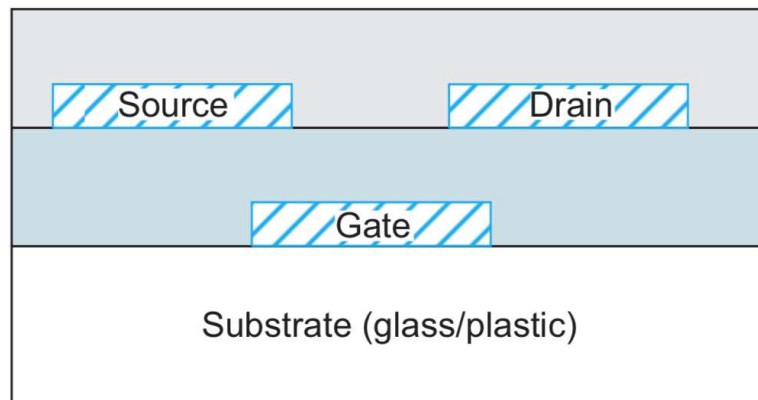
Mark Bohr, "The new era of scaling in an SoC world," plenary session, ISSCC 2009




Intel Technology Trend



Plastic Transistor

- Electronic paper



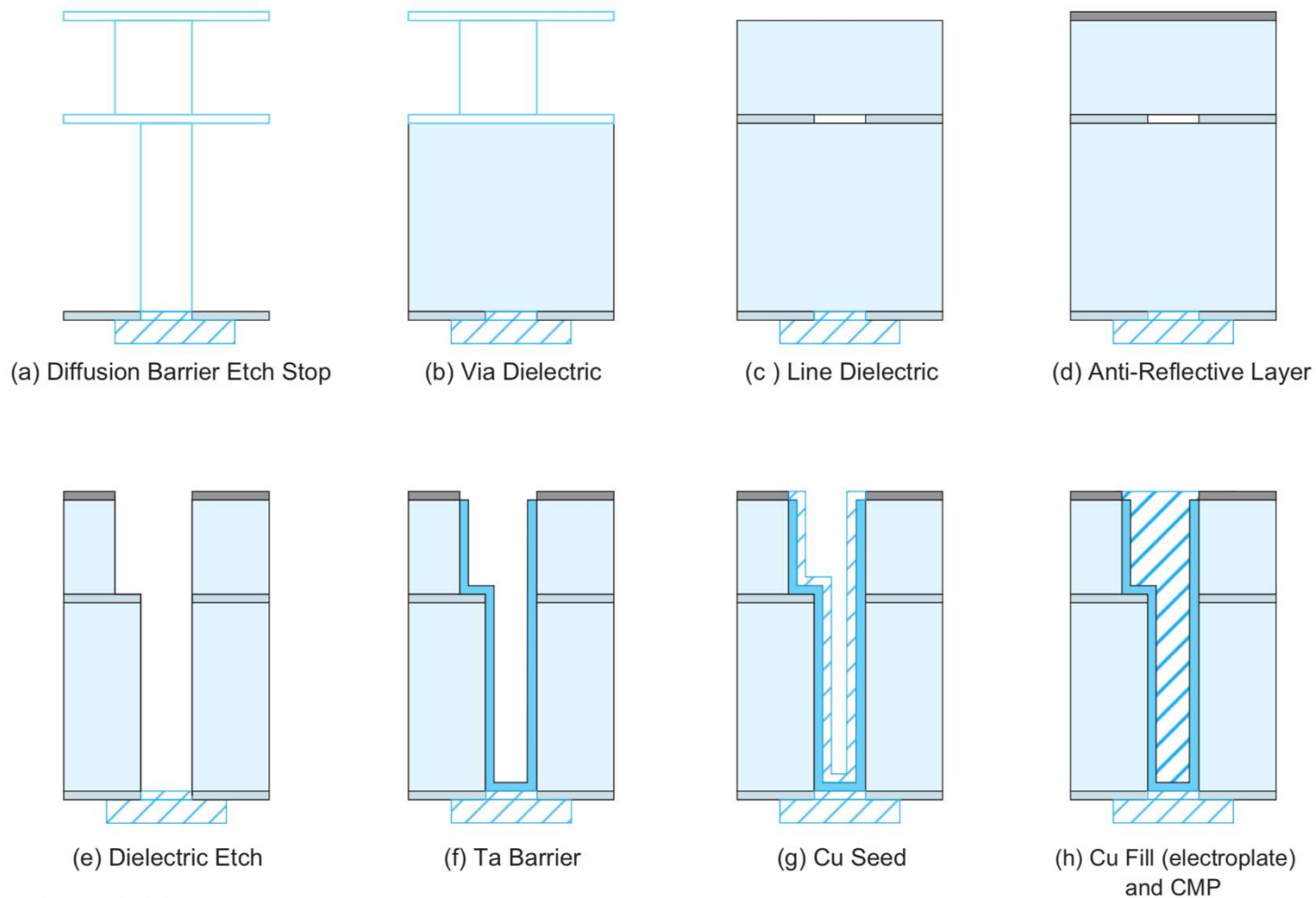
-  Semiconductor (Pentacene)
-  Gold Terminals
-  Insulator (Polymer Si/Nx)



Copper ^{Al}Interconnect

- Copper atoms diffuse into the silicon and dielectric, destroying transistors
 - Barrier layers are necessary
- The required process to etch copper wires is tricky
- Copper oxide forms readily and interferes with good contacts
- Care has to be taken not to introduce copper into the environment as pollutant

Copper Damascene Process

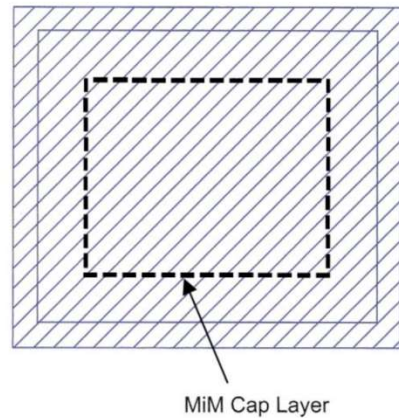
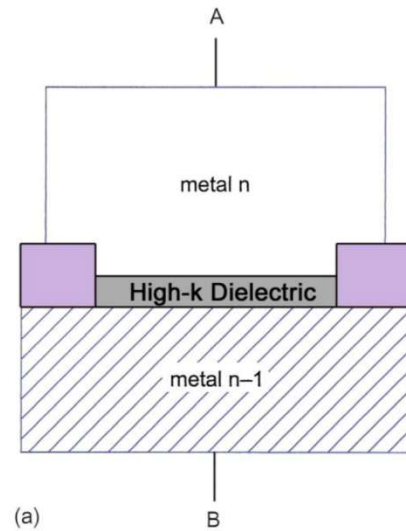


- Pros – high conductivity
- Cons – complex process

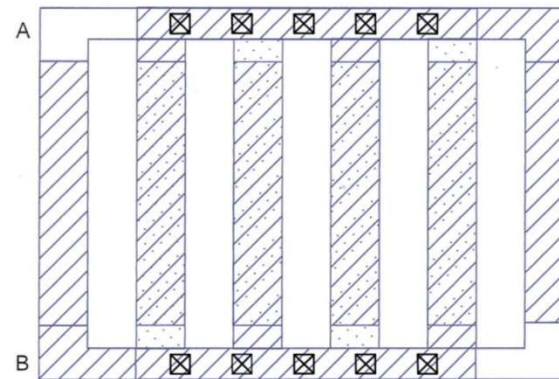
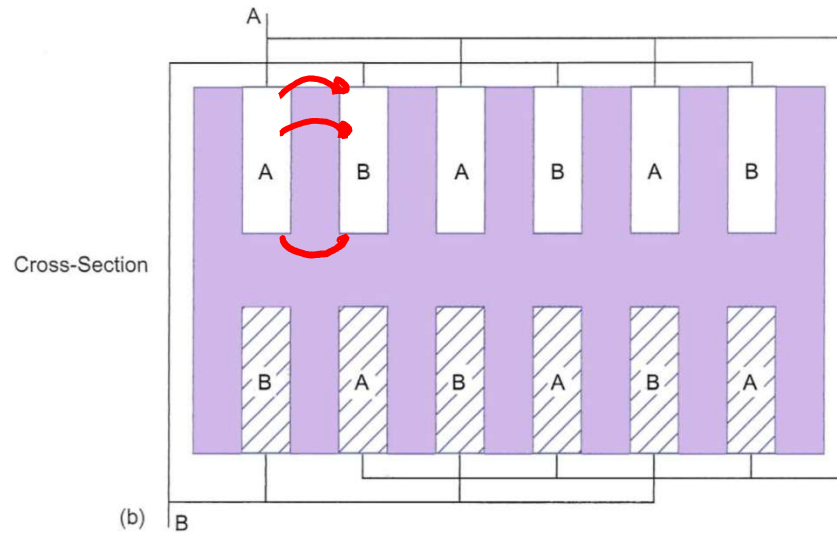
Capacitors

C · R · L

MIM Capacitor



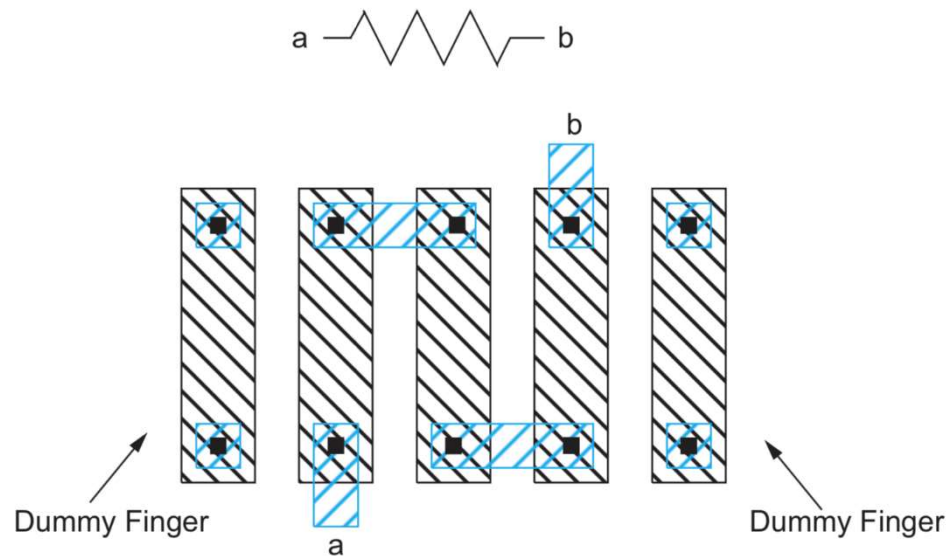
Fringe Capacitor



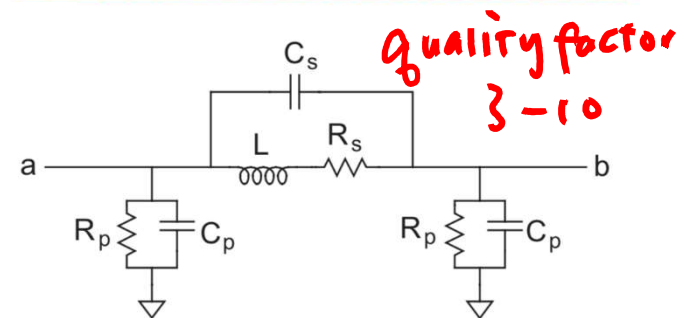
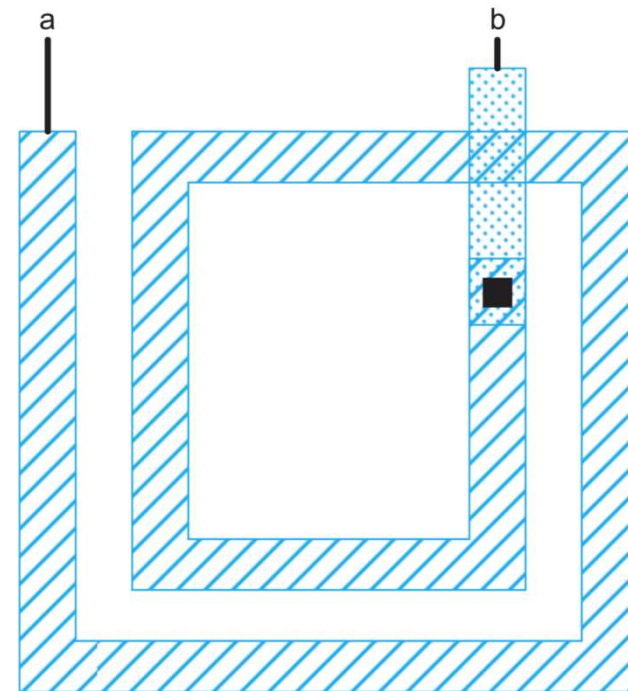
Resistor and Inductor

silicide block mask

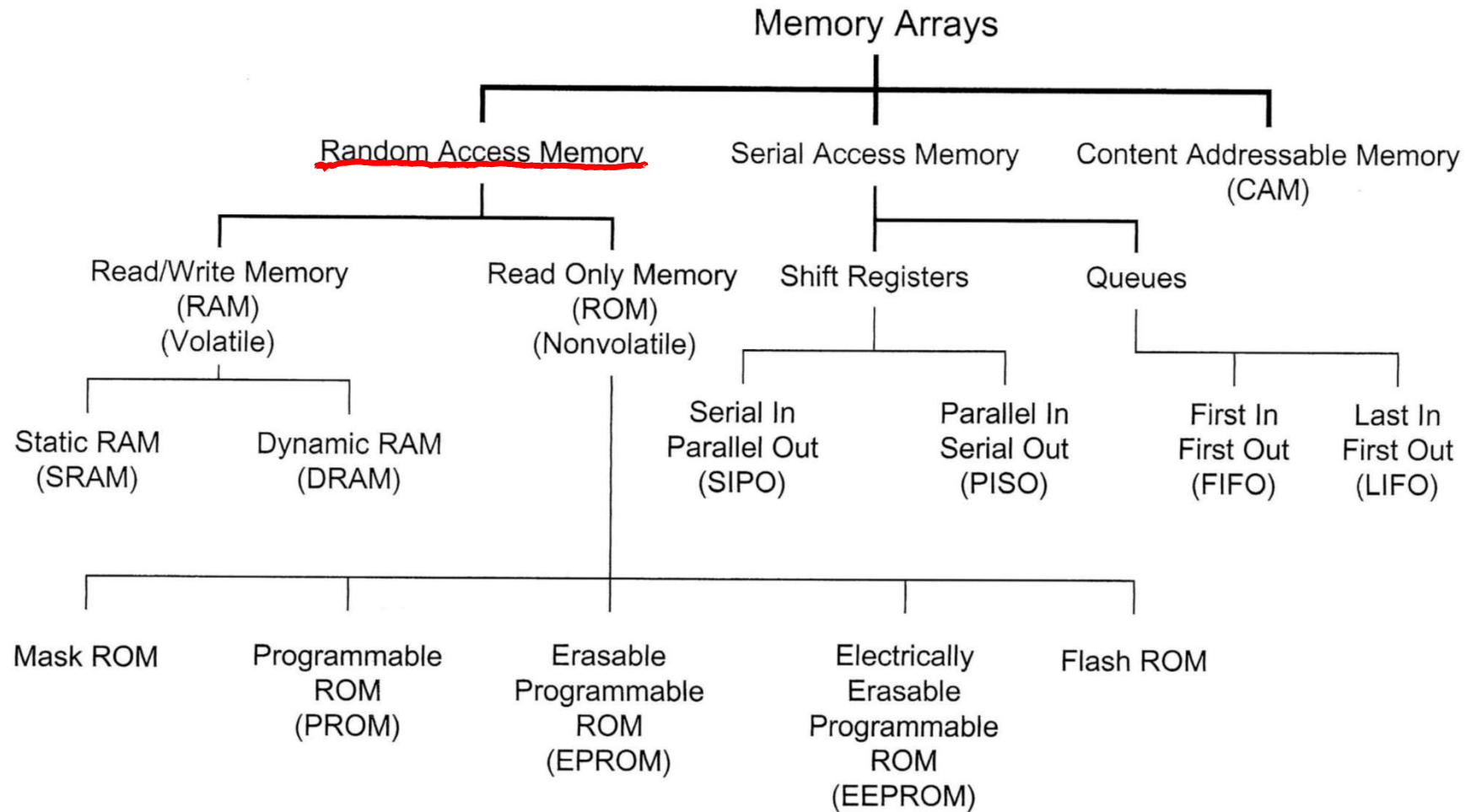
Non-silicide high-resistivity
poly resistor



Planar spiral inductor

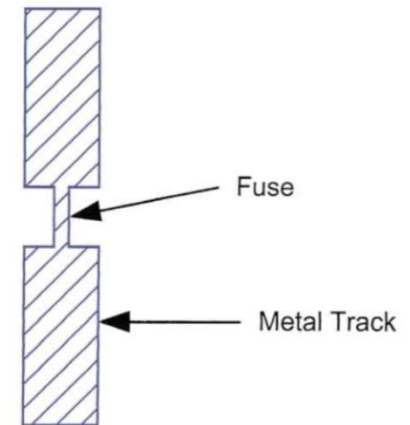


Memory Category

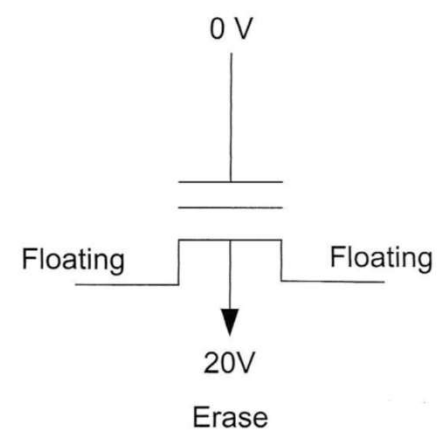
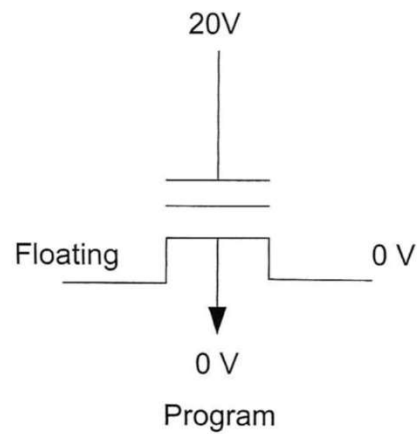
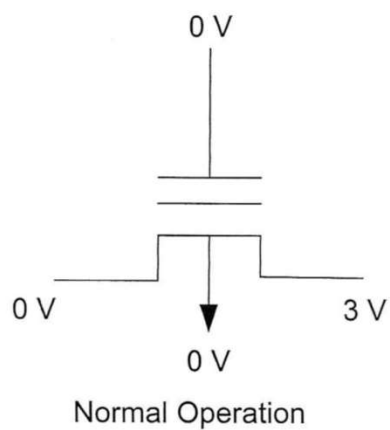
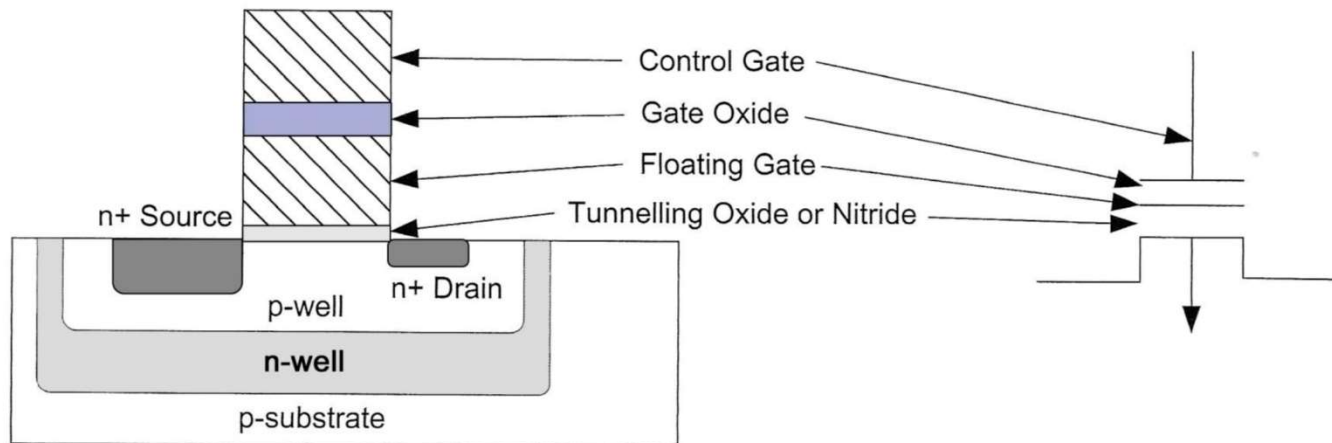


Non-Volatile Memory (NVM)

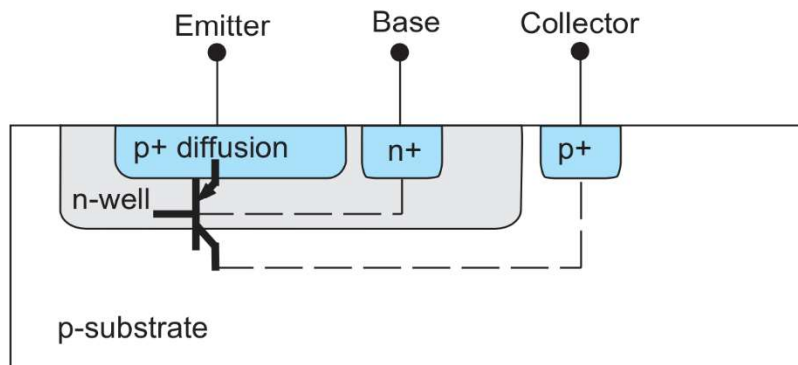
- Mask-programmed ROM (read-only memory)
 - Not programmable after manufacture
- One-time programmable (OTP) memory
 - Fuse structured programming flow
- EPROM: electrically programmable ROM
 - Electrical programming, UV erase
- EEPROM: electrically erasable PROM
 - Electrical programmable & erase, byte-level programming
- Flash
 - Block-level programming, faster and cheaper than EEPROM



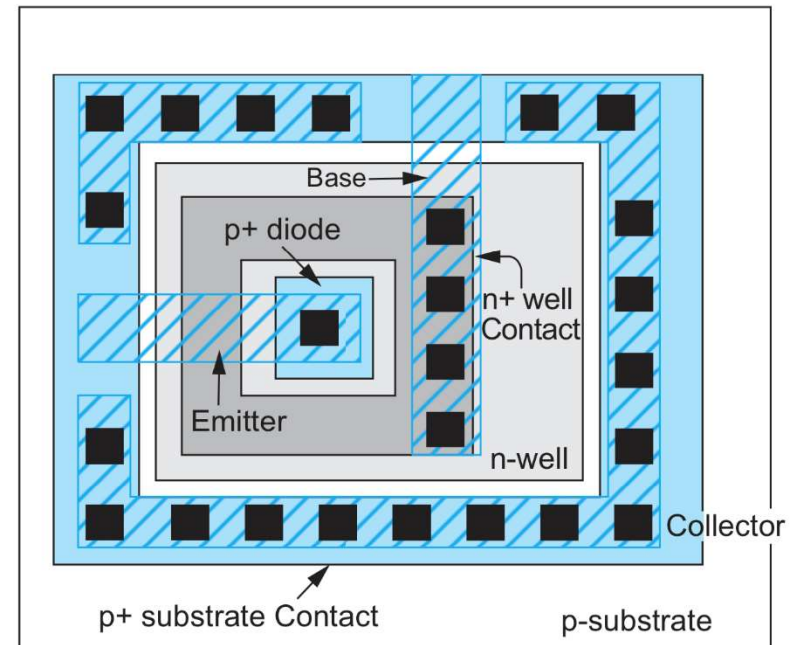
Flash Memory



BJT in CMOS Process



Cross-Section



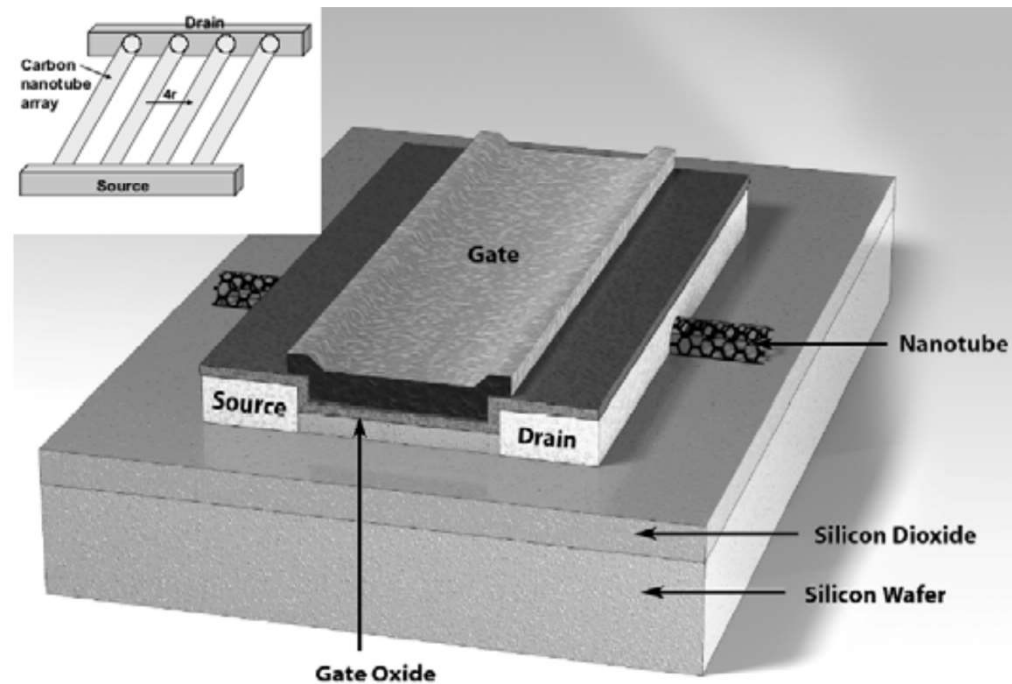
Representative Layout

- Used in bandgap voltage reference

带隙电压

Carbon Nanotube (CNT) Transistor

- Better electrical performance than Si but complex process
- Smaller channel length
- Higher speed
- Lower power

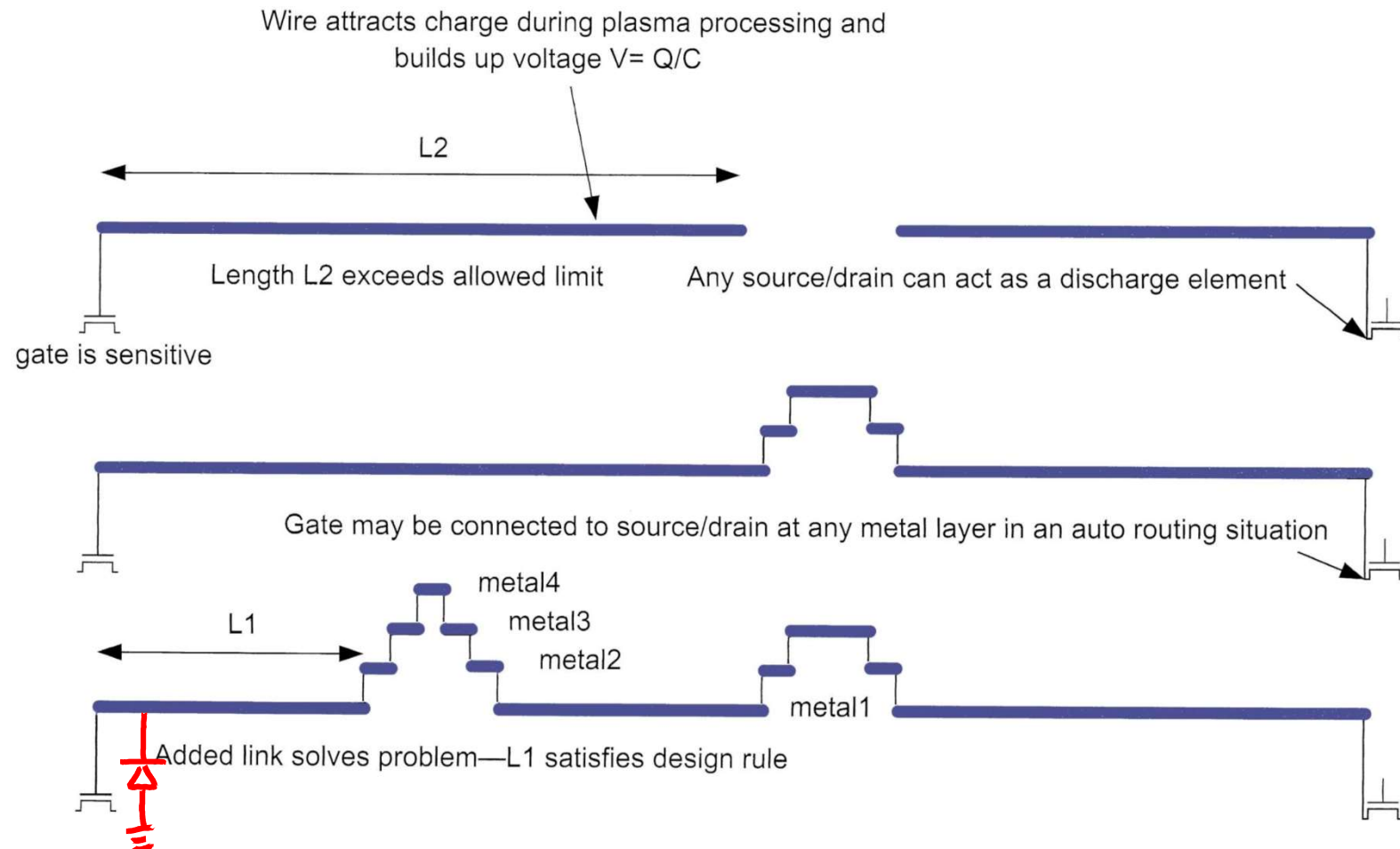


Outline

- CMOS Technology
- Layout Design Rules
- CMOS Process Enhancements
- **Manufacturing Issues**

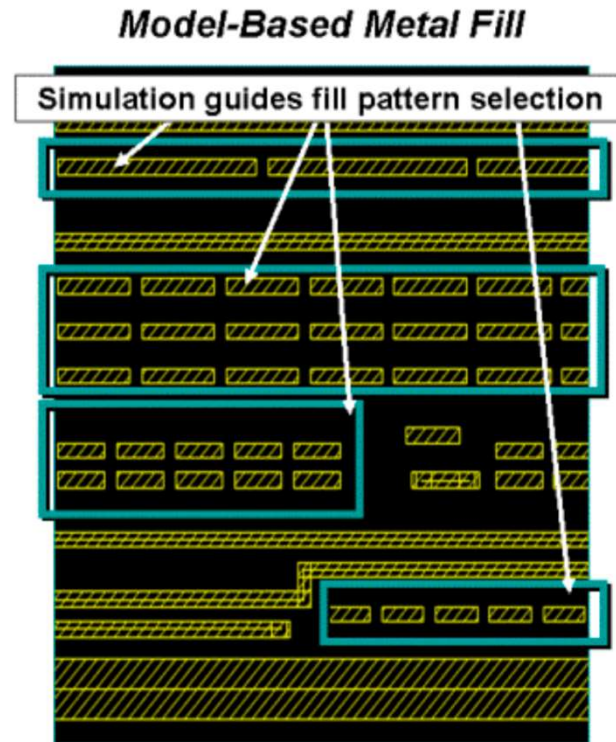
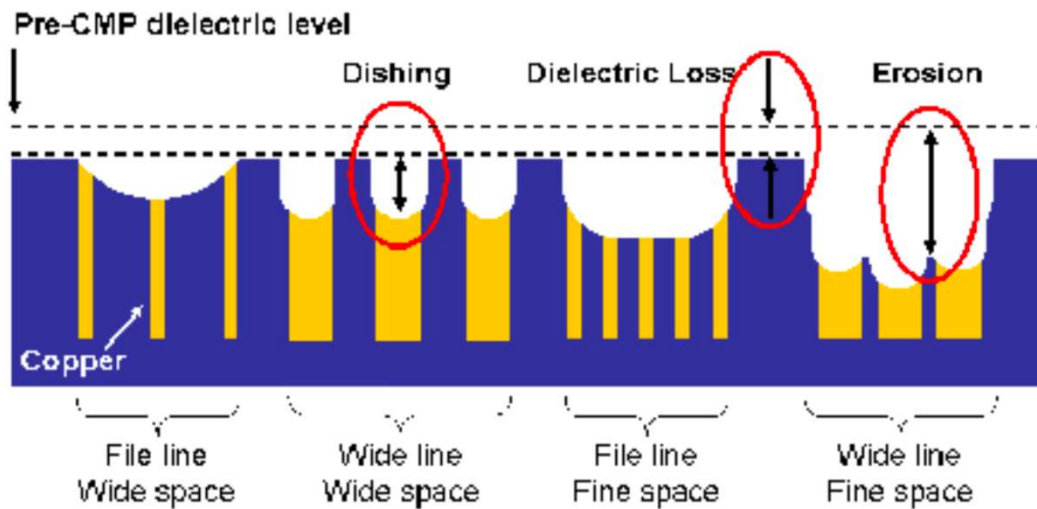
Antenna Rules

- Maximum area of metal connected to gates without discharging element



Density Rules 30% - 70%

- CMP and uniform etching process requirement
 - Planarization



- Solution: pattern fill (by CAD) floating metal

ref: https://www.eetimes.com/document.asp?doc_id=1276065