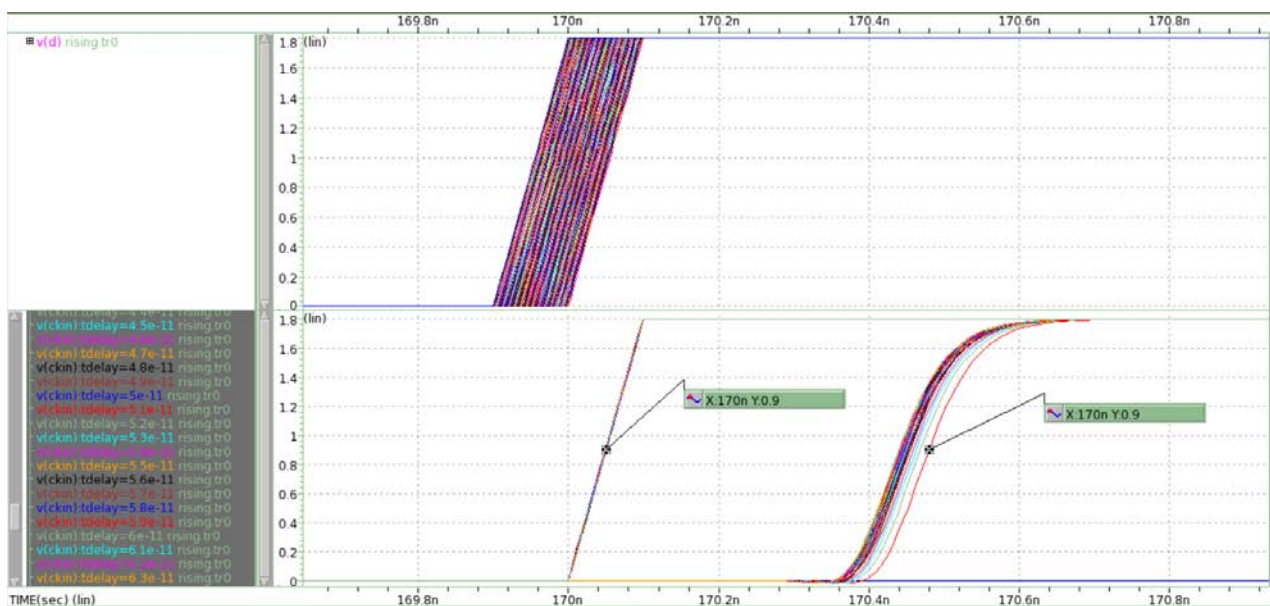
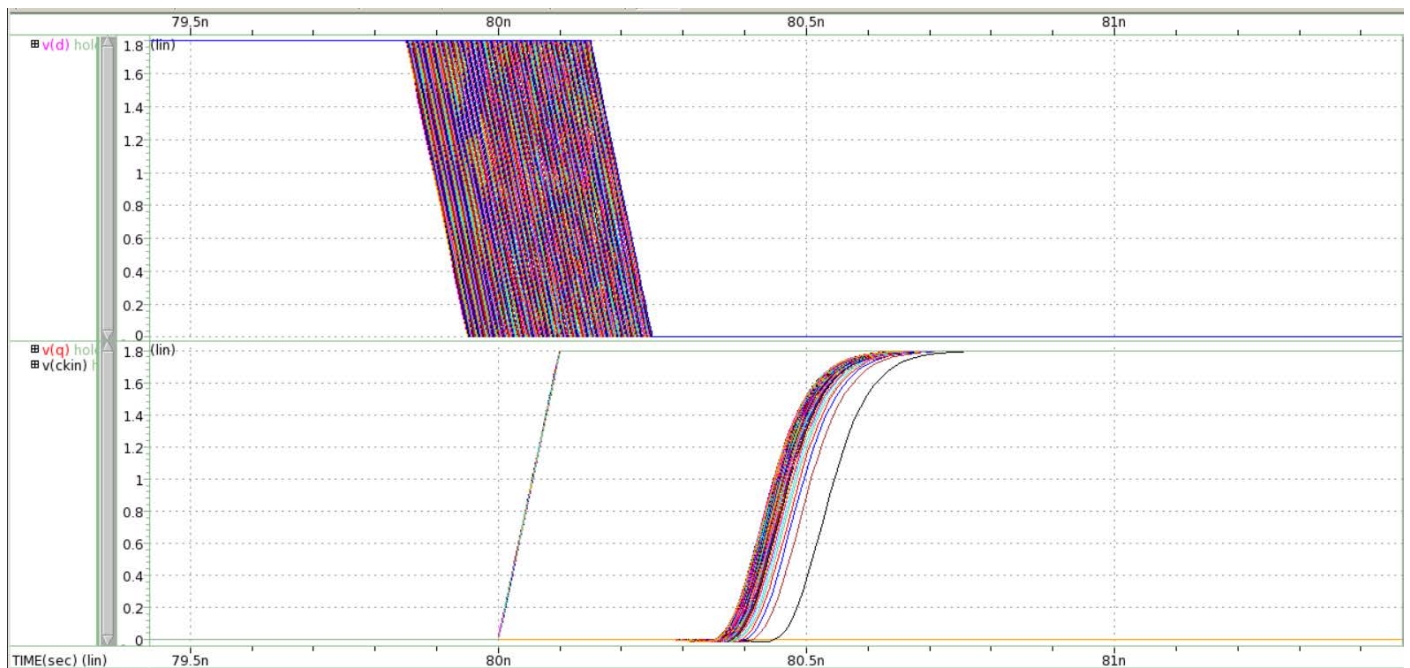
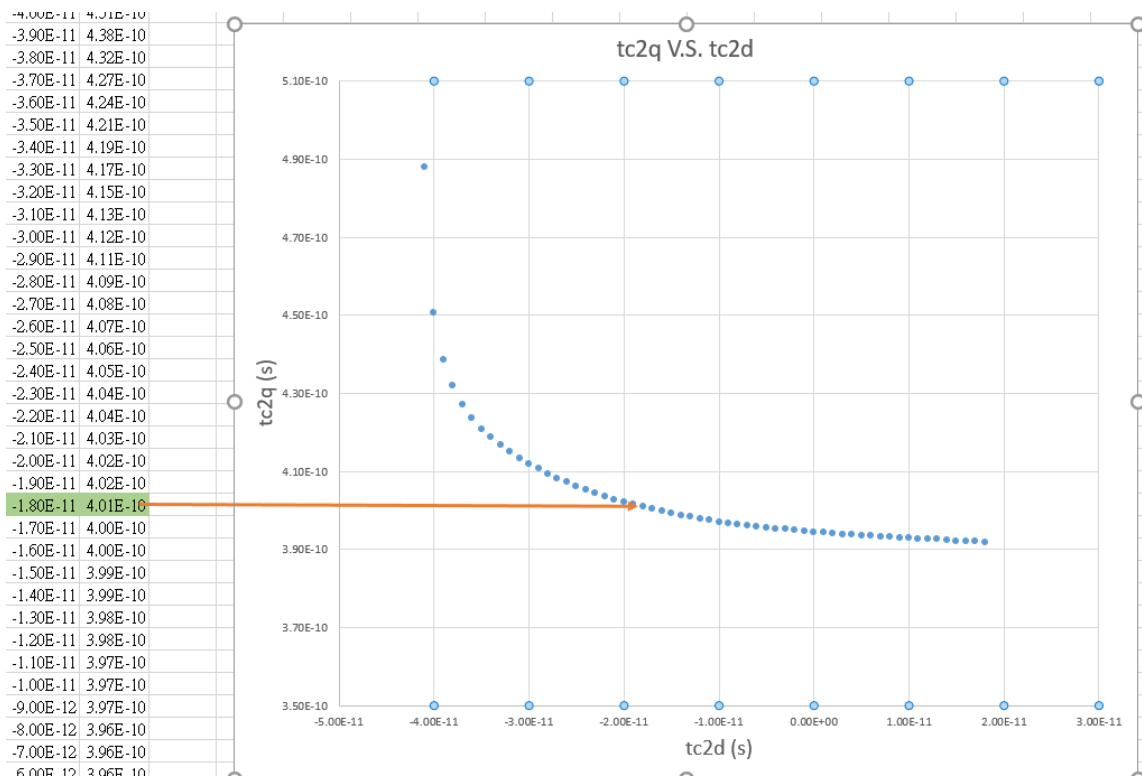


1.

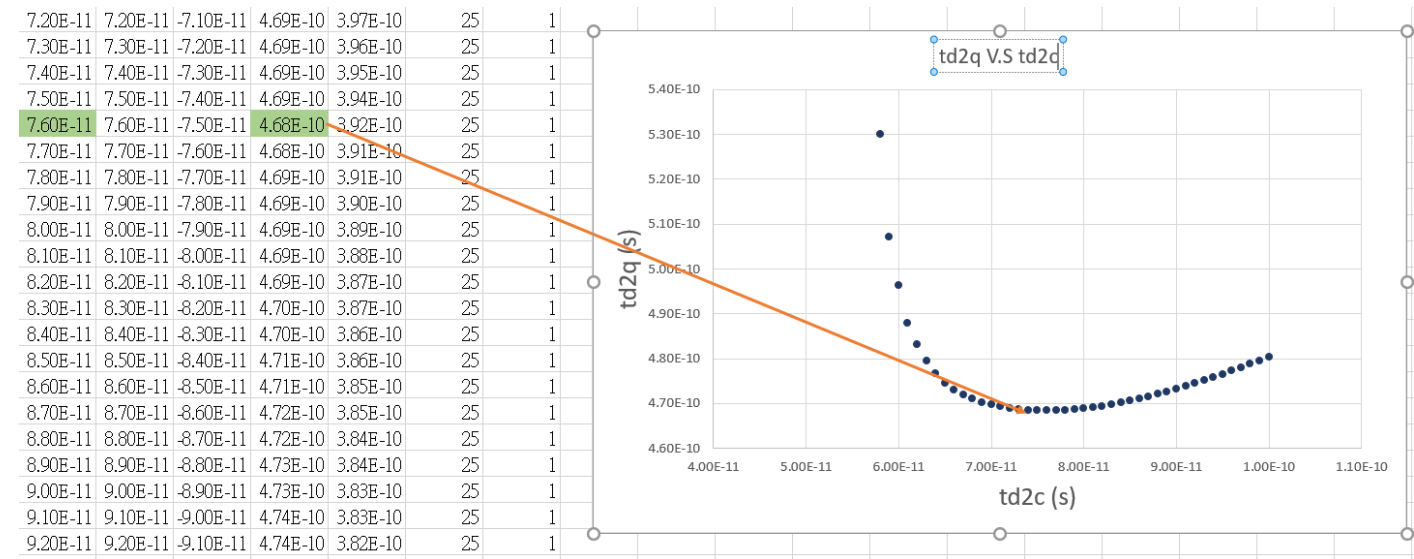
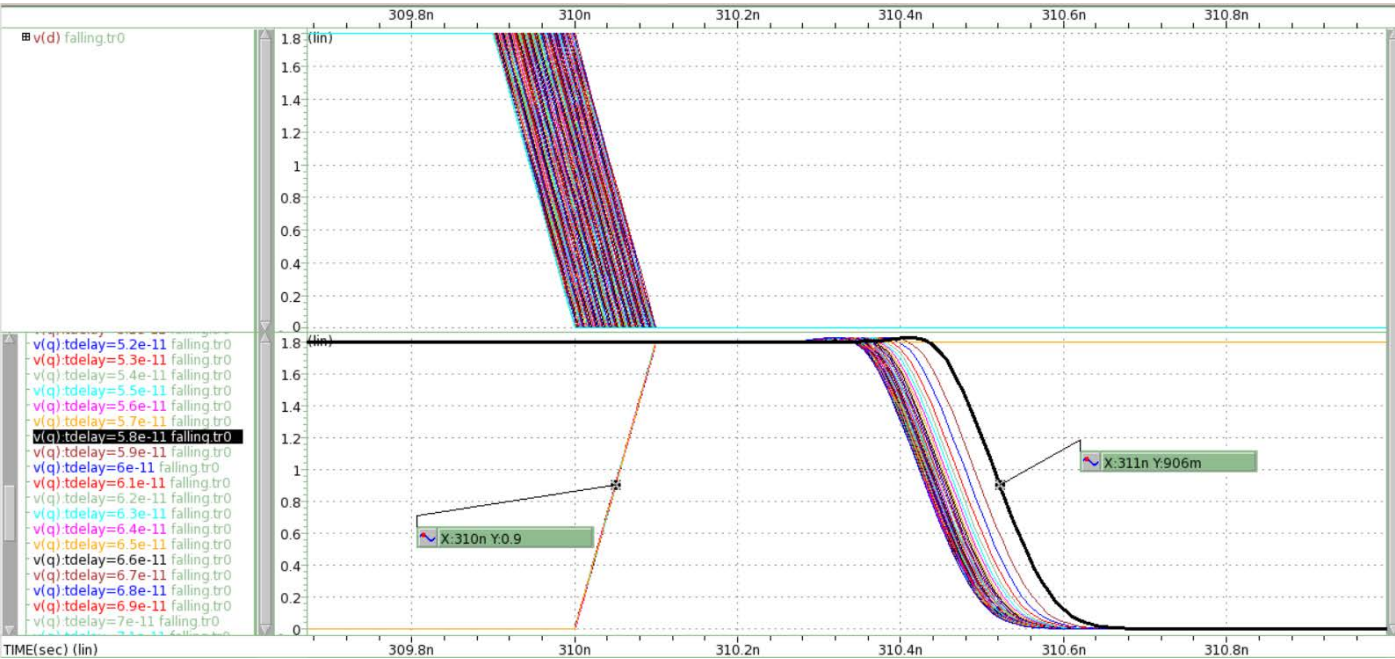


| 5.10E-11 | 5.10E-11 | ##### | 2.04E-08 | 2.04E-08 | 25 | 1 |
|----------|----------|-------|----------|----------|----|---|
| 5.20E-11 | 5.20E-11 | ##### | 2.04E-08 | 2.04E-08 | 25 | 1 |
| 5.30E-11 | 5.30E-11 | ##### | 2.04E-08 | 2.04E-08 | 25 | 1 |
| 5.40E-11 | 5.40E-11 | ##### | 2.04E-08 | 2.04E-08 | 25 | 1 |
| 5.50E-11 | 5.50E-11 | ##### | 2.04E-08 | 2.04E-08 | 25 | 1 |
| 5.60E-11 | 5.60E-11 | ##### | 4.89E-10 | 4.32E-10 | 25 | 1 |
| 5.70E-11 | 5.70E-11 | ##### | 4.75E-10 | 4.18E-10 | 25 | 1 |
| 5.80E-11 | 5.80E-11 | ##### | 4.71E-10 | 4.13E-10 | 25 | 1 |
| 5.90E-11 | 5.90E-11 | ##### | 4.68E-10 | 4.09E-10 | 25 | 1 |
| 6.00E-11 | 6.00E-11 | ##### | 4.66E-10 | 4.06E-10 | 25 | 1 |
| 6.10E-11 | 6.10E-11 | ##### | 4.65E-10 | 4.04E-10 | 25 | 1 |
| 6.20E-11 | 6.20E-11 | ##### | 4.65E-10 | 4.03E-10 | 25 | 1 |
| 6.30E-11 | 6.30E-11 | ##### | 4.65E-10 | 4.02E-10 | 25 | 1 |
| 6.40E-11 | 6.40E-11 | ##### | 4.65E-10 | 4.00E-10 | 25 | 1 |
| 6.50E-11 | 6.50E-11 | ##### | 4.65E-10 | 4.00E-10 | 25 | 1 |
| 6.60E-11 | 6.60E-11 | ##### | 4.65E-10 | 3.99E-10 | 25 | 1 |
| 6.70E-11 | 6.70E-11 | ##### | 4.65E-10 | 3.98E-10 | 25 | 1 |
| 6.80E-11 | 6.80E-11 | ##### | 4.66E-10 | 3.98E-10 | 25 | 1 |
| 6.90E-11 | 6.90E-11 | ##### | 4.66E-10 | 3.97E-10 | 25 | 1 |
| 7.00E-11 | 7.00E-11 | ##### | 4.67E-10 | 3.97E-10 | 25 | 1 |
| 7.10E-11 | 7.10E-11 | ##### | 4.67E-10 | 3.96E-10 | 25 | 1 |
| 7.20E-11 | 7.20E-11 | ##### | 4.68E-10 | 3.96E-10 | 25 | 1 |
| 7.30E-11 | 7.30E-11 | ##### | 4.68E-10 | 3.95E-10 | 25 | 1 |
| 7.40E-11 | 7.40E-11 | ##### | 4.69E-10 | 3.95E-10 | 25 | 1 |

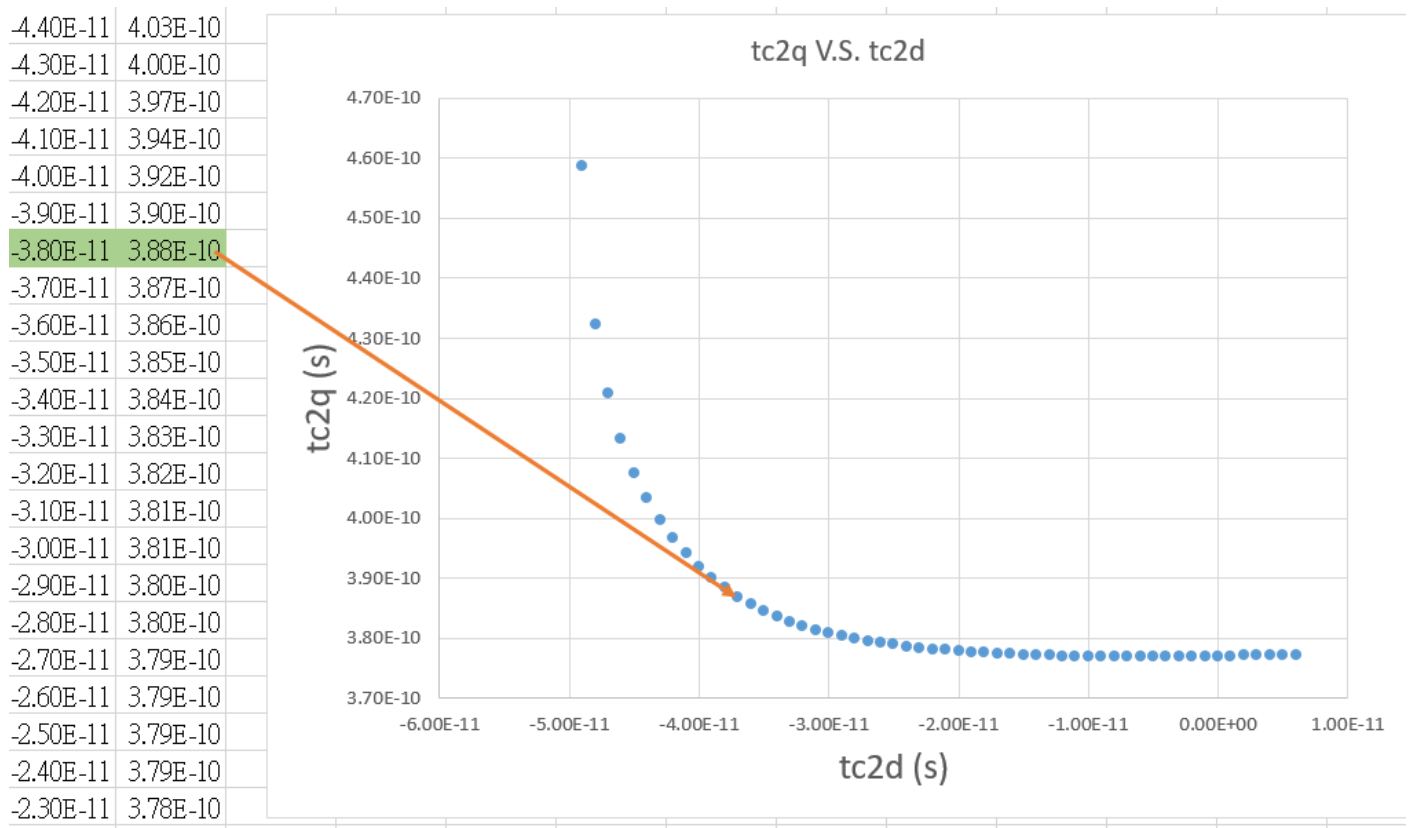
So, when t_{d2c} has minimum (465ps), $t_{c2q} = 465 - 64$ (setup time) = 401ps. I found $t_{c2q}=401ps$ on hold time excel file, and then $t_{c2q} = -18ps$, which is hold time.



Falling characterization



So, when $td2c$ has minimum (468ps), $tc2q = 465 - 76$ (setup time) = 389ps. I found $tc2q = 388ps$ (~389ps) on hold time excel file, and then $tc2d = -38ps$, which is hold time.



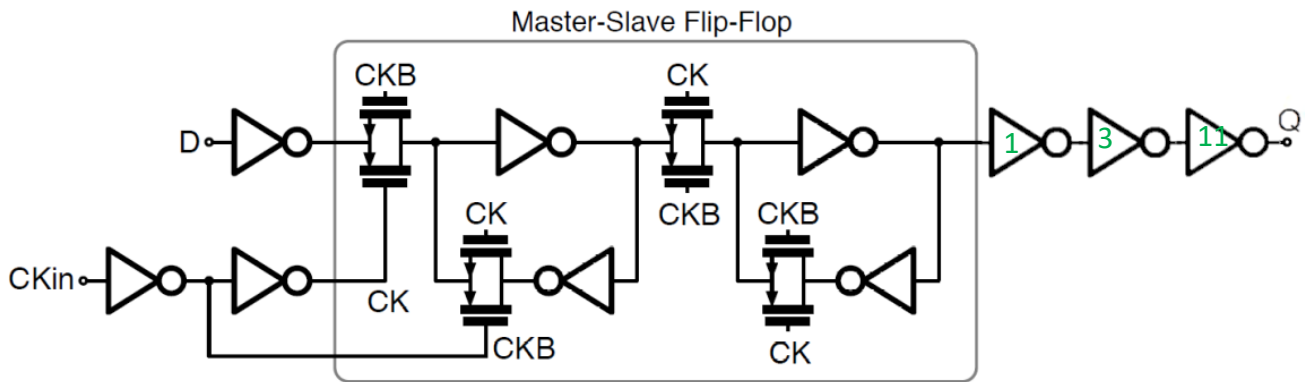
Power

```

*****
* -----
***** transient analysis tnom= 25.000 temp= 25.000 *****
total_avg_pwr_uw= 33.65845 from= 610.00000n to= 1.01000u

***** job concluded
*****

```



Explain:

I added another two inverters at node Q to reduce the delay. From the last homework, I knew total capacitance of an inverter (PMOS $\frac{W}{L} = \frac{1.5u}{0.18u}$, NMOS $\frac{W}{L} = \frac{0.5u}{0.18u}$) looking from gate is 3.78fF.

$$\text{Therefore, } F = GBH = 1 \times 1 \times \frac{200}{3.78} = 52.91. \log_4 F = 2.862$$

Since the Q is supposed to follow the polarity of D, I could only add even number of inverters.

Add 2 more inverters,

$$\hat{f} = \sqrt[3]{52.91} = 3.754$$

$$D = 3 \times (3.754 + 1) = 14.26$$

Add 4 more inverters,

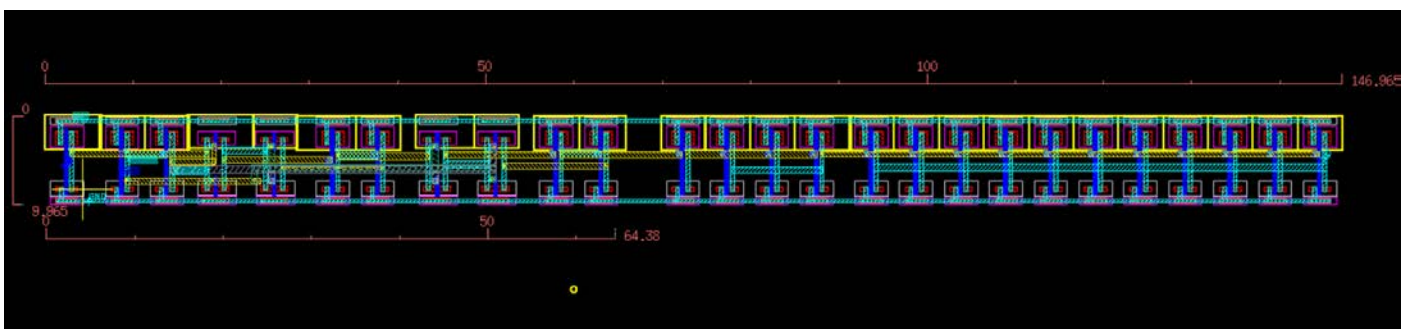
$$\hat{f} = \sqrt[5]{52.91} = 2.21$$

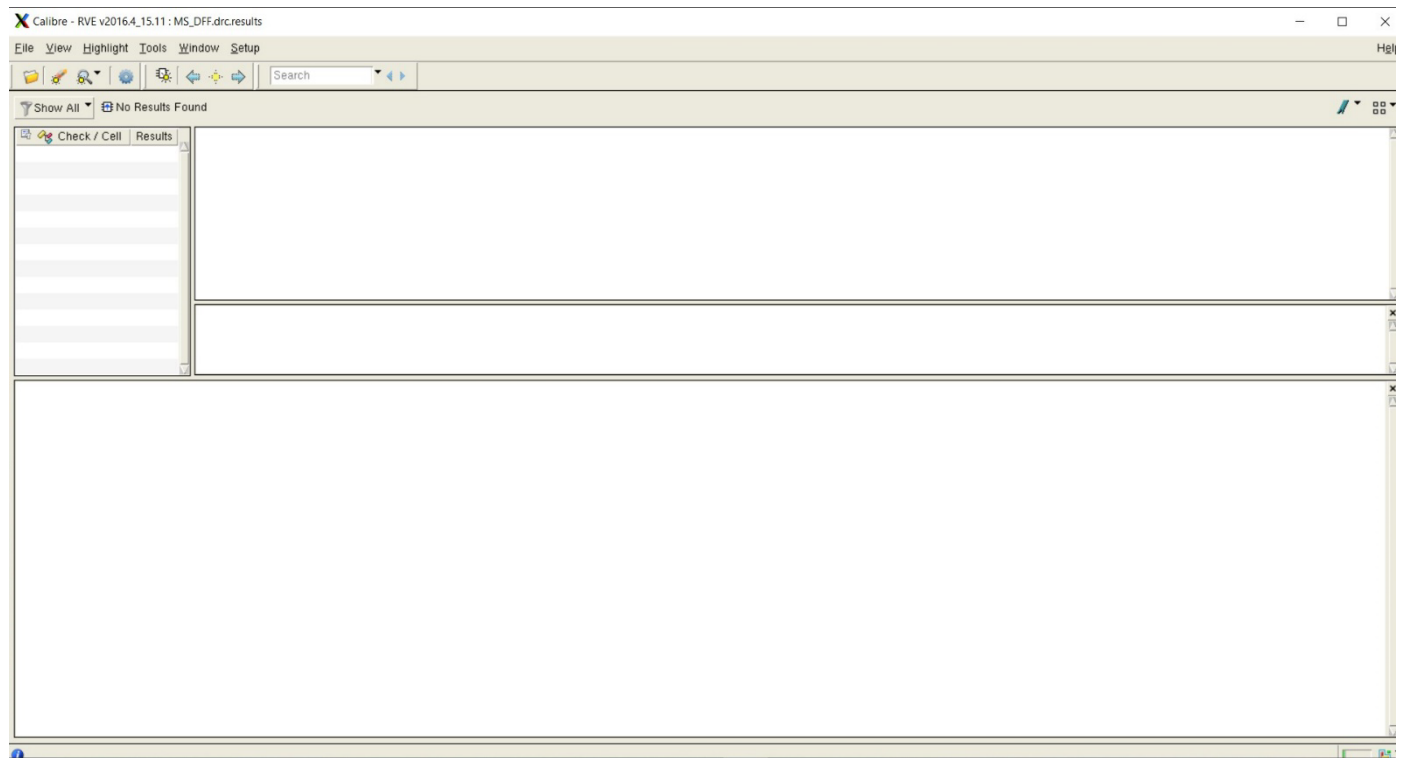
$$D = 3 \times (3.754 + 1) = 16.058$$

So, I added 2 more inverters! 2nd inverter's size is 3X 1st inverter's size, 3rd inverter's size is 11X 1st inverter's size. (3*3.75=11.25)

Originally, without any extra inverters, minimum td2q is about 700ps~800ps. After adding them, minimum td2q goes down to 465ps.

3.





Calibre - RVE v2016.4.15.11: sldb MS_DFF

File View Highlight Tools Window Setup

Comparison Results x

| Layout Cell / Type | Source Cell | Nets | Instances | Ports |
|--------------------|-------------|----------|-----------|--------|
| MS_DFF | MS_DFF | 14L, 14S | 12L, 12S | 7L, 7S |

Cell MS_DFF Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

CORRECT

LAYOUT CELL NAME: MS_DFF
SOURCE CELL NAME: MS_DFF

INITIAL NUMBERS OF OBJECTS

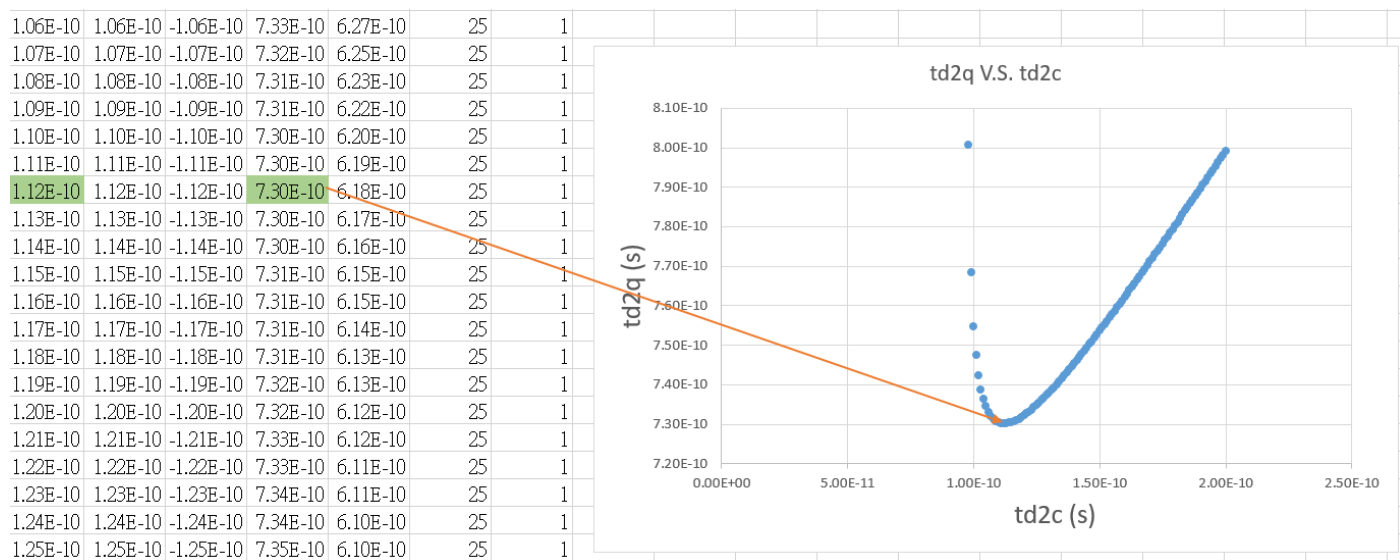
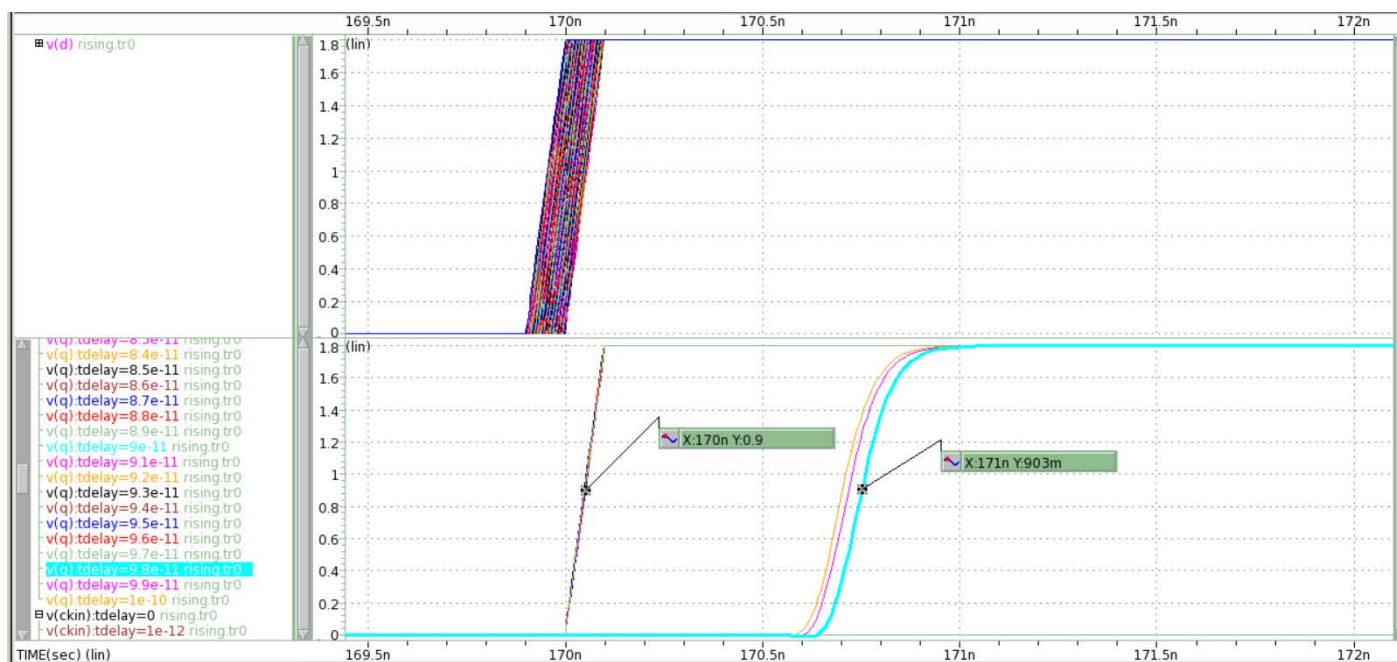
| | Layout | Source | Component Type |
|-------------|--------|--------|--------------------------------|
| Ports: | 7 | 7 | |
| Nets: | 16 | 16 | |
| Instances: | 26 | 14 | * MN (4 pins) * MP (4 pins) |
| Total Inst: | 52 | 28 | |

NUMBERS OF OBJECTS AFTER TRANSFORMATION

Layout consideration:

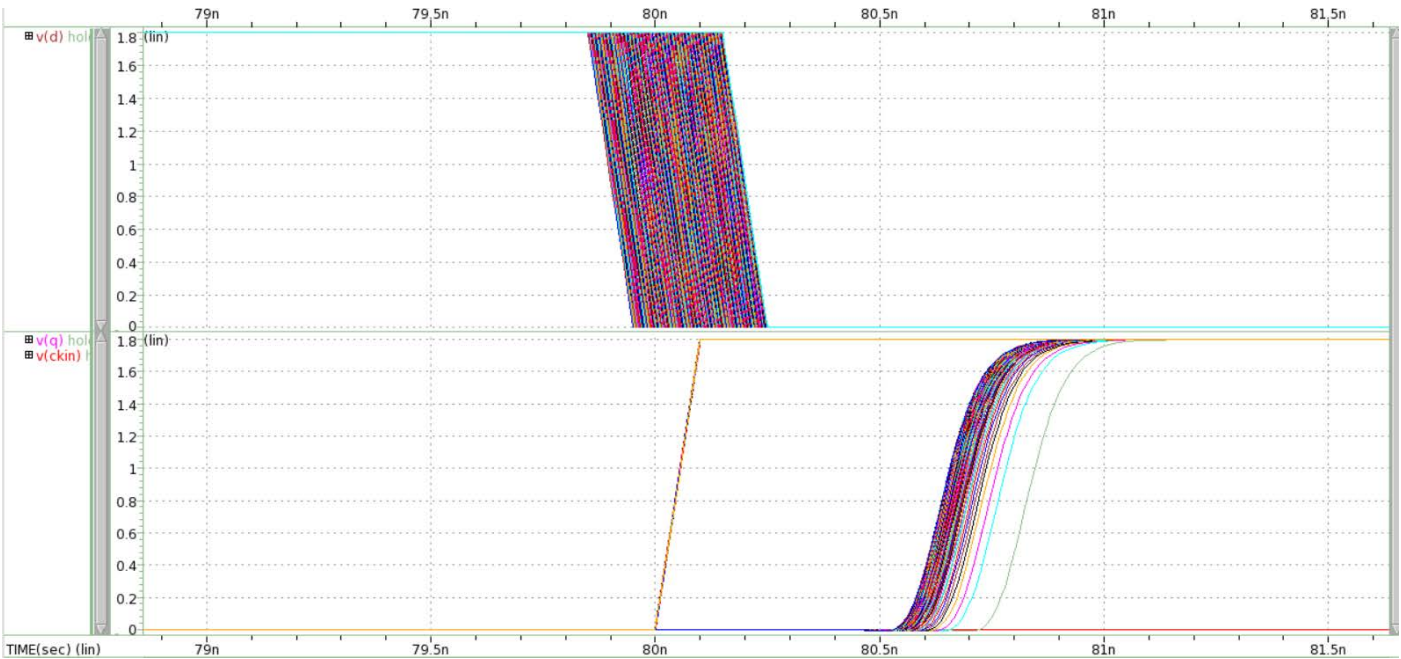
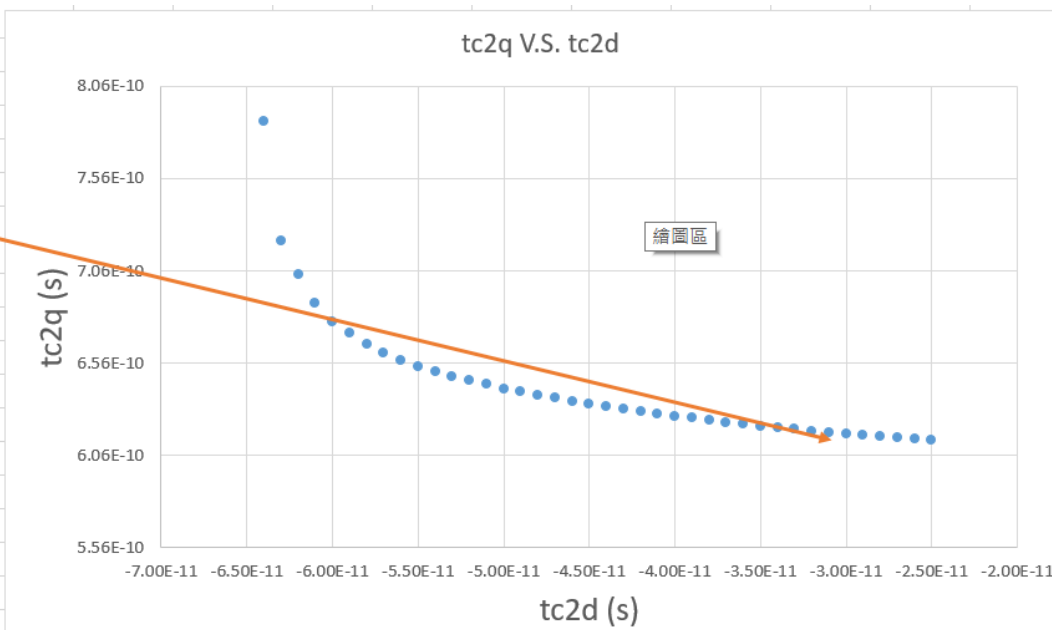
I put each transistor close to each other to reduce the length of metal, which would lead to parasitic resistors and capacitors, so that the delay wouldn't be bad. And I tried to connect nodes and nodes with metal instead of polysilicon as polysilicon has high resistance (impact the performance especially when two nodes are far away from each other).

4. Rising characterization

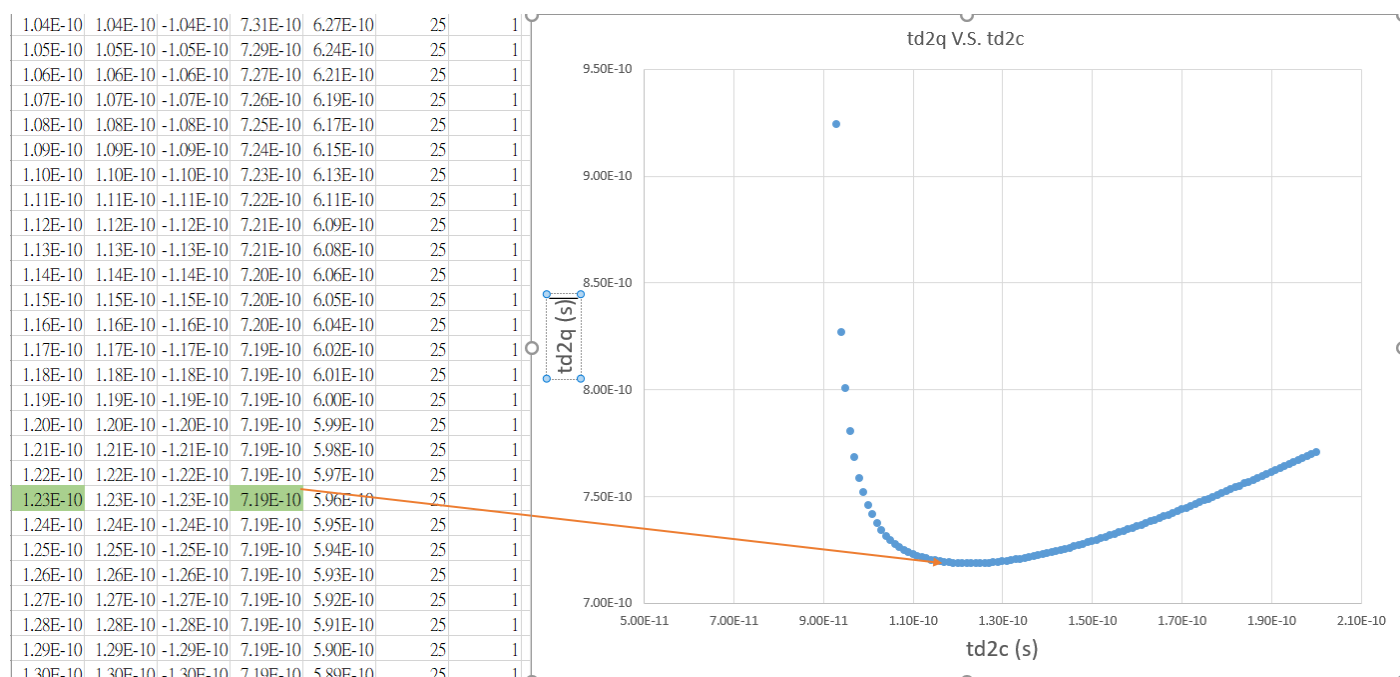
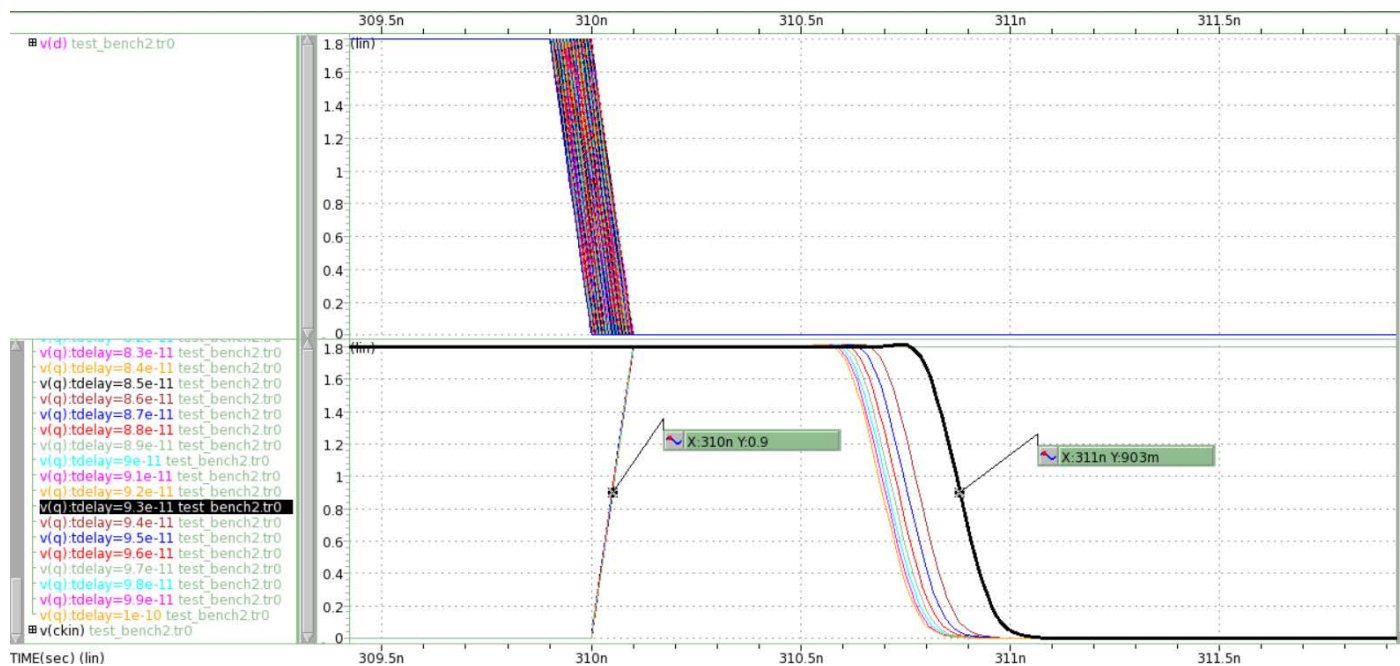


So, when td2c has minimum (730ps), tc2q = 730- 112 (setup time) = 618ps. I found tc2q= 618ps on hold time excel file, and then tc2d = -31ps, which is hold time.

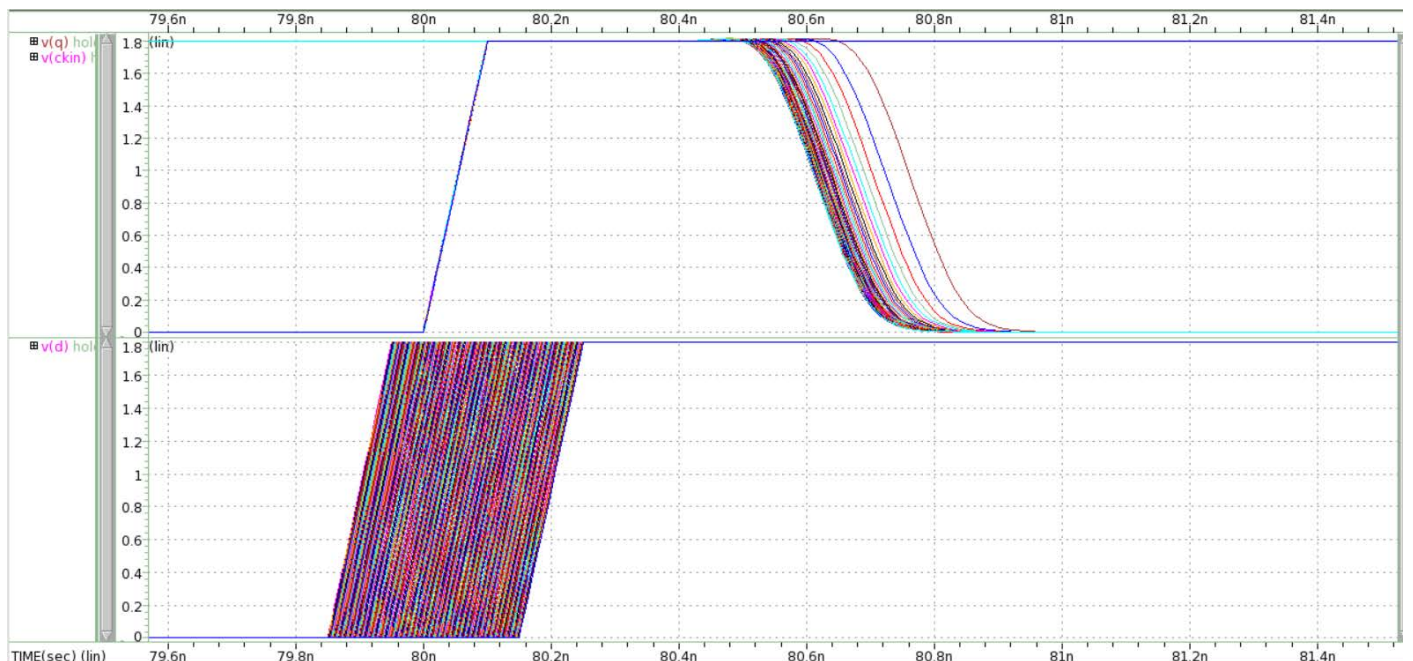
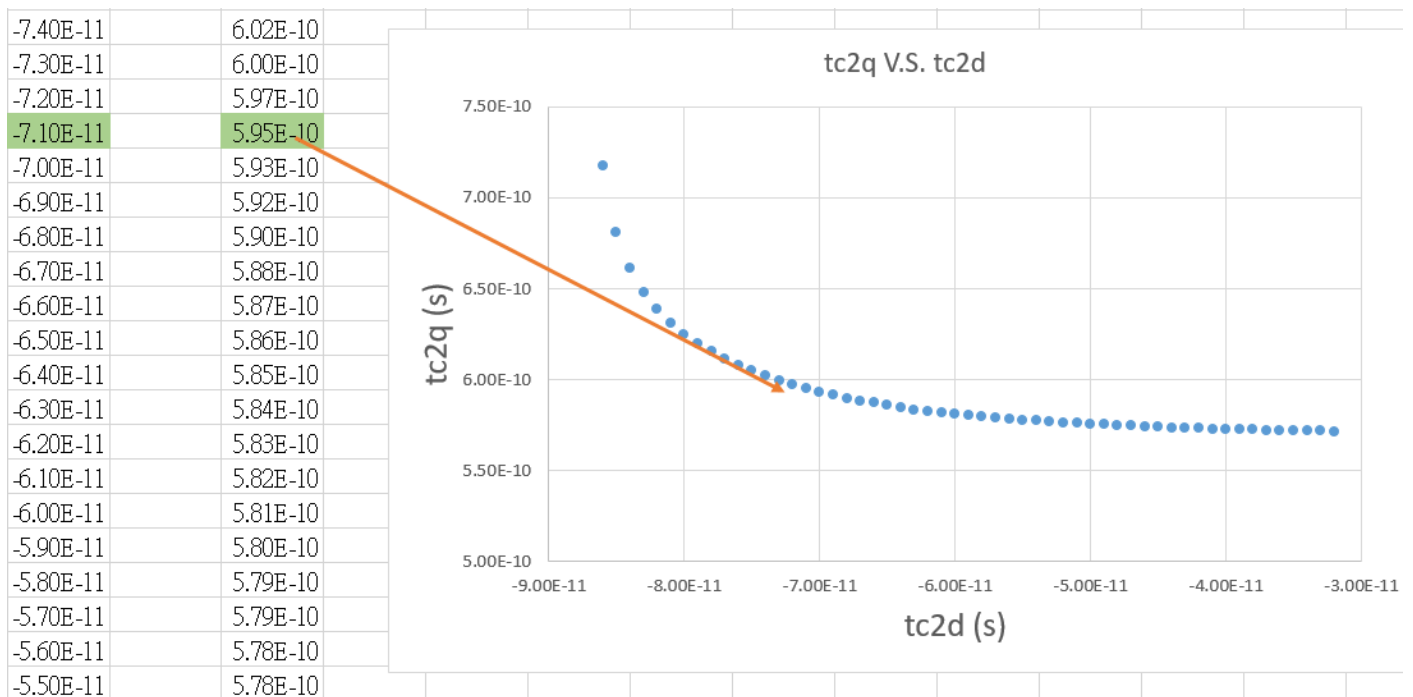
| | |
|-----------|----------|
| -3.70E-11 | 6.24E-10 |
| -3.60E-11 | 6.23E-10 |
| -3.50E-11 | 6.22E-10 |
| -3.40E-11 | 6.21E-10 |
| -3.30E-11 | 6.20E-10 |
| -3.20E-11 | 6.19E-10 |
| -3.10E-11 | 6.18E-10 |
| -3.00E-11 | 6.18E-10 |
| -2.90E-11 | 6.17E-10 |
| -2.80E-11 | 6.16E-10 |
| -2.70E-11 | 6.15E-10 |
| -2.60E-11 | 6.15E-10 |
| -2.50E-11 | 6.14E-10 |



Falling characterization



So, when t_{d2c} has minimum (719ps), $t_{c2q} = 719 - 123$ (setup time) = 596ps. I found $t_{c2q} = 595\text{ps}$ (~596ps) on hold time excel file, and then $t_{c2d} = -71\text{ps}$, which is hold time.



Power

```

* -----
***** transient analysis tnom= 25.000 temp= 25.000 *****
total_avg_pwr_uw= 44.80439 from= 610.00000n to= 1.01000u
***** job concluded
*****
* -----

```

5.

| | Pre-layout simulation | | Post-layout simulation | |
|---------------------------|-----------------------|---------|------------------------|---------|
| | Rising | Falling | Rising | Falling |
| t_{SU} | 64ps | 76ps | 112ps | 123ps |
| $\underline{t_H}$ | -18ps | -38ps | -31ps | -71ps |
| minimum t_{D2Q} | 465ps | 468ps | 730ps | 719ps |
| minimum t_{CK2Q} | 390ps | 380ps | 599ps | 569ps |
| Power consumption (mW) | 0.033658 | | 0.04480439 | |
| Layout area (μm^2) | 1460 | | | |