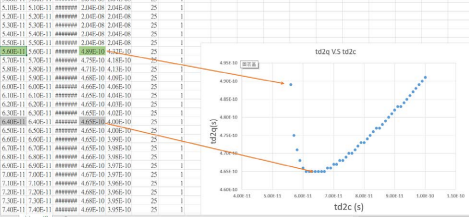
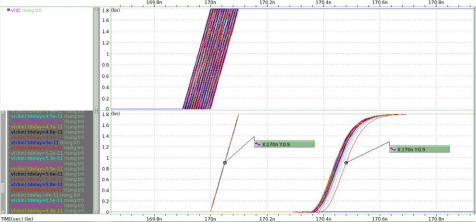
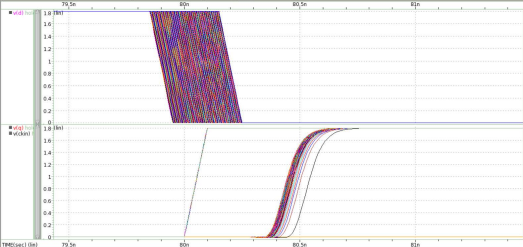
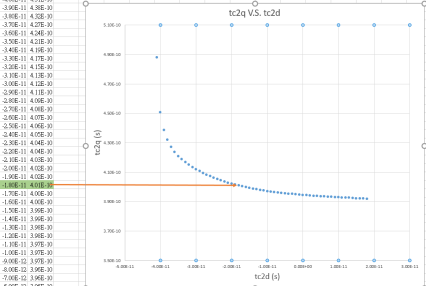
1.

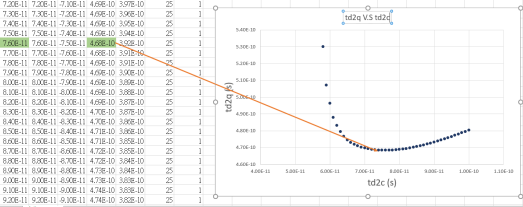
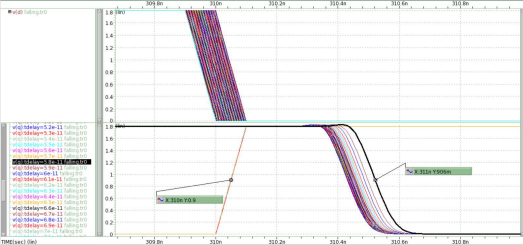
Rising characterization



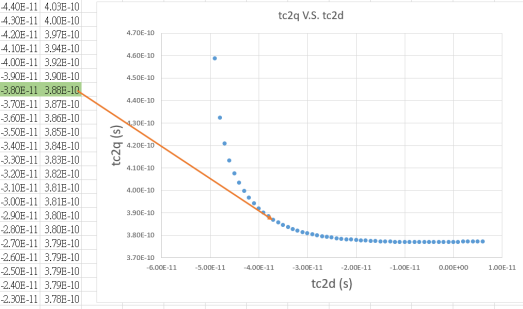
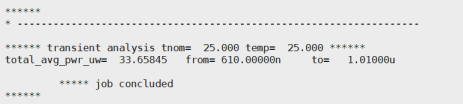
So, when td2c has minimum (465ps), tc2q = 465- 64 (setup time) = 401ps. I found tc2q=401ps on hold time excel file, and then tc2q = -18ps, which is hold time.



Falling characterization

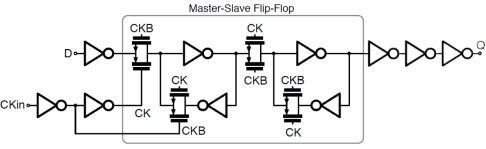


So, when td2c has minimum (468ps), tc2q = 465- 76 (setup time) = 389ps. I found tc2q= 388ps (~389ps) on hold time excel file, and then tc2d = -38ps, which is hold time.

Power

2

Explain:

1 3 11

I added another two inverters at node Q to reduce the delay. From the last homework, I knew total capacitance of an inverter (PMOS �������� = 1.5����

0.18���� ,NMOS �������� = 0.5����

0.18����) looking from

gate is 3.78fF.

Therefore, F = GBH = 1 × 1 ×200

3.78 = 52.91. log4 ���� = 2.862

Since the Q is supposed to follow the polarity of D, I could only add even number of inverters.

Add 2 more inverters,

����̂ = √52.91 3 = 3.754

D = 3 × (3.754 + 1) = 14.26

Add 4 more inverters,

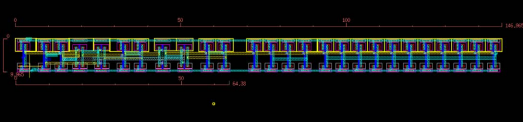
����̂ = √52.91 5 = 2.21

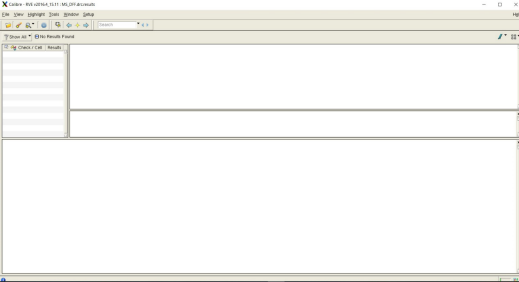
D = 3 × (3.754 + 1) = 16.058

So, I added 2 more inverters! 2nd inverter’s size is 3X 1st inverter’s size, 3rd inverter’s size is 11X 1st inverter’s size. (3\*3.75=11.25)

Originally, without any extra inverters, minimum td2q is about 700ps~800ps. After adding them, minimum td2q goes down to 465ps.

3.





Layout consideration:

I put each transistor close to each other to reduce the length of metal, which would lead to parasitic resistors and capacitors, so that the delay wouldn’t be bad. And I tried to connect nodes and nodes with metal instead of polysilicon as polysilicon has high resistance (impact the performance especially when two nodes are far away from each other).

4.

Rising characterization



So, when td2c has minimum (730ps), tc2q = 730- 112 (setup time) = 618ps. I found tc2q= 618ps on hold time excel file, and then tc2d = -31ps, which is hold time.



Falling characterization



So, when td2c has minimum (719ps), tc2q = 719- 123 (setup time) = 596ps. I found tc2q= 595ps (~596ps) on hold time excel file, and then tc2d = -71ps, which is hold time.

Power



5.

