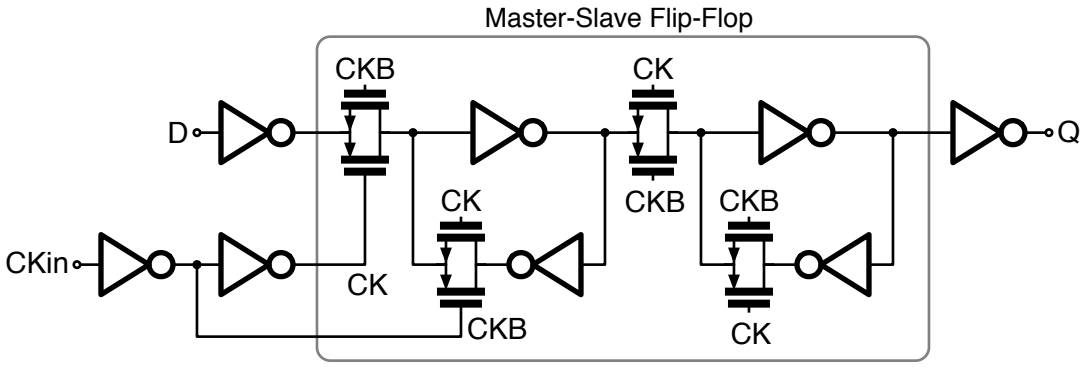
EE3230 VLSI Design (2019 Fall) HW #4

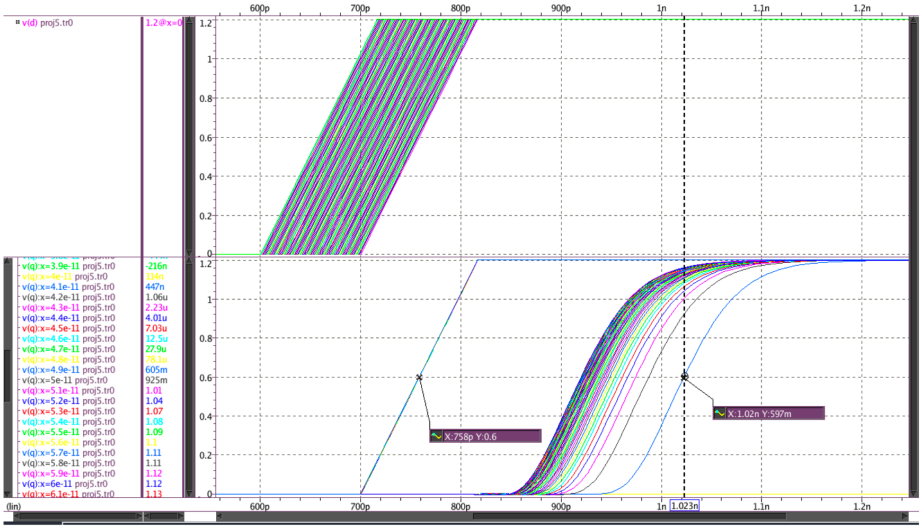
Due date: 2019/12/16 (Monday) 10am

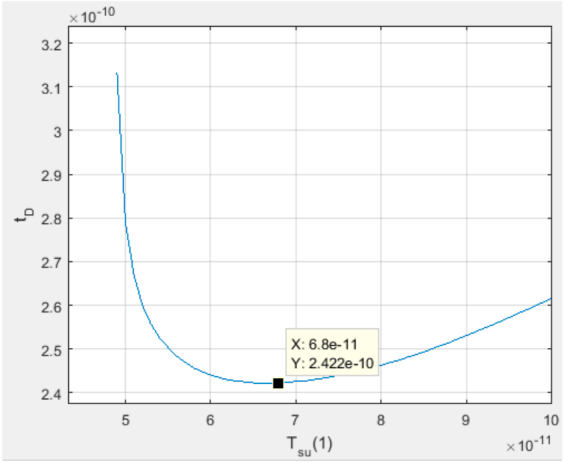
No plagiarism is allowed!!

1. Please design a master-slave flip-flop with the following schematics.
   - V_{DD}=1.8 V, and the input clock CKin runs at 50MHz.
   - For all the input ports (D and CKin), before entering the module, each input sees a unit inverter (and only the unit inverter) with the following specified size: $(W/L)_N$=0.5μ/0.18μ and $(W/L)_P$=1.5μ/0.18μ.
   - The output (Q) drives a capacitor load of 200*f*F.
   - The rise and fall times of input signals (D and CKin) are 0.1ns.
   - You are allowed to insert inverters wherever you like to improve the performance. In this case, please provide an updated schematic and explain you design considerations. However, remember to keep the polarity of Q correct. (In other words, Q should follow the polarity of D.)
   - You can decide all the transistor sizes by yourself except the unit inverters that D and CKin sees.
   - TA will provide a testbench file for your convenience later.



1. Please characterize the flilp-flop's setup time, hold time, and propagation delays, for both rising and falling input transitions. Also, with an input signal that transitions once every clock cycle, please measure the power consumption.
    - The measurement accuracy should be better than 1ps. That is to say, when sweeping the relative delay between D and Ckin, change it with a step smaller than 1ps.
    - In the report, please provide the timing waveforms of D, Ckin, and Q for all the characteristics you measure. The following shows one example that I found on Internet of setup time for rising input. Please put all delay cases into one figure.
    - Please also plot t_{D2Q} vs. t_{D2CK} for all the characteristics that you measure. Label the curve and show how you measure the setup time like the following example that I found on Internet.





2. Explain what you have done to improve the performance (i.e., to speed up the operation and/or to reduce the power consumption). If you ever modify the schematics, provide the updated version in your report.

3. Complete the layout. Snapshot the screens that show DRC and LVS clean. Show a snapshot of the layout (with rulers placed that show x and y dimensions) in your report. Report the area. Furthermore, explain your layout considerations.

4. Run post-layout simulation (R-C-CC extraction) and measure the power consumption, setup time, hold time, and propagation delays, for both rising and falling input transitions again.

5. Complete the following table and show it in your report.

	Pre-layout simulation		Post-layout simulation	
	Rising	Falling	Rising	Falling
t_{SU}	64ps	76ps	112ps	123ps
t_H	-18ps	-38ps	-31ps	-71ps
minimum t_{D2Q}	465ps	468ps	730ps	719ps
minimum t_{CK2Q}	390ps	380ps	599ps	569ps
Power consumption (mW)	0.033658		0.04480439	
Layout area (μm^2)	1460			