Problem 1.

(a)

Use the following hspice code to check ‘’a inverter’’ total gate capacitance.

```
v1 VDD 0 1.8
*VPULSE Vin 0 PULSE 0 1.8 1p 0.1n 0.1n 9.9n
v2 Vin 0 0.9

M0 drain_0 Vin VDD VDD p_18 w = 1.5u l = 0.18u m = 1
M1 drain_0 Vin gnd gnd n_18 w = 0.5u l = 0.18u m = 1

.op
```

In *.lis file, I can check out the result as following

```
**** mosfets


subckt
element  0:m0       0:m1
model    0:p_18.1   0:n_18.1
region     Saturati   Saturati
 id       -66.7119u   66.7119u
 ibs      1.013e-20 -2.999e-20
 ibd      146.3393a  -50.0901a
 vgs     -900.0000m  900.0000m
 vds       -1.3362   463.8172m
 vbs         0.          0.
 vth     -529.5173m  477.9329m
 vdsat   -381.3316m  299.8501m
 vod     -370.4827m  422.0671m
 beta     805.0019u  973.3697u
 gam eff  557.0840m  507.4537m
 gm       265.0277u  214.6819u
 gds       10.6478u   33.9348u
 gmb       84.1057u   28.3871u
 cdtot      1.6788f  827.4834a
 cgtot      2.8502f  930.1441a
 cstot      4.1715f    1.4545f
 cbtot      3.4260f    1.4895f
 cgs        2.1375f  655.4393a
 cgd      530.1466a  187.2222a
```

With this information, I can compute path effort (F = GBH).

G = 1 (since it’s an inverter chain)

B = 1 (no branching)

H = $\frac{10p}{2.8502f+930.1441a} = 2645.261843$

Therefor, F = 2645.261843.

N (number of stages) = $\log_4 F$ = 5.685

Parasitic delay of an inverter = 1

If N = 5,

$\hat{f} = \sqrt[5]{2645.261843} = 4.836$

D = 5× $(4.836 + 1)$ = 29.18

If N = 7,

$\hat{f} = \sqrt[7]{2645.261843} = 3.083$

D = 7× $(3.083 + 1)$ = 28.58

If N = 9,

$\hat{f} = \sqrt[9]{2645.261843} = 2.4$

D = 9× $(2.4 + 1)$ = 30.6

So if total stage is equal to 7, the inverter chain will have shortest propagation delay.

當 N = 7 時，每個 inverter 要推 3.083 個自己，所以我調整 multiple device ratio 來達成要求。所以 m 會一直乘 3.083。(如 Fig. 1 所示)

```
M0 drain_1 Vin VDD VDD p_18 w = 1.5u l = 0.18u m = 1
M1 drain_1 Vin gnd gnd n_18 w = 0.5u l = 0.18u m = 1

M2 drain_2 drain_1 VDD VDD p_18 w = 1.5u l = 0.18u m = 3
M3 drain_2 drain_1 gnd gnd n_18 w = 0.5u l = 0.18u m = 3

M4 drain_3 drain_2 VDD VDD p_18 w = 1.5u l = 0.18u m = 9
M5 drain_3 drain_2 gnd gnd n_18 w = 0.5u l = 0.18u m = 9 $3*3.083 = 9.249

M6 drain_4 drain_3 VDD VDD p_18 w = 1.5u l = 0.18u m = 29 $9.249*3.083 = 28.5
M7 drain_4 drain_3 gnd gnd n_18 w = 0.5u l = 0.18u m = 29

M8 drain_5 drain_4 VDD VDD p_18 w = 1.5u l = 0.18u m = 89 $29*3.083 = 89.407
M9 drain_5 drain_4 gnd gnd n_18 w = 0.5u l = 0.18u m = 89

M10 drain_6 drain_5 VDD VDD p_18 w = 1.5u l = 0.18u m = 276 $89.407*3.083 = 275.64
M11 drain_6 drain_5 gnd gnd n_18 w = 0.5u l = 0.18u m = 276

M12 Vout drain_6 VDD VDD p_18 w = 1.5u l = 0.18u m = 851
M13 Vout drain_6 gnd gnd n_18 w = 0.5u l = 0.18u m = 851 $276*3.083 = 850.908
```

Fig. 1 My design of the inverter chain

(b)

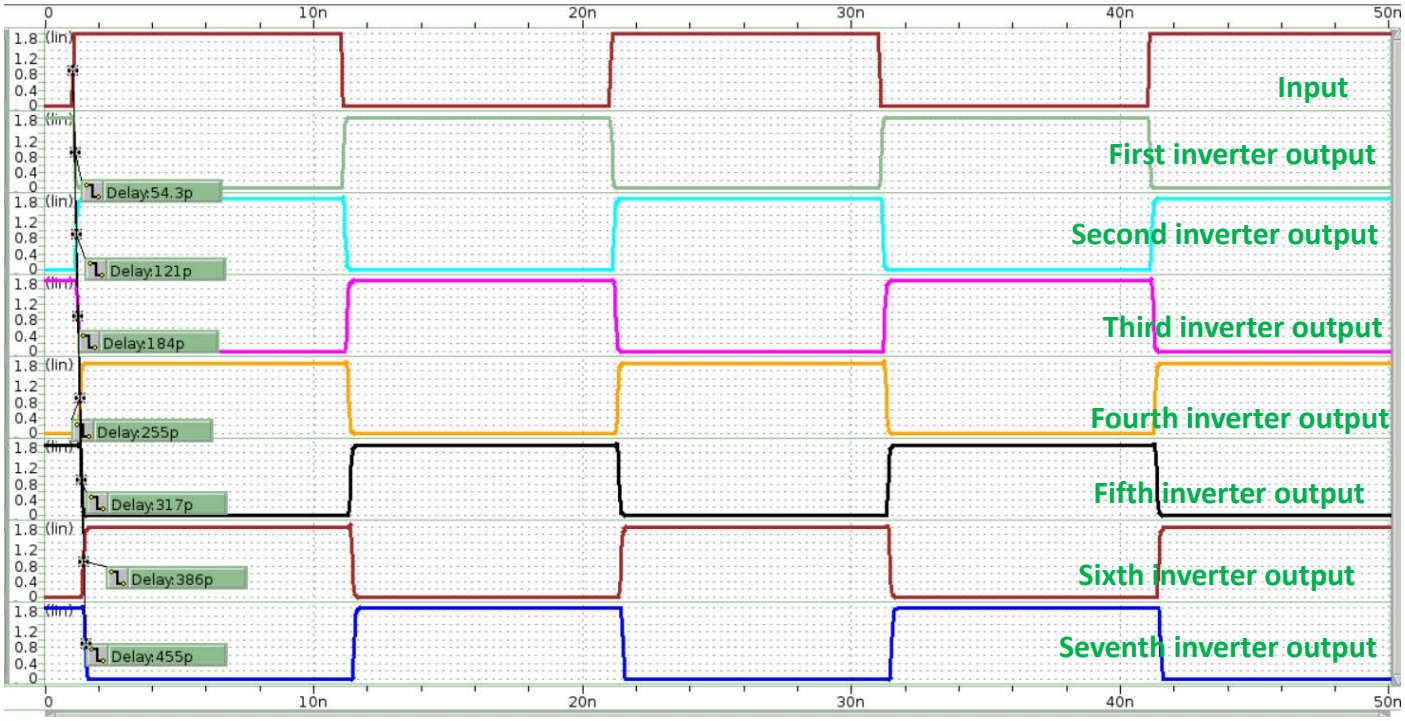


Fig. 2 Delay of each inverter output (compared with the first input of a first inverter) when the first input of first inverter is rising.

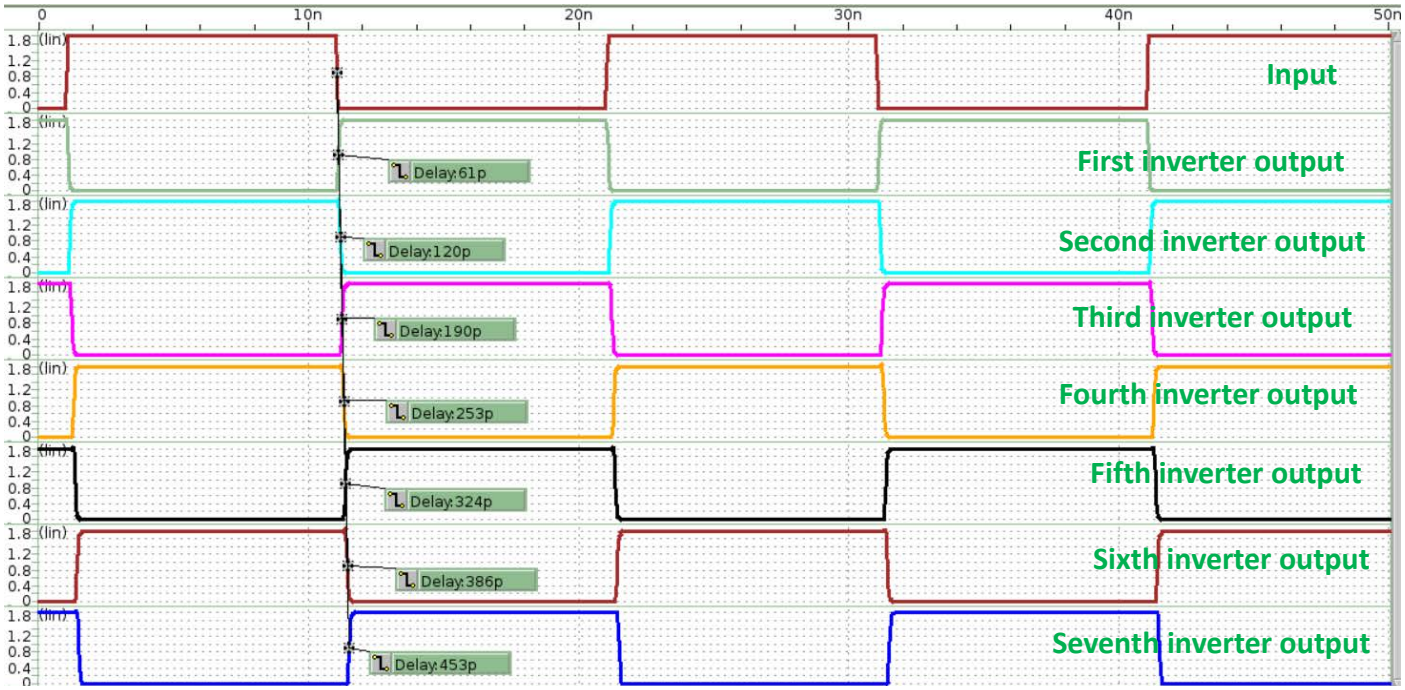


Fig. 3 Delay of each inverter output (compared with the first input of a first inverter) when the first input of first inverter is falling

(c)

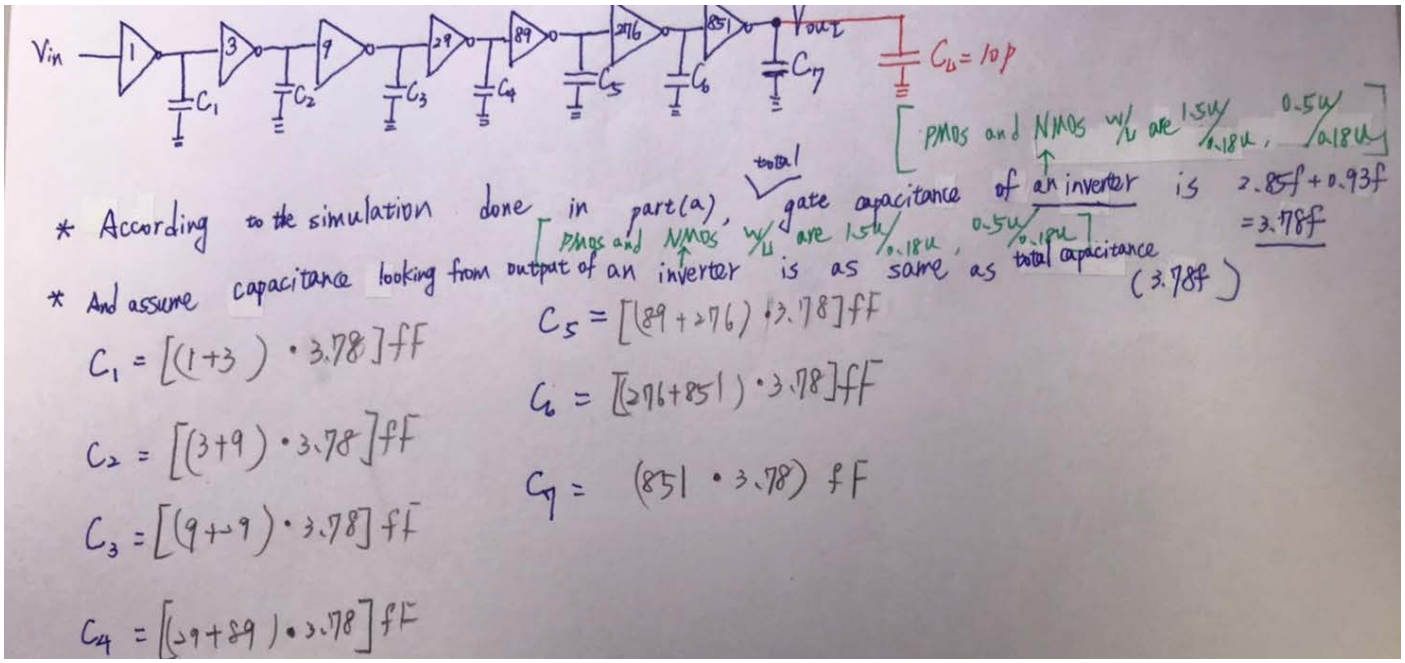


Fig. 4 My design of an inverter chain and some analysis

My estimation:

$$P = C \times VDD^2 \times f = (C_1 + C_2 + C_3 + C_4 + C_5 + C_6 + C_7 + C_L) \times 1.8^2 \times 50M = [2515 \times 3.78f + 10p) \times 1.8^2 \times 50M = 3.16mW$$

(d)

Use the following hspice code to measure average power of a period.

```
.meas tran power AVG power from = 0.5n to =  20.5n
```

The result can be found in *.lis as shown below.

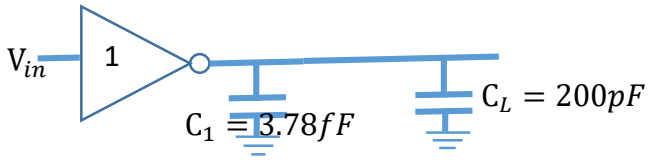
```
****** transient analysis tnom=  25.000 temp=  25.000 ******
power=   3.3908m  from= 500.0000p     to=  20.5000n
```

Discussion: The estimated power (3.16mW) is less than measured power (3.39mW). The error rate is $\frac{3.16-3.39}{3.39} = 6.78\%$. I think the difference comes from static power. To be specific, when performing hand analysis, I didn't take static power into consideration, including subthreshold leakage, gate leakage, etc. However, hspice simulation will consider static power, which leads to the difference between hand analysis and hspice simulation.

Problem 2.

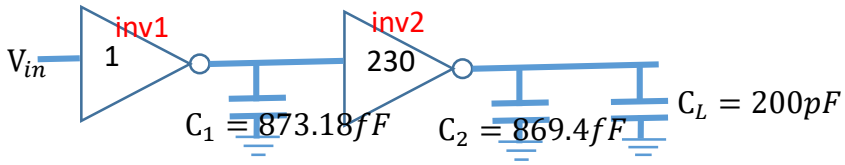
(a) Same as problem 1 (c), I assume capacitance looking from an inverter (with PMOS and NMOS (W/L) are 1.5u/0.18u and 0.5u/0.18u respectively) output and input is all 3.78fF

n = 1,



$P = C_{total} \times VDD^2 \times f = (C_1 + C_L) \times 1.8^2 \times 50M = (3.78f\text{+200p}) \times 1.8^2 \times 50M$ =32.4 mW

n = 2,



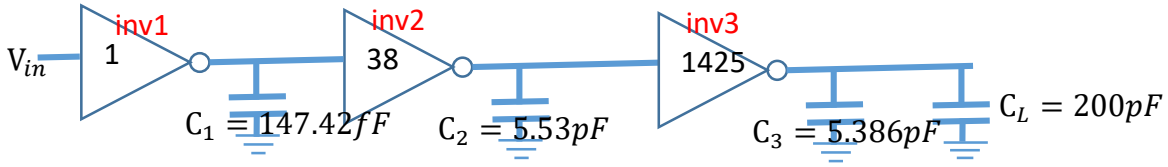
By the calculation in problem 2_(b), inv2 size is 230X inv1 ($\hat{f}$=230)

Thus, $C_1 = (1 + 230) \times 3.78f = 873.18fF$

$C_2 = 230 \times 3.78f = 869.4fF$

$P = C_{total} \times VDD^2 \times f = (C_1 + C_2 + C_L) \times 1.8^2 \times 50M = (873.18f + 869.4f\text{+200p}) \times 1.8^2 \times 50M$ =32.68 mW

n = 3,



By the calculation in problem 2_(b), inv2 size is 38X inv1, inv3 size is 1425X inv1

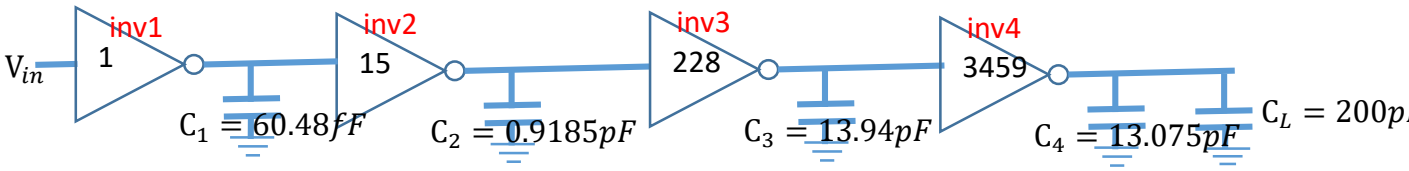
Thus, $C_1 = (1 + 38) \times 3.78f = 147.42fF$

$C_2 = (38 + 1425) \times 3.78f = 5.53pF$

$C_3 = 1425 \times 3.78f = 5.386pF$

$P = C_{total} \times VDD^2 \times f = (C_1 + C_2 + C_3 + C_L) \times 1.8^2 \times 50M = (0.147p + 5.53p + 5.38p\text{+200p}) \times 1.8^2 \times 50M$ =34.19 mW

n = 4,

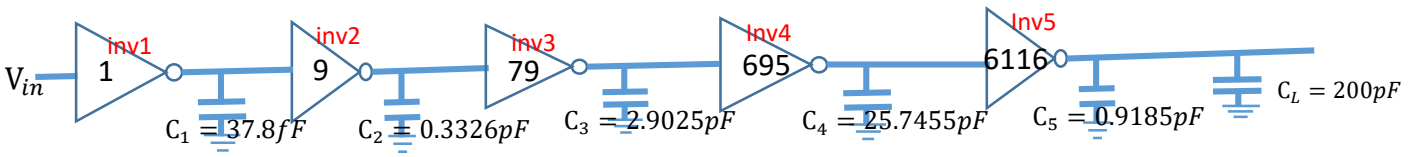


By the calculation in problem 2_(b), inv2 size is 15X inv1 ($\hat{f}$=15.17), inv3 size is 228X inv1 ($15\times 15.17 = 228$), inv4 size is 3459X inv1 ($228\times 15.17 = 3459$)

$$\text{Thus,}\quad C_1 = (1+15)\times 3.78f = 60.48fF,$$
$$C_2 = (15+228)\times 3.78f = 0.9185pF$$
$$C_3 = (228+3459)\times 3.78f = 13.94pF$$
$$C_4 = (3459)\times 3.78f = 13.075pF$$

$P = C_{total}\times VDD^2\times f = (C_1+C_2+C_3+C_4+C_L)\times 1.8^2\times 50M = (0.0648p + 0.9185p + 13.94p + 13.075p + 200p)\times 1.8^2\times 50M$ = 36.94 mW

n = 5,

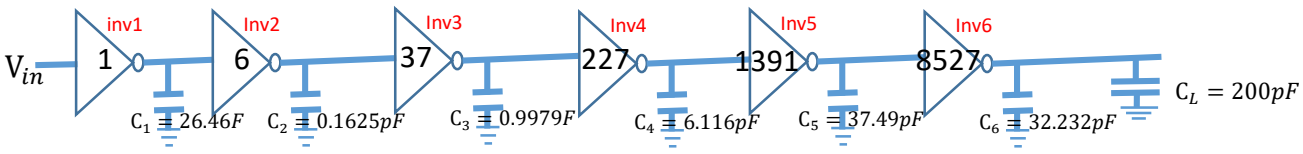


By the calculation in problem 2_(b), inv2 size is 9X inv1 ($\hat{f}$=8.8), inv3 size is 79X inv1 ($9\times 8.8 = 79.2$), inv4 size is 695X inv1 ($79\times 8.8 = 695.2$), inv5 size is 6116X inv1 ($695\times 8.8 = 6116$)

$$\text{Thus,}\quad C_1 = (1+9)\times 3.78f = 37.8fF$$
$$C_2 = (9+79)\times 3.78f = 0.3326pF$$
$$C_3 = (79+695)\times 3.78f = 2.9025pF$$
$$C_4 = (695+6116)\times 3.78f = 25.7455pF$$
$$C_5 = 6116\times 3.78f = 23.1184pF$$

$P = C_{total}\times VDD^2\times f = (C_1+C_2+C_3+C_4+C_5+C_L)\times 1.8^2\times 50M = (0.0378p + 0.3326p + 2.9025p + 25.7455p + 23.1184p + 200p)\times 1.8^2\times 50M$ = 40.85 mW

n = 6,



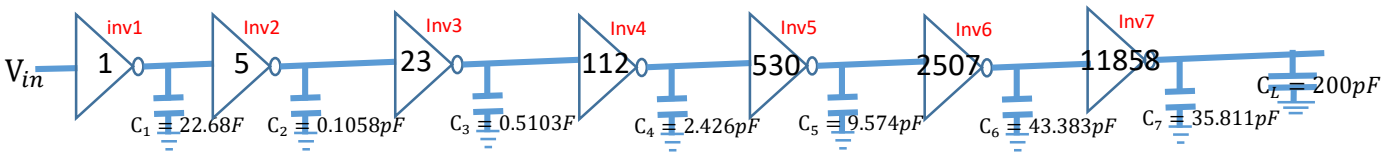
By the calculation in problem 2_(b), inv2 size is 6X inv1 ($\hat{f}$=6.13), inv3 size is 37X inv1 ($6\times 6.13 = 36.78$), inv4 size is 227X inv1 ($37\times 6.13 = 226.81$), inv5 size is 1391X inv1 ($227\times 6.13 =$

1391.51), inv6 size is 8527X inv1 (1391× 6.13 = 8526.83)

$$\text{Thus, } C_1 = (1+6) \times 3.78f = 26.46fF$$
$$C_2 = (6+37) \times 3.78f = 0.16254pF$$
$$C_3 = (37+227) \times 3.78f = 0.99792pF$$
$$C_4 = (227+1391) \times 3.78f = 6.11604pF$$
$$C_5 = (1391+8527) \times 3.78f = 37.49004pF$$
$$C_6 = 8527 \times 3.78f = 32.23206pF$$

$P = C_{total} \times VDD^2 \times f = (C_1 + C_2 + C_3 + C_4 + C_5 + C_6 + C_L) \times 1.8^2 \times 50M = (0.02646p + 0.16254p + 0.99792p$+6.11604p+37.49004$p$+32.23206p+200p)× $1.8^2 \times 50M$=44.88mW

n = 7,

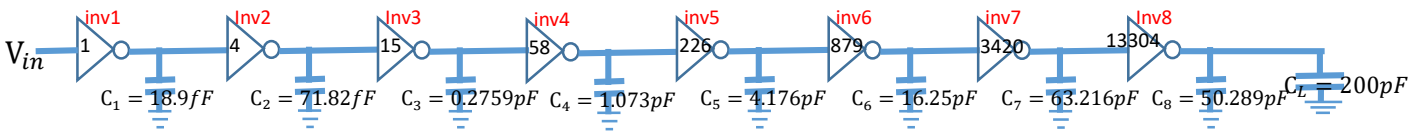


By the calculation in problem 2_(b), inv2 size is 5X inv1 ($\hat{f}$=4.73), inv3 size is 23X inv1 (5× 4.73 = 23.65), inv4 size is 112X inv1 (23.65× 4.73 = 111.86), inv5 size is 530X inv1 (112× 4.73 = 529.76), inv6 size is 2507X inv1 (530× 4.73 = 2506.9), inv7 size is 11858X inv1 (2507× 4.73 = 11858.11)

$$\text{Thus, } C_1 = (1+5) \times 3.78f = 22.68fF$$
$$C_2 = (5+23) \times 3.78f = 0.10584pF$$
$$C_3 = (23+112) \times 3.78f = 0.5103pF$$
$$C_4 = (112+530) \times 3.78f = 2.42676pF$$
$$C_5 = (530+2507) \times 3.78f = 11.479pF$$
$$C_6 = (2507+11858) \times 3.78f = 54.299pF$$
$$C_7 = 11858 \times 3.78f = 44.823pF$$

$P = C_{total} \times VDD^2 \times f = (C_1 + C_2 + C_3 + C_4 + C_5 + C_6 + C_7 + C_L) \times 1.8^2 \times 50M =$ (0.02268p + 0.10584p + 0.5103p+2.42676p+11.479p+54.299p+44.823p+200p)× $1.8^2 \times 50M$= 50.814 mW

n = 8,



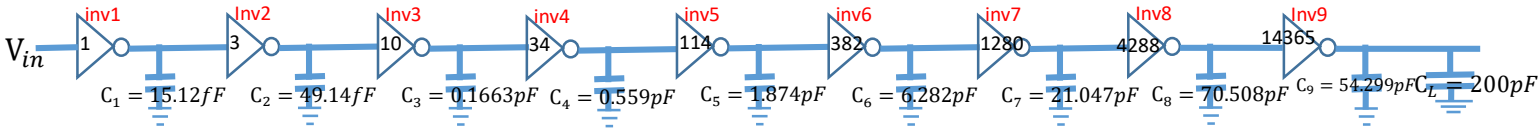
By the calculation in problem 2_(b), inv2 size is 4X inv1 ($\hat{f}$=3.89), inv3 size is 15X inv1 ($4\times 3.89 = 15.56$), inv4 size is 58X inv1 ($15\times 3.89 = 58.35$), inv5 size is 226X inv1 ($58\times 3.89 = 225.62$), inv6 size is 879X inv1 ($226\times 3.89 = 879.14$), inv7 size is 3420X inv1 ($879\times 3.89 = 3419.31$), inv8 size is 13304X inv1 ($3420\times 3.89 = 13303.8$)

Thus,

$$C_1 = (1+4)\times 3.78f = 18.9fF,$$
$$C_2 = (4+15)\times 3.78f = 71.82fF$$
$$C_3 = (15+58)\times 3.78f = 0.2759pF$$
$$C_4 = (58+226)\times 3.78f = 1.073pF$$
$$C_5 = (226+879)\times 3.78f = 4.176pF$$
$$C_6 = (2003+9474)\times 3.78f = 16.25pF$$
$$C_7 = (3420+13304)\times 3.78f = 63.216pF$$
$$C_8 = 13304\times 3.78f = 50.289pF$$

$P = C_{total}\times VDD^2\times f = (C_1+C_2+C_3+C_4+C_5+C_6+C_7+C_8+C_L)\times 1.8^2\times 50M =$ $(0.0189p + 0.07182p + 0.2759p$+1.073p+4.176$p$+16.25p+63.216p+50.289p+200p)$\times 1.8^2\times 50M$= 54.33 mW

n = 9,



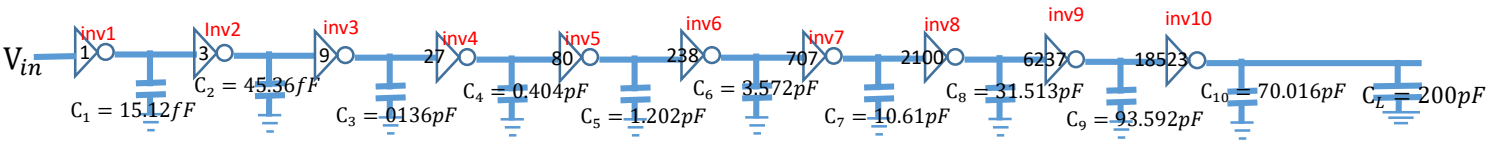
By the calculation in problem 2_(b), inv2 size is 3X inv1 ($\hat{f}$=3.35), inv3 size is 10X inv1 ($3\times 3.35 = 10.05$), inv4 size is 34X inv1 ($10\times 3.35 = 33.5$), inv5 size is 114X inv1 ($34\times 3.35 = 113.9$), inv6 size is 382X inv1 ($114\times 3.35 = 381.9$), inv7 size is 1280X inv1 ($382\times 3.35 = 1297.7$), inv8 size is 4288X inv1 ($1280\times 3.35 = 4288$), inv9 size is 14365X inv1 ($4288\times 3.35 = 14364.8$)

Thus, $C_1 = (1+3)\times 3.78f = 15.12fF$
$$C_2 = (3+10)\times 3.78f = 49.14f$$
$$C_3 = (10+34)\times 3.78f = 0.1663pF$$
$$C_4 = (34+114)\times 3.78f = 0.559pF$$
$$C_5 = (114+382)\times 3.78f = 1.874pF$$
$$C_6 = (382+1280)\times 3.78f = 6.282pF$$
$$C_7 = (1280+4288)\times 3.78f = 21.047pF$$
$$C_8 = (4288+14365)\times 3.78f = 70.508pF$$

$$C_9 = 14365 \times 3.78f = 54.299pF$$

$$P = C_{total} \times VDD^2 \times f = (C_1 + C_2 + C_3 + C_4 + C_5 + C_6 + C_7 + C_8 + C_9 + C_L) \times 1.8^2 \times 50M = (0.01512p + 0.04914p + 0.1663p + 0.559p + 1.874p + 6.282p + 21.047p + 70.508p + 54.299p + 200p) \times 1.8^2 \times 50M = 57.47\ mW$$

n = 10,



By the calculation in problem 2_(b), inv2 size is 3X inv1 ($\hat{f}$=2.97), inv3 size is 9X inv1 ($3\times 2.97 = 8.91$), inv4 size is 27X inv1 ($9\times 2.97 = 26.73$), inv5 size is 80X inv1 ($27\times 2.97 = 80.19$), inv6 size is 238X inv1 ($80\times 2.97 = 237.6$), inv7 size is 707X inv1 ($238\times 2.97 = 706.86$), inv8 size is 2100X inv1 ($707\times 2.97 = 2099.79$), inv9 size is 6237X inv1 ($2100\times 2.97 = 6237$), inv10 size is 18523X inv1 ($6237\times 2.97 = 18523.89$)

Thus, $C_1 = (1 + 3) \times 3.78f = 15.12fF$

$$C_2 = (3 + 9) \times 3.78f = 45.36fF$$

$$C_3 = (9 + 27) \times 3.78f = 0.136pF$$

$$C_4 = (27 + 80) \times 3.78f = 0.404pF$$

$$C_5 = (80 + 238) \times 3.78f = 1.202pF$$

$$C_6 = (238 + 707) \times 3.78f = 3.572pF$$

$$C_7 = (707 + 2100) \times 3.78f = 10.61pF$$

$$C_8 = (2100 + 6237) \times 3.78f = 31.513pF$$

$$C_9 = (6237 + 18523) \times 3.78f = 93.592pF$$

$$C_{10} = 18523 \times 3.78f = 70.016pF$$

$$P = C_{total} \times VDD^2 \times f = (C_1 + C_2 + C_3 + C_4 + C_5 + C_6 + C_7 + C_8 + C_9 + C_{10} + C_L) \times 1.8^2 \times 50M = (0.01512p + 0.04536p + 0.136p + 0.404p + 1.202p + 3.572p + 10.61p + 31.513p + 93.592 + 70.016p + 200p) \times 1.8^2 \times 50M = 66.59mW$$

(b) Same as problem 1 (c), I assume capacitance looking from an inverter (with PMOS and NMOS (W/L) are 1.5u/0.18u and 0.5u/0.18u respectively) output and input is all 3.78fF. And assume parasitic delay = 1 for an inverter

n = 1,

F = GBH = $1 \times 1 \times \frac{200pF}{3.78fF} = 52910$

$\hat{f} = 52910$

D = 52910+1=52911

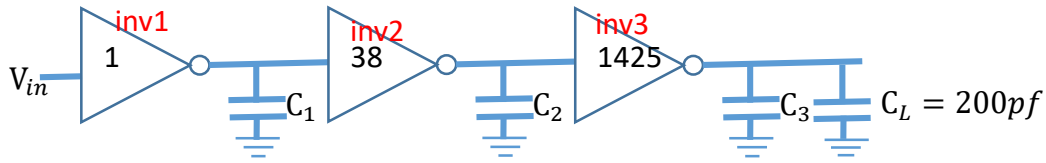
n = 2,

F = 52910

$\hat{f} = \sqrt{52910} = 230$

D = 2(230+1) = 462

n = 3,



F = 52910

$\hat{f} = \sqrt[3]{52910} = 37.5$

D = 3(37.5+1) = 115.5

For inv2,

PMOS W/L = $(1.5u \times 37.5)/0.18u$ (w = 1.5u l = 0.18u m = 38 in hspice)

NMOS W/L = $(0.5u \times 37.5)/0.18u$ (w = 0.5u l = 0.18u m = 38 in hspice)

For inv3,

PMOS W/L = $(1.5u \times 38 \times 37.5)/0.18u$ (w = 1.5u l = 0.18u m = 1425 in hspice)

NMOS W/L = $(0.5u \times 38 \times 37.5)/0.18u$ (w = 0.5u l = 0.18u m = 1425 in hspice)

n = 4,

F = 52910

$\hat{f} = \sqrt[4]{52910} = 15.17$

D = 4(15.17+1) = 64.7

n = 5,

F = 52910

$$\hat{f} = \sqrt[5]{52910} = 8.8$$

D = 5(8.8+1) = 49

n = 6,

F = 52910

$$\hat{f} = \sqrt[6]{52910} = 6.127118695$$

D = 6(6.127118695+1) = 42.76271217

n = 7,

F = 52910

$$\hat{f} = \sqrt[7]{52910} = 4.729237328$$

D = 7(4.729237328+1) = 40.10466129

n = 8,

F = 52910

$$\hat{f} = \sqrt[8]{52910} = 3.89$$

D = 8(3.89+1) = 39.16

n = 9,

F = 52910

$$\hat{f} = \sqrt[9]{52910} = 3.35$$

D = 9(3.35+1) = 39.15

n = 10,

F = 52910

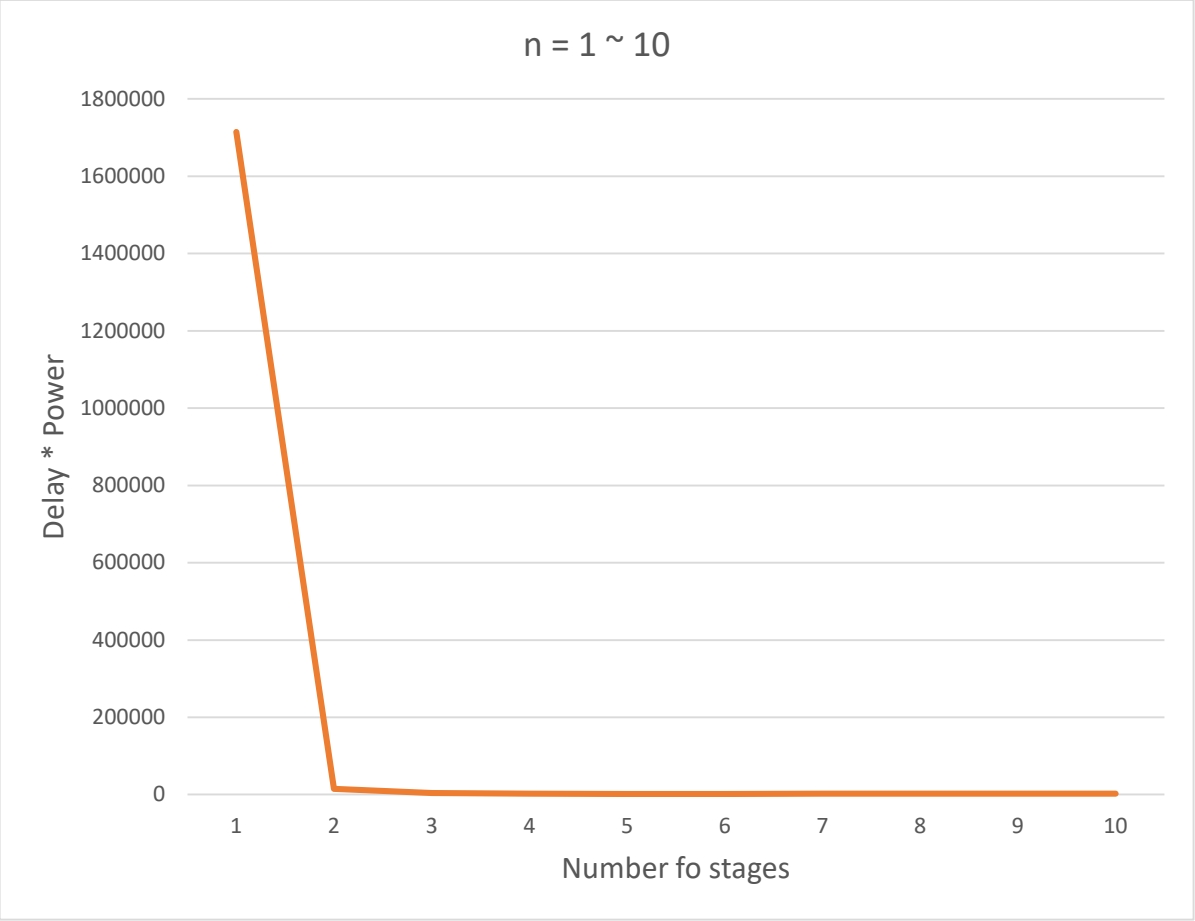
$$\hat{f} = \sqrt[10]{52910} = 2.97$$

D = 10(2.97+1) = 39.7

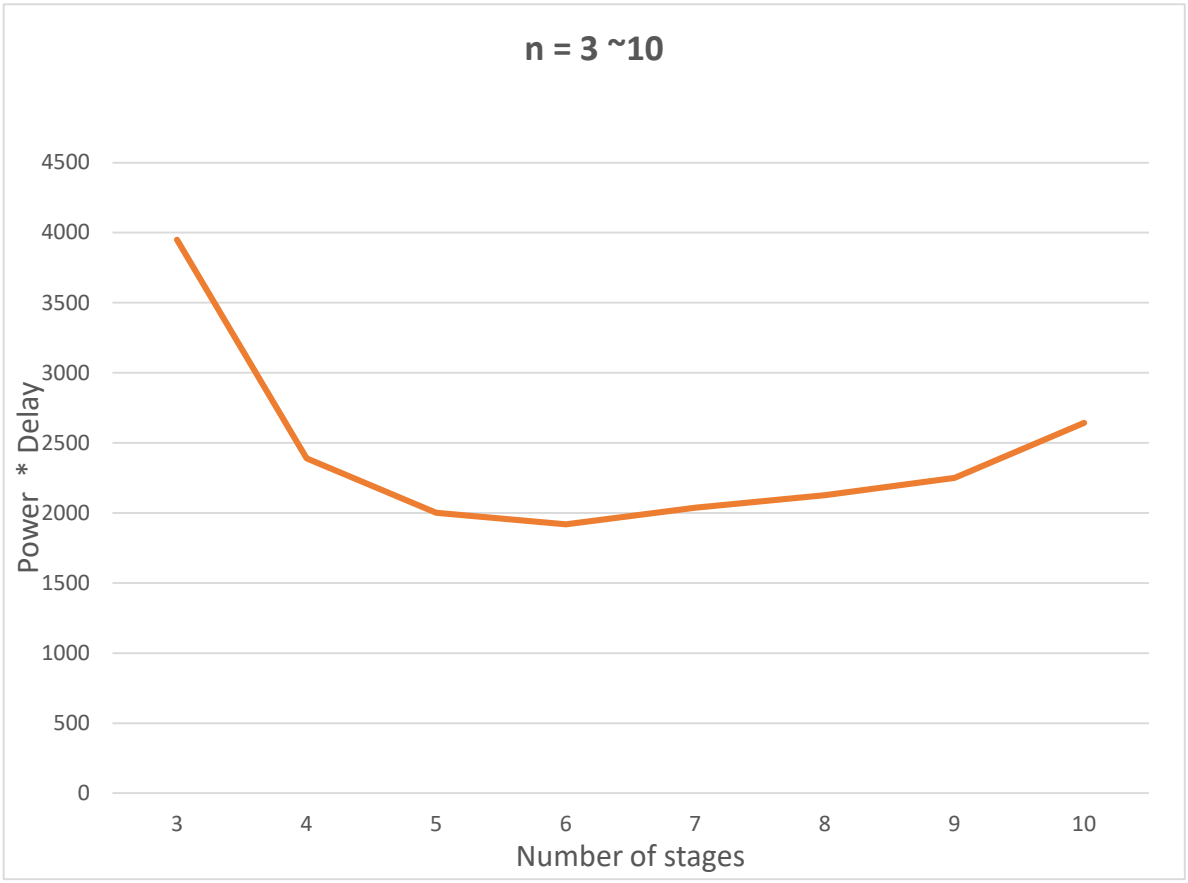
(c)

Combined results from (a), (b). I made a table and graph as the following!

N	Delay	Power consumption (mW)	Product
1	52910	32.4	1714284
2	462	32.68	15098.16
3	115.5	34.19	3948.945
4	64.7	36.94	2390.018
5	49	40.85	2001.65
6	42.763	44.88	1919.203
7	40.105	50.81	2037.735
8	39.16	54.33	2127.563
9	39.15	57.47	2249.951
10	39.7	66.59	2643.623



When n = 1, the delay is too large to observe the difference between other stages' delay. So, I drew another figure which is n = 3 ~ n = 10 below!



When n = 6, Power × delay has smallest value.

In Q2_b, when n = 9, it has the shortest propagation delay. So, 'n' is smaller when Power × delay has smallest value compared to n that caused the shortest propagation delay.

Discussion:

因為 delay 一開始會隨著級數增加而下降，但後來會因為級數的增加，parasitic delay 會增加，delay 反而開始上升 (in this problem, after n > 10)。至於 power 一定會隨著級數增加，每個 node capacitance 加總起來會越來越多，所以根據公式 Power = $C_{total} \times VDD^2 \times f$，power 會越來越多。如果 n 太小 delay 會太大，n 很大 power 會太大。所以要 Power × delay 最小，級數應該落在中間的地方(ex: n = 4, 5, 6, 7)。所以實際算出來 Power × delay 最小的級數 (n = 6)會小於 delay 最小的級數 (n = 9).

(d)

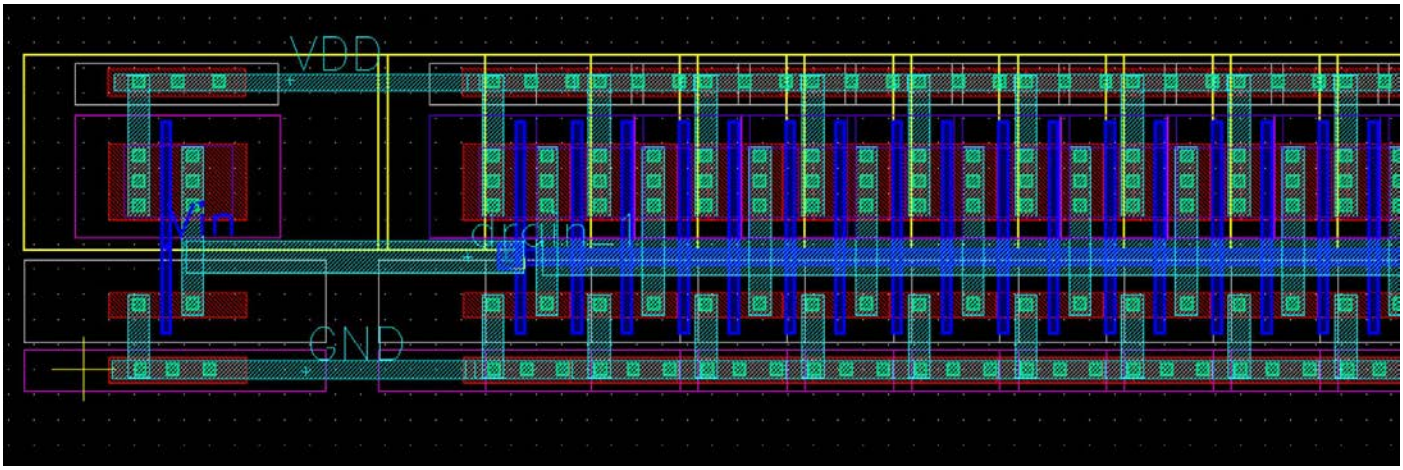


Fig. 5 Part of my layout (version 1)

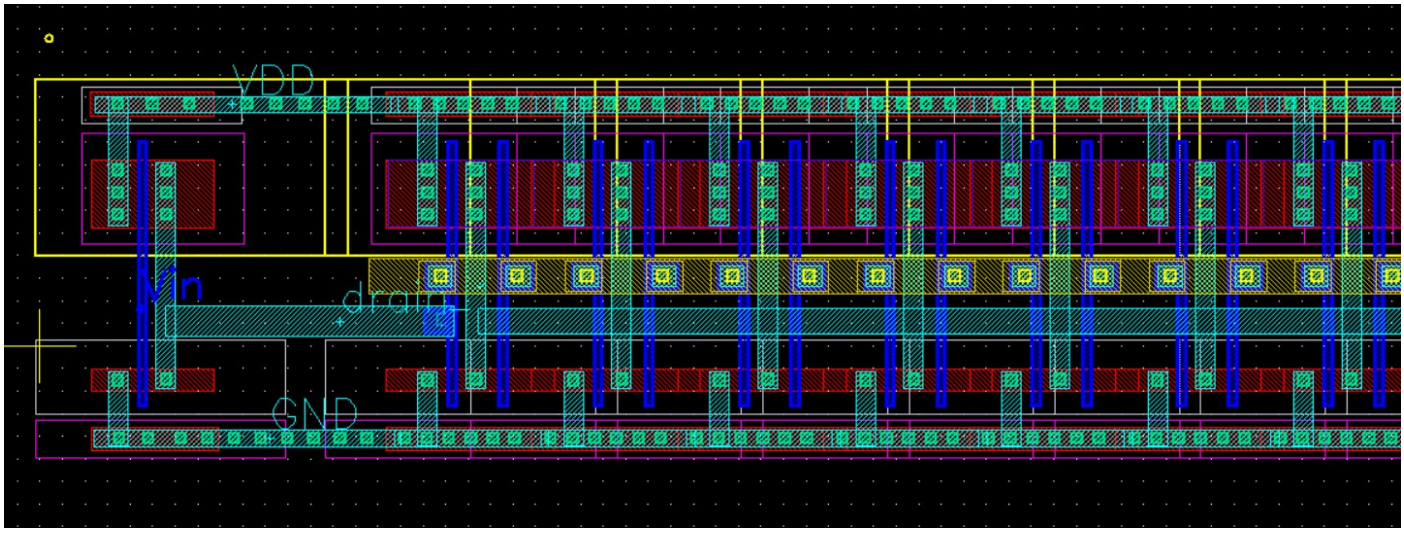


Fig. 6 Part of my layout (version_2)

Layout consideration: 我總共畫了 2 種 layout，兩個版本主要差在 gate 之間的連接方式。Fig. 5 是使用 polysilicon 連接 gate，Fig. 6 是使用 Metal 2 連接 gate。由於 Polysilicon 的電阻太大，所以當訊號在這上面傳遞得時候，遞減的很快速，會產生大的 delay，尤其第 3 級要 1400 多個 unit inverter 的時候，這種情形更嚴重。因此我換使用 Fig. 6 的畫法，使用 Metal 2 連接 gate，因為 Metal 2 相較於 polysilicon 的電阻小很多，可以有效增加訊號的傳遞的速度。另外就是把 contact 盡量打滿讓電盡量快速的流到 diffusion region 的每個地方。還有再畫 layout 的時候是將相鄰 MOS 的 source 或 drain 共用，可以降低面積，因此降低寄生電容。

For the following problem, I used Fig. 6 layout to measure!

Propagation delays for both the rising and falling inputs as well as the power consumption:

Pre-layout simulation:

Delay:

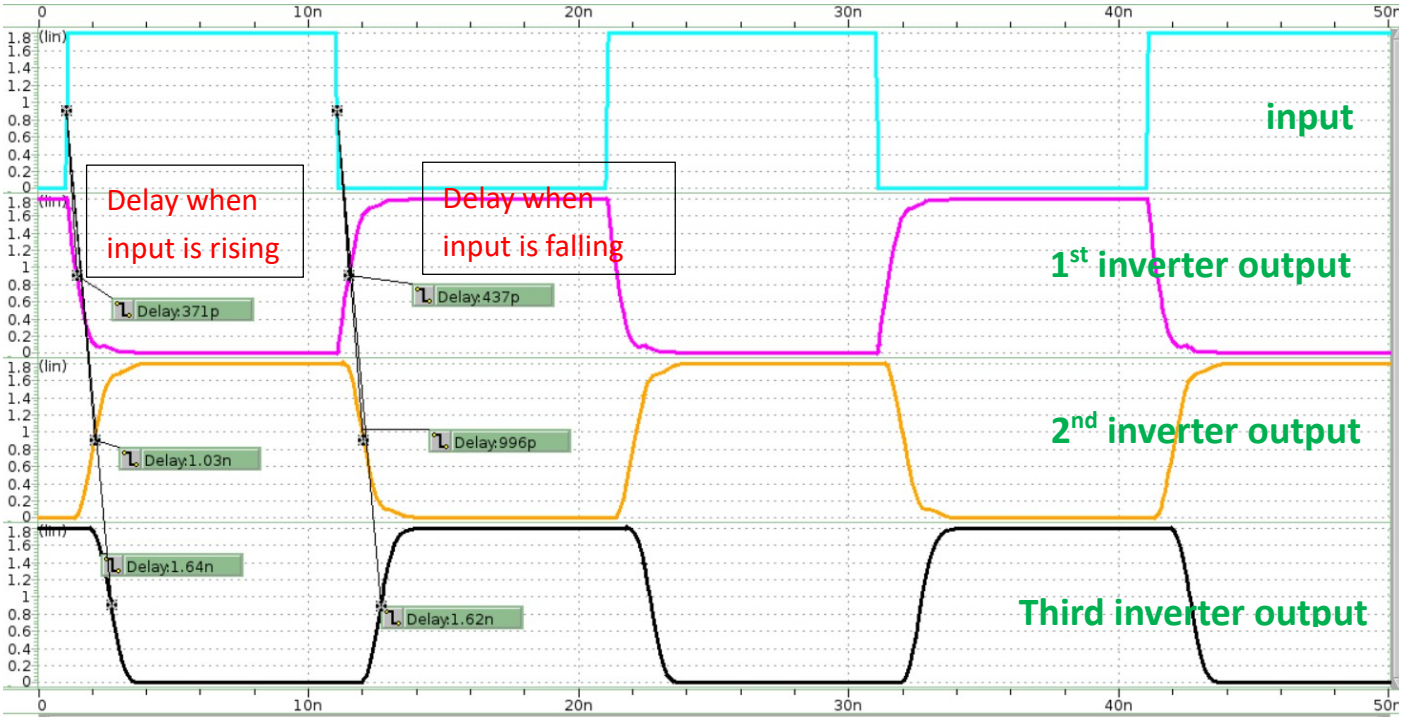


Fig. 7 Delay simulation for each node before post-simulation

Power:

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
power=  35.4541m  from= 500.0000p     to=  20.5000n
```

Fig. 8 Power simulation before post-simulation

After post-layout simulation:

Delay:

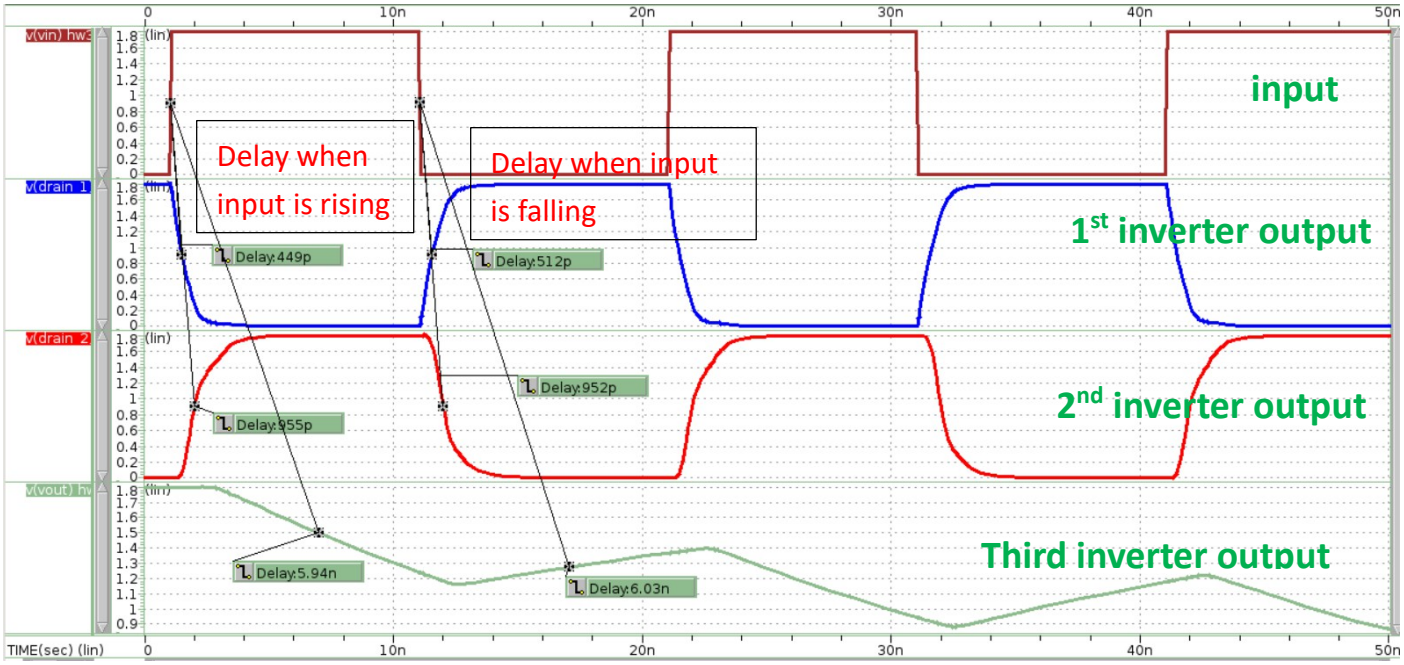


Fig. 9 Delay simulation for each node before post-simulation

Power:

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
power=  13.9138m   from= 500.0000p     to=  20.5000n
```

Fig. 10 Power simulation after post-simulation

Discussion:

Delay:

因為在 layout 中為了將 gate 用 Metal2 連接起來，使得 gate 之間不能靠得太近(polysilicon 上的 via,metal1, metal2 之間有最短距離限制)，所以 gate 之間距離必須拉開因此增加了 diffusion region 的面積，造成 parasitic capacitor 增加。另外，每一級並聯那麼多的 unit inverter 用把 gate 跟 drain 連起來的 metal2 跟 metal1 本身帶有電阻會造成訊號傳遞的 delay，這是原本 pre-layout simulation 無法考慮的。又因為第 3 級連接了 1400 多個 unit inverter，所以產生更嚴重的 delay。因此

對於最後 200pF 的外接電容無法完全的充放電。

Power:

可以觀察 Fig. 9 最後一級的波形，其實並不會完全的充電及放電，相較於 pre-layout simulation 的完全充放電來說，消耗的 power 會小很多，我認為這是 power 大幅降低的主因。