EE3230 VLSI Design (2019 Fall) HW #3

Due date: 2019/11/29 (Friday) 10am

No plagiarism is allowed!!

1. Please design an inverter chain with odd number of inverters that achieves the shortest propagation delay with the following conditions:

- V_{DD}=1.8 V.
- The size of the first inverter is fixed. $(W/L)_N$=0.5μ/0.18μ, and $(W/L)_P$=1.5μ/0.18μ.
- The inverter chain drives a capacitor load of 10 pF.
- The rise and fall time of the input is 0.1 ns, and the frequency is 50 MHz.

Hint: Estimate or simulate the input capacitance of the first inverter.

a. Explain the hand calculation or analysis you perform to reach this result.
b. Simulate and plot the waveforms for each node, including the input, for 50 ns. Use one row for each waveform. Label the key data points and show the propagation delays for both the rising and falling inputs.

c. Perform hand analysis and estimate the power consumption of this inverter chain.
d. Simulate the power consumption of this inverter chain. What is the difference between the simulation result and the calculation in question c? Explain why they are different with reasons as clear as possible.

2. Please design an inverter chain with either even or odd number of inverters with the following conditions:

- V_{DD}=1.8 V.
- The size of the first inverter is fixed. $(W/L)_N$=0.5μ/0.18μ, and $(W/L)_P$=1.5μ/0.18μ.
- The inverter chain drives a capacitor load of **200 pF**.
- The rise and fall time of the input is 0.1 ns, and the frequency is 50 MHz.

a. Perform hand analysis and estimate the power consumption vs. the number of stages *n* with *n* = 1~10. (Of course, for each *n*, you'd carefully choose the inverter sizes.)

b. Perform hand analysis and estimate the propagation delay vs. the number of stages *n* with *n* = 1~10. (Of course, for each *n*, you'd carefully choose the inverter sizes.)

c. Plot the product of power consumption and propagation delay for each *n* value vs. *n*. What is the *n* number for the minimum 'power-delay product'? Is it larger or smaller than the number of stages that you designed for the inverter chain in question 1? Can you explain why?

d. For *n* = 3, complete the layout. Run post-layout simulation (R-C-CC extraction) and show the waveforms of each node. Explain your layout considerations. (What did you do to minimize the delay of each stage and the resulting propagation delay?) Measure the propagation delays for both the rising and falling inputs as well as the power consumption. How different are the results compared to previous questions? Explain why they are different with reasons as clear as possible. (Don't just say something like 'layout causes additional parasitics'.)

   Hint: Don't forget to put the 200-pF capacitor load in your simulation!