積體電路 HW2

1. Please design an inverter with $(W/L)_N = 1.8\ \mu m/0.2\ \mu m$.

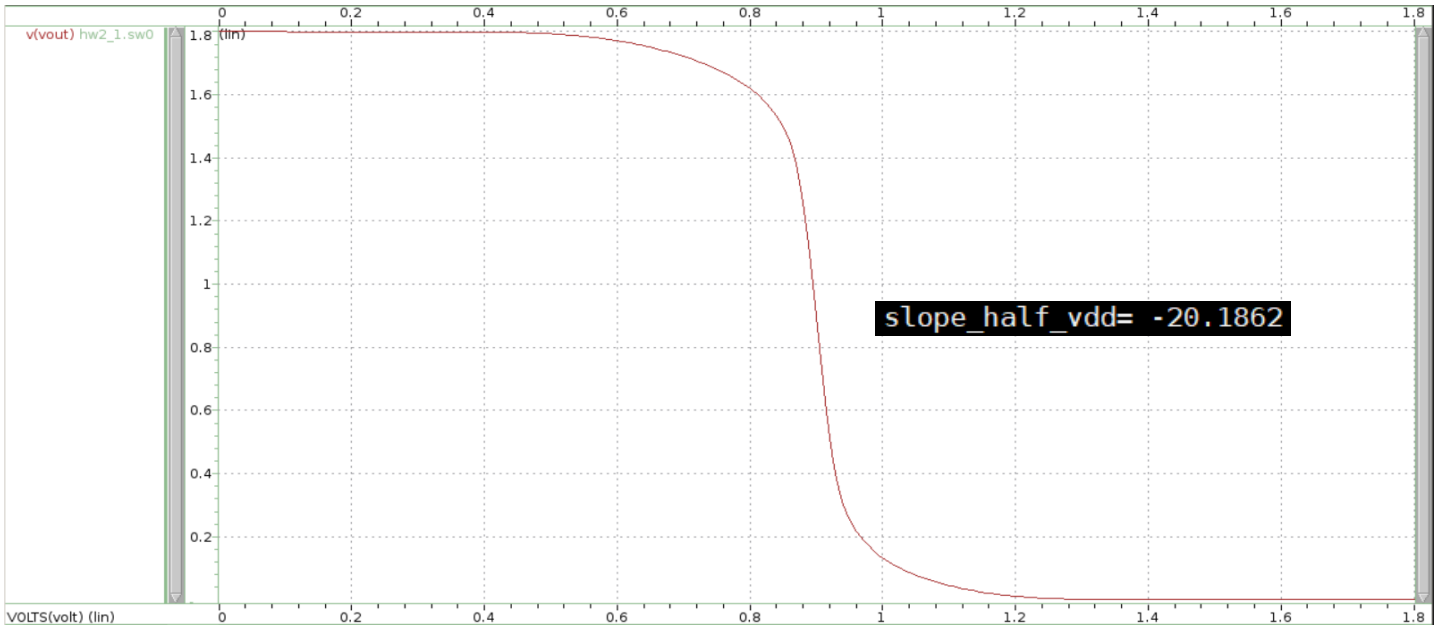
   a. Find and report the PMOS size such that the transition point happens at $V_{out} = 0.5 \cdot V_{DD}$ when V_{in} is also $0.5 \cdot V_{DD}$.

      Ans. (W/L)p = 6.07 um/ 0.2 um

   b. What is the ratio between PMOS and NMOS? Why?

      Ans. The ratio between PMOS and NMOS is (W/L)p/(W/L)n = 6.07 um/ 1.8 um = 3.37。when Vin = Vout = 0.5VDD, NMOS and PMOS are in Saturation region, and Id,n = Id,p. 有很多影響因素，如：μ, Cox, (Vgs-Vth), (1+ λVds)，其中μ的影響較其他因素大，μ_n約是μ_p的3倍。(1+ λVds)的影響大約為1.1倍左右。所以最後 (W/L)p/(W/L)n 的值會落在3附近。另外，Beta ratio約為0.906。

   c. Simulate and plot the DC voltage transfer curve of this inverter as V_{out} vs. V_{in}.



   d. Find the values of V_{IL}, V_{OH}, V_{IH}, and V_{OL} at points with slope of -1.

      V_{IL} = 0.7554 V　　V_{OL} = 92.3 mV

      V_{IH} = 1.035 V　　V_{OH} = 1.68 V

      用measure直接測量slope = -1的value

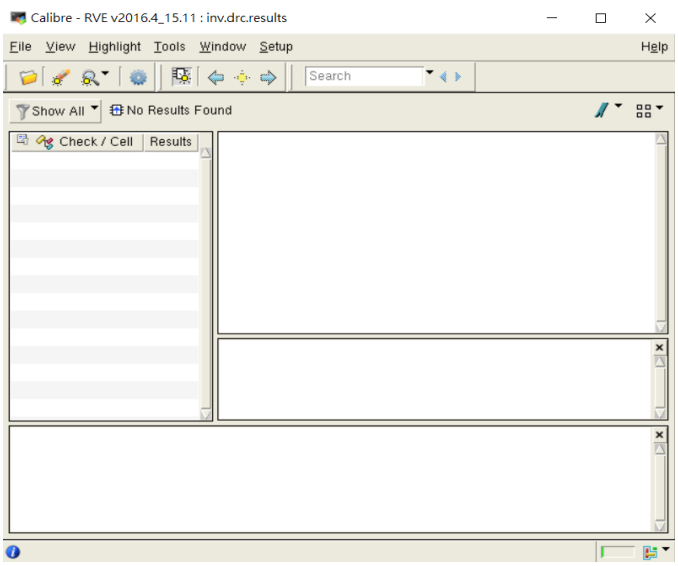
```
.meas DC VIL when deriv('V(VOUT)')=-1 fall=1
.meas DC VOH find V(VOUT) when deriv('V(VOUT)')=-1 fall=1
.meas DC VIH when deriv('V(VOUT)')=-1 rise=1
.meas DC VOL find V(VOUT) when deriv('V(VOUT)')=-1 rise=1
```

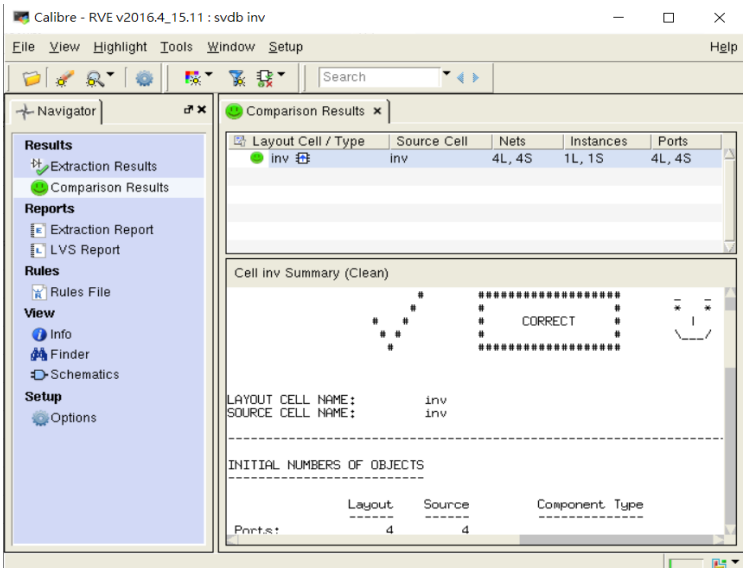
e. What are the noise margins NM_L and NM_H of your design?

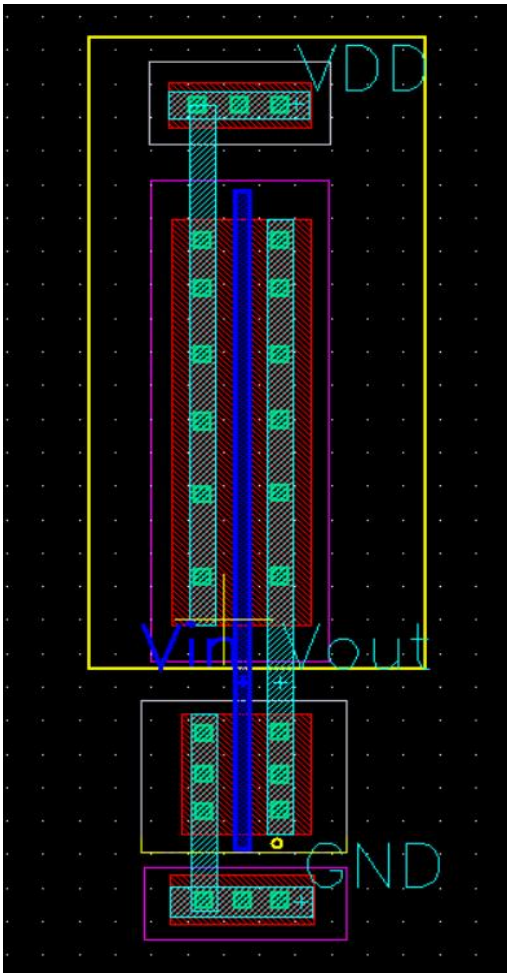
$NM_L = V_{IL} - V_{OL} = 0.7554 - 0.0923 = 0.6631$ V

$NM_H = V_{OH} - V_{IH} = 1.68 - 1.035 = 0.6450$ V

f. Complete the layout (including DRC and LVS). Show figures of your layout with DRC and LVS reports.







2. Please design a NAND3 gate with all 3 NMOS sizes of $5.4\ \mu m/0.2\ \mu m$.

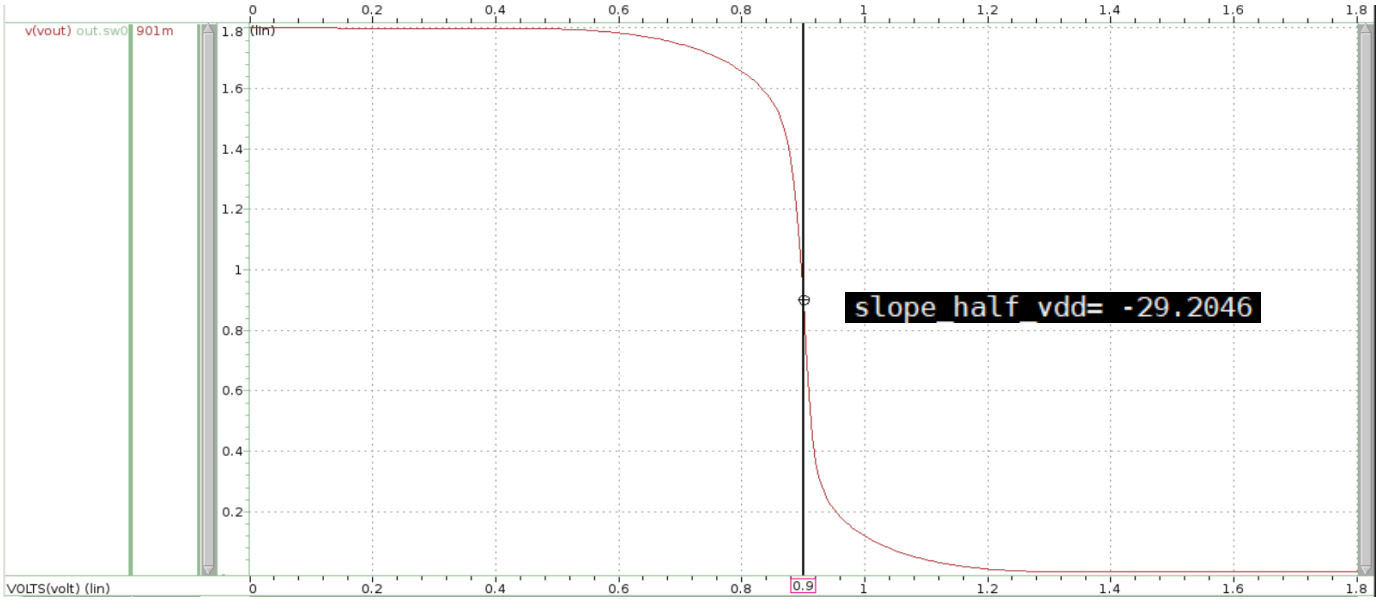
   a. Connect all three inputs together and design the PMOS sizes such that the transition point happens at $V_{out} = 0.5 \cdot V_{DD}$ when V_{in} is $0.5 \cdot V_{DD}$, the same as the inverter in Q1. All three PMOS sizes should be the same.

Ans. All PMOS sizes will be (W/L)p = 2.218 um/ 0.2 um

   b. What is the ratio between PMOS and NMOS? How is it compared to the answer to Q1b and why?

Ans. The ratio between PMOS and NMOS is (W/L)p/(W/L)n = 2.218 um/ 5.4 um = 0.411，ratioQ1/ratioQ2=3.37/0.411=8.2會接近9倍，落在8～9倍之間。將Q1的inverter當作基準，Q2串聯3個NMOS，並且讓Wn從1.8um變成5.4um，藉此維持和Q1一樣的current(等效Q1的NMOS)。上半部並聯三個PMOS，且要維持一樣的current(等效Q1的PMOS)，所以測得的Wp會幾乎是原本Q1的1/3。

   c. Simulate and plot the DC voltage transfer curve of this inverter as V_{out} vs. V_{in} (with all three inputs tied together).



   d. Find the values of V_{IL}, V_{OH}, V_{IH}, and V_{OL} at points with slope of -1.

V_{IL} = 770.115 mV　　V_{OL} = 96.412 mV　　get the values
V_{IH} = 1.0209 V　　V_{OH} = 1.6937 V　　by meas. Method

   e. What are the noise margins NM_L and NM_H of this design? How are they compared to those of the inverter in Q1? Explain reasons for the difference.

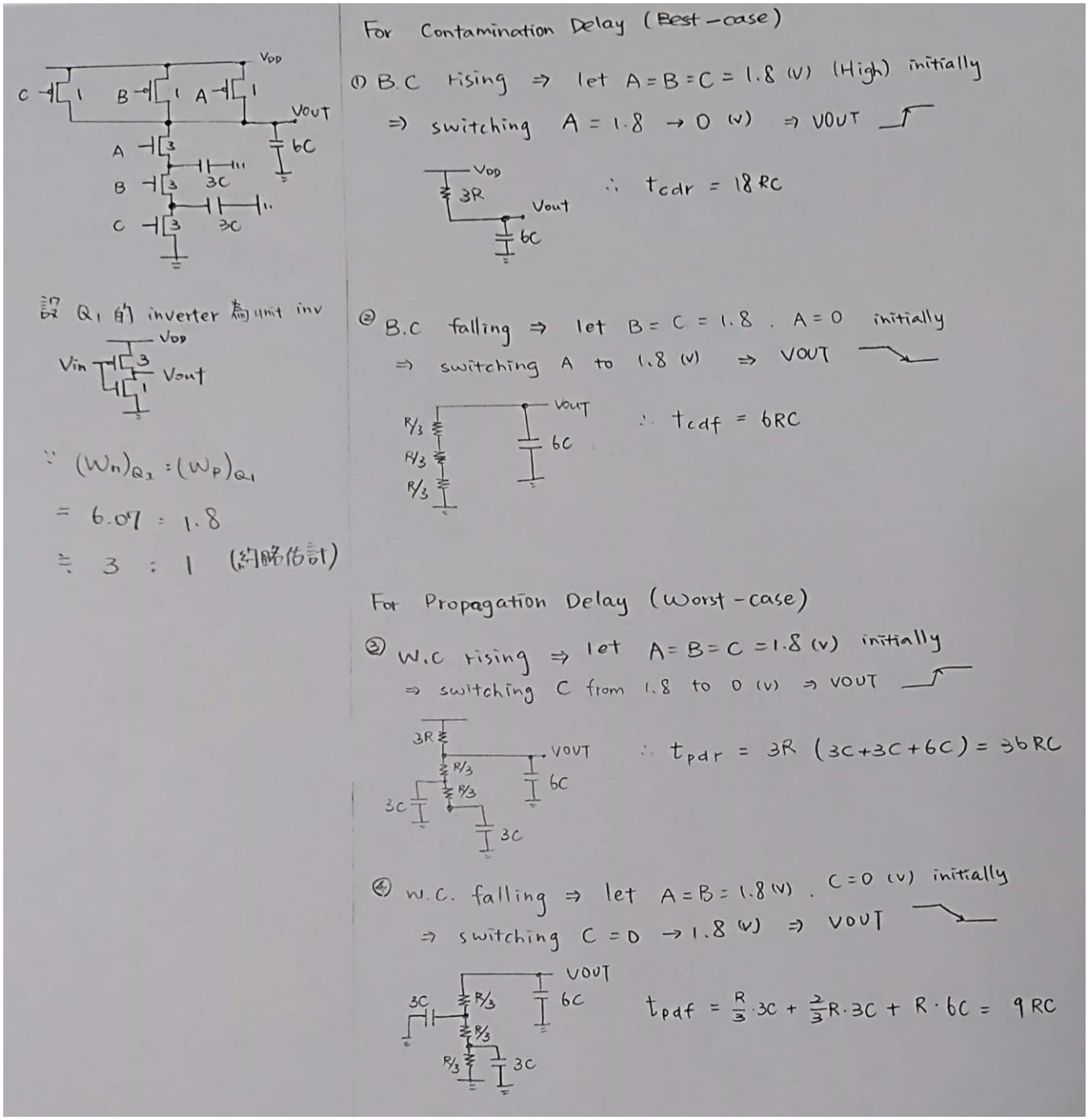
$NM_L = V_{IL} - V_{OL}$ = 0.770115 - 0.096412 = 0.673703 V
$NM_H = V_{OH} - V_{IH}$ = 1.6937 - 1.0209 = 0.6728 V

NM_L, NM_H兩題的值相近。
由Hspice模擬結果，整體來看的等效Q1的NMOS, PMOS的(W/L)都略為上升，使得兩者在Linear範圍變大，Saturation範圍變小，中間部分的|ΔVout/ΔVin|的斜率變大，所以NM_L, NM_H相較Q1仍略微增加。此外Beta ratio和Q1相比，也較為接近1。

3. Simulate the above NAND3 gate with C_{load} of 100 fF at the output. Consider input signals that go between 0 V and VDD with both the rise and fall time of 100 ps. Furthermore, only one of the three inputs is switching at a time.

Process	Temperature	t_{cdr}	t_{cdf}	t_{pdr}	t_{pdf}
TT	25°C	275ps	86ps	362ps	101ps
FF	–40°C	228ps	65.6ps	297ps	75ps
SS	125°C	555ps	217ns	791ps	280ps
SF	25°C	250ps	164ns	346ps	209ps
FS	25°C	259ps	93.1ps	345ps	111ps

Explanation for Q3_a, Q3_b

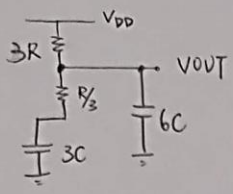


承Explanation for Q3_a, Q3_b

⑤ rising delay for switching B

let A = B = C = 1.8 at first

⇒ B = 1.8 → 0 ⇒ VOUT ↑

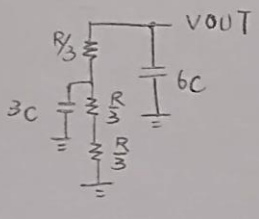


$\tau = 3R \cdot 9C = 27RC$

⑥ falling delay for switching B

let A = C = 1.8 , B = 0 at first

⇒ B = 0 → 1.8 (V) ⇒ VOUT ↓



$\tau = \frac{2}{3}R \cdot 3C + R \cdot 6C = 8RC$

由①.③.⑤知 rising delay

$36RC > 27RC > 18RC$

由②.④.⑥知 falling delay

$9RC > 8RC > 6RC$

所以推論得：

Contamination Delays 為 ① & ②

∵ 經過 less capacitors (1個)

Propagation Delays 為 ③ & ④

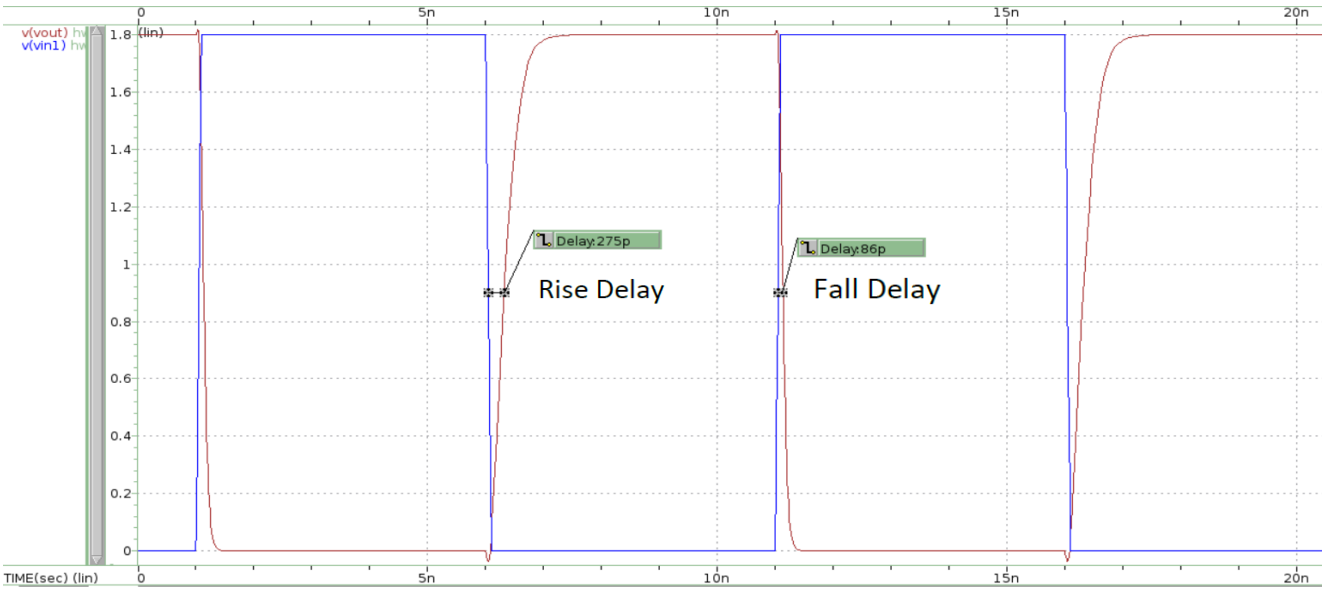
∵ 經過 more capacitors (3個)

In worst case rising, more capacitors need to be charged.
In worst case falling, more capacitors need to be discharged.

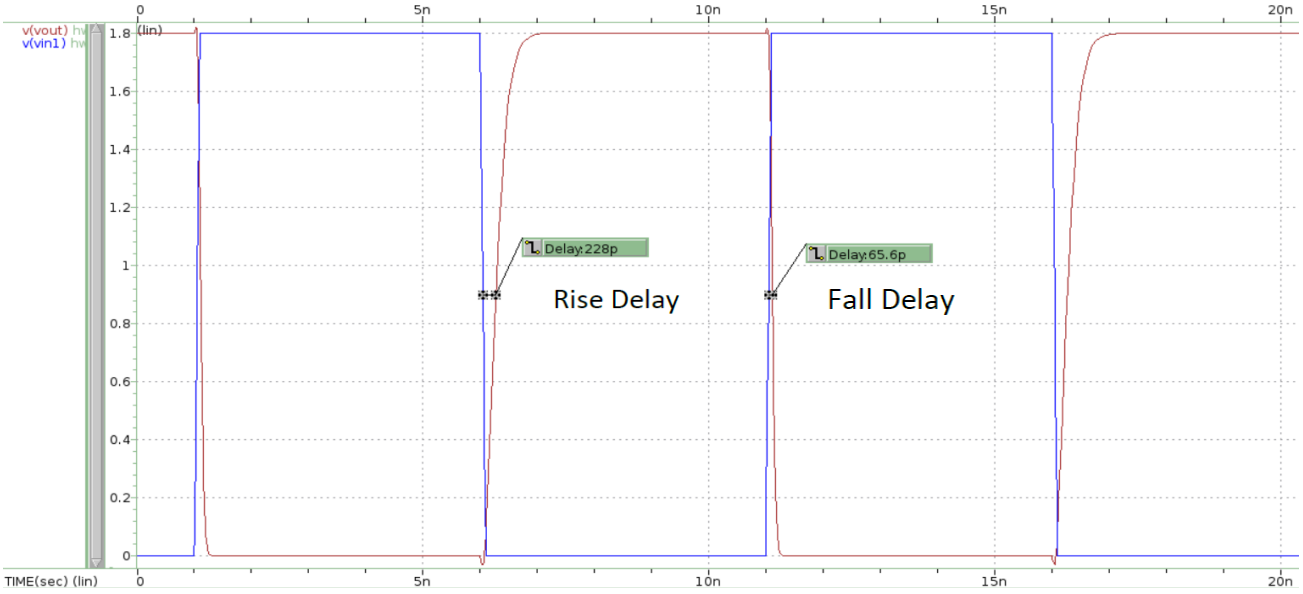
In best case rising, less capacitors need to be charged.
In best case falling, less capacitors need to be discharged.

a. Simulate the contamination delays for both rising and falling output. For both rising and falling cases, explain the input pattern that results in this shortest delay.

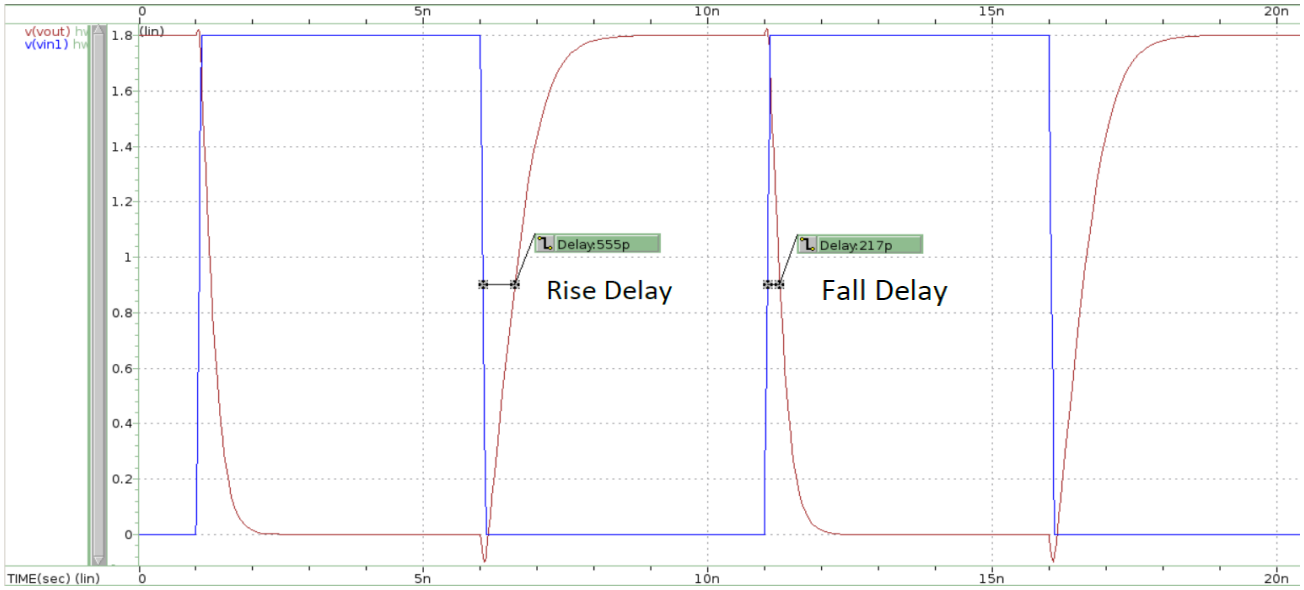
TT 25℃



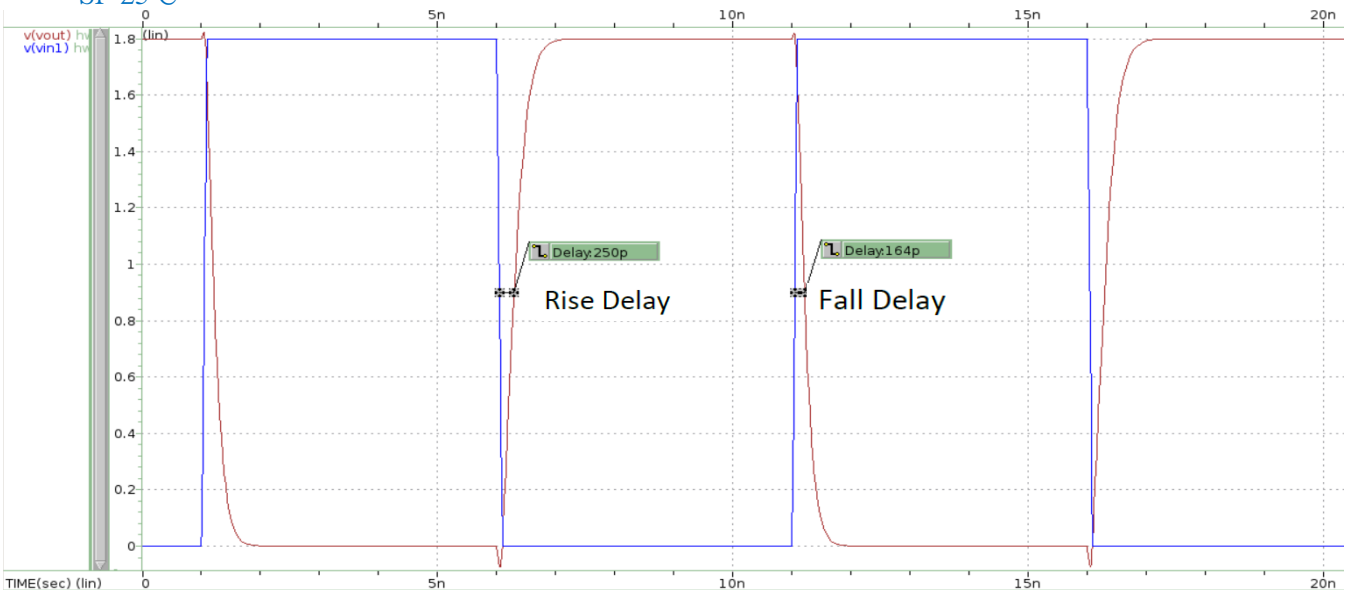
FF -40℃



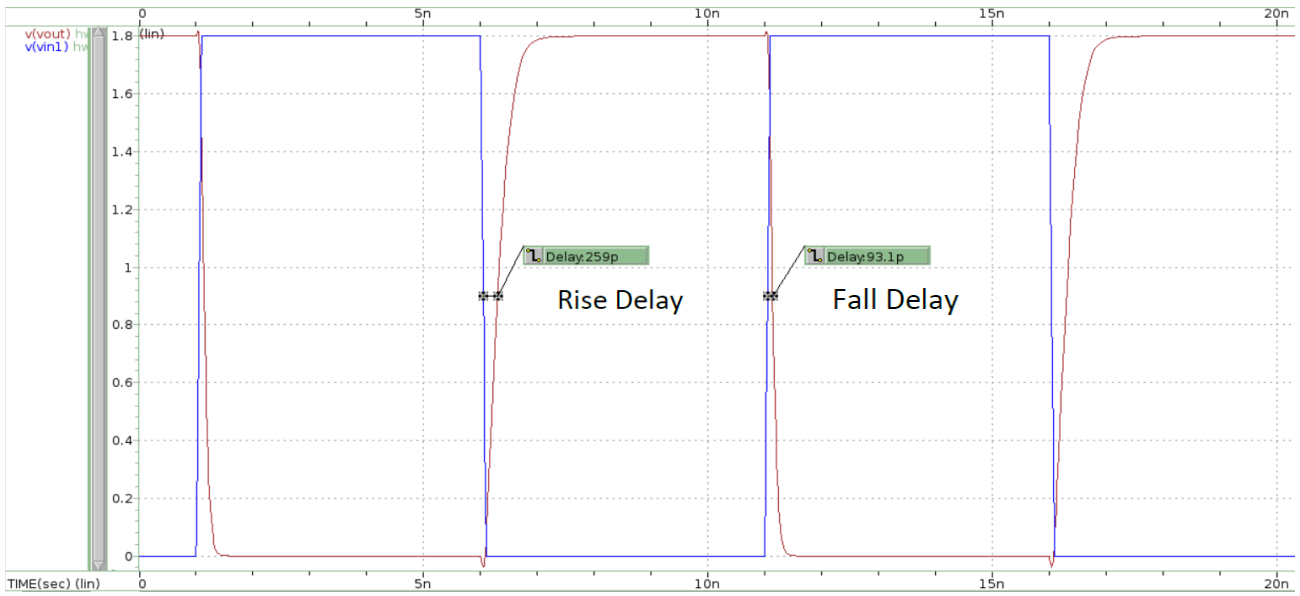
SS 125℃



SF 25℃



FS 25℃



nand3.sp for tcdr and tcdf

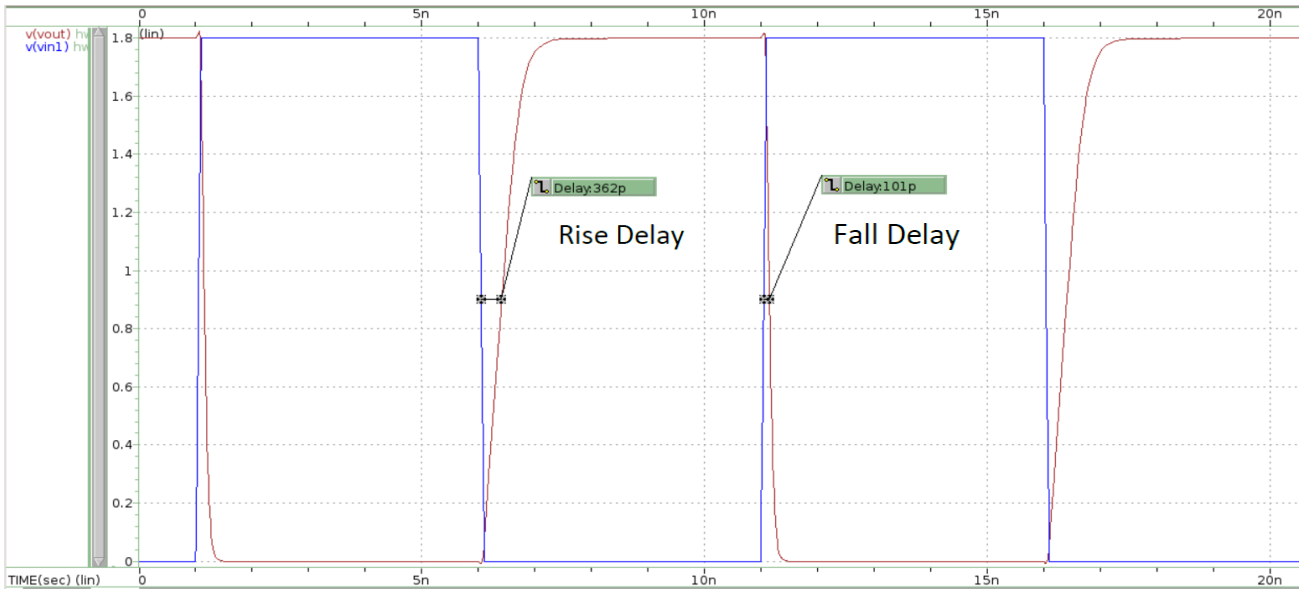
```
********************************************************************************
* auCdl Netlist:
*
* Library Name:  HW2_3
* Top Cell Name: NAND3
* View Name:     schematic
* Netlisted on:  Oct 17 23:44:57 2019
********************************************************************************

*.BIPOLAR
*.RESI = 2000
*.RESVAL
*.CAPVAL
*.DIOPERI
*.DIOAREA
*.EQUATION
*.SCALE METER
*.MEGA
.PARAM width = 0.25u



********************************************************************************
* Library Name: HW2_3
* Cell Name:    NAND3
* View Name:    schematic
********************************************************************************

.SUBCKT NAND3 GND VDD VIN VOUT VIN1
*.PININFO GND:I VDD:I VIN:I VOUT:O
MM5 VOUT VIN1 VDD VDD P_18 W='width' L=200.0n m=1
MM4 VOUT VIN VDD VDD P_18 W='width' L=200.0n m=1
MM3 VOUT VIN VDD VDD P_18 W='width' L=200.0n m=1
```

hw2_3.sp for tcdr and tcdf

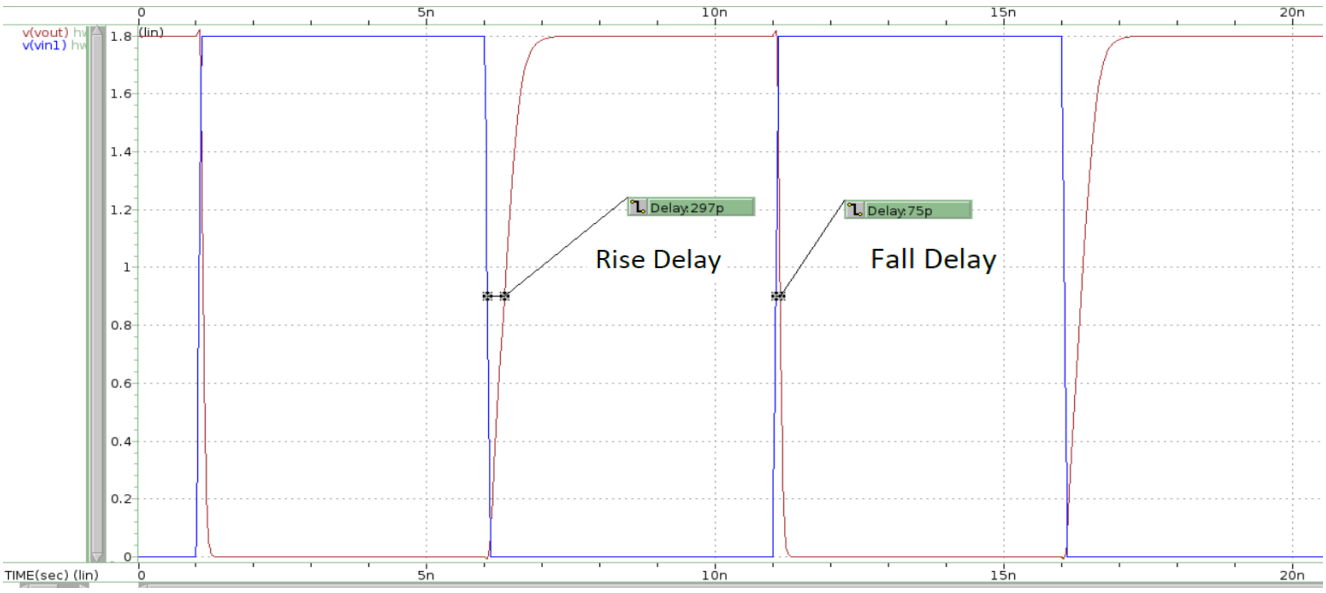
```
** design nand3 ***
.prot
.lib "cic018.l" TT
.unprot
.inc "nand3.sp"
.option post=1
.option accurate=1

.param width = 2.218u
x1 GND VDD VIN VOUT VIN1 nand3
Cout VOUT 0 100f
v1 VDD 0 1.8
v2 GND 0 0
v3 VIN 0 1.8
v4 VIN1 0 PULSE(0 1.8 1ns 100ps 100ps 4900ps 10ns)
.tran 1ns 21ns
.temp 25
.probe V(VOUT)
.op

.alter
.lib 'cic018.l' ff
.temp -40

.alter
.lib 'cic018.l' ss
.temp 125


.alter
.lib 'cic018.l' sf
.temp 25

.alter
.lib 'cic018.l' fs
.temp 25

.end
```

b. Simulate the worst-case propagation delays for both rising and falling output. For both rising and falling cases, explain the input patterns that result in this worst-case propagation delay.

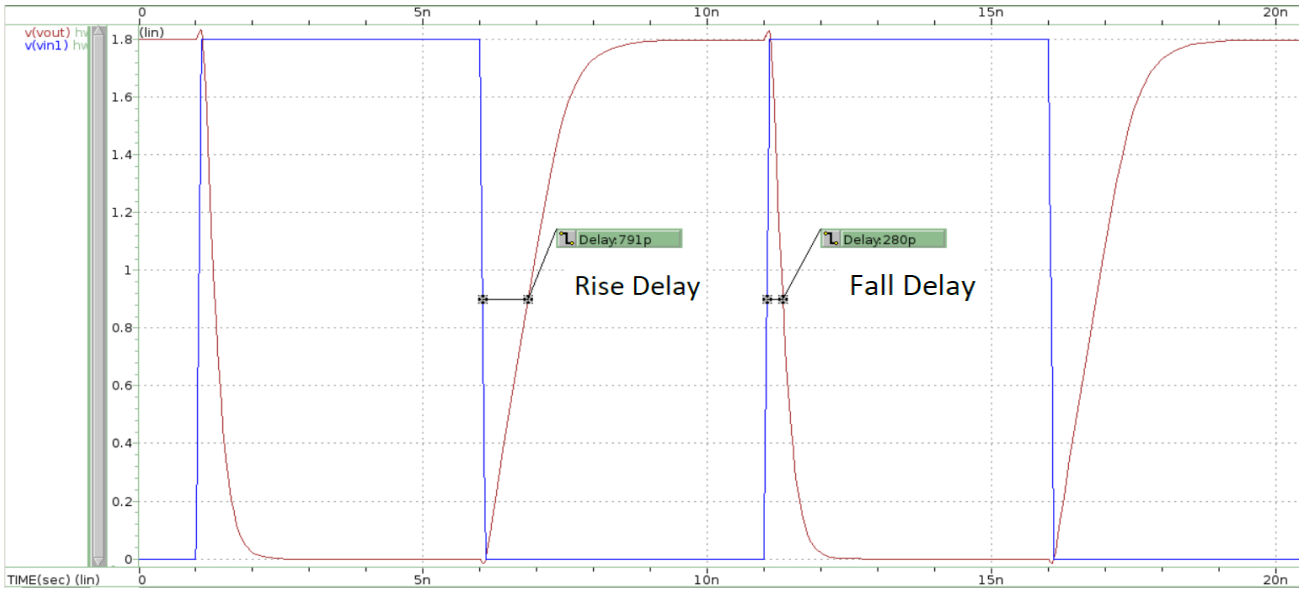
TT 25℃



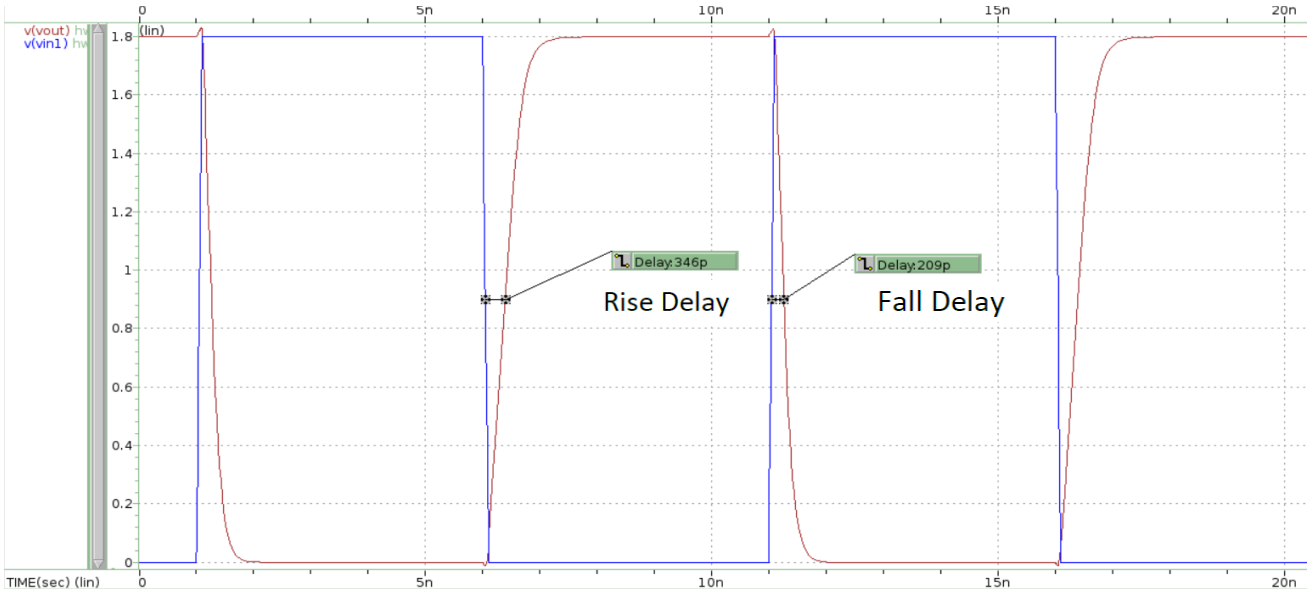
FF -40℃



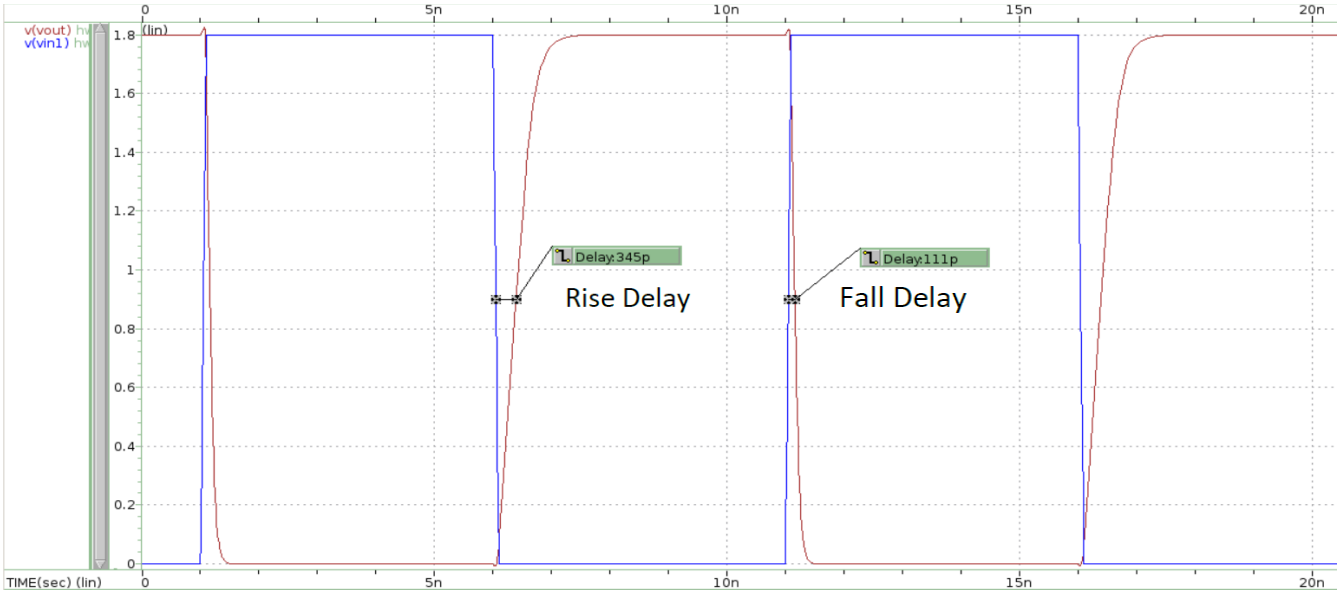
SS 125℃



SF 25℃



FS 25℃



nand3.sp for tpdr and tpdf

```
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* Top Cell Name: NAND3
* View Name:     schematic
* Netlisted on:  Oct 17 23:44:57 2019
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*.RESVAL
*.CAPVAL
*.DIOPERI
*.DIOAREA
*.EQUATION
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*.MEGA
.PARAM width = 0.25u



********************************************************************************
* Library Name: HW2_3
* Cell Name:    NAND3
* View Name:    schematic
********************************************************************************

.SUBCKT NAND3 GND VDD VIN VOUT VIN1
*.PININFO GND:I VDD:I VIN:I VOUT:O
MM5 VOUT VIN VDD VDD P_18 W='width' L=200.0n m=1
MM4 VOUT VIN VDD VDD P_18 W='width' L=200.0n m=1
MM3 VOUT VIN1 VDD VDD P_18 W='width' L=200.0n m=1
MM2 net20 VIN1 GND GND N_18 W=5.4u L=200.0n m=1
MM1 net24 VIN net20 GND N_18 W=5.4u L=200.0n m=1
MM0 VOUT VIN net24 GND N_18 W=5.4u L=200.0n m=1
.ENDS
```

hw2_3.sp for tpdr and tpdf

```
** design nand3 ***
.prot
.lib "cic018.l" TT
.unprot
.inc "nand3.sp"
.option post=1
.option accurate=1

.param width = 2.218u
x1 GND VDD VIN VOUT VIN1 nand3
Cout VOUT 0 100f
v1 VDD 0 1.8
v2 GND 0 0
v3 VIN 0 1.8
v4 VIN1 0 PULSE(0 1.8 1ns 100ps 100ps 4900ps 10ns)
.tran 1ns 21ns
.temp 25
.probe V(VOUT)
.op

.alter
.lib 'cic018.l' ff
.temp -40

.alter
.lib 'cic018.l' ss
.temp 125


.alter
.lib 'cic018.l' sf
.temp 25

.alter
.lib 'cic018.l' fs
.temp 25

.end
```