EE3230 VLSI Design (2019 Fall) HW #2

Due date: 2018/10/30 (Wednesday) 10am

No plagiarism is allowed!!

Run HSpice simulations to answer the following questions.

1. Please design an inverter with $(W/L)_N = 1.8\ \mu m/0.2\ \mu m$.
    a. Find and report the PMOS size such that the transition point happens at $V_{out} = 0.5 \cdot V_{DD}$ when V_{in} is also $0.5 \cdot V_{DD}$. W/L = 6.065u/0.2u
    b. What is the ratio between PMOS and NMOS? Why?
    c. Simulate and plot the DC voltage transfer curve of this inverter as V_{out} vs. V_{in}.
    0.755, 1.68, 1.03, 0.092
    d. Find the values of V_{IL}, V_{OH}, V_{IH}, and V_{OL} at points with slope of -1.
    0.755-0.092=0.663 1.68-1.03=0.65
    e. What are the noise margins NM_L and NM_H of your design?
    f. Complete the layout (including DRC and LVS). Show figures of your layout with DRC and LVS reports.
2. Please design a NAND3 gate with all 3 NMOS sizes of $5.4\ \mu m/0.2\ \mu m$.
    a. Connect all three inputs together and design the PMOS sizes such that the transition point happens at $V_{out} = 0.5 \cdot V_{DD}$ when V_{in} is $0.5 \cdot V_{DD}$, the same as the inverter in Q1. All three PMOS sizes should be the same.
    b. What is the ratio between PMOS and NMOS? How is it compared to the answer to Q1b and why?
    c. Simulate and plot the DC voltage transfer curve of this inverter as V_{out} vs. V_{in} (with all three inputs tied together).
    d. Find the values of V_{IL}, V_{OH}, V_{IH}, and V_{OL} at points with slope of -1.
    e. What are the noise margins NM_L and NM_H of this design? How are they compared to those of the inverter in Q1? Explain reasons for the difference.

3. Simulate the above NAND3 gate with C_{load} of 100 fF at the output. Consider input signals that go between 0 V and VDD with both the rise and fall time of 100 ps. Furthermore, only one of the three inputs is switching at a time.
    a. Simulate the contamination delays for both rising and falling output. For both rising and falling cases, explain the input pattern that results in this shortest delay.
    b. Simulate the worst-case propagation delays for both rising and falling output. For both rising and falling cases, explain the input patterns that result in this worst-case propagation delay.
    c. Repeat the above two questions across the following 5 corners. Show the waveforms with proper markers and complete the following table.
    d. Please also submit the sp netlist along with your report.

Process	Temperature	t_{cdr}	t_{cdf}	t_{pdr}	t_{pdf}
TT	25°C	275.324ps	86.017ps	362.504ps	100.7664ps
FF	–40°C	227.489ps	65.637ps	295.949ps	74.591ps
SS	125°C	553.499ps	213.721ps	786.171ps	263.788ps
SF	25°C	250.21ps	164.09ps	345.681ps	206.971ps
FS	25°C	259.679ps	93.065ps	344.883ps	110.713ps