1.(a)

Y = A' + B' = (AB)' = A NAND B





1.(b)

Y = A'B'C' = (A NOR B)' NOR C

NOT(A NOR B) NOR C



1.(c)

Y = AC+BC+B' = AC+C+B' = B'+C = (BC')' 對此 function 而言,Input A 不影響 Output Y





2.



2-2

Self-Aligned poly-silicon gate :

先做 Gate,再以 Gate 為 Mask 做 Source, Drain

Prons:

- 1. Source and Drain automatically aligned precisely
- 2. Gate is just the size required to cover the channel(Gate is smaller)
- 3. Since Gate is smaller, the device is faster

2-3

Lightly-Doped Drain(LDD) :

Since channel length is shorter, the electrons from the Source are accelerated in the channel and arrive at the Drain with high velocity and cause **hot carrier effect**.

So we lightly doped the drain near the channel compared to the main drain area to reduced hot acrrier effect.

3.(a)

Set NMOS channel length to 1.125u ,such that Vin = Vout = 0.5xVDD = 0.9



3.(b)-1



TT / 25°C

3.(b)-2







SS / 125°C



SF / 25°C

FS / 25°C

NMOS width 1X 如 3.(b) 所示 NMOS width 5X 如下所示

TT / 25°C / 5X

FF / -40°C / 5X

SF / 25°C / 5X

0.6

0.8

0.9 1

FS / 25°C / 5X

		NMOS width 1X	NMOS width 5X	
		Vout	Vout	
Process	Temperature	at Vin=0.5×VDD	at Vin=0.5×VDD	
TT	25°C	903mV	71.9mV	
FF	-40°C	561mV	56.8mV	
SS	125°C	1.54V	89.3mV	
SF	25°C	1.74V	1.2V	
FS	25°C	1.49V	111mV	

4. TT / 25°C 1X / 5X Fall/Rise Delay 如下

TT / 25°C 1X Fall Delay

TT / 25°C 1X Rise Delay

TT / 25°C 5X Rise Delay

其餘如下

		NMOS width 1X		NMOS width 5X	
Process	Temperature				
		Fall Delay	Rise Delay	Fall Delay	Rise Delay
Π	25°C	0.938ns	0.711ns	0.337ns	0.728ns
FF	-40°C	0.696ns	0.613ns	0.271ns	0.63ns
SS	125°C	2.38ns	1.336ns	0.641ns	1.363ns
SF	25°C	1.988ns	0.607ns	0.566ns	0.621ns
FS	25°C	1.061ns	0.661ns	0.370ns	0.681ns