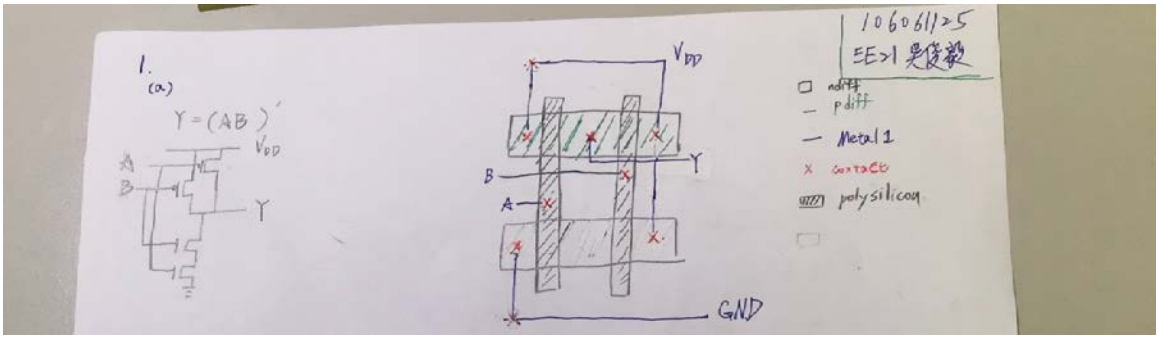
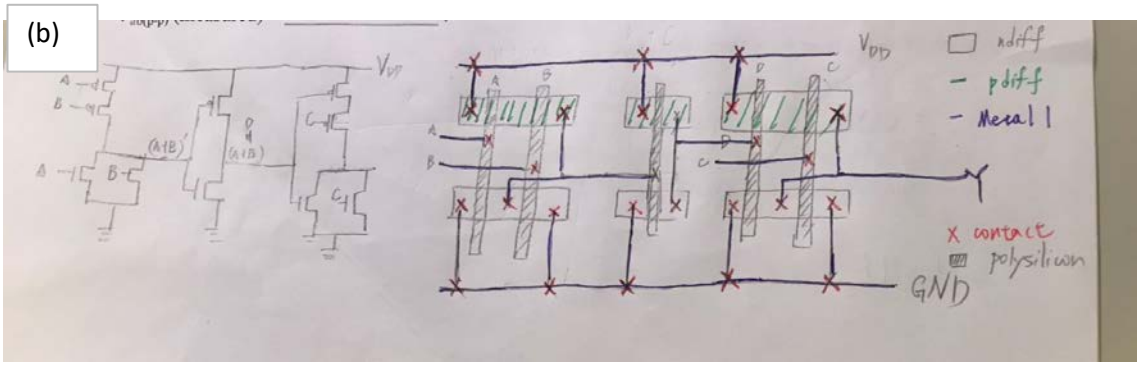
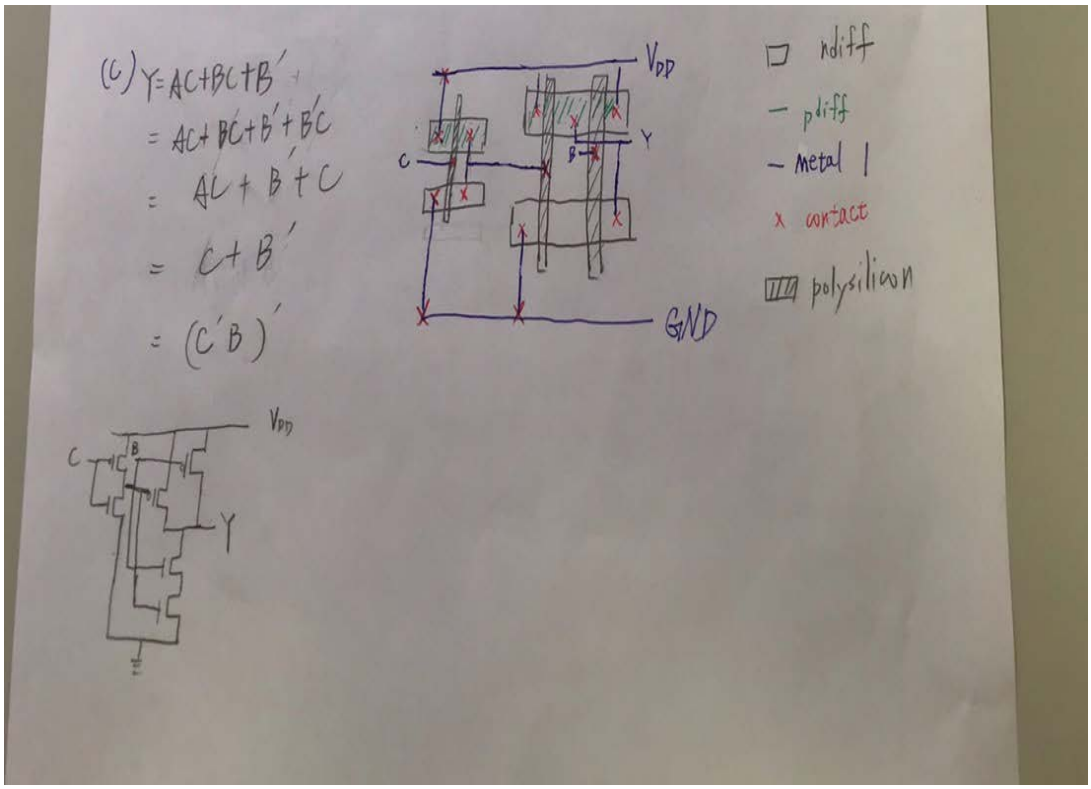
Problem1


1.
(a)
Y=(AB)'
V_{DD}
A
B
Y
B
A
Y
GND
ndiff
pdiff
Metal 1
contact
polysilicon

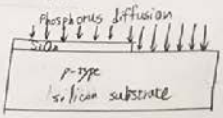

(b)
V_{DD}
A
B
(A+B)'
B
C
V_{DD}
ndiff
pdiff
Metal 1
contact
polysilicon
GND


(c) Y=AC+BC+B'
=AC+BC+B'+BC
=AC+B'+C
=C+B'
=(CB)'
V_{DD}
C
B
Y
V_{DD}
C
B
Y
GND
ndiff
pdiff
Metal 1
contact
polysilicon

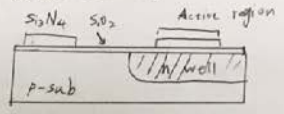
Problem2

2.

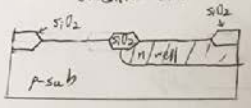
(a) Define n-well diffusion



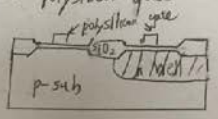
(b) Define active regions (thick oxide)



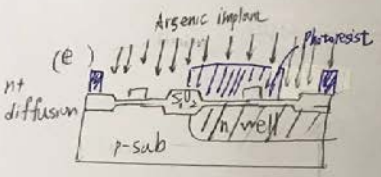
(c) LOCOS oxidation (field oxide)



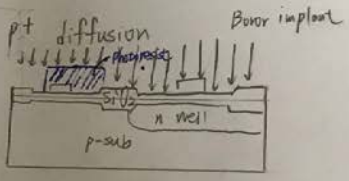
(d) polysilicon gate



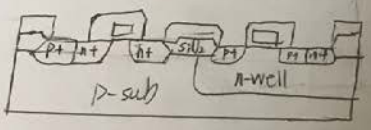
(e)



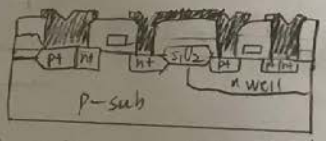
(f) p+ diffusion



(g) Contact holes



(h) Metalization



Self-aligned gate: we put gate first, and use it as a mask for the doping of the source and drain regions, which ensures the gate will slightly overlap the edges of the source and drain

Lightly doped drain: In nmos, when V_{DS} is very large, the electrons arrives at the drain with high velocities and high kinetic energies. It's called hot carrier effect. To overcome it, the doping concentration at drain near the channel is less compared to the main drain area to reduce electric field.

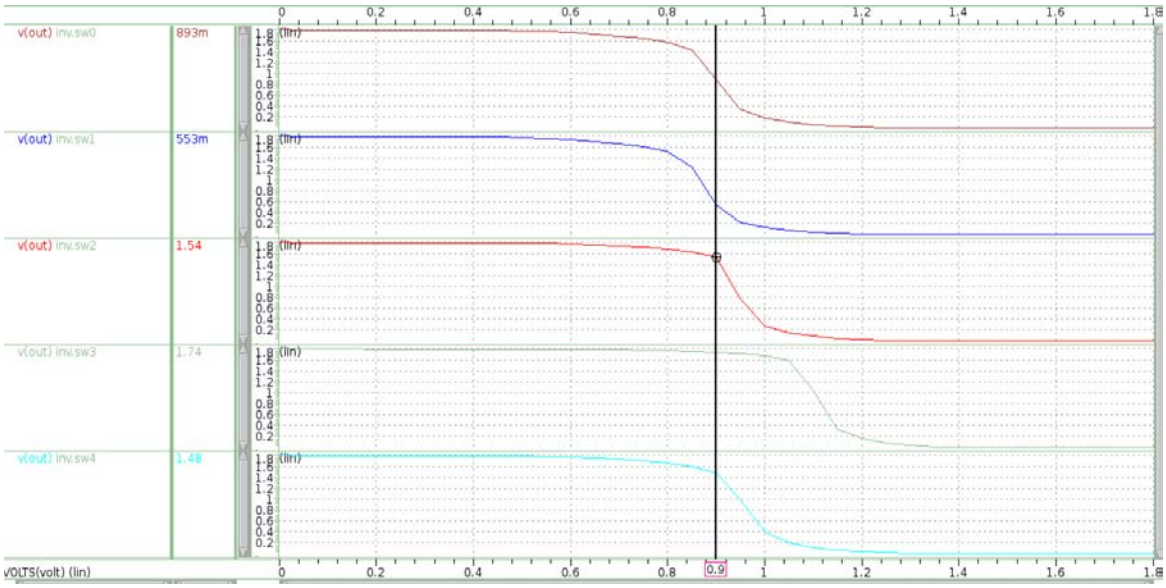
Problem3

3a) Find and report the optimal width for PMOS for a balanced trigger point of inverter at TT corner and 25°C. The meaning of a balanced trigger point is as the following.

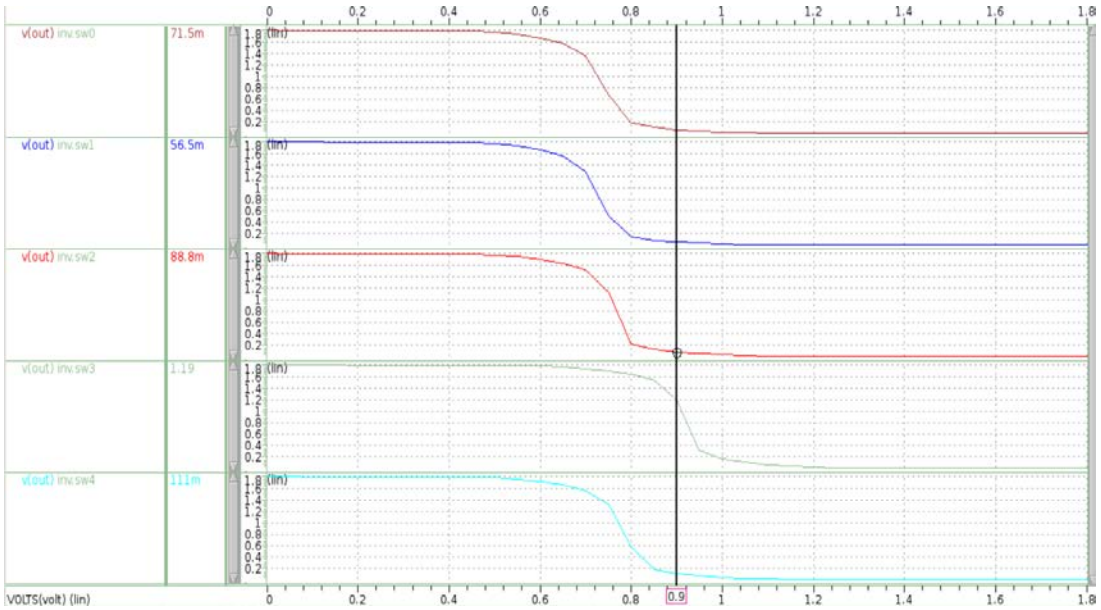
Vin = Vout = 0.5×VDD (That is to say, Vout equals to Vin when Vin is set to half of VDD.)

PMOS width = 1.12um

3b) Perform DC sweep and plot Vout vs. Vin as Vin sweeps from 0 V to VDD with the step of 0.05 V in five different process/temperature corners.



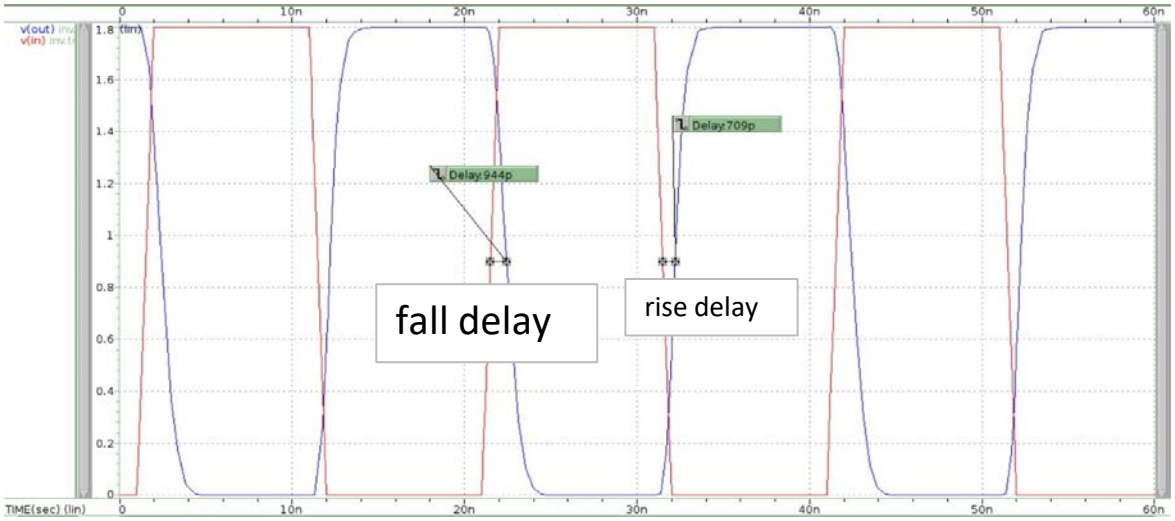
3c) Repeat 3b) with the NMOS width set to 5X of minimum channel width. Then complete the following table. (Report Vout value when Vin is set to half of VDD.)



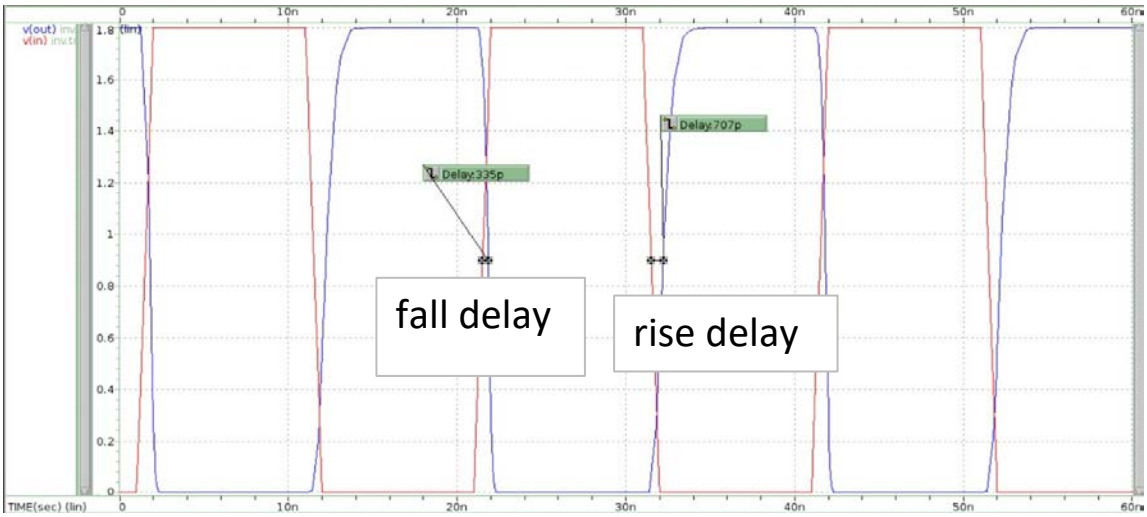
Process	Temperature	NMOS width 1X	NMOS width 5X
		Vout at Vin=0.5×VDD	Vout at Vin=0.5×VDD
TT	25°C	0.893V	0.0715V
FF	–40°C	0.553V	0.056V
SS	125°C	1.54V	0.088V
SF	25°C	1.74V	1.19V
FS	25°C	1.48V	0.111V

Problem4

NMOS width 1X



NMOS width 5x



Process	Temperature	NMOS width 1X		NMOS width 5X	
		Fall Delay	Rise Delay	Fall Delay	Rise Delay
TT	25°C	943.8836ps	708.5825ps	335.2387ps	707.1004ps
FF	–40°C	682.9803ps	596.8875ps	269.8264s	6599.0176ps
SS	125°C	2.3957ns	1.3317ns	633.3349ps	1.3249ns
SF	25°C	1.9824ns	600.0654ps	557.7148ps	617.1248ps
FS	25°C	1.0699ns	657.0862ps	367.5949ps	679.5118ps