

EE3230 VLSI Design (2019 Fall) HW #1

Due date: 2019/10/04 (Friday) 10am

No plagiarism is allowed!!

0. Go through the tutorial document on the class webpage.

1. Use a combination of 2-input CMOS logic gates (in gate-level symbols) to generate the schematics for the following functions from inputs of A, B, and C.

Then complete the stick diagrams for each of the following functions according to the schematics you draw.

(a) $Y = A' + B'$ (15%)

(b) $Y = A'B'C'$ (15%)

(c) $Y = AC + BC + B'$ (15%)

2. Draw the fabrication steps of an inverter (cross section).

Explain the “self-aligned poly-silicon gate” as well as “lightly-doped drain (LDD)”. (35%)

3. Please simulate and analyze a CMOS inverter according to the following conditions using the model provided by TA (CIC018.I).

- * Set the supply voltage to 1.8 V.
- * Set the output load of this inverter to 0.15 pF.
- * Use the minimum channel length for both NMOS and PMOS.
- * Use the minimum channel width for NMOS.

3a) Find and report the optimal width for PMOS for a balanced trigger point of inverter at TT corner and 25°C. The meaning of a balanced trigger point is as the following.

$V_{in} = V_{out} = 0.5 \times V_{DD}$ (That is to say, V_{out} equals to V_{in} when V_{in} is set to half of V_{DD} .)

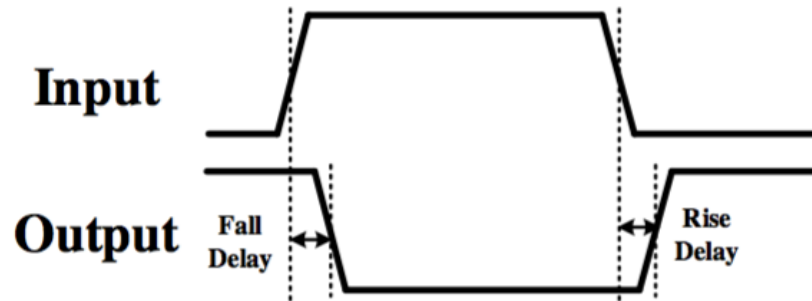
PMOS width = 1.12um

3b) Perform DC sweep and plot V_{out} vs. V_{in} as V_{in} sweeps from 0 V to V_{DD} with the step of 0.05 V in five different process/temperature corners.

3c) Repeat 3b) with the NMOS width set to 5X of minimum channel width. Then complete the following table. (Report V_{out} value when V_{in} is set to half of V_{DD} .)

Process	Temperature	NMOS width 1X	NMOS width 5X
		V_{out} at $V_{in}=0.5 \times V_{DD}$	V_{out} at $V_{in}=0.5 \times V_{DD}$
TT	25°C	0.893V	0.0715V
FF	-40°C	0.553V	0.056V
SS	125°C	1.54V	0.088V
SF	25°C	1.74V	1.19V
FS	25°C	1.48V	0.111V

4. Follow the previous question, run transient simulations for all 10 conditions and measure the input to output delay of the inverter. Set the rise and fall time of the input waveforms to 1 ns.



Attach the simulated waveforms for TT 25°C (with rise and fall time labeled clearly) for both 1X NMOS and 5X NMOS.

Process	Temperature	NMOS width 1X		NMOS width 5X	
		Fall Delay	Rise Delay	Fall Delay	Rise Delay
TT	25°C	943.8836ps	708.5825ps	335.2387ps	707.1004ps
FF	−40°C	682.9803ps	596.8875ps	269.8264s	6599.0176ps
SS	125°C	2.3957ns	1.3317ns	633.3349ps	1.3249ns
SF	25°C	1.9824ns	600.0654ps	557.7148ps	617.1248ps
FS	25°C	1.0699ns	657.0862ps	367.5949ps	679.5118ps