# VLSI_FINAL_PROJECT

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## Block Diagram

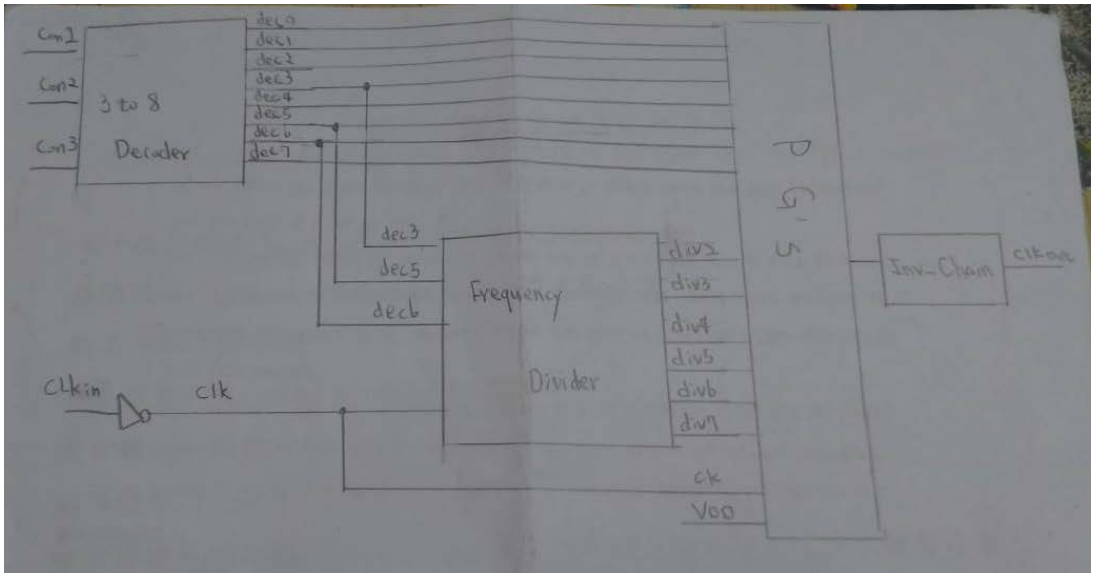



Fig1. The top view of our system design

**Why this architecture?**

This architecture is simple and easy to understand. And we only need to draw some easy logic gates (ex: NAND, NOR, inverter) to implement. Also, it's easy to draw layout.

**How our design operates?**

Our frequency divider produces different kinds of clock frequency and we used decoder results to choose our final clock output.

**Design consideration:**

In layout, we try to put each module close to each other to reduce the layout area. And we try to share area as much as possible. For example, our VDD and VSS almost share with each other almost across all layout. Also we add inverter chain to push 1p output capacitance. And we connect VDD and GND with higher level metal (M5 & M6) to avoid voltage drop due to resistance in the wire.

## Gate level

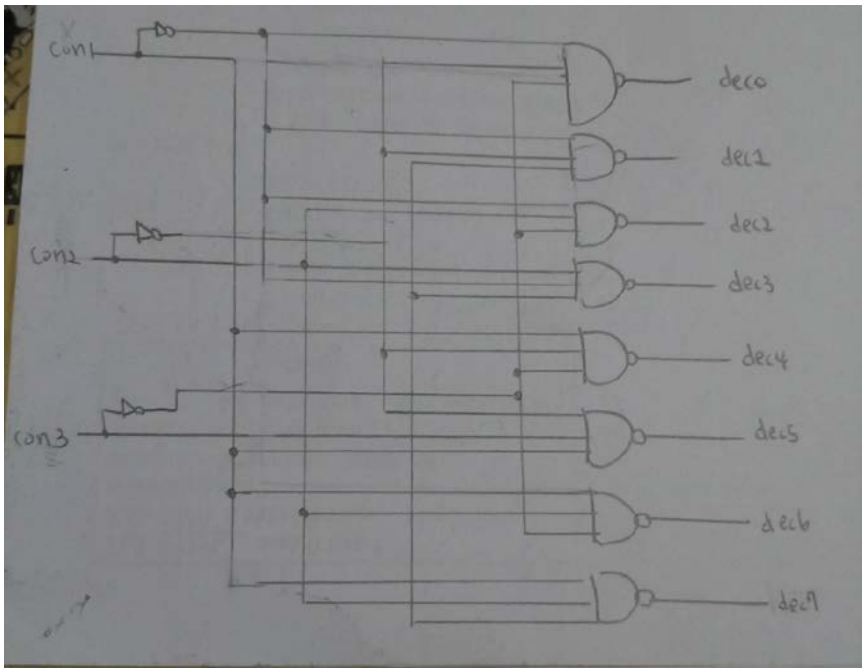



Fig2. 3-8 decoder

| con1 | con2 | con3 | dec0 | dec1 | dec2 | dec3 | dec4 | dec5 | dec6 | dec7 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

The 3-8 decoder we designed is different with the common one.

Only 1 output is 0, others are 1 as we use NAND3 instead of AND3.

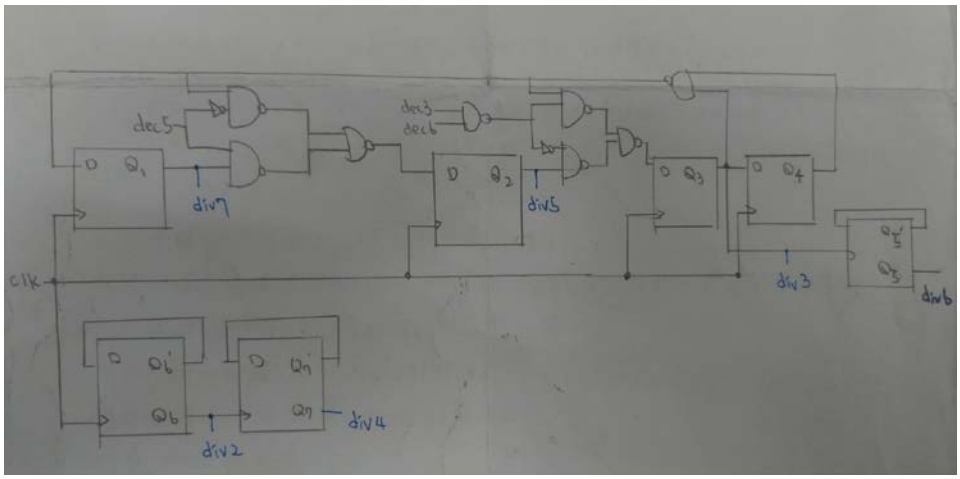
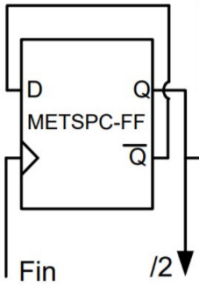
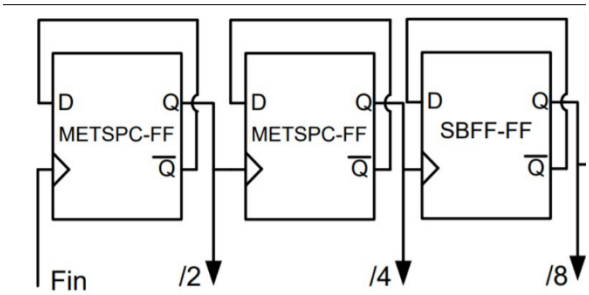



Fig3. D flip-flop. The same as that in HW4

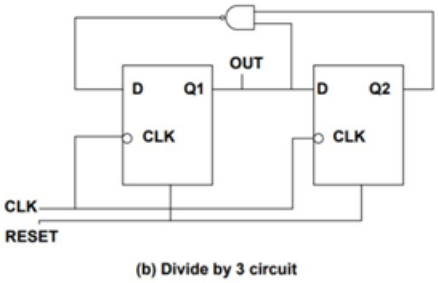



A flip flop with its complementary output $(\bar{Q})$ connect to its own input (D), its output (Q) will have half of its clock frequency.

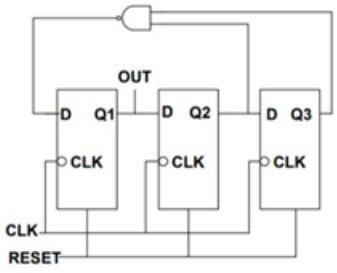
So connect  output to next stage flip flop (also complementary output $(\bar{Q})$ connect to input (D) ).



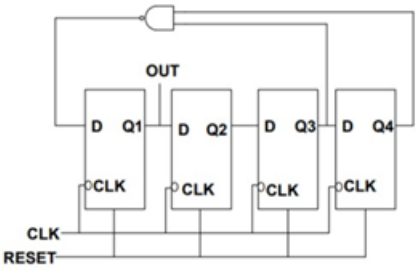
We could produce $\frac{1}{4}$, $\frac{1}{8}$, $\frac{1}{16}$.. of original clock frequency. Thus we use this architecture to produce clock output with $\frac{1}{2}$, $\frac{1}{4}$ and $\frac{1}{6}$ (produce $\frac{1}{3}$ of original frequency then use this method to produce $\frac{1}{6}$ of original frequency).




(b) Divide by 3 circuit




(c) Divide by 5 circuit




(d) Divide by 7 circuit

And we use the circuit above to produce 1/3 (and 1/6), 1/5, 1/7 but without reset function. And because these circuits looks similar to each other. So we try to combine them into a whole circuit by adding extra multiplexer like what we show on Fig. 3 to choose which frequency divide result according to decoder result, which will change along with con1, con2, con3 of course.

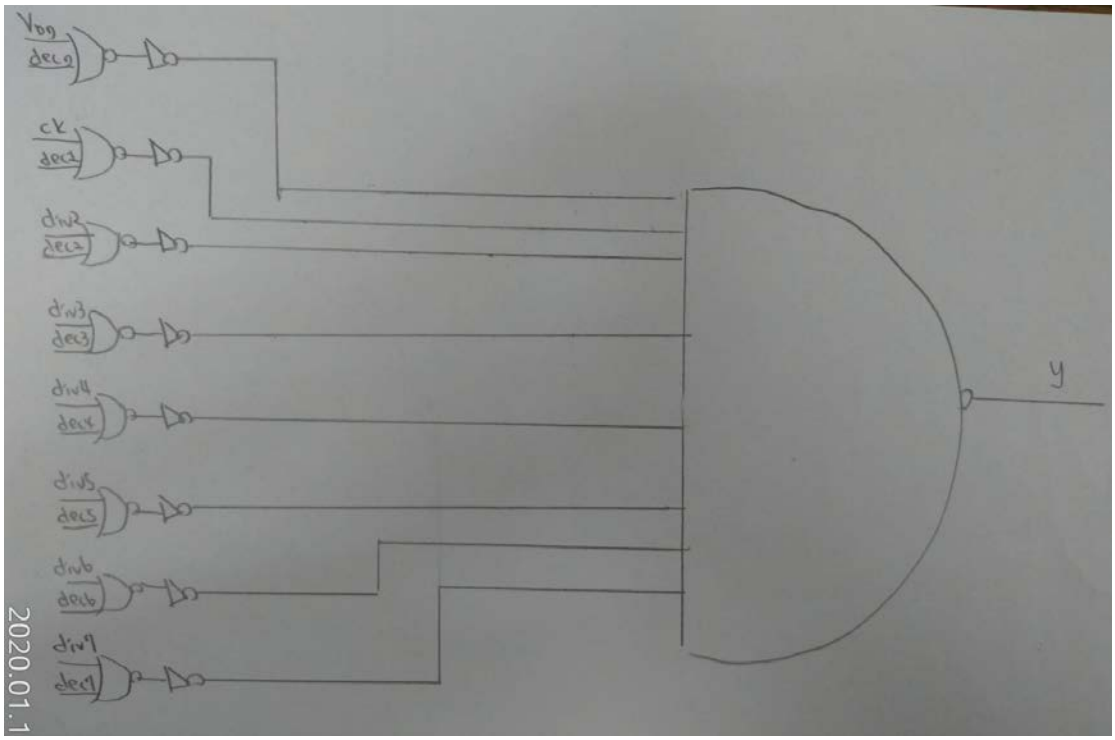



Fig4. PG’s

First NOR2 dec0~7 with VDD、ck、div2~7, then we get 7 zeros and 1 clock signal with bar.

Because only one of dec0~7 is 0 that what we need, other are 1.

(1+div)’ = 0, (0+div)’ = div’

Then we put these 8 results into a unit inverter respectively, we get one clock signal without bar and seven 1’s.

After that we put 8 results into nand8, we get (1.1.1.1.1.1.1.div)’=div’=y

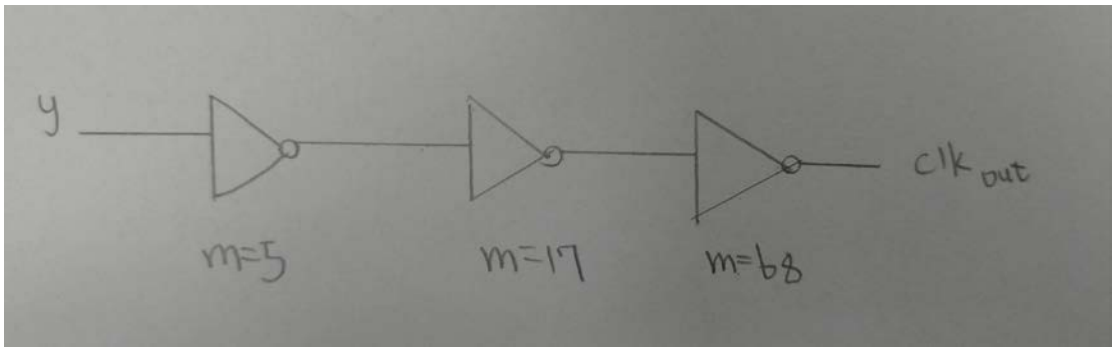



Fig5. Inverter chain

w=1.5um,l=0.18um, m=5、17、68

y is the output result with bar, so we add odd numbers of inverters to get rid of bar and reduce delay as well.

NAND8, we set all input of NAND8 to 0.9V, and recorded capacitance of one of eight inputs, which is 12fF. G (logical effort) of NAND8 = $\frac{11}{4}$. (PMOS: 8, NMOS: 3; unit inverter with NMOS: 1, PMOS: 3) And, parasitic delay of NAND8 is $8 + 3 \times 8 = 32/4 = 8$(output sees 8 PMOS and 1 NMOS. And unit inverter parasitic delay $= 4$, we divided 32 by 4).

F = GBH

= $\frac{11}{4} \times 1 \times \frac{1000}{12}$ = 229.166

$\log_4 F = 3.9$

Adding 1 inverter,

$\hat{f} = \sqrt{229.166} = 15.13$

Total delay = 15.13× $2 + 8 + 1$ = 39.27

Adding 3 inverters,

$\hat{f} = \sqrt[4]{229.166} = 3.89$

Total delay = 3.89× $4 + 8 + 1 \times 3$ = 26.56

Adding 5 inverters,

$\hat{f} = \sqrt[6]{229.166} = 2.47$

Total delay = 2.47× $6 + 8 + 1 \times 5$ = 27.84

After computing n=1、3、5, we found n=3 has the minimum delay. Thus we add 3 more inverters at the output of NAND8. (Note that: from previous homework, an unit inverter with PMOS 1.5u/0.18u and NMOS 0.5u/0.18u has total gate capacitance of 3.78fF as input = 0.9V)

1st inverter size:

GBH = 3.89 => $\frac{11}{4} \times 1 \times \frac{x*3.78}{12} = 3.89$ => x = 4.49. We pick 5 unit inverters.

2nd inverter size:

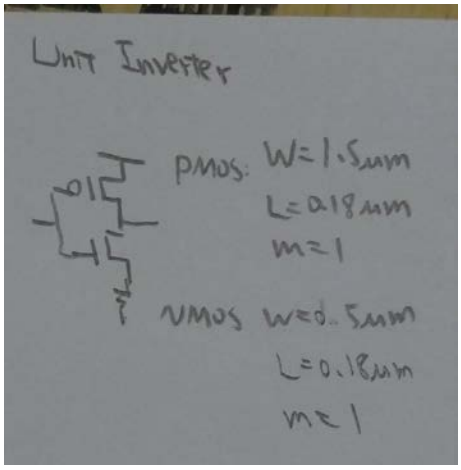
GBH = 3.89 => $\frac{y \times 3.78}{4.49 \times 3.78}$ = 3.89 => y = 17.47. We pick 17 unit inverters.

3rd inverter size

GBH = 3.89 => $\frac{z \times 3.78}{17.47} = 3.89$ => z = 67.99. We pick 68 unit inverters.

## Transistor Level

(All bodies of PMOS/NMOS are connected to VDD/VSS)



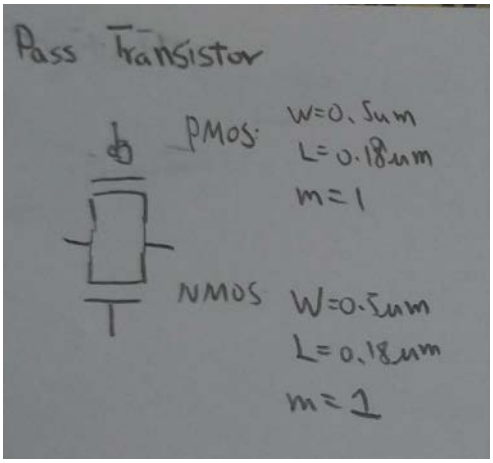




Fig6. Unit inverter 3x/1x

Fig7. Pass Transistor used in D flip-flop

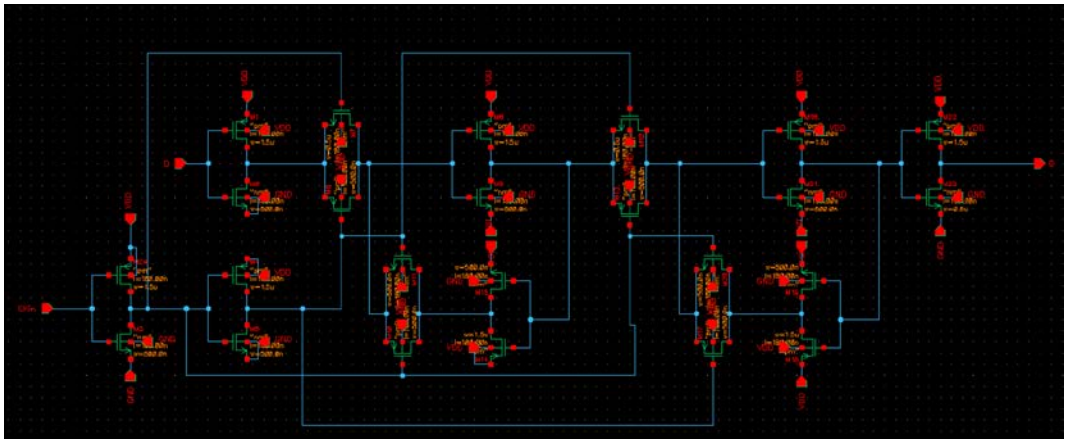


Fig8. Master-Slave Flip-Flop with unit inverters and pass transistors inside.

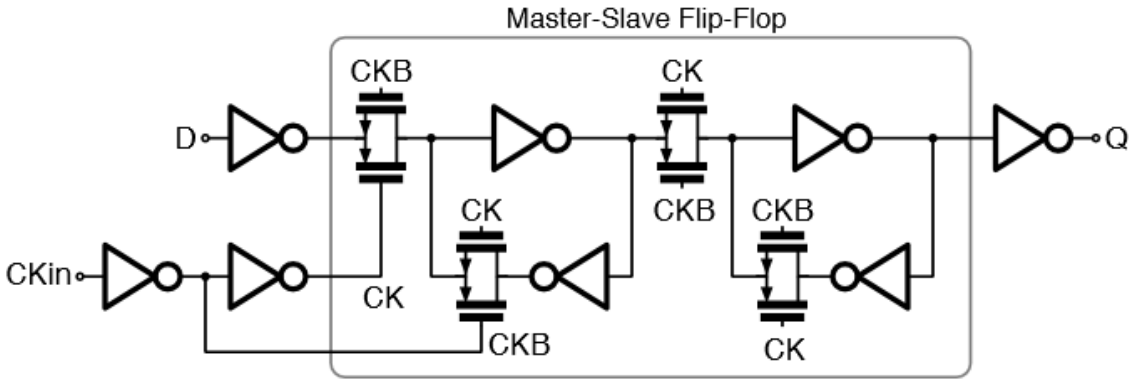



Fig9. View of Master-Slave Flip-Flop

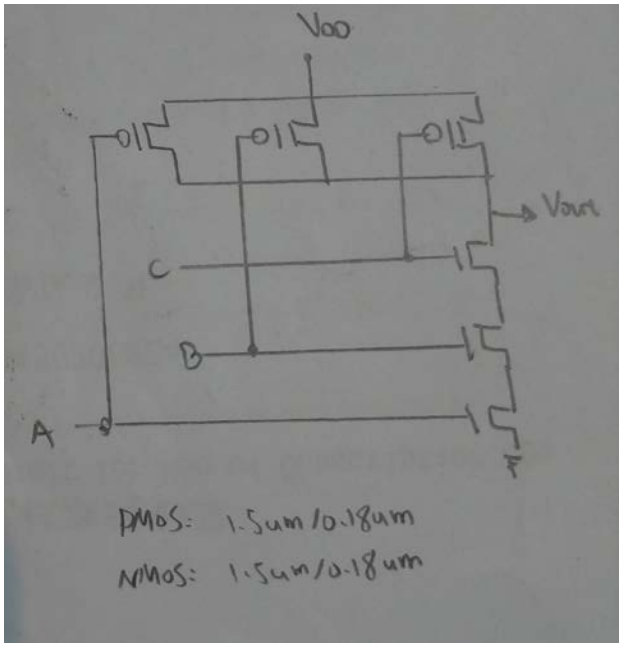



Fig10. NAND3

PMOS/NMOS = 3x/3x, to get equal speed to the unit inverter.

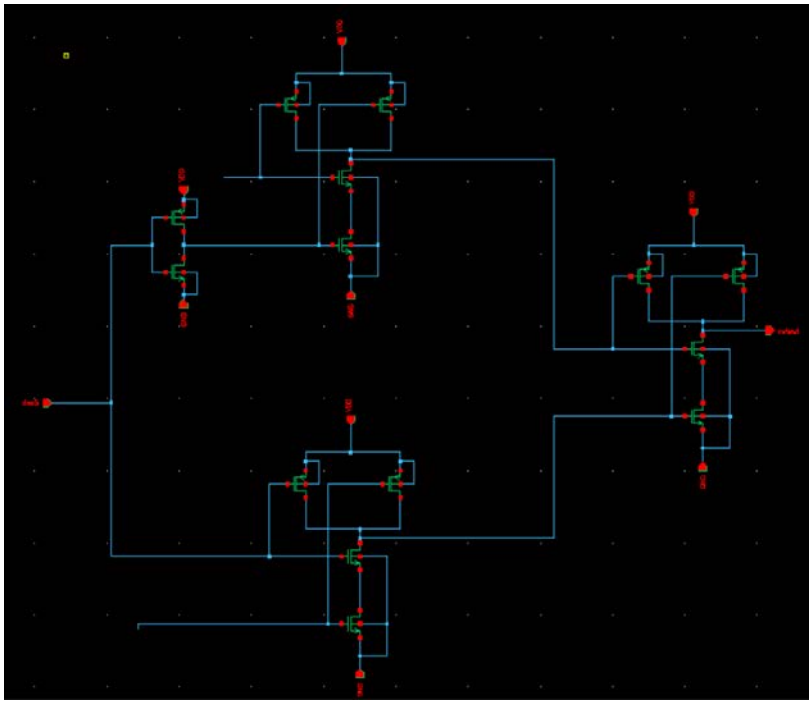


Fig11. Selector with 1 unit inverter and 3 NAND2

NAND2 PMOS/NMOS =3x/2x, to get equal speed to the unit inverter.

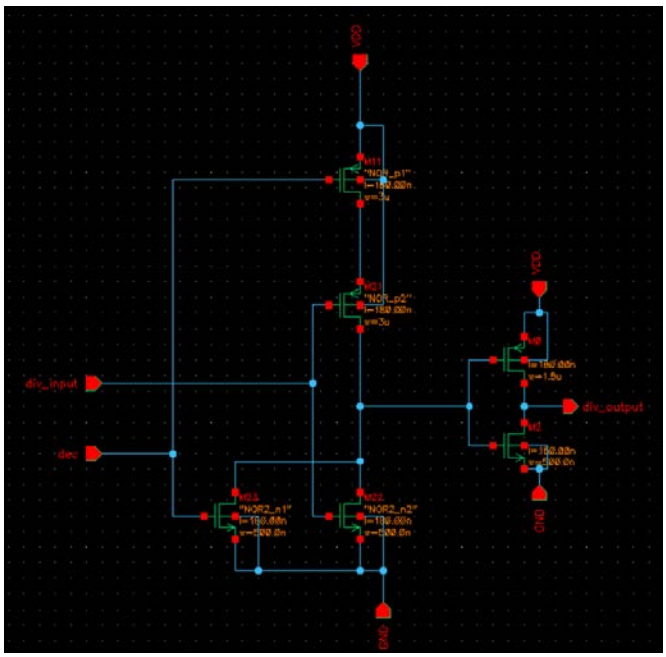



Fig12. NOR2 with an unit inverter

NOR2 PMOS/NMOS =6x/1x, to get equal speed to the unit inverter.

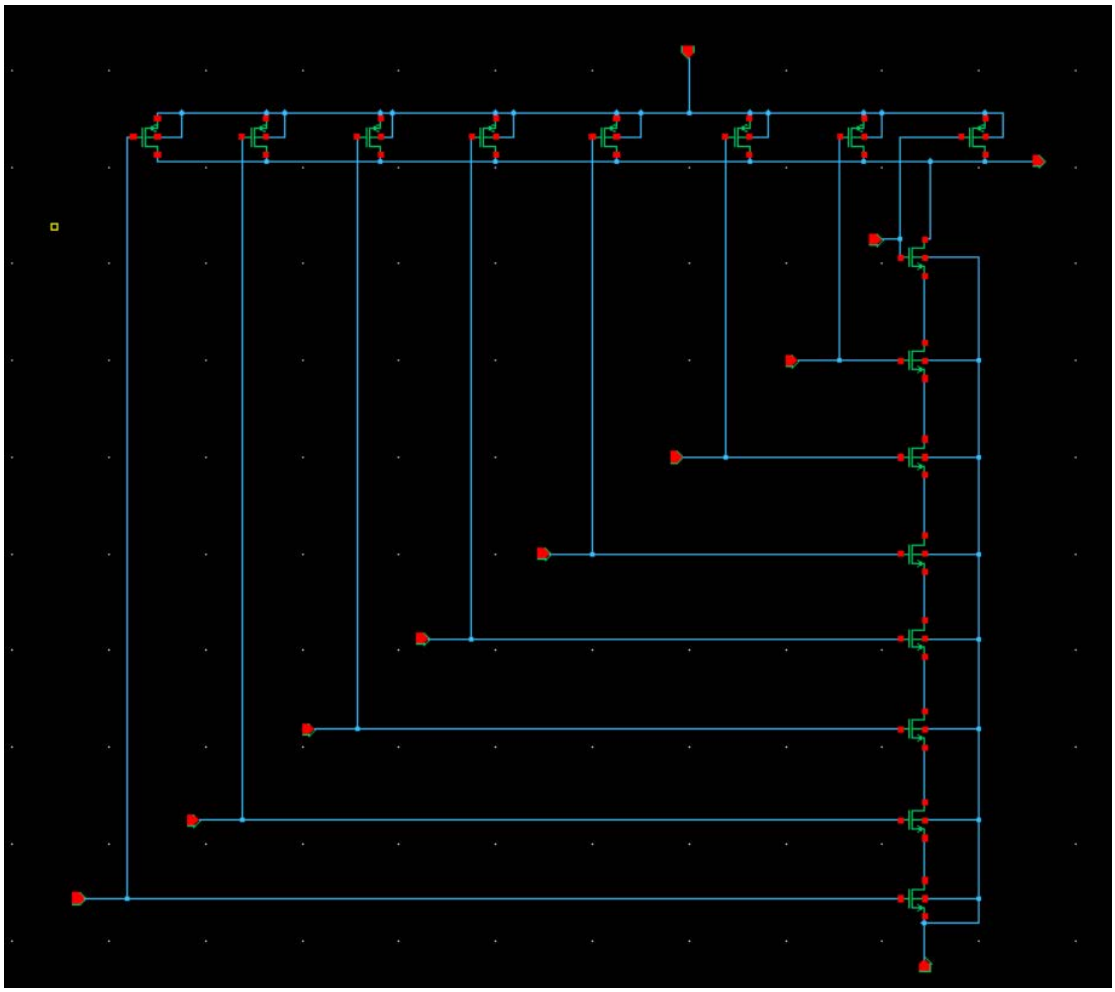


Fig13. NAND8

PMOS/NMOS = 3x/8x, to get equal speed to the unit inverter.

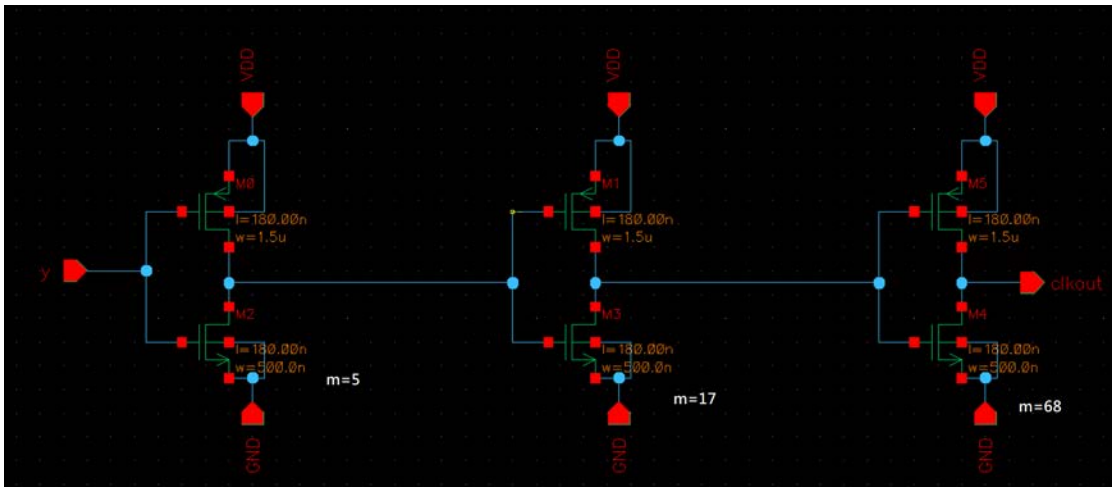
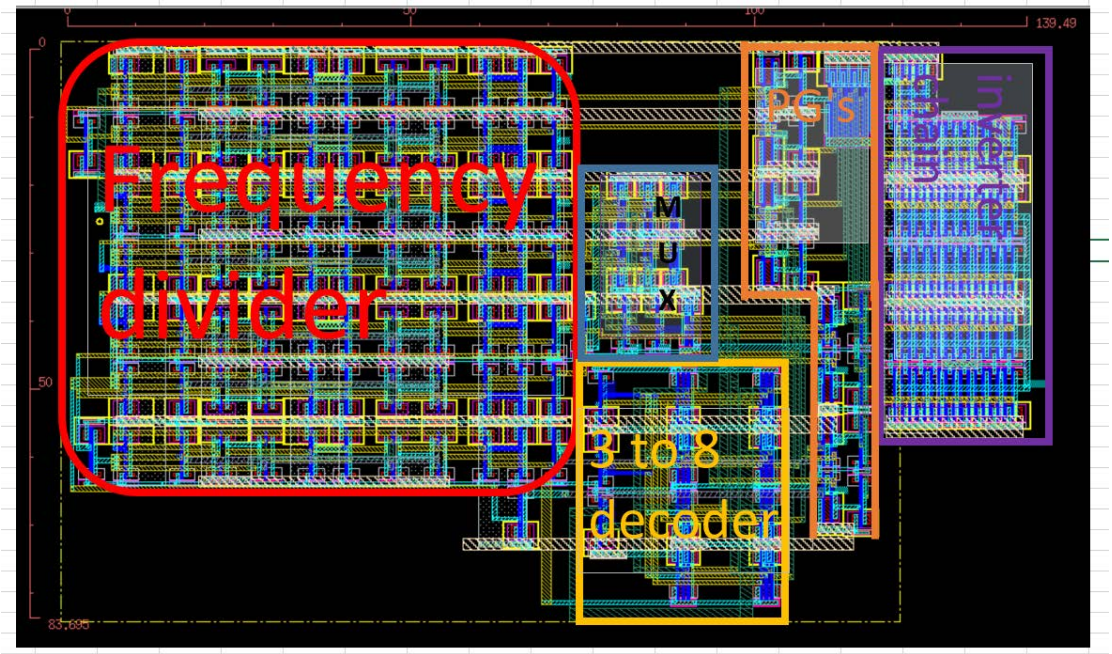
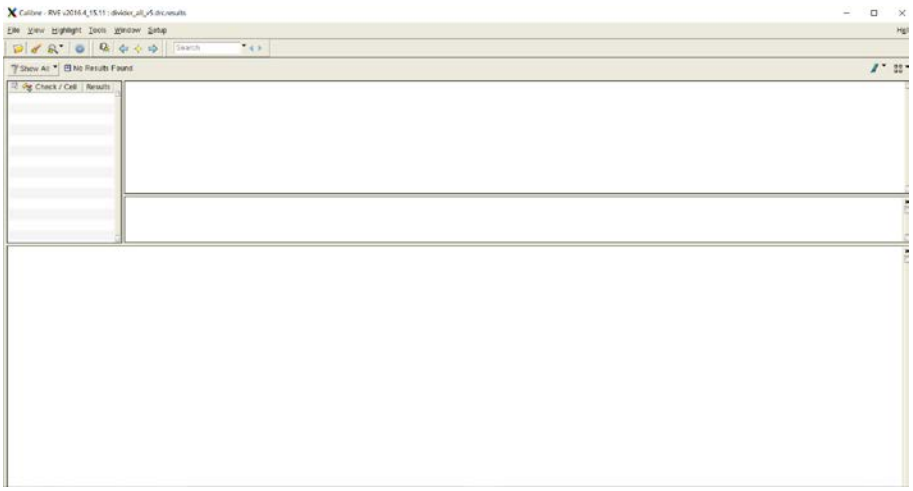


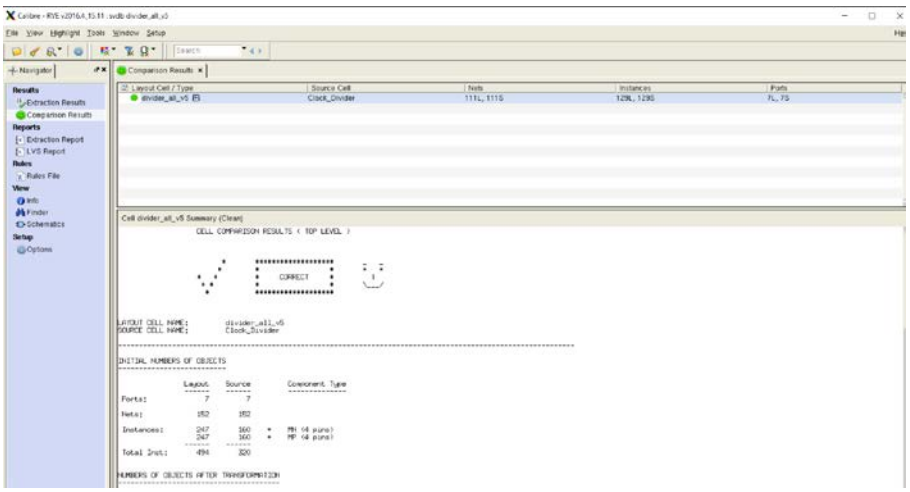

Fig14. Inverter chain 3stages, m=5、17、68

# Layout:



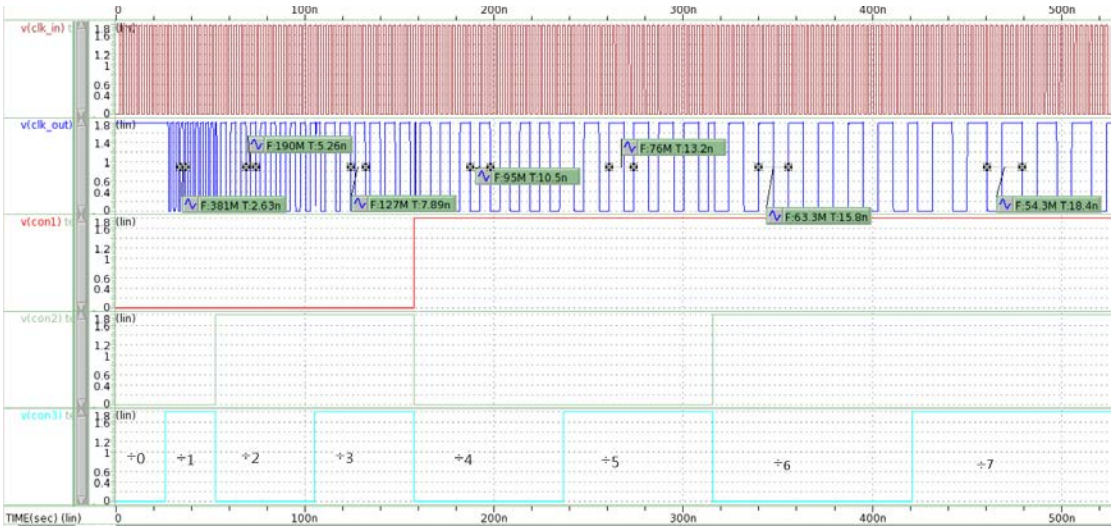

Layout area: 139.49(um)*83.69(um) = 11673.9(um^2)



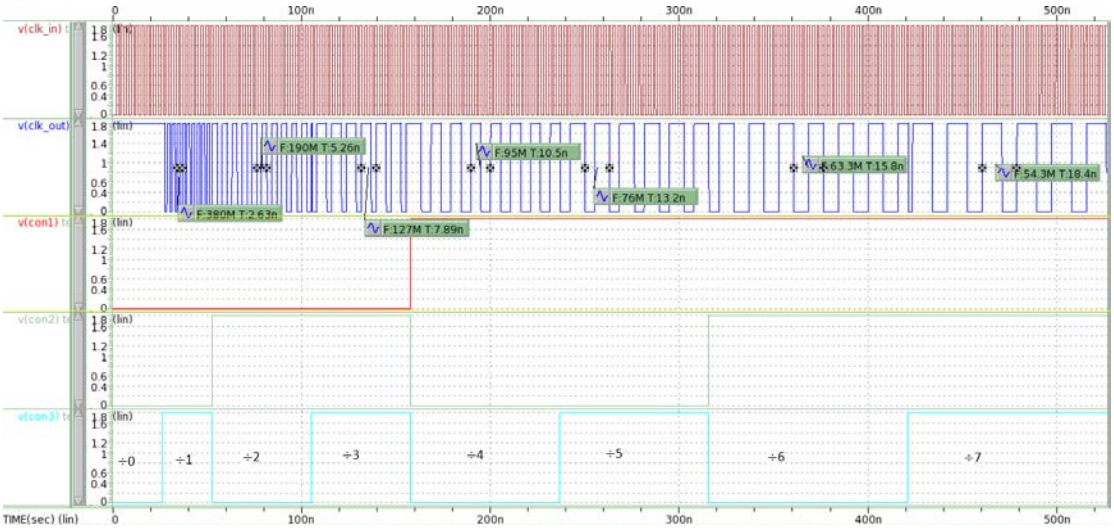


# Pre-sim:Waveview & Simulation Result 380MHz

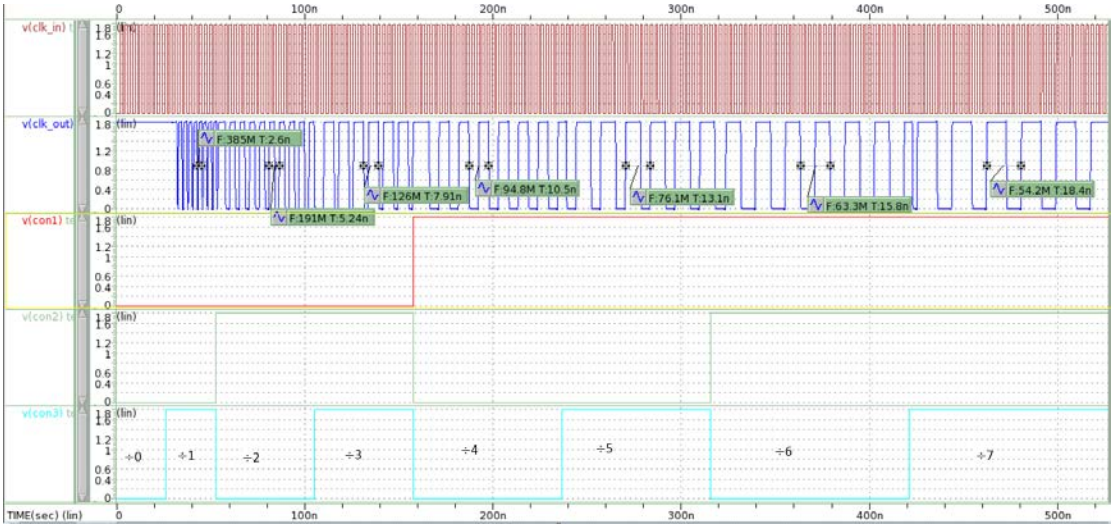
TT 25°



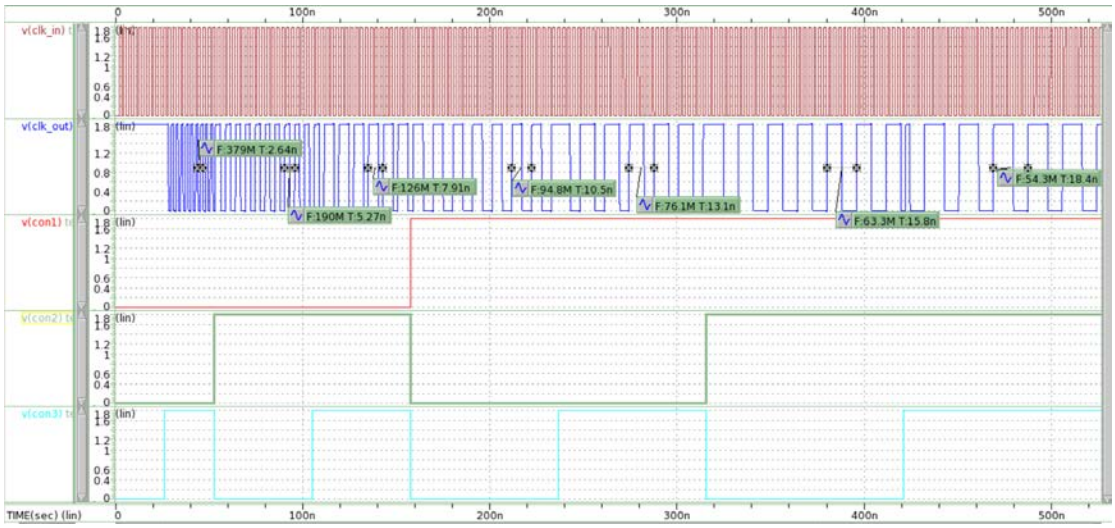

FF -40°



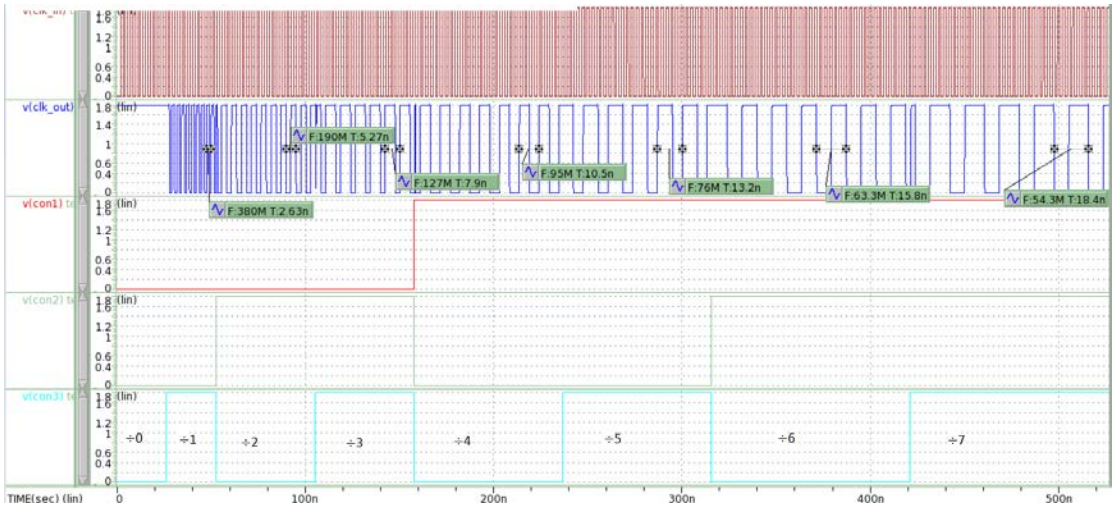

SS 125°



SF 25°




FS 25°




Pre-sim 頻率 380MHz

| | TT 25° | FF -40° | SS 125° | SF 25° | FS 25° |
|---|---|---|---|---|---|
| T0 | 2.64E-09 | 2.63E-09 | 2.67E-09 | 2.62E-09 | 2.64E-09 |
| T1 | 2.63E-09 | 2.63E-09 | 2.67E-09 | 2.65E-09 | 2.63E-09 |
| T2 | 5.26E-09 | 5.27E-09 | 5.26E-09 | 5.25E-09 | 5.26E-09 |
| T3 | 7.89E-09 | 7.90E-09 | 7.92E-09 | 7.91E-09 | 7.89E-09 |
| T4 | 1.05E-08 | 1.05E-08 | 1.06E-08 | 1.05E-08 | 1.05E-08 |
| T5 | 1.32E-08 | 1.32E-08 | 1.32E-08 | 1.32E-08 | 1.32E-08 |
| T6 | 1.58E-08 | 1.58E-08 | 1.58E-08 | 1.58E-08 | 1.58E-08 |
| T7 | 1.84E-08 | 1.84E-08 | 1.84E-08 | 1.84E-08 | 1.84E-08 |

| | TT 25° | FF -40° | SS 125° | SF 25° | FS 25° |
|---|---|---|---|---|---|
| freq_1 | 3.81E+08 | 3.8E+08 | 3.74E+08 | 3.78E+08 | 3.81E+08 |
| freq_2 | 1.9E+08 | 1.9E+08 | 1.90E+08 | 1.91E+08 | 1.90E+08 |
| freq_3 | 1.27E+08 | 1.27E+08 | 1.26E+08 | 1.26E+08 | 1.27E+08 |
| freq_4 | 9.50E+07 | 94970000 | 9.48E+07 | 9.52E+07 | 9.51E+07 |
| freq_5 | 7.60E+07 | 76020000 | 7.59E+07 | 7.59E+07 | 7.60E+07 |
| freq_6 | 6.33E+07 | 63330000 | 6.33E+07 | 6.33E+07 | 6.33E+07 |
| freq_7 | 5.43E+07 | 54280000 | 5.42E+07 | 5.42E+07 | 5.43E+07 |

| | TT 25° | FF -40° | SS 125° | SF 25° | FS 25° |
|---|---|---|---|---|---|
| freq_1_err | 1.447e-03 | 1.109e-03 | 1.53E-02 | 5.33E-03 | 1.67E-03 |
| freq_2_err | 8.459e-04 | 2.734e-04 | 1.30E-04 | 3.20E-03 | 9.57E-04 |
| freq_3_err | 6.009e-04 | 4.115e-04 | 2.54E-03 | 2.15E-03 | 6.11E-04 |
| freq_4_err | 4.354e-04 | 3.206e-04 | 1.91E-03 | 1.59E-03 | 4.91E-04 |
| freq_5_err | 3.487e-04 | 2.408e-04 | 1.43E-03 | 1.27E-03 | 3.86E-04 |
| freq_6_err | 2.140e-05 | 1.265e-06 | 8.97E-06 | 6.09E-06 | 1.72E-05 |
| freq_7_err | 2.301e-04 | 1.745e-04 | 1.02E-03 | 8.99E-04 | 2.67E-04 |

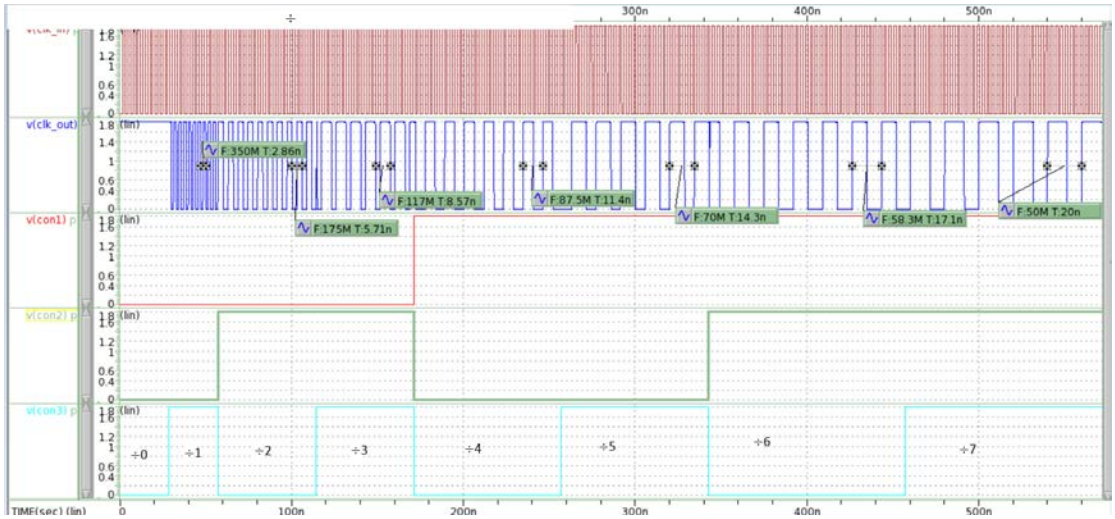
| | TT 25° | FF -40° | SS 125° | SF 25° | FS 25° |
|---|---|---|---|---|---|
| vdd_energy_0 | 1.569e-12 | 1.522e-12 | 1.58E-12 | 1.60E-12 | 1.55E-12 |
| vdd_energy_1 | 2.775e-11 | 2.795e-11 | 2.89E-11 | 2.90E-11 | 2.77E-11 |
| vdd_energy_2 | 2.295e-11 | 2.317e-11 | 2.48E-11 | 2.41E-11 | 2.29E-11 |
| vdd_energy_3 | 2.482e-11 | 2.378e-11 | 2.35E-11 | 2.63E-11 | 2.48E-11 |
| vdd_energy_4 | 2.084e-11 | 2.133e-11 | 2.28E-11 | 2.20E-11 | 2.07E-11 |
| vdd_energy_5 | 2.330e-11 | 2.321e-11 | 2.85E-11 | 2.46E-11 | 2.32E-11 |
| vdd_energy_6 | 3.067e-11 | 3.086e-11 | 3.32E-11 | 2.91E-11 | 2.72E-11 |
| vdd_energy_7 | 2.404e-11 | 2.407e-11 | 2.57E-11 | 2.52E-11 | 2.39E-11 |

| | TT 25° | FF -40° | SS 125° | SF 25° | FS 25° |
|---|---|---|---|---|---|
| pwr_0 | 0.000298 | 0.000289 | 3.00E-04 | 3.05E-04 | 2.95E-04 |
| pwr_1 | 0.002636 | 0.002655 | 2.75E-03 | 2.75E-03 | 2.63E-03 |
| pwr_2 | 0.001453 | 0.001468 | 1.57E-03 | 1.53E-03 | 1.45E-03 |
| pwr_3 | 0.001179 | 0.001129 | 1.12E-03 | 1.25E-03 | 1.18E-03 |
| pwr_4 | 0.000792 | 0.000811 | 8.67E-04 | 8.36E-04 | 7.88E-04 |
| pwr_5 | 0.000738 | 0.000735 | 9.04E-04 | 7.79E-04 | 7.34E-04 |
| pwr_6 | 0.000833 | 0.000838 | 9.01E-04 | 7.90E-04 | 7.37E-04 |
| pwr_7 | 0.000571 | 0.000572 | 6.11E-04 | 5.99E-04 | 5.67E-04 |
| total | 1.063e-03 | 1.062e-03 | 1.13E-03 | 1.10E-03 | 1.05E-03 |

# Post-sim:Waveview & Simulation Result 350MHz

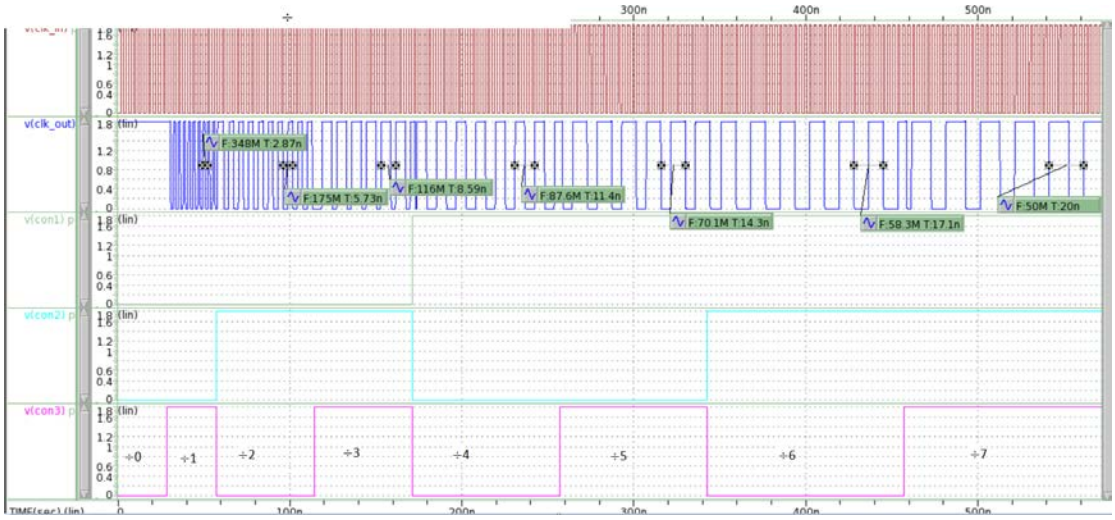
TT 25°


FF -40°

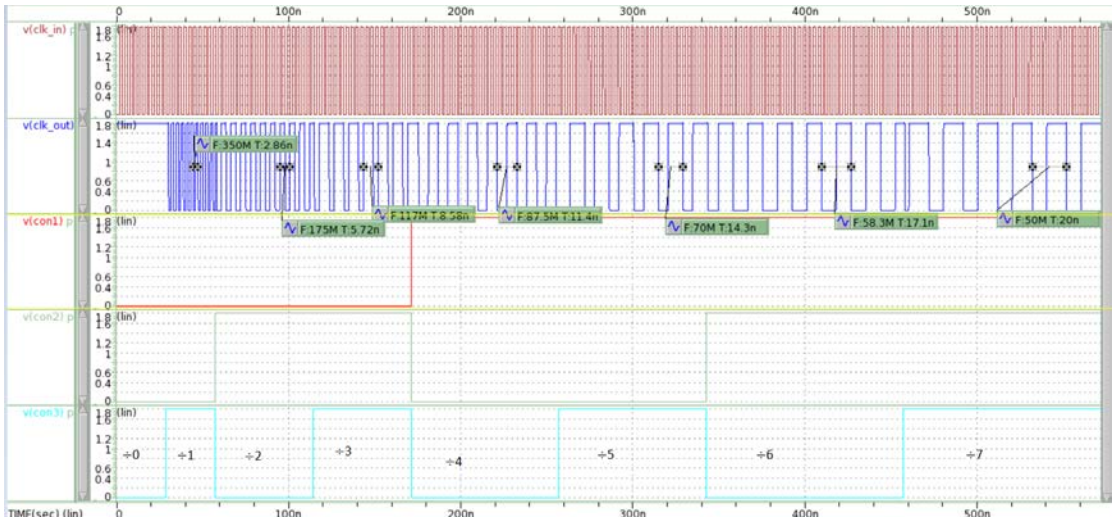



SS 125°

SF 25°




FS 25°




Post-sim 頻率 350MHz

| | TT 25° | FF -40° | SS 125° | SF 25° | FS 25° |
|---|---|---|---|---|---|
| T0 | 2.86E-09 | 2.86E-09 | 2.86E-09 | 2.85E-09 | 2.86E-09 |
| T1 | 2.85E-09 | 2.85E-09 | 2.85E-09 | 2.88E-09 | 2.85E-09 |
| T2 | 5.72E-09 | 5.71E-09 | 5.89E-09 | 5.72E-09 | 5.72E-09 |
| T3 | 8.57E-09 | 8.57E-09 | 1.14E-08 | 8.59E-09 | 8.57E-09 |
| T4 | 1.14E-08 | 1.14E-08 | 1.41E-08 | 1.14E-08 | 1.14E-08 |
| T5 | 1.43E-08 | 1.43E-08 | 1.71E-08 | 1.43E-08 | 1.43E-08 |
| T6 | 1.71E-08 | 1.71E-08 | 2.29E-08 | 1.71E-08 | 1.71E-08 |
| T7 | 2.00E-08 | 2.00E-08 | 2.00E-08 | 2.00E-08 | 2.00E-08 |

| | TT 25° | FF -40° | SS 125° | SF 25° | FS 25° |
|---|---|---|---|---|---|
| freq_1 | 3.50E+08 | 3.50E+08 | 3.51E+08 | 3.48E+08 | 3.51E+08 |
| freq_2 | 1.75E+08 | 1.75E+08 | 1.70E+08 | 1.75E+08 | 1.75E+08 |
| freq_3 | 1.17E+08 | 1.17E+08 | 8.75E+07 | 1.17E+08 | 1.17E+08 |
| freq_4 | 8.75E+07 | 8.75E+07 | 7.07E+07 | 8.74E+07 | 8.75E+07 |
| freq_5 | 7.00E+07 | 7.00E+07 | 5.83E+07 | 6.99E+07 | 7.00E+07 |
| freq_6 | 5.83E+07 | 5.83E+07 | 4.38E+07 | 5.83E+07 | 5.83E+07 |
| freq_7 | 5.00E+07 | 5.00E+07 | 5.00E+07 | 5.00E+07 | 5.00E+07 |

| | TT 25° | FF -40° | SS 125° | SF 25° | FS 25° |
|---|---|---|---|---|---|
| freq_1_err | 1.24E-03 | 9.65E-04 | 2.91E-03 | 6.40E-03 | 1.31E-03 |
| freq_2_err | 6.84E-04 | 2.41E-05 | 2.92E-02 | 1.17E-04 | 7.93E-04 |
| freq_3_err | 4.72E-04 | 3.42E-04 | 0.25 | 1.79E-03 | 5.44E-04 |
| freq_4_err | 2.37E-04 | 2.39E-04 | 0.1919 | 1.33E-03 | 2.72E-04 |
| freq_5_err | 2.80E-04 | 2.06E-04 | 0.1666 | 1.08E-03 | 3.02E-04 |
| freq_6_err | 3.37E-07 | 9.00E-06 | 0.25 | 2.34E-06 | 2.40E-06 |
| freq_7_err | 1.98E-04 | 1.51E-04 | 6.50E-06 | 7.72E-04 | 2.35E-04 |

| | TT 25° | FF -40° | SS 125° | SF 25° | FS 25° |
|---|---|---|---|---|---|
| vdd_energy_0 | 3.03E-12 | 3.05E-12 | 3.29E-12 | 2.99E-12 | 2.99E-12 |
| vdd_energy_1 | 3.15E-11 | 3.17E-11 | 3.29E-11 | 3.23E-11 | 3.14E-11 |
| vdd_energy_2 | 2.89E-11 | 2.93E-11 | 2.83E-11 | 3.00E-11 | 2.87E-11 |
| vdd_energy_3 | 3.11E-11 | 3.16E-11 | 2.87E-11 | 3.15E-11 | 3.09E-11 |
| vdd_energy_4 | 3.40E-11 | 3.42E-11 | 3.13E-11 | 3.12E-11 | 3.39E-11 |
| vdd_energy_5 | 3.84E-11 | 3.83E-11 | 3.25E-11 | 3.93E-11 | 3.82E-11 |
| vdd_energy_6 | 4.29E-11 | 4.33E-11 | 3.80E-11 | 4.72E-11 | 4.61E-11 |
| vdd_energy_7 | 3.84E-11 | 3.87E-11 | 4.00E-11 | 3.90E-11 | 3.82E-11 |

| | TT 25° | FF -40° | SS 125° | SF 25° | FS 25° |
|---|---|---|---|---|---|
| pwr_0 | 5.31E-04 | 5.33E-04 | 5.76E-04 | 5.23E-04 | 5.24E-04 |
| pwr_1 | 2.76E-03 | 2.77E-03 | 2.88E-03 | 2.83E-03 | 2.75E-03 |
| pwr_2 | 1.68E-03 | 1.71E-03 | 1.65E-03 | 1.75E-03 | 1.68E-03 |
| pwr_3 | 1.36E-03 | 1.38E-03 | 1.26E-03 | 1.38E-03 | 1.35E-03 |
| pwr_4 | 1.19E-03 | 1.20E-03 | 1.10E-03 | 1.09E-03 | 1.19E-03 |
| pwr_5 | 1.12E-03 | 1.12E-03 | 9.48E-04 | 1.15E-03 | 1.12E-03 |
| pwr_6 | 1.07E-03 | 1.08E-03 | 9.51E-04 | 1.18E-03 | 1.15E-03 |
| pwr_7 | 8.41E-04 | 8.46E-04 | 8.75E-04 | 8.53E-04 | 8.36E-04 |
| total | 1.32E-03 | 1.33E-03 | 1.28E-03 | 1.34E-03 | 1.32E-03 |

## Pre-sim results & Post-sim results Comparison

在題目要求的頻率準確率下，pre-sim 的 CLKin 最高頻率是 380MHz,而 post-sim 的 CLKin 最高頻率是 350MHz。(在 SS 125°, freq_2_到 10^-2 左右)。

從 waveview 以及 pex 所產生的 spi 丟進 testbench 的結果來看，因為 pre-sim 是理想狀況下的，post-sim 為真實 layout，layout 裡一定會有寄生電容和電阻，造成可操作最高頻率下降(pre-sim 380MHz v.s. post-sim 350MHz)，layout 面積也不可能達到完美，因此造成表現下降。

VDD_energy 則是在畫 layout 時會有額外的電阻，因此 pre-sim 的 VDD_energy 皆小於 post-sim 的 VDD_energy。

$$P = CVDD^2 f$$

由於 pre-sim 操作頻率較高，理論上如果 c 和 VDD 固定的話，pre-sim 的功率會大約是 post-sim 的 380/350 倍(頻率大小)。然而，畫 layout 會產生許多額外的寄生電容，造成 Cpre 和 Cpost 不一樣，且 Cpost>Cpre。因此在這五個 corner 中，post-sim 的功率都大於 pre-sim 的功率。

**TT 最高頻率:** Pre-sim,2.3G Post-sim,1.4G

| | TT 25°(pre-sim,2.3G) | TT 25°(post-sim,1.4G) |
|---|---|---|
| T0 | 8.69E-10 | 6.89E-10 |
| T1 | 8.69E-10 | 7.35E-10 |
| T2 | 8.69E-10 | 2.15E-09 |
| T3 | 2.17E-09 | 4.28E-09 |
| T4 | 1.73E-09 | 3.84E-09 |
| T5 | 3.04E-09 | 6.43E-09 |
| T6 | 4.35E-09 | 8.57E-09 |
| T7 | 3.48E-09 | 9.29E-09 |

| | TT 25°(pre-sim,2.3G) | TT 25°(post-sim, 1.4G) |
|---|---|---|
| freq_1 | 1.15E+09 | 1.36E+09 |
| freq_2 | 1.15E+09 | 4.65E+08 |
| freq_3 | 4.61E+08 | 2.34E+08 |
| freq_4 | 5.77E+08 | 2.61E+08 |
| freq_5 | 3.29E+08 | 1.56E+08 |
| freq_6 | 2.30E+08 | 1.17E+08 |
| freq_7 | 2.88E+08 | 1.08E+08 |

| | TT 25°(pre-sim,2.3G) | TT 25°(post-sim, 1.4G) |
|---|---|---|
| freq_1_err | 0.4996 | 2.88E-02 |
| freq_2_err | 8.22E-04 | 0.3358 |
| freq_3_err | 0.3987 | 0.4994 |
| freq_4_err | 2.68E-03 | 0.2558 |
| freq_5_err | 0.2846 | 0.4445 |
| freq_6_err | 0.4 | 0.5 |
| freq_7_err | 0.125 | 0.4616 |
| | TT 25°(pre-sim,2.3G) | TT 25°(post-sim, 1.4G) |
| vdd_energy_0 | 1.25E-12 | 4.36E-13 |
| vdd_energy_1 | 3.38E-12 | 2.84E-11 |
| vdd_energy_2 | 2.14E-11 | 1.99E-11 |
| vdd_energy_3 | 1.41E-11 | 2.22E-11 |
| vdd_energy_4 | 2.36E-11 | 2.34E-11 |
| vdd_energy_5 | 1.57E-11 | 2.35E-11 |
| vdd_energy_6 | 1.75E-11 | 2.65E-11 |
| vdd_energy_7 | 2.26E-11 | 2.49E-11 |

| | TT 25°(pre-sim,2.3G) | TT 25°(post-sim, 1.4G) |
|---|---|---|
| pwr_0 | 1.43E-03 | 3.05E-04 |
| pwr_1 | 1.95E-03 | 9.95E-03 |
| pwr_2 | 8.20E-03 | 4.63E-03 |
| pwr_3 | 4.05E-03 | 3.89E-03 |
| pwr_4 | 5.43E-03 | 3.28E-03 |
| pwr_5 | 3.01E-03 | 2.74E-03 |
| pwr_6 | 2.87E-03 | 2.65E-03 |
| pwr_7 | 3.24E-03 | 2.18E-03 |
| total | 3.77E-03 | 3.70E-03 |