EE3230 VLSI Design (2019 Fall) Final Project

Due date: 2019/01/14 (Tuesday) 1pm

No plagiarism is allowed!!

Please design a frequency divider with total 8 modes of operation, which is controlled by the signal CON1/CON2/CON3. The block diagram is shown below, where N is the division number determined by three control signals CON1/CON2/CON3 in binary, as shown in Table 1.

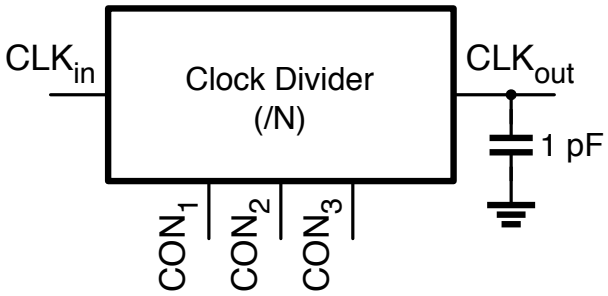

Table 1

CON_1	CON_2	CON_3	N
0	0	0	X (output stays HIGH)
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

In this final project, you can design the circuit in whatever implementation of your choice using the provided c018.l model file. However, the number of I/O pins is restricted to 1 input clock (CLK_{in}), 3 control signals (CON_{1-3}), and 1 output clock (CLK_{out}).

Specifications

CLK_{in}	Input clock with the highest frequency your design is able to operate at correctly. (T_r = T_f = 10 ps, duty cycle of 50%) This clock input sees a unit inverter (and only the unit inverter) with the following specified size: $(W/L)_N$=0.5μ/0.18μ and $(W/L)_P$=1.5μ/0.18μ.	
CON_{1-3}	Control signals that determine the operation	
VDD	1.8 V	
CLK_{out}	Output clock signal with the frequency determined by the input clock and the control signals The output duty cycle does not have to be 50%. However, this clock output sees a capacitive load of 1pF.	
Simulation accuracy	.option accurate = 1 runlvl = 5 With transient step of <1/1000 of input clock period	
Corners	**Process**	**Temperature**
	TT	25°C
	FF	–40°C
	SS	125°C
	SF	25°C
	FS	25°C

In your report, please provide the followings

Block Diagram

1. Draw top view of your system design and explain why you choose the architecture and how your design operates.
2. Draw sub-block in gate-level and transistor-level hierarchy and explain your design considerations in details.

Layout

1. Print-screen the whole design (with size & area) and label the sub-blocks.
2. DRC summary with no error (excluding the optional rules).
3. LVS report.

Simulation Results

1. Pre-sim results & post-sim results, need to compare and explain the difference between them.
2. Waveforms (with markers on important timing points) and tables (filled with measured data, including operating frequencies, power consumptions, important timing information, etc.) for the 8 operation modes.

Demo: (2019/01/14)

1. Explain to TAs why you choose the architecture and how your design operated.
2. Start from DRC/LVS/PEX and then the pre-sim and post-sim for 8-different results.
3. Show your best results on the Demo day.
   The grade of your project depends on the demo results.
   Data in the report should match the results on the Demo day.

Grading:

Demo (70%)

1. Layout (10%)
2. DRC (10%)
3. LVS (10%)
4. Waveforms (pre-sim & post-sim) (15%)
5. Simulation results, including **maximum operating frequency, power, and area** (pre-sim & post-sim) (15%)
6. Competition (based on TT corner results)
    - Max operating frequency (@ worst case) of CK_{in} node
      (4% for #1, 3% for #2, 2% for #3, and 1% for #4~10)
    - Area
      (4% for #1, 3% for #2, 2% for #3, and 1% for #4~10)
    - FoM = Max clock frequency/(Power*Area) (@ worst case)
      (4% for #1, 3% for #2, 2% for #3, and 1% for #4~10)

Report (30%)

- Block diagram (5%)
- Layout (5%)
- Simulation Results (5%)
- Explanations on design considerations as well as comments on simulation results (15%)

Reference:

2008 University/College IC Design Contest (Full-custom Final Competition)
(http://icdc.ee.ccu.edu.tw/2016/index2.php?page=OldExams)