EE3230 VLSI Design (2018 Fall) HW #3

Due date: 2017/12/06 (Thursday) 10am

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Please design an inverter chain with odd number of inverters that achieves the shortest propagation delay with the following conditions:

- V_{DD}=1.8 V.
- The size of the first inverter is fixed. $(W/L)_N$=0.5μ/0.18μ, and $(W/L)_P$=1.5μ/0.18μ.
- The inverter chain drives a capacitor load of 150 pF.
- The rise and fall time of the input is 0.01 ns, and the frequency is 50 MHz.

Hint: Estimate or simulate the input capacitance of the first inverter.

a. Explain the hand calculation or analysis you perform to reach this result.
b. Simulate and plot the waveforms for each node, including the input, for 30 ns. Use one row for each waveform. Label the key data points and show the propagation delay for both the rising and falling input.
c. Discard the input voltage source. Connect the output back to input to form an oscillation loop. Use the simulation results in question b to estimate the oscillation frequency before you simulate the oscillator.
d. Simulate and measure the oscillation frequency. What is the difference between the simulation result and the estimation in question c? Explain why they are different.
e. Perform hand analysis and estimate the power consumption of the oscillator.
f. Simulate the power consumption of the oscillator. What is the difference between the simulation result and the calculation in question e? Explain why they are different.
g. Complete the layout of the oscillator. Run post-layout simulation (R-C-CC extraction) and show the waveforms of each node. Explain your layout considerations. (What did you do to minimize the delay of each stage and the resulting oscillation period?) Measure the oscillation frequency and power consumption. (Don't forget the 150-pF capacitor load.) How different are the results compared to those in question d and question f? Explain why.