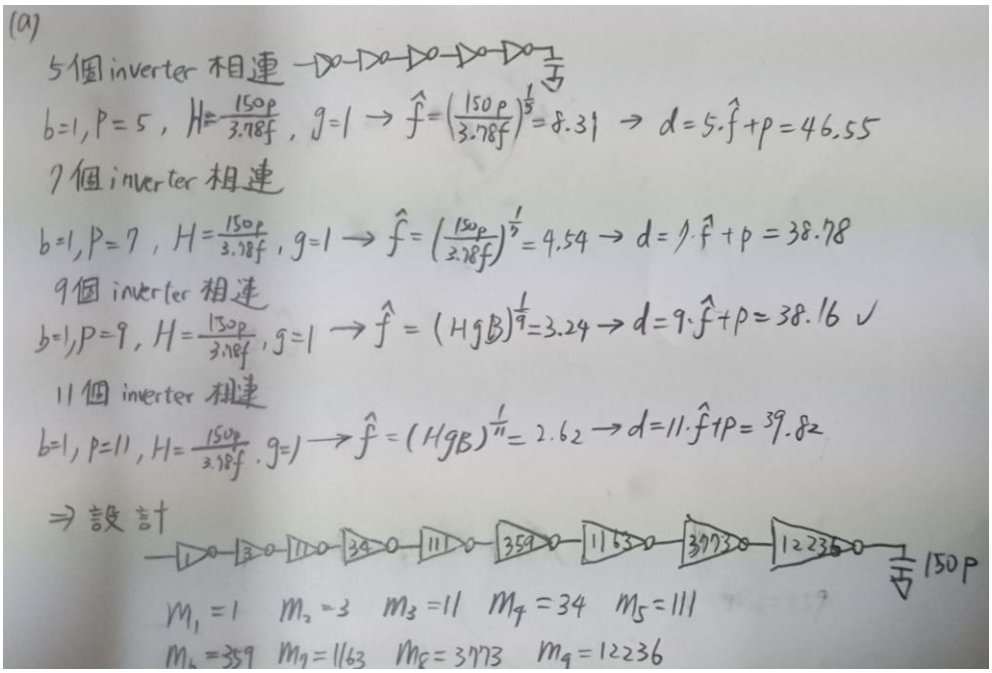
1.

```
hw3
.protect
.lib 'cic018.l' TT
.unprotect
.temp   25
.option post
.option captab

$ DGSB
Mn1 out1 in gnd gnd N_18 w=0.5u l=0.18u m=1
Mp1 out1 in vdd vdd P_18 w=1.5u l=0.18u m=1

Cl out1 gnd 150p

Vdd vdd gnd 1.8
Vin in gnd 0.9
*Vin in gnd pulse (0 1.8 0 0.01n 0.01 9.99n 100n)

.op

*.dc Vin 0 1.8 0.01
*.measure tran V_deriv find V(Vout) when deriv('V(Vout)')=-1

.end
```

```
****** operating point status is all       simulation time is
0.
    node    =voltage      node    =voltage      node    =voltage

+0:in      = 900.0000m 0:out1    = 463.8172m 0:vdd     =   1.8000


 maximum nodal capacitance=   1.500E-10         on node
0:out1

    nodal  capacitance table

    node    =    cap       node    =    cap       node    =    cap

+0:in      =   3.7804f 0:out1    = 150.0025p 0:vdd     =   7.5975f


**** voltage sources

subckt                  |
element  0:vdd      0:vin
 volts      1.8000   900.0000m
 current  -66.7119u    0.
 power    120.0815u    0.

    total voltage source power dissipation=  120.0815u       watts
```

由上圖可知$(W/L)_N = 0.5\mu/0.18\mu$, $(W/L)_P = 1.5\mu/0.18\mu$組成的 inverter 的 input capacitance $C_{in} = 3.78fF$

(a)



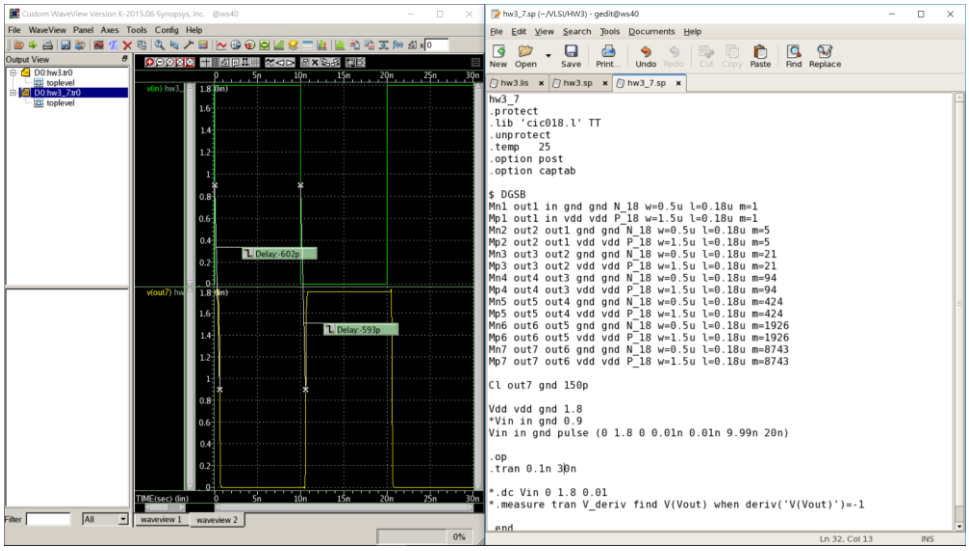
I. 由上圖手算估算出 9 個 inverter 會有較小的 delay，以下用”9 個 inverter 相連”(理論值)與”7 個 inverter 相連”以及”11 個 inverter 相連”的 delay 進行比較

	Fall delay	Rise delay
7 個 inverter 相連	602ps	593ps
9 個 inverter 相連	598ps	593ps
11 個 inverter 相連	628ps	622ps

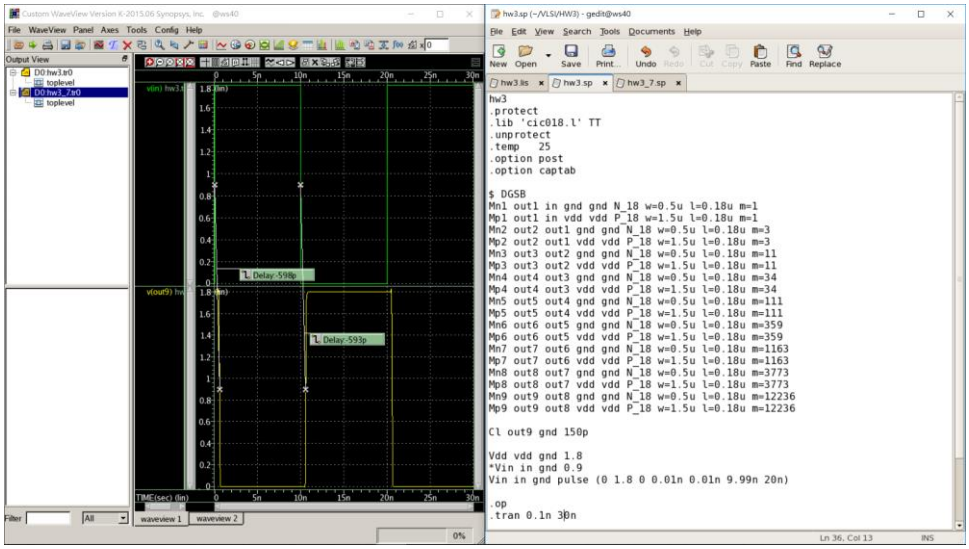
由上表顯示，” 9 個 inverter 相連”的形式不管是在 Fall delay 還是 Rise delay 都是三者內最佳，符合手算的結果。

II. 以下為” 7 個 inverter 相連”、”9 個 inverter 相連”、”11 個 inverter 相連”delay 圖

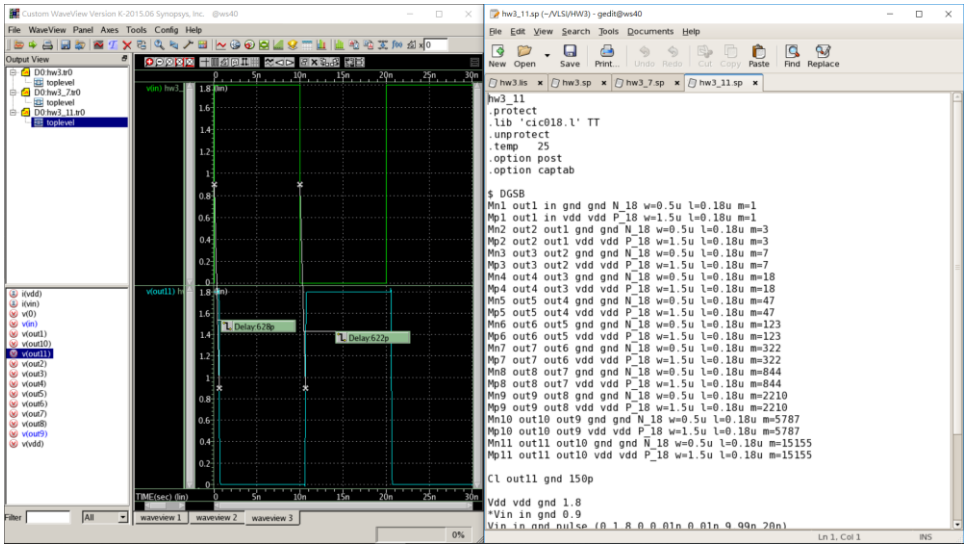
- 7 個 inverter 相連



I. 9 個 inverter 相連(理論值)



II. 11 個 inverter 相連



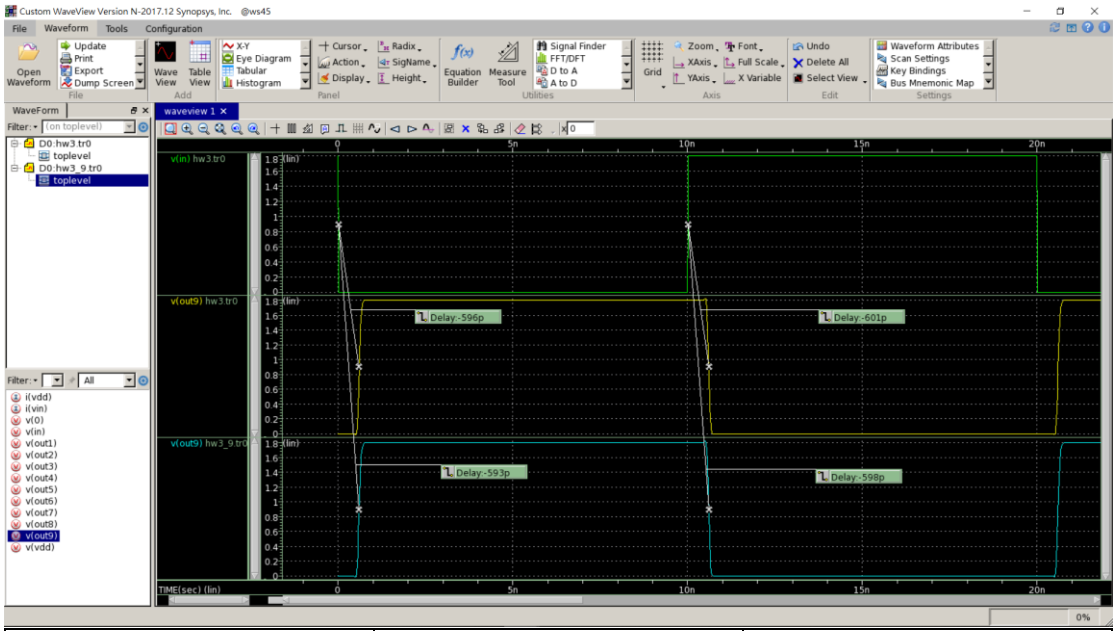
(b)

I. 為了增加之後 layout 的可行性，以下便會用 W 等比例的增加，以減少 MOS 並聯數(減少 m 值)的方法，實現上述的目的

- 改變後的 size

```
Mn1 out1 in   gnd gnd N_18 w=0.5u   l=0.18u m=1
Mp1 out1 in   vdd vdd P_18 w=1.5u   l=0.18u m=1
Mn2 out2 out1 gnd gnd N_18 w=1.62u  l=0.18u m=1
Mp2 out2 out1 vdd vdd P_18 w=4.86u  l=0.18u m=1
Mn3 out3 out2 gnd gnd N_18 w=5.26u  l=0.18u m=1
Mp3 out3 out2 vdd vdd P_18 w=15.78u l=0.18u m=1
Mn4 out4 out3 gnd gnd N_18 w=5.68u  l=0.18u m=3
Mp4 out4 out3 vdd vdd P_18 w=17.04u l=0.18u m=3
Mn5 out5 out4 gnd gnd N_18 w=5.53u  l=0.18u m=10
Mp5 out5 out4 vdd vdd P_18 w=16.59u l=0.18u m=10
Mn6 out6 out5 gnd gnd N_18 w=5.98u  l=0.18u m=30
Mp6 out6 out5 vdd vdd P_18 w=17.94u l=0.18u m=30
Mn7 out7 out6 gnd gnd N_18 w=5.82u  l=0.18u m=100
Mp7 out7 out6 vdd vdd P_18 w=17.46u l=0.18u m=100
Mn8 out8 out7 gnd gnd N_18 w=6.29u  l=0.18u m=300
Mp8 out8 out7 vdd vdd P_18 w=18.87u l=0.18u m=300
Mn9 out9 out8 gnd gnd N_18 w=6.12u  l=0.18u m=1000
Mp9 out9 out8 vdd vdd P_18 w=18.36u l=0.18u m=1000
```

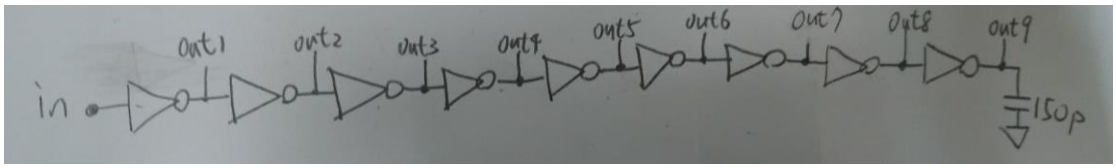
- Hw3_9(第二個波形)(改變前), Hw3(第一個波形)(改變後)



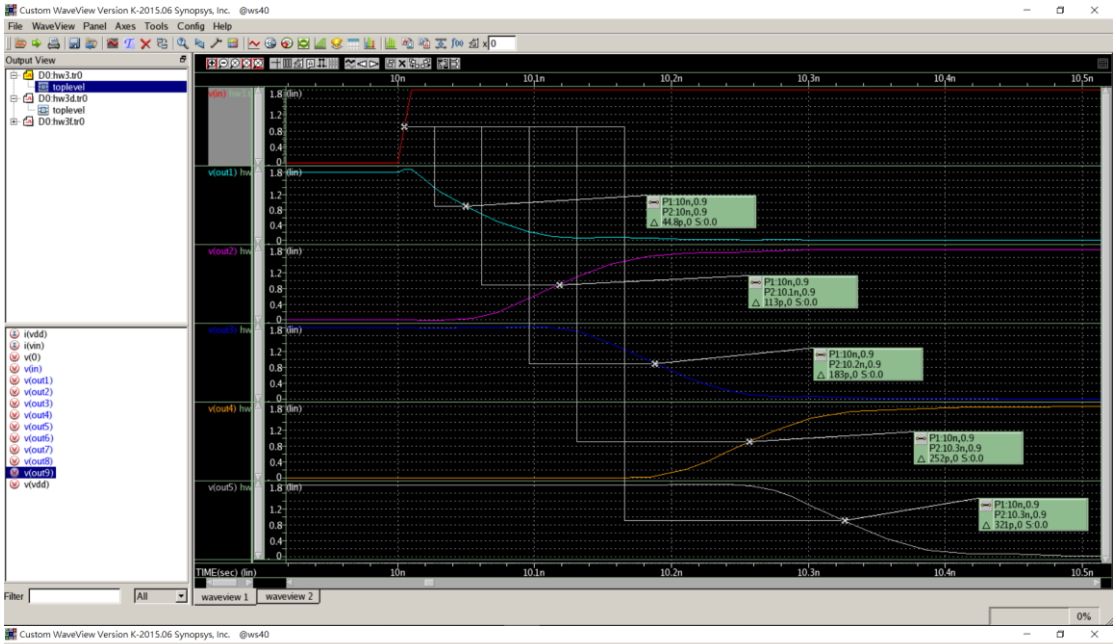
	Fall delay	Rise delay
Hw3_9(改變前)	598ps	593ps
Hw3(改變後)	601ps	596ps

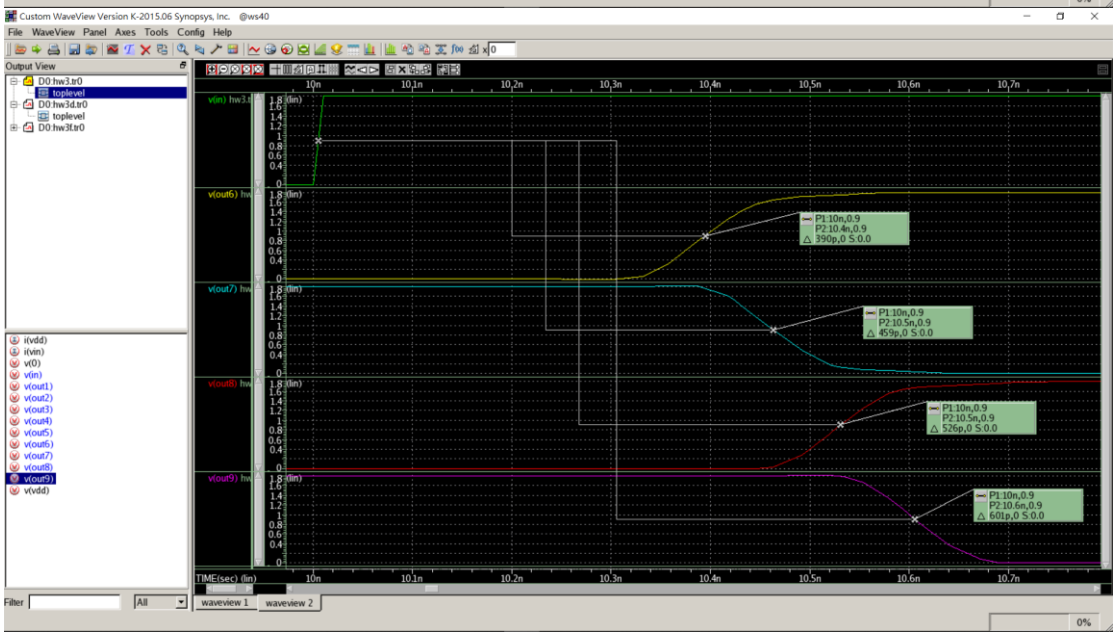
改變後的 delay 與(a)的” 7 個 inverter 相連”、”11 個 inverter 相連”相比，仍擁有相對最小的 delay。

II. 以下為各個 node 的 Fall delay 以及 Rise delay

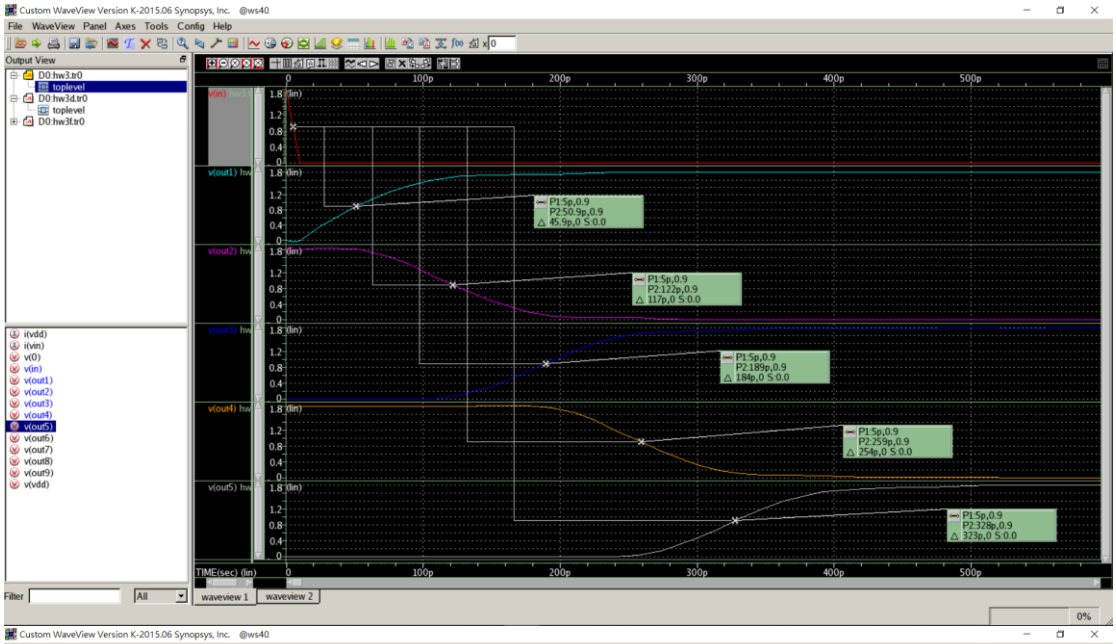


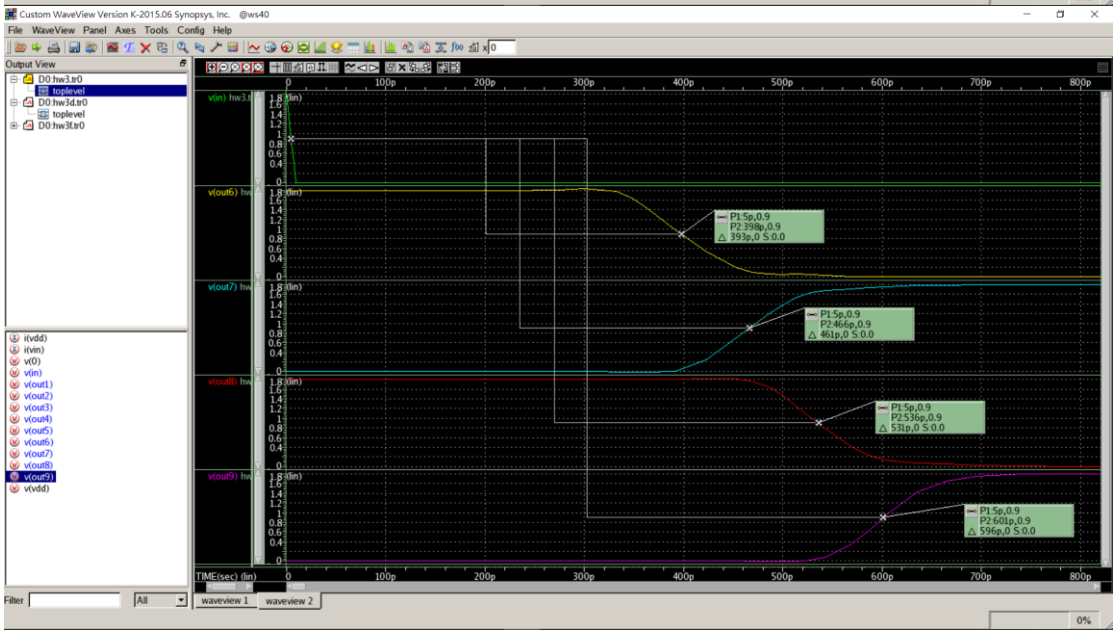
- 各級 propagation delay for rising input 圖





■ 各級 propagation delay for falling input 圖





	For rising input	For falling input
Out1	44.8ps	45.9ps
Out2	113ps	117ps
Out3	183ps	184ps
Out4	252ps	254ps
Out5	321ps	323ps
Out6	390ps	393ps
Out7	459ps	461ps
Out8	526ps	531ps
Out9	601ps	596ps

(c)

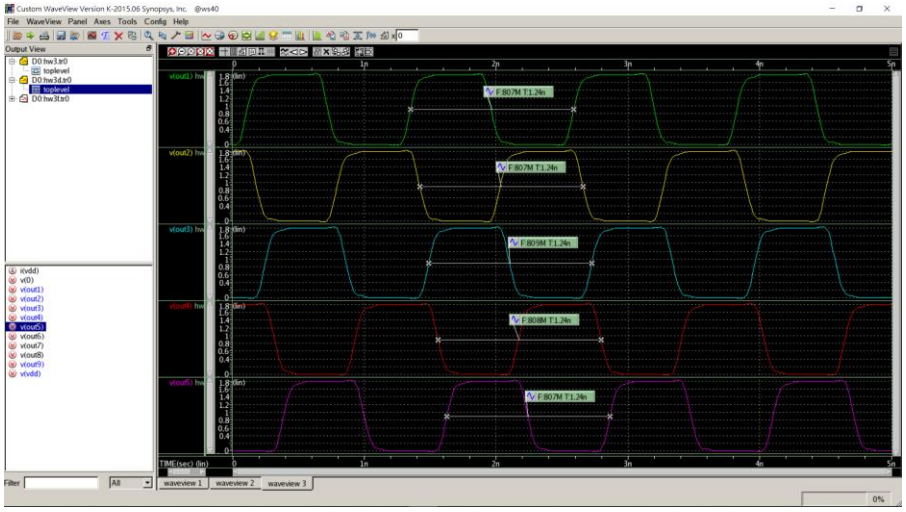
N=9, 每一級的 delay(d)取 $\frac{\text{out}_9\ \text{Fall delay} + \text{out}_9\ \text{Rise delay}}{2} \times \frac{1}{9} = \text{d}$

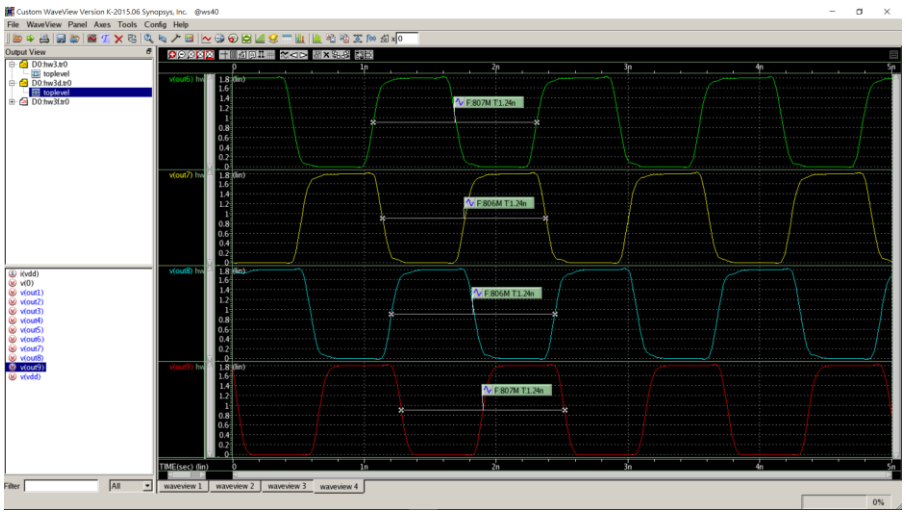
$$\text{f} = \frac{1}{2Nd} = \frac{1}{(601+596)\times 10^{-12}} \approx 835\text{MHz}$$

由估算得出 oscillation loop 的 frequency 應該在 835MHz 附近

(d)

- 各個 node 的 frequency 圖





- 實驗結果：顯示 oscillation loop 的 frequency 大約落在 807MHz，與估算結果有者 3.4%的誤差(= (835 − 807/835))。
- 分析：因為 node out9，也就是接回原本 Input 輸入點本身會自帶一個 output loading(C_{out9})，接回去第一級與第一級的 input loading 並聯 → Capacitance 增加 → RC time constant 增加 → 平均各級的 delay 增加 → 頻率(f = 1/(2Nd))下降，所以估算的頻率會比實驗值來的大。

(e)

```
    node    =    cap      node    =    cap      node    =    cap

+0:out1     =  14.7890f 0:out2     =  47.4627f 0:out3     = 153.2581f
+0:out4     = 497.1704f 0:out5     =   1.6130p 0:out6     =   5.2325p
+0:out7     =  18.5610p 0:out8     =  47.9602p 0:out9     = 178.6220p
+0:vdd      = 105.8697p
```

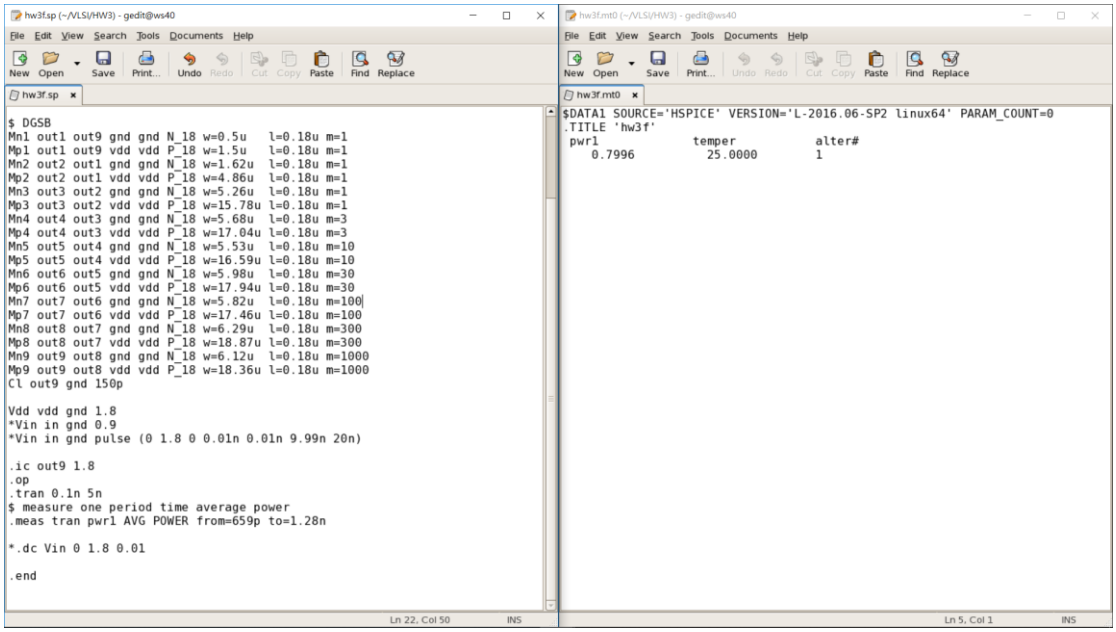
以上是在 out9=0.9V 下個 node 的電容值，C_{total}沒有含括C_{vdd}，因為此電容不會充放電，會一直保持在充飽的狀態。

→$C_{total} = C_{out1} + C_{out2} + C_{out3} + C_{out4} + C_{out5} + C_{out6} + C_{out7} + C_{out8} + C_{out9}$

$P = C_{total} \times V_{dd}^2 \times f = (252.7 \times 10^{-12}) \times 1.8^2 \times (807 \times 10^6) = 660.7mW$

由上述估算出 Power≈ 660.7mW

(f)



- 實驗結果：Power = 799.6mW
- 分析：由上圖實驗顯示，其測得 power 結果799.6mW，與(e)估算出 Power=660.7mW 相差138.9mW，這是因為我們在(e)估算時只有算到 dynamic power 部分，然而power = dynamic power + static power，因此(e)估算的值必會小於(f)測出來的值，且(f)、(e)間的差值為此電路的static power。

(g)