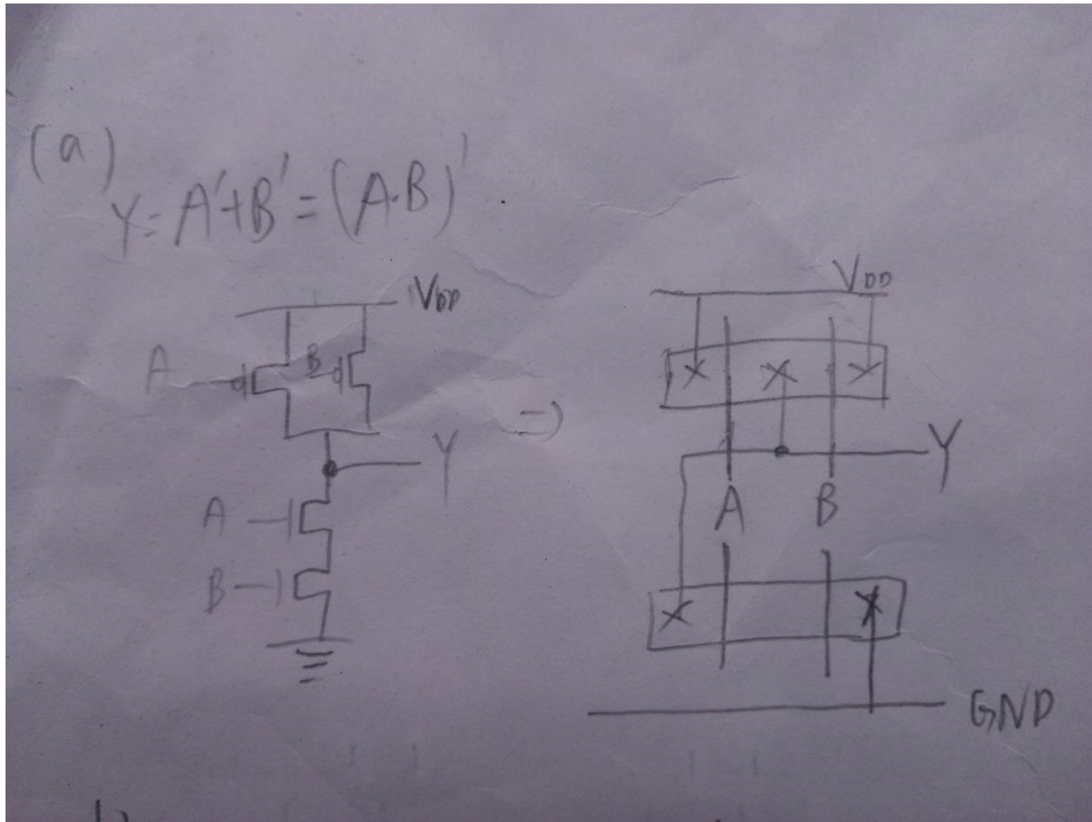
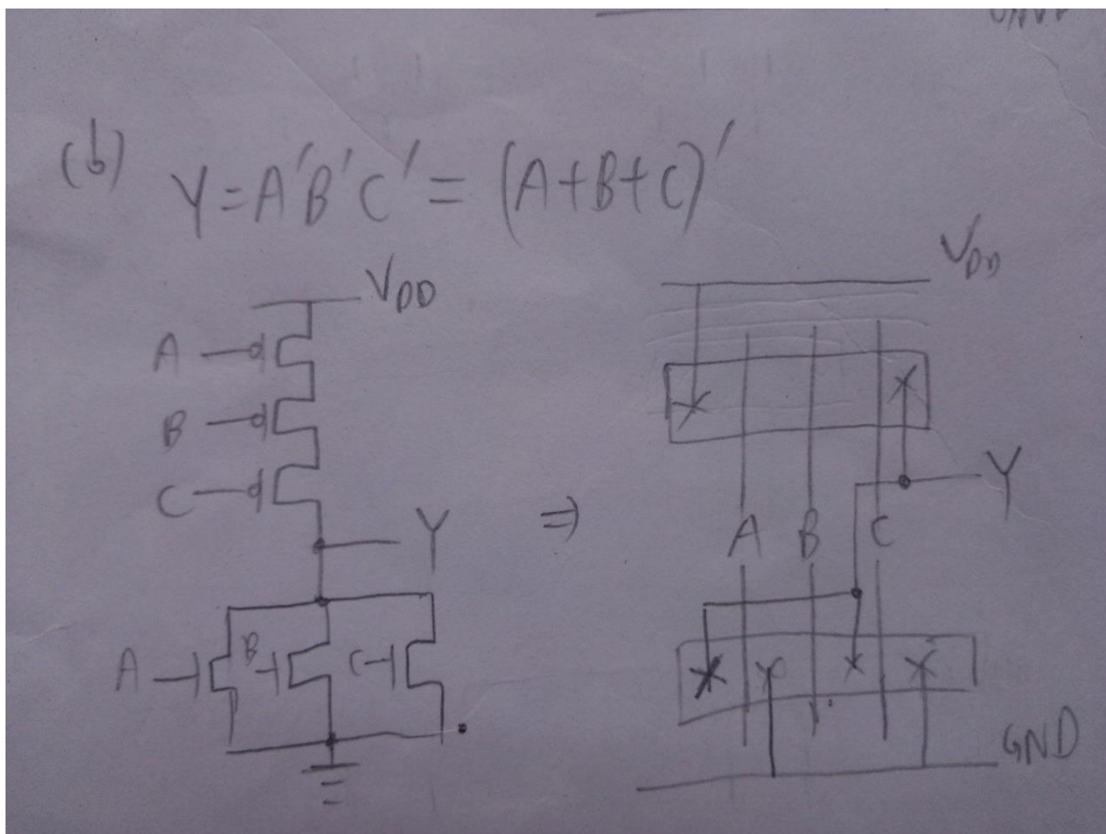
1.

(a)



(b)



(c)

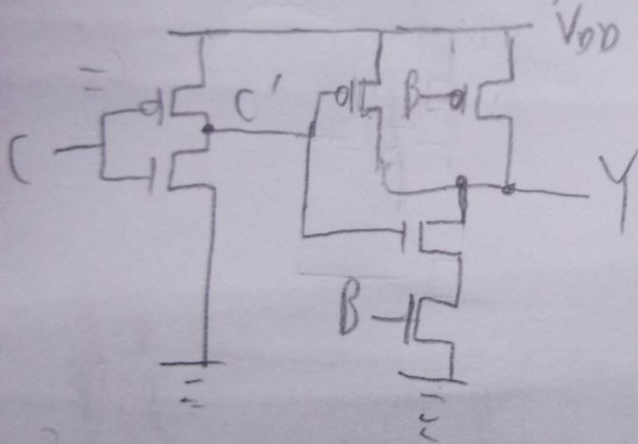
(c) $Y = AC + BC + B'$

K-Map

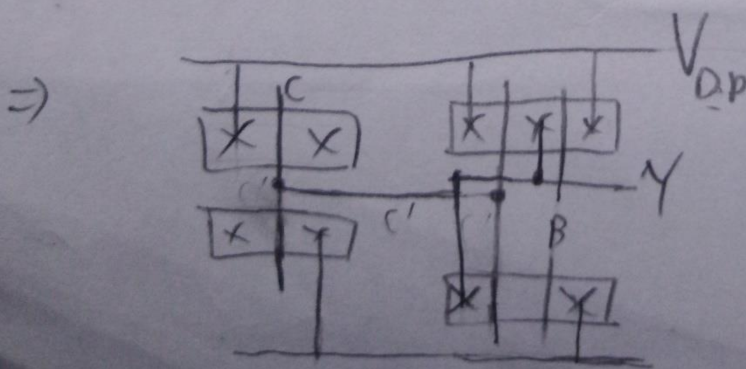
C \ AB	00	01	11	10
0	1	0	0	1
1	1	1	1	1

$\Rightarrow Y = B' + C$

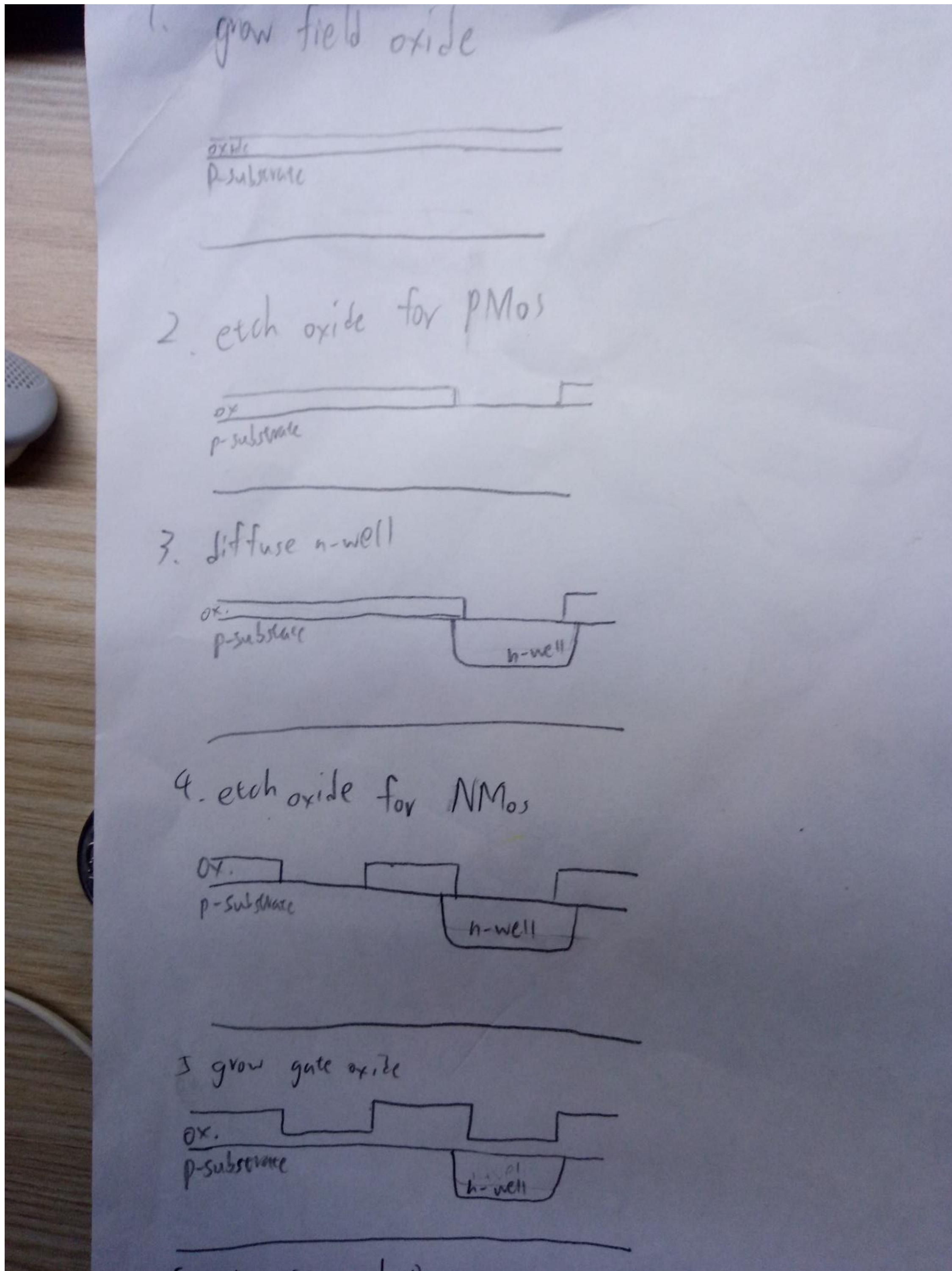
$Y = B' + C = (BC')'$

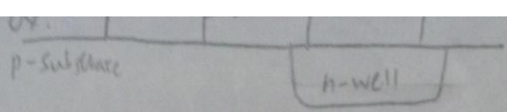


$\Rightarrow$

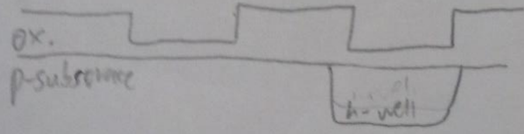


2.

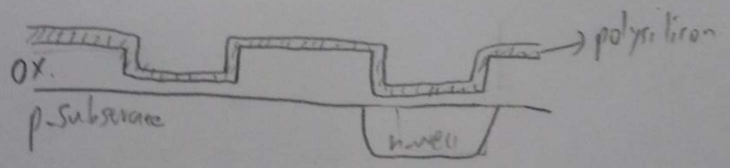




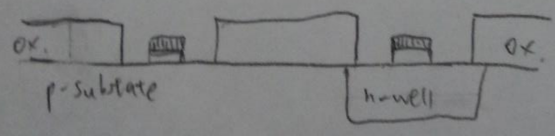
5 grow gate oxide



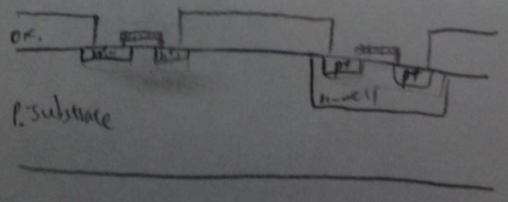
6. deposit polysilicon



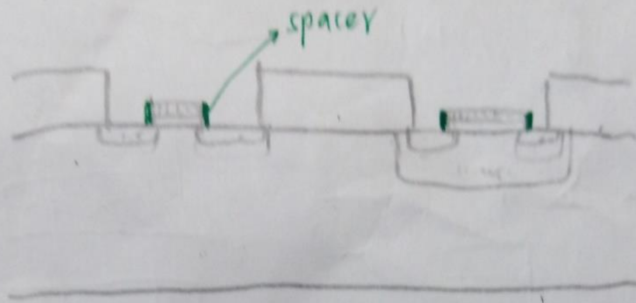
7. etch polysilicon and oxide



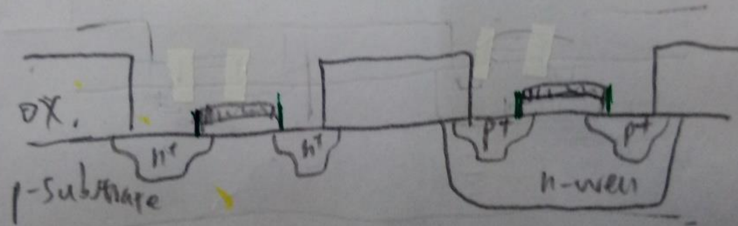
8. implant lightly doped sources and drains



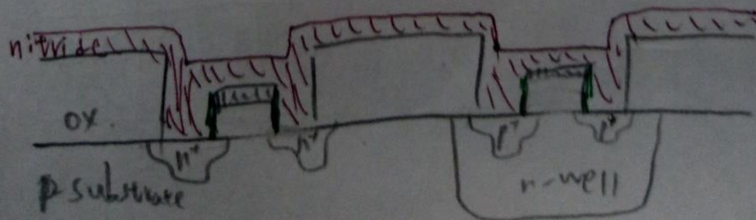
9. place Si_3N_4 spacer

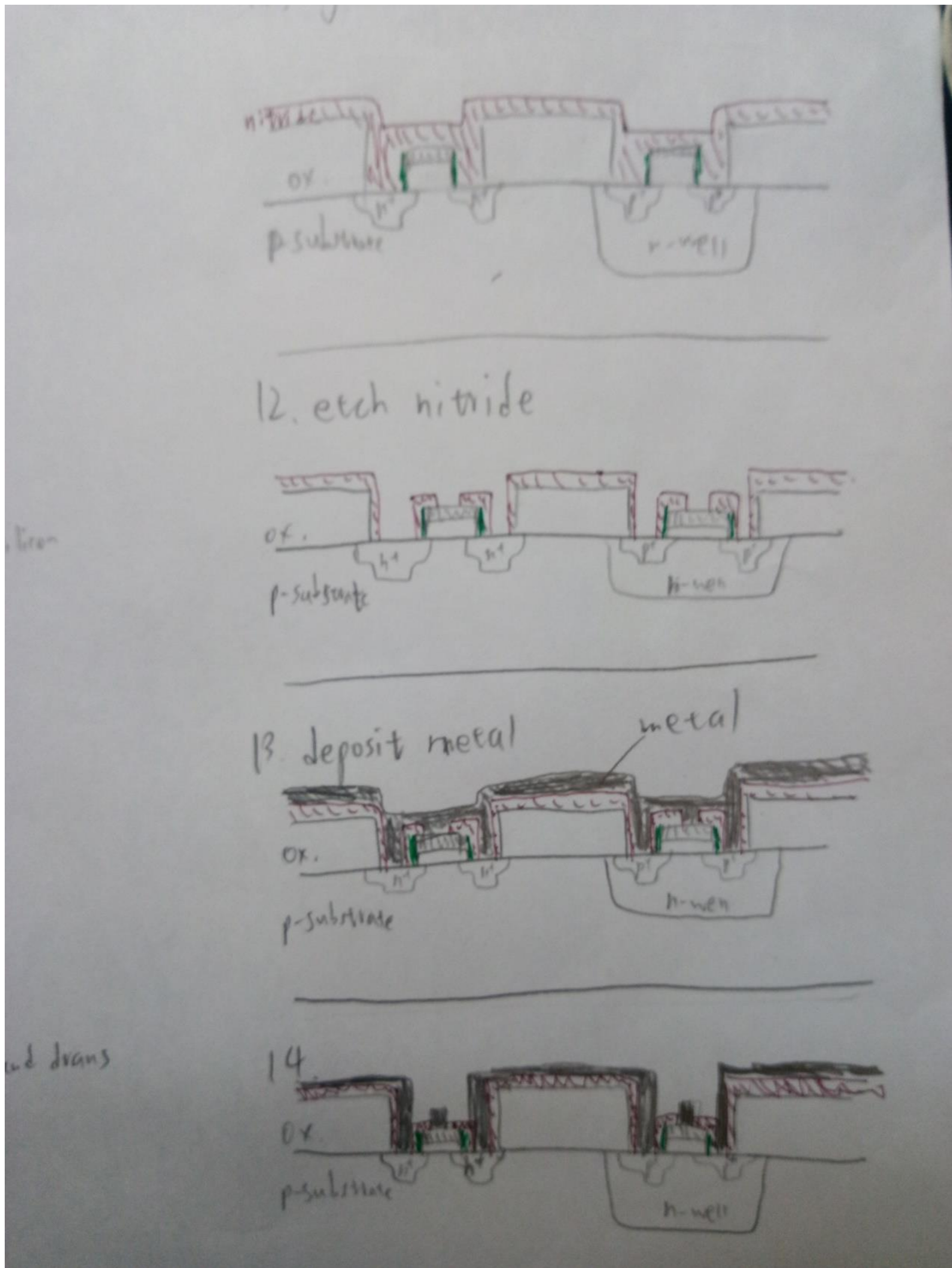


10. implant deep sources, drain



11. grow nitride





self-aligned poly-silicon gate:Cover a silicide layer on gate,source and drain,in order to reduce interconnection resistance of gate,source and drain.

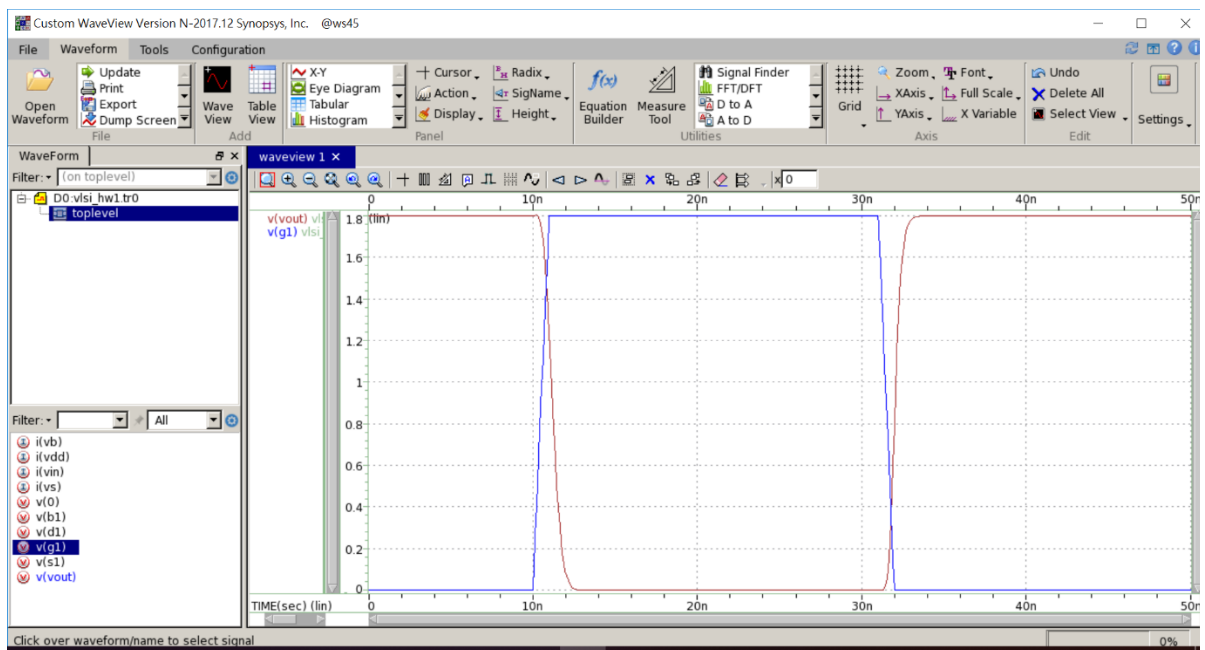
lightly-doped drain: 在 step 8 先 implant lightly doped sources and drains,再放 SiN spacer 於 gates 兩旁,再 implant normally doped sources and drains。Lightly doping 相較於正常的 doping 可以減少擴散,再用 SiN spacer 把正常 doping 的部分控制在想要的範圍內,能夠有效防止 doped sources and drains 的部分擴散太多以致於減少 channel length 與減少 gate 和 source,drain 的 overlap。

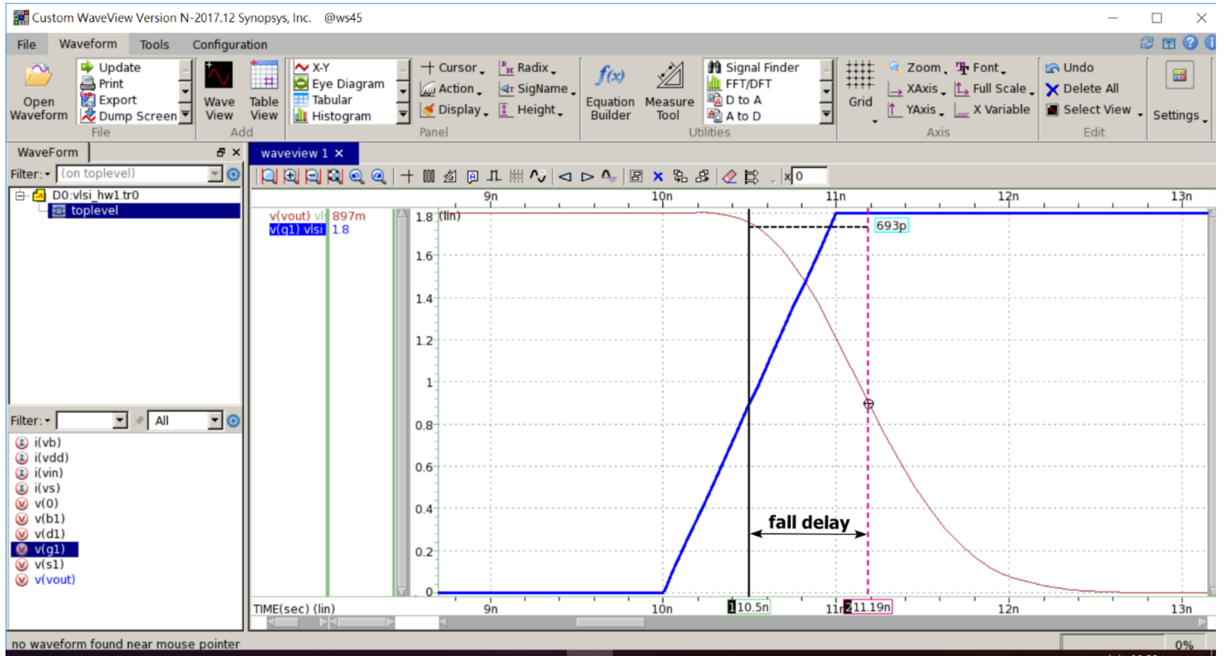
3.

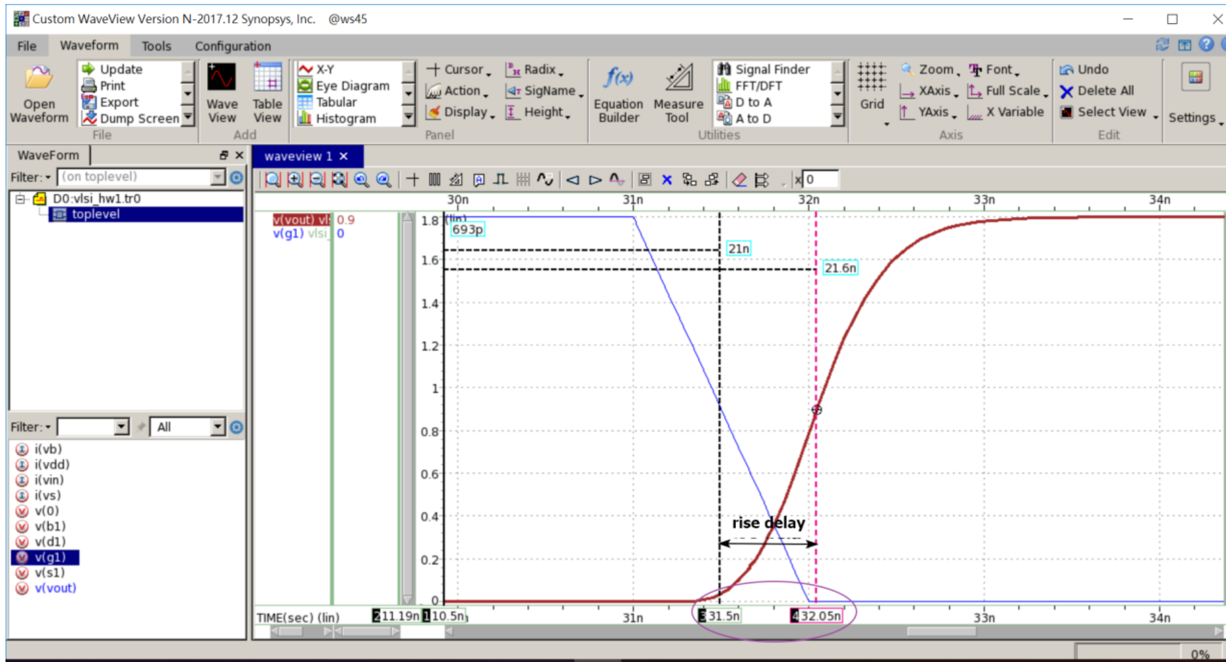
Process	temperature	NMOS width 1X	NMOS width 5X
		PMOS width	PMOS width
TT	25°C	1.125μm	3.8μm
FF	-40°C	1.325μm	4.094μm
SS	125°C	0.8μm	3.185μm
SF	25°C		0.9853μm
FS	25°C	0.74μm	2.78μm

4.

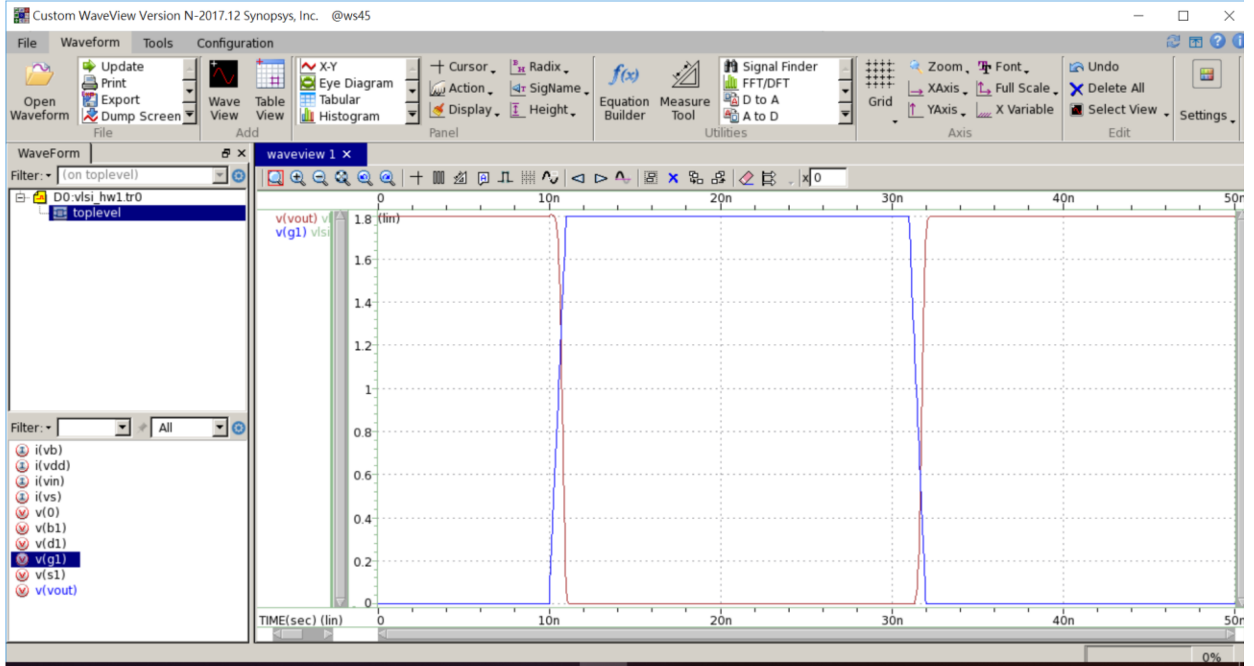
TT 25 NMOS width 1X

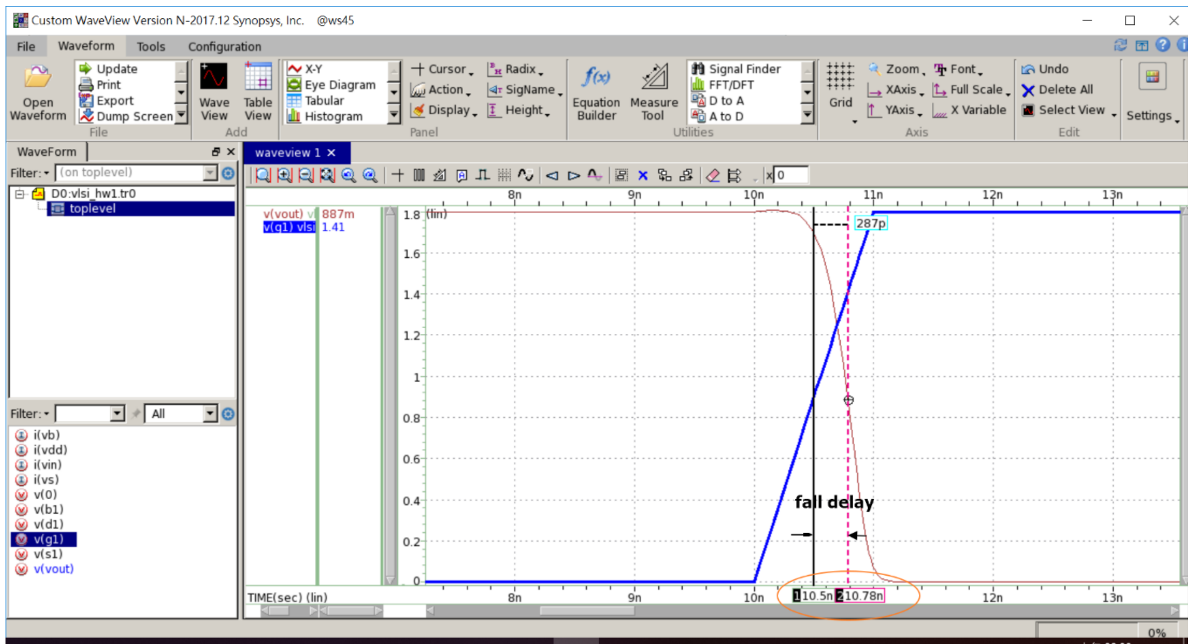


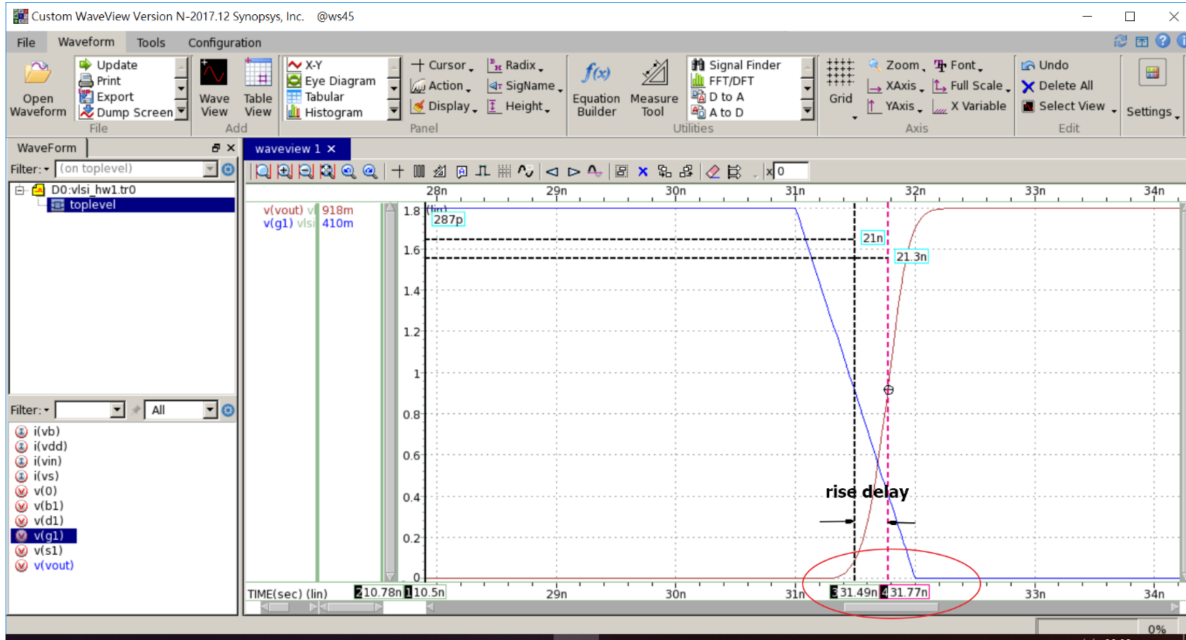

Custom WaveView Version N-2017.12 Synopsys, Inc. @ws45
waveview 1
v(vout) 897m
v(g1) 1.8
693p
fall delay
10.5n
11.19n
TIME(sec) (lin)
no waveform found near mouse pointer


Custom WaveView Version N-2017.12 Synopsys, Inc. @ws45
waveview 1
v(vout) 0.9
v(g1) 0
693p
21n
21.6n
rise delay
31.5n
32.05n
TIME(sec) (lin)

TT 25 NMOS width 5X







process	temperature	NMOS width 1X		NMOS width 5X	
		FALL DELAY	RISE DELAY	FALL DELAY	RISE DELAY
TT	25°C	0.59ns	0.55ns	0.28ns	0.28ns
FF	-40°C	0.52ns	0.43ns	0.22ns	0.23ns
SS	125°C	1.7ns	1.3ns	0.52ns	0.5ns
SF	25°C			0.45ns	0.53ns
FS	25°C	0.75ns	0.66ns	2.9ns	0.31ns