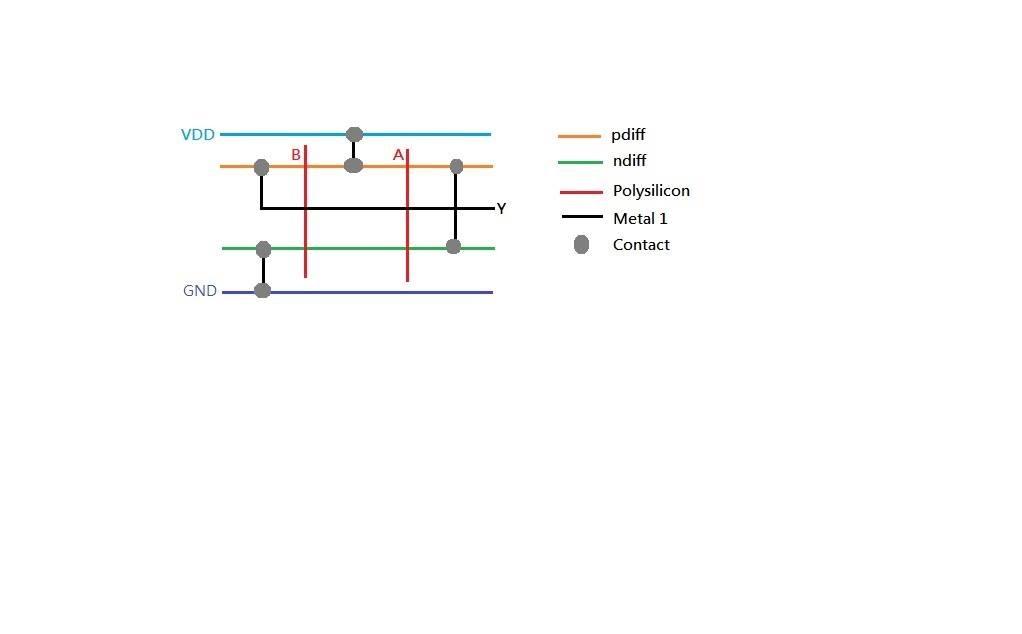
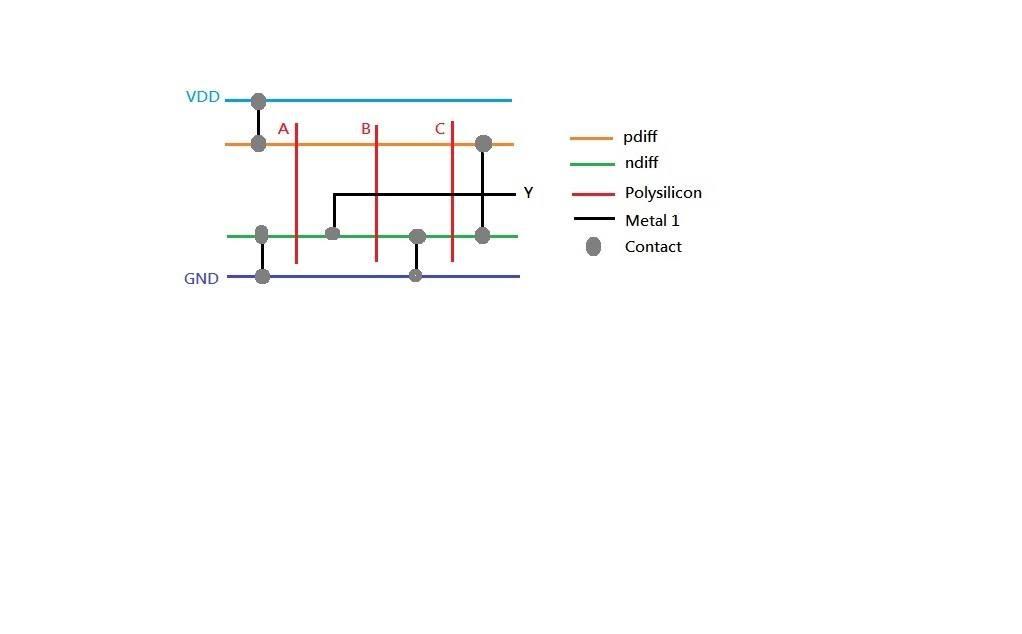
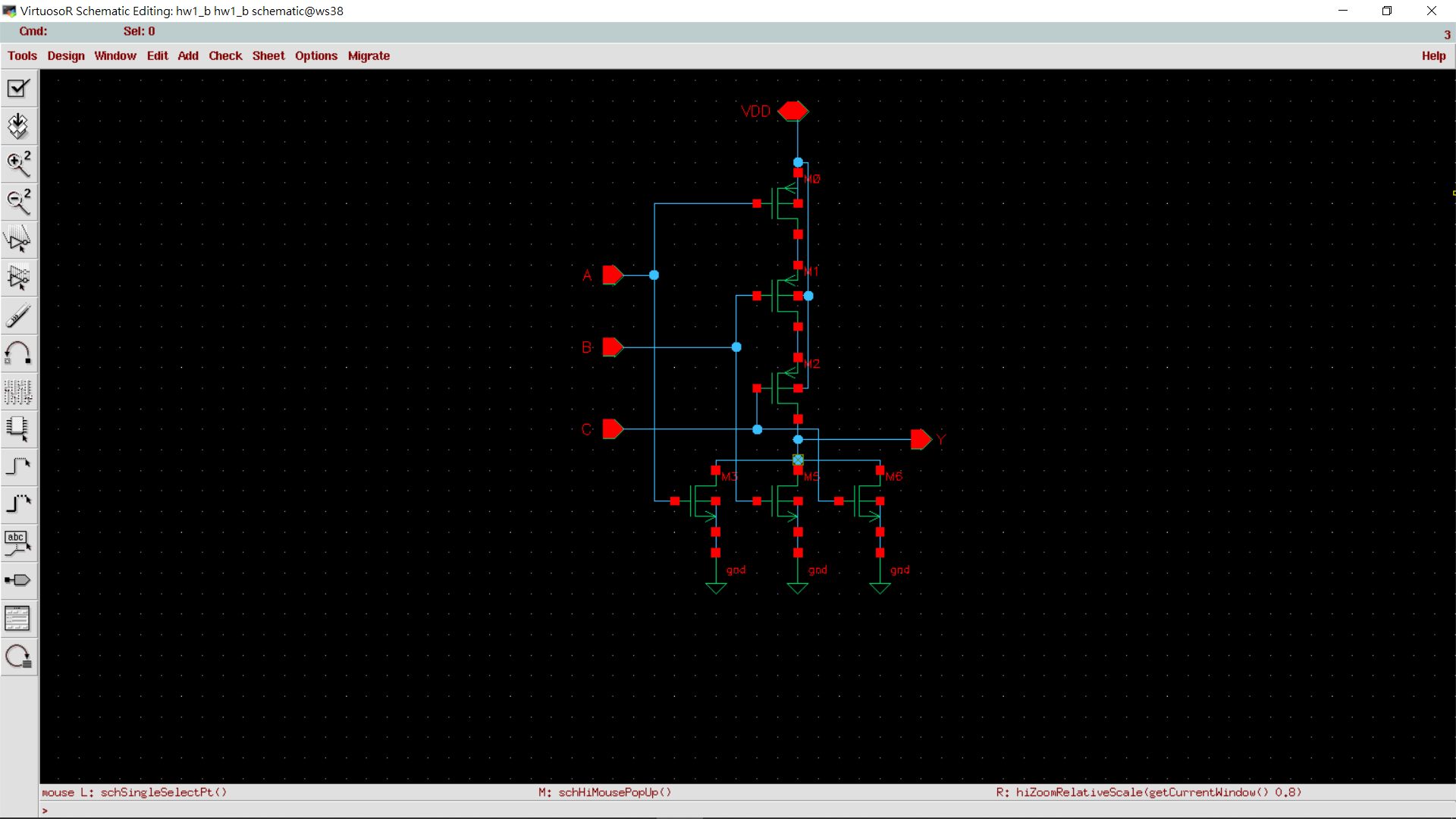
1.Use a combination of CMOS gates (in gate level symbols) and the corresponding stick diagrams to generate the following functions from A, B, and C.

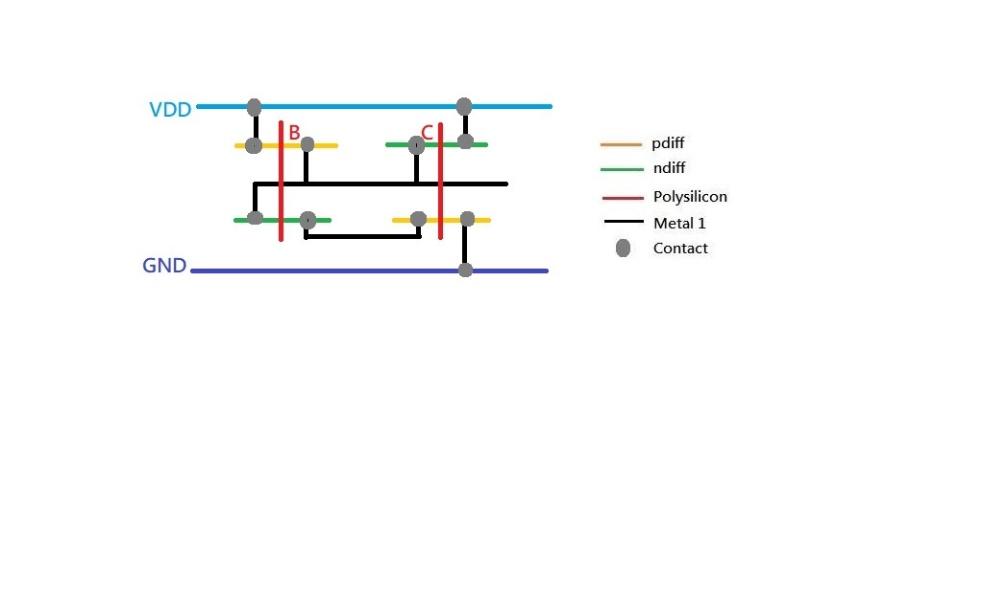
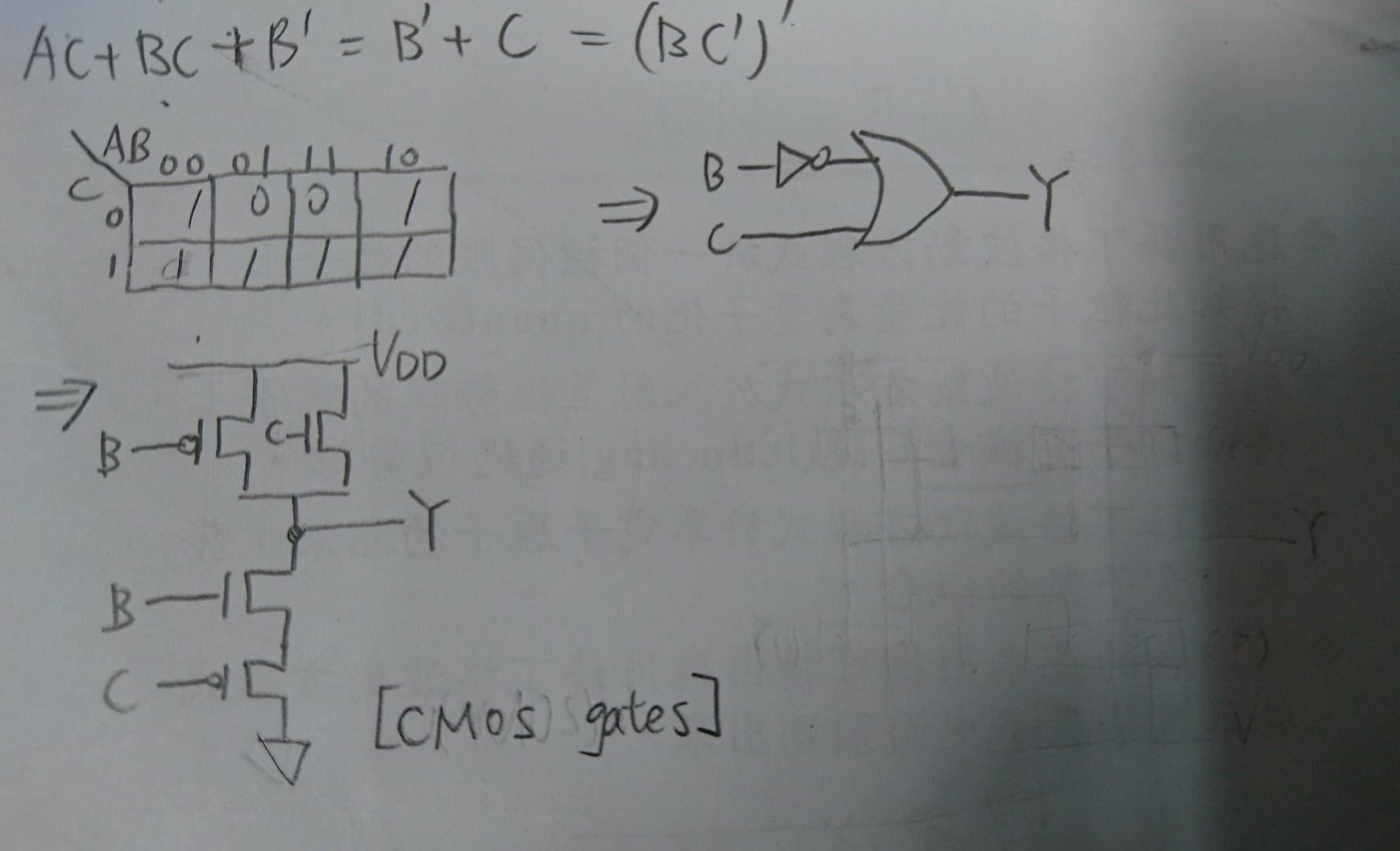
(a) Y=A’+B’(15%)



(b) Y=A’B’C’(15%)

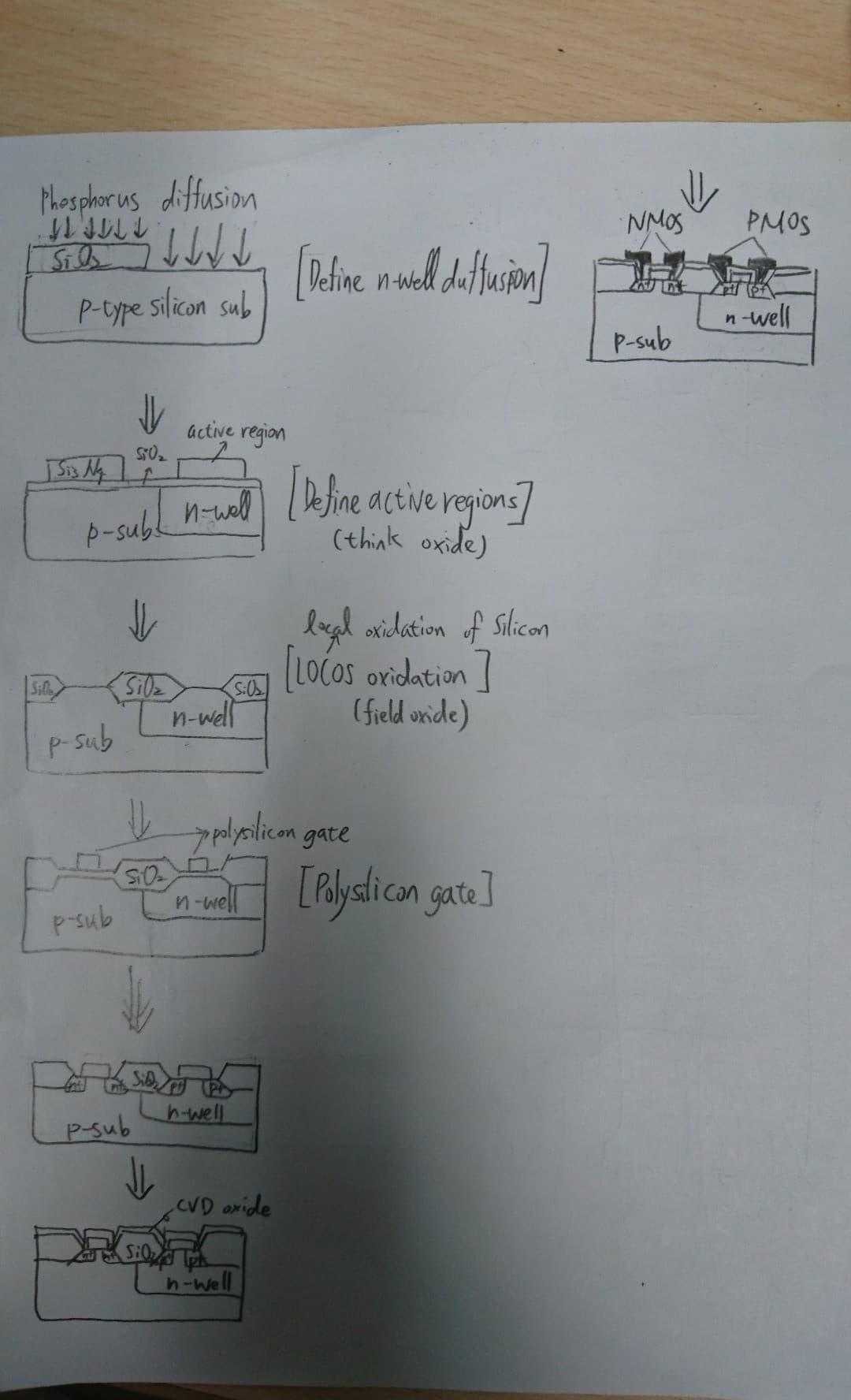


(c) Y=AC+BC+B’(15%)

‘

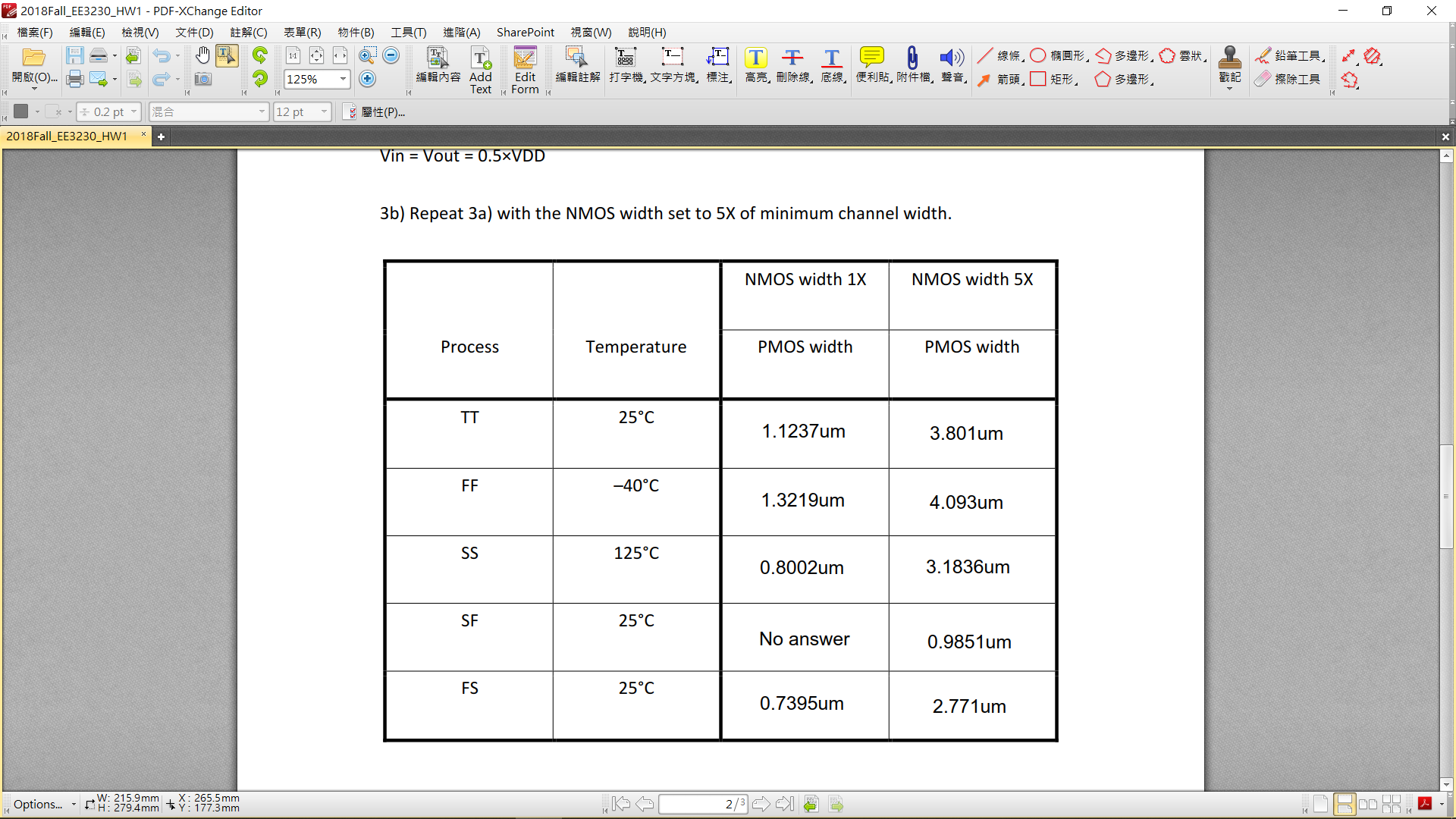
2. Draw the fabrication steps of an inverter (cross section).

Explain the “self-aligned poly-silicon gate” as well as “lightly-doped drain (LDD)”.

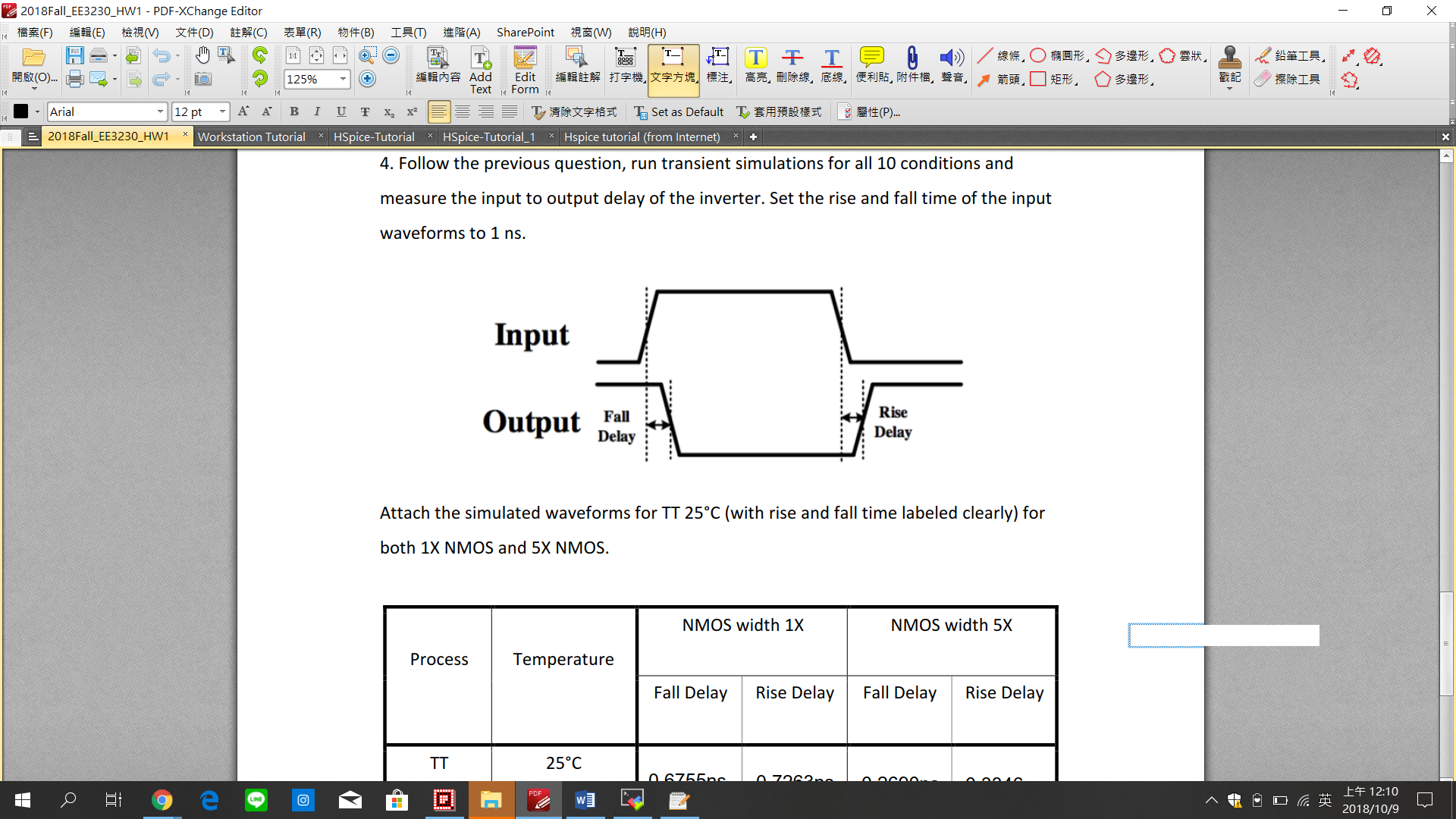


* LDD：gate愈做愈小，使得source和drain兩端的距離縮短，使得電場強度因為距離縮短而增大，因此在gate兩端接面間的載子易受到大電場而被加速，形成熱載子，造成導通。為了避免大量的熱載子產生，將gate兩旁S、D緊鄰gate的地方做輕微的摻雜，以降低熱載子效應。
* self-aligned poly-silicon gate：用refractory metal以降低gate, source/drain間的連接電阻。

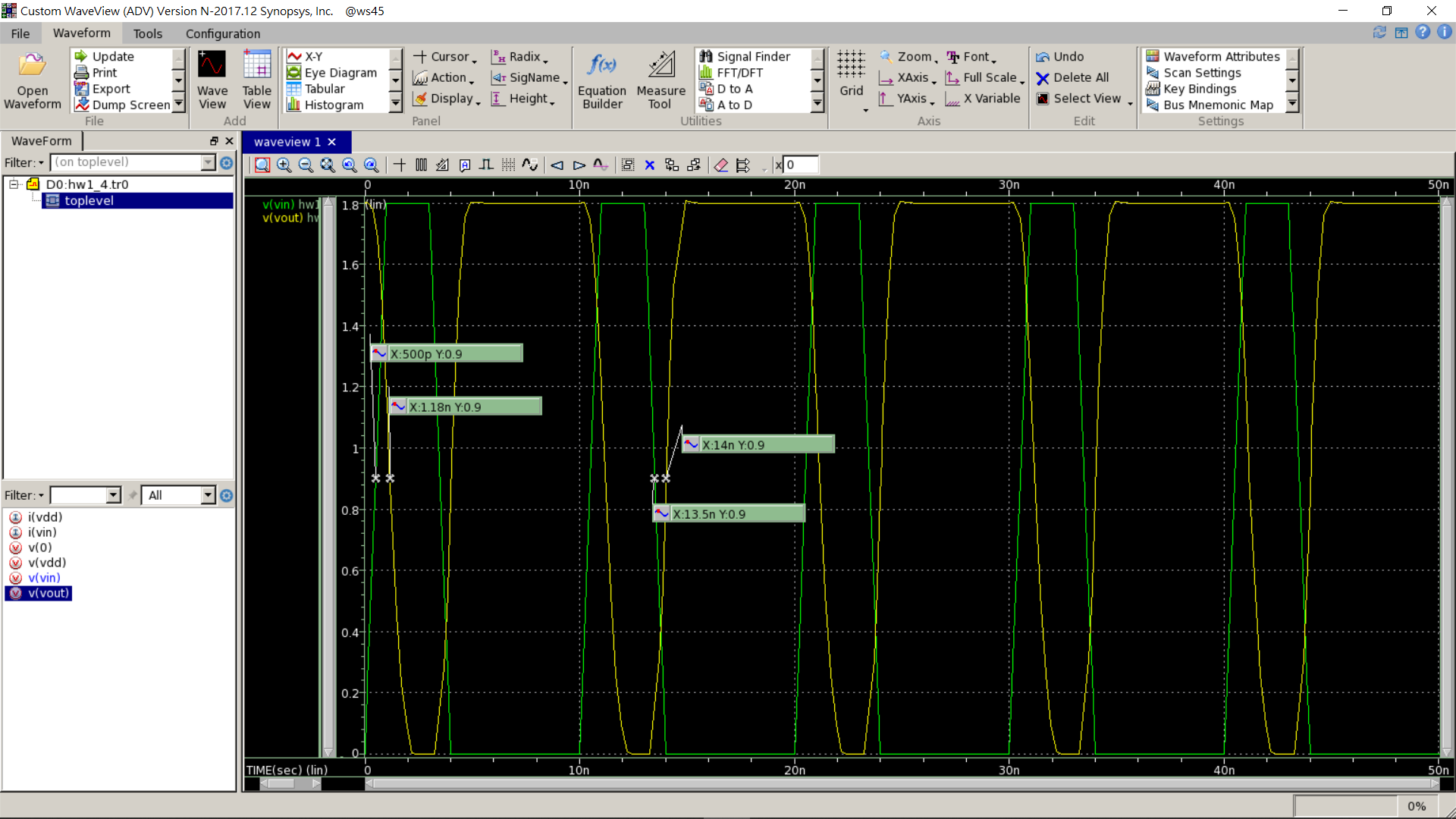
3. Please simulate and analysis a CMOS inverter



4. Follow the previous question, run transient simulations for all 10 conditions and measure the input to output delay of the inverter. Set the rise and fall time of the input waveforms to 1 ns.



* TT 25°C for 1X NMOS



* TT 25°C for 5X NMOS

