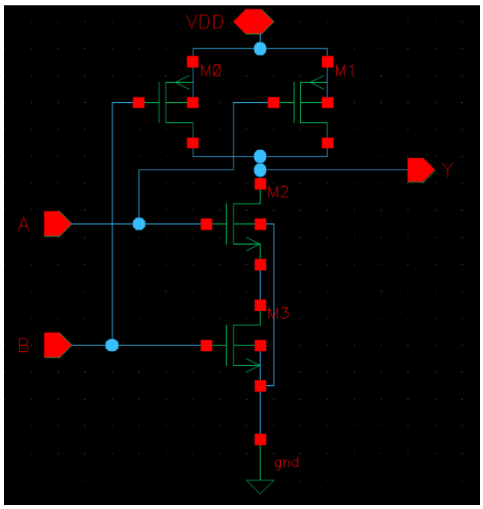
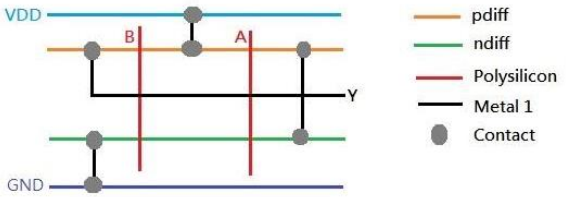
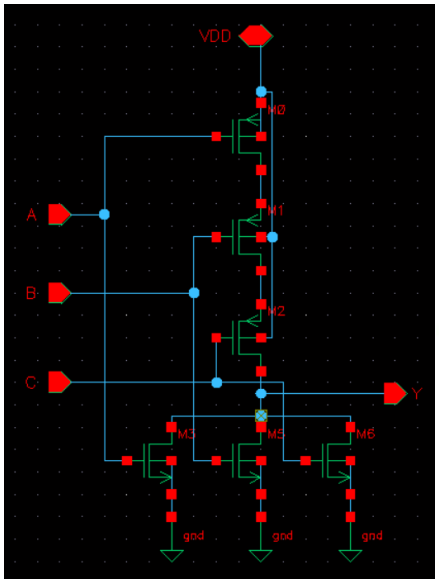
1.Use a combination of CMOS gates (in gate level symbols) and the corresponding stick diagrams to generate the following functions from A, B, and C.

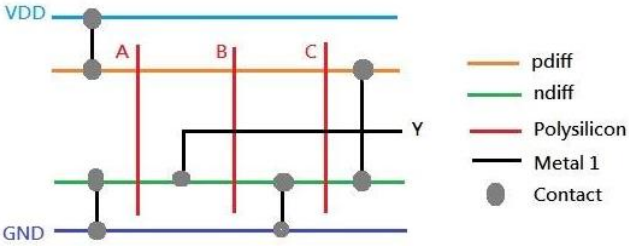
(a) Y=A'+B'(15%)



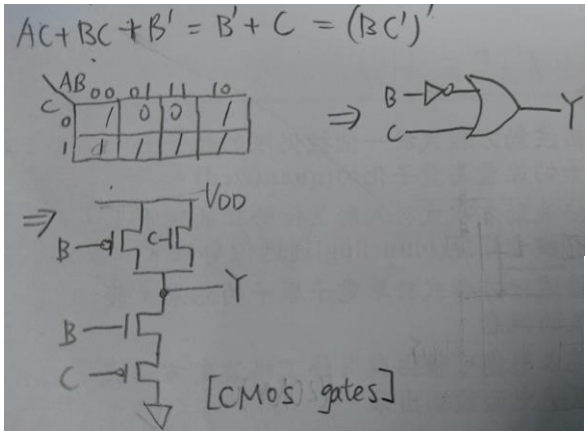


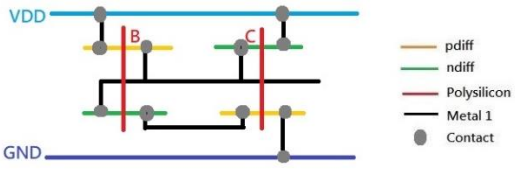
(b) Y=A'B'C'(15%)





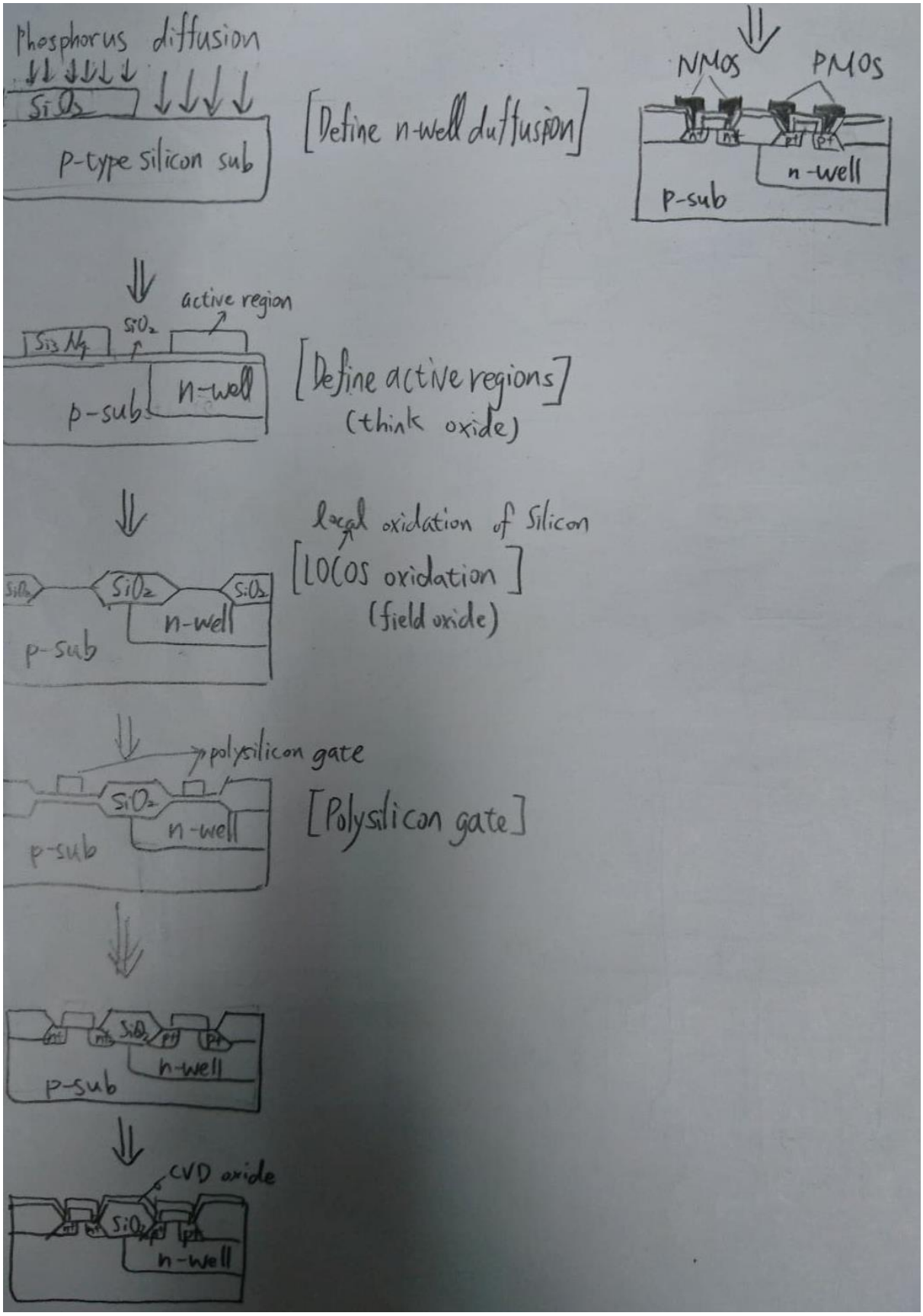
(c) Y=AC+BC+B'(15%)





2. Draw the fabrication steps of an inverter (crosssection).

Explain the “self-aligned poly-silicon gate” as well as “lightly-doped drain (LDD)”.

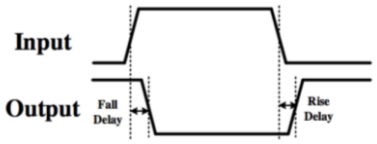


- LDD：gate 愈做愈小，使得 source 和 drain 兩端的距離縮短，使得電場強度因為距離縮短而增大，因此在 gate 兩端接面間的載子易受到大電場而被加速，形成熱載子，造成導通。為了避免大量的熱載子產生，將 gate 兩旁 S、D 緊鄰 gate 的地方做輕微的摻雜，以降低熱載子效應。
- self-aligned poly-silicon gate：用 refractory metal 以降低 gate, source/drain 間的連接電阻。

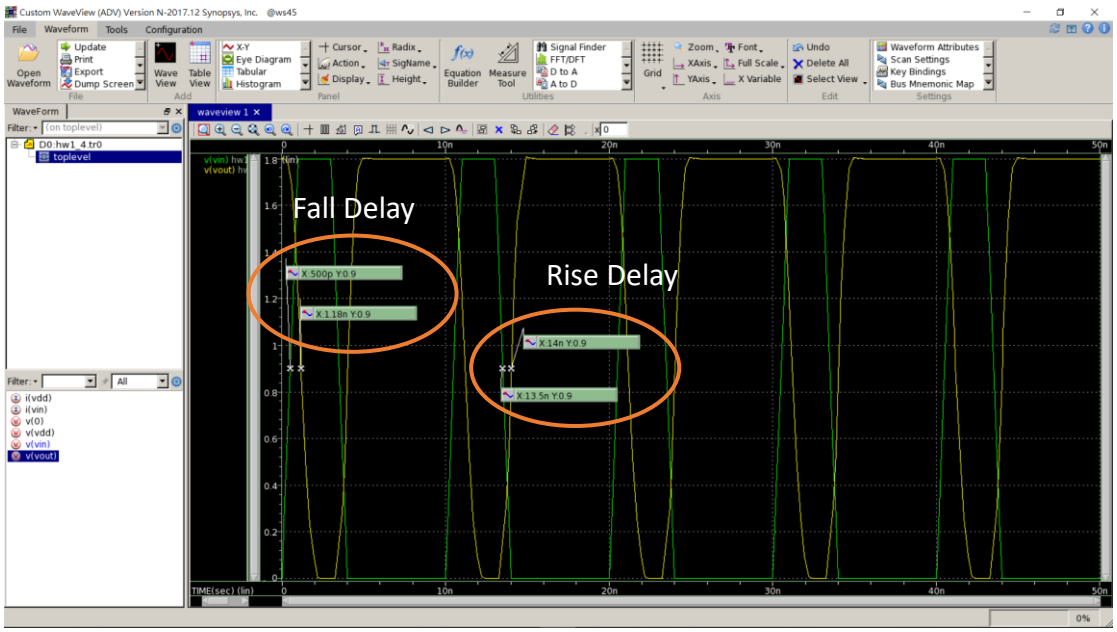
3. Please simulate and analysis a CMOS inverter

Process	Temperature	NMOS width 1X PMOS width	NMOS width 5X PMOS width
TT	25°C	1.1237um	3.801um
FF	–40°C	1.3219um	4.093um
SS	125°C	0.8002um	3.1836um
SF	25°C	No answer	0.9851um
FS	25°C	0.7395um	2.771um

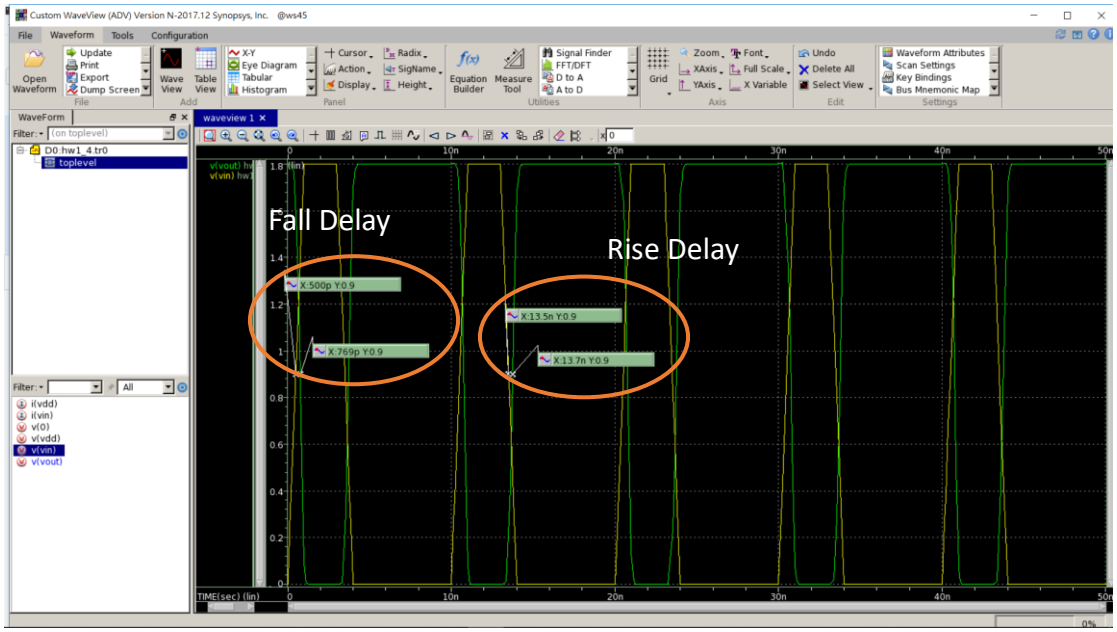
4. Follow the previous question, run transient simulations for all 10 conditions and measure the input to output delay of the inverter. Set the rise and fall time of the input waveforms to 1 ns.



- TT 25°C for 1X NMOS



- TT 25°C for 5X NMOS



Process	Temperature	NMOS width 1X		NMOS width 5X	
		Fall Delay	Rise Delay	Fall Delay	Rise Delay
TT	25°C	0.6700ns	0.5234ns	0.2690ns	0.2473ns
FF	–40°C	0.5175ns	0.4128ns	0.2105ns	0.1821ns
SS	125°C	1.686ns	0.8738ns	0.5018ns	0.4832ns
SF	25°C	No answer	No answer	0.4247ns	0.5071ns
FS	25°C	0.7570ns	0.6500ns	0.2904ns	0.2888ns