EE3230 VLSI Design (2018 Fall) HW #1

Due date: 2017/10/11 (Thursday) 10am

No plagiarism is allowed!!

1.Use a combination of CMOS gates (in gate level symbols) and the corresponding stick diagrams to generate the following functions from A, B, and C.

(a) Y=A'+B'(15%)

(b) Y=A'B'C'(15%)

(c) Y=AC+BC+B' (15%)

2. Draw the fabrication steps of an inverter (cross section).

Explain the "self-aligned poly-silicon gate" as well as "lightly-doped drain (LDD)". (35%)

3. Please simulate and analysis a CMOS inverter according to the following conditions using the model provided by TA (CIC018.l).

* Set the supply voltage to 1.8 V.
* Set the output load of this inverter to 0.1 pF.
* Use the minimum channel length for both NMOS and PMOS. 0.18um
* Use the minimum channel width for NMOS. 0.25um

3a) Find the optimal width for PMOS for a balanced trigger point of inverter in five different process/temperature corners.

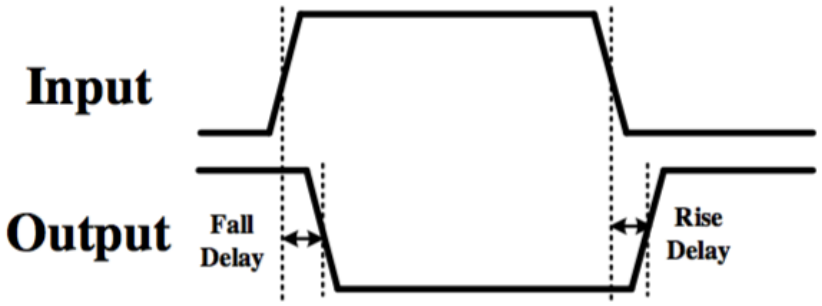
The meaning of a balanced trigger point is as the following.

Vin = Vout = 0.5×VDD

3b) Repeat 3a) with the NMOS width set to 5X of minimum channel width.

Process	Temperature	NMOS width 1X PMOS width	NMOS width 5X PMOS width
TT	25°C	1.1237um	3.801um
FF	–40°C	1.3219um	4.093um
SS	125°C	0.8002um	3.1836um
SF	25°C	No answer	0.9851um
FS	25°C	0.7395um	2.771um

4. Follow the previous question, run transient simulations for all 10 conditions and measure the input to output delay of the inverter. Set the rise and fall time of the input waveforms to 1 ns.



Attach the simulated waveforms for TT 25°C (with rise and fall time labeled clearly) for both 1X NMOS and 5X NMOS.

Process	Temperature	NMOS width 1X		NMOS width 5X	
		Fall Delay	Rise Delay	Fall Delay	Rise Delay
TT	25°C	0.6700ns	0.5234ns	0.2690ns	0.2473ns
FF	–40°C	0.5175ns	0.4128ns	0.2105ns	0.1821ns
SS	125°C	1.686ns	0.8738ns	0.5018ns	0.4832ns
SF	25°C	No answer	No answer	0.4247ns	0.5071ns
FS	25°C	0.7570ns	0.6500ns	0.2904ns	0.2888ns