

HSPICE

Source : Jh-He Lin

Speaker Jh-He Lin

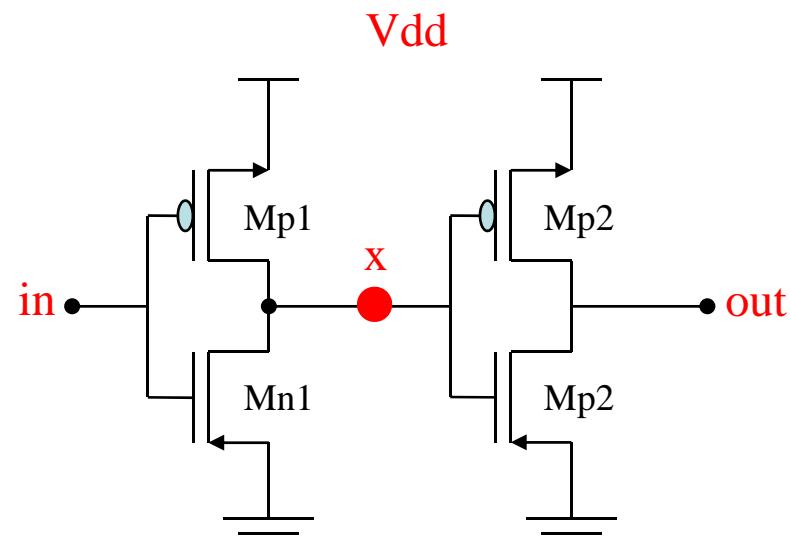
Design Flow

- Declaration
- Voltage Source
- Circuit Statements
 - Sub-circuit
- Measures
- Operation
- Others

Declaration (1/2)

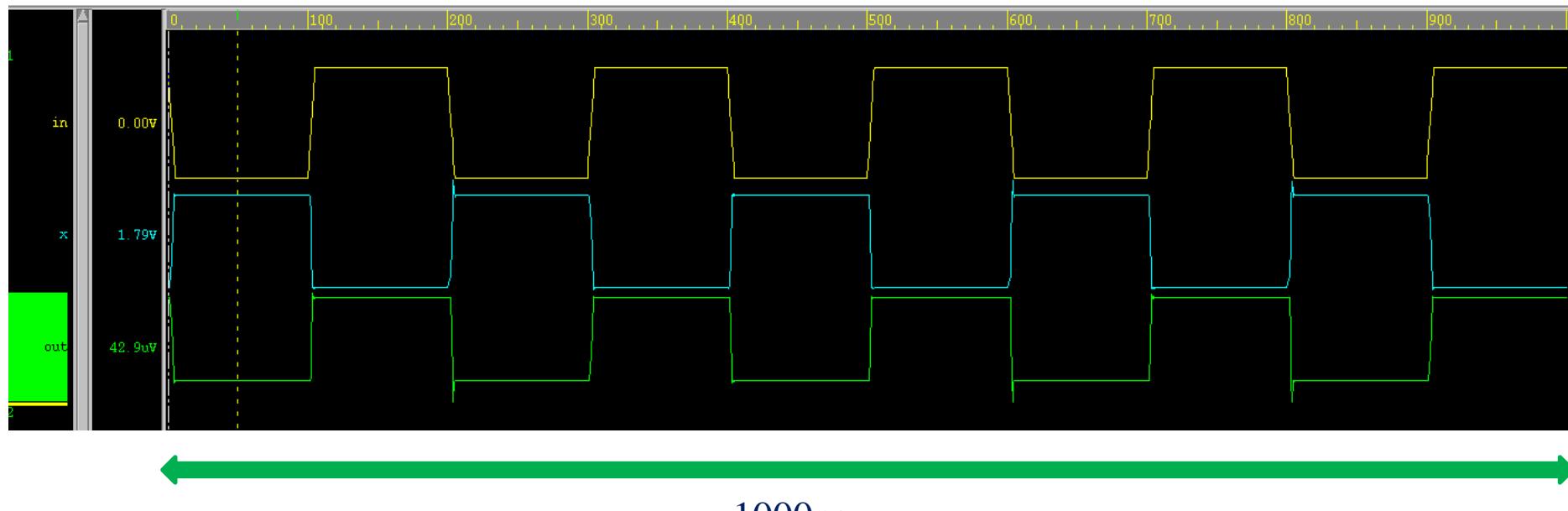
- *****example of inverter 1*****
- .LIB 'mm018.l' tt
- .GLOBAL Vdd
- .TRAN 1ns 1000ns
- .OPTION post
- *****voltage source*****
- Vsourece Vdd 0 1.8v
- Vsignal in 0 pulse(1.8v 0 0ns 5ns 5ns 95ns 200ns)
- ***** circuit statement*****
- Mp1 x in Vdd Vdd pch L=0.18u W=0.44u M=1
- Mn1 x in 0 0 nch L=0.18u W=0.22u M=1

- Mp2 out x Vdd Vdd pch L=0.18u W=0.44u M=1
- Mn2 out x 0 0 nch L=0.18u W=0.22u M=1
- *****measure*****
- .MEAS TRAN out_rise_delay TRIG v(in) VAL=0.9v TD=0 FALL=3 TARG v(x) VAL=0.9v RISE=3
- .MEAS TRAN pwr AVG POWER
- .END



Declaration (2/2)

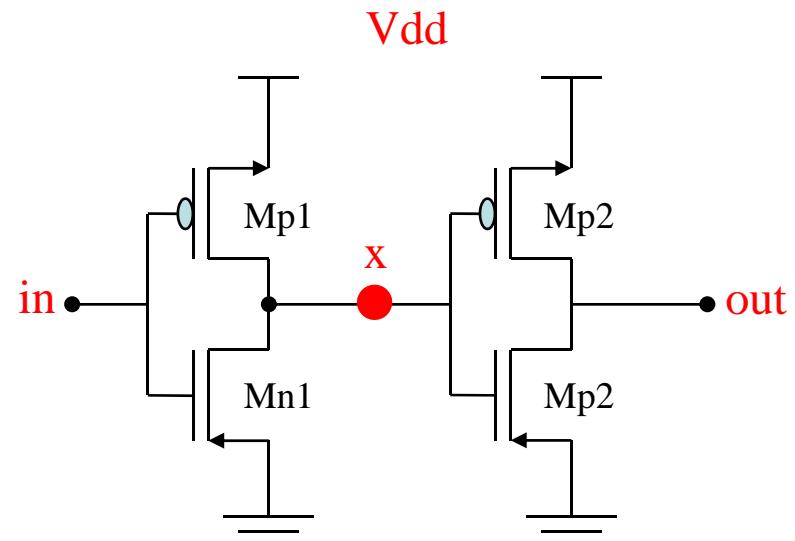
- **.LIB 'mm018.l' tt**
 - Using 0.18 technology to design
 - tt : typical model for 1.8V devices
- **.GLOBAL Vdd**
- **.TRAN 1ns 1000ns**
- **.OPTION post**



Voltage Source (1/4)

- *****example of inverter 1*****
- .LIB 'mm018.l' tt
- .GLOBAL Vdd
- .TRAN 1ns 1000ns
- .OPTION post
- *****voltage source*****
- Vsourece Vdd 0 1.8v
- Vsignal in 0 pulse(1.8v 0 0ns 5ns 5ns 95ns 200ns)
- ***** circuit statement*****
- Mp1 x in Vdd Vdd pch L=0.18u W=0.44u M=1
- Mn1 x in 0 0 nch L=0.18u W=0.22u M=1

- Mp2 out x Vdd Vdd pch L=0.18u W=0.44u M=1
- Mn2 out x 0 0 nch L=0.18u W=0.22u M=1
- *****measure*****
- .MEAS TRAN out_rise_delay TRIG v(in) VAL=0.9v TD=0 FALL=3 TARG v(x) VAL=0.9v RISE=3
- .MEAS TRAN pwr AVG POWER
- .END



Voltage Source (2/4)

■ Syntax

Vxxx n+ n- <<DC=>dcval>

Iyyy n+ n- <<DC=>dcval>

■ Example

V1 node1 0 DC=5v

V2 node2 0 5v

I3 node3 0 3mA

Voltage Source (3/4)

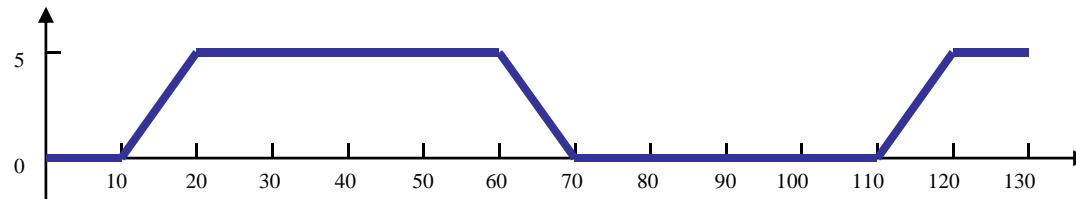
■ Pulse source function: PULSE

□ Syntax

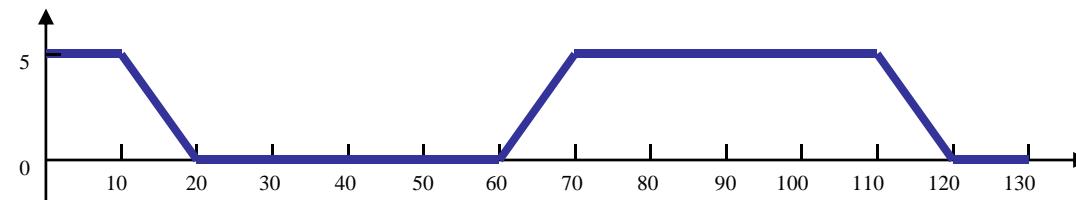
PULSE (V1 V2 Tdelay Trise Tfall duty_cycle_width Period)

□ Example

V1 node1 node2 **PULSE** (0V 5V 0ns 10ns 10ns 40ns 100ns)



V2 node3 node4 **PULSE** (5V 0V 0ns 10ns 10ns 40ns 100ns)



Voltage Source (4/4)

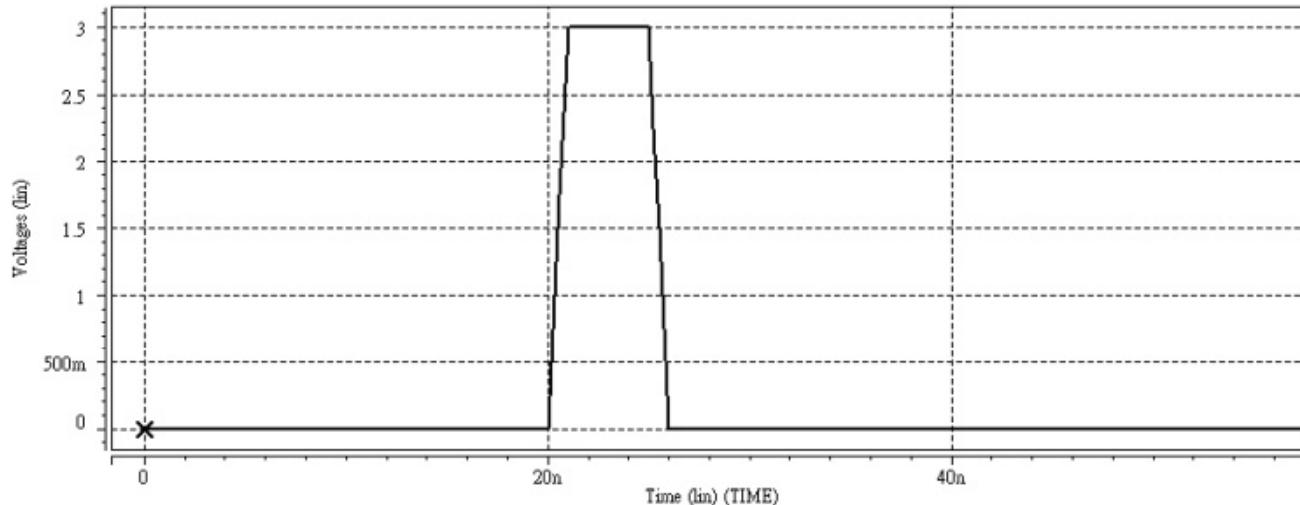
- Piecewise linear source function: PWL

- Syntax

PWL (t1 v1, t2 v2,)

- Example

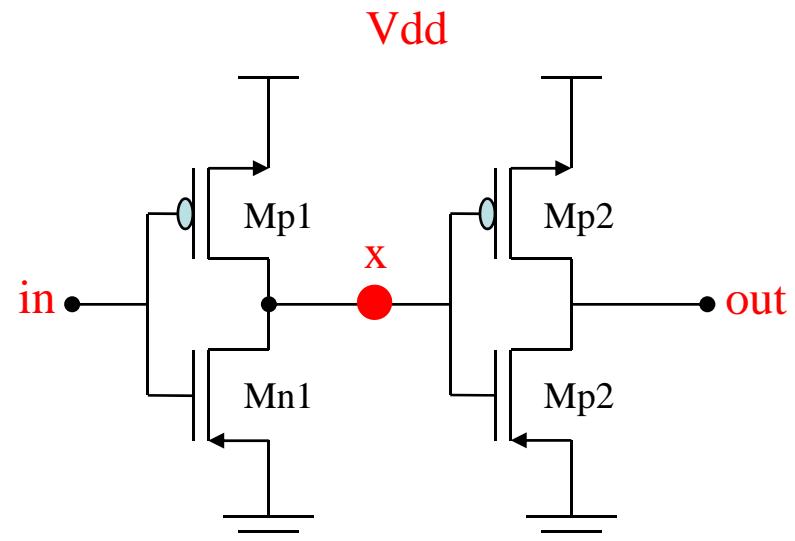
V1 node1 0 PWL (0n 0v, 20n 0v, 21n 3v, 25n 3v, 26n 0v,30n 0v)



Circuit Statements (1/5)

- *****example of inverter 1*****
- .LIB 'mm018.l' tt
- .GLOBAL Vdd
- .TRAN 1ns 1000ns
- .OPTION post
- *****voltage source*****
- VsOURCE Vdd 0 1.8v
- VsIGNAL in 0 pulse(1.8v 0 0ns 5ns 5ns 95ns 200ns)
- ***** circuit statement*****
- Mp1 x in Vdd Vdd pch L=0.18u W=0.44u M=1
- Mn1 x in 0 0 nch L=0.18u W=0.22u M=1

- Mp2 out x Vdd Vdd pch L=0.18u W=0.44u M=1
- Mn2 out x 0 0 nch L=0.18u W=0.22u M=1
- *****measure*****
- .MEAS TRAN out_rise_delay TRIG v(in) VAL=0.9v TD=0 FALL=3 TARG v(x) VAL=0.9v RISE=3
- .MEAS TRAN pwr AVG POWER
- .END



Circuit Statements (2/5)

■ Instance and element names

• C	Capacitor	 [Cxxx Node1 Node2 Value]
• D	Diode	 [Ixxx Node1 Node2 Value]
• E,F,G,H	Dependent current and voltage controlled source	 [Lxxx Node1 Node2 Value]
• I	Current	 [Mxxx D G S B Type L=val W=val M=val]
• J	JFET or MESFET	 [Rxxx Node1 Node2 Value]
• K	Mutual inductor	 [Vxxx Node1 Node2 Value]
• L	Inductor	
• M	MOSFET	
• Q	BJT	
• R	Resistor	
• O,T,U	Transmission line	
• V	Voltage source	
• X	Subcircuit call	

Circuit Statements (3/5)

■ Units

- Ohm *Resistance
- Farad *Capacitor

- Henry *Inductor

■ Scales

- T 10^{12}
- G 10^9
- Meg 10^6
- K 10^3

- M 10^{-3}
- U 10^{-6}
- N 10^{-9}
- P 10^{-12}
- F 10^{-15}

Circuit Statements (4/5)

■ MOSFET element

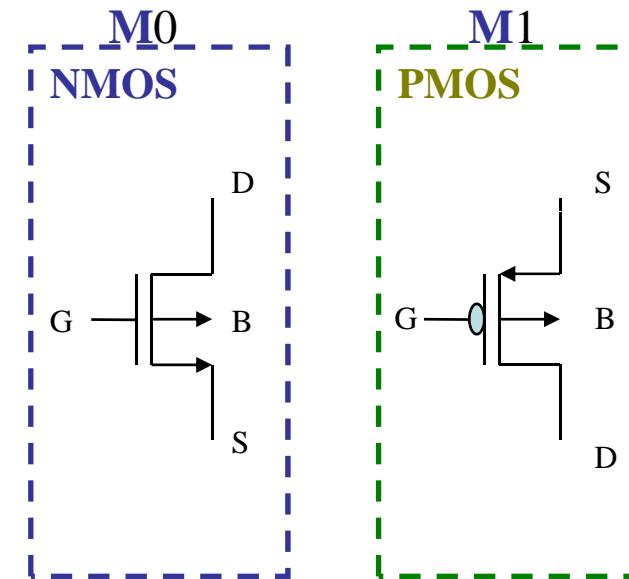
□ Syntax

Mxxx nd ng ns nb *mname* <**L=val**> <**W=val**> <**M=val**>

□ Example

M0 d0 g0 s0 b0 **nch** **L=0.18u** **W=0.22u** **M=1**

M1 d1 g1 s1 b1 **pch** **L=0.18u** **W=0.22u** **M=4**



Circuit Statements (5/5)

****resistance “R”****

R1 node1 node2 10k

****voltage source “V”****

V4 node3 node4 1v

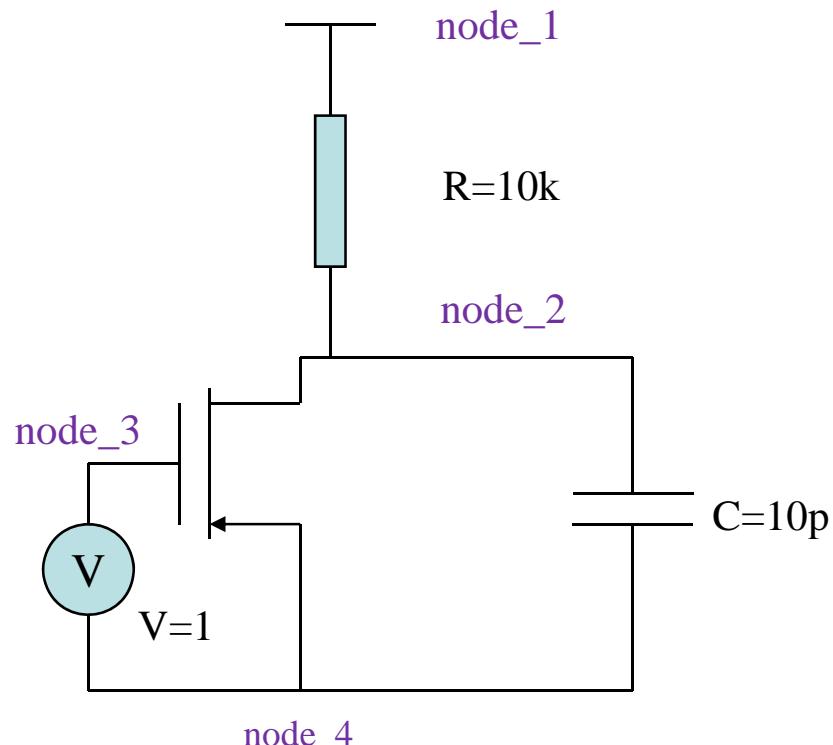
****capacitor “C”****

C2 node2 node4 10p

****MOS “M”****

M3 node2 node3 node4 node4

(+ nch W=0.22u L=0.18u M=1



SUBCKT of Circuit Statement(1/3)

■ .SUBCKT statement

□ **.SUBCKT** subname Node1 <Node2 ... >

- The following are not included in node
 - Ground node (**0**)
 - Nodes are assigned by .GLOBAL statement
 - **.ENDSNodes** are assigned by using BULK=node in MOSFET or BJT models
- Param is used only in sbucircuit and it can be overridden by subckt call or values in .PARAM statement

□ Subcircuit calls example

.XInstantName n1 <n2 n3> SubcktName <param=val> <**M**=val>

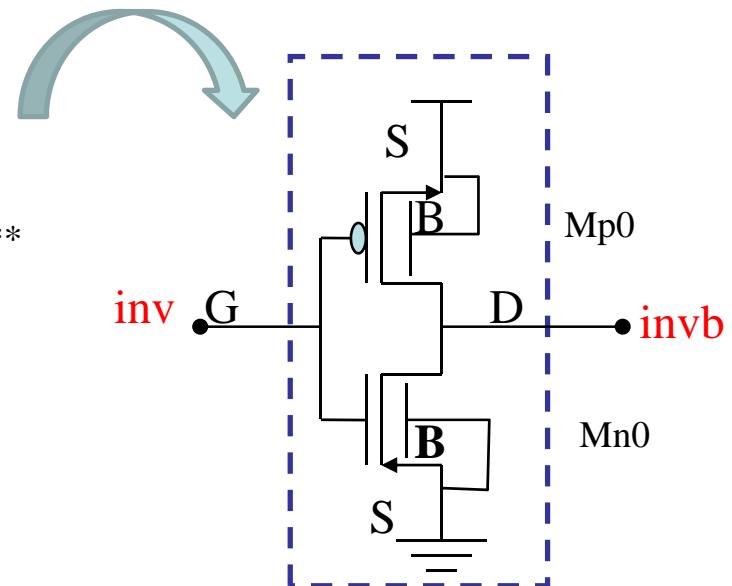
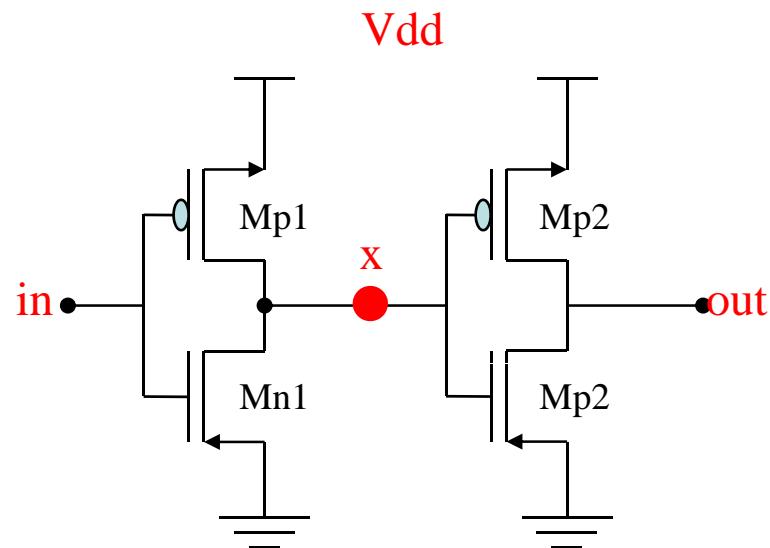
.Xadd1 n1 n2 n3 n4 n5 FA WN=3u LN=1u **M**=3

.xnmos1 1 2 3 4 nos Wsize=0.2u Lsize=0.18u **M**=2

$$W = WN$$

SUBCKT of Circuit Statement(2/3)

- *****SUBCKT statement*****
- .SUBCKT inverter inv invb
- Mp0 invb inv Vdd Vdd pch L=0.18u W=0.66u M=1
- Mn0 invb inv 0 0 nch L=0.18u W=0.22u M=1
- .ENDS inverter
- *****circuit statement*****
- Xinv1 in x inverter
- Xinv2 x out inverter



SUBCKT of Circuit Statement(3/3)

- ***** circuit statement*****
- .SUBCKT inverter inv invb
- Mp1 x in Vdd Vdd pch L=0.18u W=0.44u M=1
- Mn1 x in 0 0 nch L=0.18u W=0.22u M=1

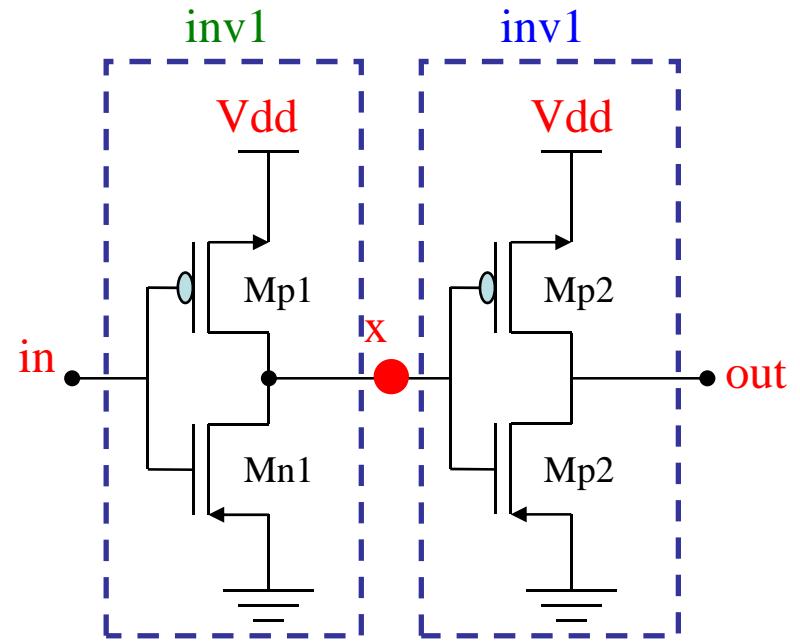
- Mp2 out x Vdd Vdd pch L=0.18u W=0.44u M=1
- Mn2 out x 0 0 nch L=0.18u W=0.22u M=1



- *****SUBCKT statement*****
- .SUBCKT inverter inv invb
- Mp0 invb inv Vdd Vdd pch L=0.18u W=0.66u M=1
- Mn0 invb inv 0 0 nch L=0.18u W=0.22u M=1
- .ENDS inverter
- *****circuit statement*****
- Xinv1 in x inverter
- Xinv2 x out inverter

Measures (1/4)

- *****example of inverter 2*****
- .LIB 'mm018.l' tt
- .OPTION post
- .GLOBAL Vdd
- .TRAN 1ns 1000ns
- *****voltage source*****
- Vsourece Vdd 0 1.8v
- Vsignal in 0 pulse(1.8v 0 0ns 5ns 5ns 95ns 200ns)
- *****SUBCKT statement*****
- .SUBCKT inverter inv invb
- Mp0 invb inv Vdd Vdd pch L=0.18u W=0.66u M=1
- Mn0 invb inv 0 0 nch L=0.18u W=0.22u M=1
- .ENDS inverter
- *****circuit statement*****
- Xinv1 in x inverter
- Xinv2 x out inverter
- *****measure*****
- .MEAS TRAN out_rise_delay TRIG v(in) VAL=0.9v TD=0 FALL=3 TARG v(x) VAL=0.9v RISE=3
- .MEAS TRAN pwr AVG POWER
- .END



Measures (2/4)

■ Syntax

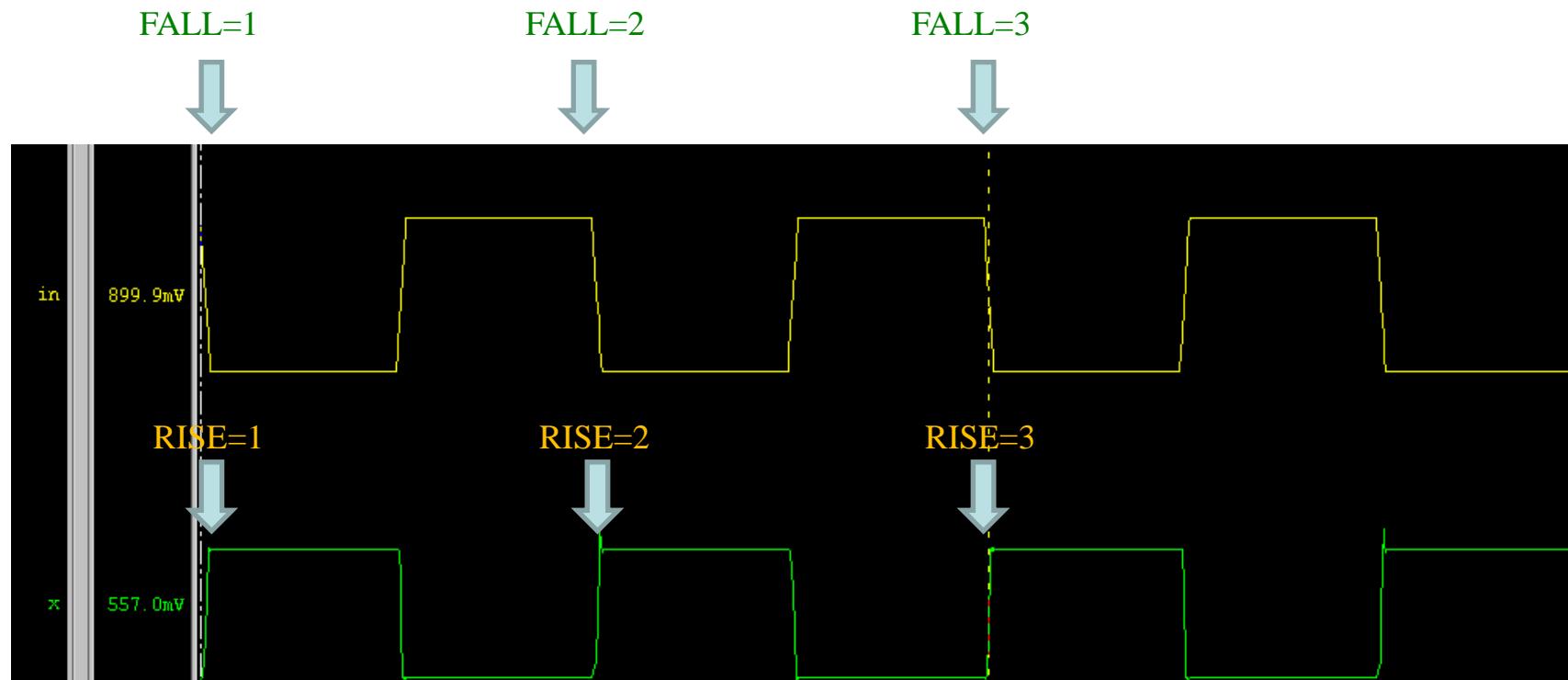
- **.MEASURE TRAN** result **TRIG...** **TARG...**
 - **result:** name is given the measured value in HSPICE output
 - **TRIG... :** **TRIG** trig_var **VAL**=trig_value <**TD**=time_delay> <**RISE**=n> +<**FALL**=n>
- **.TRAN power AVG POWER**

■ Example

- **.MEAS TRAN** result1 **TRIG** v(in) **VAL**=2v **RISE**=2 **TARG** v(out) **VAL**=1.5v **FALL**=1
- **.MEAS TRAN pwr AVG POWER**

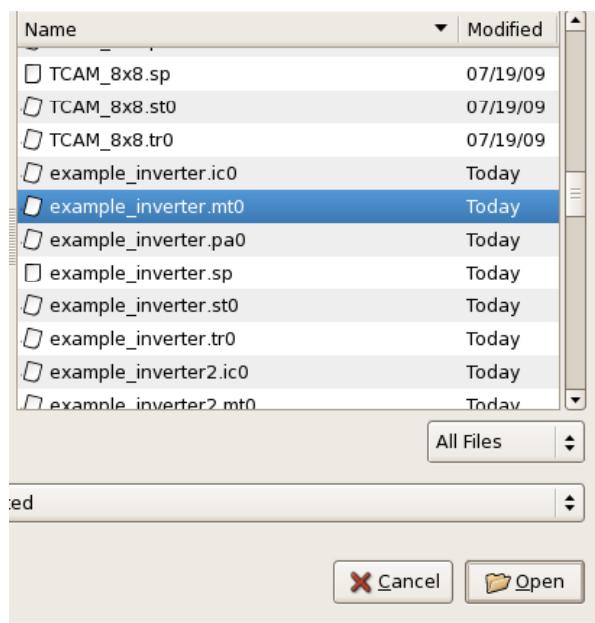
Measures (3/4)

- *****measure*****
- .MEAS TRAN out_rise_delay TRIG v(in) VAL=0.9v TD=0 FALL=3 TARG v(x) VAL=0.9v RISE=3



Measure (4/4)

- .MEAS TRAN pwr AVG POWER
- .END



An HSPICE editor window showing a script with measurement commands:

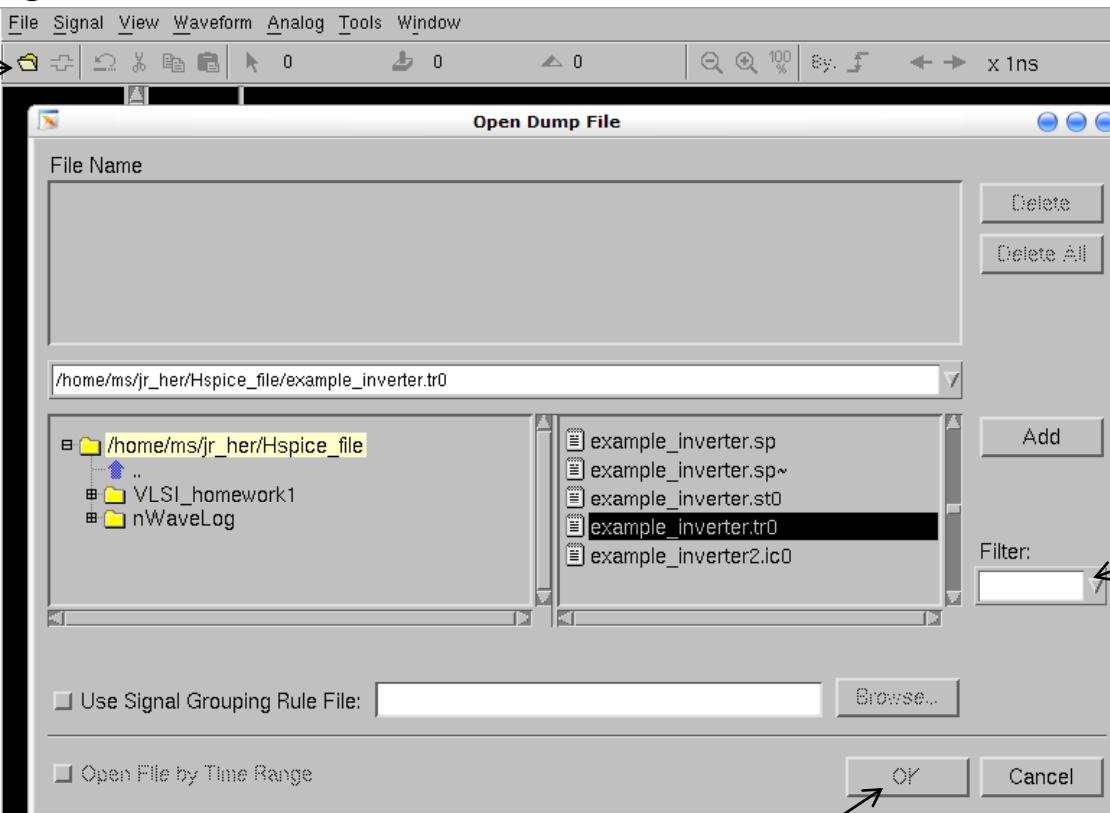
```
$DATA1 SOURCE='HSPICE' VERSION='Z-2007.03-SP1'
.TITLE '*****example of inverter 2*****'
out_rise_delay    pwr          temper        alter#
2.448e-10    6.048e-07    25.0000    1.0000
```

Operation (1/3)

■ .OPTION post

- Creating a “.tr0” file to view waveform

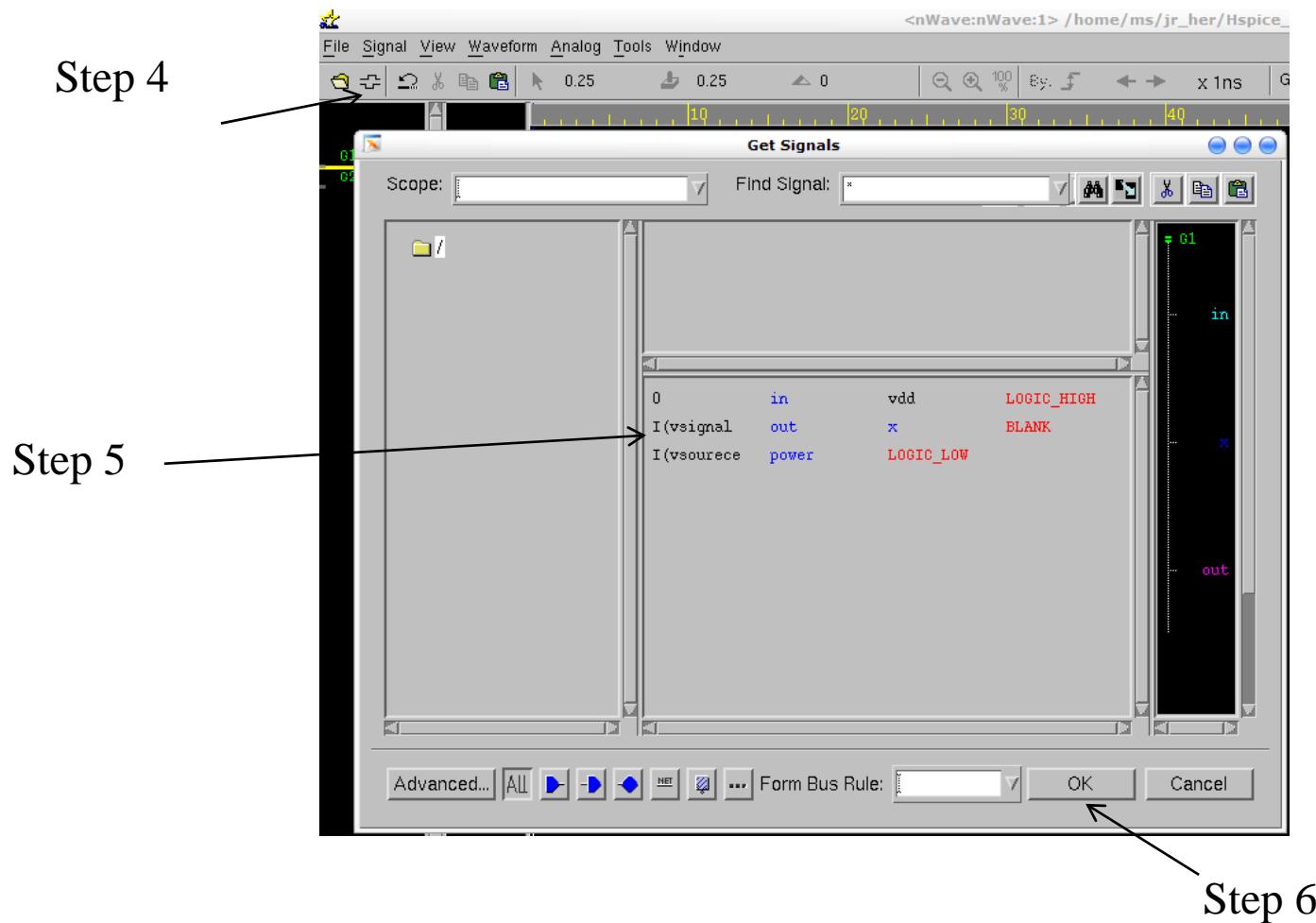
Step 1



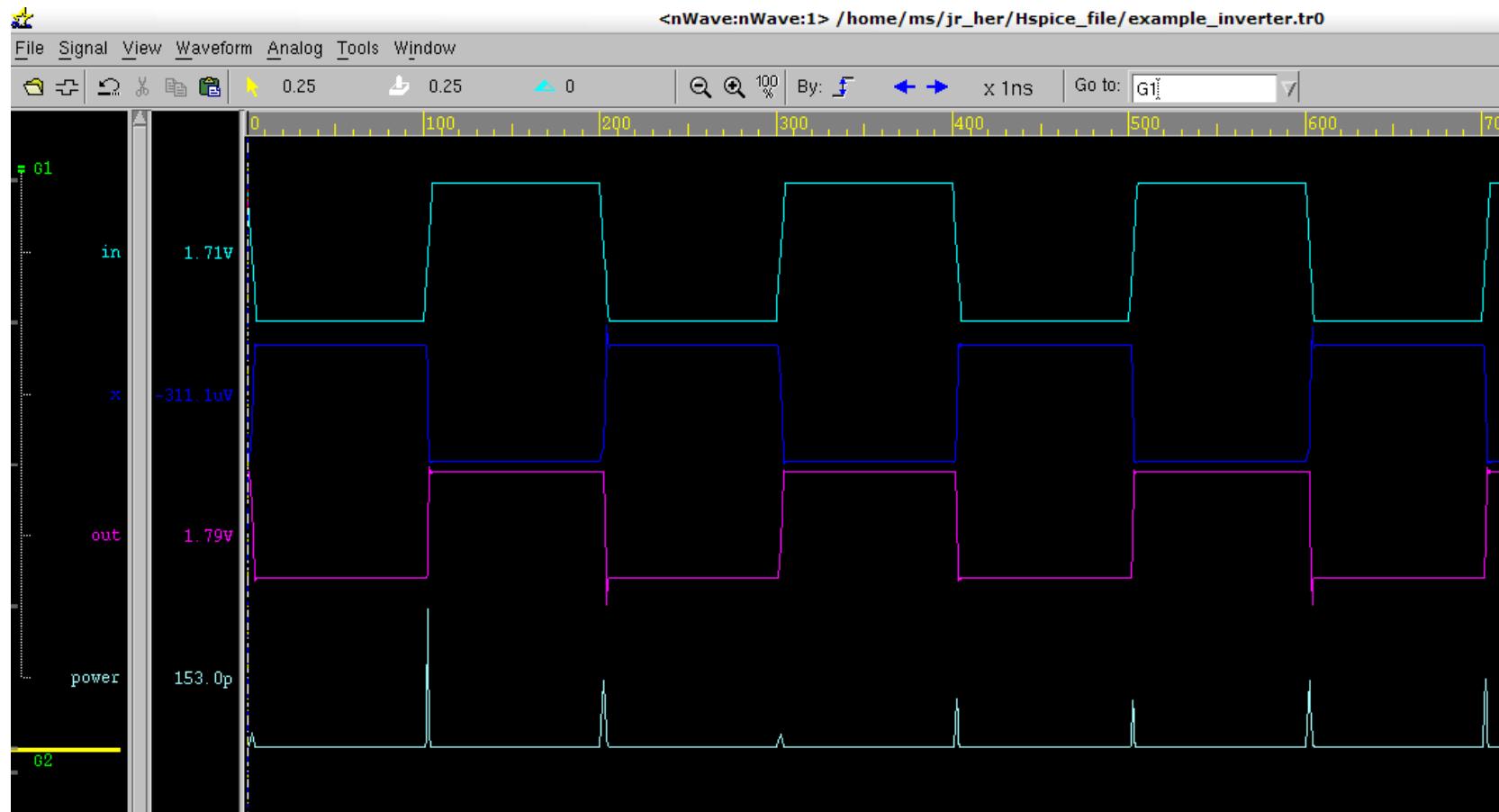
Step 2

Step 3

Operation (2/3)



Operation (3/3)



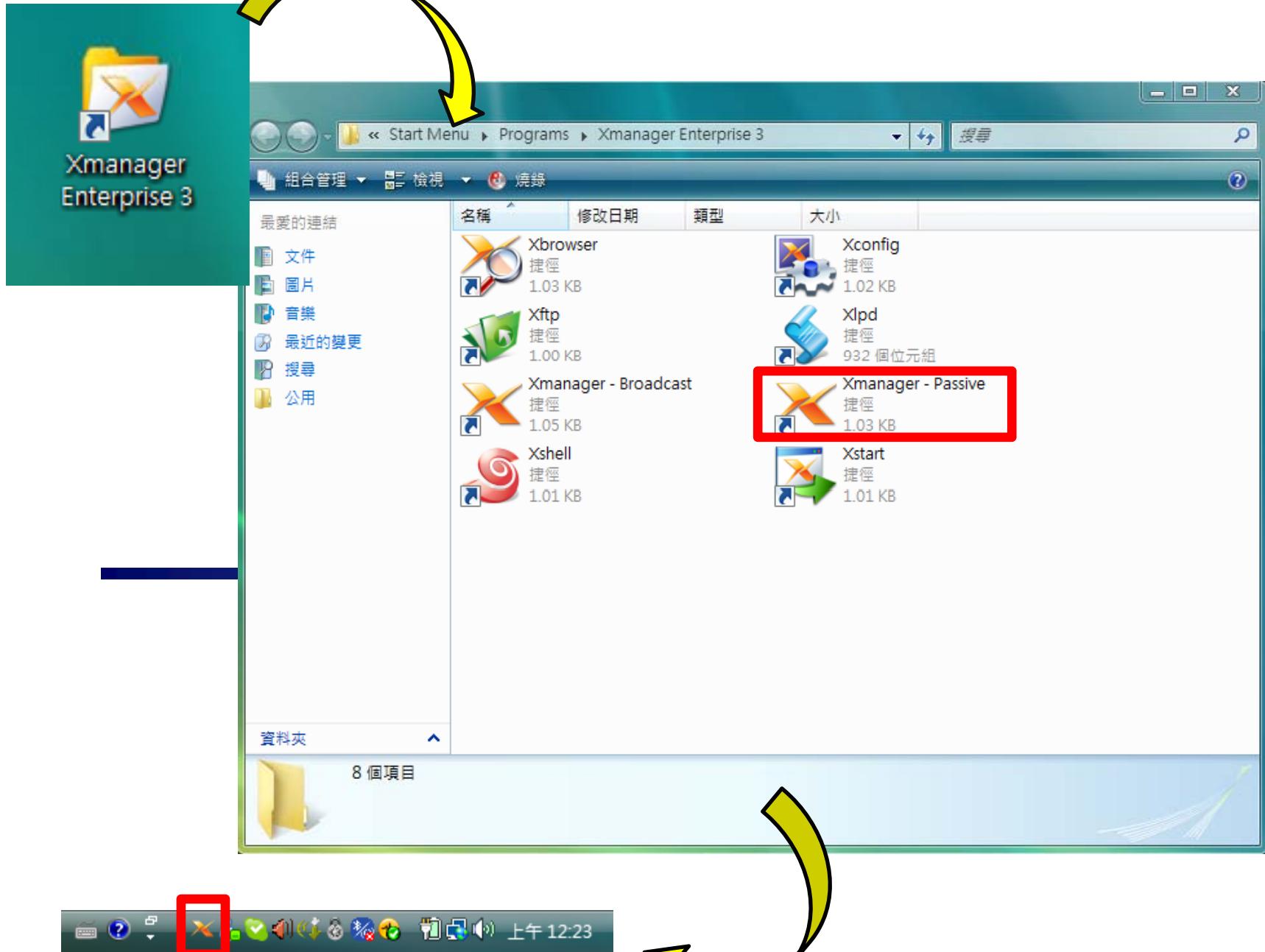
Others

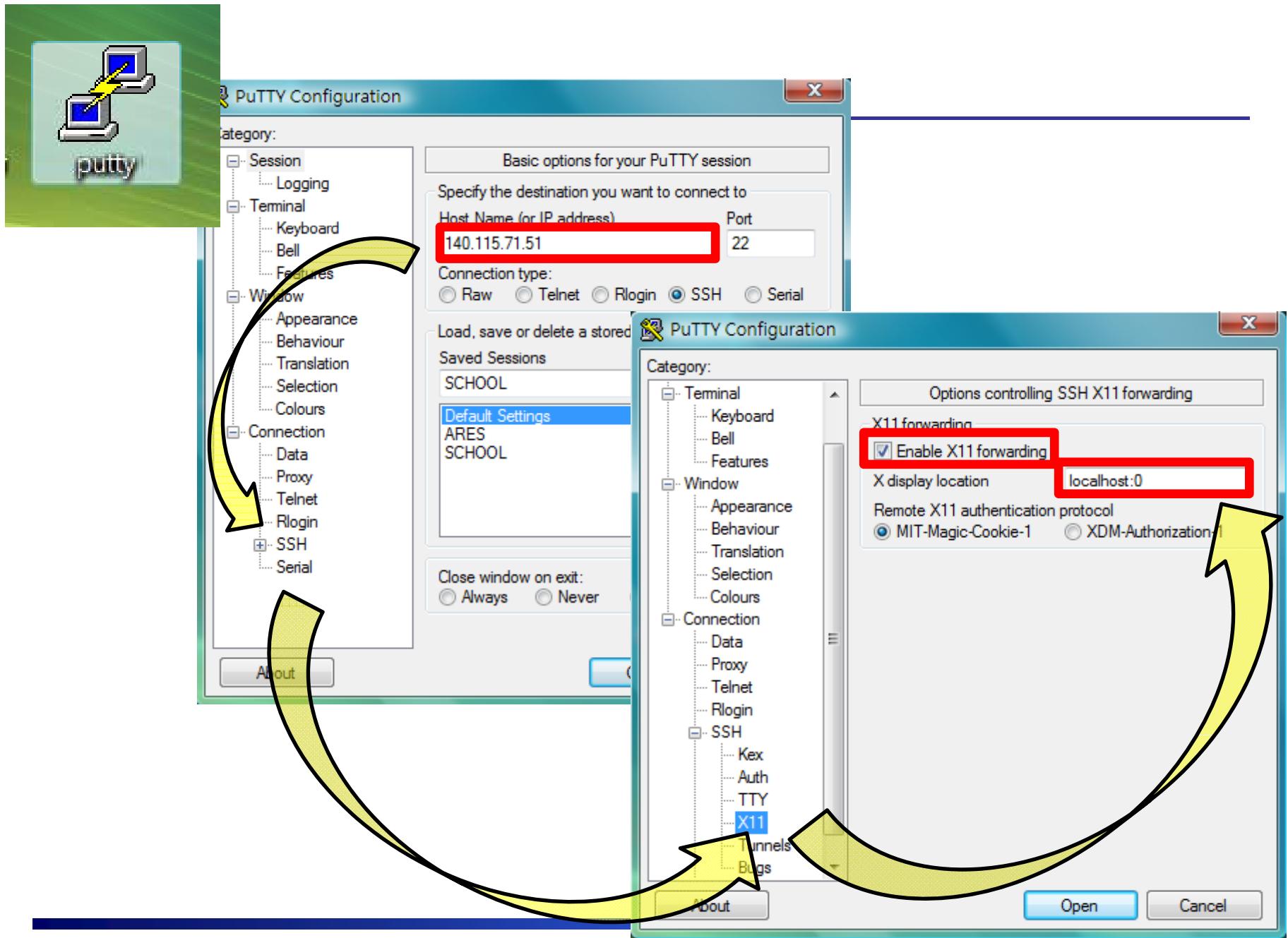
- Minimum width size is 0.22u (in meter)
- Minimum length size is 0.18u (in meter)
- Capital and lowercase are equivalence in HSPICE
- 0 and GND are equivalence
 - Vsourece Vdd 0 1.8v
 - Vsourece Vdd GND 1.8v

工作站指令教學

Source : 侯致聖

Speaker : 吳冠德





帳號

密碼

```
140.115.71.51 - PuTTY
login as: mimiboy
mimiboy@140.115.71.51's password: [REDACTED]
```

```
140.115.71.51 - PuTTY
+-----+
Any question or problem, please go to 417 and ask mongy
*****NOTE*****
*  
*****  
<1> Please limit your hard disk space up to 2GB  
<2> Don't run multi jobs for single project  
  
+-----+
server No. | CPU | Mem.  
cae01      1x1.2GHz  1.5GB  
cae04      1x1.6GHz  2 GB'  
cae09      1x1.2GHz  4 GB  
cae11      1x1.2GHz  3 GB  
cae14      2x1.6GHz  2 GB  
cae15      4x1.2GHz  16GB  
cae18      1x1.2GHz  2 GB  
cae21      2x1.5GHz  2 GB  
cae24      1x1.6GHz  2 GB'  
cae25      1x1.6GHz  2 GB'  
cae34      1x1.2GHz  2 GB  
cae35      1x1.2GHz  2 GB  
cae36      2x1.2GHz  6 GB
```

```
[cae01]/usr2/grad98/mimiboy <mimiboy> [REDACTED]
```

工作站環境介紹

■ 工作站與IP對照表

Hostname	IP
cae01	140.115.71.51
cae04	140.115.71.54
cae09	140.115.71.59
cae14	140.115.71.64
cae18	140.115.71.68
cae24	140.115.71.74
cae25	140.115.71.75
<i>Cae27 (NIS)</i>	140.115.71.77
<i>Cae28 (NFS)</i>	140.115.71.78
cae33	140.115.71.83
cae34	140.115.71.84
cae35	140.115.71.85
cae36	140.115.71.86

vi 文書編輯軟體

■ 在終端機執行

- vi
- vi filename

■ vi 模式

- 一般模式 與 編輯模式

➤ 一般模式

- 用方向鍵移動游標
- x(X) 刪除後面(前面)的字
- dd 刪除一整行
- v 標記範圍
- y 複製(yy 複製該行)
- p 貼上
- u 復原
- Ctrl+r 重作

➤ 編輯模式

- i 插入(在游標字元前)
- a 插入(在游標字元後)
- o 覆蓋
- [Esc] 離開編輯模式

基本指令

- cd
 - 目錄資料夾切換
- ls
 - 列出有關檔案（file）及目錄（directory）的資訊
- pwd
 - 列出目前所在位置
- cp
 - 複製檔案
- mv
 - 搬移檔案或是重新命名
- rm
 - 刪除檔案或是資料夾
- mkdir
 - 建立資料夾
- rmdir
 - 移除空的資料夾
- ps
 - 列出所有執行程式
- kill
 - 刪除執行的程式
- tar
 - 壓縮解壓縮程式
- passwd
 - 變更使用者密碼

基本指令 (1/12)

■ cd

□ cd xxx

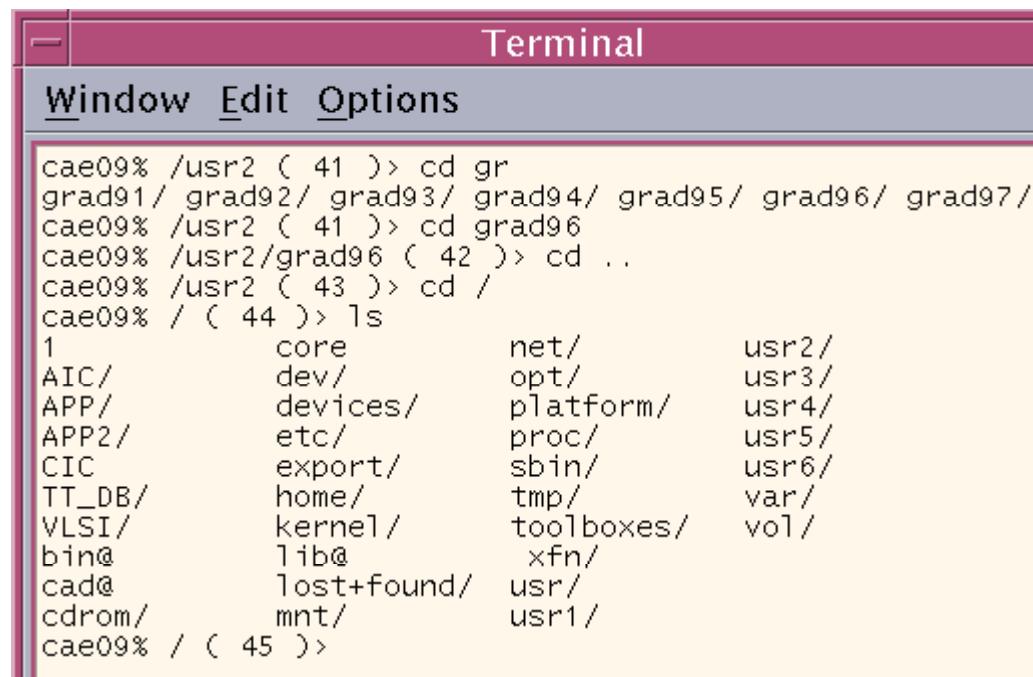
切換到xxx的資料夾

□ cd ..

回到上一層的資料夾

□ cd /

回到根目錄



The screenshot shows a terminal window titled "Terminal". The window has a menu bar with "Window", "Edit", and "Options". The main area displays a directory listing with the command "ls". The output shows the following directory structure:

```
cae09% /usr2 ( 41 )> cd gr
grad91/ grad92/ grad93/ grad94/ grad95/ grad96/ grad97/
cae09% /usr2 ( 41 )> cd grad96
cae09% /usr2/grad96 ( 42 )> cd ..
cae09% /usr2 ( 43 )> cd /
cae09% / ( 44 )> ls
1 core net/ usr2/
AIC/ dev/ opt/ usr3/
APP/ devices/ platform/ usr4/
APP2/ etc/ proc/ usr5/
CIC export/ sbin/ usr6/
TT_DB/ home/ tmp/ var/
VLSI/ kernel/ toolboxes/ vol/
bin@ lib@ xfn/
cad@ lost+found/ usr/
cdrom/ mnt/ usr1/
cae09% / ( 45 )>
```

基本指令 (2/12)

■ ls

● ls -l 所顯示的檔案或目錄格式如下：

-rw-r----	1	ucat	dynix	18417	Jan 23 24:00	catalog.doc
檔案性質與權限	連結檔案數量	擁有此檔案的人	擁有此檔案的群體	檔案大小	最後修改日期與時間	檔案名稱

有關檔案性質與權限共有十個字元，可分為四組如下：

d	r w x	r w x	r w x
檔案(-)/目錄(d)	擁有人的權限	擁有團體的權限	他人的使用權限

其中：

r	read	可查看此檔案或目錄的內容
w	write	可更改此檔案或目錄的內容
x	execute	可執行此檔案
-		不具此權限

例如：“-rwxrwx---” 表示其是為一個檔案，此檔案的擁有人及擁有團體可以讀、寫、與執行此檔案，而其他非同一團體的人則完全沒有權限讀、寫、或執行此檔案。

基本指令 (3/12)

■ pwd

```
cae09% / ( 45 )> cd usr2/grad96/
afree/      ct/      helofox/  omega3/    tmp002/
alpha/      cwchang/ hsiny/    ponin/    tmp003/
ansgoing/   d3501017/ jun901/   ritama/   tseng/
applelee/   d3501092/ jyhong/  rogmark/  tzuo1012/
b9201027/   dragon/   ken/     sam1201/  usefun/
bbpow/      dsefkn/   kimi4231/ sapidog/  vd96/
binghung/   eda0612/  lawalaua/ shanglu/  weiciang/
brain/      garbo/   lkz/     shen/     winson/
caspar/     ggbetty/  maple/   sip04/    yuchia/
changwc/   gyamwoo/ mark1101/ temp01/   zack7465/
cloudyu/   handyc/  maxwellf/ thunder/
csk618/    headrun/ mikeeee/ tmp001/
cae09% / ( 45 )> cd usr2/grad96/ct/
CDS.log          LVS.tar        d3501101/
CDS.log.1        LVS/          hspice/
CDS.log.2        Mail/         ic_contest/
CDS.log.3        PDK13.tar    libManager.log
CDS.log.4        PDK13D/      libManager.log.1
CSHRC            PEX.tar      nsmail/
DRC.tar          PEX/         panic.log
DRC/             command.log temp/
DRE_CDS.log     core
DRE_CDS.log.1   d3501064/
cae09% / ( 45 )> cd usr2/grad96/ct/hspice/
cae09% /usr2/grad96/ct/hspice ( 46 )> pwd
/usr2/grad96/ct/hspice
cae09% /usr2/grad96/ct/hspice ( 47 )>
```

■ 目前所在位置



基本指令 (4/12)

■ cp

□ cp 來源檔案 目的檔案

```
cp abc.txt xyz.txt
```

□ cp 來源檔案 目的路徑

```
cp /usr3/abc.txt ~/document/
```

```
cp /usr3/abc.txt .
```

□ cp 來源檔案 路徑/目的檔案

```
cp /usr3/abc.txt ~/document/xyz.txt
```

□ cp -r 來源資料夾 路徑/

```
cp -r /usr3/tf/ ~/document/
```

```
cp -r /usr3/tf/ ~/document/035tf/
```

基本指令 (5/12)

■ mv

□ mv 來源檔案 目標檔案

mv abc.txt abc.txt.old

□ mv 來源檔案 路徑/目標檔案

mv abc.txt ~/document/abc.txt

□ mv 來源資料夾 目標資料夾

mv folder/ work/

□ mv 來源資料夾 路徑/目標資料夾

mv folder/ ~/document/work/

基本指令 (6/12)

■ rm

□ rm 移除檔案

rm abc.txt

rm ~/document/abc.txt

□ rm -r 移除資料夾

rm -r ~/document/

基本指令 (7/12)

■ Mkdir

□ mkdir 欲建立的名稱

mkdir temp

mkdir temp_34

mkdir temp-34 (不好)

□ mkdir 路徑/欲建立的名稱

mkdir ~/temp/

基本指令 (8/12)

■ rmdir

□ rmdir 欲刪除的資料夾

rmdir temp

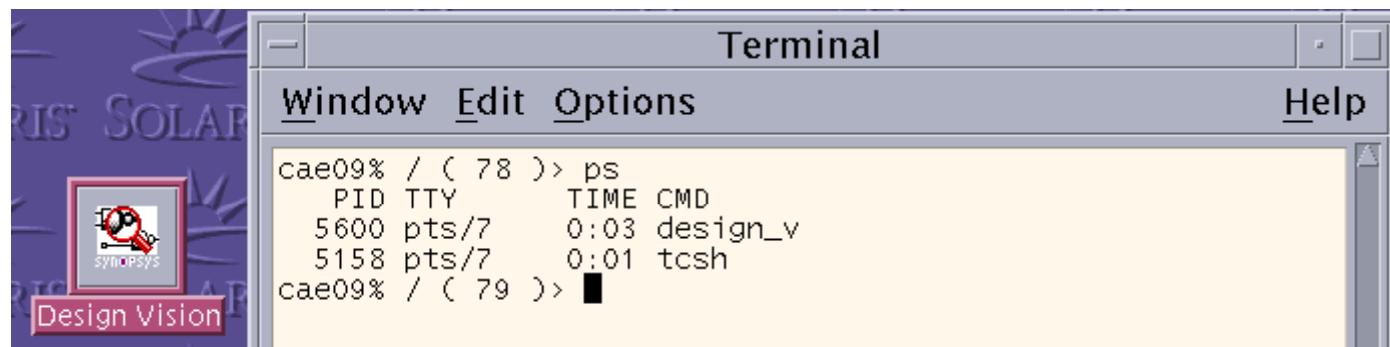
rmdir temp_34

□ rmdir 路徑/欲刪除的資料夾

rmdir ~/temp/

基本指令 (9/12)

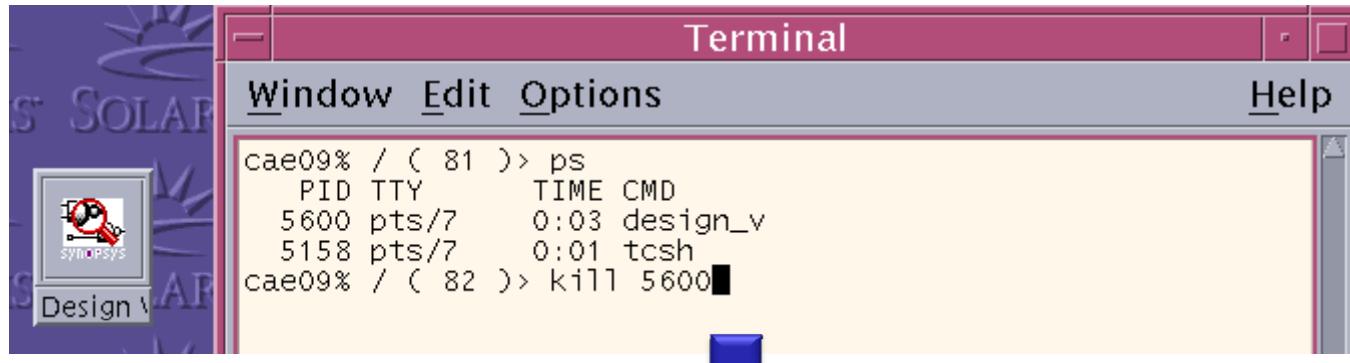
■ ps



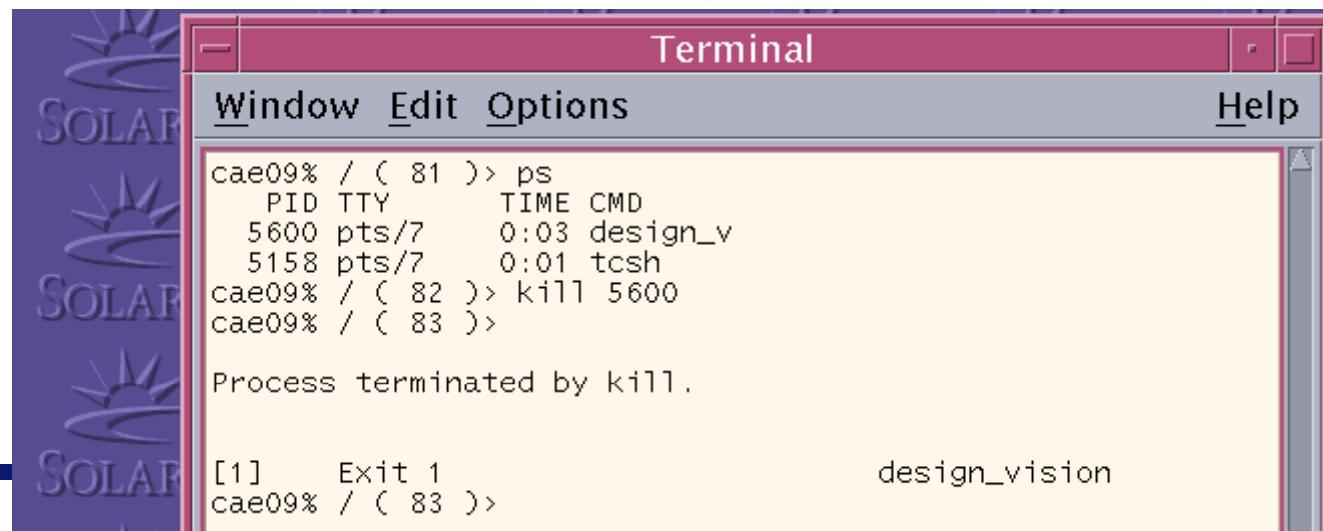
基本指令 (10/12)

■ kill

□ kill PID(執行緒)



```
cae09% / ( 81 )> ps
 PID TTY      TIME CMD
 5600 pts/7    0:03 design_v
 5158 pts/7    0:01 tcsh
cae09% / ( 82 )> kill 5600
```



```
cae09% / ( 81 )> ps
 PID TTY      TIME CMD
 5600 pts/7    0:03 design_v
 5158 pts/7    0:01 tcsh
cae09% / ( 82 )> kill 5600
cae09% / ( 83 )>
Process terminated by kill.

[1]  Exit 1
cae09% / ( 83 )>
```

基本指令 (11/12)

■ tar

- tar -cvf 完成壓縮後的名稱 欲壓縮的資料夾
tar -cvf document.tar ~document/

- tar -cvf 路徑/完成壓縮後的名稱 欲壓縮的資料夾
tar -cvf ~/temp/document.tar ~document/

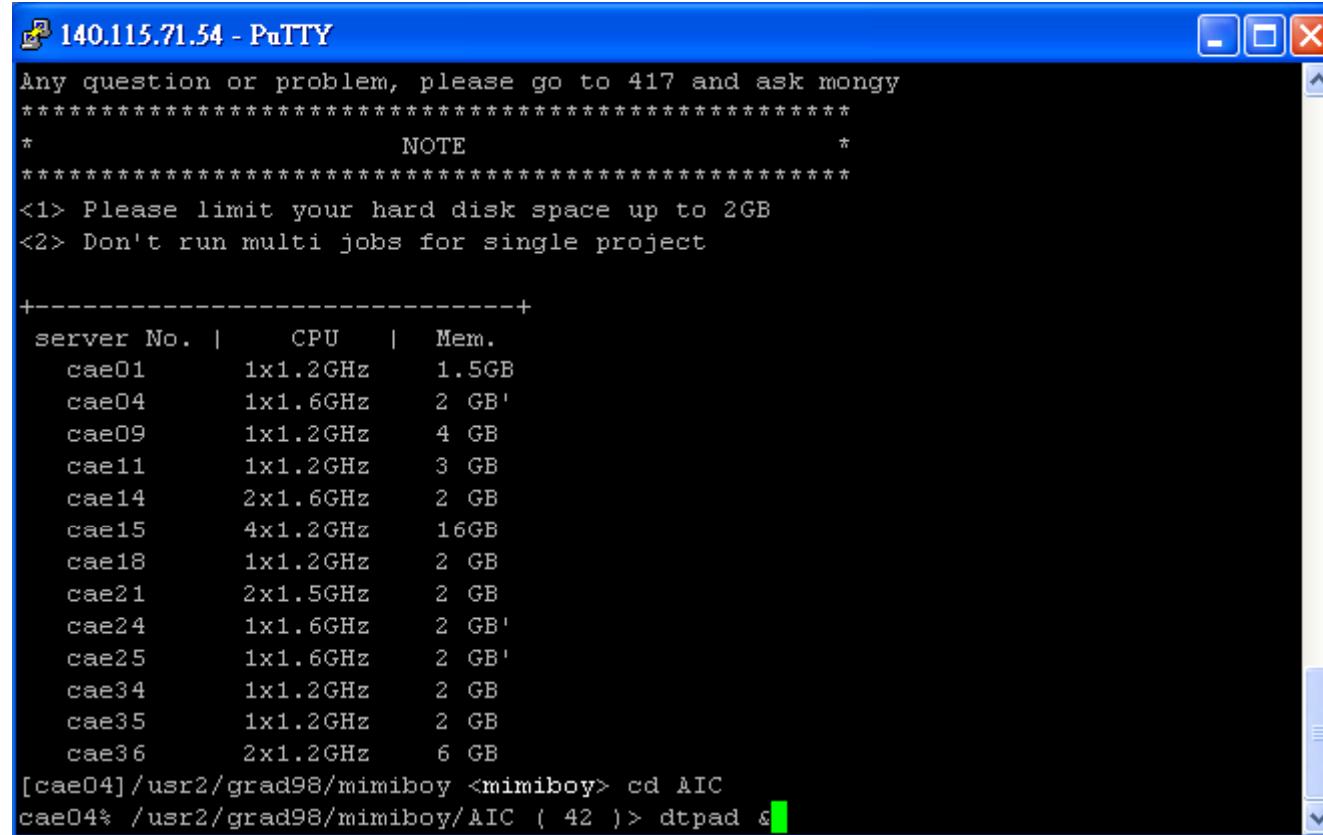
- tar -xvf 欲解壓縮的壓縮檔
tar -xvf document.tar

基本指令 (12/12)

■ passwd

```
cae09% /usr2/grad94/mongy ( 101 )> passwd ←  
passwd: Changing password for mongy  
Enter existing login password: ← 舊的密碼  
New Password: ← 新的密碼  
Re-enter new Password: ← 新的密碼再次確認  
passwd: password successfully changed for mongy  
cae09% /usr2/grad94/mongy ( 102 )> █
```

Operation (1/8)

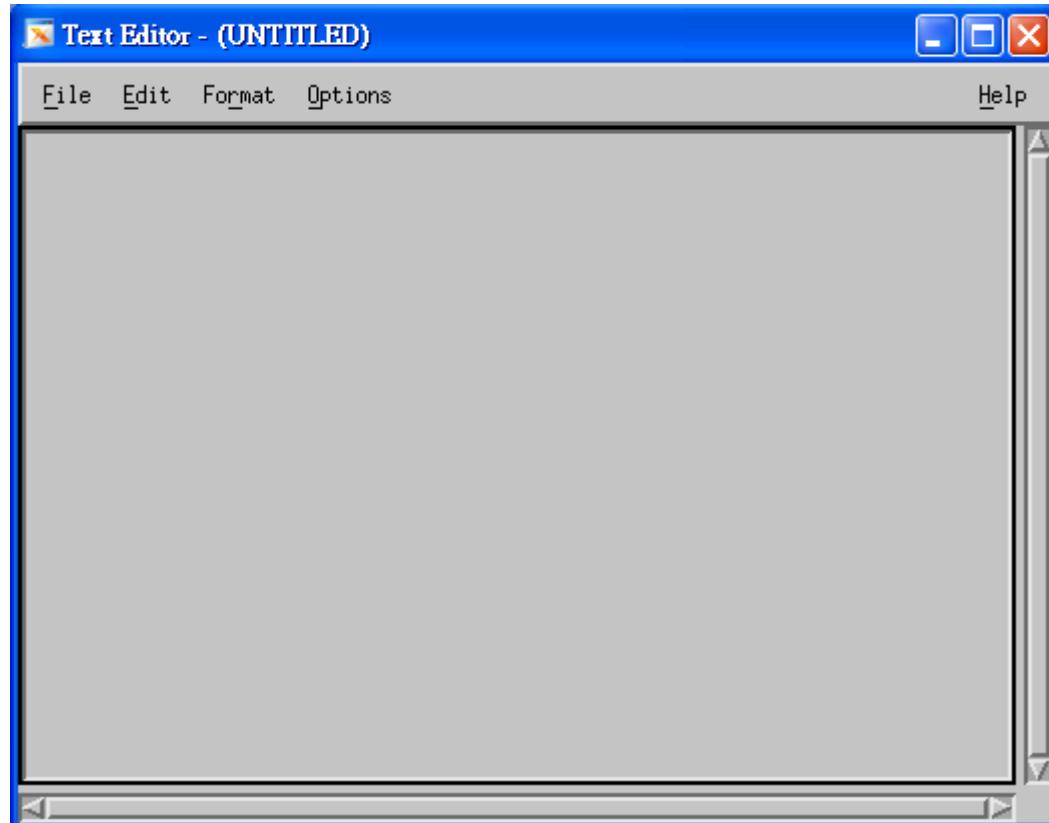


A screenshot of a PuTTY terminal window titled "140.115.71.54 - PuTTY". The window displays a configuration file or script. It starts with a note about hard disk space and multi-jobs, followed by a table of server specifications, and ends with a command prompt.

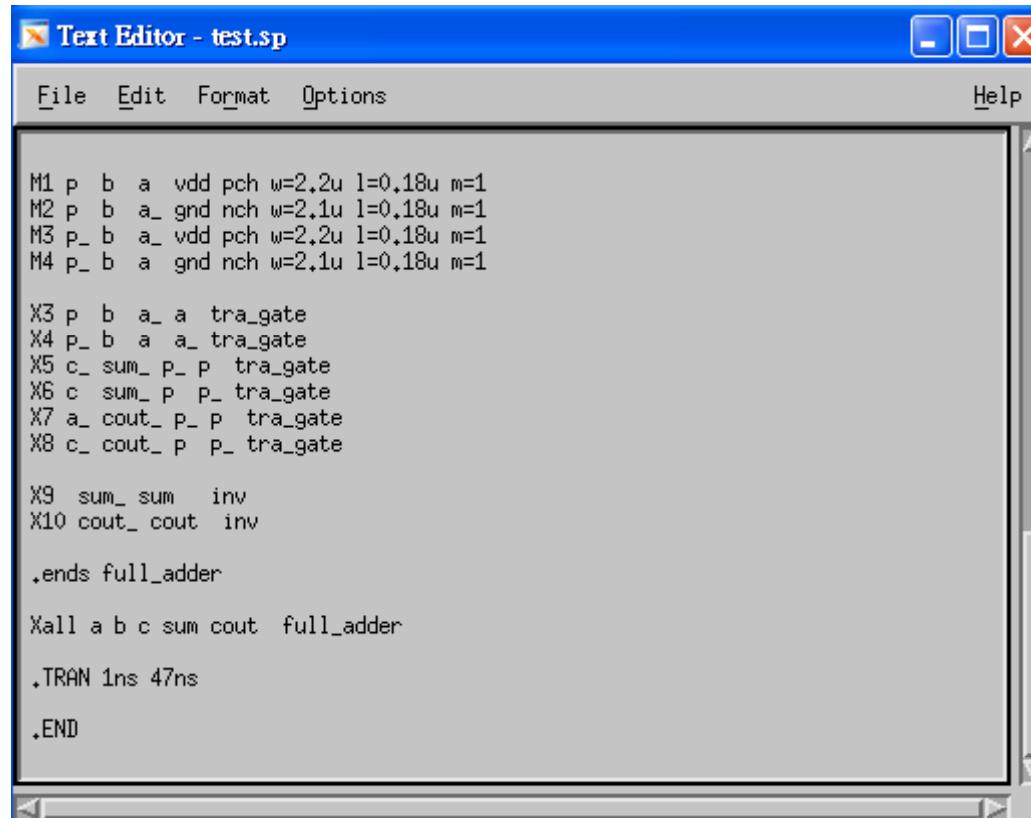
```
Any question or problem, please go to 417 and ask mongy
*****
*                               NOTE
*****
<1> Please limit your hard disk space up to 2GB
<2> Don't run multi jobs for single project

+-----+
server No. |     CPU      |   Mem.
cae01      1x1.2GHz    1.5GB
cae04      1x1.6GHz    2 GB'
cae09      1x1.2GHz    4 GB
cae11      1x1.2GHz    3 GB
cae14      2x1.6GHz    2 GB
cae15      4x1.2GHz    16GB
cae18      1x1.2GHz    2 GB
cae21      2x1.5GHz    2 GB
cae24      1x1.6GHz    2 GB'
cae25      1x1.6GHz    2 GB'
cae34      1x1.2GHz    2 GB
cae35      1x1.2GHz    2 GB
cae36      2x1.2GHz    6 GB
[cae04]/usr2/grad98/mimiboy <mimiboy> cd AIC
cae04% /usr2/grad98/mimiboy/AIC ( 42 )> dtpad &
```

Operation (2/8)



Operation (3/8)



The screenshot shows a Windows-style text editor window titled "Text Editor - test.sp". The window has a standard title bar with icons for minimize, maximize, and close, and a menu bar with "File", "Edit", "Format", "Options", and "Help". The main text area contains the following SPICE code:

```
M1 p b a vdd pch w=2,2u l=0,18u m=1
M2 p b a_ gnd nch w=2,1u l=0,18u m=1
M3 p_ b a_ vdd pch w=2,2u l=0,18u m=1
M4 p_ b a_ gnd nch w=2,1u l=0,18u m=1

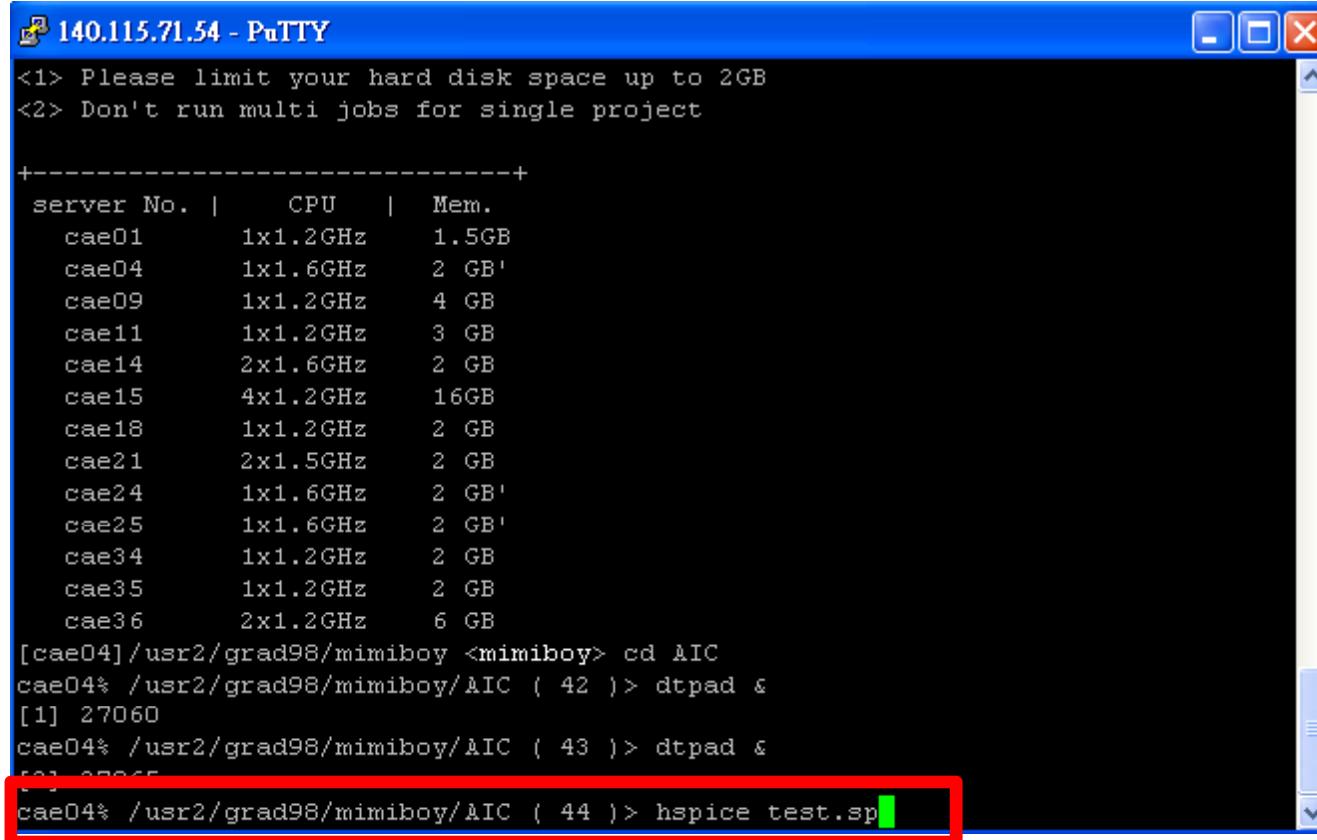
X3 p b a_ a_ tra_gate
X4 p_ b a_ a_ tra_gate
X5 c_ sum_ p_ p_ tra_gate
X6 c_ sum_ p_ p_ tra_gate
X7 a_ cout_ p_ p_ tra_gate
X8 c_ cout_ p_ p_ tra_gate

X9 sum_ sum_ inv
X10 cout_ cout_ inv

.ends full_adder

.Xall a b c sum cout full_adder
.TRAN 1ns 47ns
.END
```

Operation (4/8)



The image shows a PuTTY terminal window titled "140.115.71.54 - PuTTY". The window displays a list of servers with their specifications and a command-line session.

```
<1> Please limit your hard disk space up to 2GB  
<2> Don't run multi jobs for single project  
  
+-----+  
server No. | CPU | Mem.  
cae01     | 1x1.2GHz | 1.5GB  
cae04     | 1x1.6GHz | 2 GB  
cae09     | 1x1.2GHz | 4 GB  
cae11     | 1x1.2GHz | 3 GB  
cae14     | 2x1.6GHz | 2 GB  
cae15     | 4x1.2GHz | 16GB  
cae18     | 1x1.2GHz | 2 GB  
cae21     | 2x1.5GHz | 2 GB  
cae24     | 1x1.6GHz | 2 GB  
cae25     | 1x1.6GHz | 2 GB  
cae34     | 1x1.2GHz | 2 GB  
cae35     | 1x1.2GHz | 2 GB  
cae36     | 2x1.2GHz | 6 GB  
[cae04]/usr2/grad98/mimiboy <mimiboy> cd AIC  
cae04% /usr2/grad98/mimiboy/AIC ( 42 )> dtpad &  
[1] 27060  
cae04% /usr2/grad98/mimiboy/AIC ( 43 )> dtpad &  
[2] 27065  
cae04% /usr2/grad98/mimiboy/AIC ( 44 )> hspice test.sp
```

Operation (5/8)

```
140.115.71.68 - PuTTY

# diodes=      0 # bjts     =      0 # jfets     =      0 # mosfets =      24

analysis      time      # points  tot. iter  conv.riter

op point      0.01          1          35
transient     0.32         48        1030      338 rev=      70
readin        0.16
errchk        0.08
setup         0.00
output        0.00

total cpu time      0.57 seconds
job started at 14:24:19 10/27/2009
job ended   at 14:24:20 10/27/2009

lic: Release
>info: ***** hspice job concluded
```

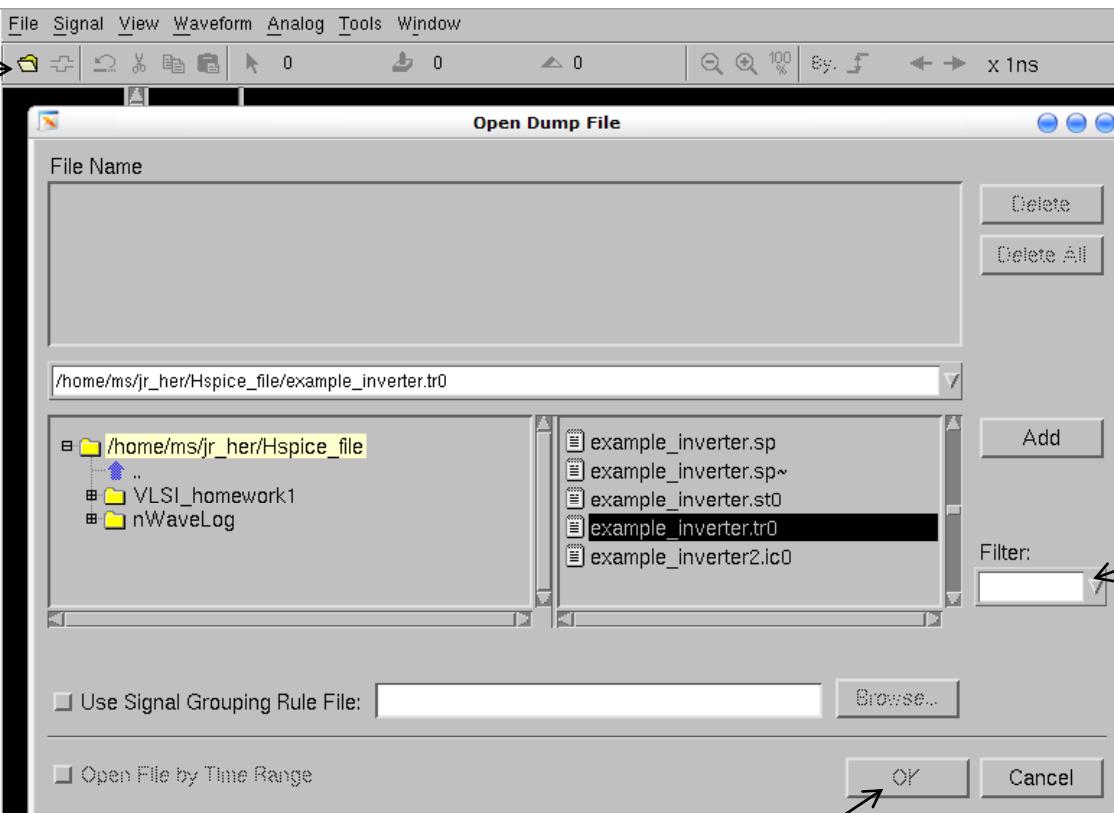
The output shows the results of an HSPICE simulation. It lists the number of diodes, BJTs, JFETs, and MOSFETs used. It provides a breakdown of analysis times for various steps like op point, transient, readin, errchk, setup, and output. The total CPU time is 0.57 seconds, and the job completed at 14:24:20 on 10/27/2009.

```
real      1.3
user      0.5
sys       0.0
HSPICE job test.sp completed.
Tue Oct 27 14:24:20 CST 2009
cae18% /usr2/grad98/mimiboy/AIC ( 44 )> nWave&
```

The final command entered was 'nWave&'.

Operation (6/8)

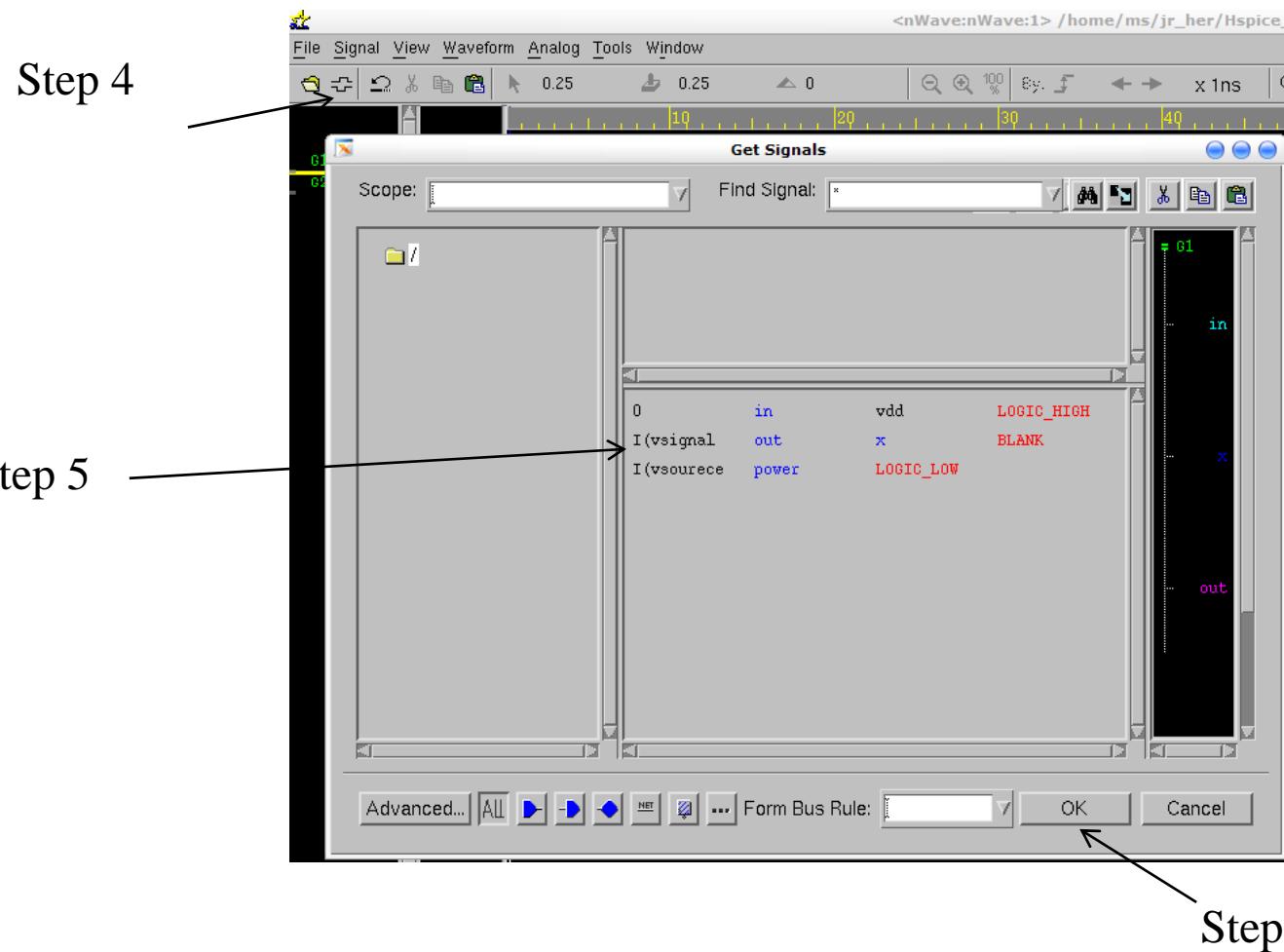
Step 1



Step 2

Step 3

Operation (7/8)



Operation (8/8)

