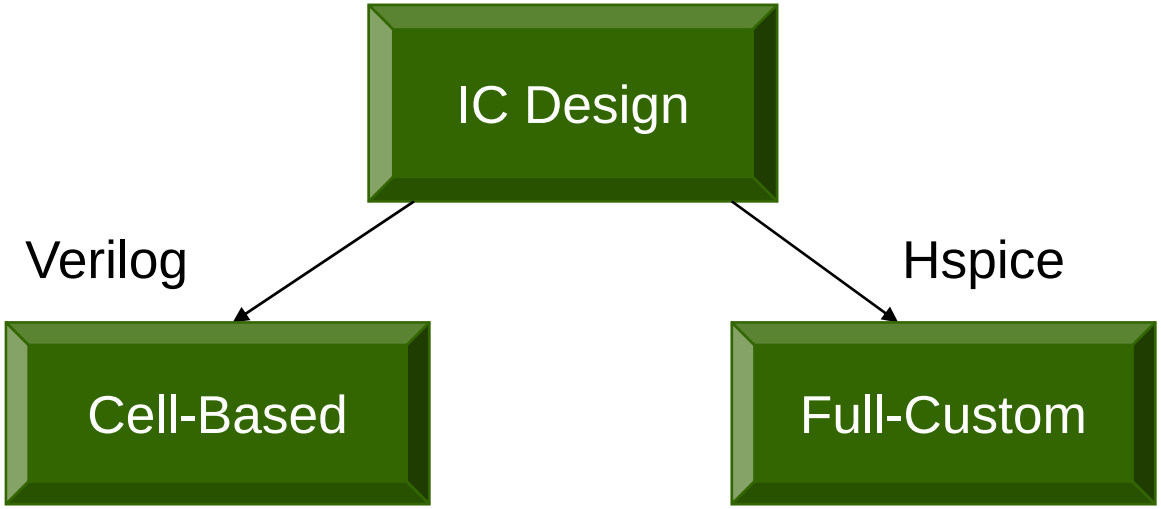
Hspice Tutorial

2010/10/21

Advisor : Jin-Fu Li
Teaching Assistant : Che-Wei Chou
Advanced Reliable Systems (ARES) Laboratory
Department of Electrical Engineering
National Central University
Jhongli, Taiwan

Contents

Introduction(1/2)



DSD

VLSI Design

…

VLSI Design

AIC

…

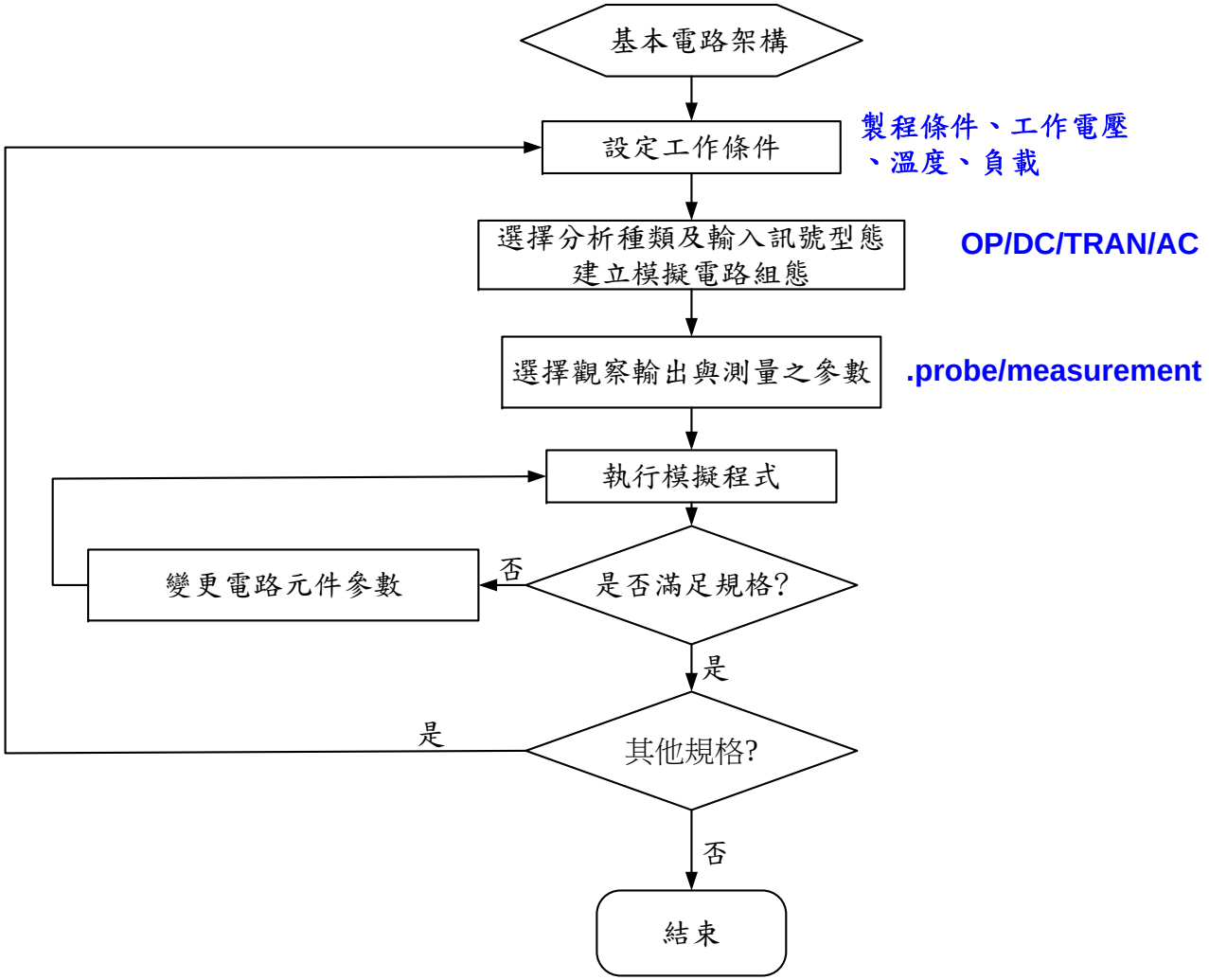
Introduction(2/2)

- **SPICE :**

  Simulation Program with Integrated Circuit Emphasis

- Hspice 是一個電路模擬軟體，用來模擬所設計電路的行為及功能特性。
- Hspice 係以電晶體、二極體、電阻及電容等各種元件模型為基礎，透過數值方法來計算電路各節點的 電壓、電流變化。
- 對於非線性的電路系統，Hspice 是在計算近似解， 所得結果的正確性和元件模型、演算法則有密切關係。
- Hspice 主要提供穩態、暫態及小信號頻率響應模擬 ，使用者需依所設計的電路種類自行規劃分析的指令及相關的輸入。

Basic Flow for SPICE



Contents

- Introduction
- **Simulation Input and Controls**
- Waveform Instructions
- Simulation Output

Instance and Element Names

C	Capacitor
I	Current
L	Inductor
★ M	MOSFET
R	Resistor
V	Voltage Source
X	Subcircuit Call

Unit and Scale Factor

- **Units:**

  R Ohm (e.g. R1 node1 node2 1K)

  L Henry (e.g. L1 node1 node2 1n)

  C Farad (e.g. C1 node1 node2 1p)

- **Scale Factors:**

F 1e-15	T 1e12
P 1e-12	K 1e3
N 1e-9	Meg 1e6
U 1e-6	G 1e9
M 1e-3	DB $20\log_{10}$

Examples:

1pF

1nH

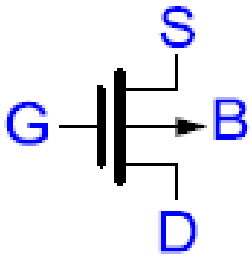
10Meg Hz

vdb(v3)

Instance and Element Descriptions

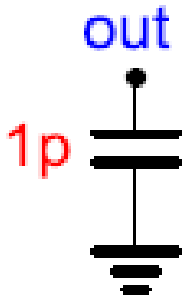
Mname D G S B N/PMOS W=?u L=?u

Mp out in vdd vdd pch W=3u L=1u



R1 A B 1K

C1 out gnd 1p



Subcircuit

.SUBCKT <Subname> <node1> <node2>……

次電路區塊描述

.ENDS <Subname>

```
.subckt inv out in Wn=0.22u Wp=0.22u Lmin=0.18u
mp0 out in vdd vdd pch w=Wp l=Lmin
mn0 out in vss vss nch w=Wn l=Lmin
.ends inv
```

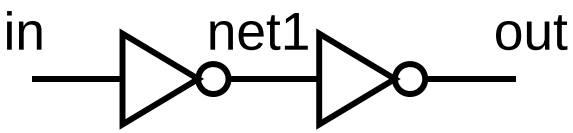
如果要在SPICE檔案中呼叫次電路時，格式如下：

Xname <node1> <node2>…… <Subname>

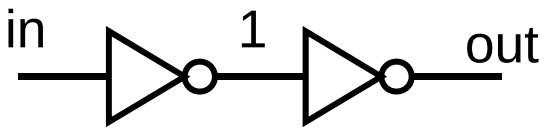
```
xinv dout0 d0 inv Wn=0.22u Wp=0.22u Lmin=0.18u
```

Example

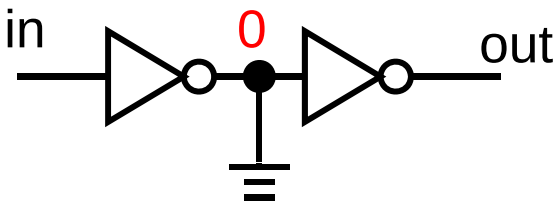
```
***** inv *****
.global vdd vss
.subckt inv in out
MM0 out in vdd vdd pch w=3u l=350n
MM1 out in vss vss nch w=1u l=350n
.ENDS
x1   in     net1   inv
x2   net1   out    inv
```




```
x1   in   1     inv
x2   1    out   inv
```




```
x1   in   0     inv
x2   0    out   inv
```

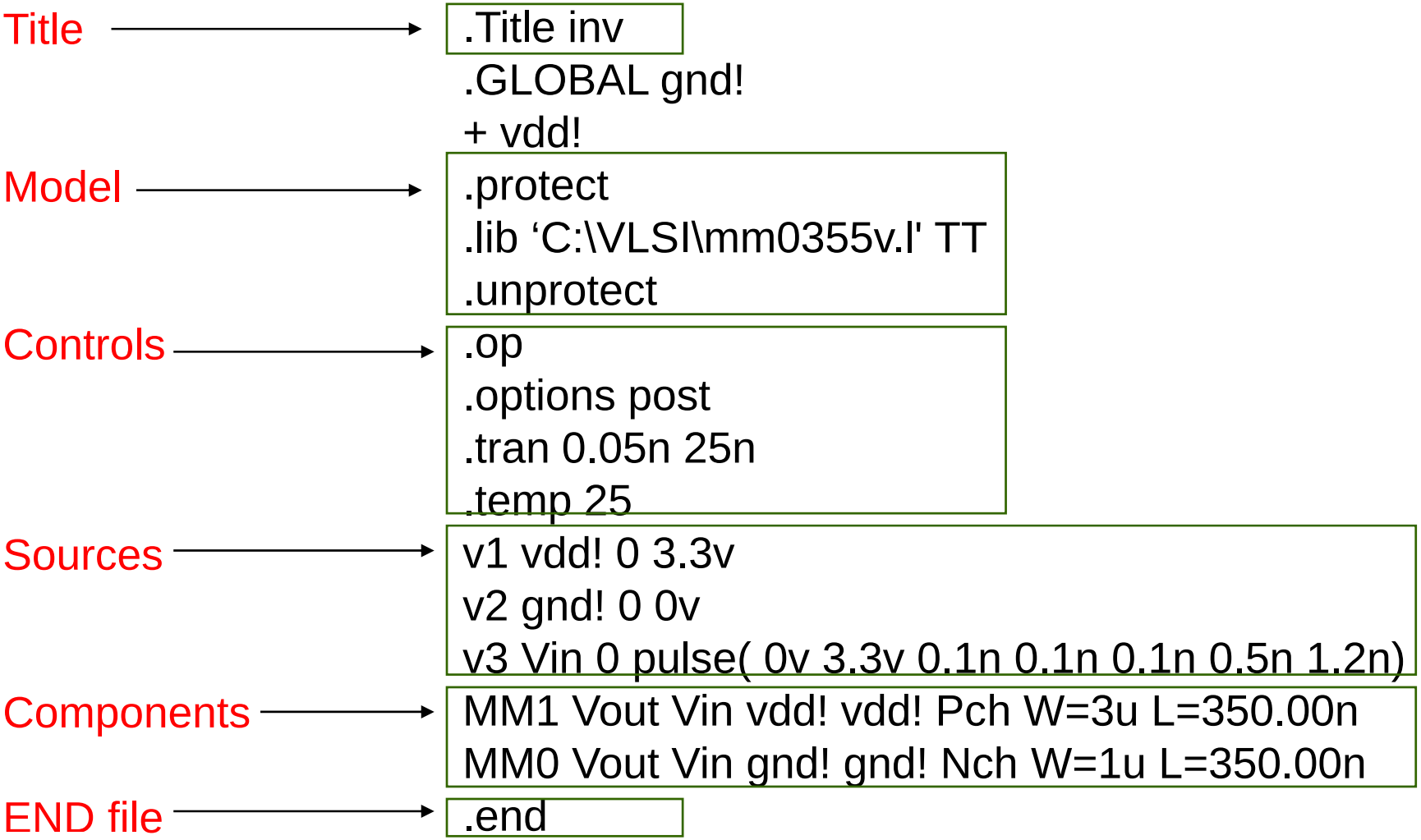


Input Control Statement

- **GLOBAL**
  - ALL nodes are assumed to be local
  - Node names can across all subcircuits by .GLOBAL

```
.GLOBAL VDD VSS
```

Netlist Structure



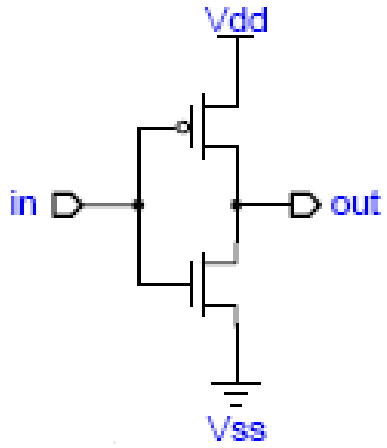
Example

```
******inverter*******
.GLOBAL gnd!
+ vdd!
.protect
.lib 'e:\temp\mm0355v.l' TT
.unprotect
.op
.options post
.tran 0.05n 25n
.temp 25
v1 vdd! 0 3.3v
v2 gnd! 0 0v
v3 Vin 0 pulse( 0v 3.3v 0.1n 0.1n 0.1n 0.5n 1.2n)
MM1 Vout Vin vdd! vdd! Pch W=3u L=350.00n
MM0 Vout Vin gnd! gnd! Nch W=1u L=350.00n
.end
```

第一行是註解，
模擬時會忽略

製程資料，需指定好路徑

TT為模擬環境



一定要有.end才會進行模擬

Control Statements

.AC	電路之交流分析(頻率響應)
.DC	電路之直流分析
.OP	靜態點分析
.NOISE	雜訊分析
★ .TRAN	暫態分析
.SUBCKT	定義次電路
.ENDS	次電路之結束
.OPTIONS	可設定參數及其他功能
.PRINT	指定輸出的內容
.PLOT	圖形式輸出
.TEMP	指定模擬環境的溫度
.END	檔案結束

Contents

- Introduction
- Simulation Input and Controls
- **Waveform Instructions**
- Simulation Output

Transient Sources

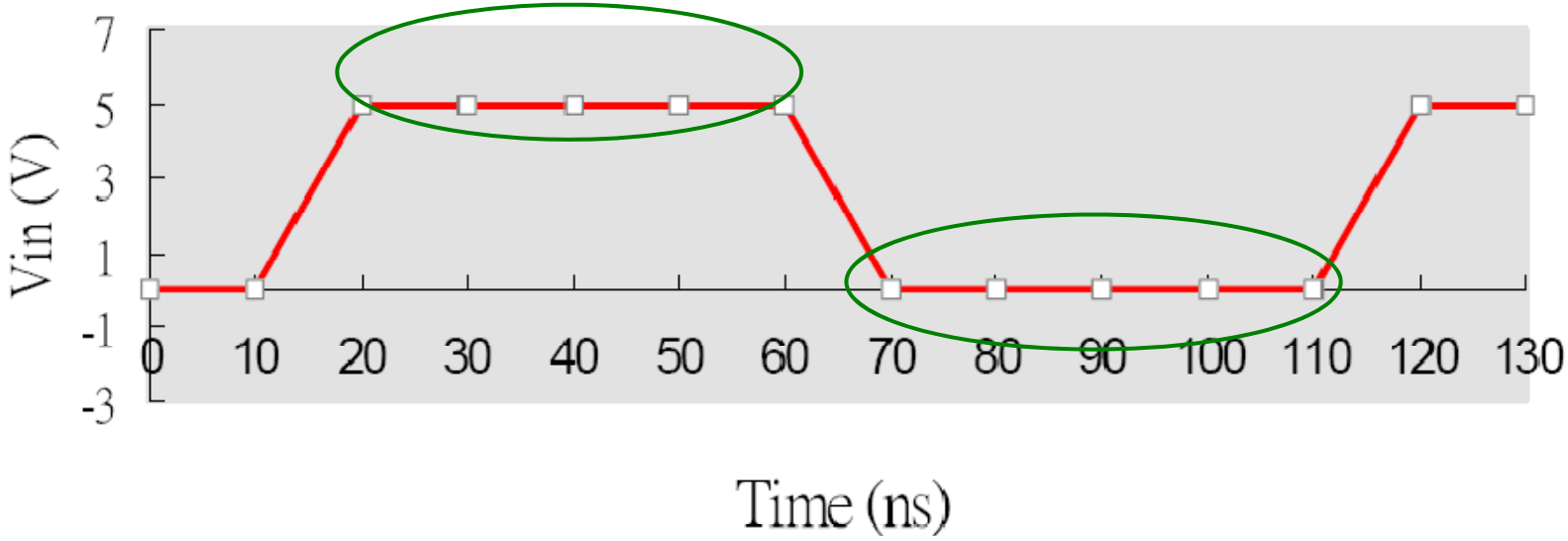
- ★ Pulse (PULSE Function)
- ★ Sinusoidal (SIN Function)
- Exponential (EXP Function)
- ★ Piecewise Linear (PWL Function)
- Single-Frequency FM (SFFM Function)
- Single-Frequency AM (AM Function)

PULSE

☐ PULSE (Periodic Waveform)

PULSE (V1 V2 td tr tf pw per)

PULSE (0V 5V 10ns 10ns10ns 40ns 100ns)

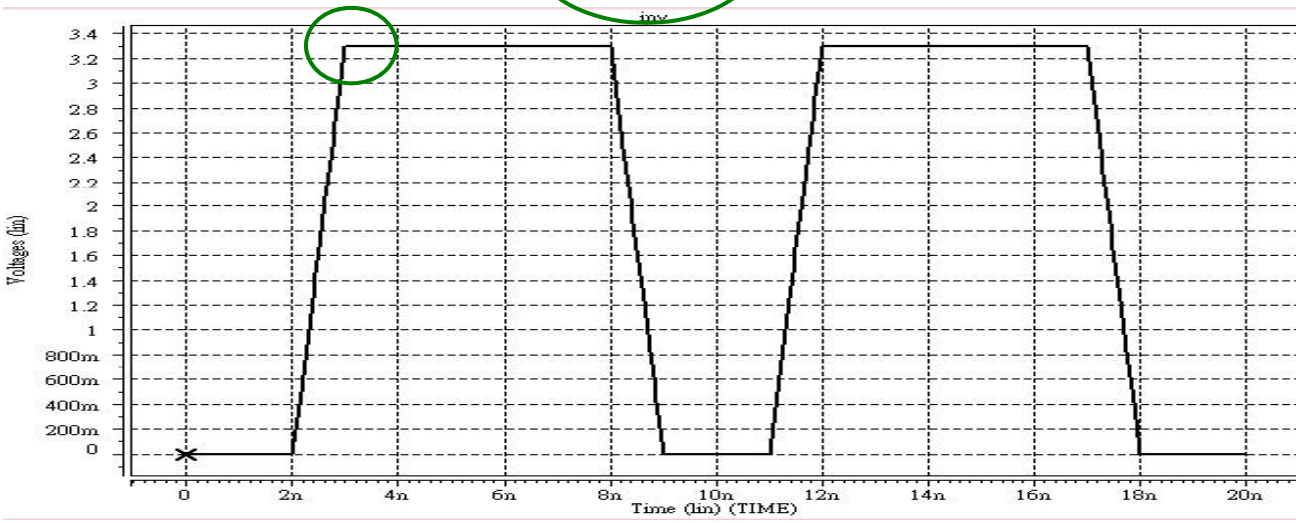


PWL

- **PWL** (Piece Wise Linear Waveform)

PWL (t1 V1 t2 V2 t3 V3 ... R)

PWL (1n 0v 2n 0v 3n 3.3v 8n 3.3v 9n 0v R 0)

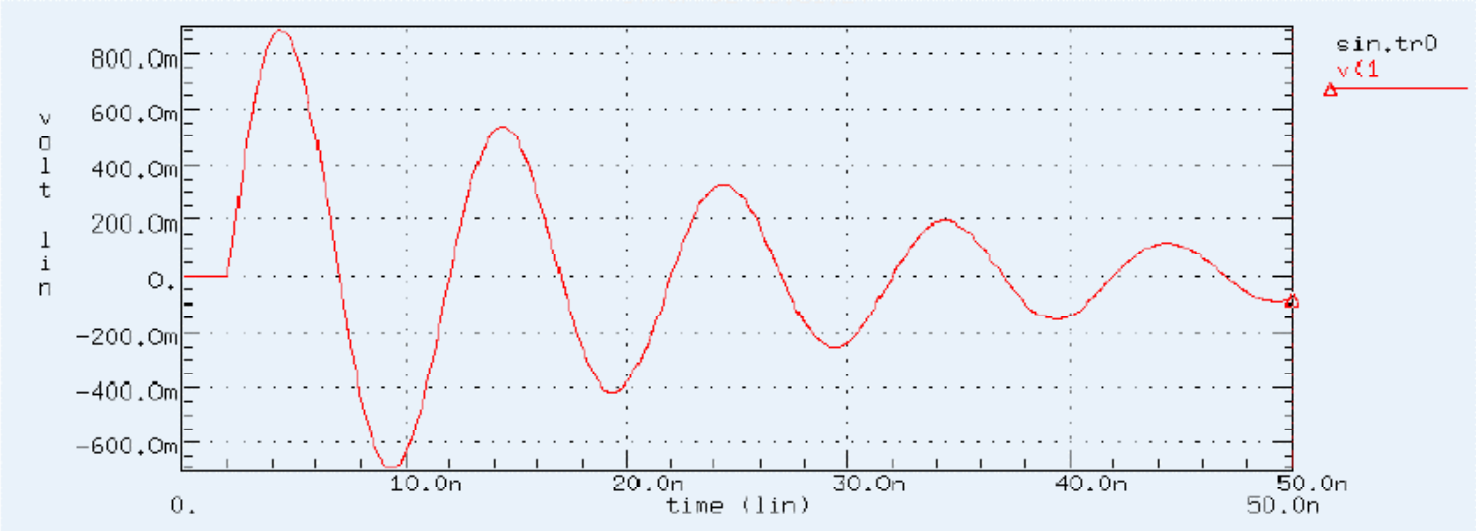


SIN

- **SIN** (Sinusoidal Waveform)

SIN (Voffset Vacmag < Freq Tdelay Dfactor >)

Vin 3 0 SIN (0V 1V 100Meg 2ns 5e7)

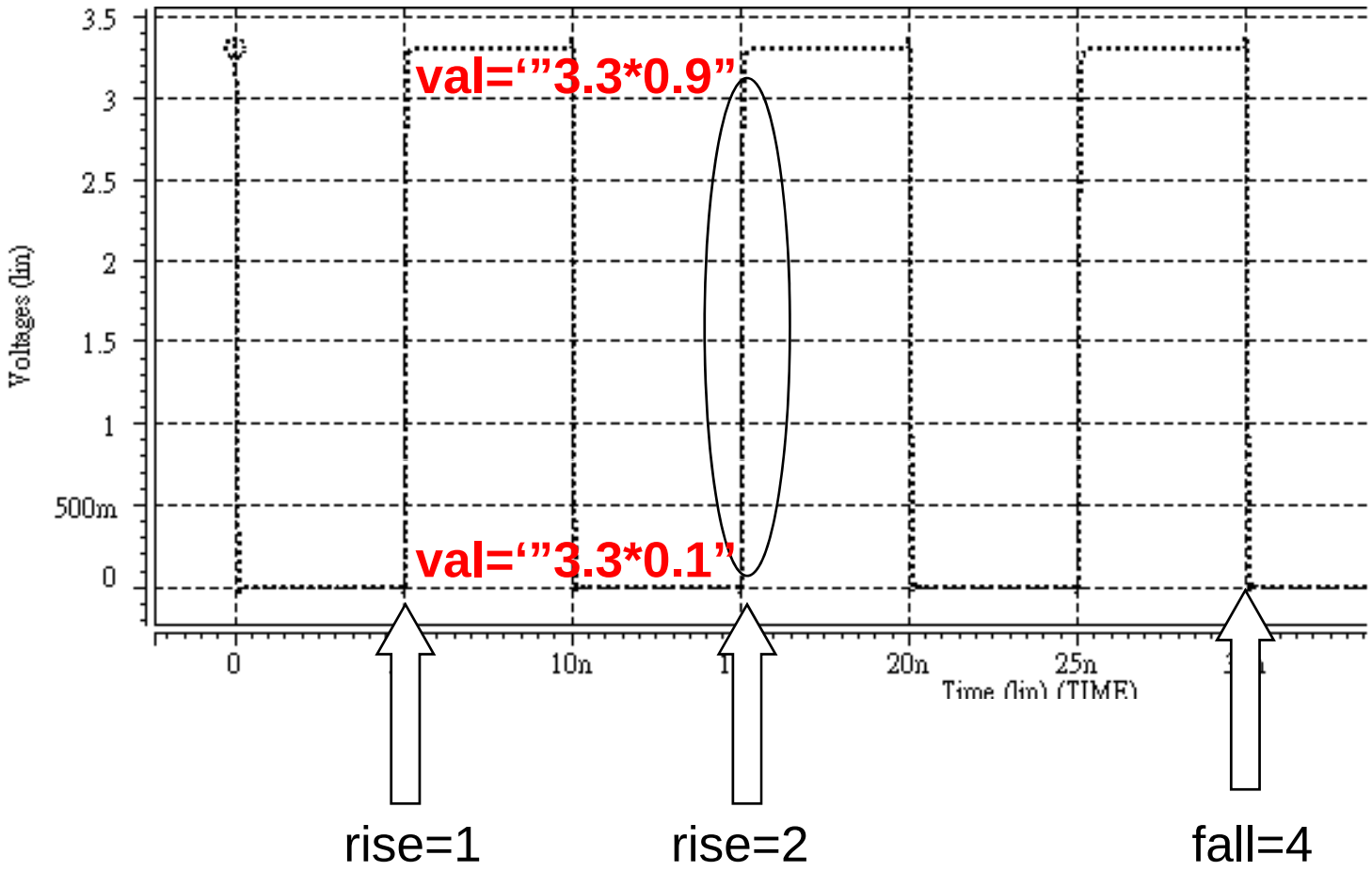


Contents

- Introduction
- Simulation Input and Controls
- Waveform Instructions
- **Simulation Output**

Timing Measurement

.meas tran Tr trig v(out) val="3.3*0.1" rise=2 targ v(out) val='"3.3*0.9" rise=2



Example

SP檔

inv - 記事本

檔案(F) 編輯(E) 格式(O) 檢視(V) 說明(H)

```
***** inv *****
.global vdd vss
.subckt inv in out
MM0 out in vdd vdd pch w=3u l=350n
MM1 out in vss vss nch w=1u l=350n
.ENDS
.protect
.lib 'mm0355v.1' TT
.unprotect
vdd vdd 0 3.3
vss vss 0 0
vin in 0 pulse(0 3.3 0n .1n .1n 4.9n 10n)
x1 in out inv
.op
.options post
.tran 0.1n 50n
.meas tran Tr trig v(out) val="3.3*0.1" rise=2
+ targ v(out) val="3.3*0.9" rise=2
.end
```

Simulate

mt0檔

inv - 記事本

檔案(F) 編輯(E) 格式(O) 檢視(V) 說明(H)

```
$DATA1 SOURCE='HSPICE' VERSION='X-2005.09        '
.TITLE '***** inv *****'
tr                    temper               alter#
  6.738e-11             25.0000              1.0000
```

Tr=6.738e-11 s

Power

- Command :
- .meas tran pwr avg power
  - 在暫態分析中，量測整個電路的平均功率消耗
  - 結果顯示在*.mt0檔

Contents

- Introduction
- Simulation Input and Controls
- Waveform Instructions
- Simulation Output
- **Appendix**

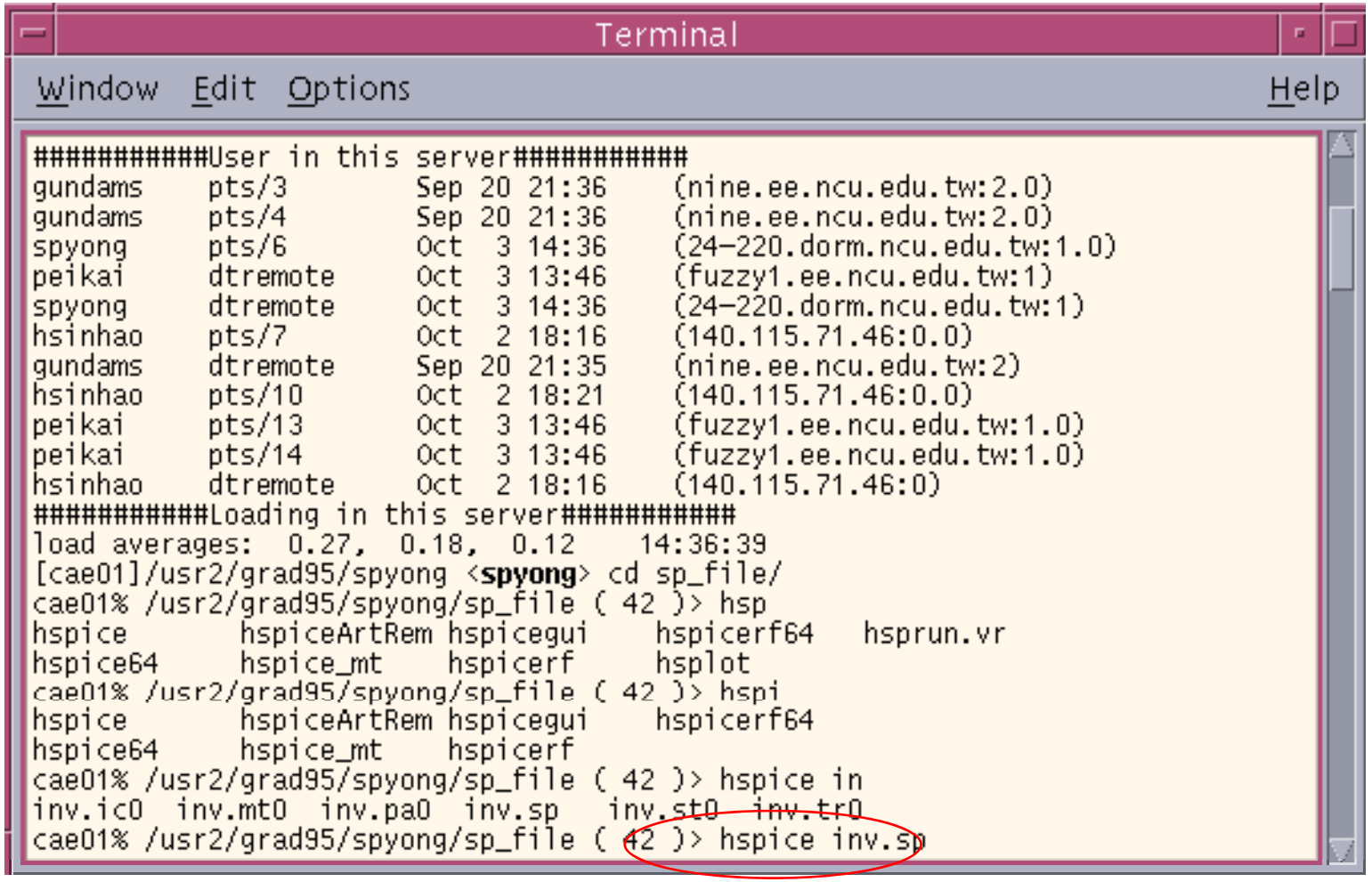
Example

inv.sp (~/sp_file) - VIM

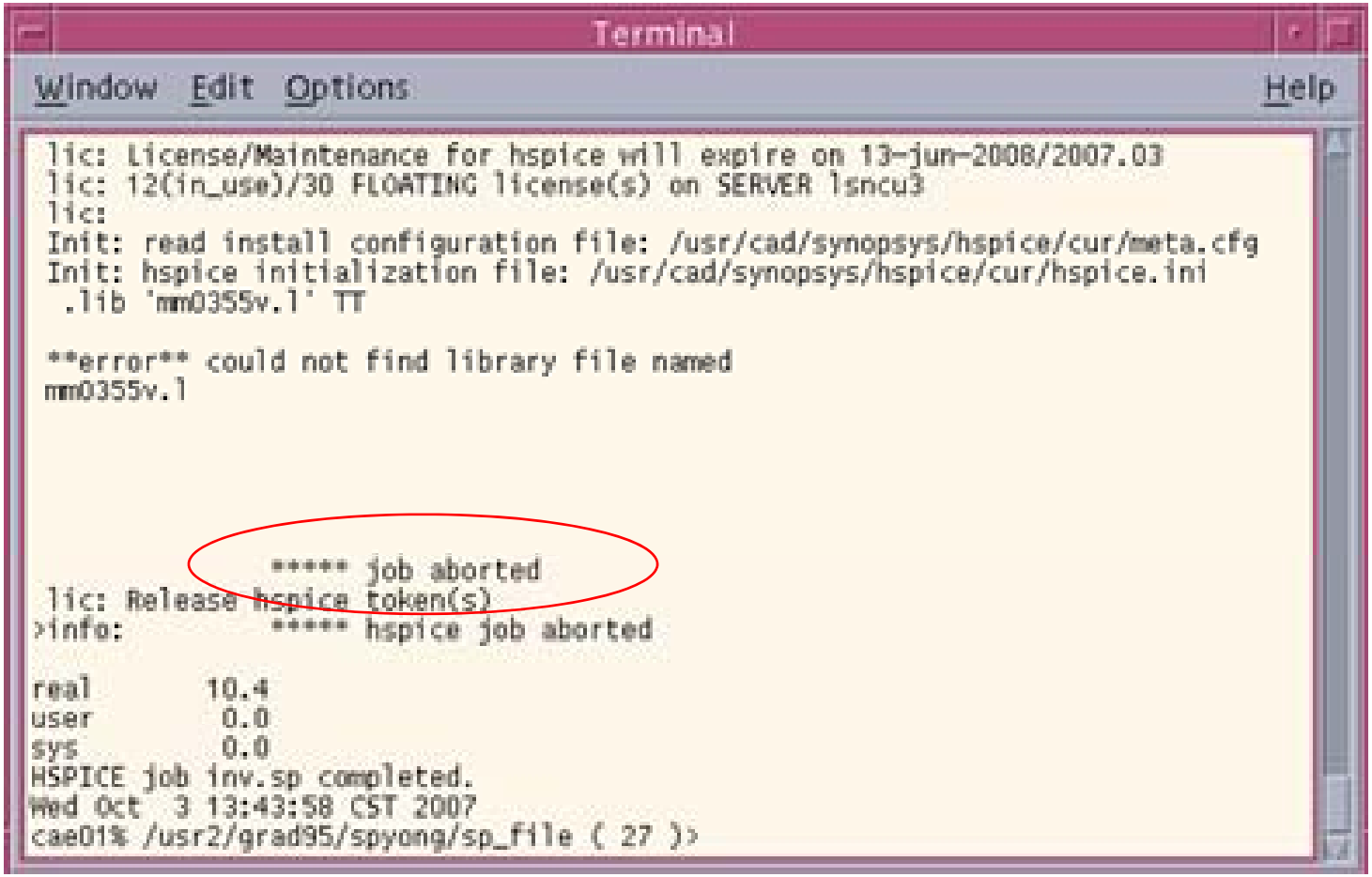
Window Edit Options Help

```
***** inv *****
.global vdd vss
.subckt inv in out
MM0 out in vdd vdd pch w=3u l=350n
MM1 out in vss vss nch w=1u l=350n
.ENDS
.protect
.lib '/usr2/grad95/spyong/sp_file/mm0355v.l' TT
.unprotect
vdd vdd 0 3.3
vss vss 0 0
vin in 0 pulse(0 3.3 0n .1n .1n 4.9n 10n)
x1 in out inv
.op
.options post
.tran 0.1n 50n
.meas tran Tr trig v(out) val="3.3*0.1" rise=2
+ targ v(out) val="3.3*0.9" rise=2
.meas tran T trig v(out) val="3.3*0.5" fall=1
+ targ v(out) val="3.3*0.5" rise=1
.end
~
~
"inv.sp" 21 lines, 479 characters
```

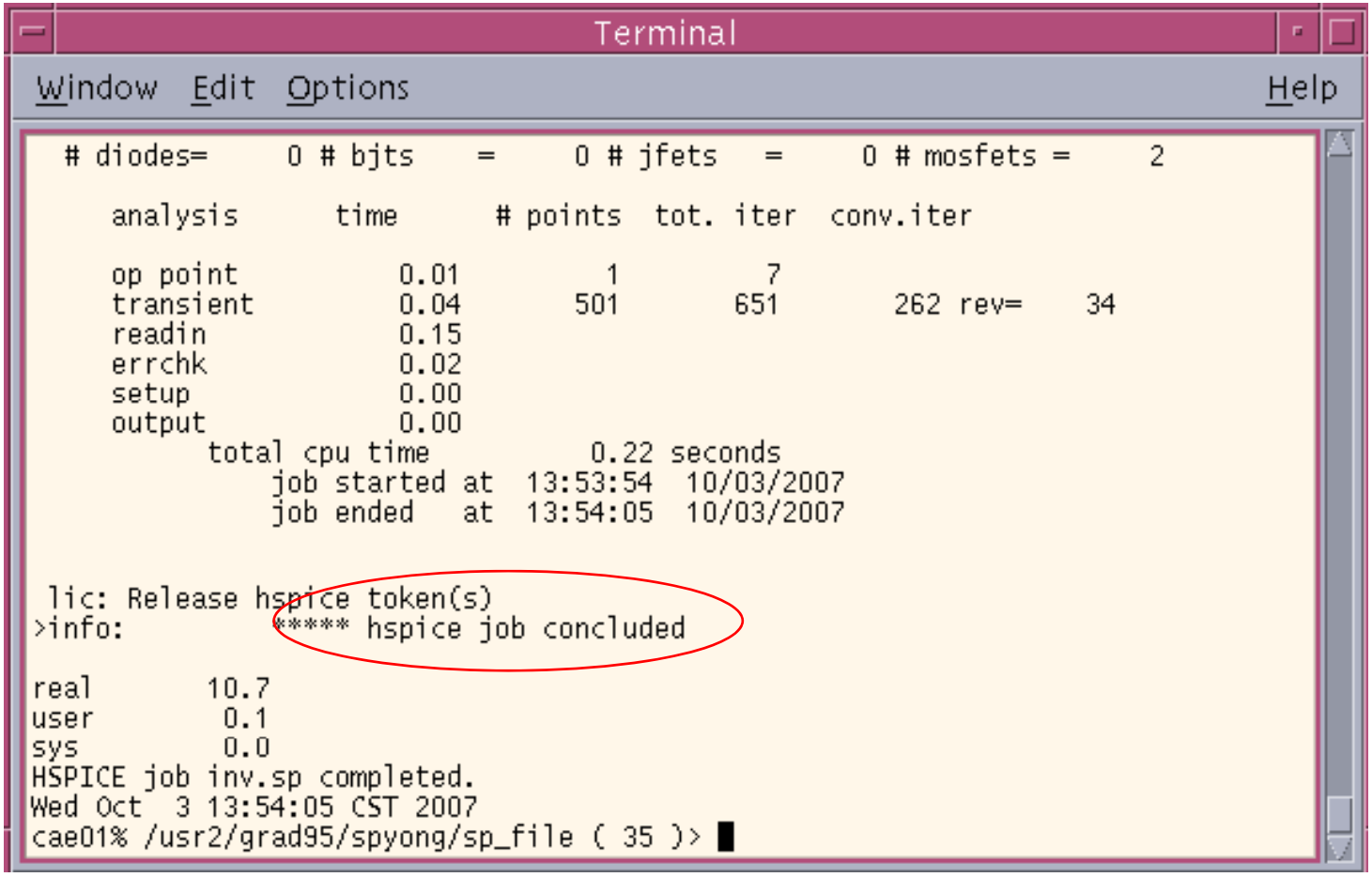
Compile


Terminal
Window Edit Options Help
############User in this server############
gundams pts/3 Sep 20 21:36 (nine.ee.ncu.edu.tw:2.0)
gundams pts/4 Sep 20 21:36 (nine.ee.ncu.edu.tw:2.0)
spyong pts/6 Oct 3 14:36 (24-220.dorm.ncu.edu.tw:1.0)
peikai dtremote Oct 3 13:46 (fuzzy1.ee.ncu.edu.tw:1)
spyong dtremote Oct 3 14:36 (24-220.dorm.ncu.edu.tw:1)
hsinhao pts/7 Oct 2 18:16 (140.115.71.46:0.0)
gundams dtremote Sep 20 21:35 (nine.ee.ncu.edu.tw:2)
hsinhao pts/10 Oct 2 18:21 (140.115.71.46:0.0)
peikai pts/13 Oct 3 13:46 (fuzzy1.ee.ncu.edu.tw:1.0)
peikai pts/14 Oct 3 13:46 (fuzzy1.ee.ncu.edu.tw:1.0)
hsinhao dtremote Oct 2 18:16 (140.115.71.46:0)
############Loading in this server############
load averages: 0.27, 0.18, 0.12 14:36:39
[cae01]/usr2/grad95/spyong <spyong> cd sp_file/
cae01% /usr2/grad95/spyong/sp_file (42)> hsp
hspice hspiceArtRem hspicegui hspicerf64 hsprun.vr
hspice64 hspice_mt hspicerf hsplot
cae01% /usr2/grad95/spyong/sp_file (42)> hspi
hspice hspiceArtRem hspicegui hspicerf64
hspice64 hspice_mt hspicerf
cae01% /usr2/grad95/spyong/sp_file (42)> hspice in
inv.ic0 inv.mt0 inv.pa0 inv.sp inv.st0 inv.tr0
cae01% /usr2/grad95/spyong/sp_file (42)> hspice inv.sp

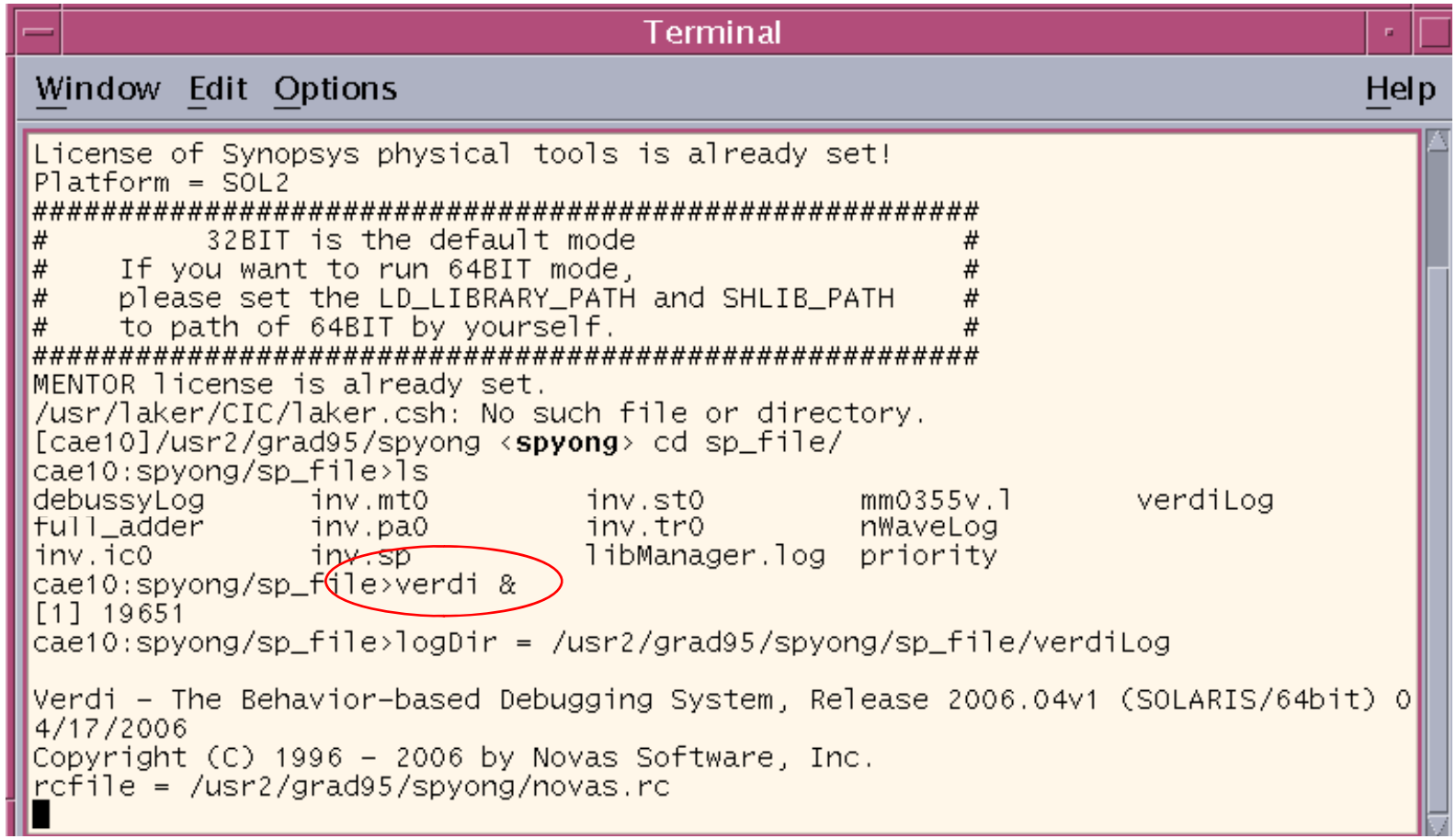
Job Aborted


Terminal
Window Edit Options Help
lic: License/Maintenance for hspice will expire on 13-jun-2008/2007.03
lic: 12(in_use)/30 FLOATING license(s) on SERVER lsncu3
lic:
Init: read install configuration file: /usr/cad/synopsys/hspice/cur/meta.cfg
Init: hspice initialization file: /usr/cad/synopsys/hspice/cur/hspice.ini
.lib 'mm0355v.l' TT
error could not find library file named
mm0355v.l
***** job aborted
lic: Release hspice token(s)
>info: ***** hspice job aborted
real 10.4
user 0.0
sys 0.0
HSPICE job inv.sp completed.
Wed Oct 3 13:43:58 CST 2007
cae01% /usr2/grad95/spyong/sp_file (27)>

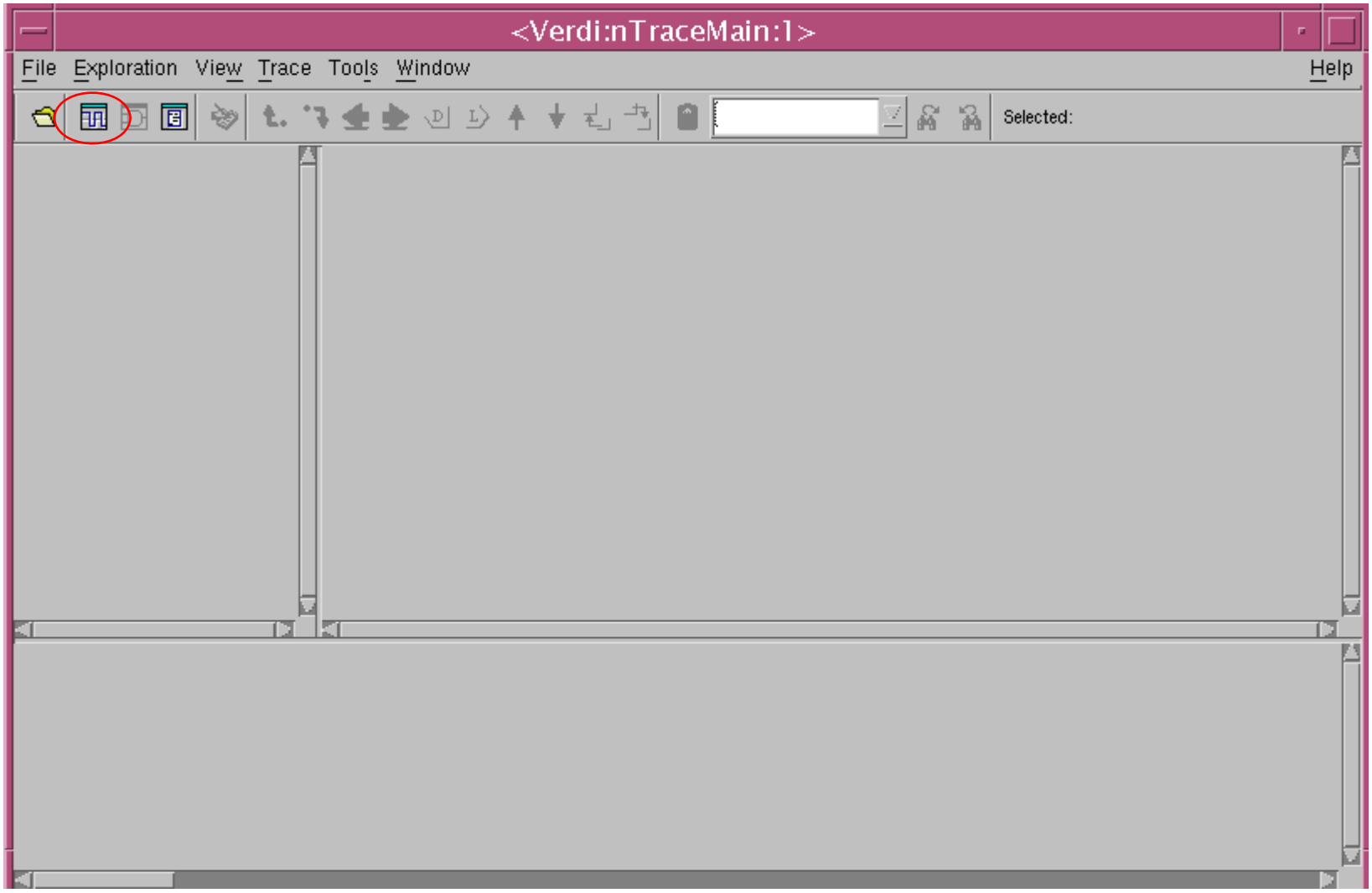
Job Conculded



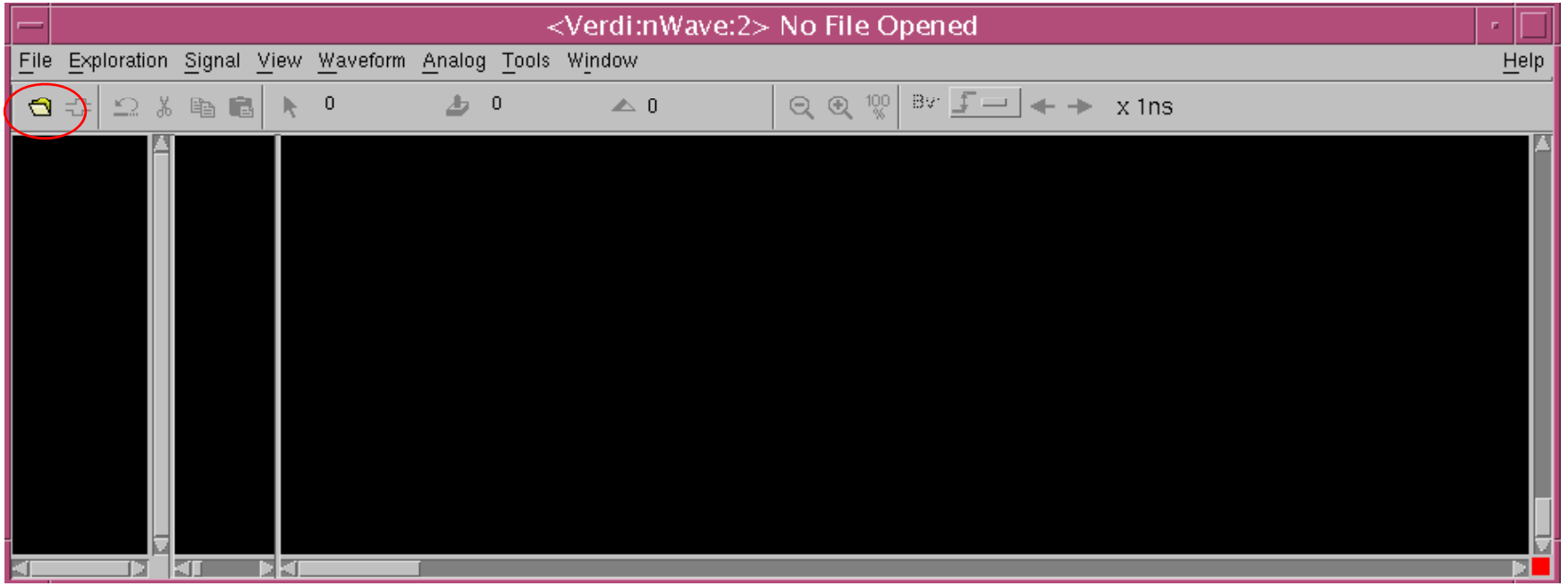
verdi

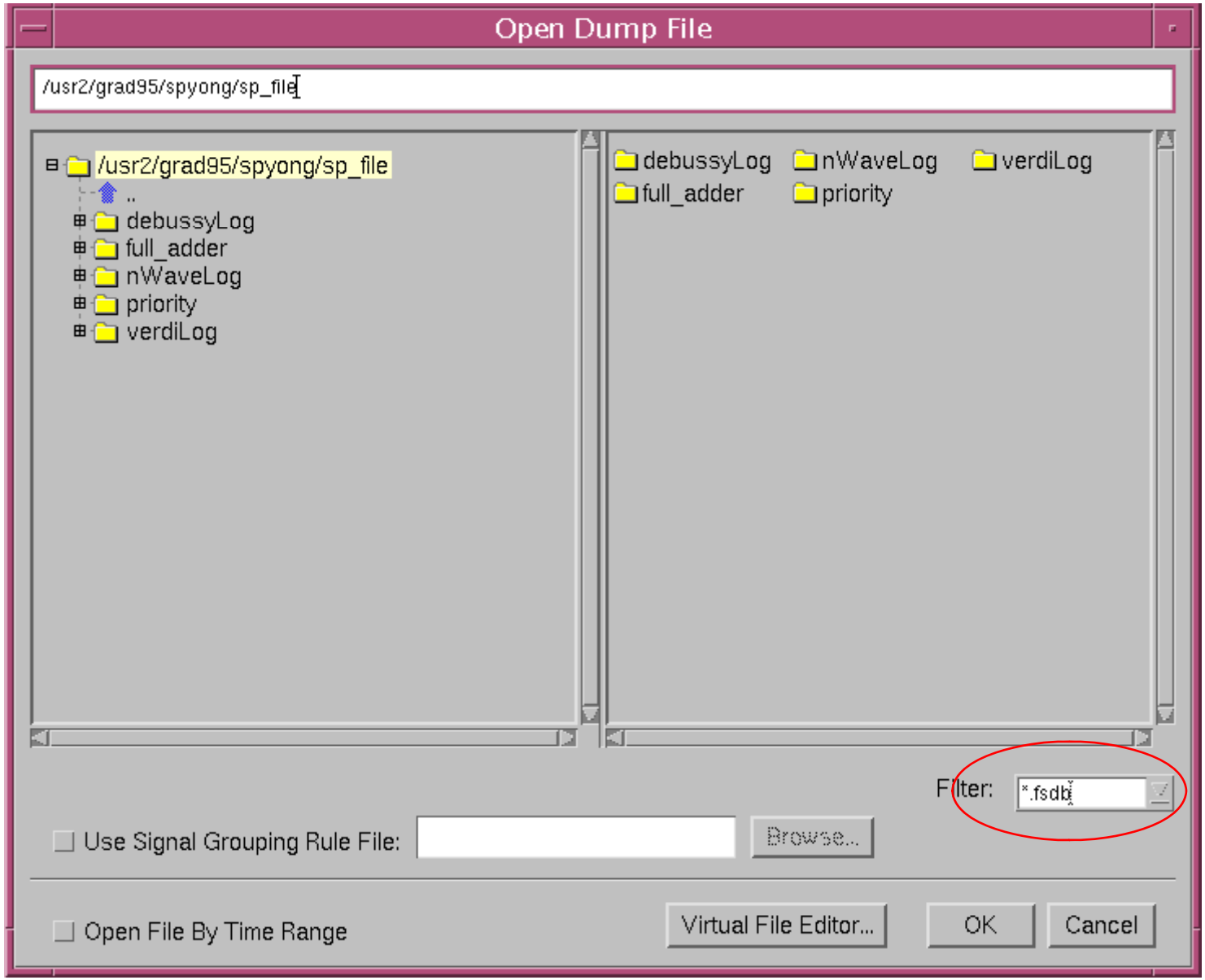

Terminal
Window Edit Options Help
License of Synopsys physical tools is already set!
Platform = SOL2
##
32BIT is the default mode
If you want to run 64BIT mode,
please set the LD_LIBRARY_PATH and SHLIB_PATH
to path of 64BIT by yourself.
##
MENTOR license is already set.
/usr/laker/CIC/laker.csh: No such file or directory.
[cae10]/usr2/grad95/spyong <spyong> cd sp_file/
cae10:spyong/sp_file>ls
debussyLog inv.mt0 inv.st0 mm0355v.l verdiLog
full_adder inv.pa0 inv.tr0 nWaveLog
inv.ic0 inv.sp libManager.log priority
cae10:spyong/sp_file>verdi &
[1] 19651
cae10:spyong/sp_file>logDir = /usr2/grad95/spyong/sp_file/verdiLog
Verdi - The Behavior-based Debugging System, Release 2006.04v1 (SOLARIS/64bit) 0
4/17/2006
Copyright (C) 1996 - 2006 by Novas Software, Inc.
rcfile = /usr2/grad95/spyong/novas.rc

New Waveform

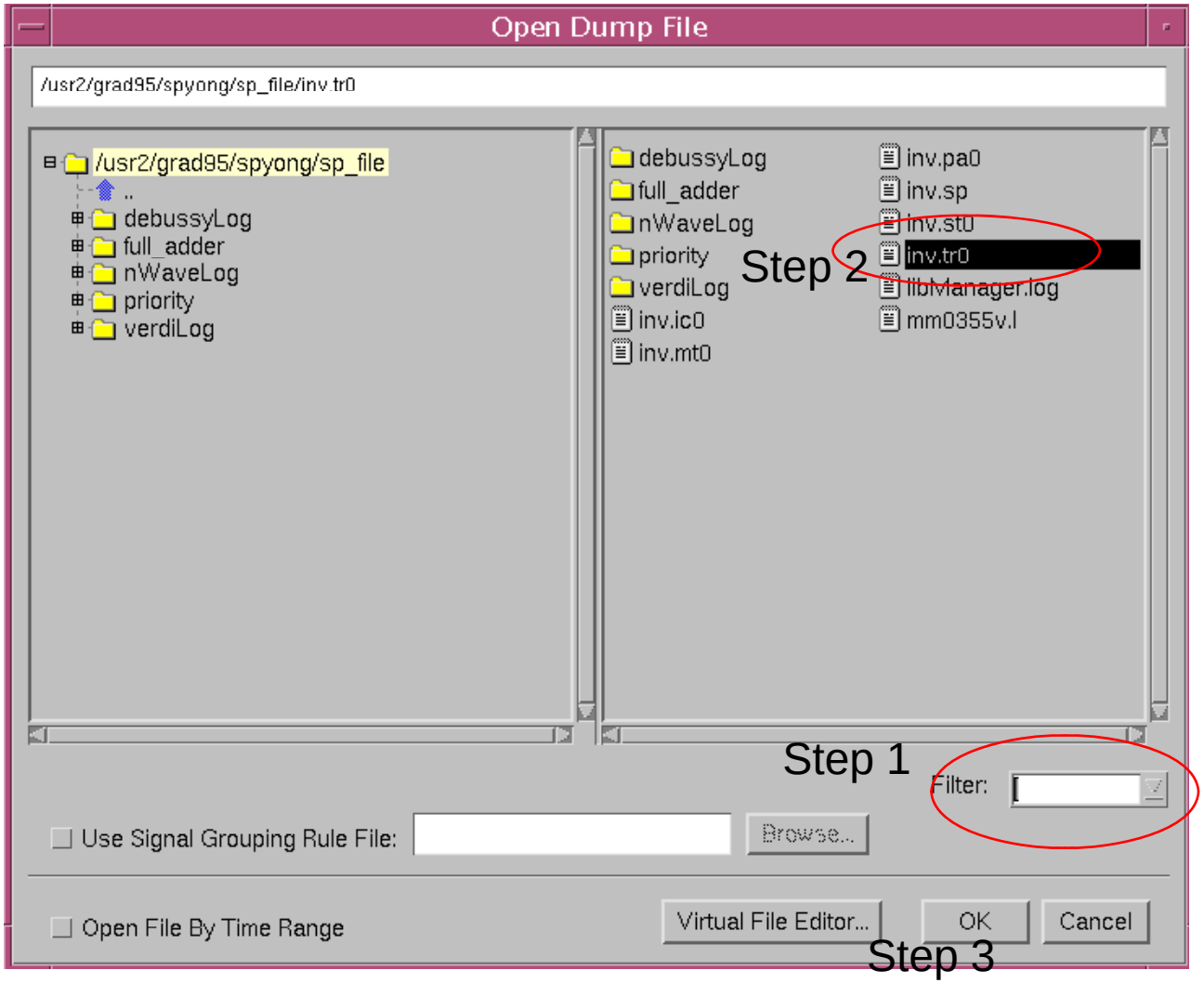


Open File

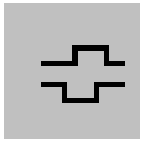

<Verdi:nWave:2> No File Opened
File Exploration Signal View Waveform Analog Tools Window Help
0
0
0
x 1ns

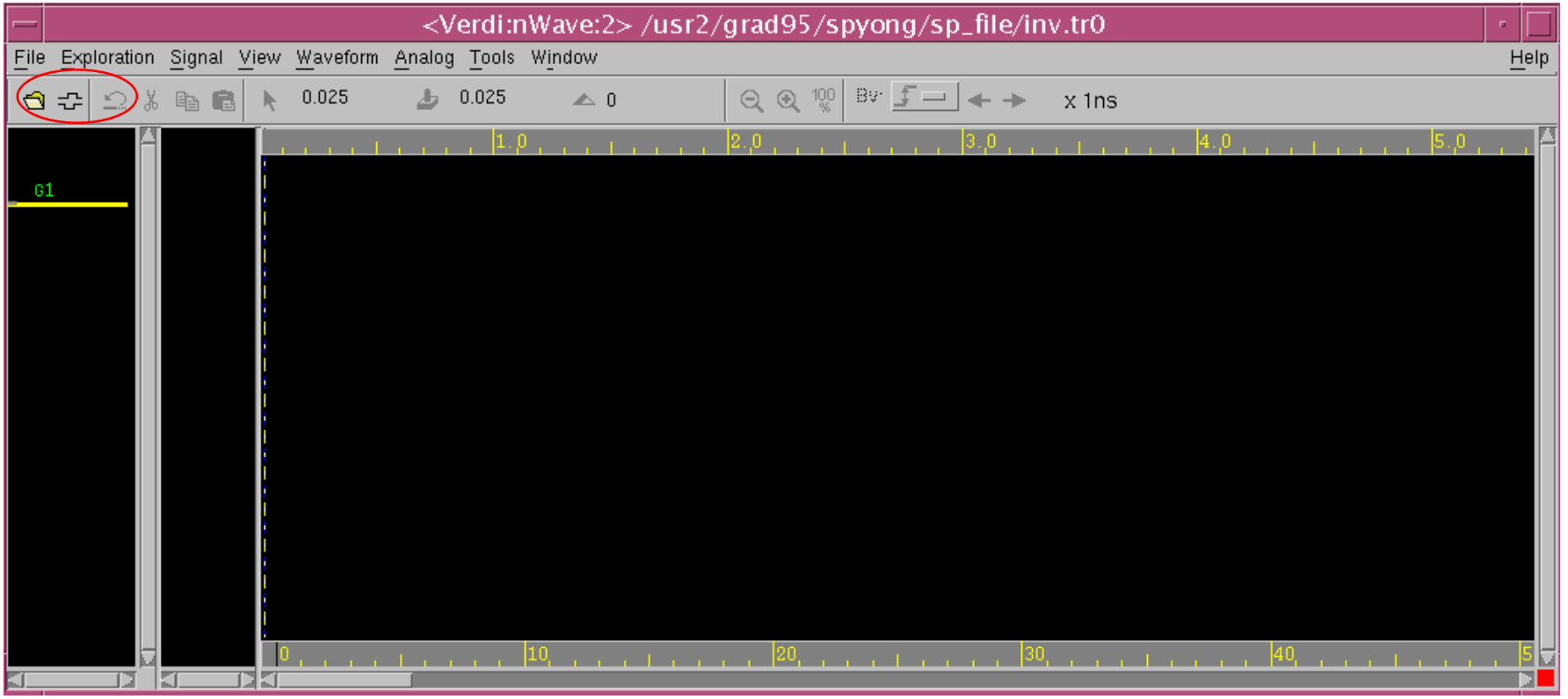

Open Dump File
/usr2/grad95/spyong/sp_file
/usr2/grad95/spyong/sp_file
..
debussyLog
full_adder
nWaveLog
priority
verdiLog
debussyLog
nWaveLog
verdiLog
full_adder
priority
Filter:
*.fsdb
Use Signal Grouping Rule File:
Browse...
Open File By Time Range
Virtual File Editor...
OK
Cancel

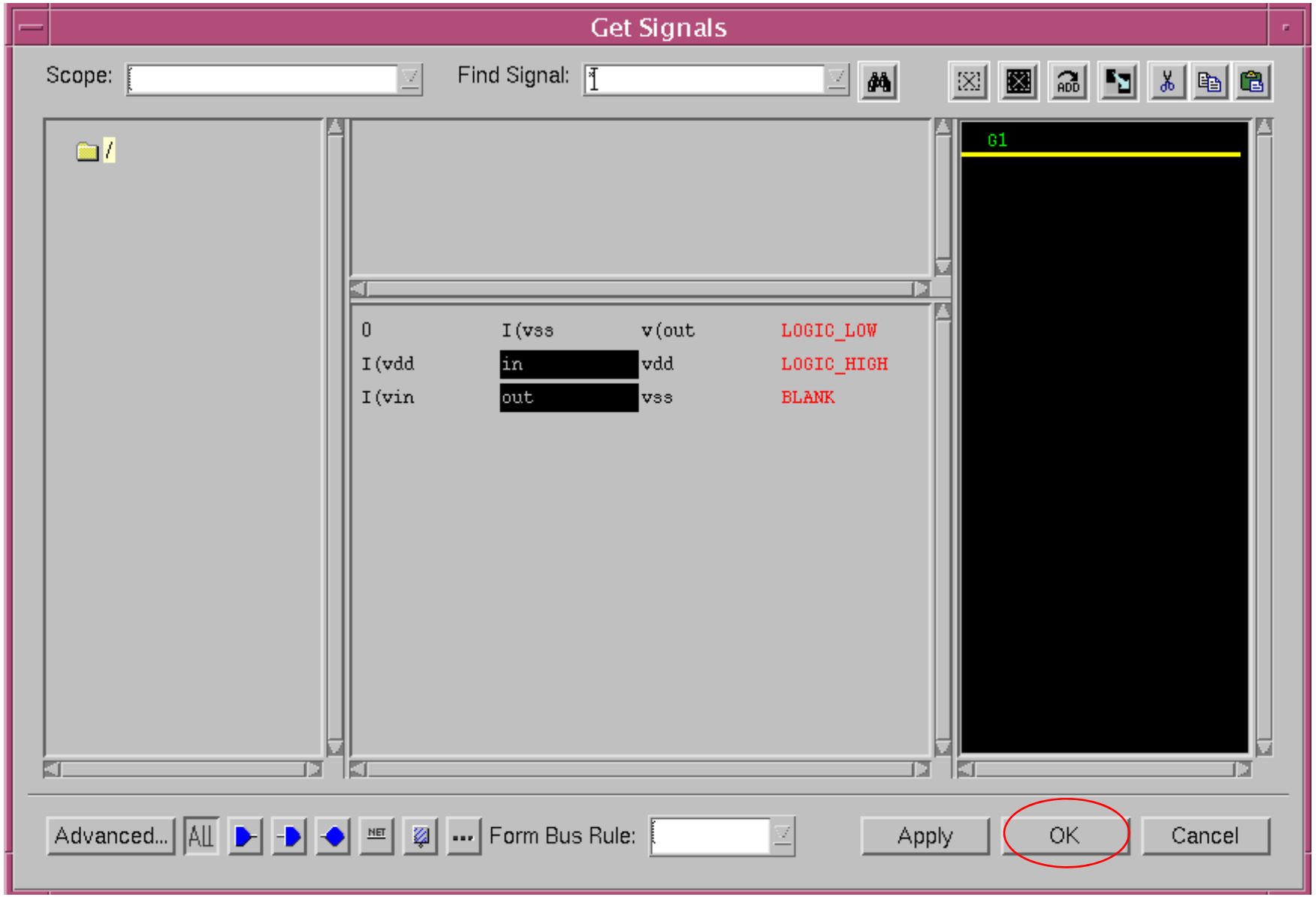
Waveform File(.tr0)

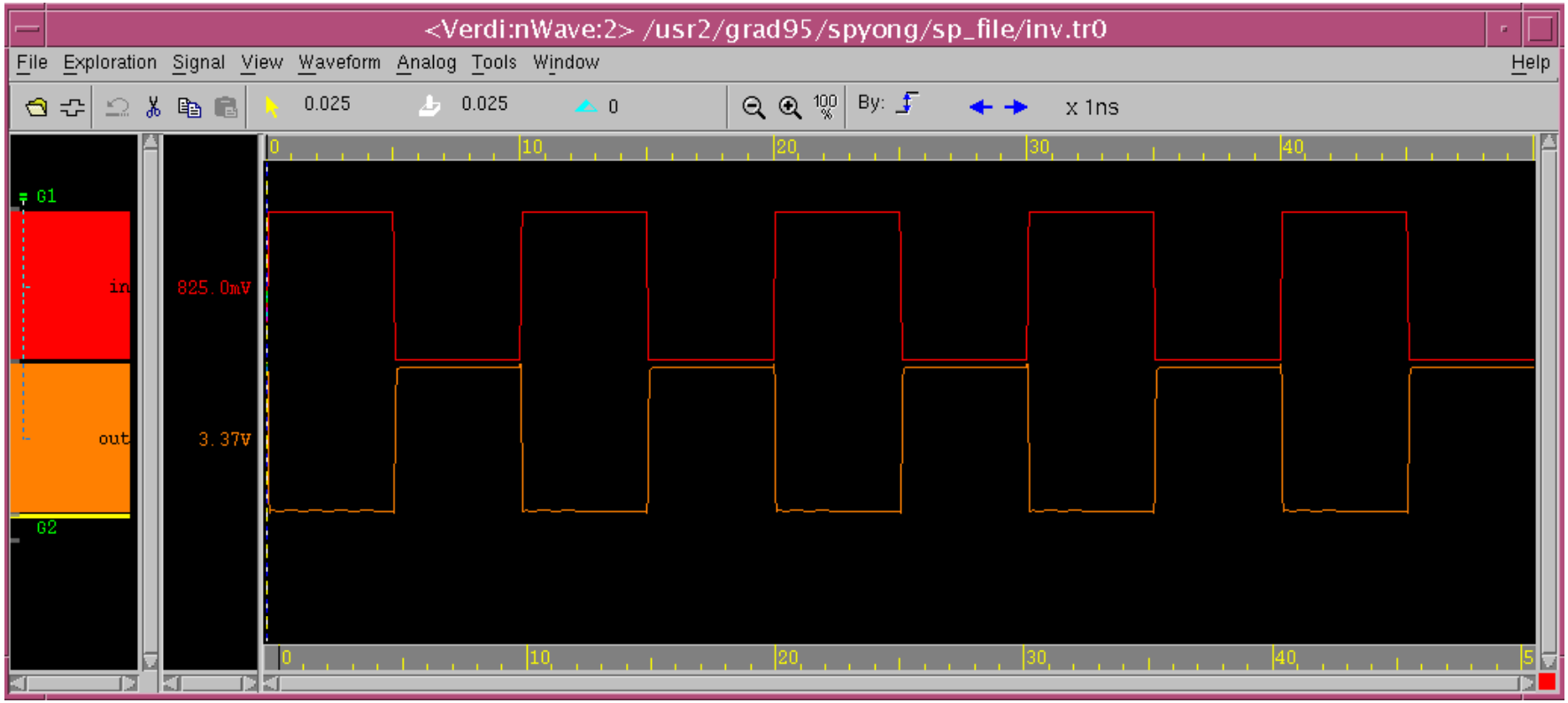


Get Signals

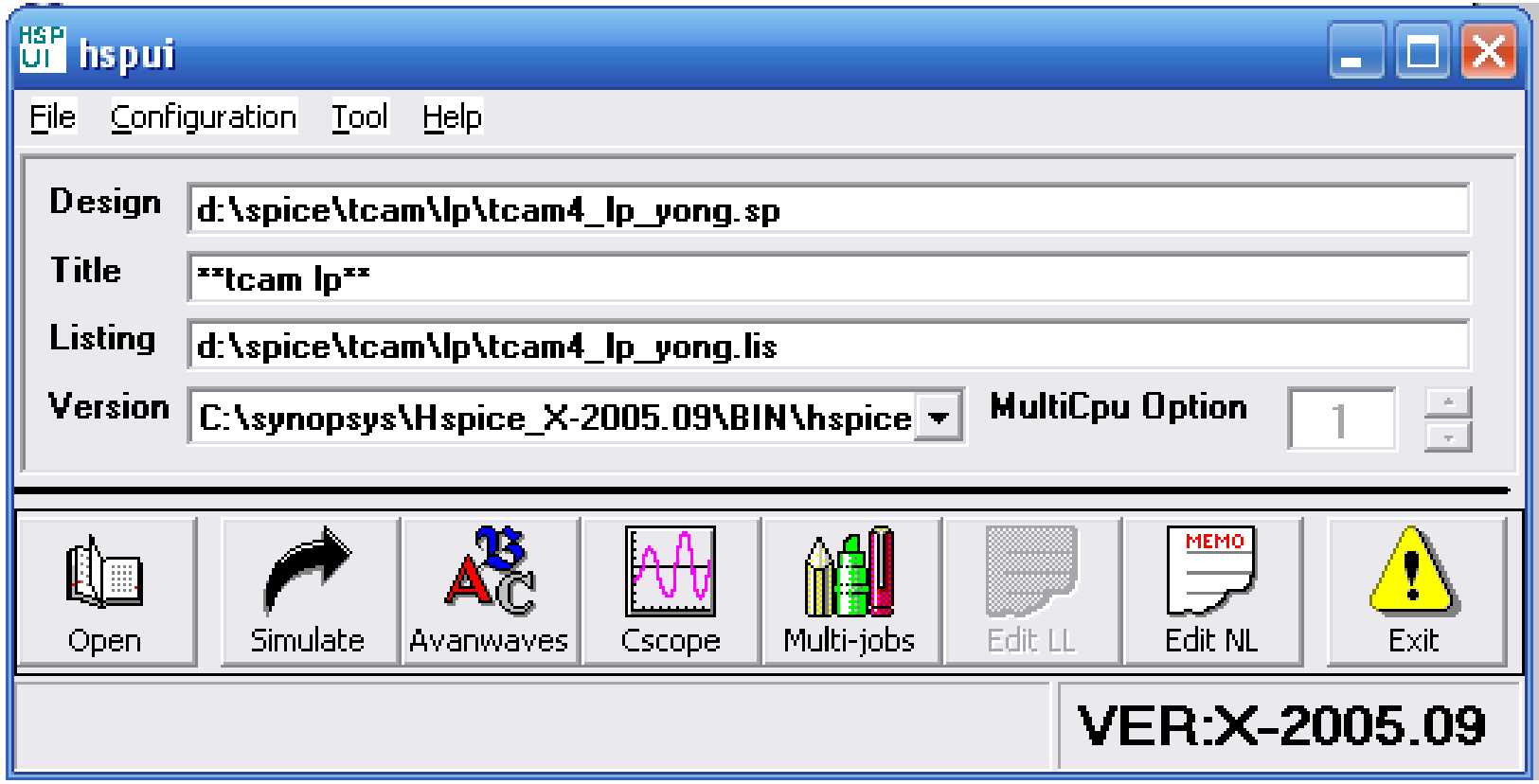



<Verdi:nWave:2> /usr2/grad95/spyong/sp_file/inv.tr0
File Exploration Signal View Waveform Analog Tools Window Help
0.025
0.025
0
x 1ns
G1
1.0
2.0
3.0
4.0
5.0
0
10
20
30
40

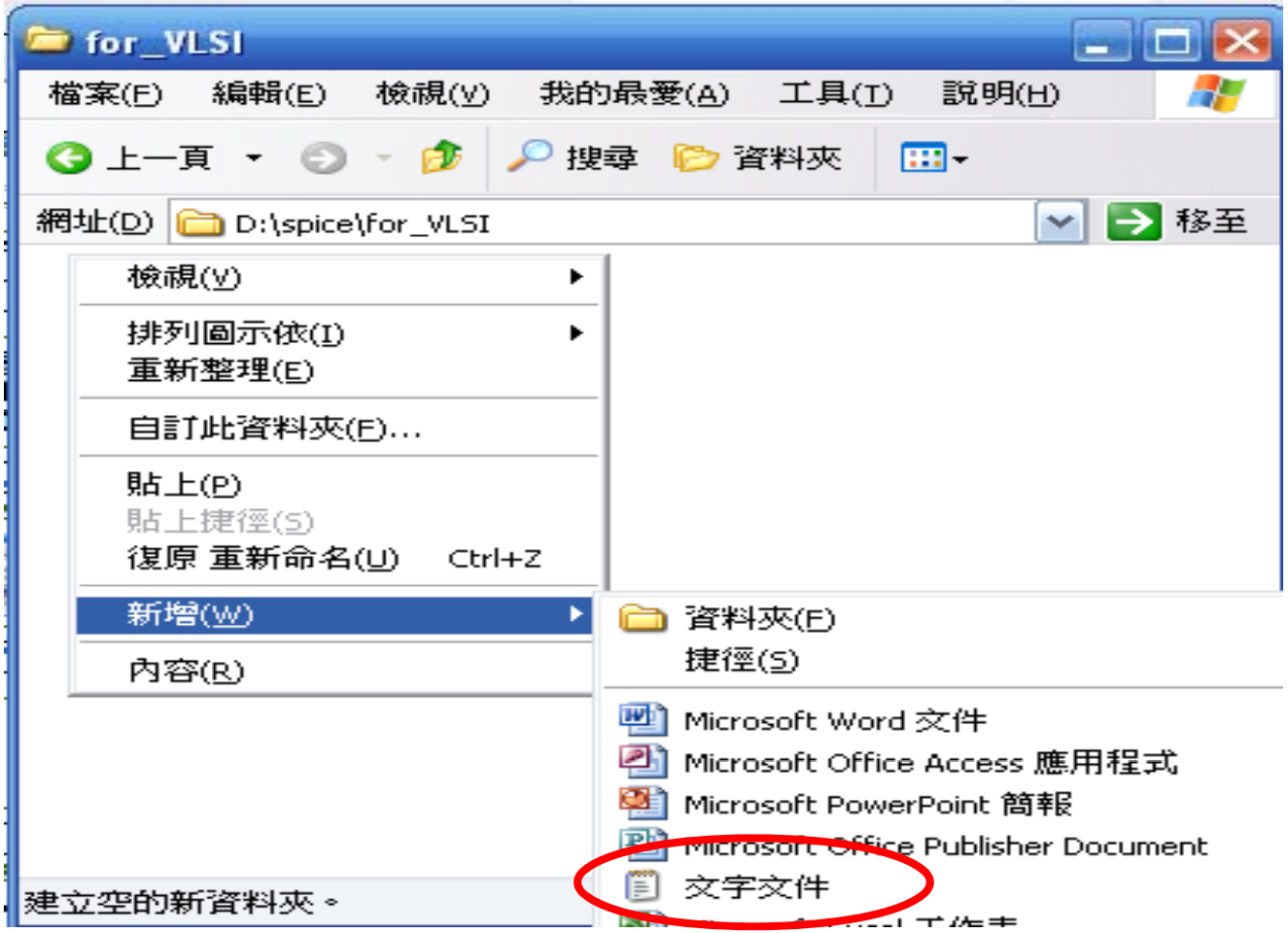

Get Signals
Scope:
Find Signal:
/
G1
0 I(vss v(out LOGIC_LOW
I(vdd in vdd LOGIC_HIGH
I(vin out vss BLANK
Advanced...
All
Form Bus Rule:
Apply
OK
Cancel


<Verdi:nWave:2> /usr2/grad95/spyong/sp_file/inv.tr0
File Exploration Signal View Waveform Analog Tools Window Help
0.025
0.025
0
By:
x 1ns
G1
in
out
G2
825.0mV
3.37V
0
10
20
30
40

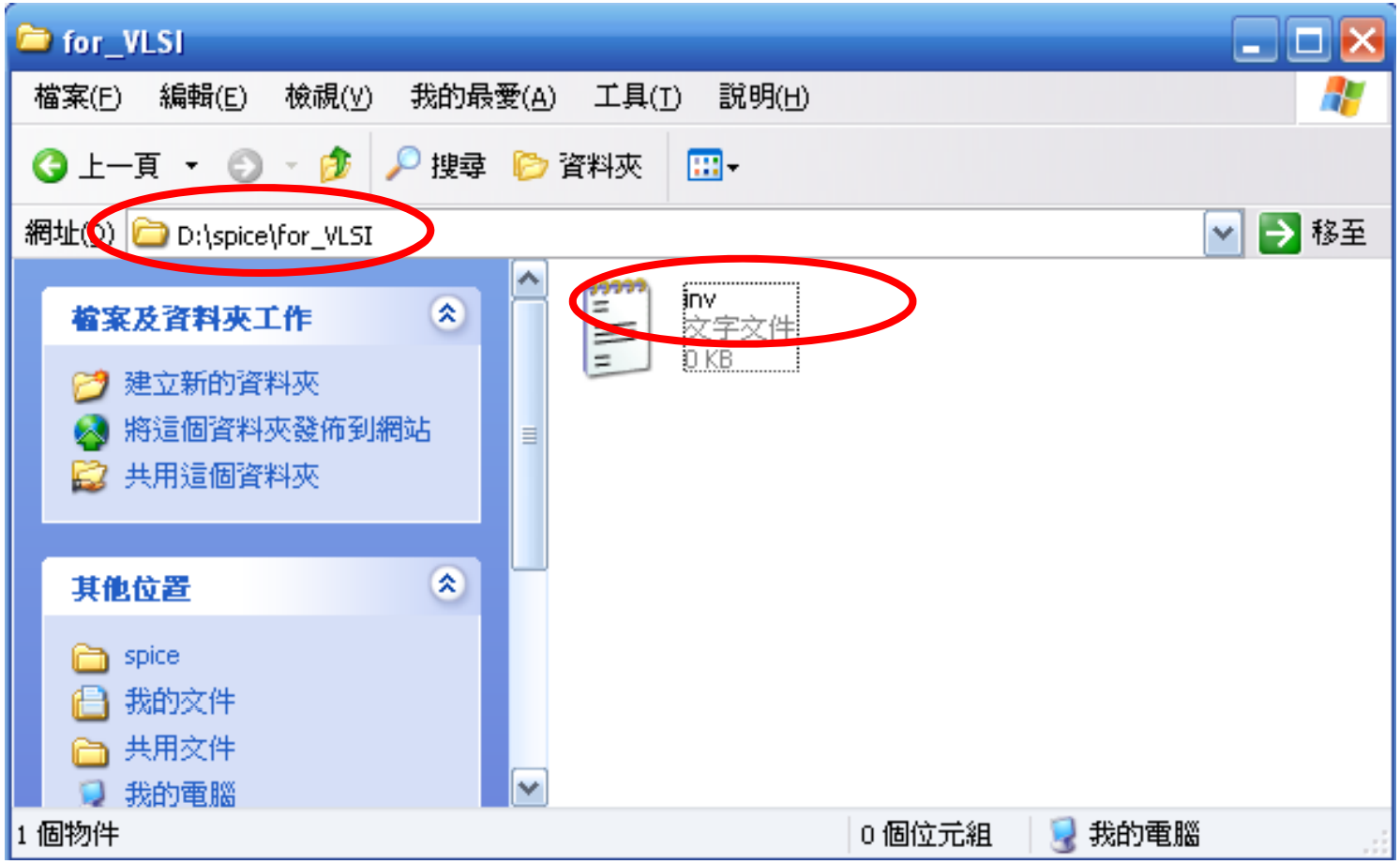
PC_Hspice 介面

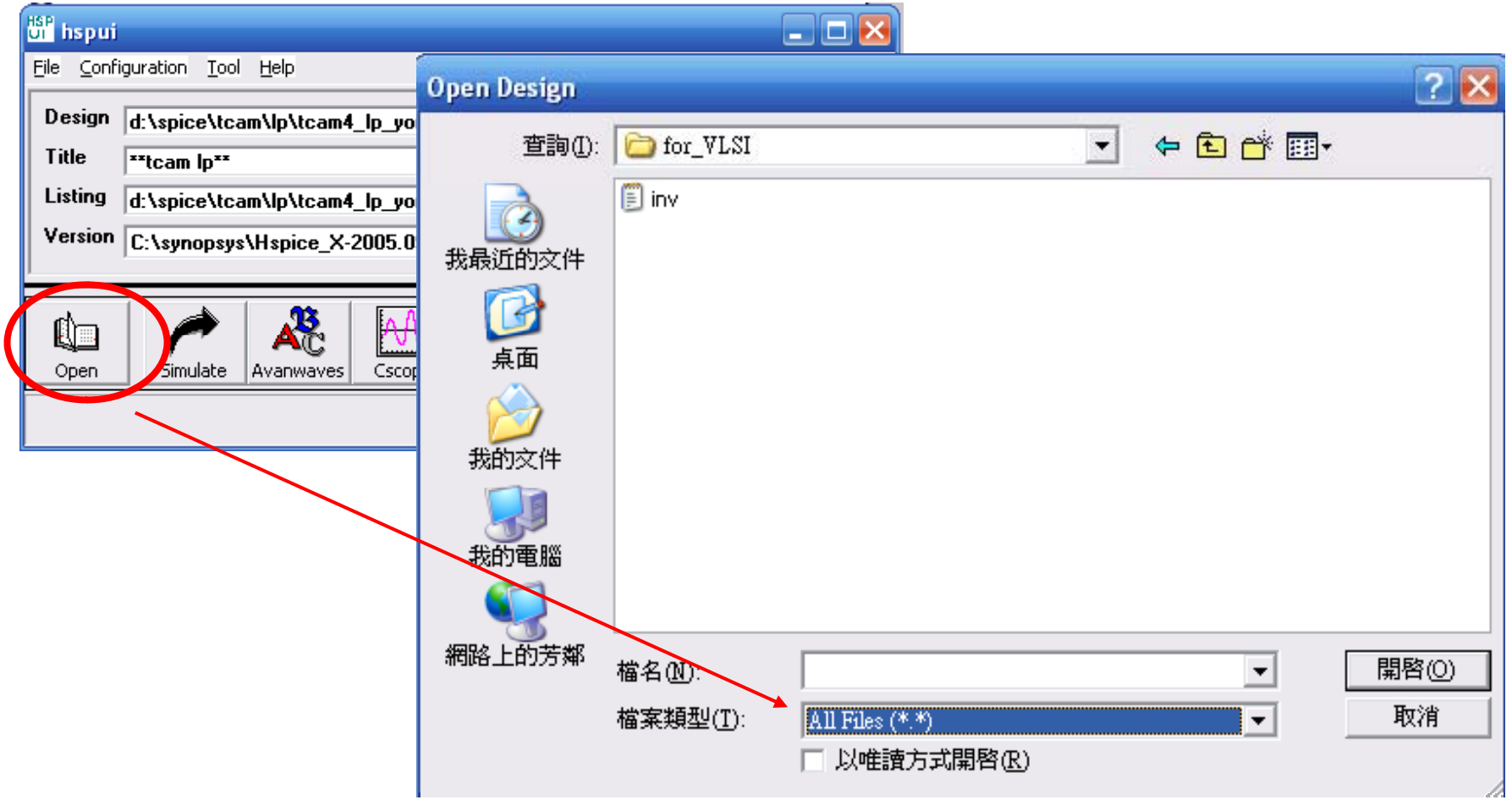

hspui
File
Configuration
Tool
Help
Design
d:\spice\tcam\lp\tcam4_lp_yong.sp
Title
tcam lp
Listing
d:\spice\tcam\lp\tcam4_lp_yong.lis
Version
C:\synopsys\Hspice_X-2005.09\BIN\hspice
MultiCpu Option
1
Open
Simulate
Avanwaves
Cscope
Multi-jobs
Edit LL
MEMO
Edit NL
Exit
VER:X-2005.09

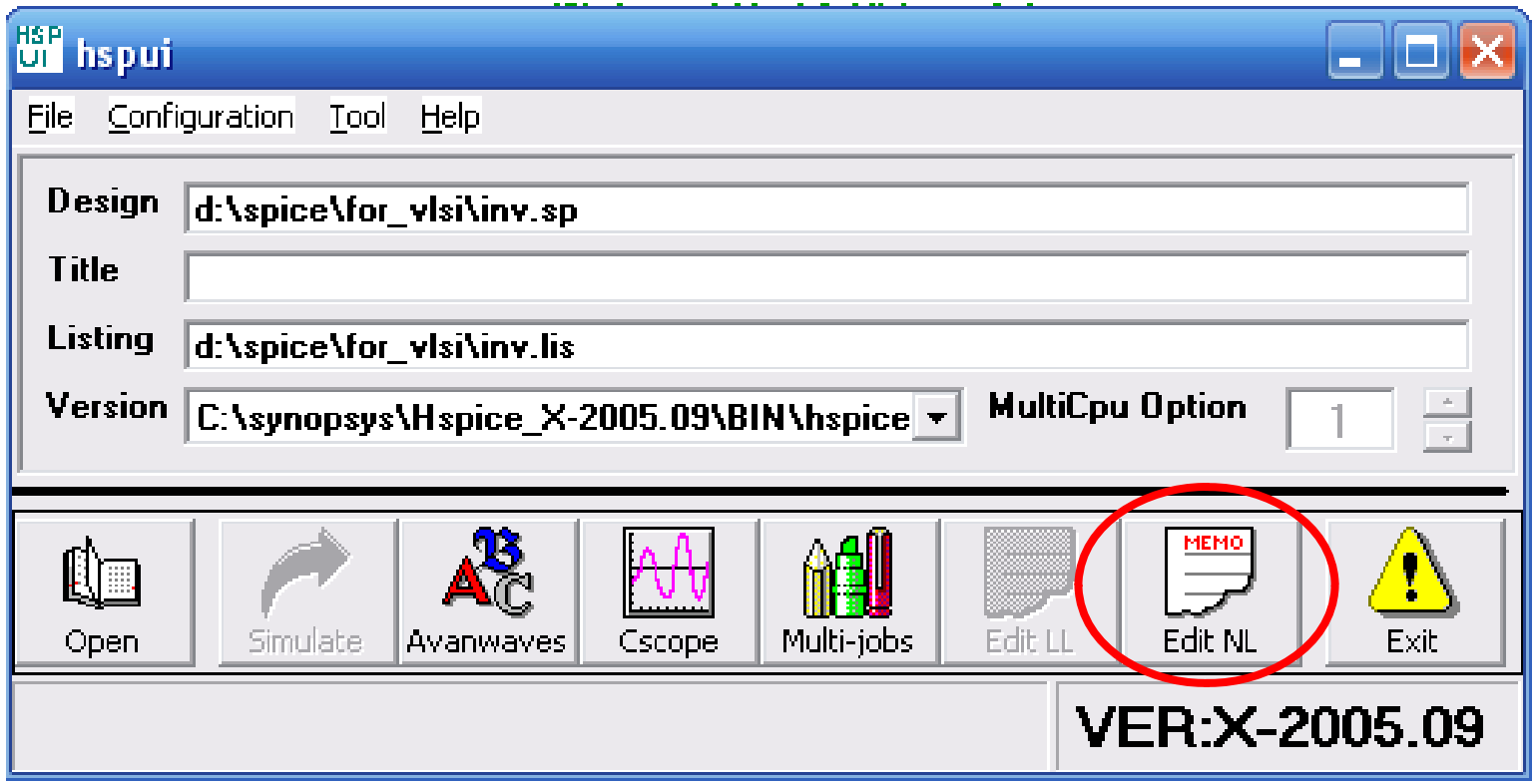
建立一個新的sp檔案


for_VLSI
檔案(F) 編輯(E) 檢視(V) 我的最愛(A) 工具(T) 說明(H)
上一頁 搜尋 資料夾
網址(D) D:\spice\for_VLSI 移至
檢視(V)
排列圖示依(I)
重新整理(E)
自訂此資料夾(F)...
貼上(P)
貼上捷徑(S)
復原 重新命名(U) Ctrl+Z
新增(W)
內容(R)
資料夾(F)
捷徑(S)
Microsoft Word 文件
Microsoft Office Access 應用程式
Microsoft PowerPoint 簡報
Microsoft Office Publisher Document
文字文件
建立空的新資料夾。

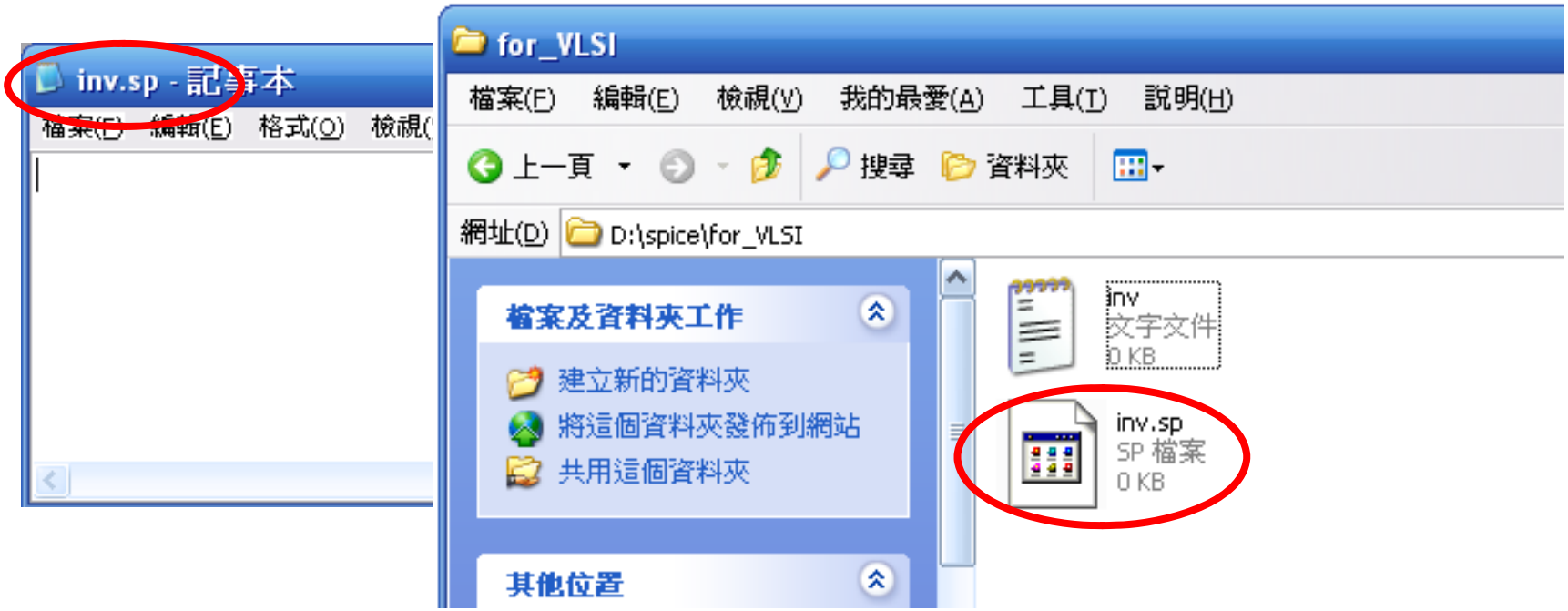
英文路徑 英文檔名

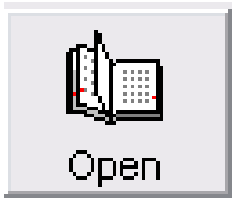

for_VLSI
檔案(F) 編輯(E) 檢視(V) 我的最愛(A) 工具(T) 說明(H)
上一頁
搜尋
資料夾
網址(D) D:\spice\for_VLSI
移至
檔案及資料夾工作
建立新的資料夾
將這個資料夾發佈到網站
共用這個資料夾
其他位置
spice
我的文件
共用文件
我的電腦
inv
文字文件
0 KB
1 個物件
0 個位元組
我的電腦


hspui
File
Configuration
Tool
Help
Design
d:\spice\tcam\lp\tcam4_lp_yo
Title
tcam lp
Listing
d:\spice\tcam\lp\tcam4_lp_yo
Version
C:\synopsys\Hspice_X-2005.0
Open
Simulate
Avanwaves
Open Design
查詢(I):
for_VLSI
inv
我最近的文件
桌面
我的文件
我的電腦
網路上的芳鄰
檔名(N):
檔案類型(T):
All Files (*.*)
以唯讀方式開啓(R)
開啓(O)
取消


hspui
File
Configuration
Tool
Help
Design
d:\spice\for_vlsi\inv.sp
Title
Listing
d:\spice\for_vlsi\inv.lis
Version
C:\synopsys\Hspice_X-2005.09\BIN\hspice
MultiCpu Option
1
Open
Simulate
Avanwaves
Cscope
Multi-jobs
Edit LL
MEMO
Edit NL
Exit
VER:X-2005.09

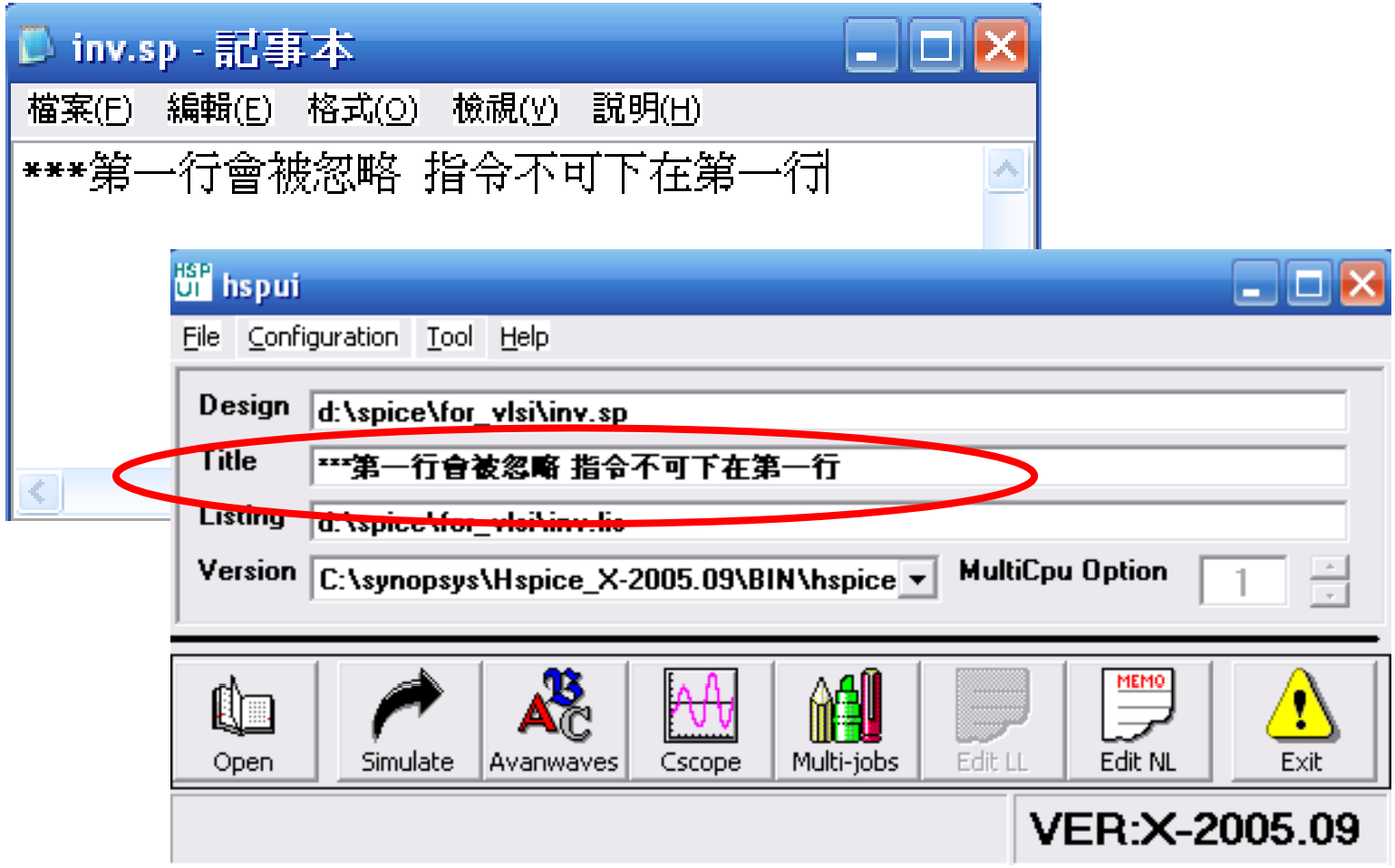

未命名 - 記事本
檔案(F) 編輯(E) 格式(O) 檢視(V) 說明(H)
記事本
找不到 d:\spice\for_vlsi\inv.sp 檔案。
是否要建立新的檔案?
是(Y)
否(N)
取消





以後直接複製sp檔，重新命名為想要的檔名，open後即可利用edit NL去更改sp檔內容

Editing


inv.sp - 記事本
檔案(F) 編輯(E) 格式(O) 檢視(V) 說明(H)
***第一行會被忽略 指令不可下在第一行
hspui
File Configuration Tool Help
Design d:\spice\for_vlsi\inv.sp
Title ***第一行會被忽略 指令不可下在第一行
Listing
Version C:\synopsys\Hspice_X-2005.09\BIN\hspice
MultiCpu Option 1
Open
Simulate
Avanwaves
Cscope
Multi-jobs
Edit LL
Edit NL
Exit
VER:X-2005.09