Full-Custom Layout

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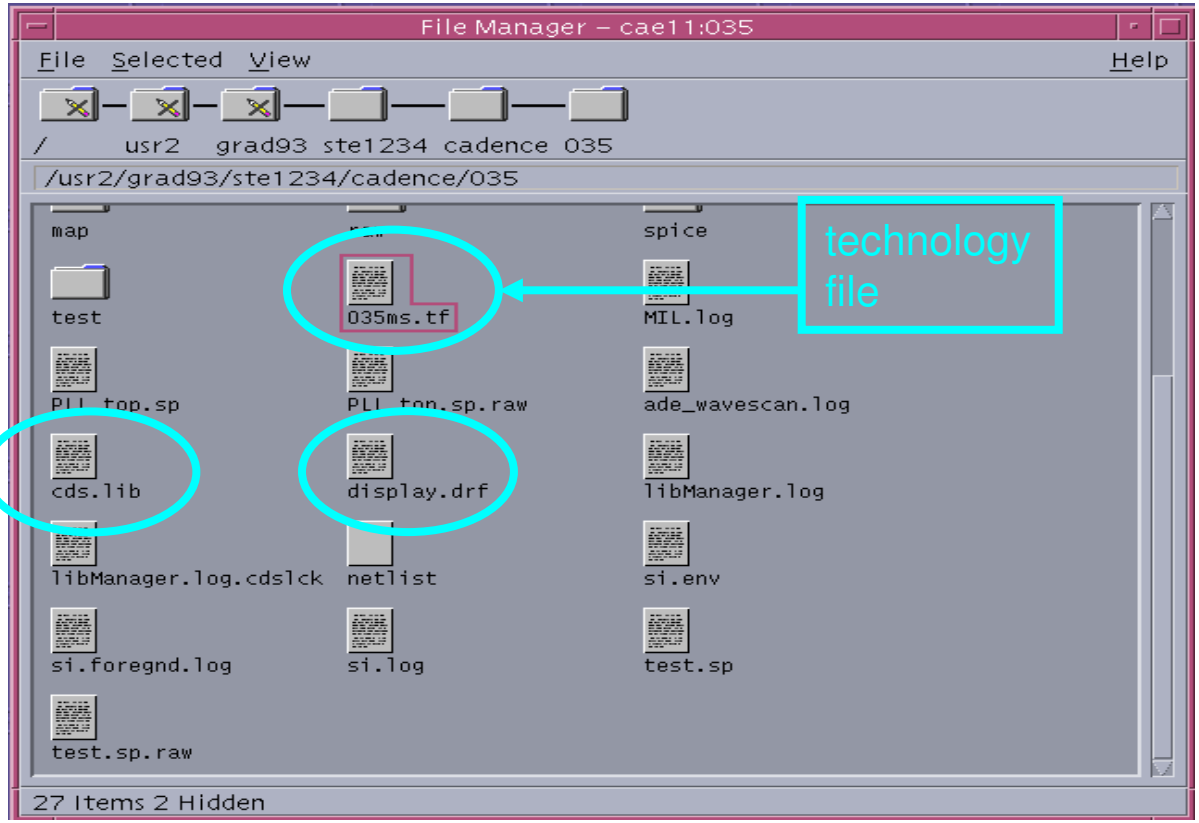
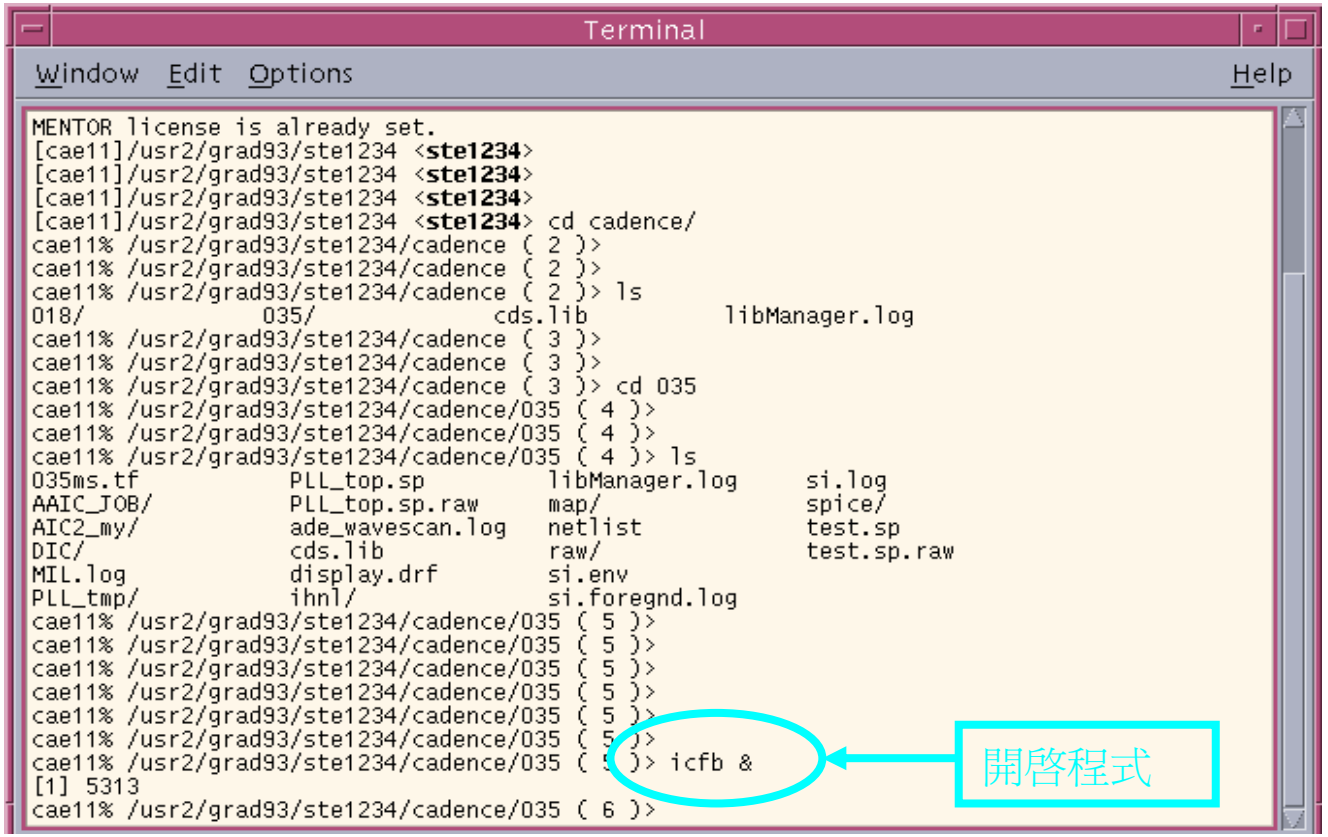
TA : C.–H. Wu

Environment Setting

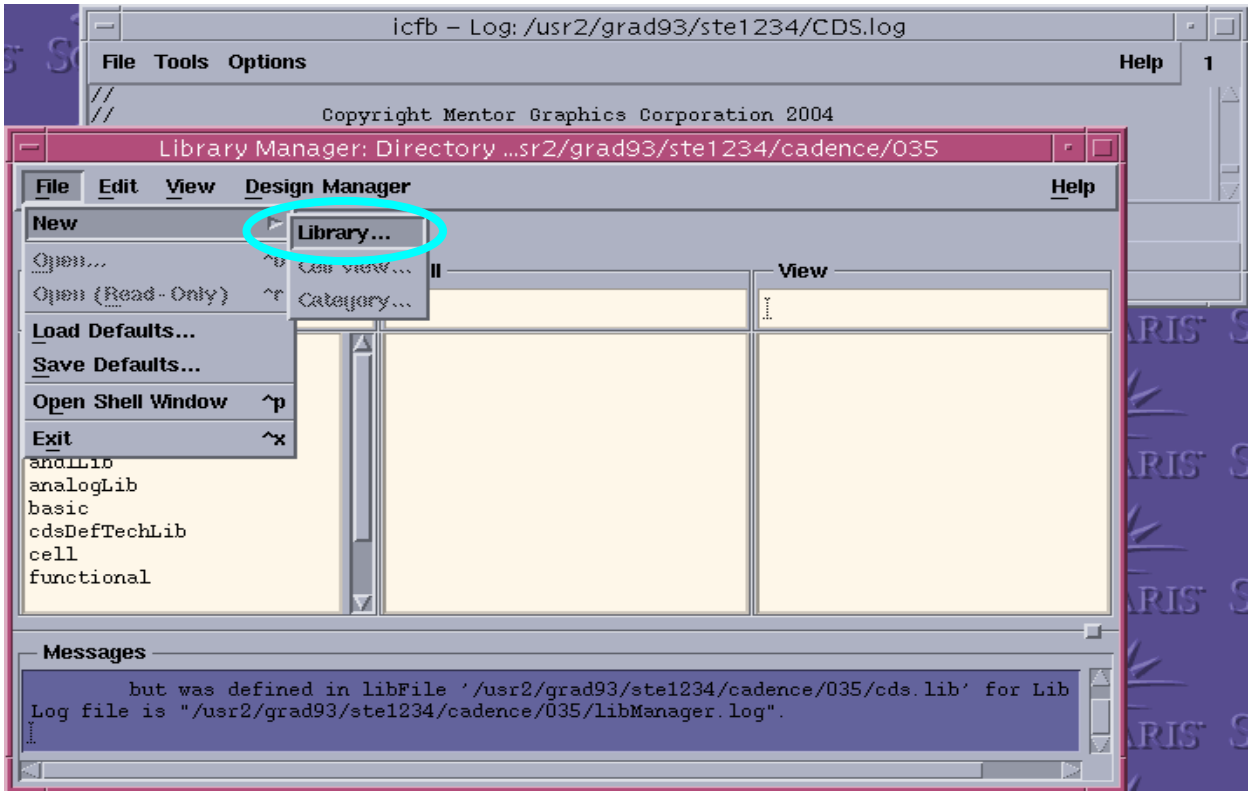


Advanced Reliable Systems (ARES) Lab.

Open Tool

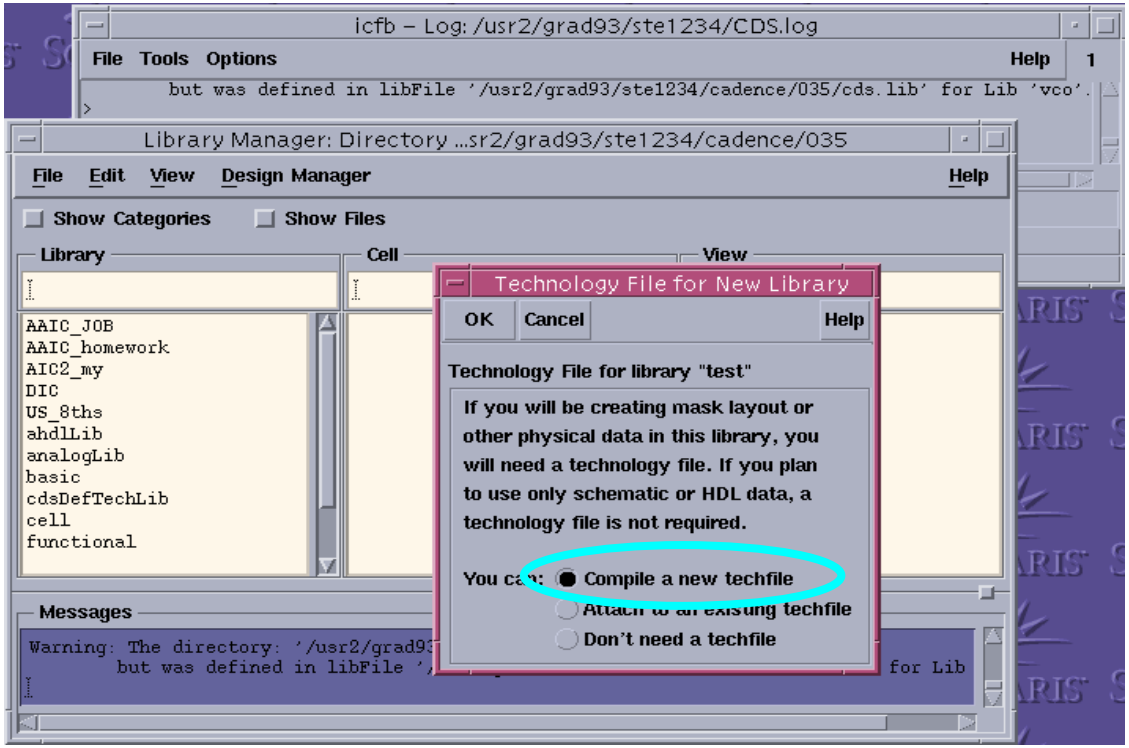

Terminal
Window Edit Options Help
MENTOR license is already set.
[cae11]/usr2/grad93/ste1234 <ste1234>
[cae11]/usr2/grad93/ste1234 <ste1234>
[cae11]/usr2/grad93/ste1234 <ste1234>
[cae11]/usr2/grad93/ste1234 <ste1234> cd cadence/
cae11% /usr2/grad93/ste1234/cadence (2)>
cae11% /usr2/grad93/ste1234/cadence (2)>
cae11% /usr2/grad93/ste1234/cadence (2)> ls
018/ 035/ cds.lib libManager.log
cae11% /usr2/grad93/ste1234/cadence (3)>
cae11% /usr2/grad93/ste1234/cadence (3)>
cae11% /usr2/grad93/ste1234/cadence (3)> cd 035
cae11% /usr2/grad93/ste1234/cadence/035 (4)>
cae11% /usr2/grad93/ste1234/cadence/035 (4)>
cae11% /usr2/grad93/ste1234/cadence/035 (4)> ls
035ms.tf PLL_top.sp libManager.log si.log
AAIC_JOB/ PLL_top.sp.raw map/ spice/
AIC2_my/ ade_wavescan.log netlist test.sp
DIC/ cds.lib raw/ test.sp.raw
MIL.log display.drf si.env
PLL_tmp/ ihnl/ si.foregnd.log
cae11% /usr2/grad93/ste1234/cadence/035 (5)>
cae11% /usr2/grad93/ste1234/cadence/035 (5)>
cae11% /usr2/grad93/ste1234/cadence/035 (5)>
cae11% /usr2/grad93/ste1234/cadence/035 (5)>
cae11% /usr2/grad93/ste1234/cadence/035 (5)>
cae11% /usr2/grad93/ste1234/cadence/035 (5)>
cae11% /usr2/grad93/ste1234/cadence/035 (5)> icfb &
[1] 5313
cae11% /usr2/grad93/ste1234/cadence/035 (6)>
開啓程式

Create Library



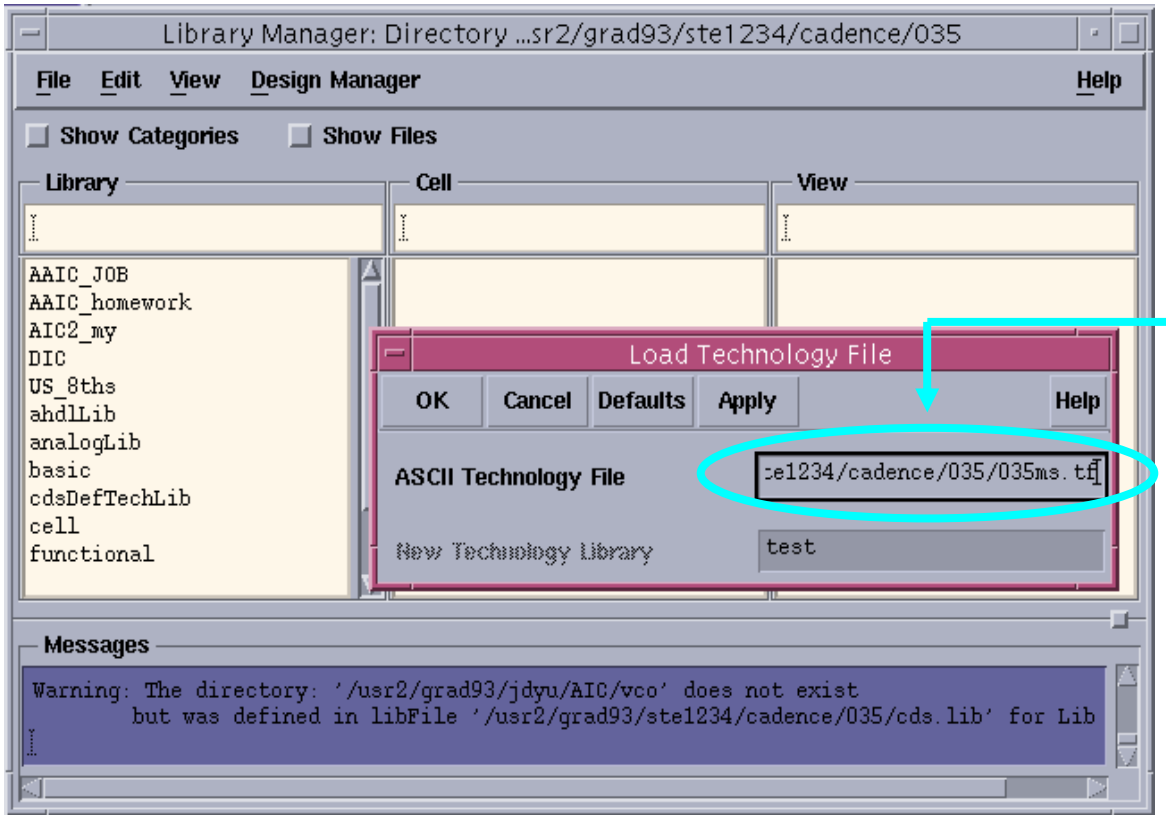
Create Library (cont.)

- After enter the library name



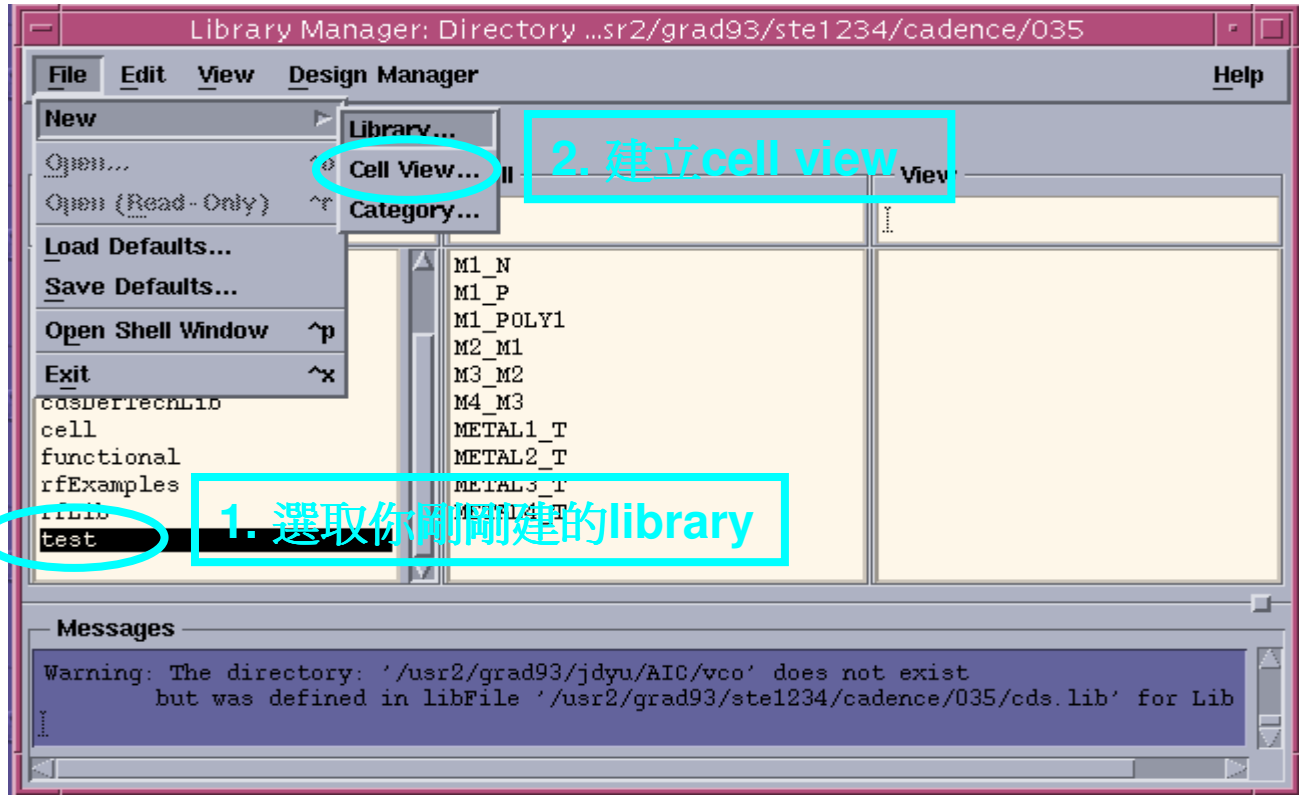
Advanced Reliable Systems (ARES) Lab.

Create Library (cont.)

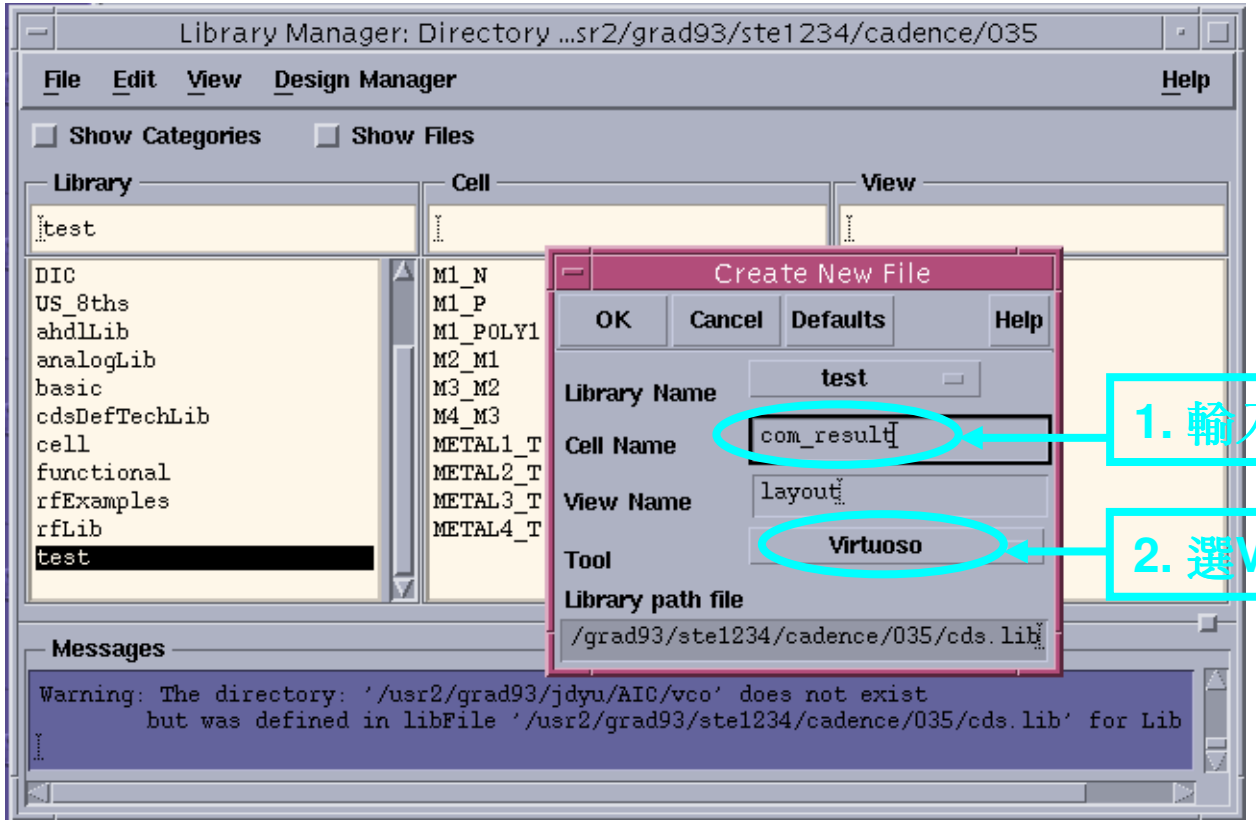


輸入technology file的路徑

Create Cell_View

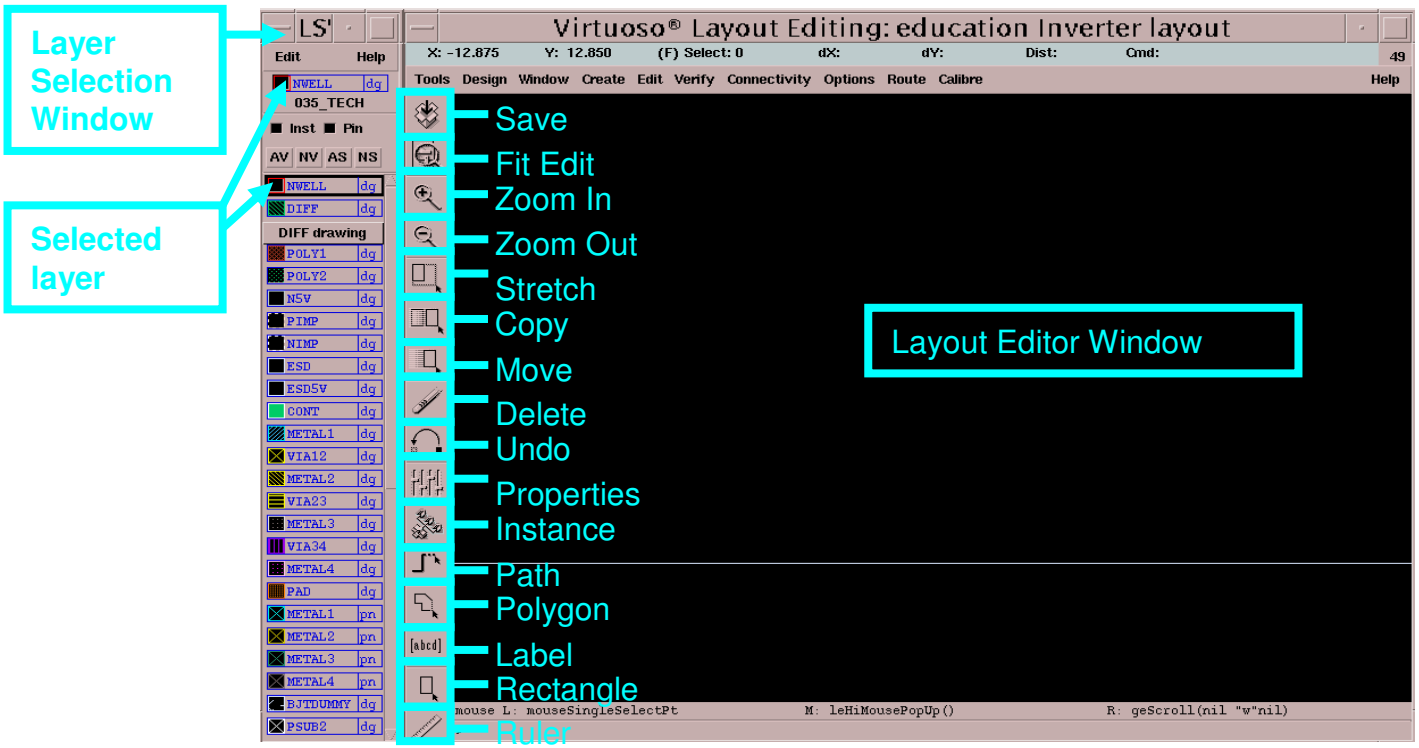


Create Cell_View (cont.)



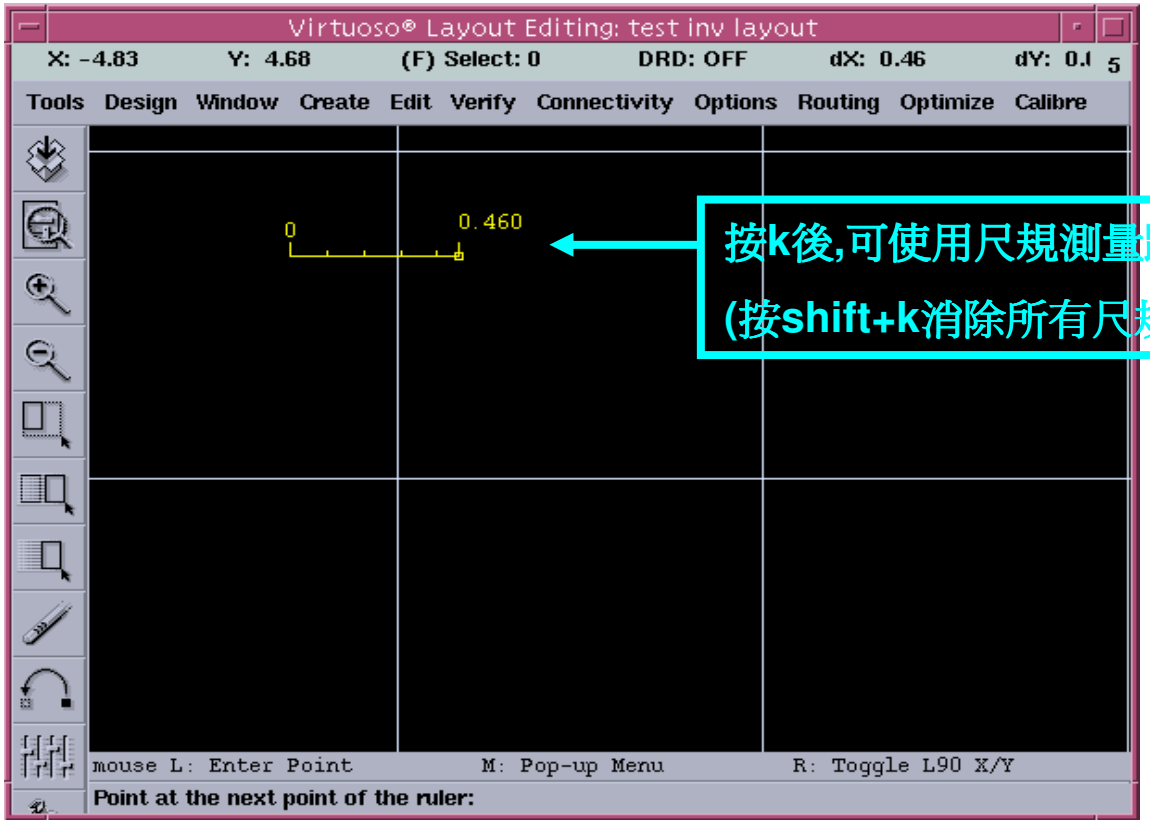
Environment

- Introduction of the option environment



Advanced Reliable Systems (ARES) Lab.

Environment (cont.)

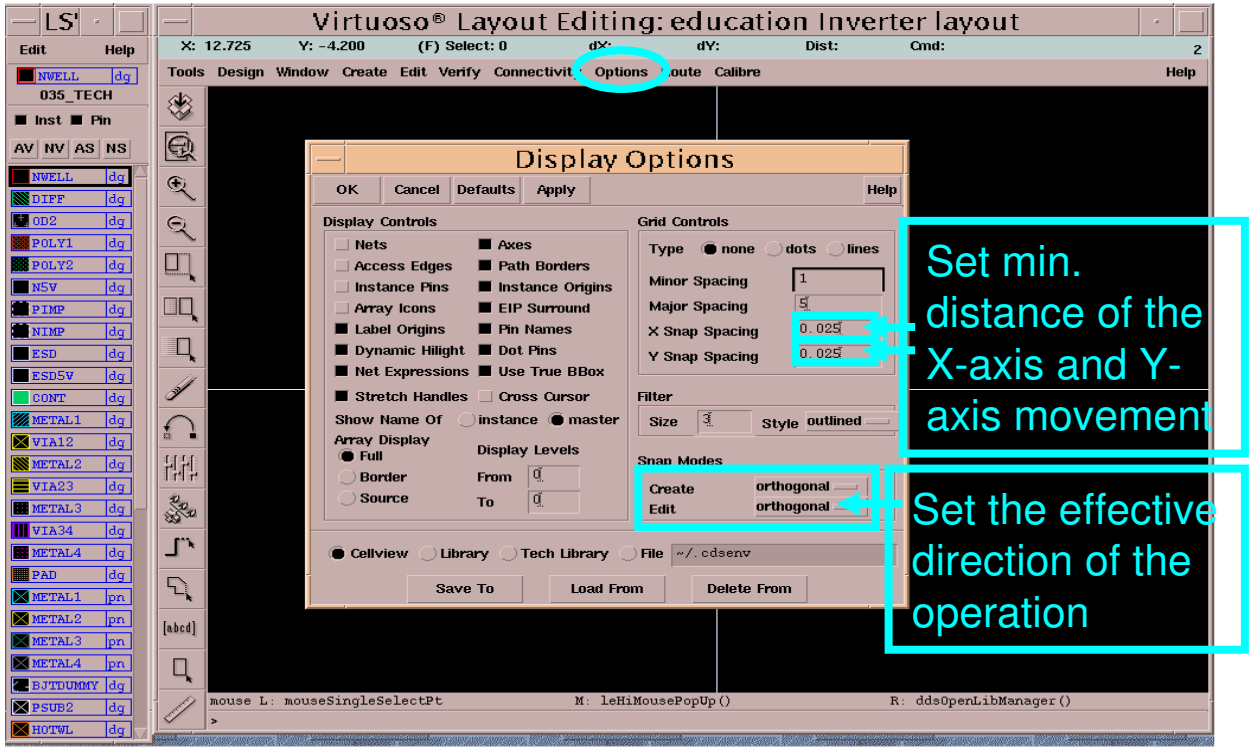


按k後,可使用尺規測量距離(um)

(按shift+k消除所有尺規)

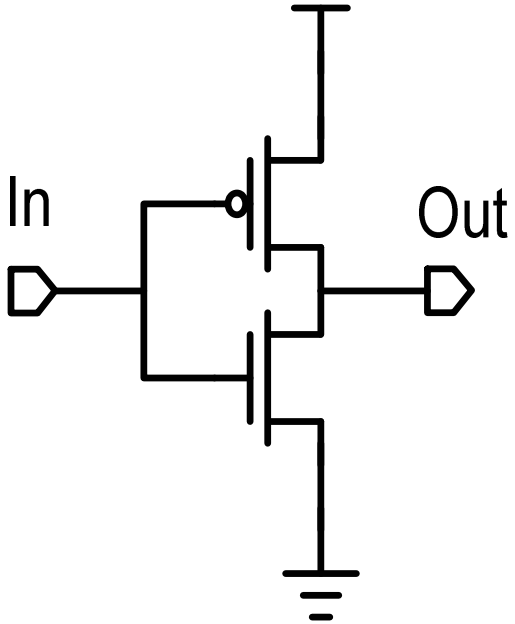
Environment (cont.)

- Options->Display



Inverter Layout

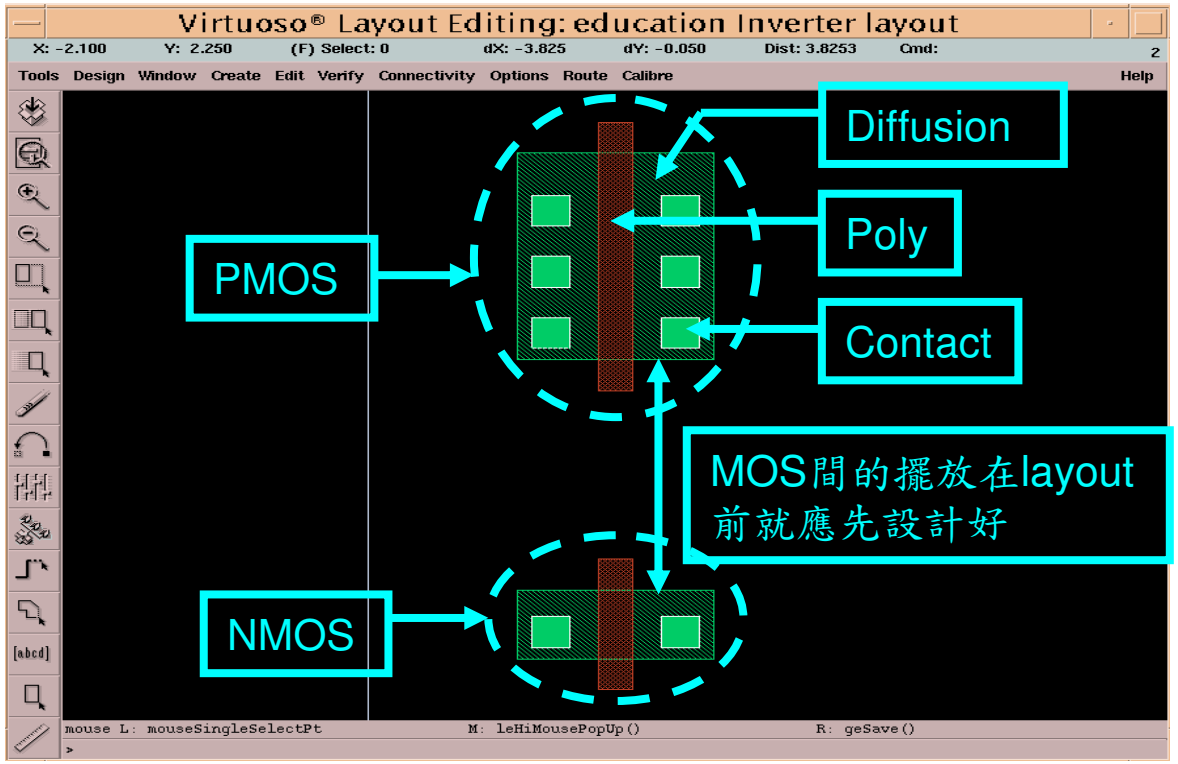
- Practice goal:
  - Understand the layout option environment
  - Accomplish a inverter circuit layout
- Content:
  - Virtuoso Layout Editor
  - Inverter Layout implement
  - Calibre
    - DRC
    - LVS



Inverter

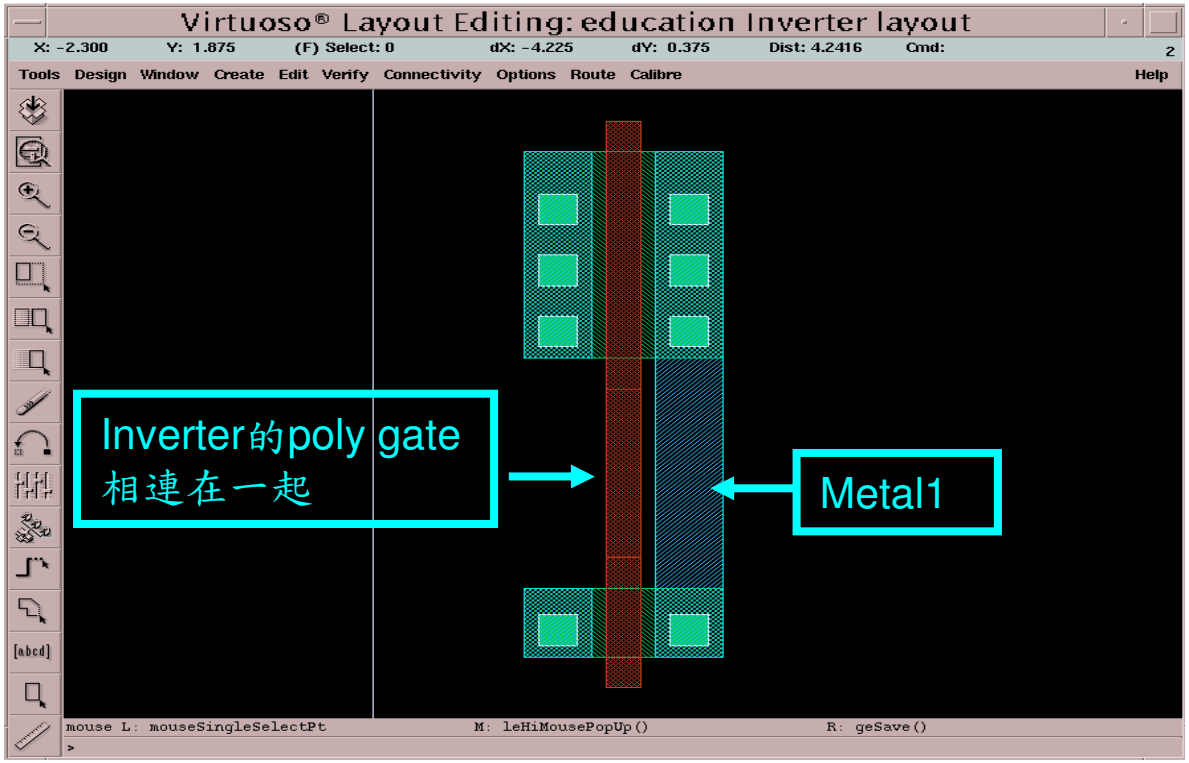
Inverter Layout (cont.)

- 先畫出 PMOS and NMOS



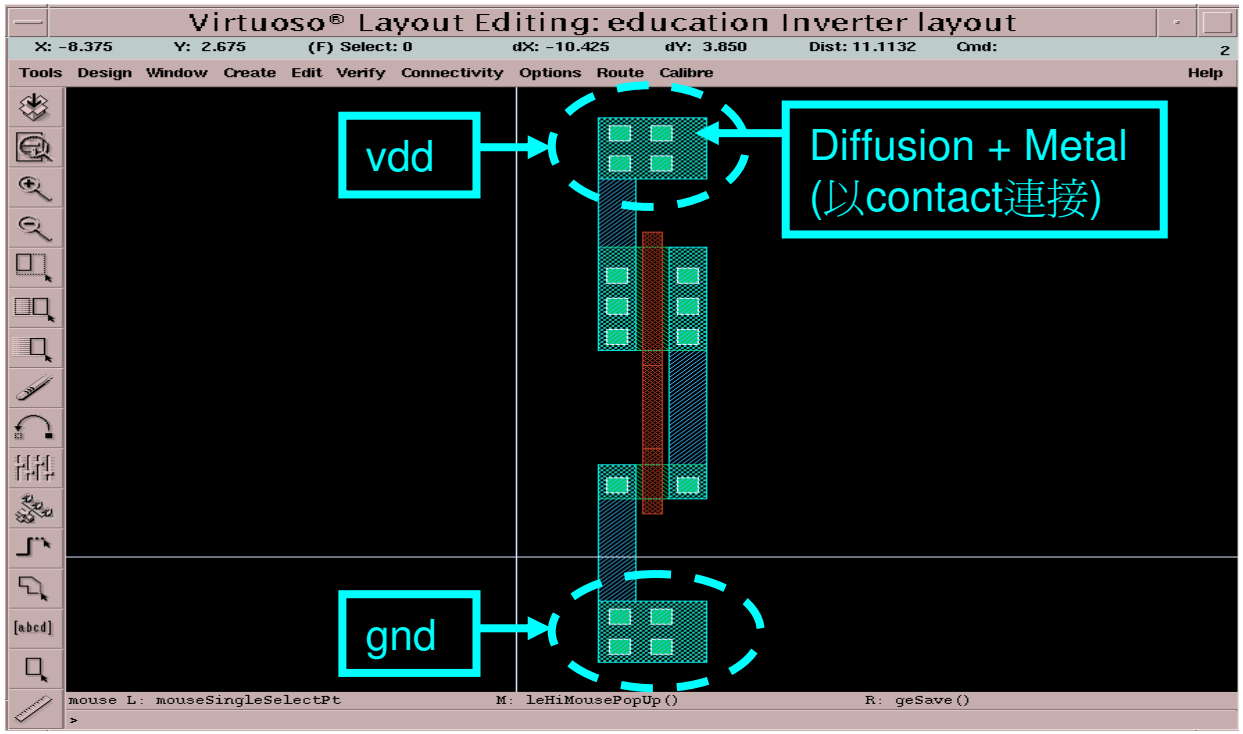
Inverter Layout (cont.)

- 將兩個MOS的drain端用metal連接



Inverter Layout (cont.)

- 在MOS的source端分別加上vdd和gnd的DIFF層

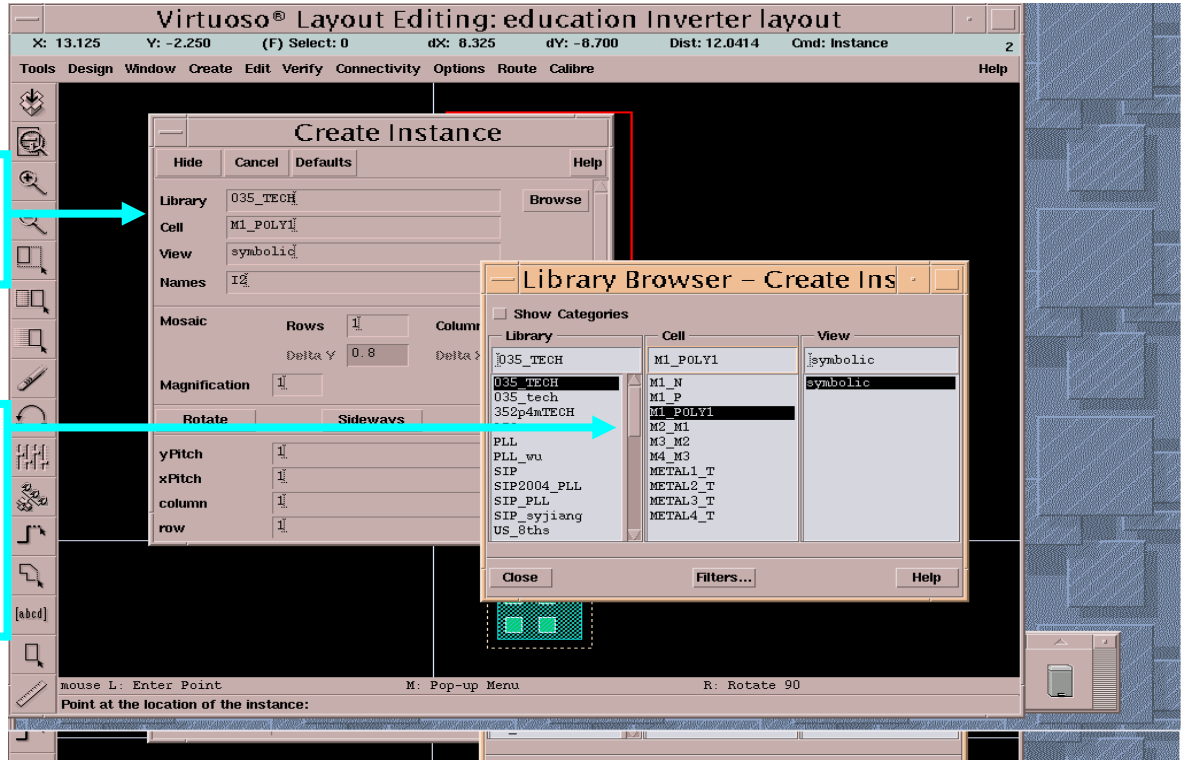


Inverter Layout (cont.)

- 呼叫tech. file內部原有的cell來使用

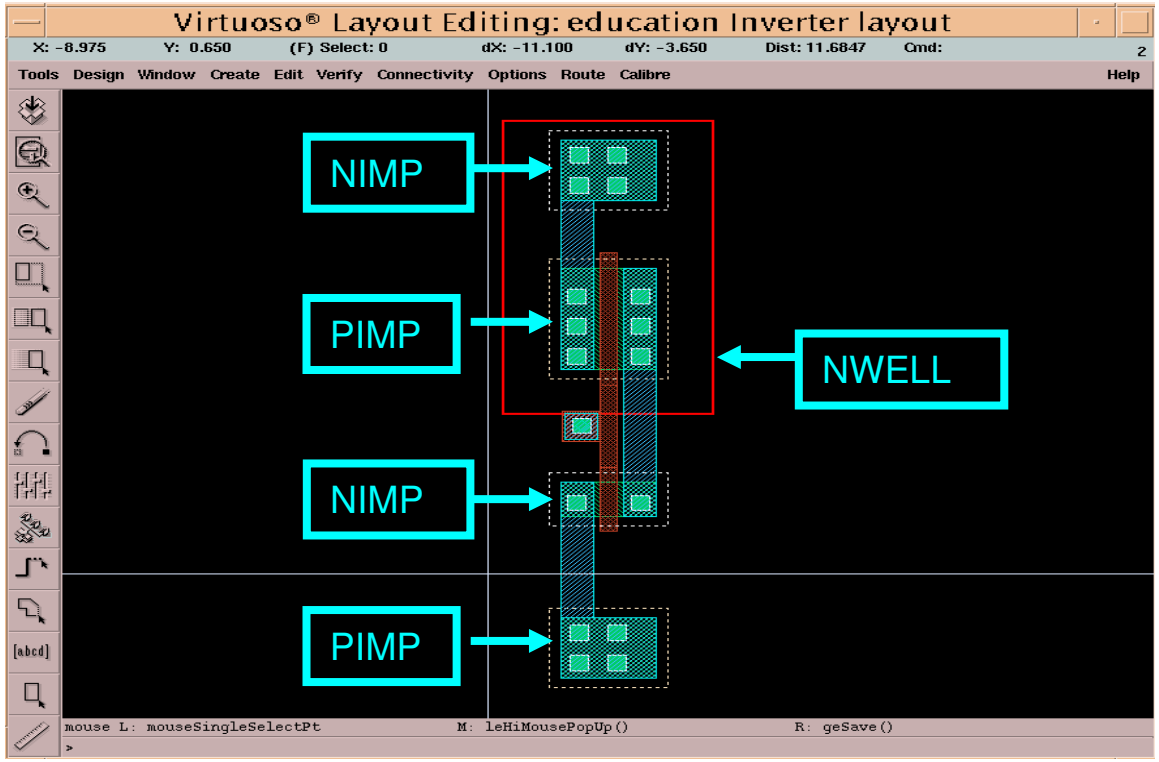
利用熱鍵"i"
呼叫此視窗

可呼叫出打上
contact和via的
poly或是metal
層(熱鍵 "o")



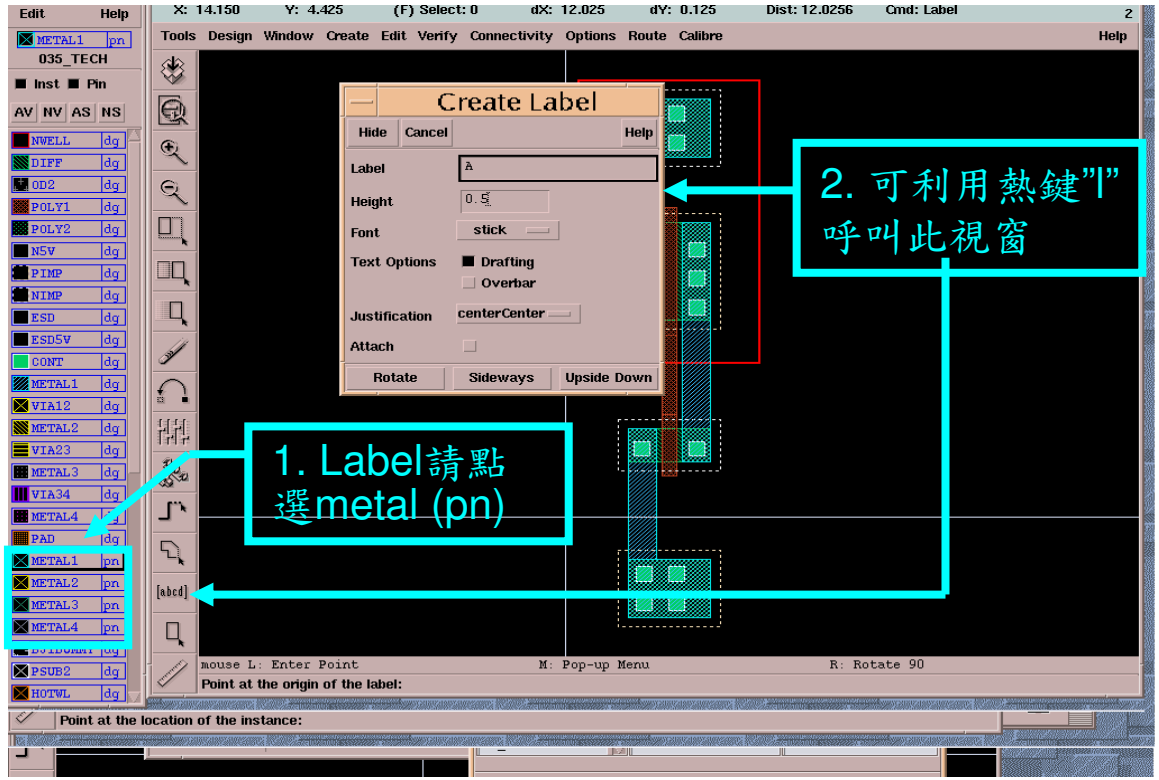
Inverter Layout (cont.)

- 加上PIMP、NIMP和NWELL層



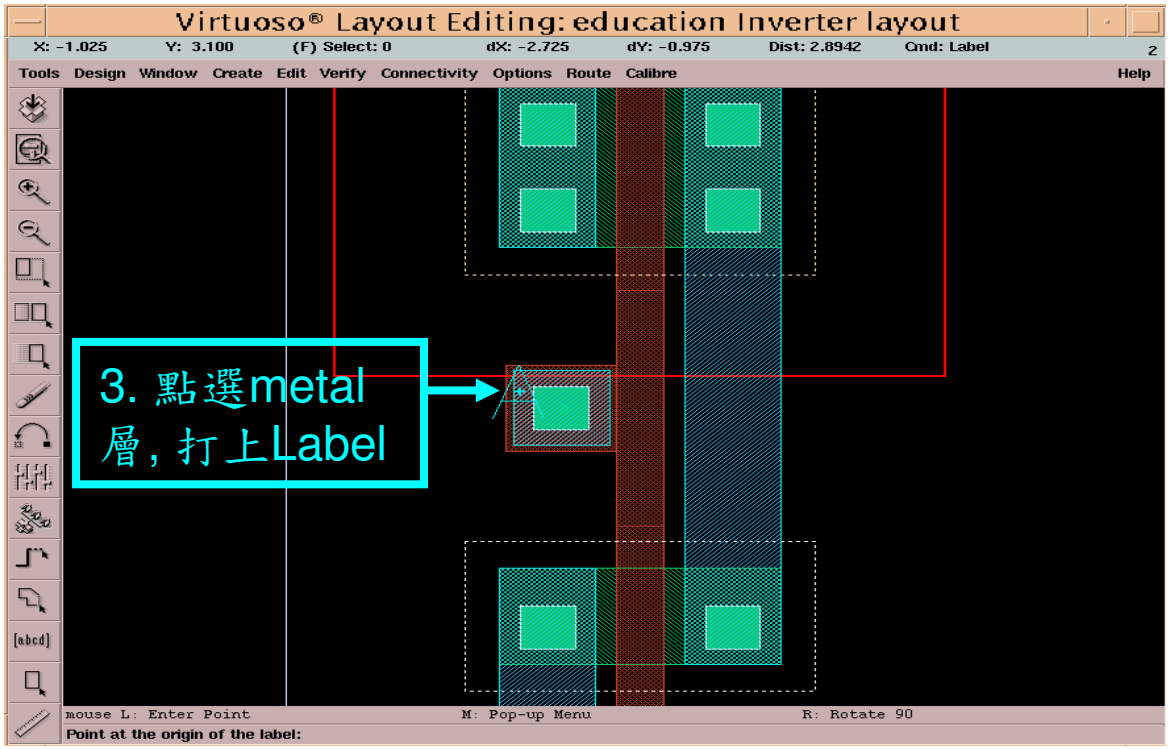
Inverter Layout (cont.)

- 在vdd、gnd和輸入輸出點打上label



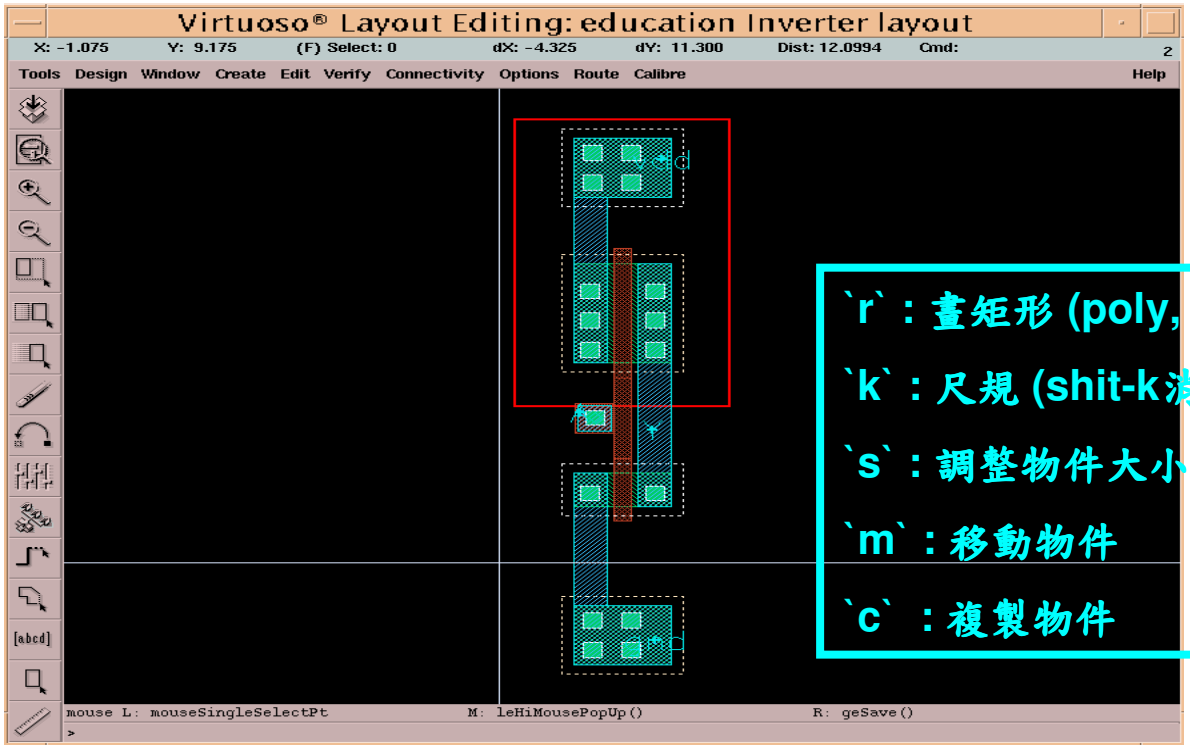
Inverter Layout (cont.)

- 打上label後的結果



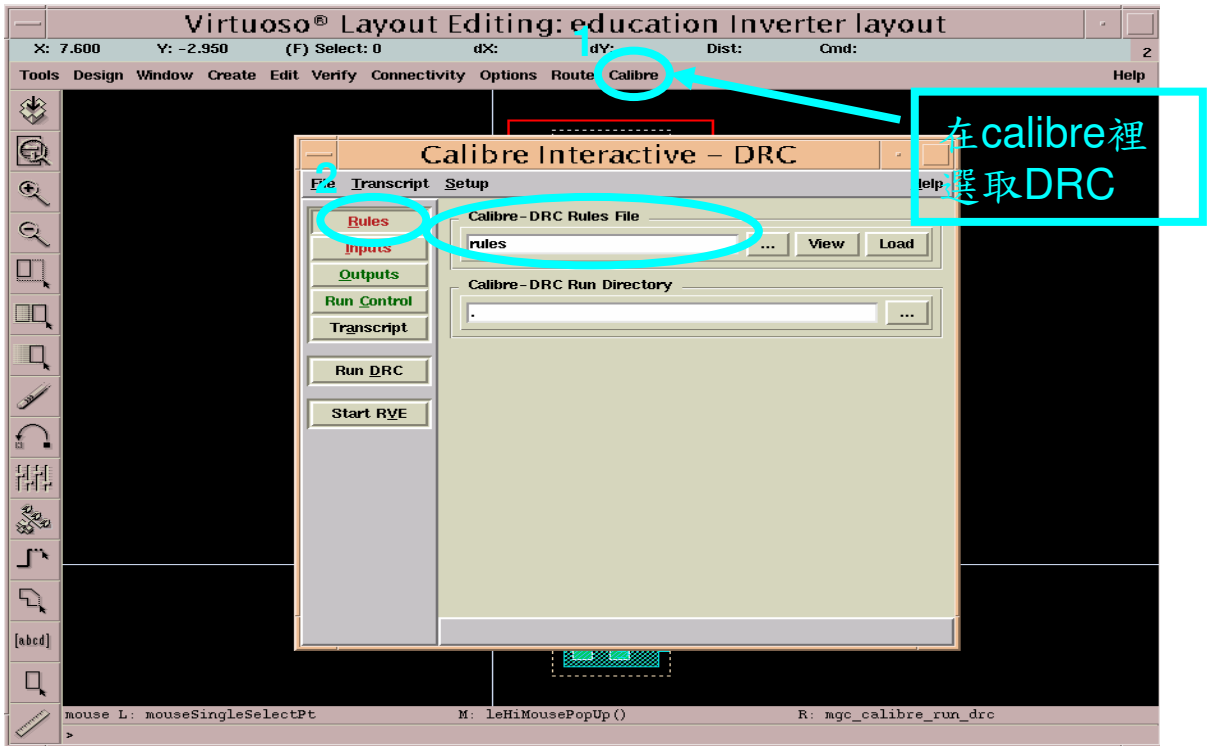
Inverter Layout (cont.)

- Inverter layout的完成圖



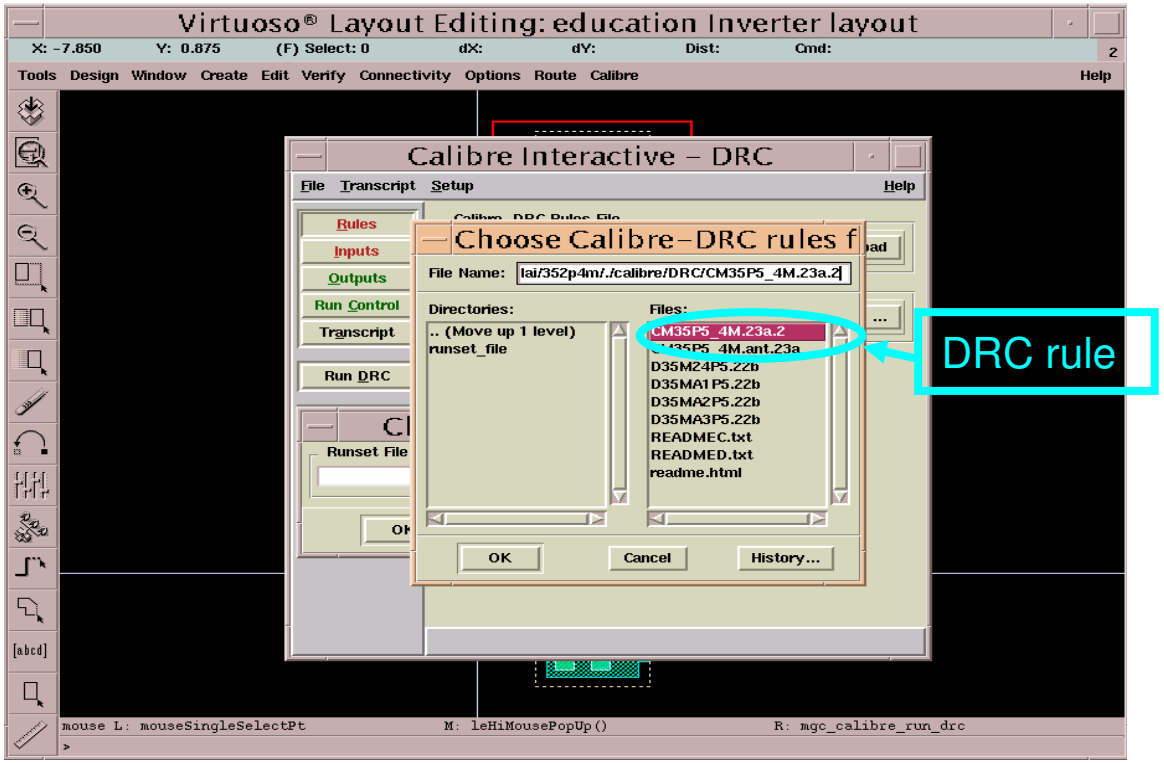
Inverter Layout (cont.)

- Calibre DRC驗證(1)



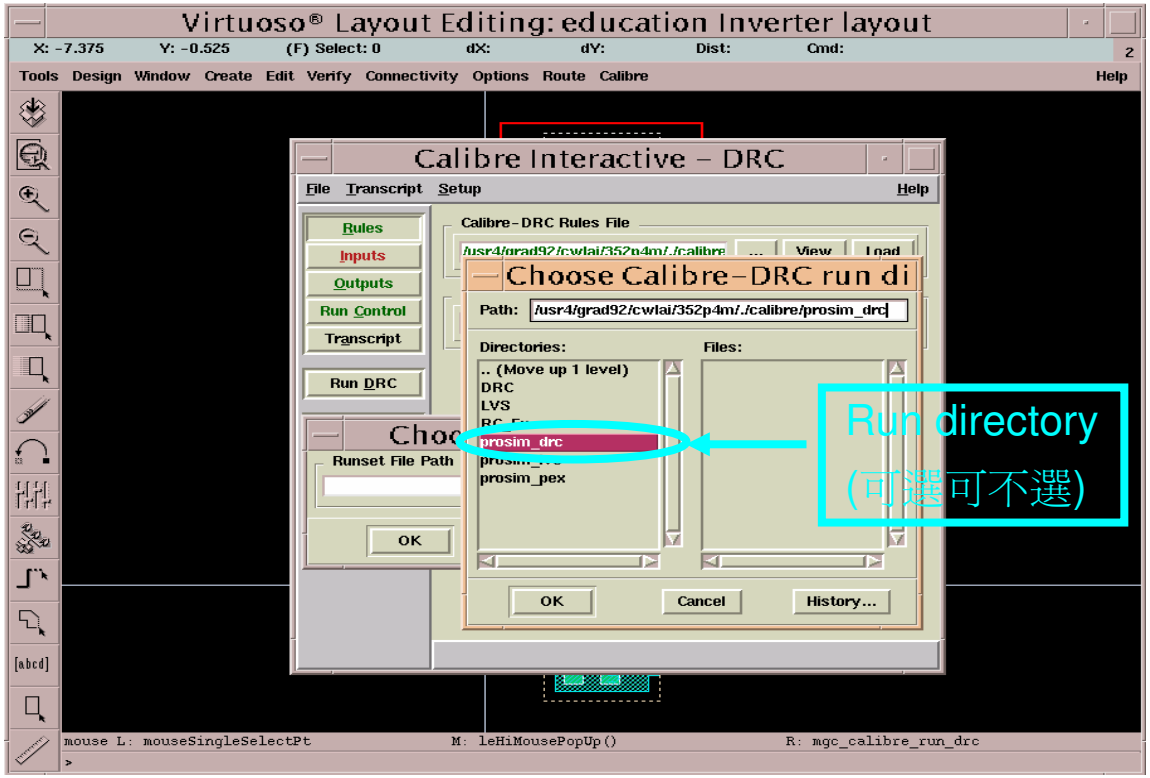
Inverter Layout (cont.)

- Calibre DRC驗證(2): CM35P5_4M.23a.2



Inverter Layout (cont.)

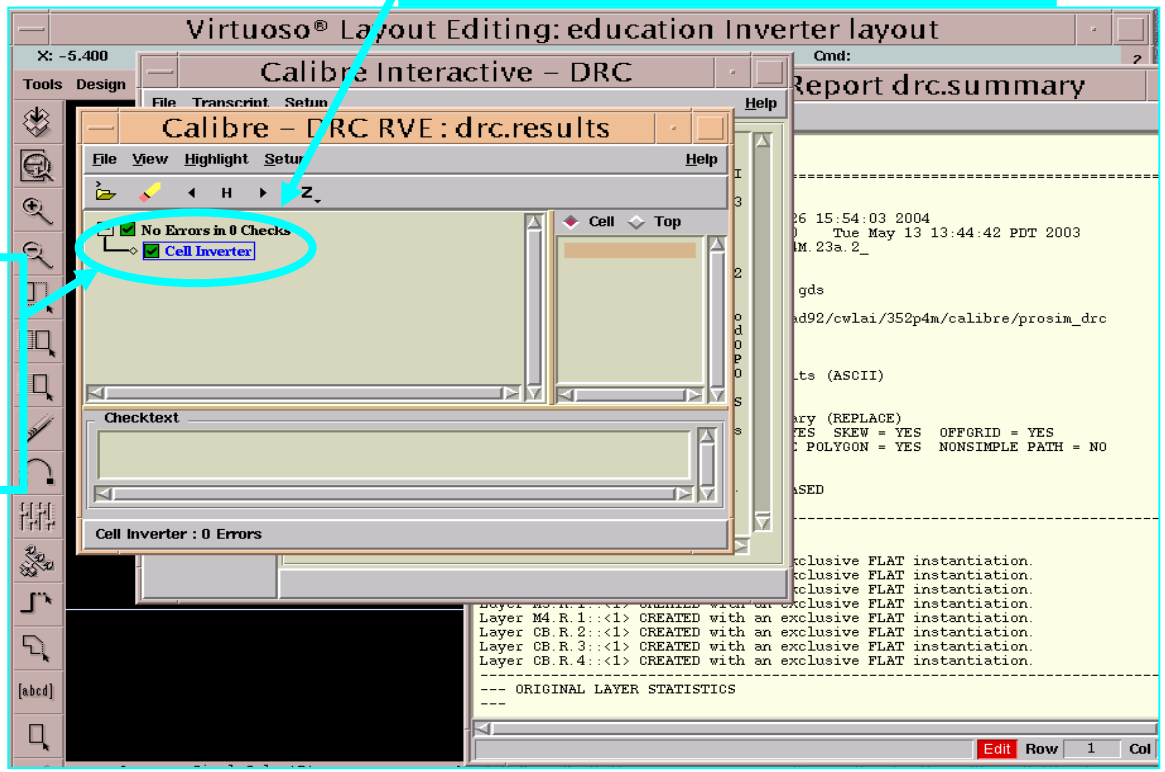
- Calibre DRC驗證(3)



Inverter Layout (cont.)

- Calibre DRC驗證(4)

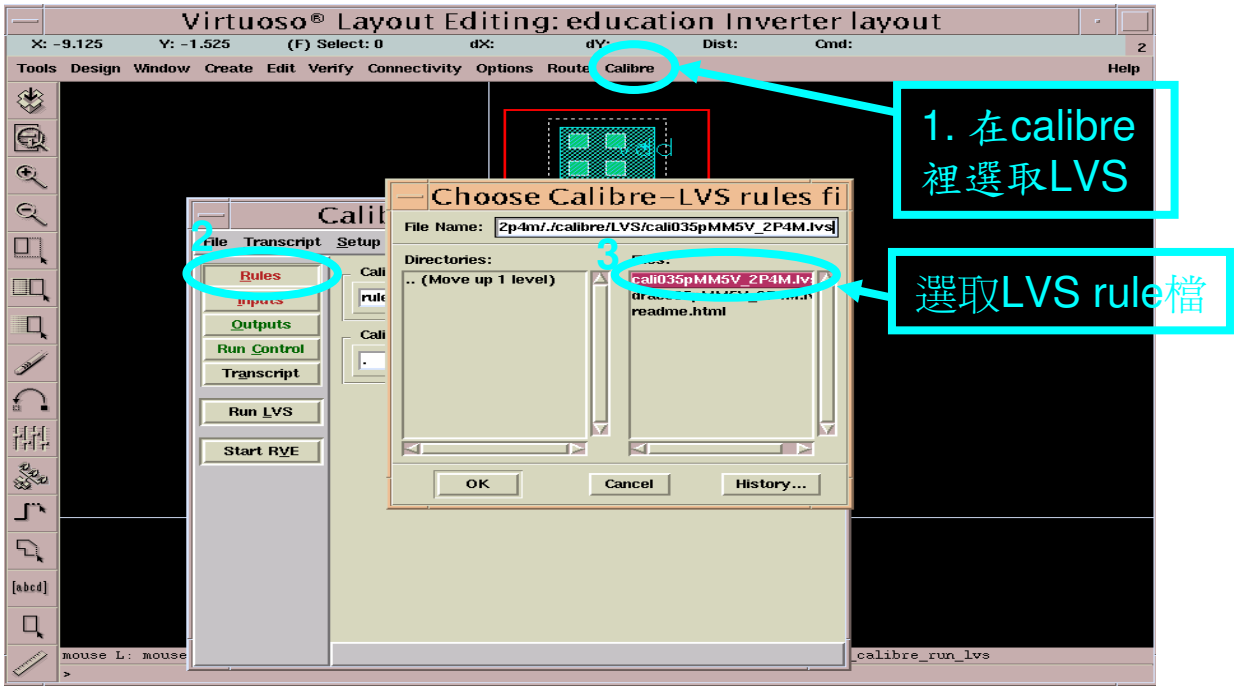
當error發生, 點選message可highlight layout之錯誤處



RVE顯示No Errors，表示電路完全符合design rule

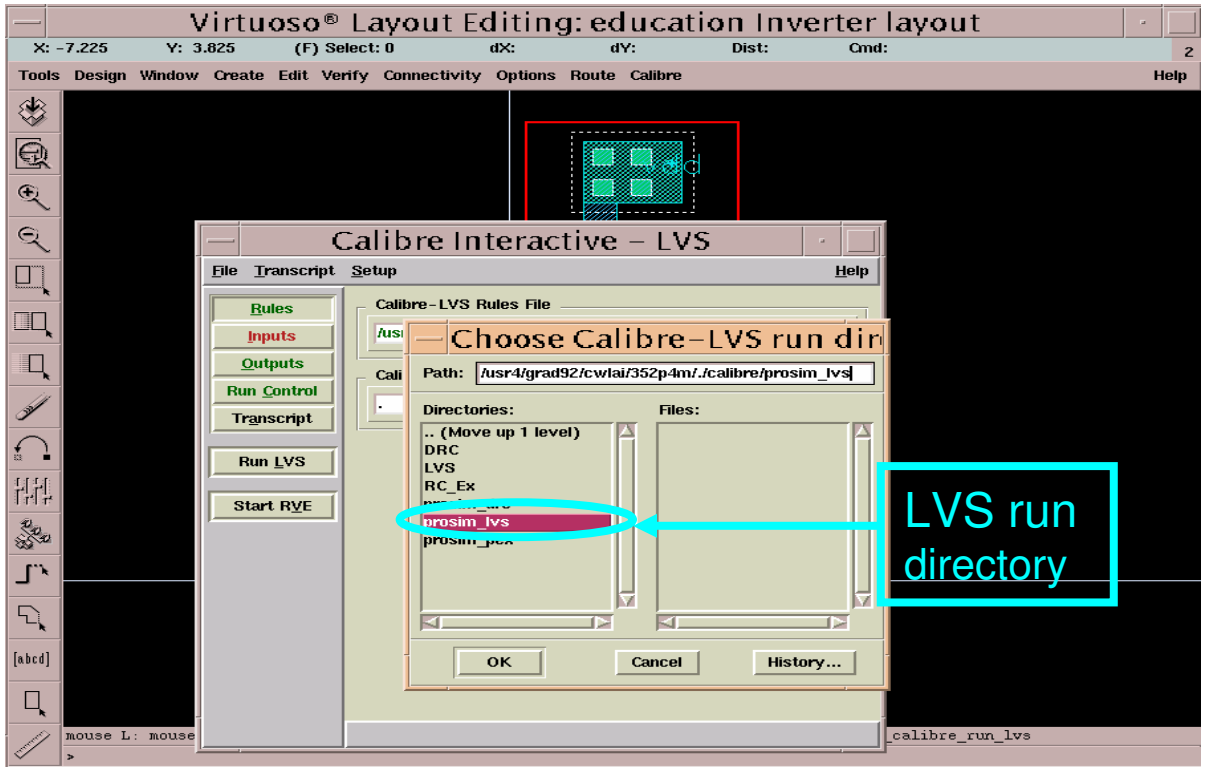
Inverter Layout (cont.)

- Calibre LVS (Layout versus schematic) 驗證(1): cali035pMM5V_2P4M.lvs



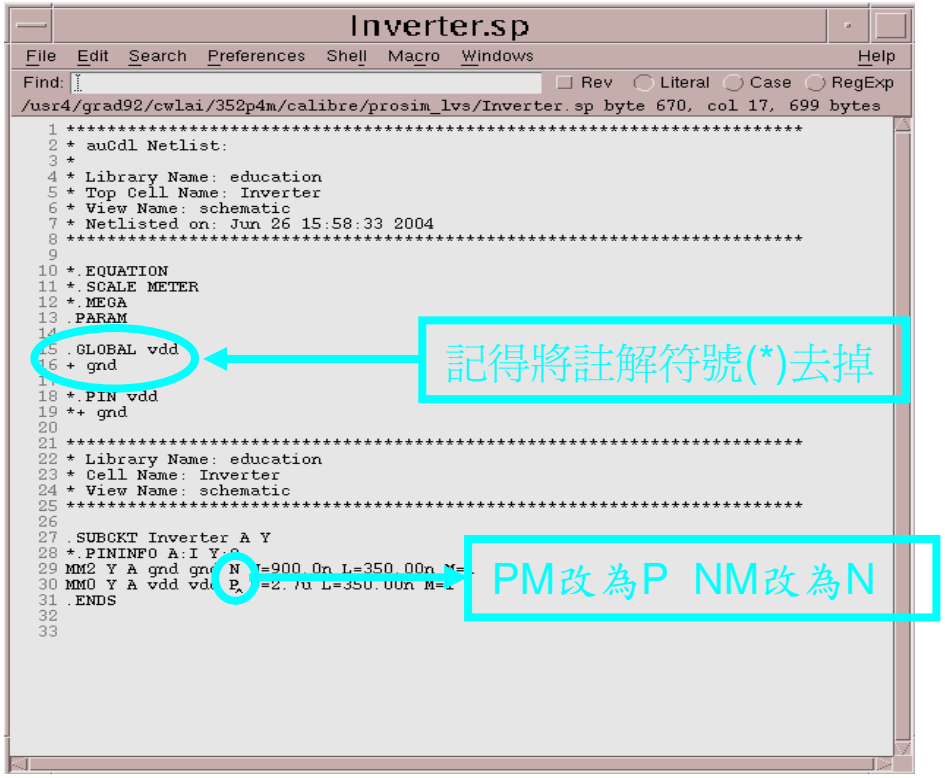
Inverter Layout (cont.)

- Calibre LVS驗證(2)



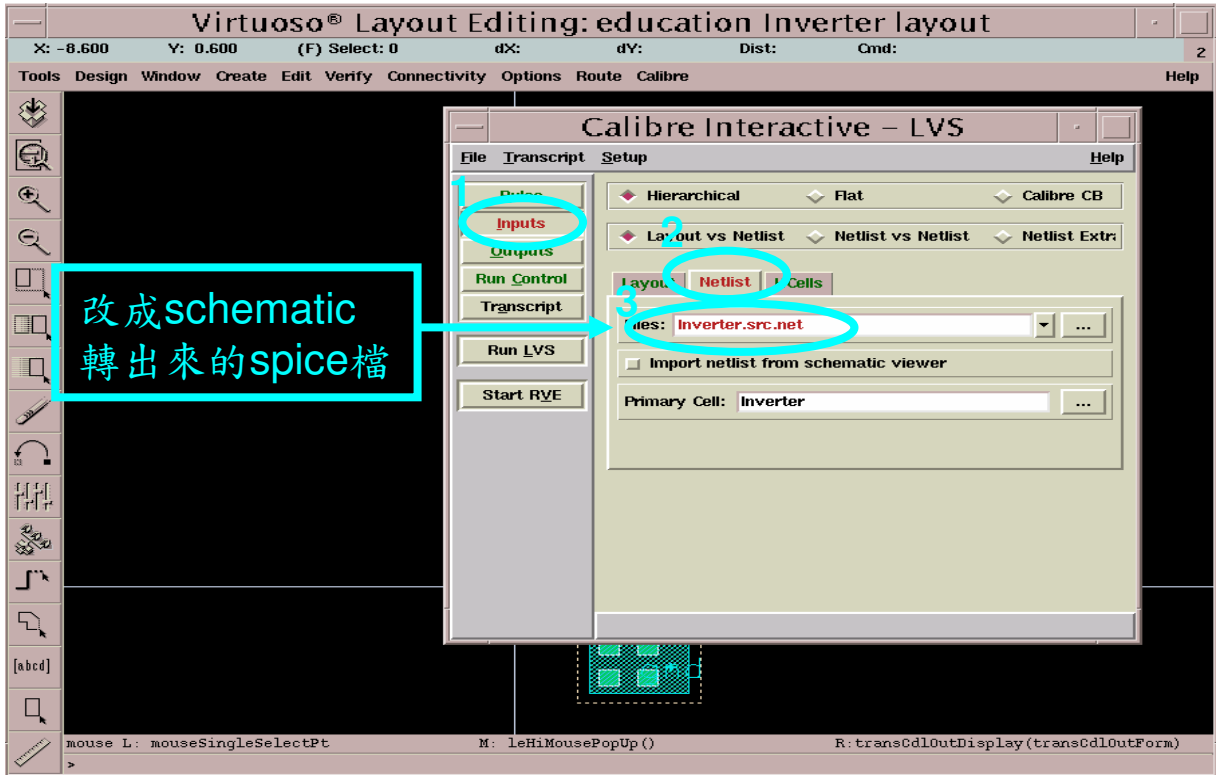
Inverter Layout (cont.)

- 用於LVS驗證的spice檔 (schematic轉出)



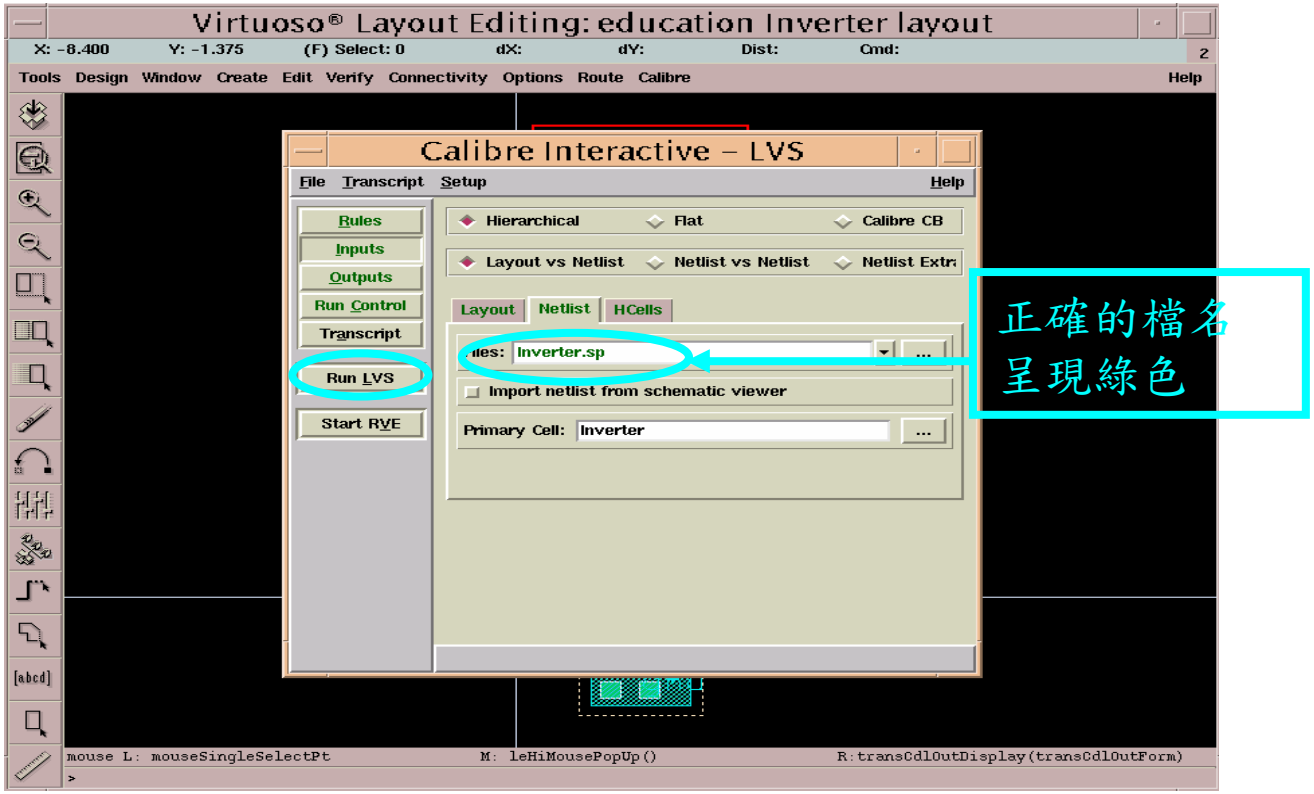
Inverter Layout (cont.)

- Calibre LVS驗證(3)



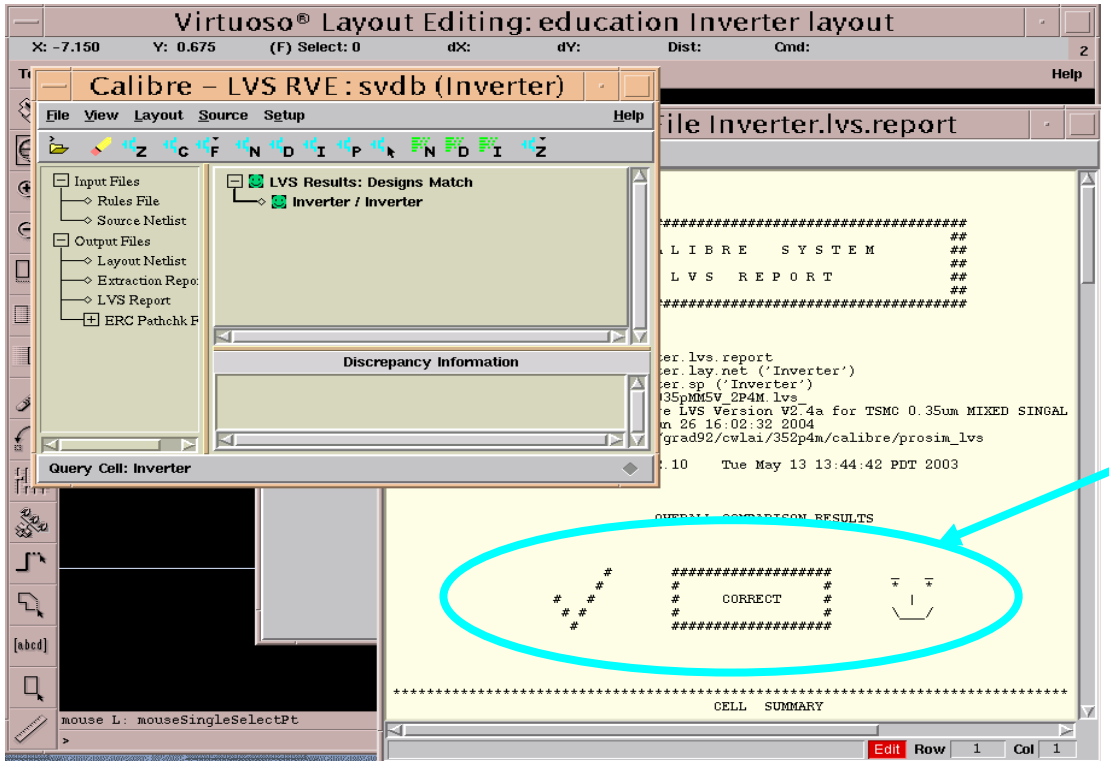
Inverter Layout (cont.)

- Calibre LVS驗證(4)



Inverter Layout (cont.)

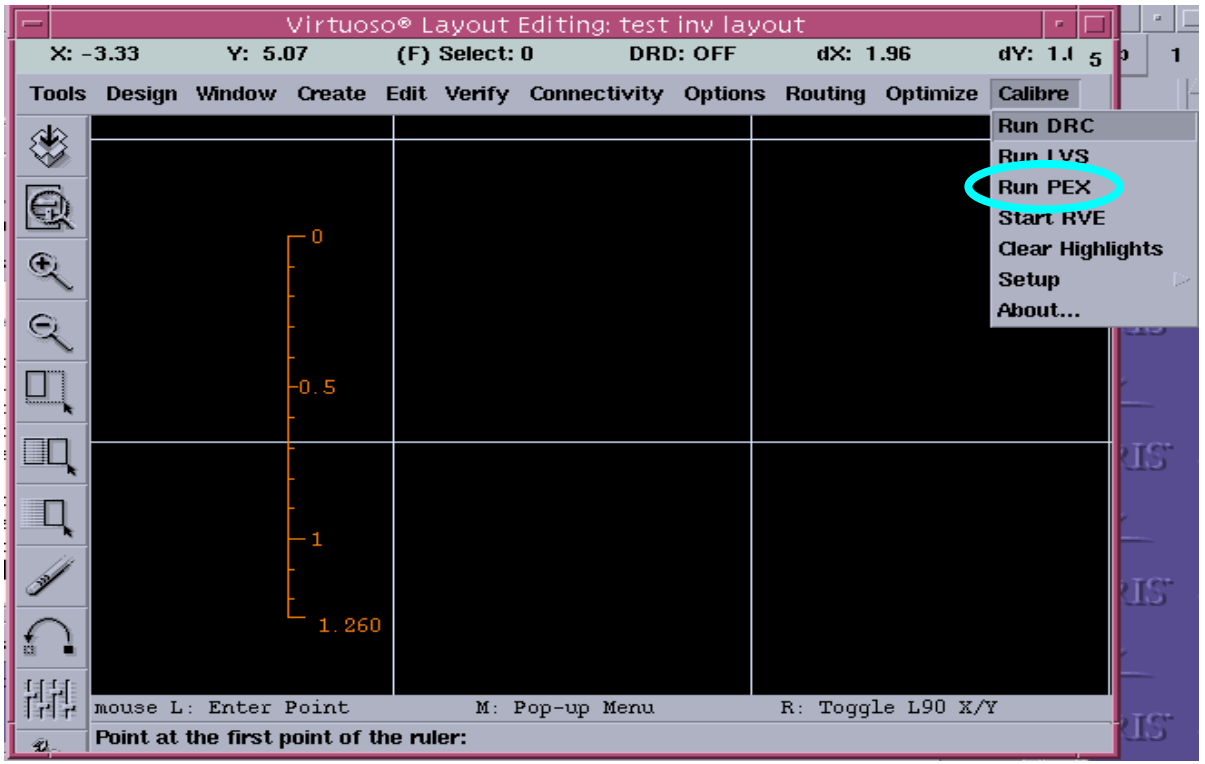
- Calibre LVS驗證(5)



LVS比對正確後所產生的正確訊息

Inverter Layout (cont.)

- Run PEX (1) : 轉出post-simulation的spice檔

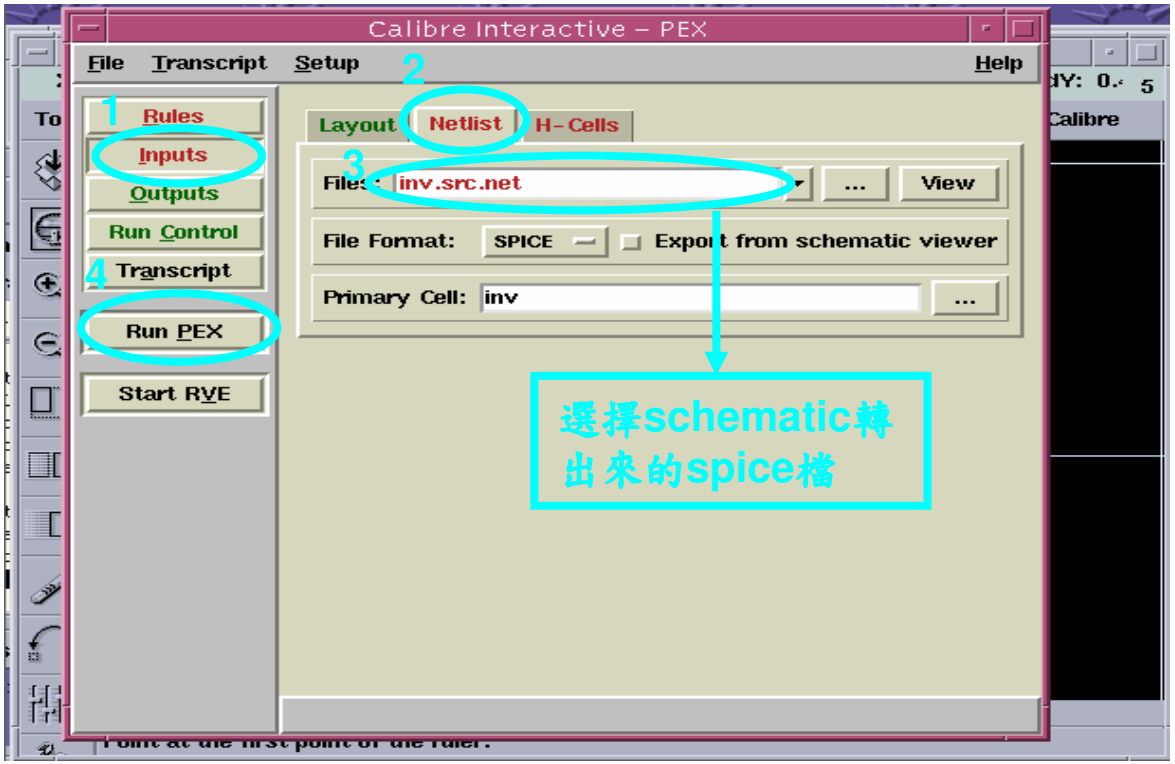


Inverter Layout (cont.)

- Run PEX (2)

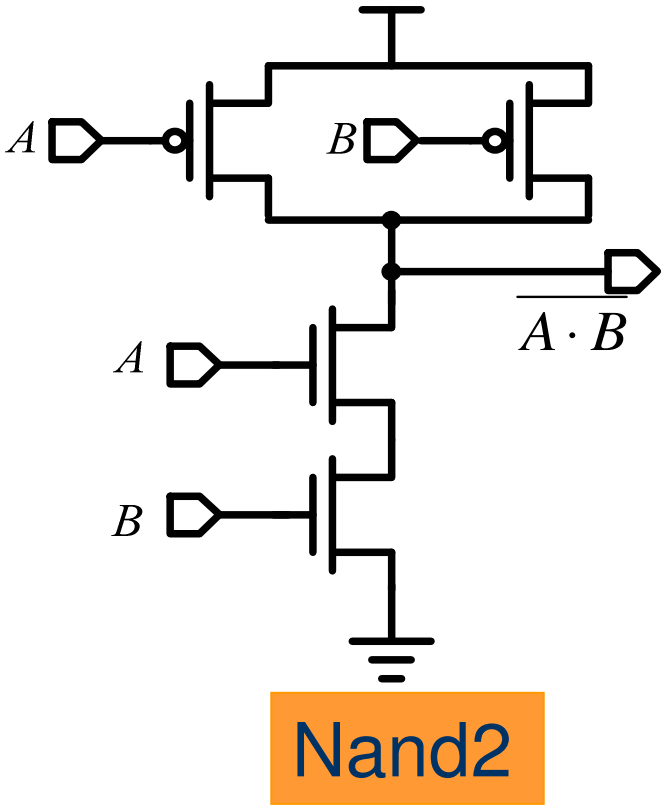
Inverter Layout (cont.)

- Run PEX (3)



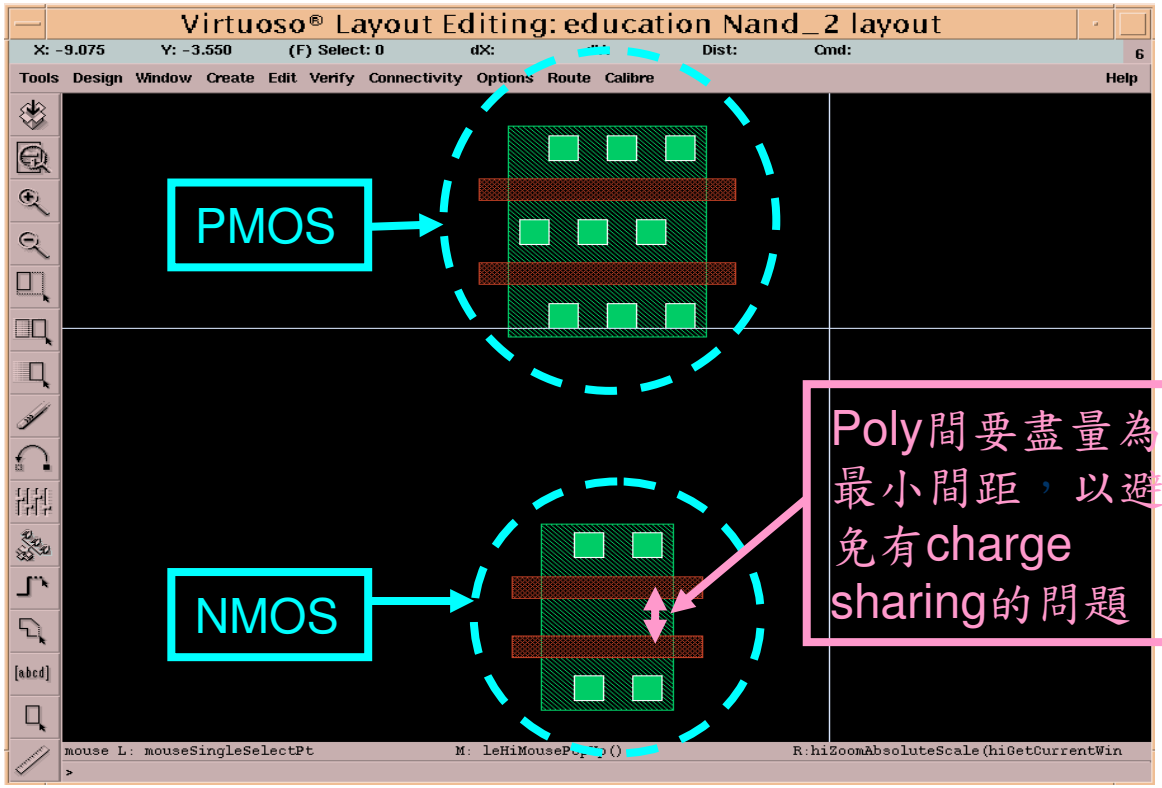
Nand2 Layout

- Practice goal:
  - Learn layout technologies
  - Accomplish a nand2 logic circuit layout
- Content:
  - Layout Editor
    - Instance cell
  - Nand2 Layout implement



Nand2 Layout (1/8)

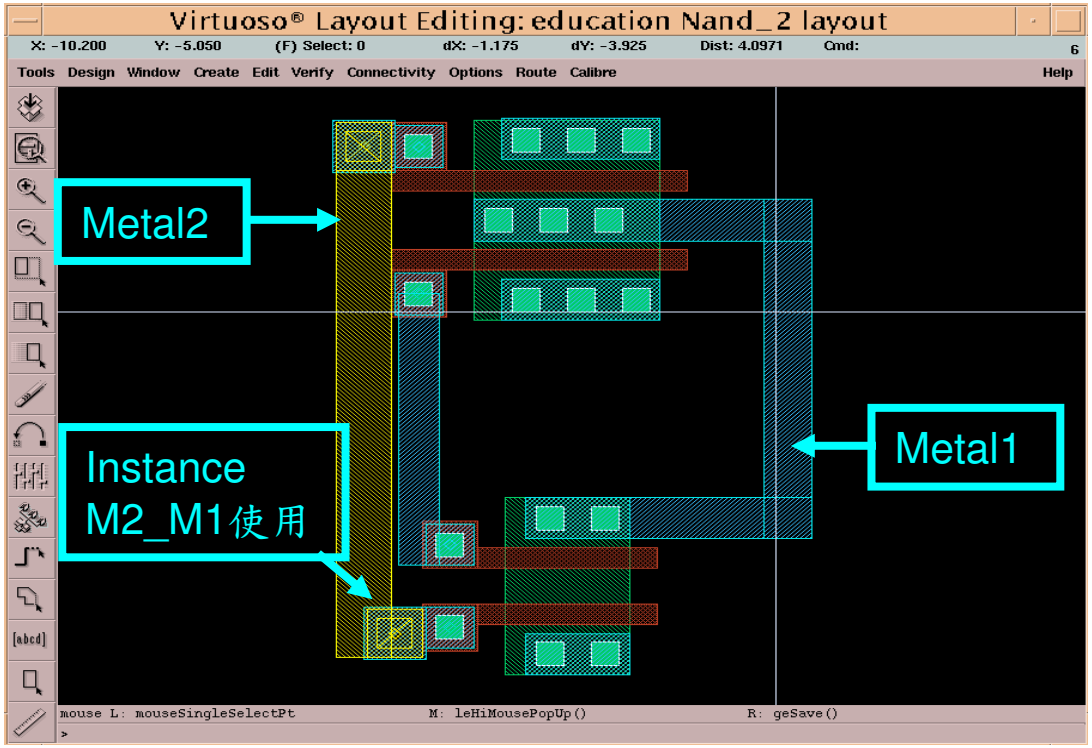
- 先畫出 PMOS and NMOS



Nand2 Layout (2/8)

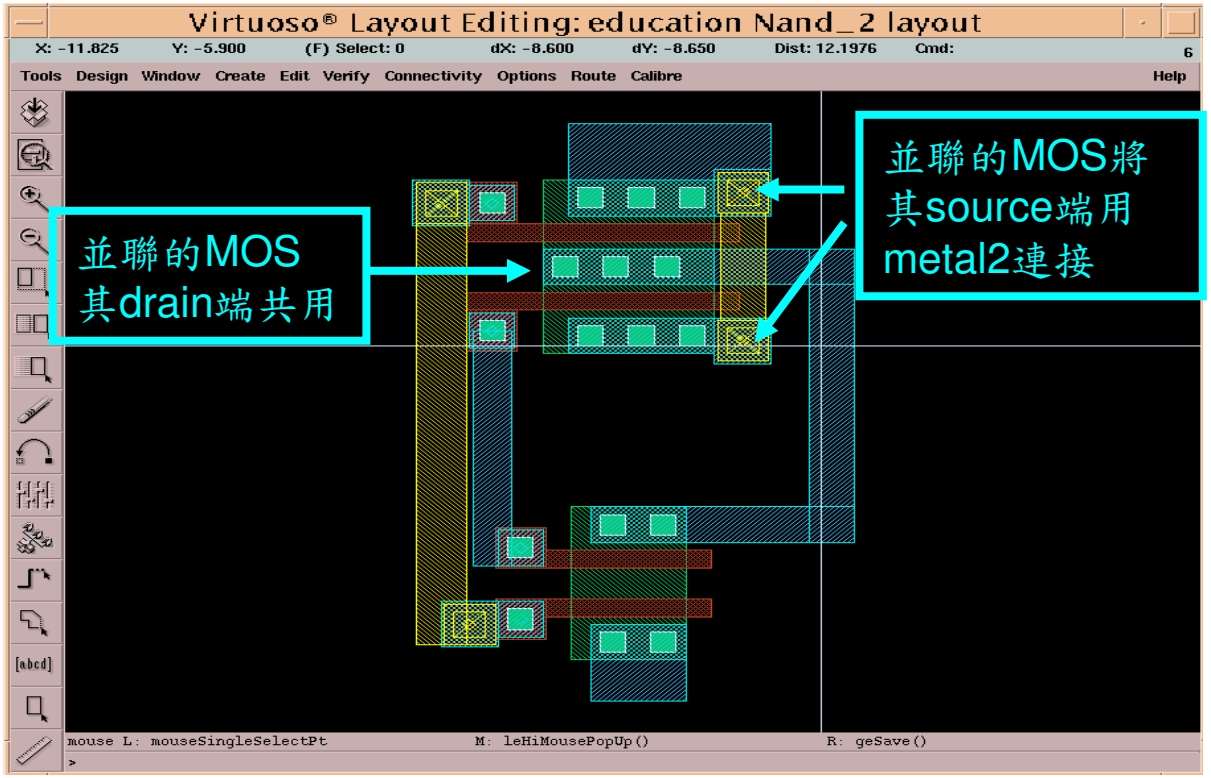
- 將MOS的gate端相連接

■在兩個MOS的gate端相距太遠時，利用metal來做連接可減少寄生的電阻值，避免使用poly做連接!!!



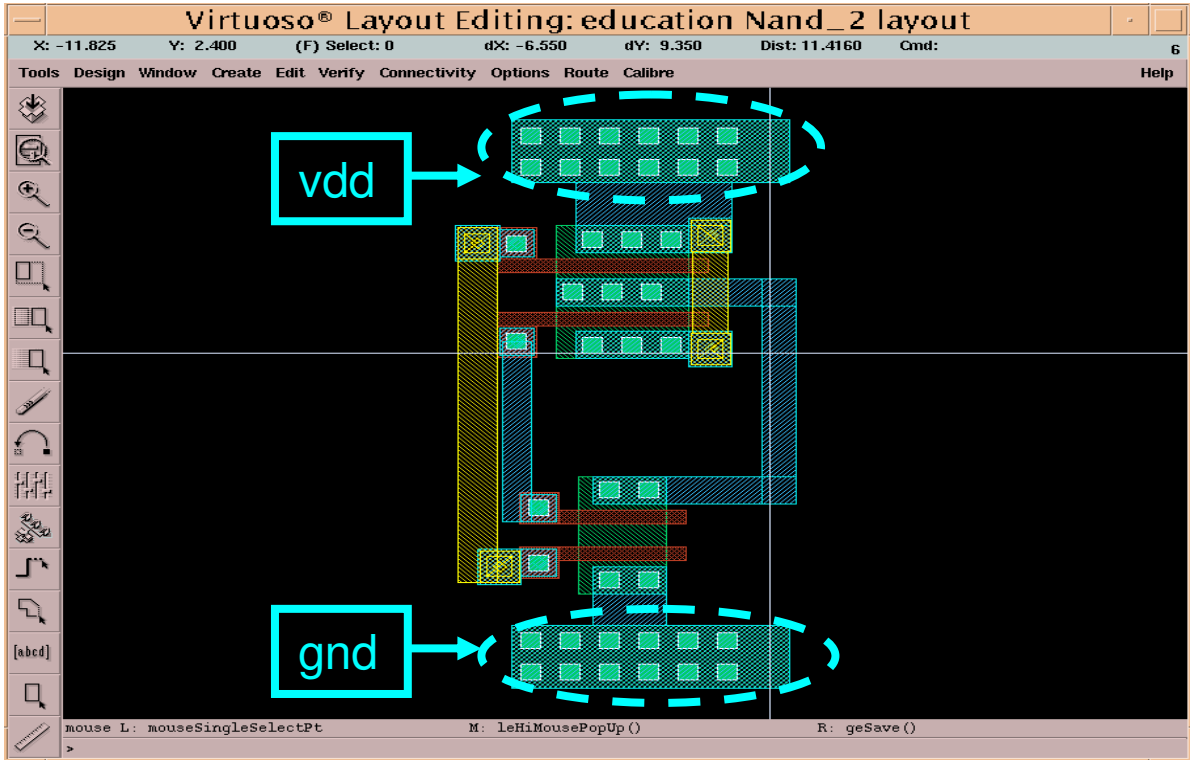
Nand2 Layout (3/8)

- 將並聯的MOS相連接（學習並聯的技巧）



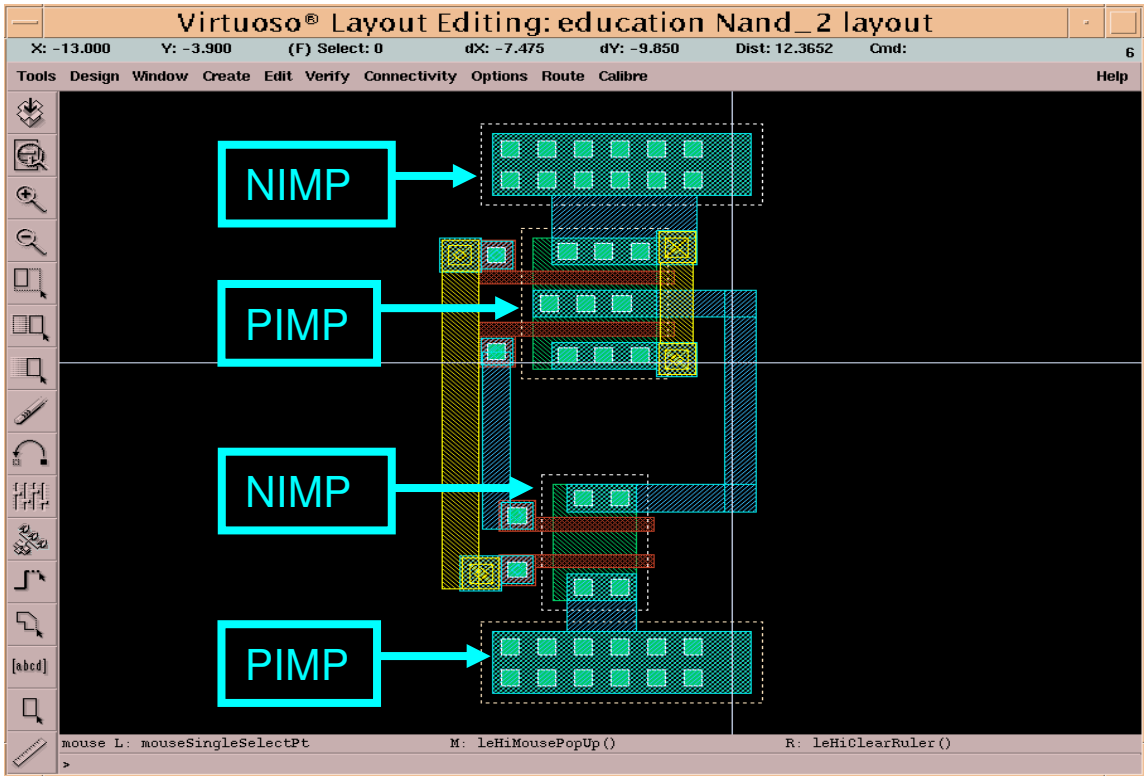
Nand2 Layout (4/8)

- 在MOS的source端分別加上vdd和gnd的DIFF層



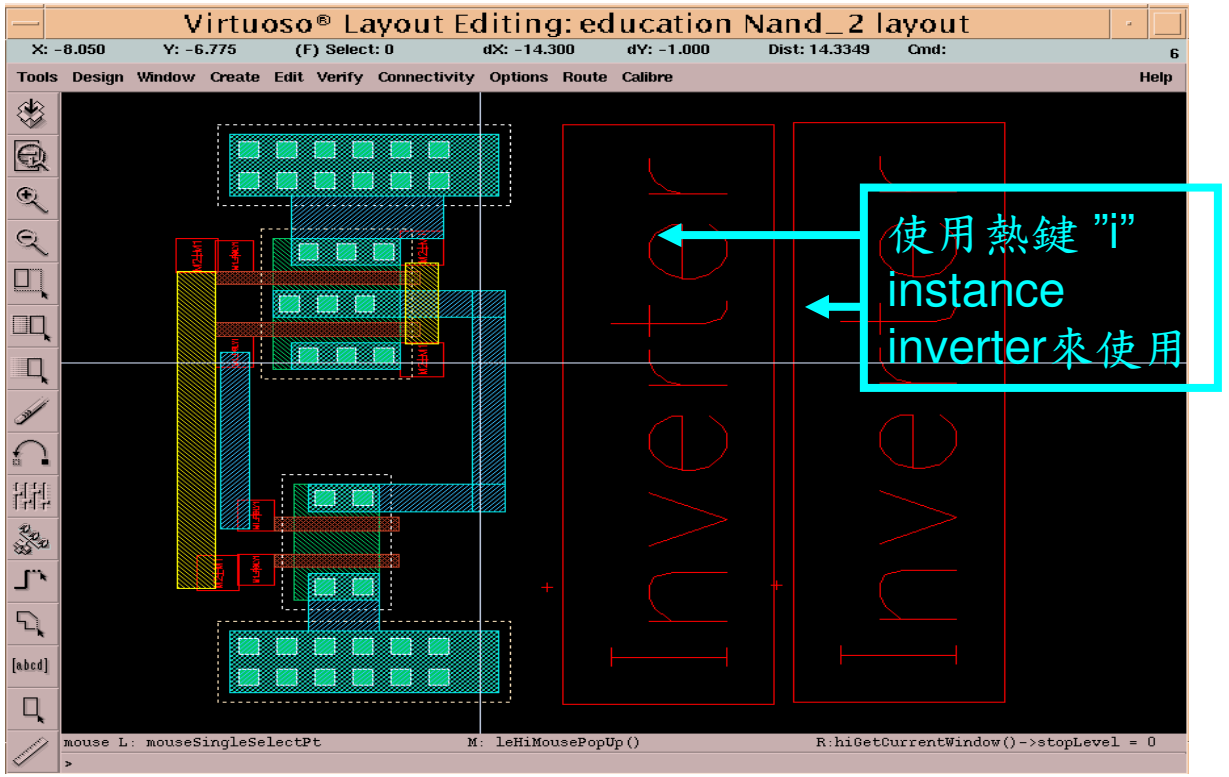
Nand2 Layout (5/8)

- 加上PIMP、NIMP層



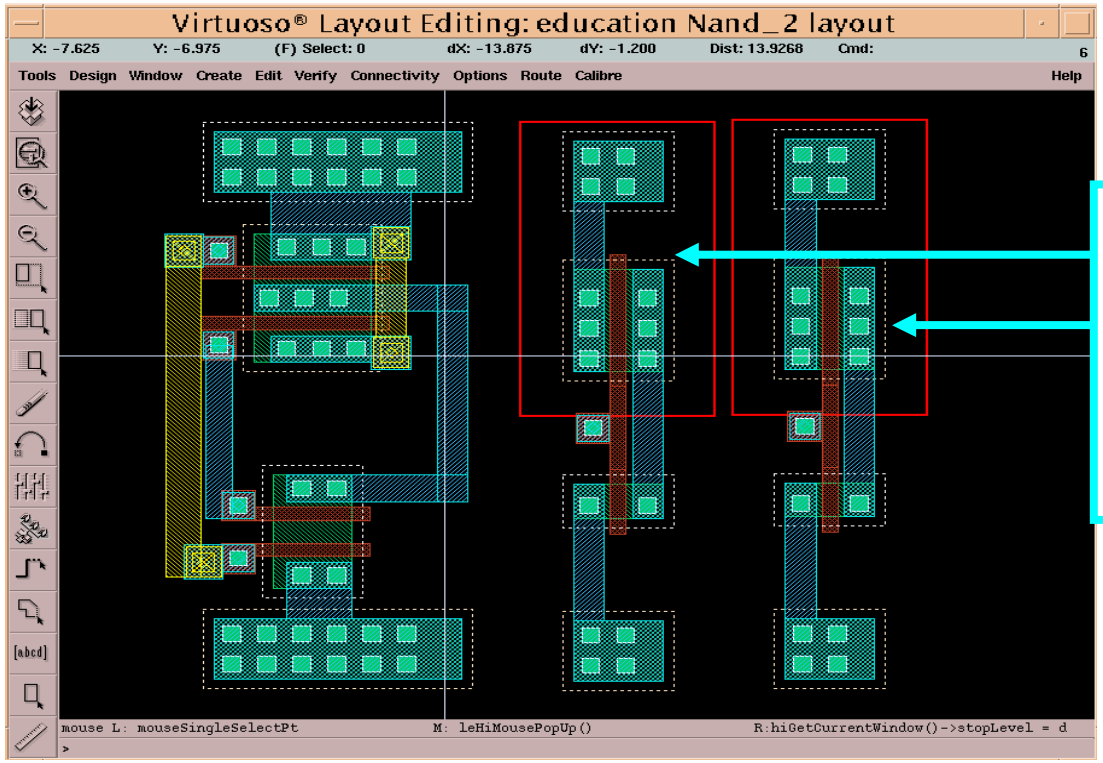
Nand2 Layout (6/8)

- Instance已畫好的layout使用



Nand2 Layout (7/8)

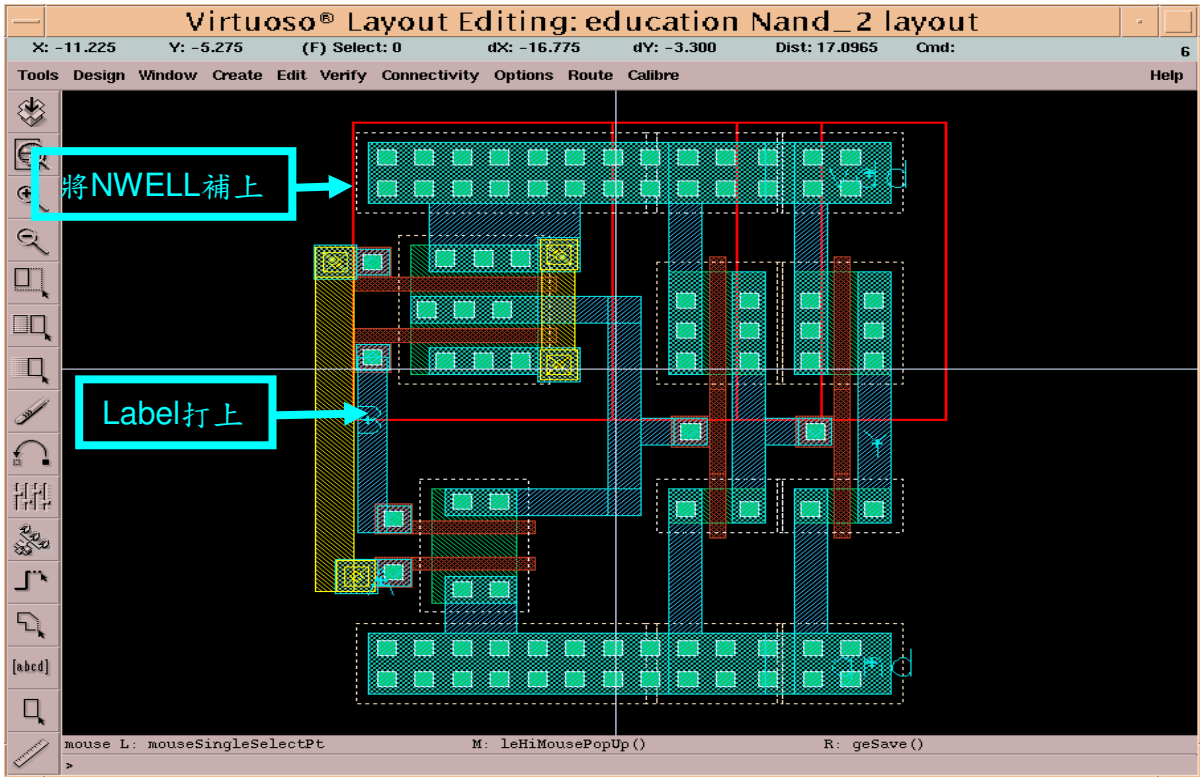
- 利用Ctrl+f、Shift+f來切換symbol的圖示



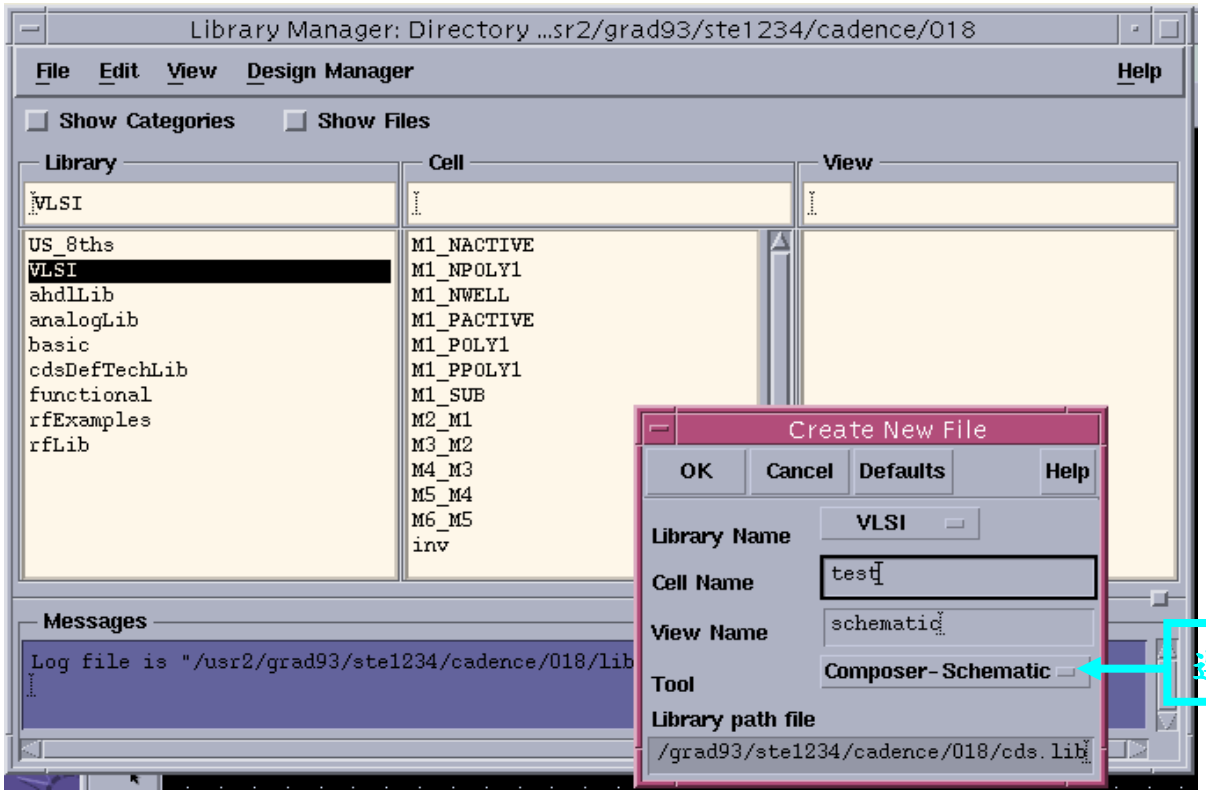
按 Shift+f 後，可以看到instance進來的layout；再按一次 Ctrl+f 就可恢復symbol的圖示，如上頁所示

Nand2 Layout (8/8)

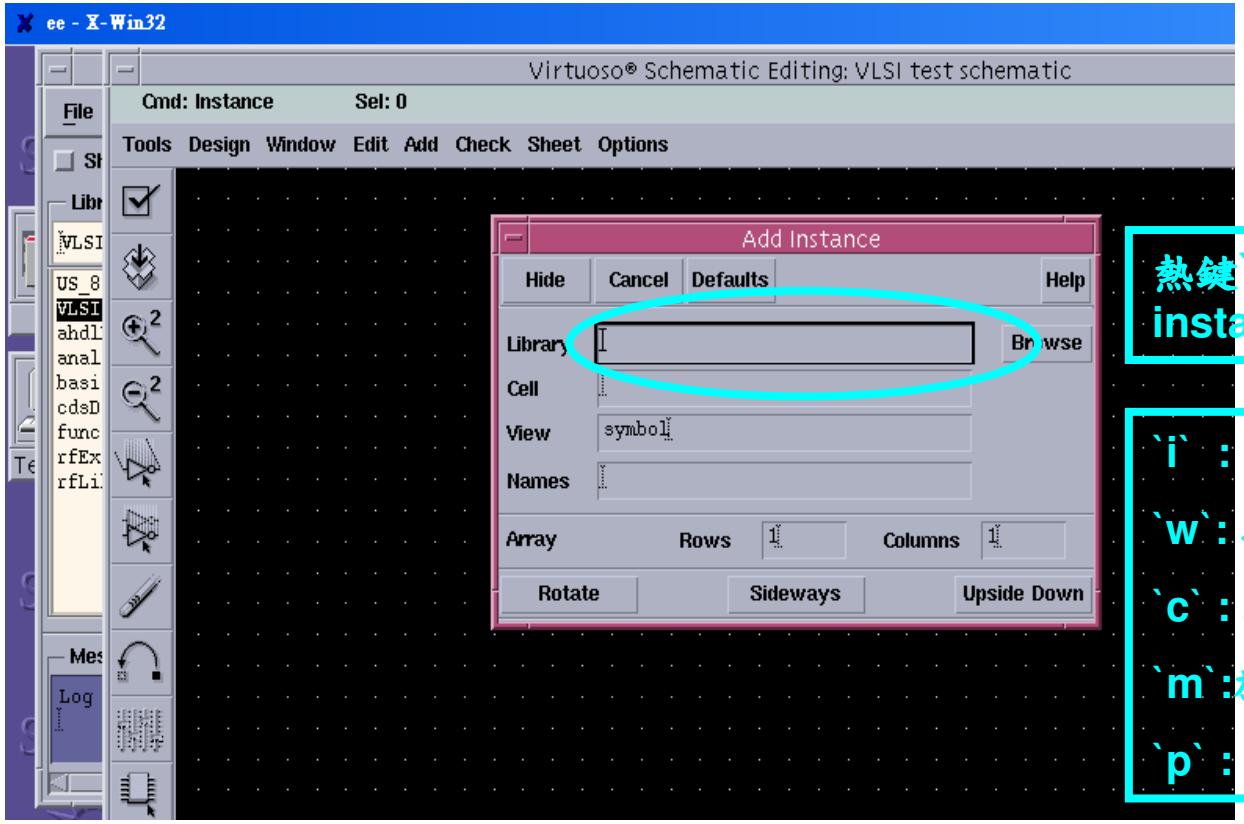
- 將個別電路的vdd、gnd相連接



Schematic


Library Manager: Directory ...sr2/grad93/ste1234/cadence/018
File Edit View Design Manager Help
Show Categories
Show Files
Library
Cell
View
VLSI
US_8ths
VLSI
ahdlLib
analogLib
basic
cdsDefTechLib
functional
rfExamples
rfLib
M1_NACTIVE
M1_NPOLY1
M1_NWELL
M1_PACTIVE
M1_POLY1
M1_PPOLY1
M1_SUB
M2_M1
M3_M2
M4_M3
M5_M4
M6_M5
inv
Messages
Log file is "/usr2/grad93/ste1234/cadence/018/lib
Create New File
OK
Cancel
Defaults
Help
Library Name
VLSI
Cell Name
test
View Name
schematic
Tool
Composer-Schematic
Library path file
/grad93/ste1234/cadence/018/cds.lib
選擇schematic

Schematic (cont.)



熱鍵`i` 呼叫 instance

`i` : 呼叫instance

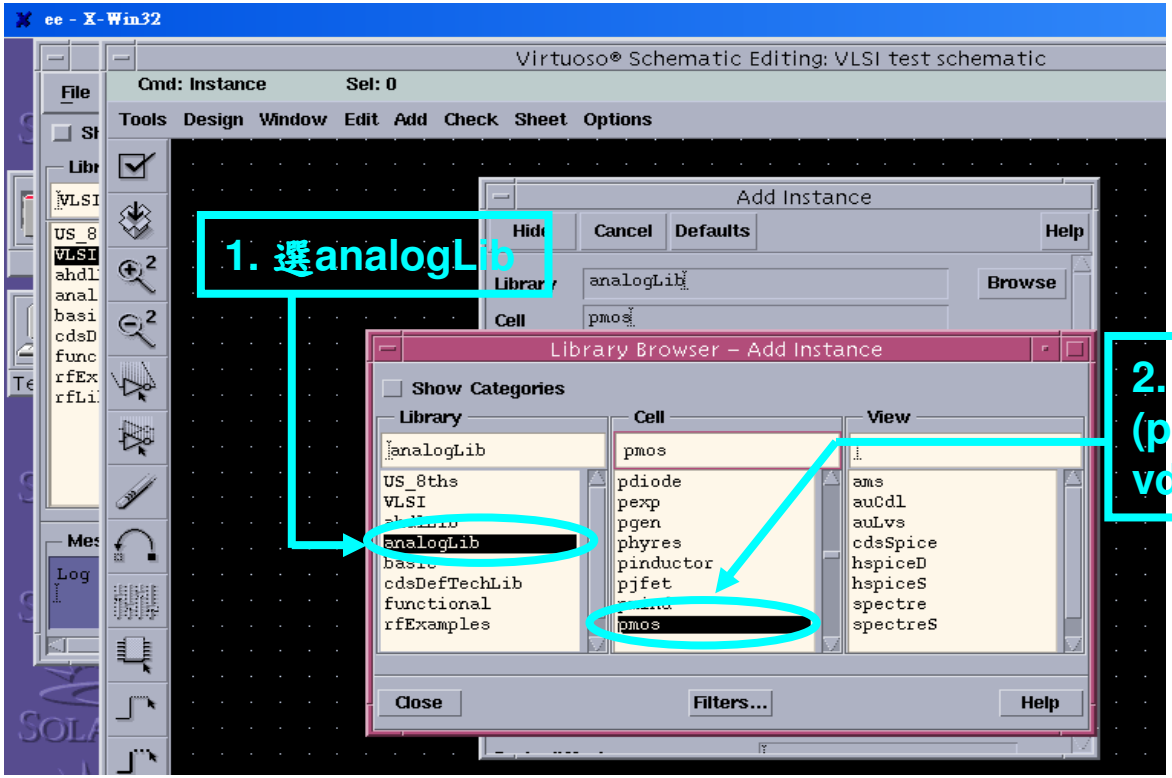
`w`: 接線

`c` : 複製物件

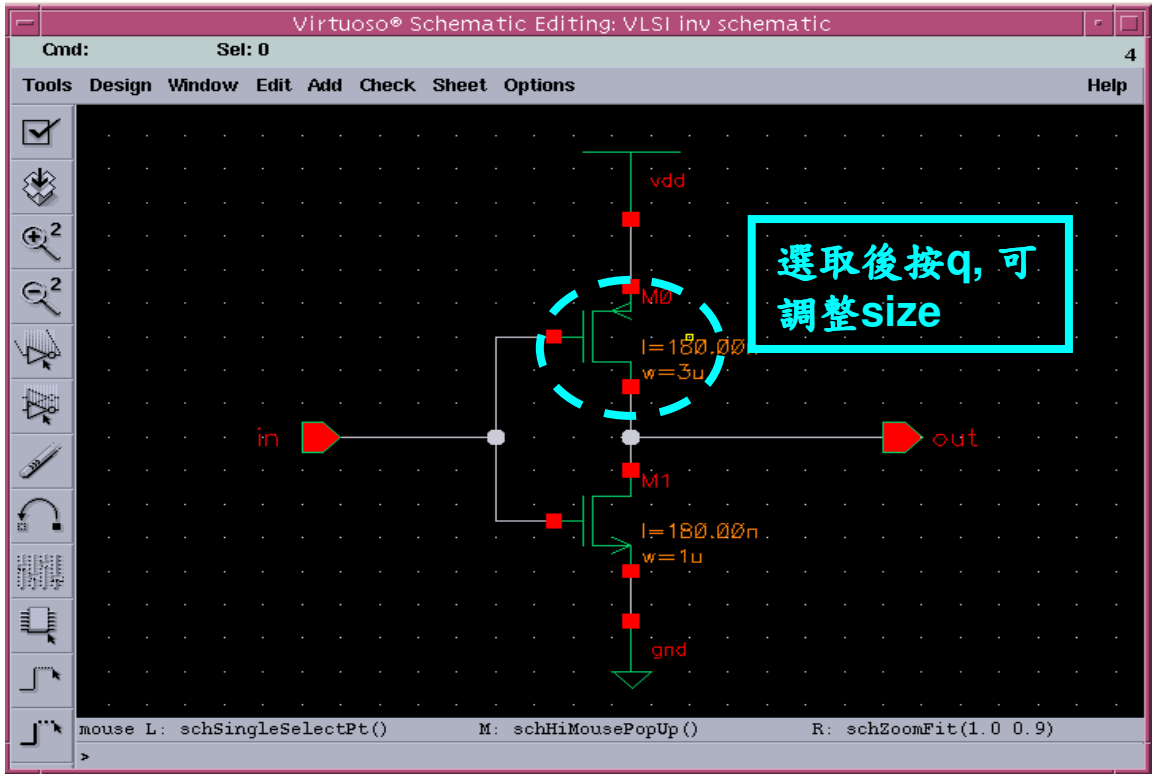
`m`:旋轉物件

`p` : 建立pin腳

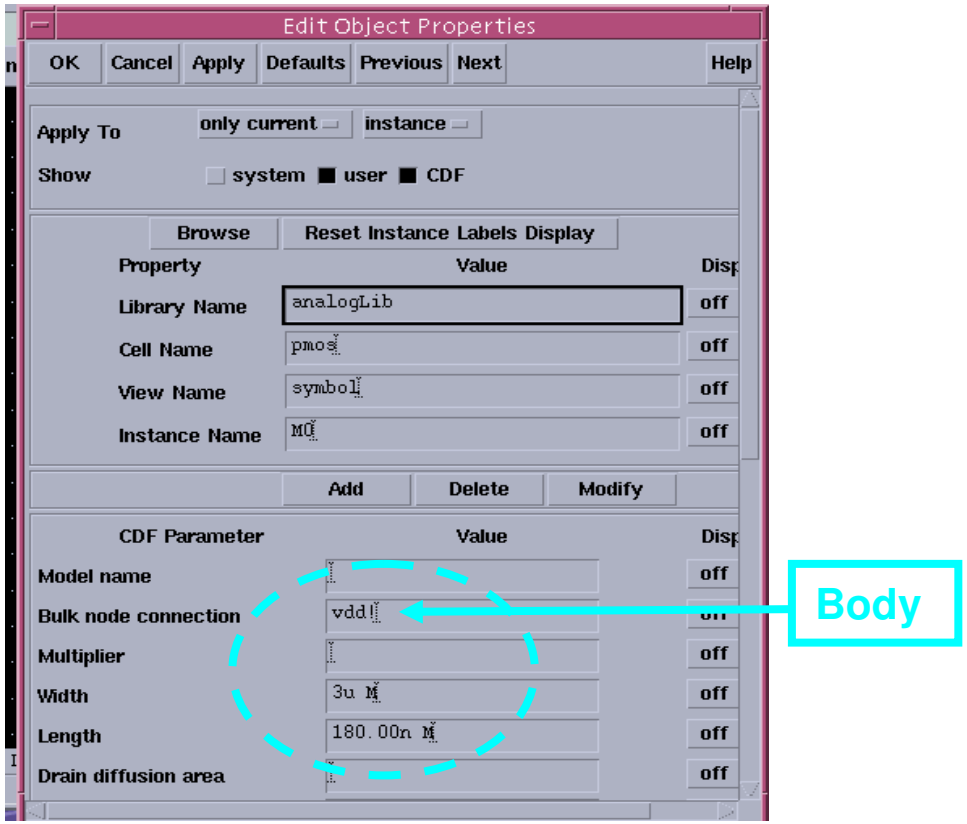
Schematic (cont.)



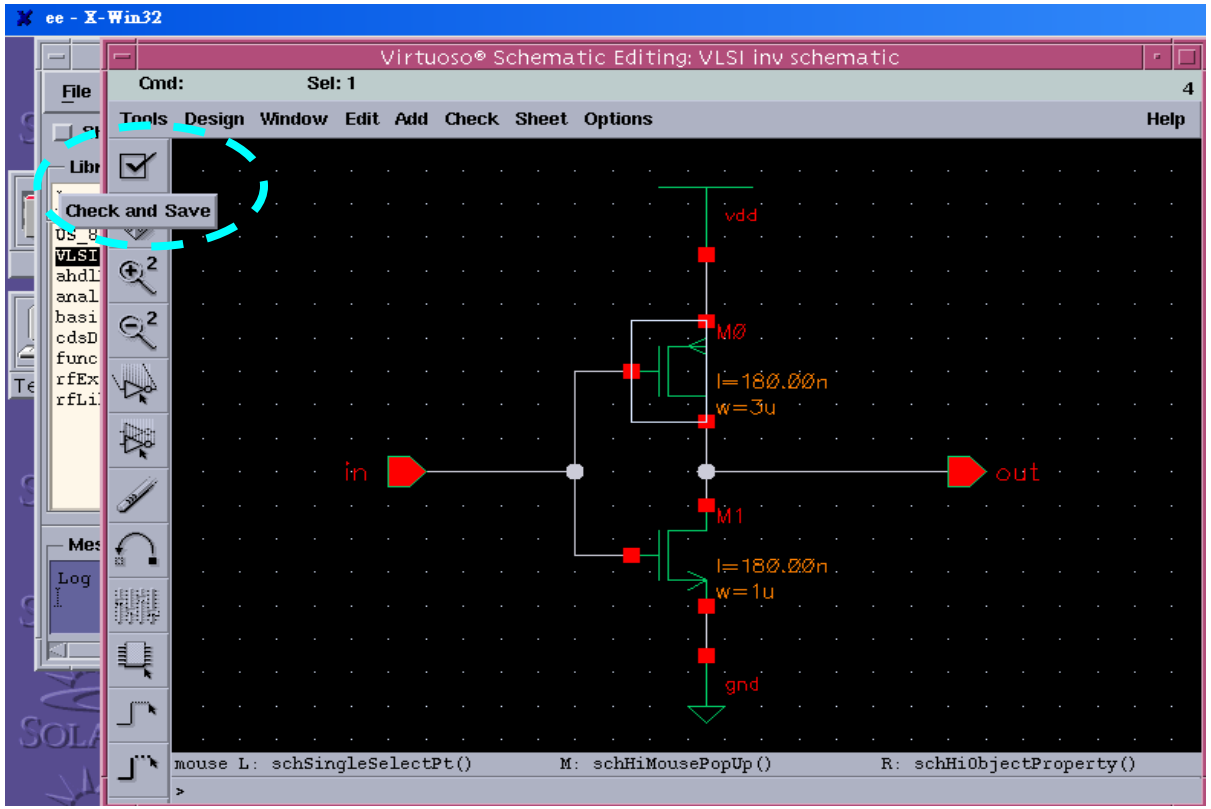
Schematic (cont.)



Schematic (cont.)

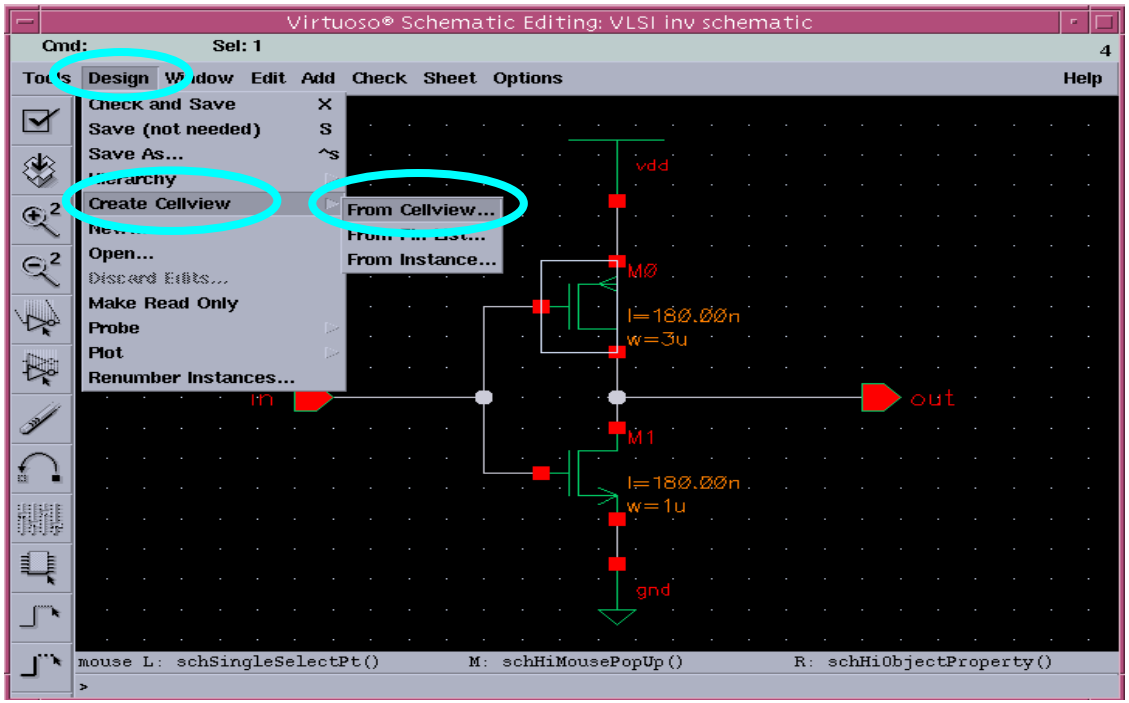


Schematic (cont.)



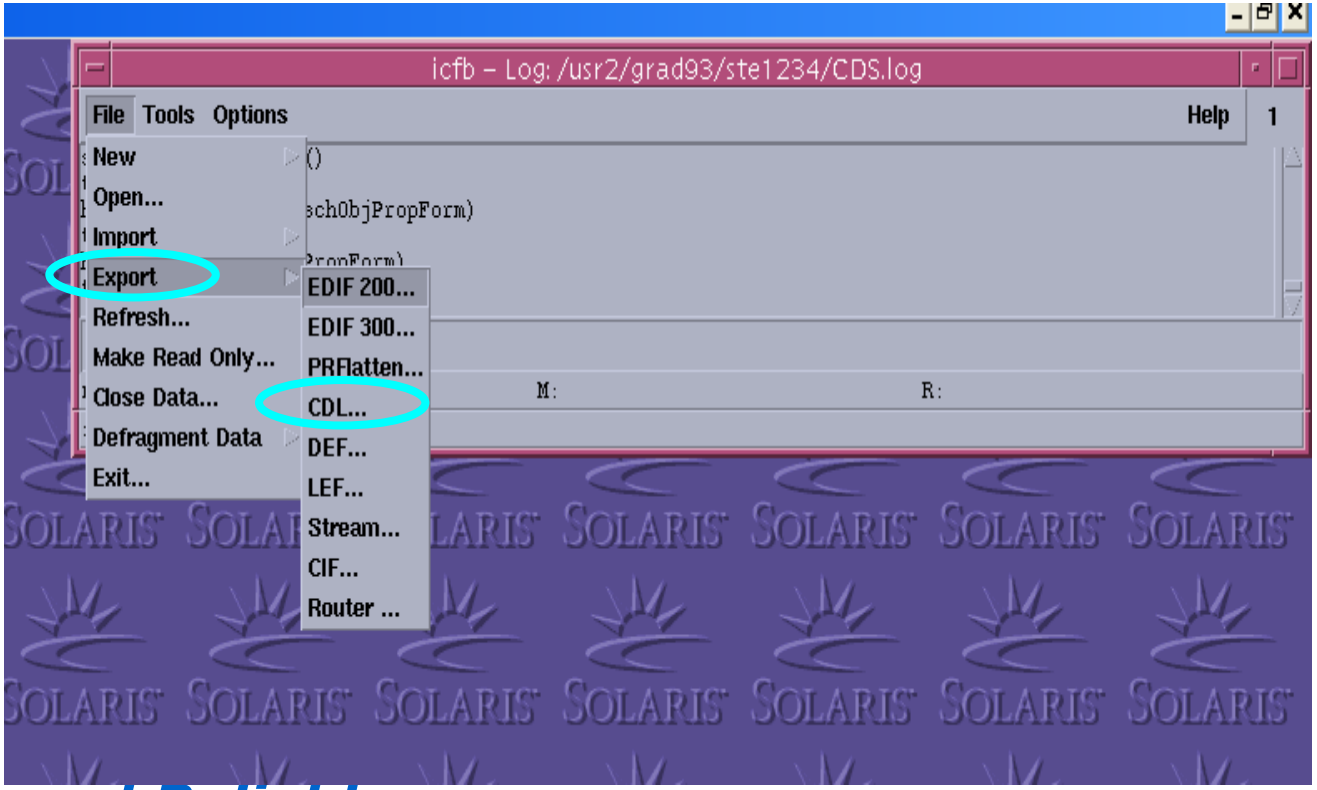
Schematic (cont.)

- 將已完成的cell存成cell_view, 供日後呼叫



Schematic (cont.)

- 將schematic轉出spice檔



Schematic (cont.)