EE3230 Lecture 3: MOS Transistor Theory

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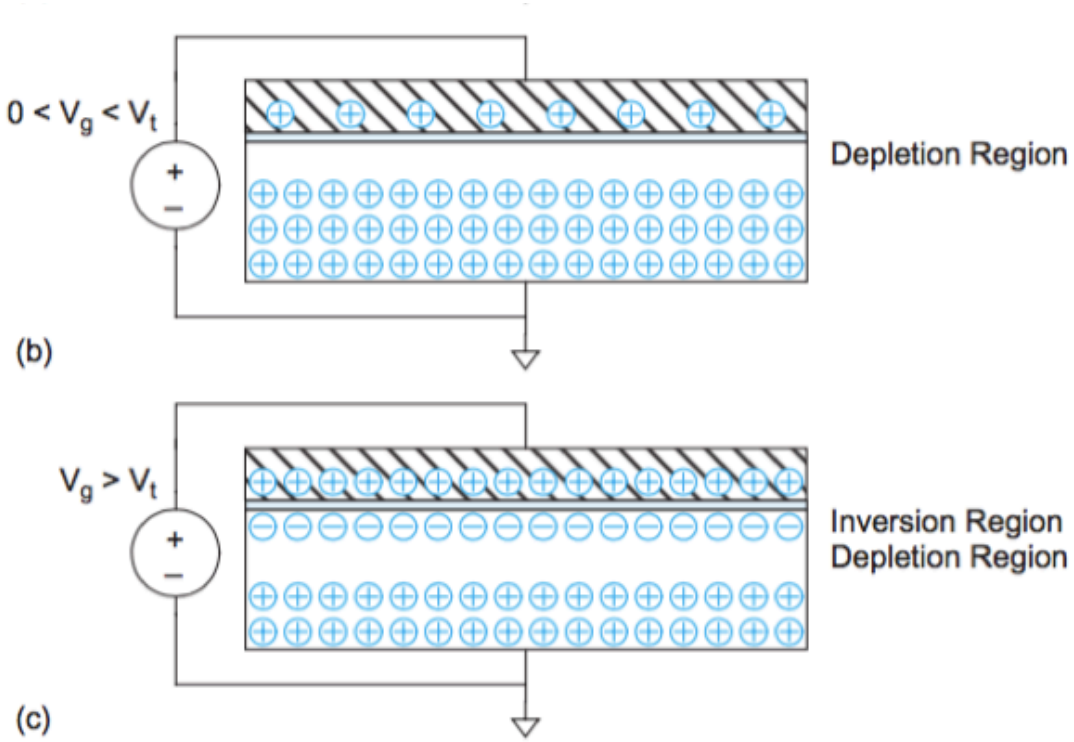
Outline

- **Introduction**
- Ideal I-V characteristics
- Nonideal Effects
- C-V characteristics
- DC transfer characteristics
- Switch-level RC delay models

MOS Transistor Symbols

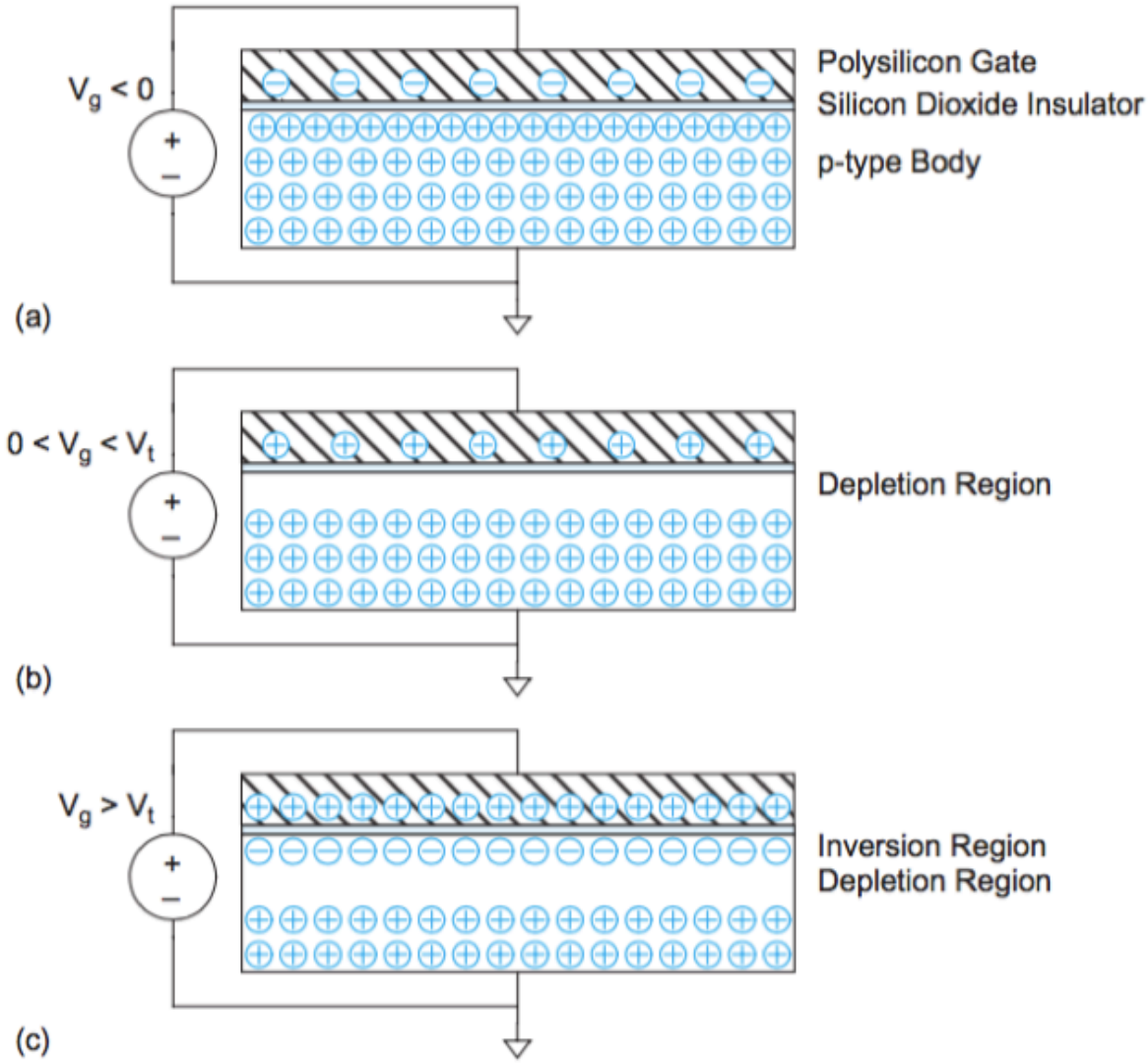
MOS Structure

- Depletion mode
- Inversion mode



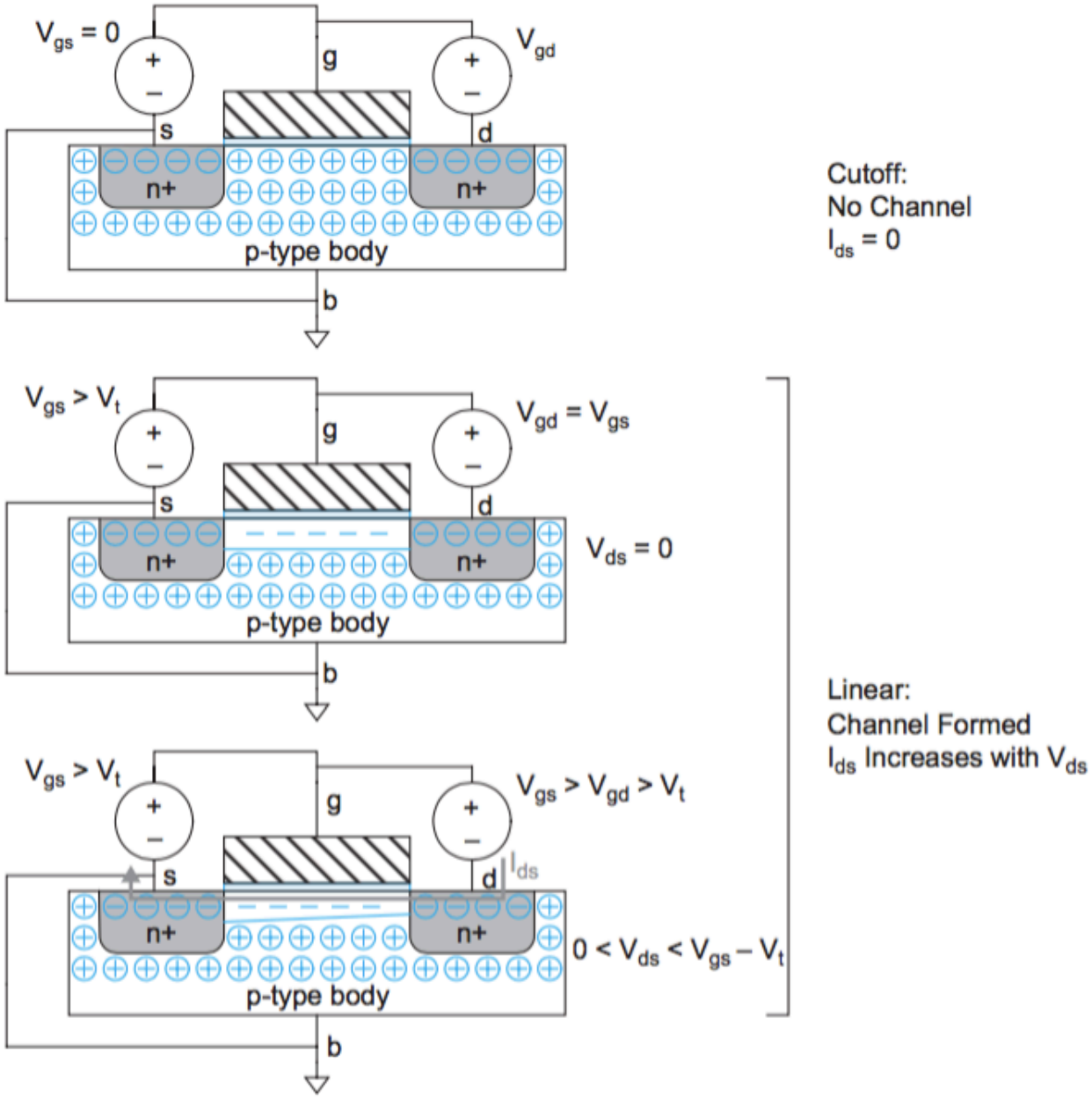
MOS Structure

- Accumulation mode
- Depletion mode
- Inversion mode



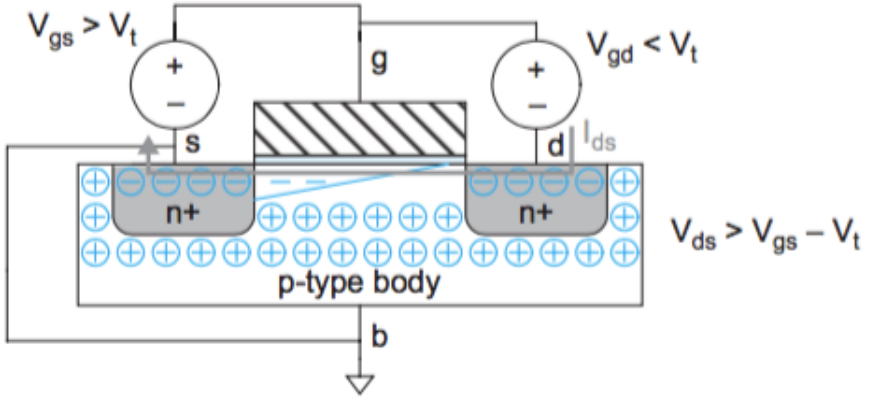
NMOS Operating Regions (I, II)

- Cutoff
- Linear



NMOS Operating Regions (III)

- Saturation



Saturation:
Channel Pinched Off
I_{ds} Independent of V_{ds}

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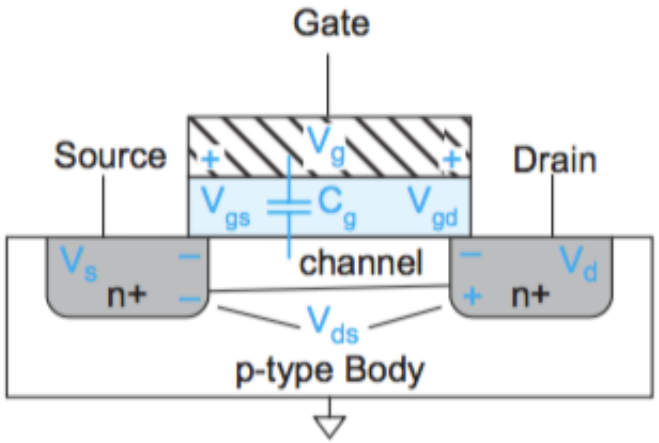
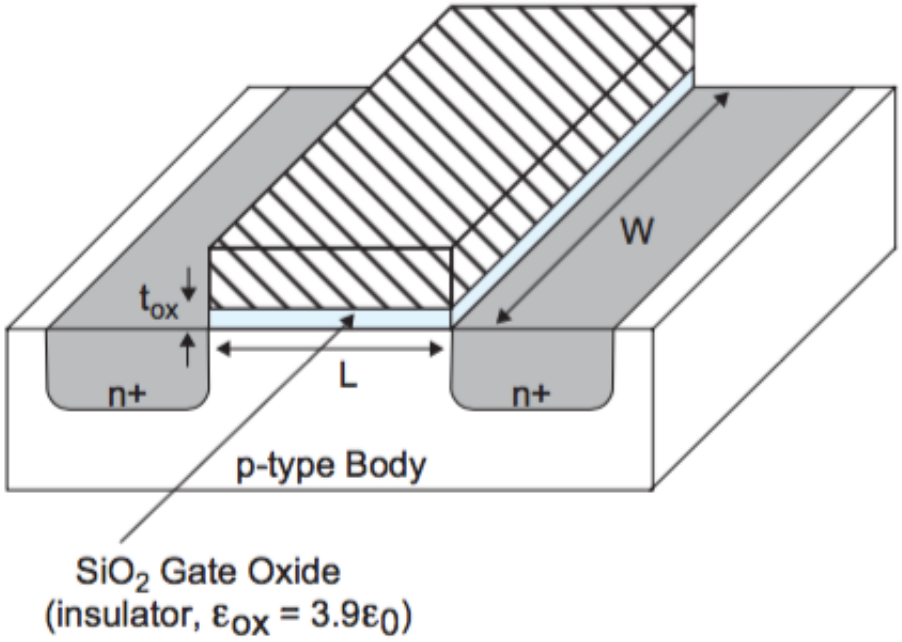
MOS Channel Charge



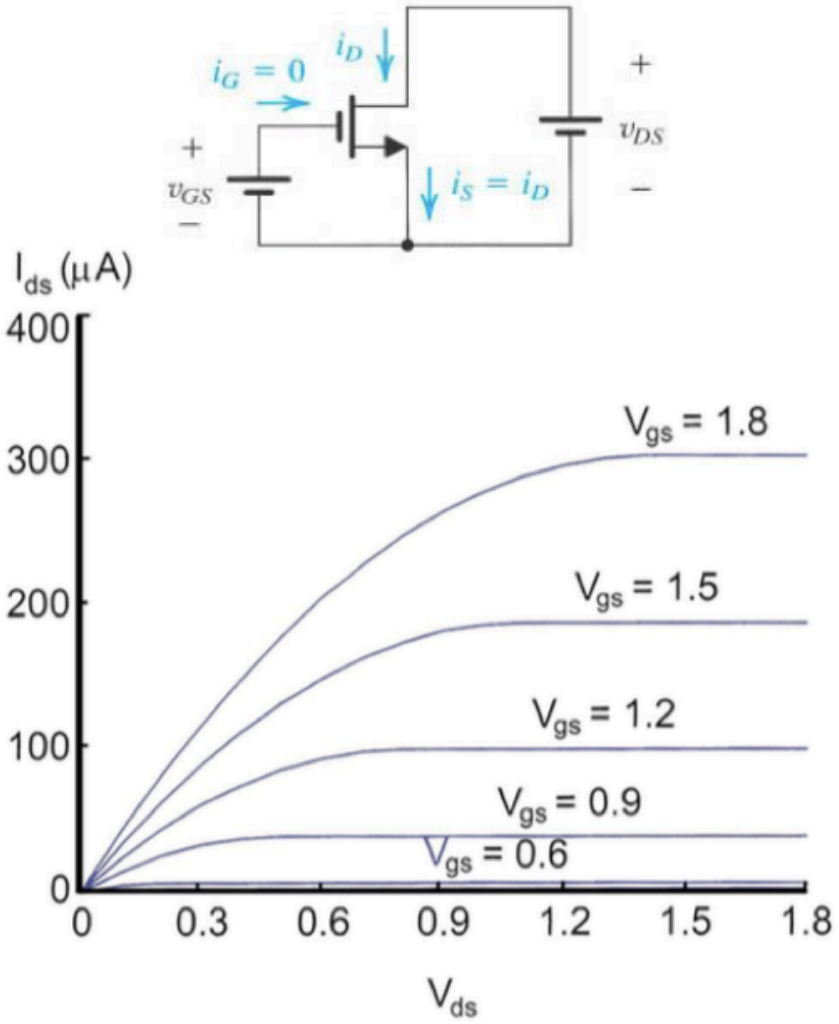
Average gate to channel potential:

$V_{gc} = (V_{gs} + V_{gd})/2 = V_{gs} - V_{ds}/2$

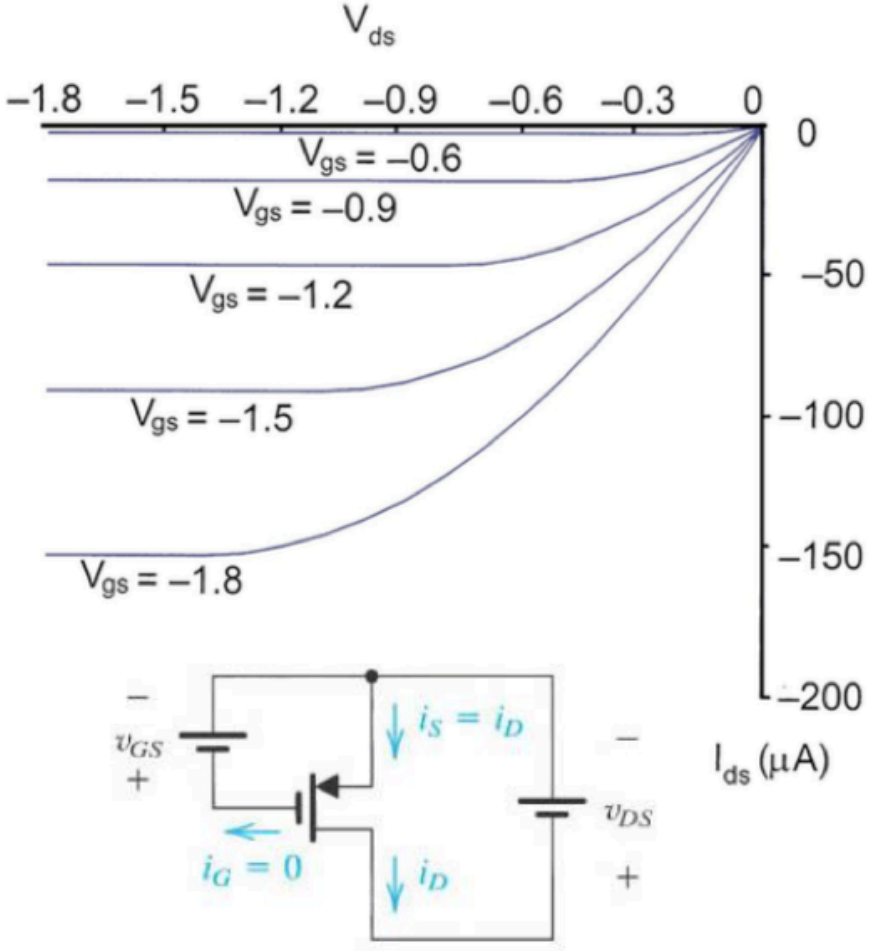


Ideal I-V Equations

Ideal I-V Characteristics



- nMOS I-V



- pMOS I-V

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- **Nonideal Effects**
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Nonideal I-V Effects

- **Velocity saturation** at high V_{ds} ↑, the carrier velocity is no longer proportional to lateral field. I_{ds} decrease ↓.
- **Mobility degradation** at high V_{gs} ↑, the carrier scatter more and mobility decreases. I_{ds} decrease ↓.
- **Channel length modulation** at high V_{ds} ↑, depletion of S/D ↑, effective L ↓, I_{ds} increase ↑.
- **Body effect** threshold voltage Vth influenced by vbs (body-to-source voltage).
- **Subthreshold conduction** Vgs < Vth, Ids is exponentially dropoff instead of abruptly becoming zero
- **Drain/source leakage** reverse diode junction leakage
- **Non-zero gate current Ig** carriers tunneling effect

Velocity Saturation

- **Carrier velocity** nonlinearly proportional to lateral electrical field before velocity saturation

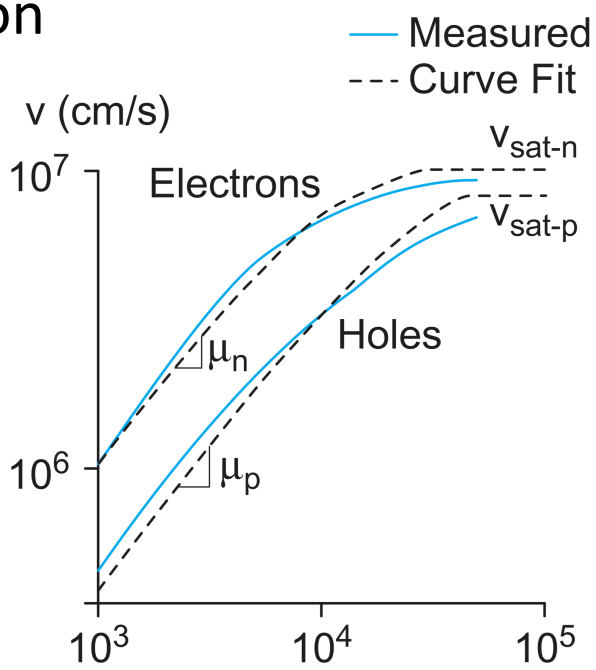
$$\upsilon = \mu E_{lat} \big/ \left(1 + E_{lat} / E_{sat}\right)$$

υ : carrier velocity

μ : mobility

$E_{lat} = V_{ds} / L$: lateral electrical field

$E_{sat} = \upsilon_{sat} / \mu$



- I_{ds} will saturate to velocity saturation, depending on channel length **L** and applied $\mathbf{V_{ds}}$

$$I_{ds} = \frac{Q_{channel}}{t_{channel}} = \frac{Q_{channel}}{L / \upsilon_{sat}} = C_{ox} W \left(V_{gs} - V_t\right) \upsilon_{sat}$$

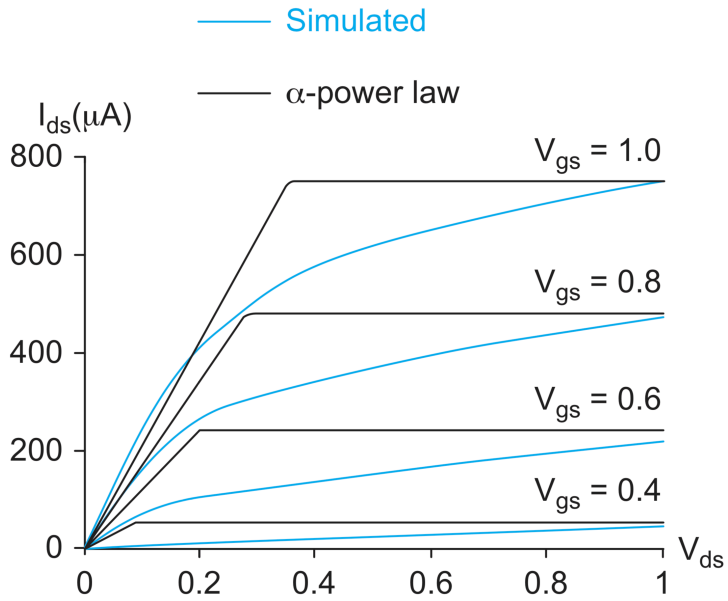
α-power Law Model

- Piecewise linear model to illustrate MOSFET's I-V characteristic with velocity saturation

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ I_{dsat}\dfrac{V_{ds}}{V_{dsat}} & V_{ds} < V_{dsat} \quad \text{linear} \\ I_{dsat} & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

$$I_{dsat} = P_c \frac{\beta}{2}\left(V_{gs} - V_t\right)^{\alpha}, \; V_{dsat} = P_v\left(V_{gs} - V_t\right)^{\alpha/2}$$

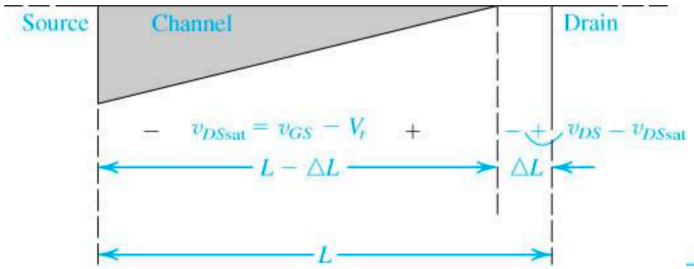
Empirical parameters: P_c, P_v, α



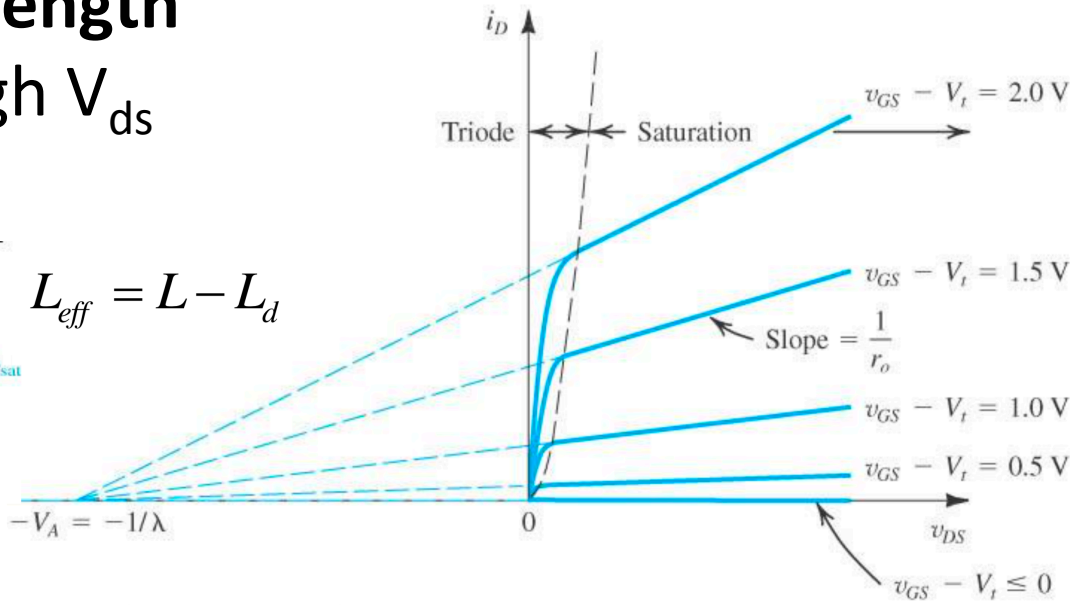
- **Because $\mu_p < \mu_n$**, PMOS experiences less velocity saturation than NMOS → $\alpha_p > \alpha_n$
- **Mobility degradation** is modeled by a $\mu_{eff} < \mu$, and it can be included in to the parameter α

Channel Length Modulation

- **Effective channel length** reduced due to high V_{ds}



$$L_{eff} = L - L_d$$



- I-V equation at saturation region:
  - λ' empirical parameter

$$I_{ds} = \beta \frac{\left(V_{gs} - V_t\right)^2}{2}\left(1 + \lambda V_{ds}\right), \lambda = \lambda' / L$$

- With shorter L ↓, λ ↑, resulting in output resistance ↓, MOSFET intrinsic gain ↓

Body Effect

- Threshold voltage Vth increased with positive V_{sb}
- $V_{sb} < 0$ → Vth ↓, OFF leakage ↑ (design trade-off)

$$V_t = V_{t0} + \gamma[\sqrt{2\varphi_s + V_{sb}} - \sqrt{2\varphi_s}], \qquad \varphi_s = 2\upsilon_T \ln\frac{N_A}{n_i}$$

$V↓t0$: threshold voltage for $V_{sb} = 0$
$\phi↓f$: process-dependent parameter

$$\gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2qN_A\varepsilon_{si}} = \frac{\sqrt{2qN_A\varepsilon_{si}}}{C_{ox}}$$

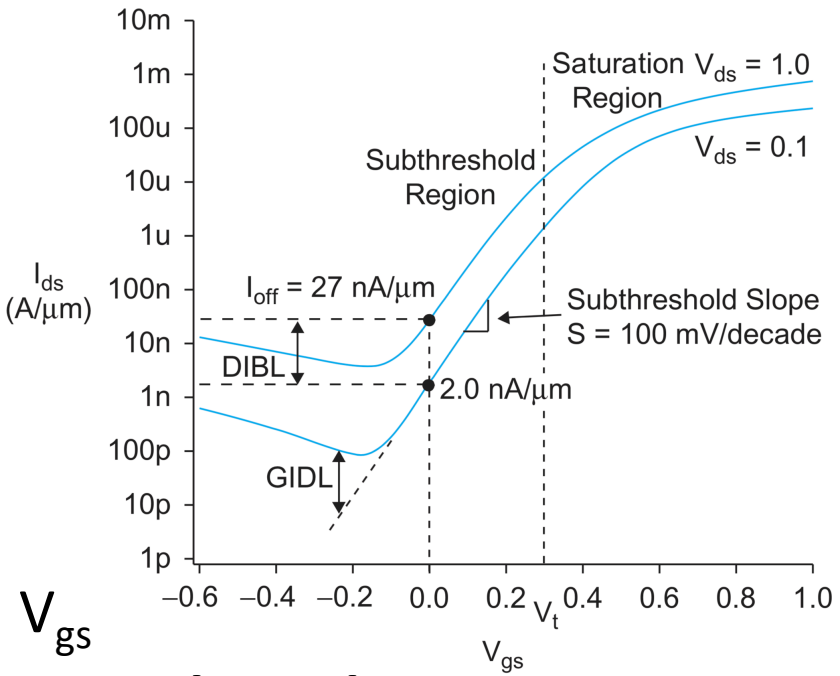
γ: body-effect coefficient (process-depedent)
$N↓A$: doping concentration of p-substrate
$\varepsilon↓s$: permittivity of silicon = 11.7 $\varepsilon↓0$

Subthreshold Conduction

- Leakage current at subthreshold region
  - $V_{gs} < V_{th}$: weak inversion

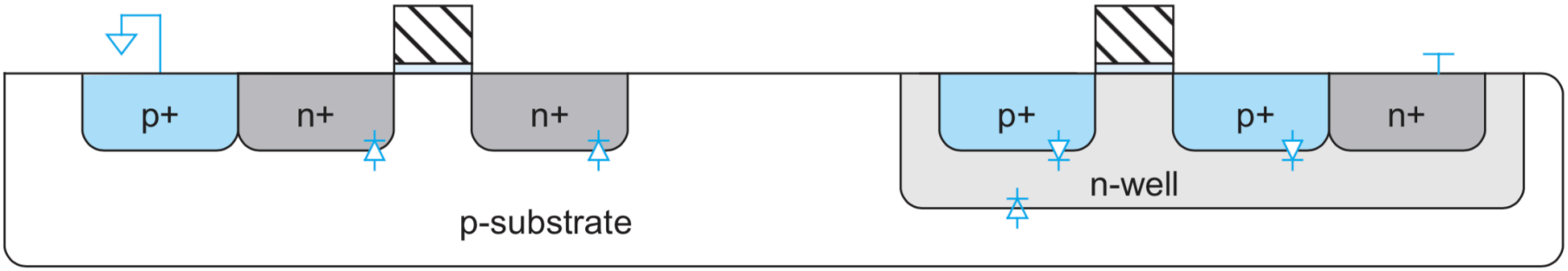
$$I_{ds} = I_{ds0} e^{\frac{V_{gs}-V_t}{n\upsilon_T}} \left(1 - e^{\frac{-V_{ds}}{\upsilon_T}}\right)$$

$$I_{ds0} = \beta \upsilon_T^2 e^{1.8}$$



- $I_d = 0$ when $V_{ds} = 0$
  - Increase exponentially with V_{gs}
- **Drain-induced barrier lowering (DIBL)**
  - V_{th} will reduce with positive V_{ds}
  - Worsens leakage at subthreshold
  - Like channel-length modulation at active mode

Junction Leakage

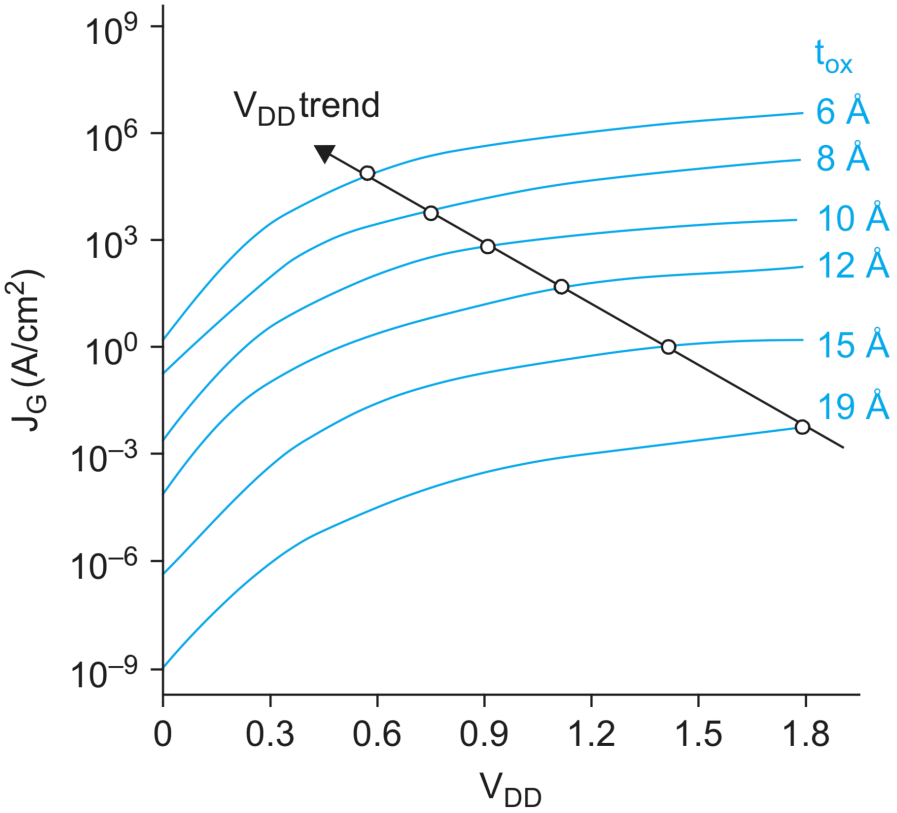


- S/D junction leakage from a reverse-biased diode

$$I_D = I_S\left(e^{\frac{V_D}{\upsilon_T}} - 1\right)$$

- Junction leakage used to be the limitation for storage time. In modern processes, subthreshold leakage becomes dominant

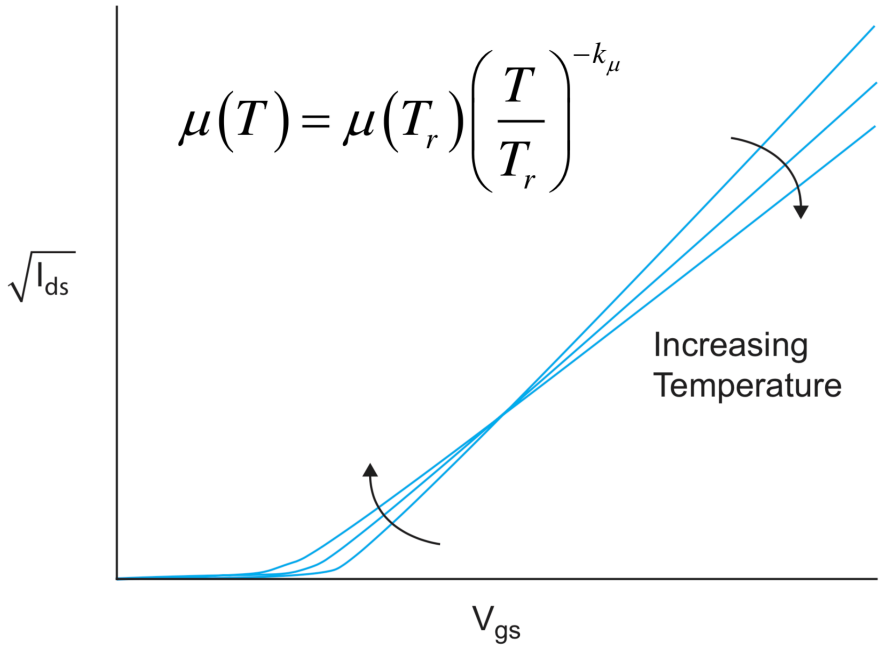
Tunneling Effect



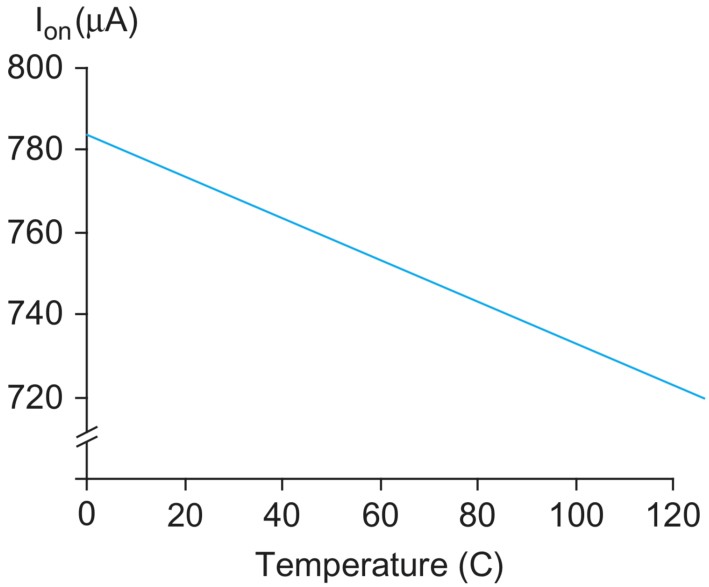
- Gate leakage: from carriers' tunneling through gate oxide. Exponentially inversely proportional to gate oxide thickness.
- High-*k* (dielectric constant) gate insulator used

Temperature Dependence

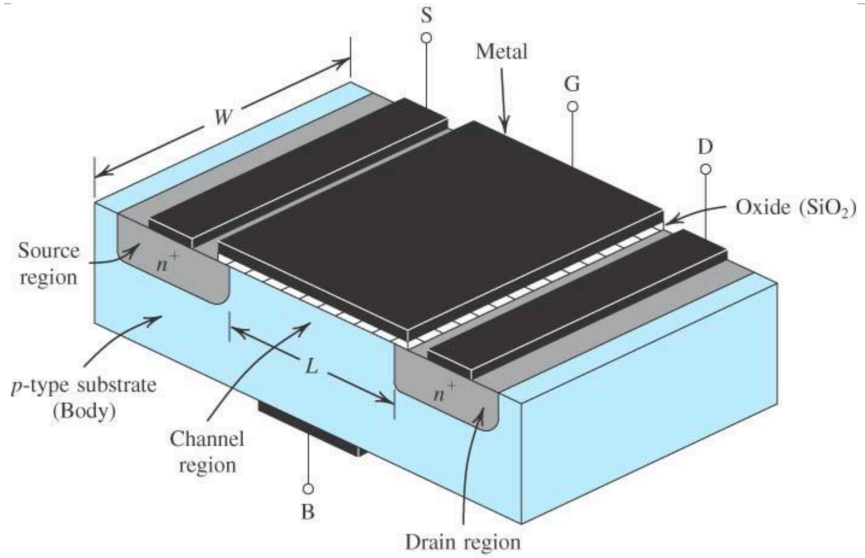
- T ↑ IOFF ↑ ION
- Circuit performance improve with T ↓: subthreshold leakage ↓, saturation velocity ↑, mobility ↑, junction capacitance ↓, but breakdown voltage ↓.

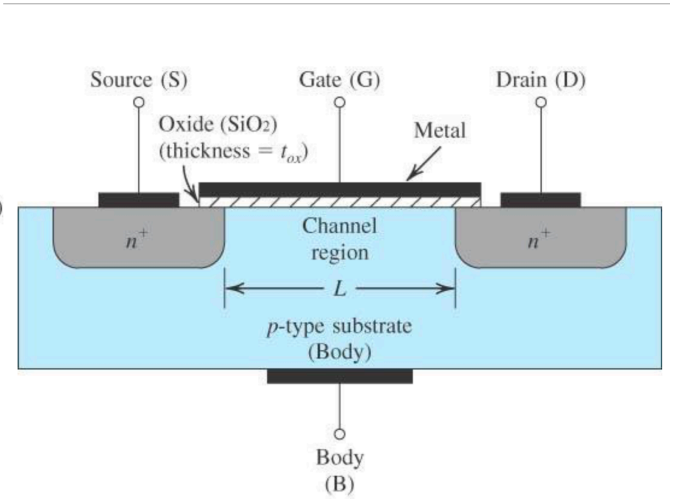


$$V_t(T) = V_t(T_r) - k_{vt}(T - T_r)$$



Geometry Dependence





- Effective channel length and width

$$L_{eff} = L_{drawn} + X_L - 2L_D \qquad X_L, X_W : \text{Poly over-etch}$$

$$W_{eff} = W_{drawn} + X_W - 2W_D \qquad L_D, W_D : \text{Source-drian lateral diffusion}$$

- Use identical and same orientation for MOSFETs for good matching – **EX:** differential pair, current mirror

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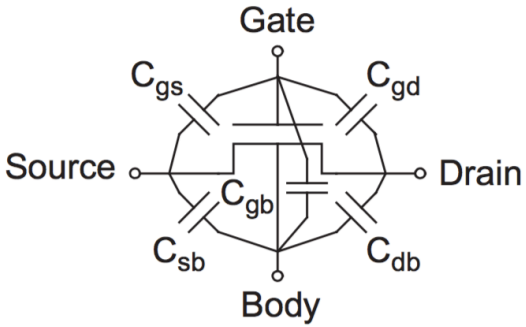
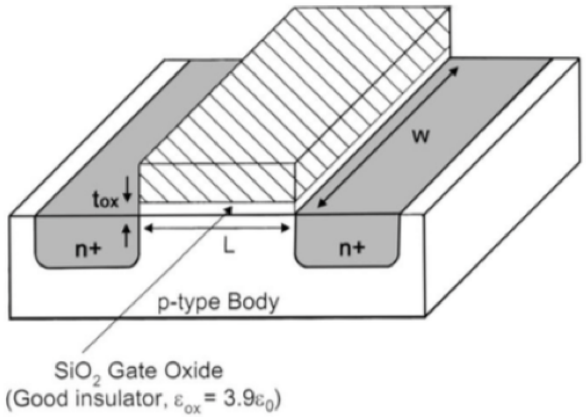
C-V Characteristics

- **Gate capacitance:** with advanced technology, t_{ox} ↓, L ↓, $C_{permicron}$ keeps constant

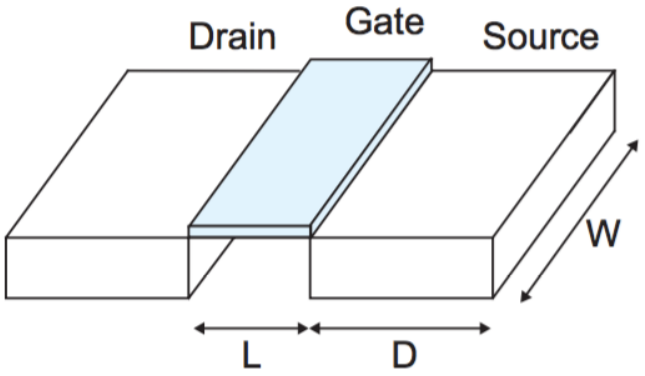
$$C_g = C_{ox}WL = C_{permicron}W$$

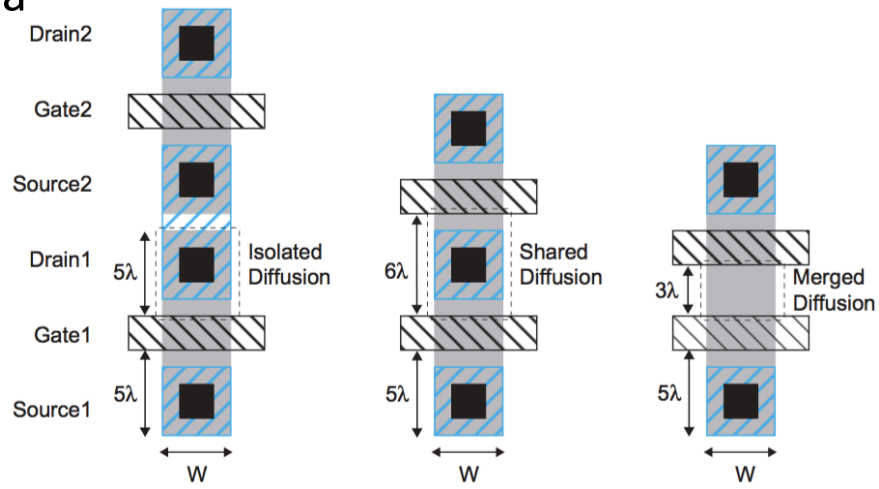
$$C_{permicron} = C_{ox}L = \frac{\varepsilon_{ox}}{t_{ox}}L$$





- **Parasitic capacitance:** C_{db} and C_{sb} from reverse-biased p-n junction and proportional to S/D area





MOS Gate Capacitance Model

- **Gate capacitance:** vary with channel behavior at different operation regions

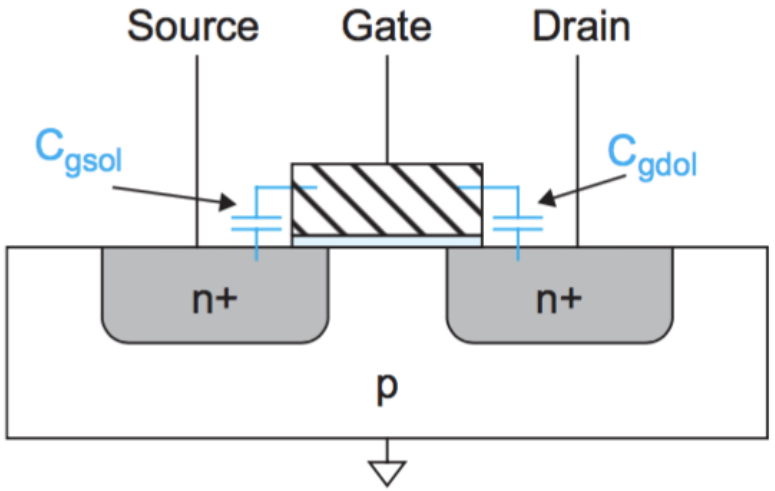
$$C_0 = C_{ox}WL$$

Parameter	Cutoff	Linear	Saturation
C_{gb}	$\leq C_0$	0	0
C_{gs}	0	$C_0/2$	$2/3\ C_0$
C_{gd}	0	$C_0/2$	0
$C_g = C_{gs} + C_{gd} + C_{gb}$	C_0	C_0	$2/3\ C_0$

- **S/D overlap capacitance:** Cgs(overlap) and Cgd(overlap) from S/D lateral diffusion

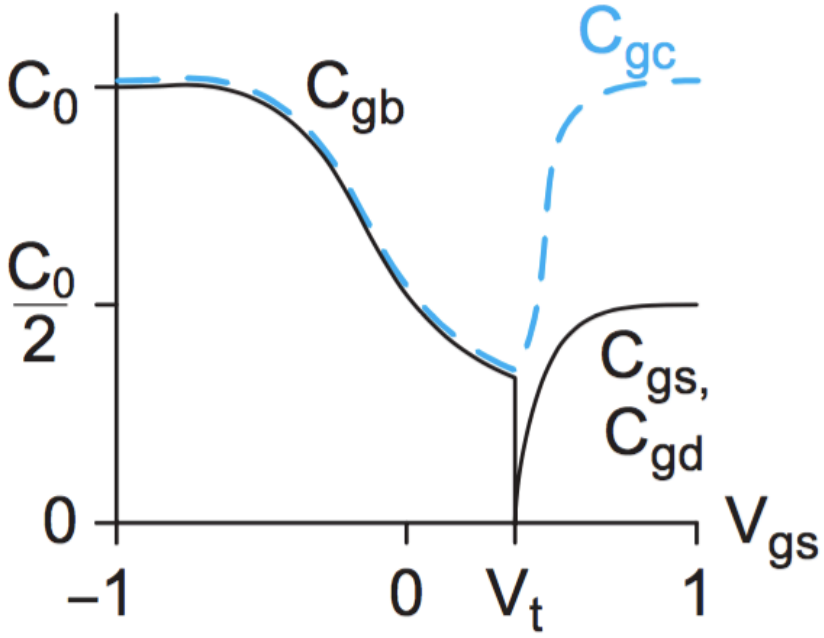
$$C_{gs(overlap)} = C_{gsol}W$$

$$C_{gd(overlap)} = C_{gdol}W$$

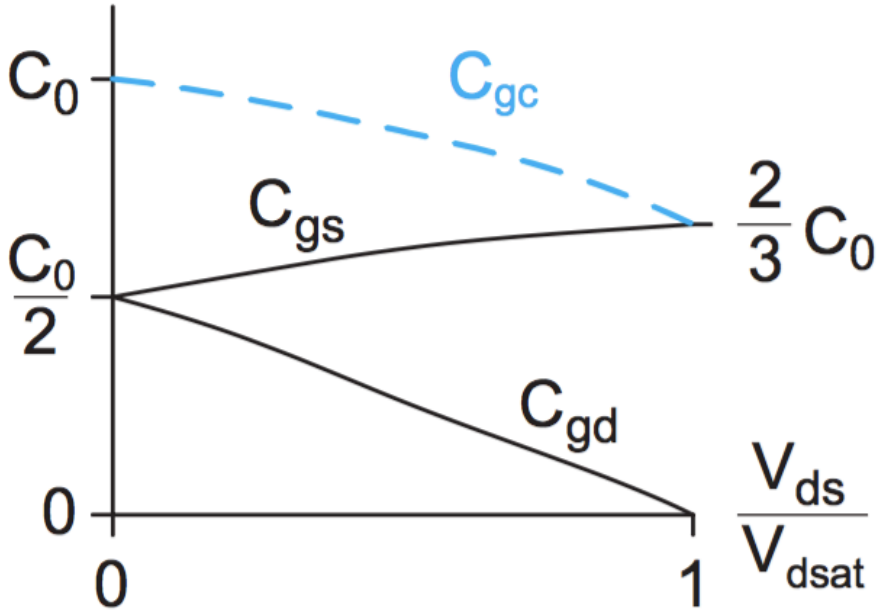


C_{gc} vs. V_{gs} and V_{ds}

- C_{gc} vs. V_{gs}

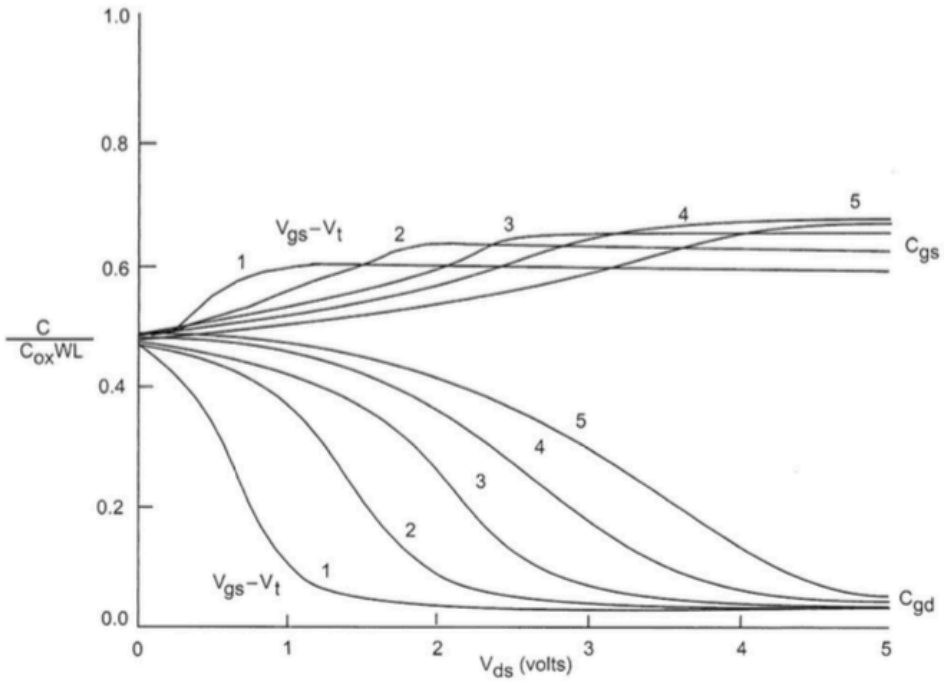


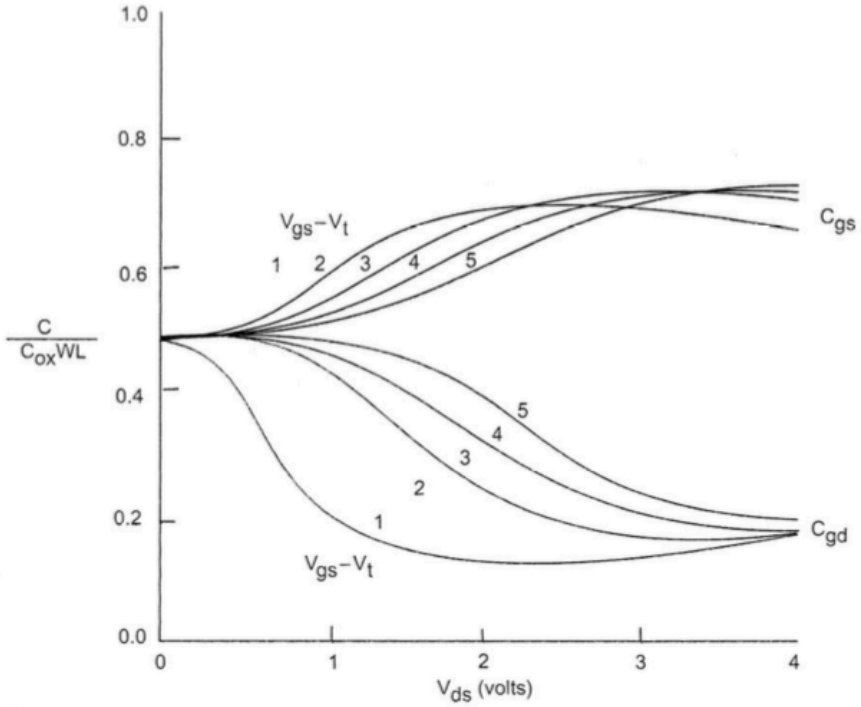
- C_{gc} vs. V_{ds}



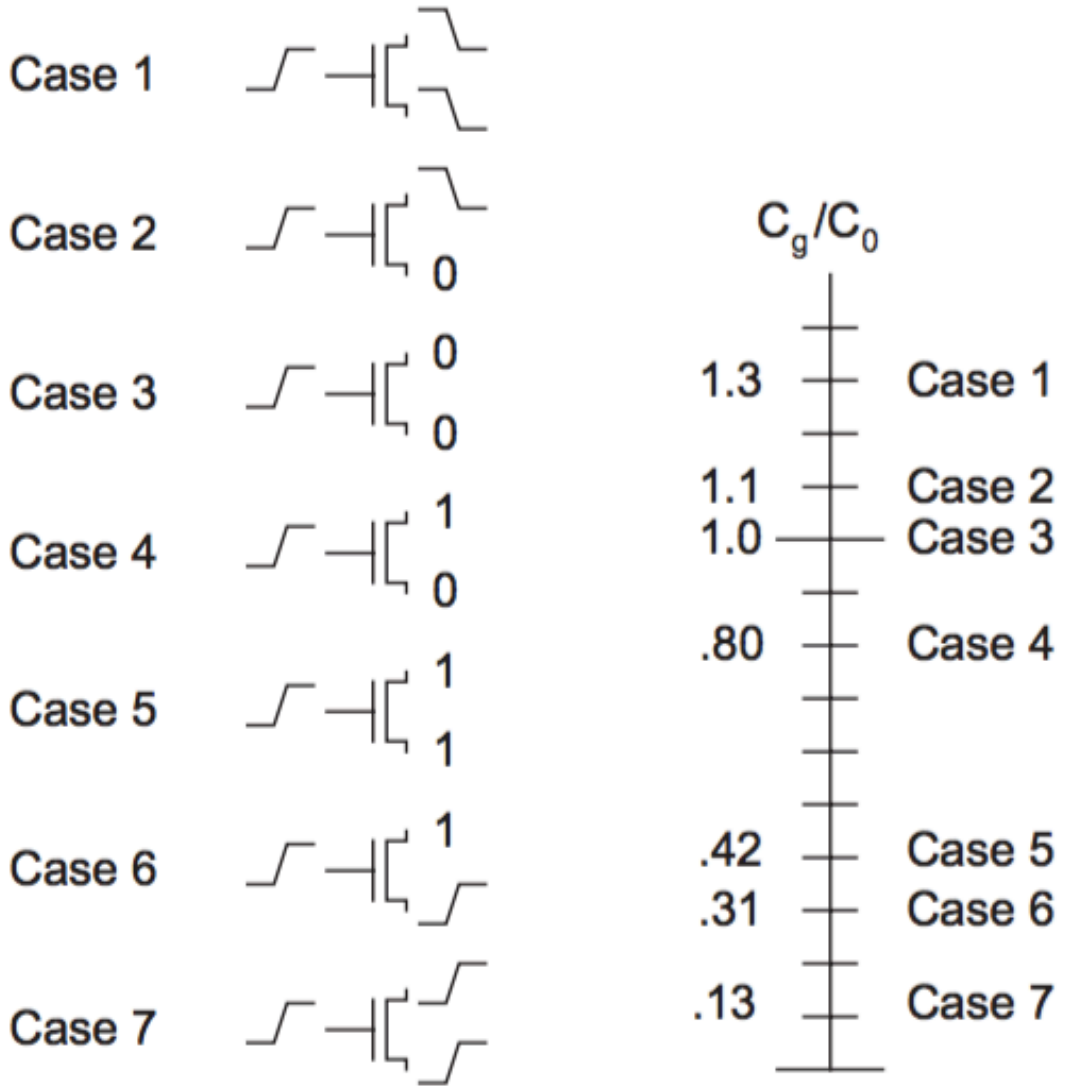
Gate Capacitance vs V_{ds}

- **Long-channel device:**
  C_{gd} becomes ~0 at saturation
- **Short-channel device:**
  more $C_{gd(overlap)}$ and $C_{gs(overlap)}$ factor





Data-Dependent Gate Capacitance



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- **DC transfer characteristics**
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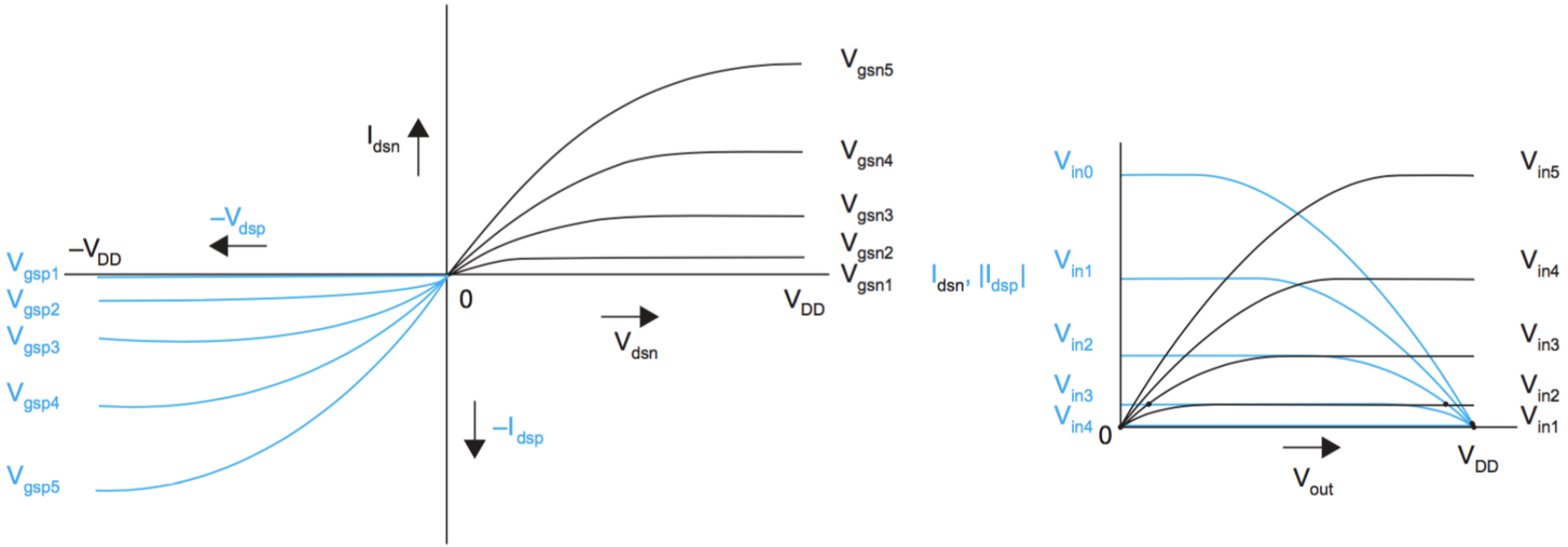
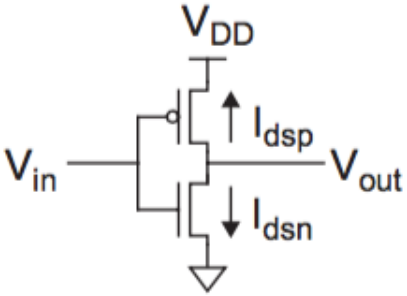
CMOS Inverter DC Characteristics (I)

	Cutoff	Linear	Saturated
nMOS	$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$	$V_{gsn} > V_{tn}$
	$V_{in} < V_{tn}$	$V_{in} > V_{tn}$	$V_{in} > V_{tn}$
		$V_{dsn} < V_{gsn} - V_{tn}$	$V_{dsn} > V_{gsn} - V_{tn}$
		$V_{out} < V_{in} - V_{tn}$	$V_{out} > V_{in} - V_{tn}$
pMOS	$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$	$V_{gsp} < V_{tp}$
	$V_{in} > V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$
		$V_{dsp} > V_{gsp} - V_{tp}$	$V_{dsp} < V_{gsp} - V_{tp}$
		$V_{out} > V_{in} - V_{tp}$	$V_{out} < V_{in} - V_{tp}$

CMOS Inverter DC Characteristics (II)

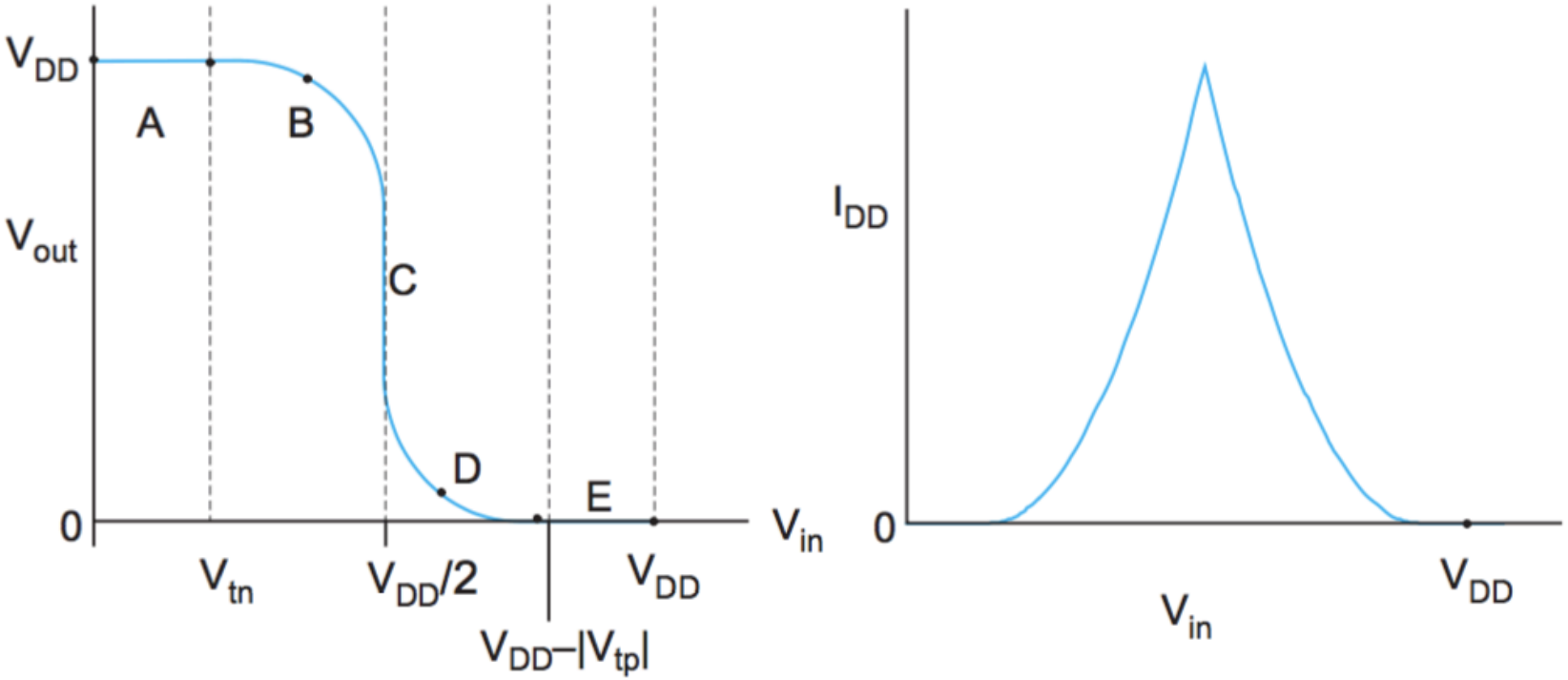


- I_{ds} vs. V_{ds} for NMOS and PMOS
- For PMOS, I_d, V_{gs}, V_{ds}, $V_{th} < 0$
- PMOS I-V as load-line for NMOS



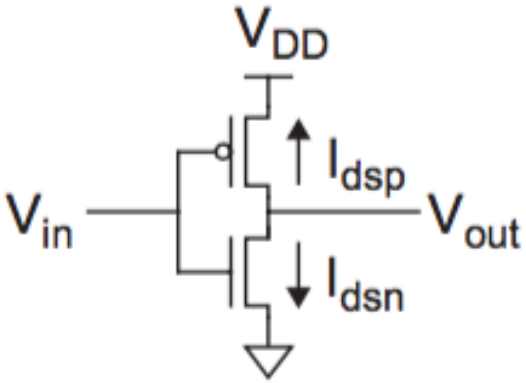
CMOS Inverter DC Characteristics (III)

- V_{in}-V_{out} DC transfer curve
- Rail-to-rail operation
- V_{in}-I_{DD} DC transfer curve
- Dynamic power dissipation



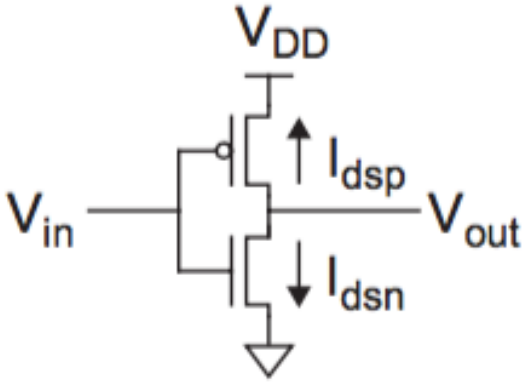
DC Response

- DC response: V_{out} vs. V_{in} for a gate
- **Ex: inverter**
  - $V_{in} = 0 \rightarrow V_{out} = V_{DD}$
  - $V_{in} = V_{DD} \rightarrow V_{out} = 0$
  - In between, V_{out} depends on transistor sizes and currents
  - By KCL must settle such that $I_{dsn} = |I_{dsp}|$
  - We could solve equations
  - Graphical solution gives more insight



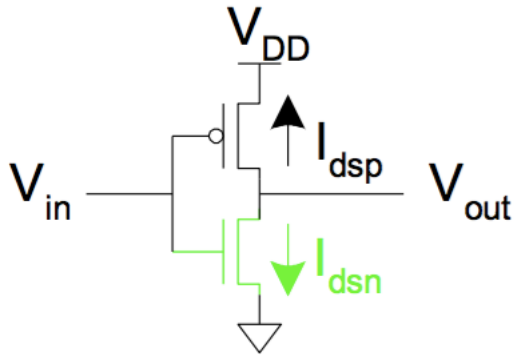
Transistor Operating Regions

- Transistor current depends on operating regions
- For what V_{in} and V_{out} are NMOS and PMOS in
  - Cutoff?
  - Linear?
  - Saturation?



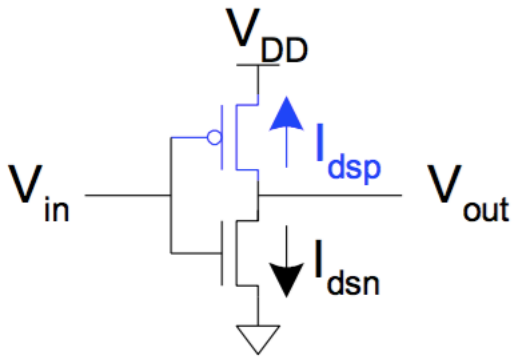
NMOS Operating Regions

Cutoff	Linear	Saturation



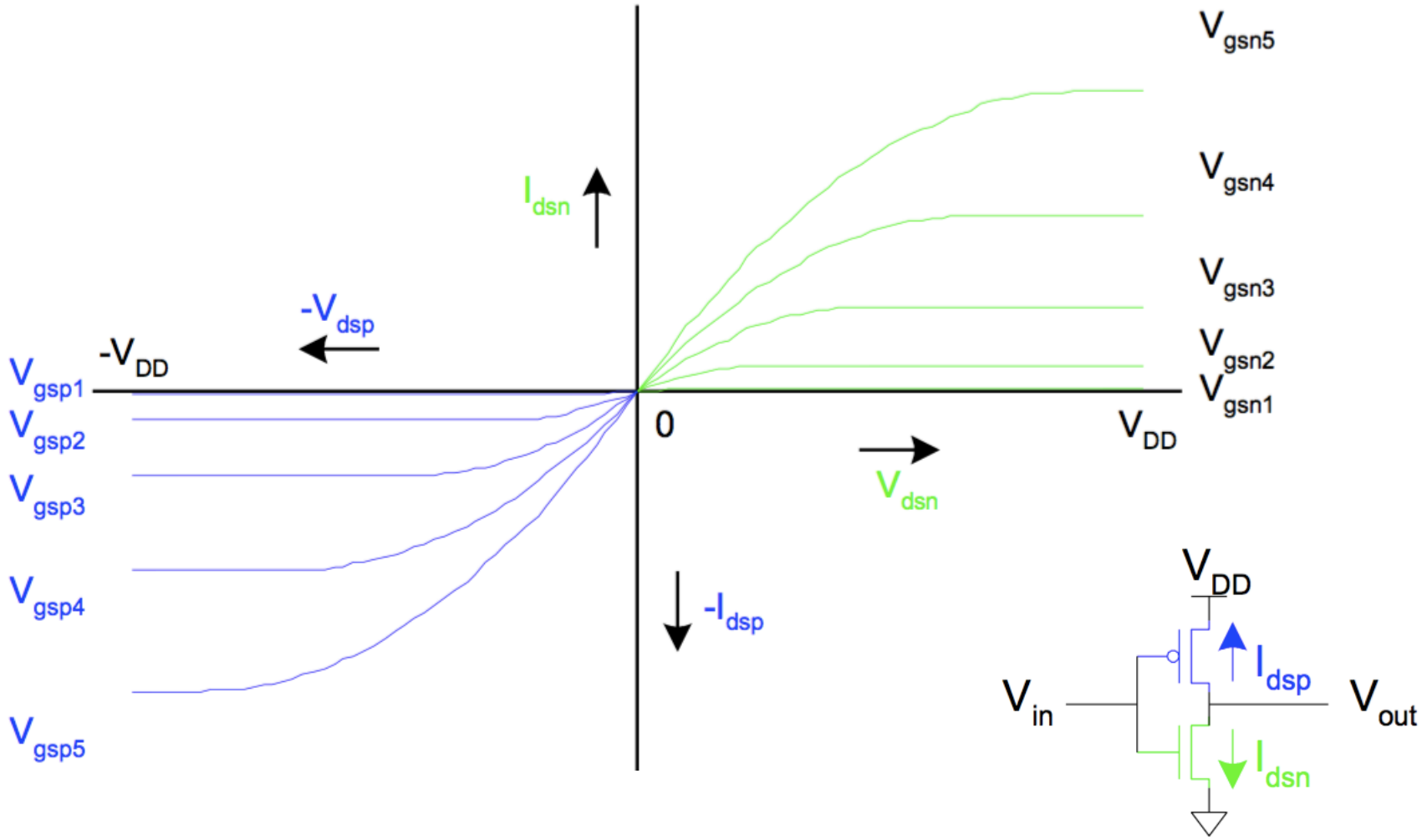
PMOS Operating Regions

Cutoff	Linear	Saturation

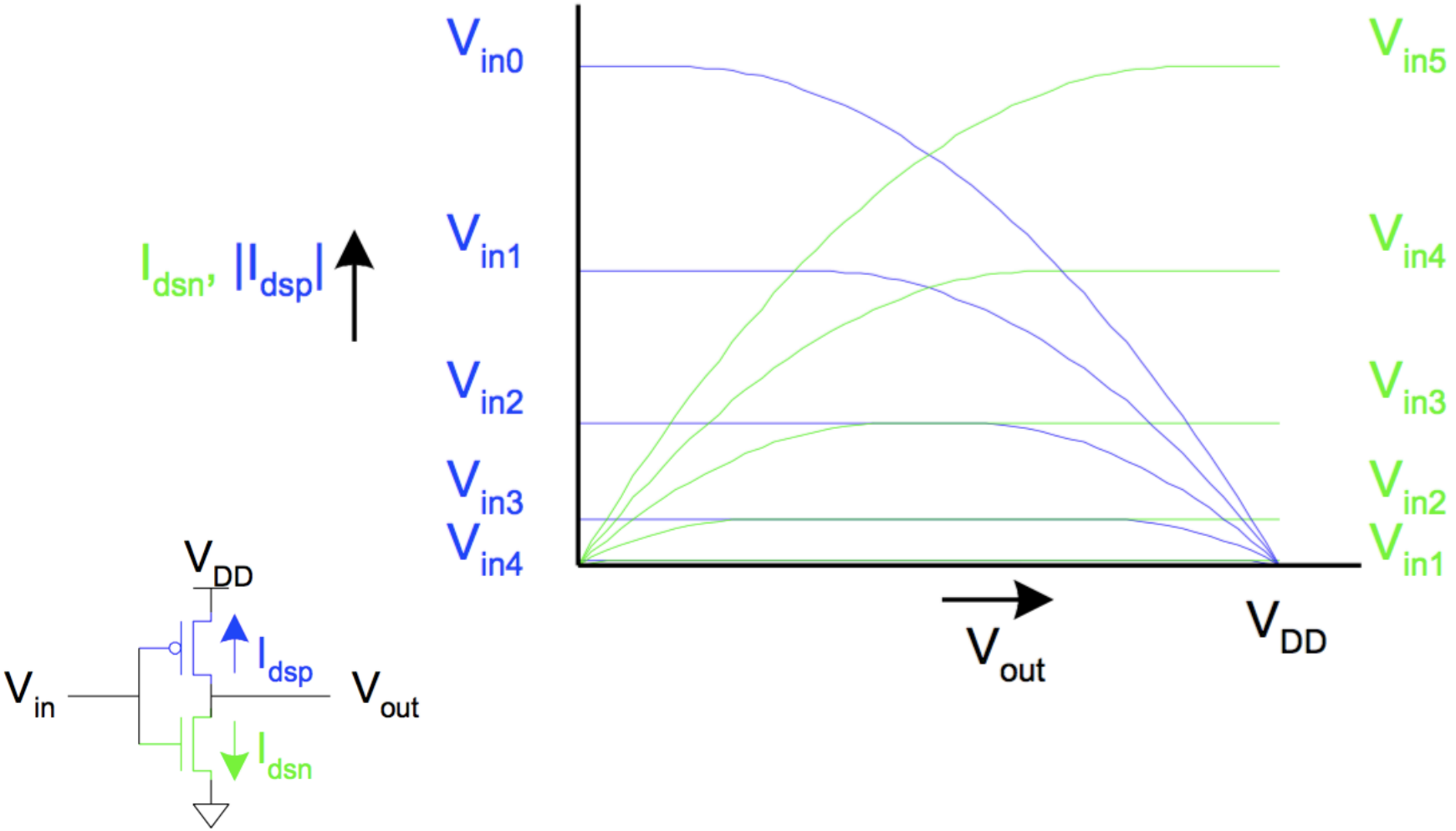


I-V Characteristics

- Make PMOS wider than NMOS so that $\beta_p = \beta_n$

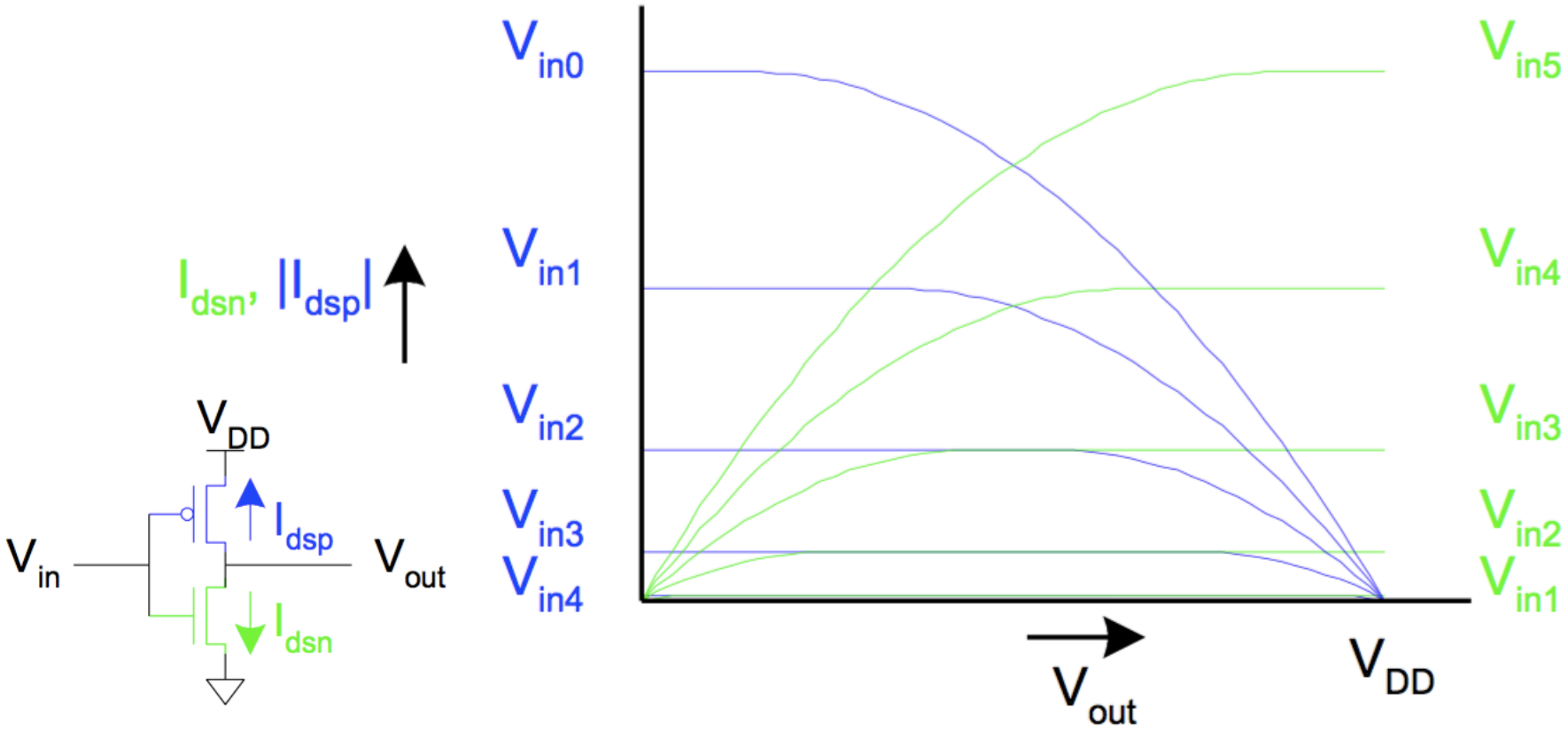


Currents vs. V_{in} and V_{out}



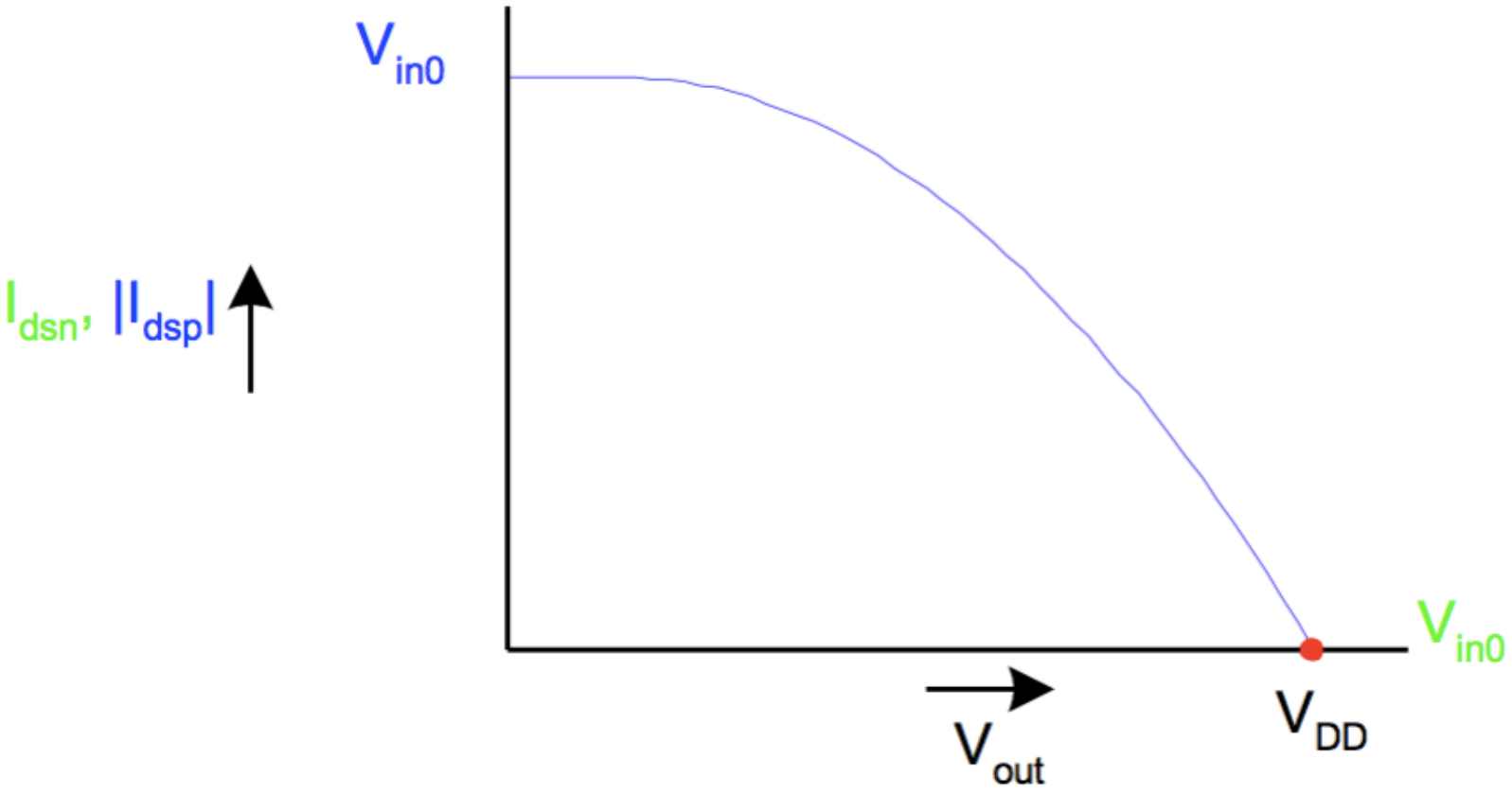
Load Line Analysis (I)

- For a given V_{in}
  - Plot I_{dsn}, I_{dsp} vs. V_{out}
  - V_{out} must be where KCL is satisfied (currents are equal)



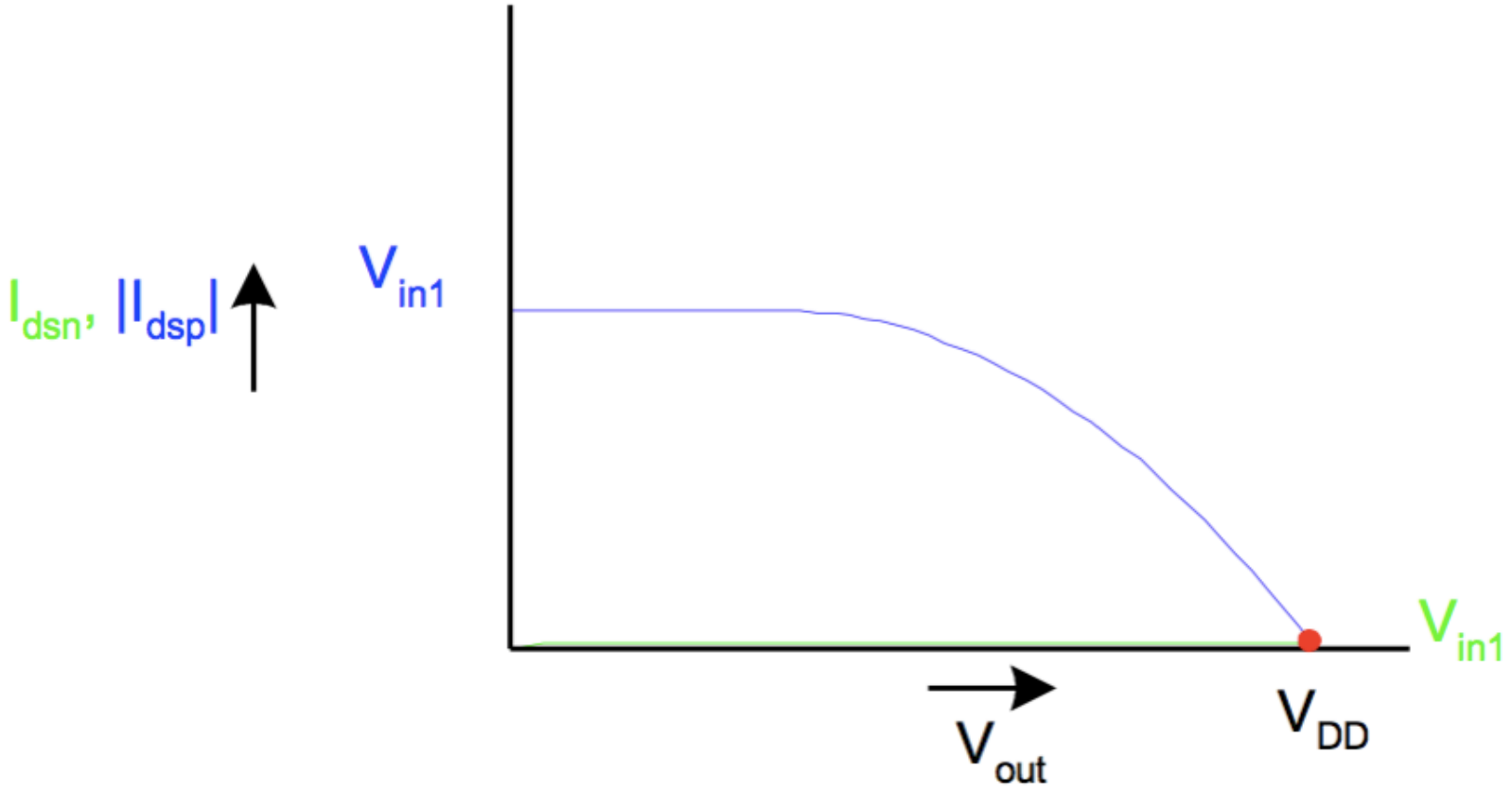
Load Line Analysis (II)

- $V_{in} = 0$



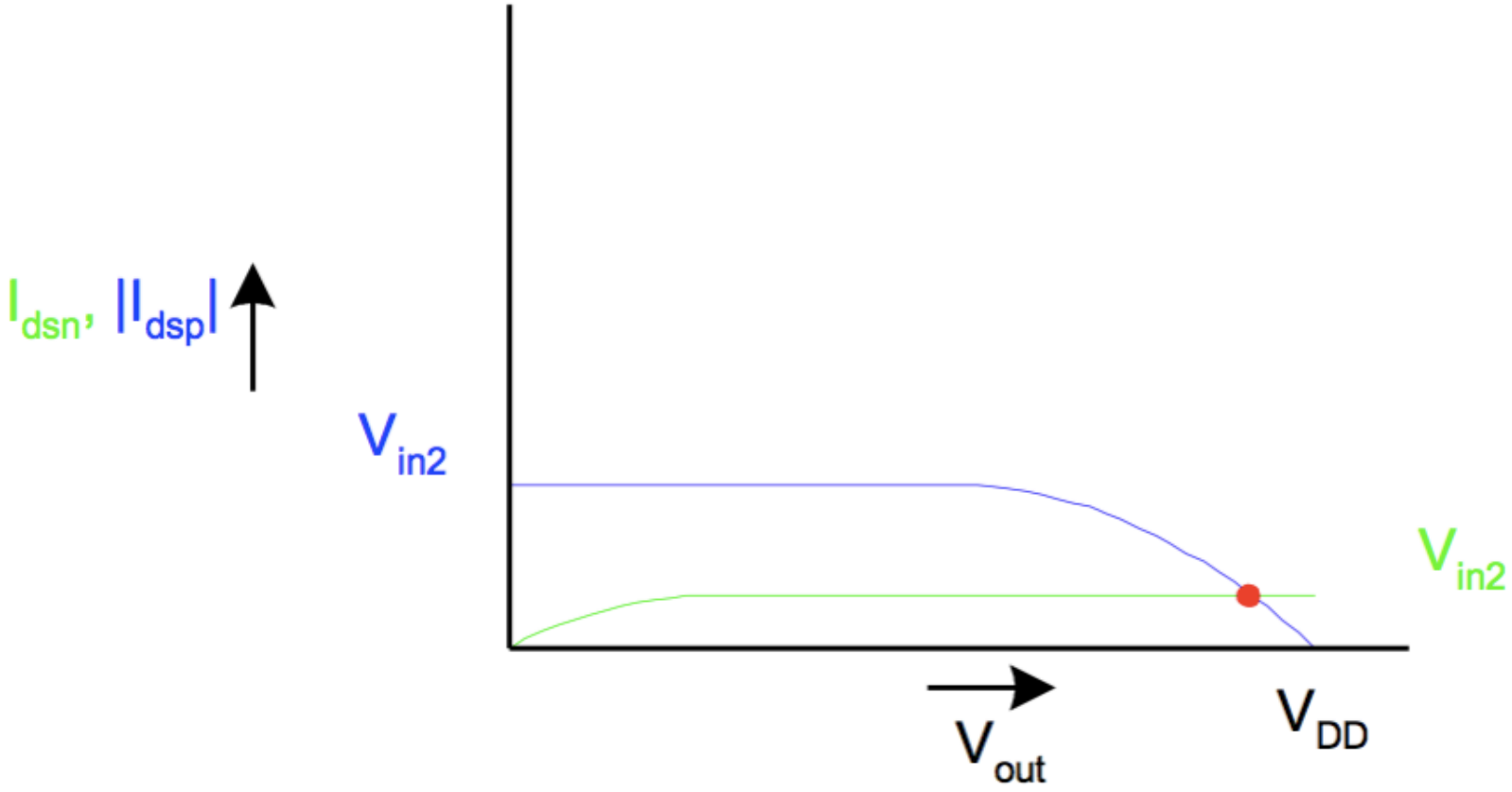
Load Line Analysis (III)

- $V_{in} = 0.2\ V_{DD}$



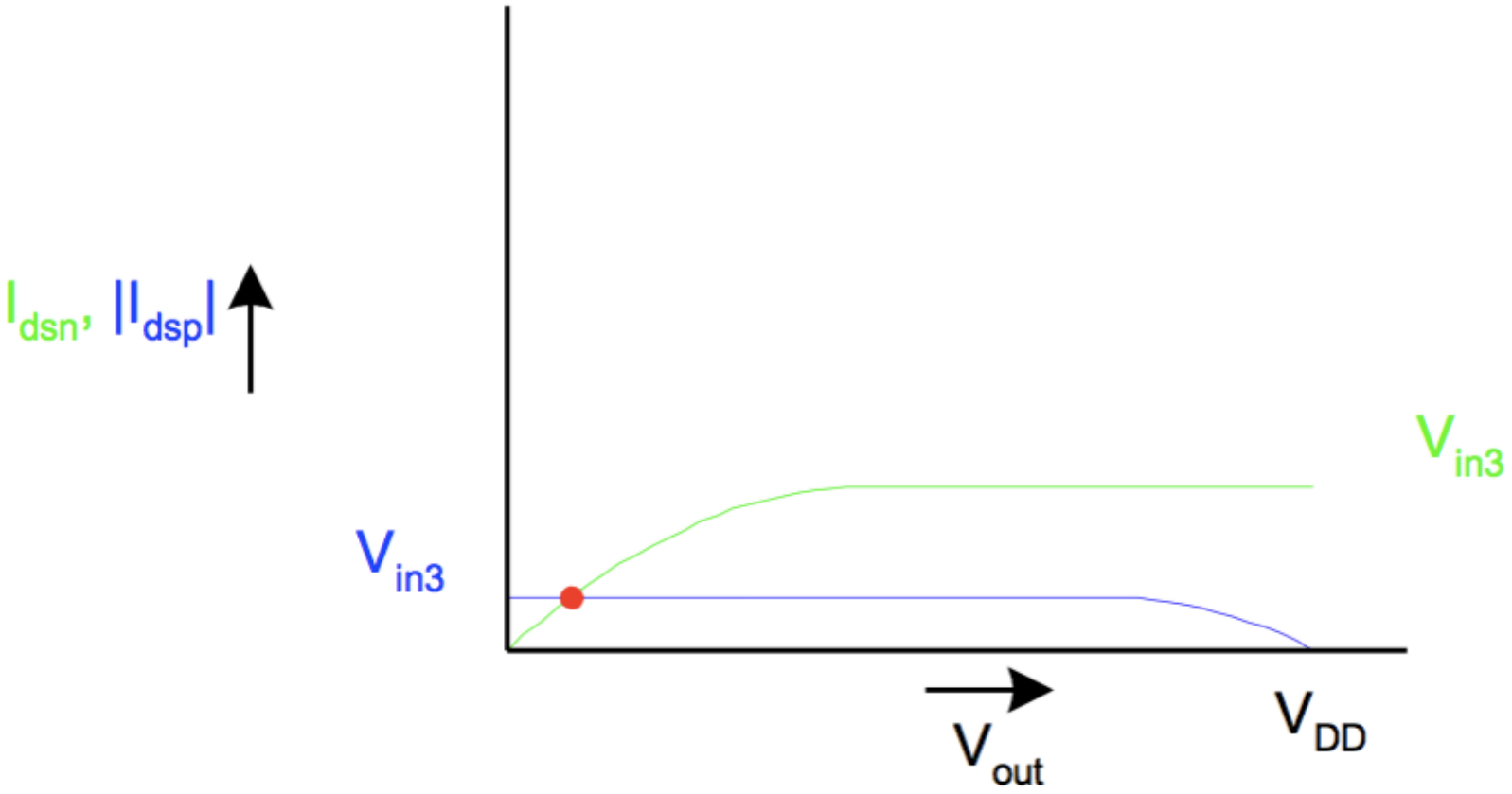
Load Line Analysis (IV)

- $V_{in} = 0.4\ V_{DD}$



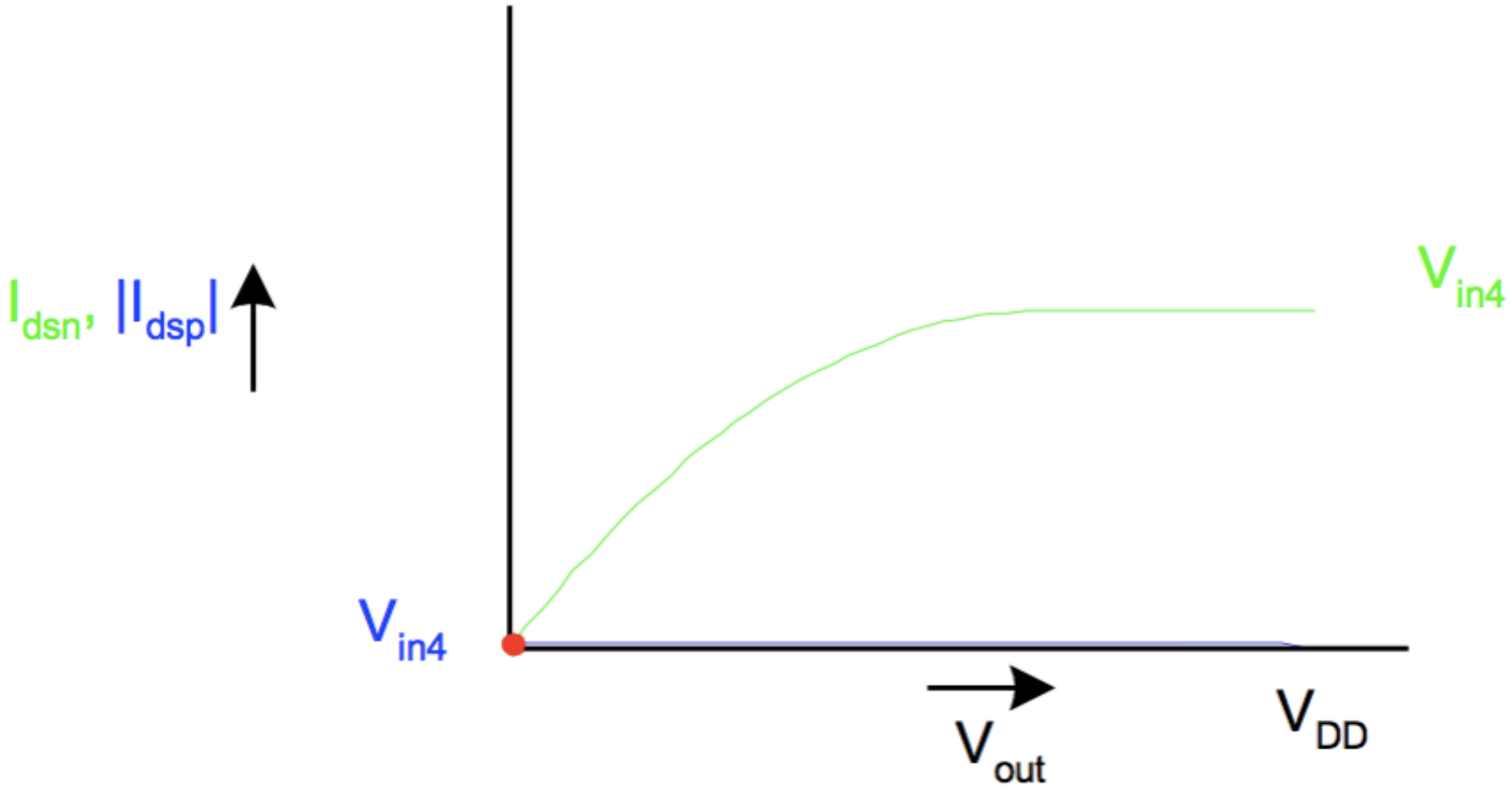
Load Line Analysis (V)

- $V_{in} = 0.6\ V_{DD}$



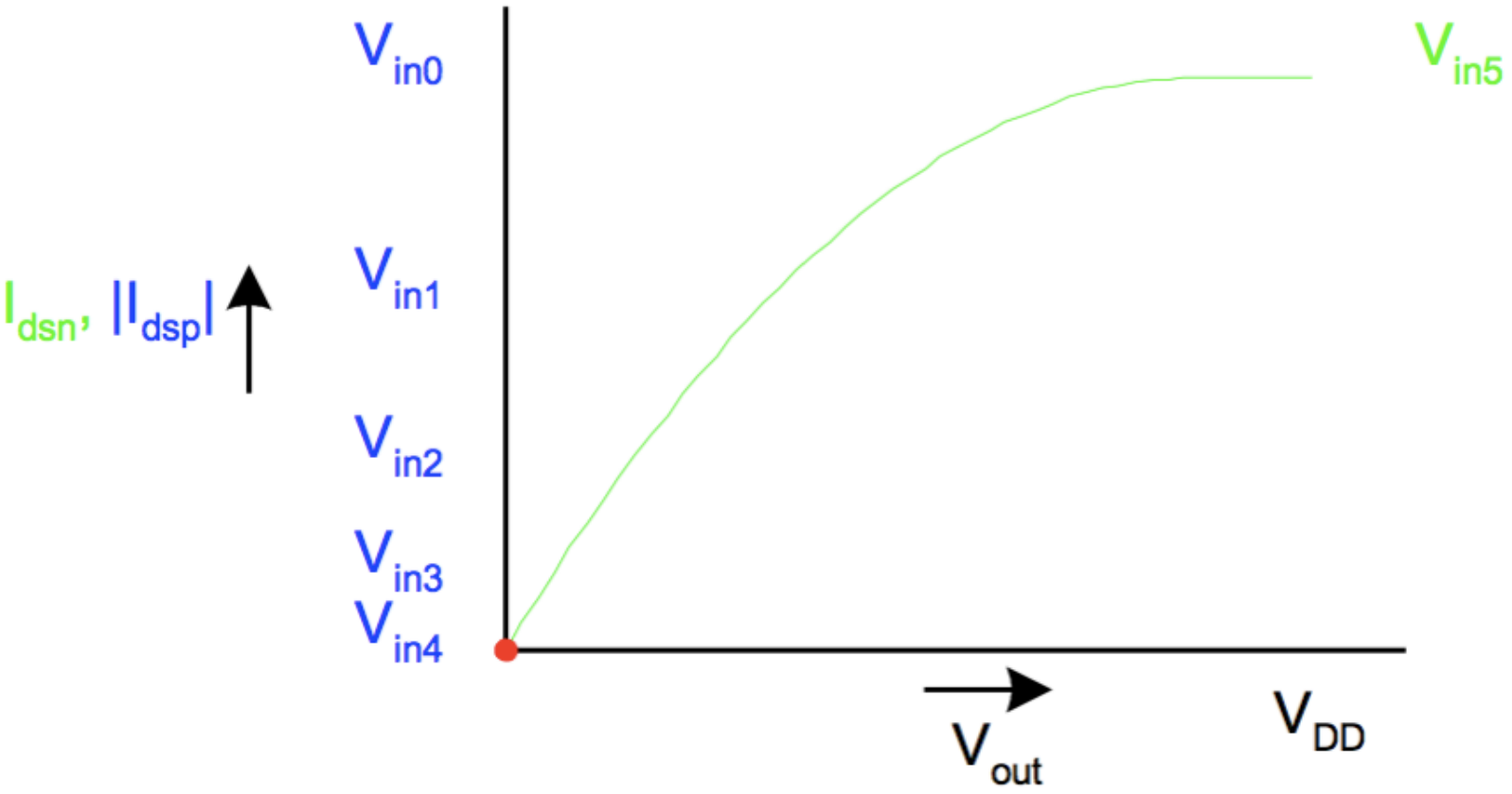
Load Line Analysis (VI)

- $V_{in} = 0.8\ V_{DD}$



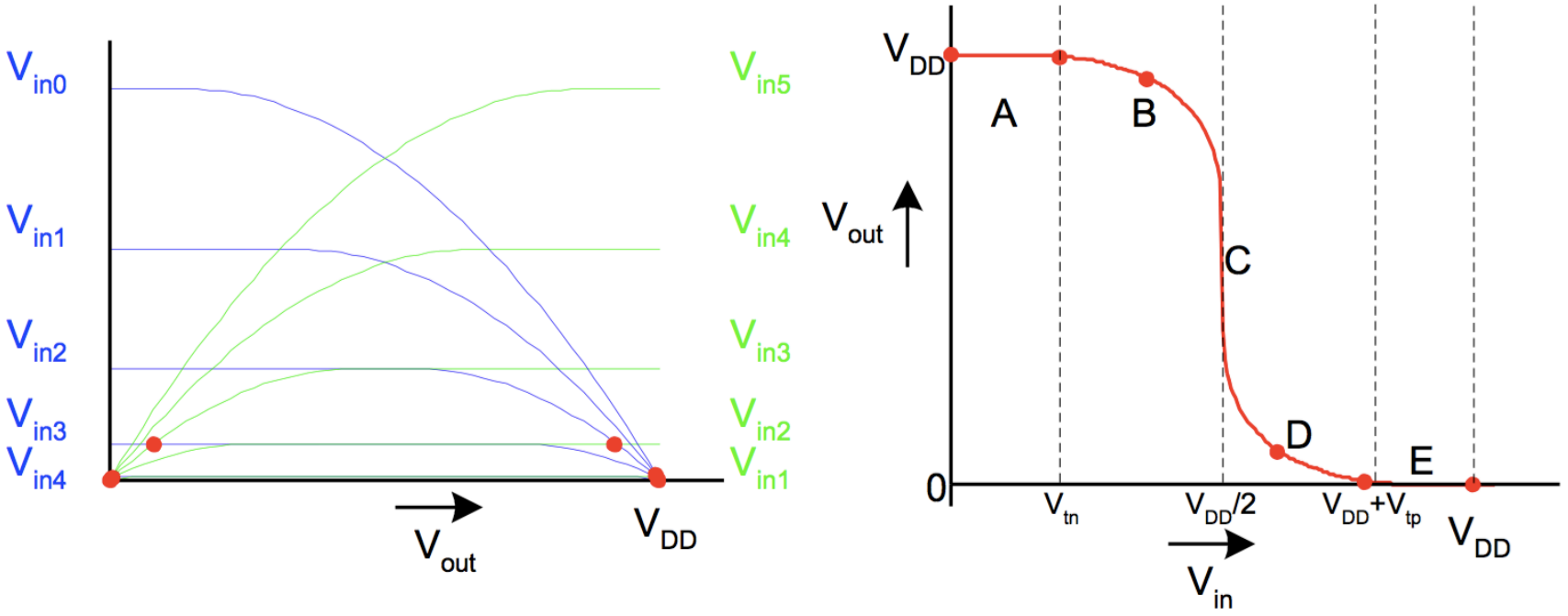
Load Line Analysis Summary

- $V_{in} = 1.0\ V_{DD}$



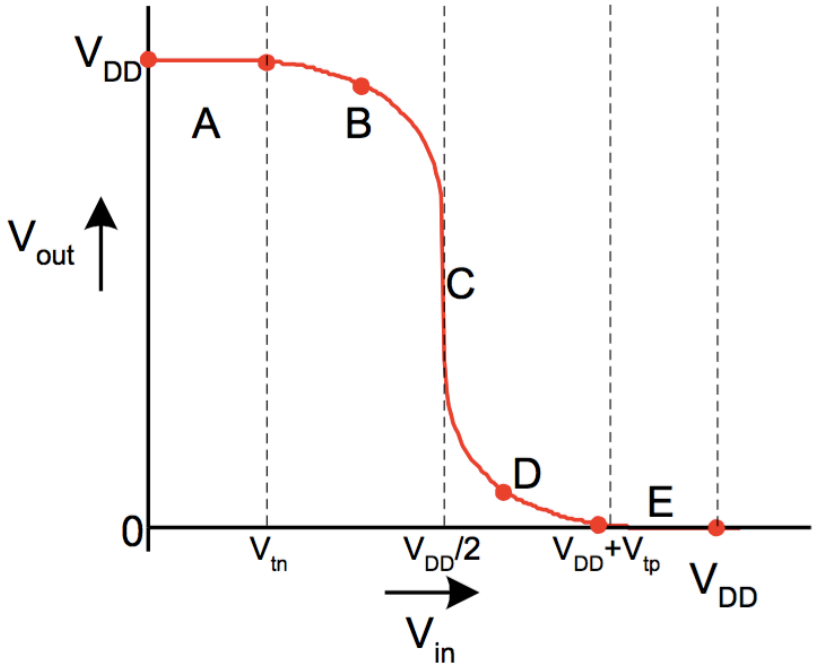
DC Transfer Curve

- Transcribe points onto V_{in} vs. V_{out} plot



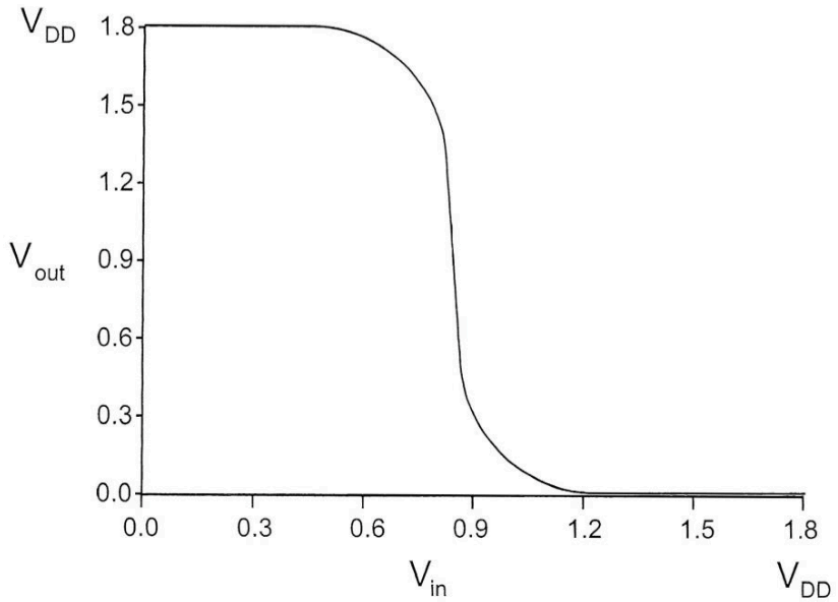
Transistor Operating Regions

	NMOS	PMOS
A		
B		
C		
D		
E		



CMOS Inverter Operation Summary

Region	Condition	p-device	n-device	Output
A	$0 \le V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \le V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \le V_{DD} - \lvert V_{tp} \rvert$	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \lvert V_{tp} \rvert$	cutoff	linear	$V_{out} = 0$



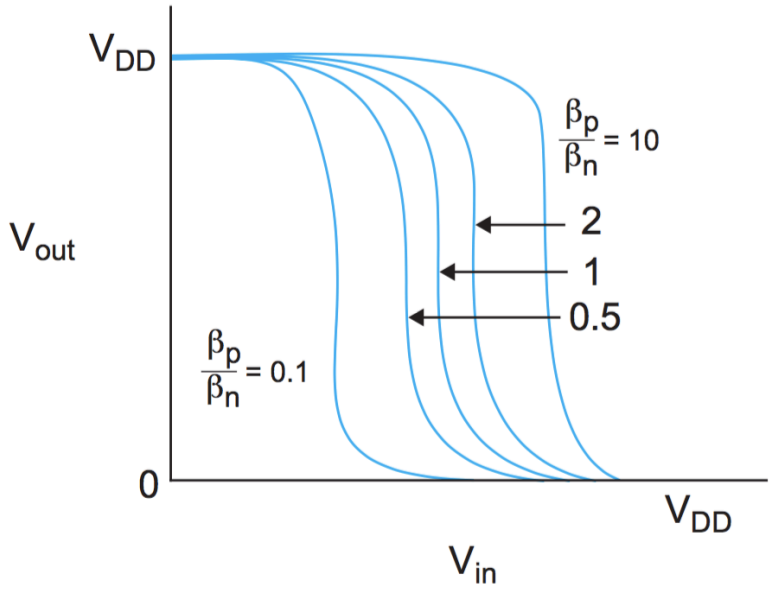
Beta Ratio Effect

- β ratio and parameters

$$\beta_p = \mu_p C_{ox} (W/L)_p$$

$$\beta_n = \mu_n C_{ox} (W/L)_n$$

$$\beta \text{ ratio} = \beta_p / \beta_n$$



- β ratio = 1 → largest noise margin
  - $\mu_n > \mu_p$, choose $(W/L)_p > (W/L)_n$ to make β ratio = 1
- β ratio > 1 → HI-skewed inverter, switching threshold > 0.5 V_{DD}
- β ratio < 1 → LO-skewed inverter, switching threshold < 0.5 V_{DD}

Noise Margin (I)

- The allowable noise voltage on the input that the output won't be corrupted

$$NM_L = V_{IL} - V_{OL}$$

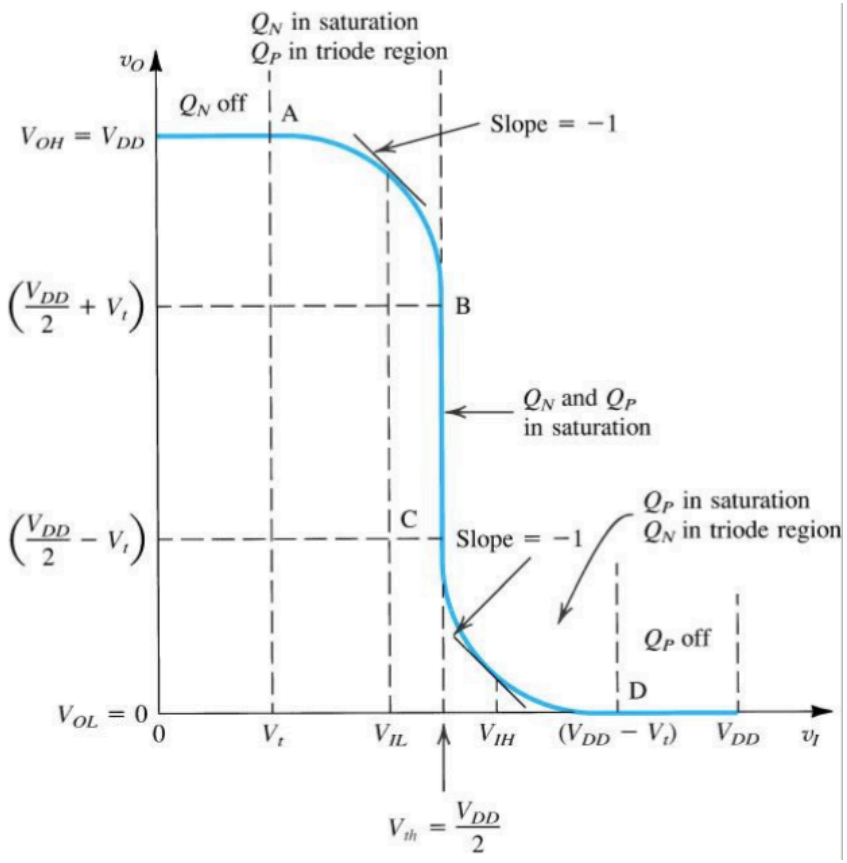
$$NM_H = V_{OH} - V_{IH}$$

V_{IH} = minimum HIGH input voltage

V_{IL} = maximum LOW input voltage

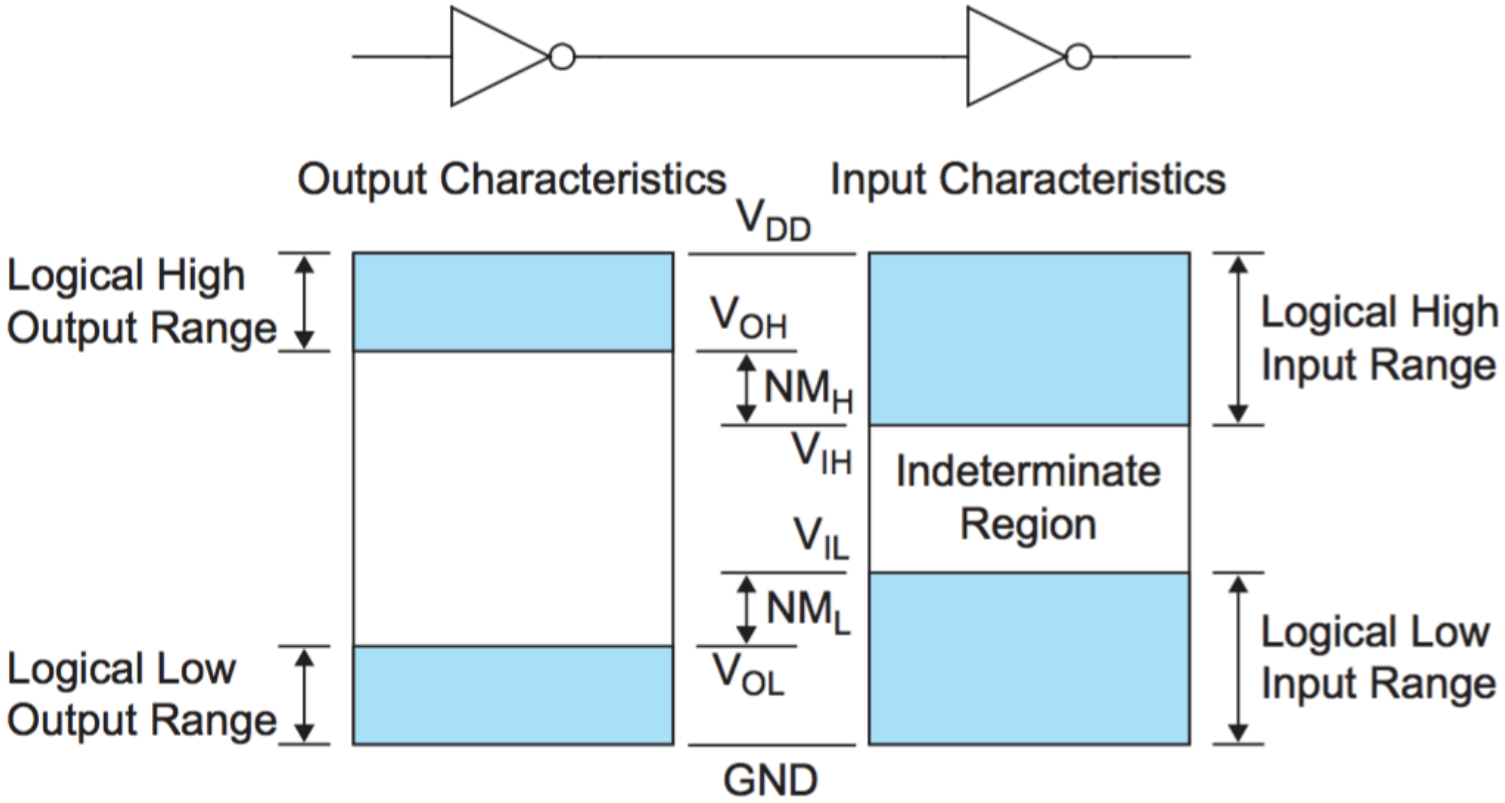
V_{OH} = minimum HIGH output voltage

V_{OL} = maximum LOW output voltage



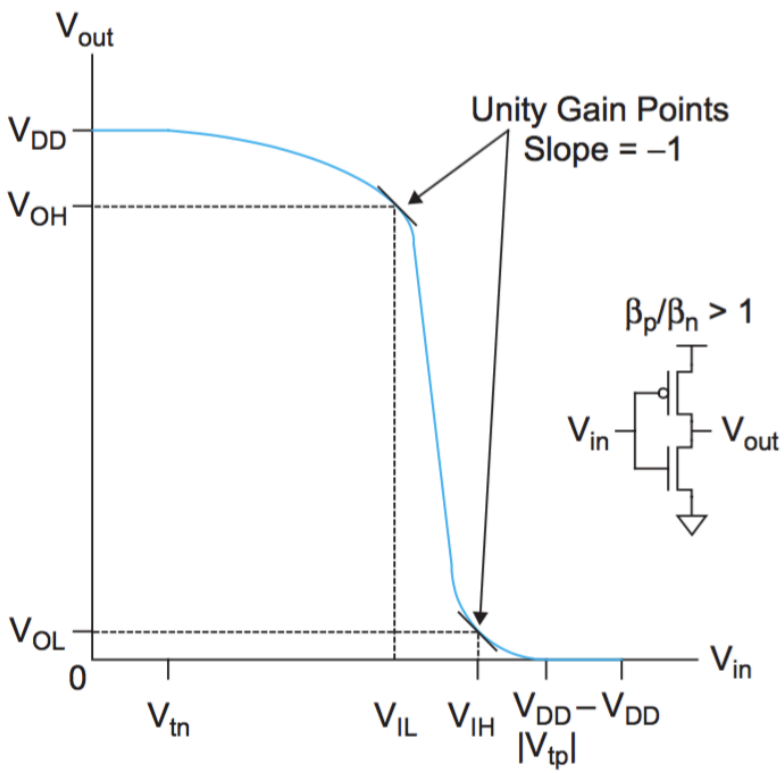
Noise Margin (II)

- Indeterminate region (*forbidden zone*)
  - $V_{IL} < V_{in} < V_{IH} \rightarrow V_{out}$ = unknown logic level



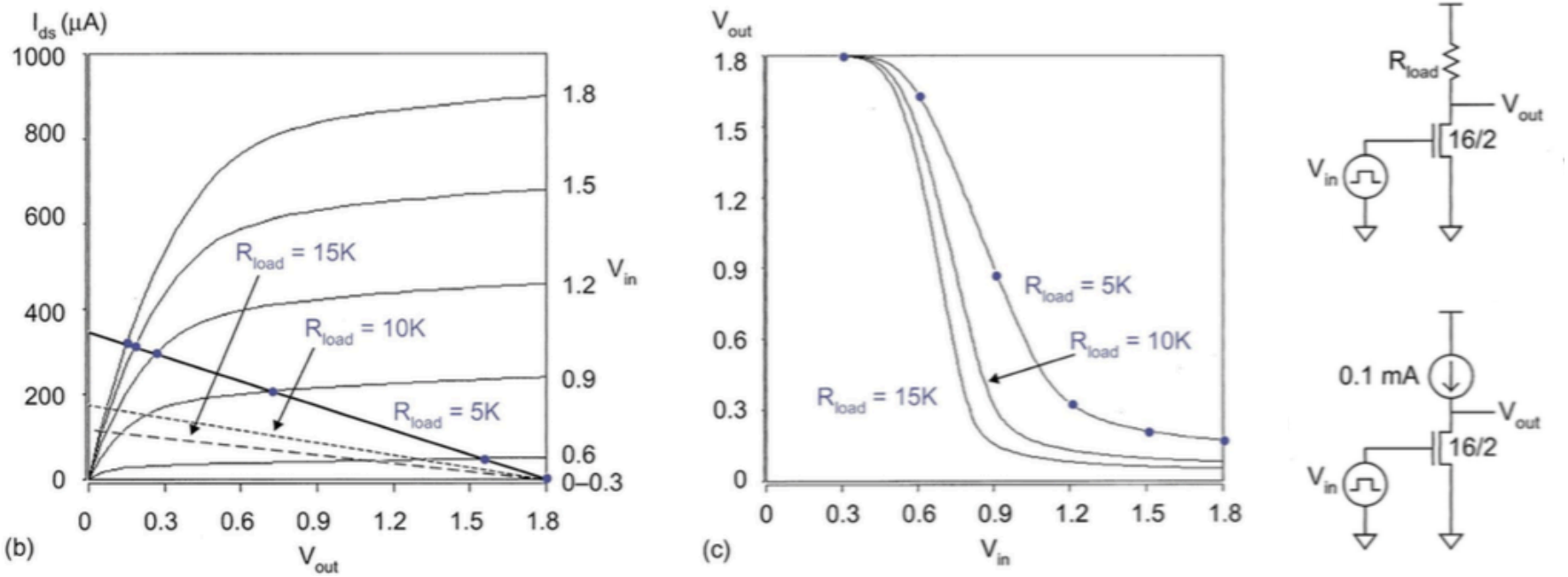
Beta Ratio and Noise Margin

- β ratio > 1
  - Switching threshold > 0.5 V_{DD}
  - VIH ↑ NMH ↓
  - VIL ↑ NML ↑
- β ratio < 1
  - Switching threshold < 0.5 V_{DD}
  - VIH ↓ NMH ↑
  - VIL ↓ NML ↓
- Noise tend to scale with V_{DD}
  - As VDD ↓
    smaller NM is acceptable



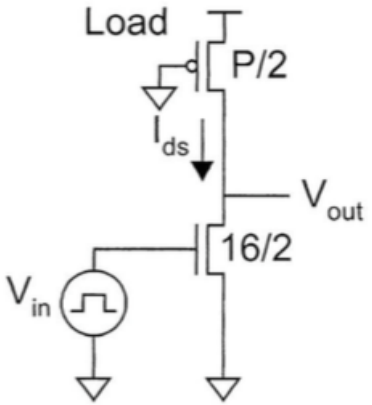
Ratioed Inverter Transfer Function (I)

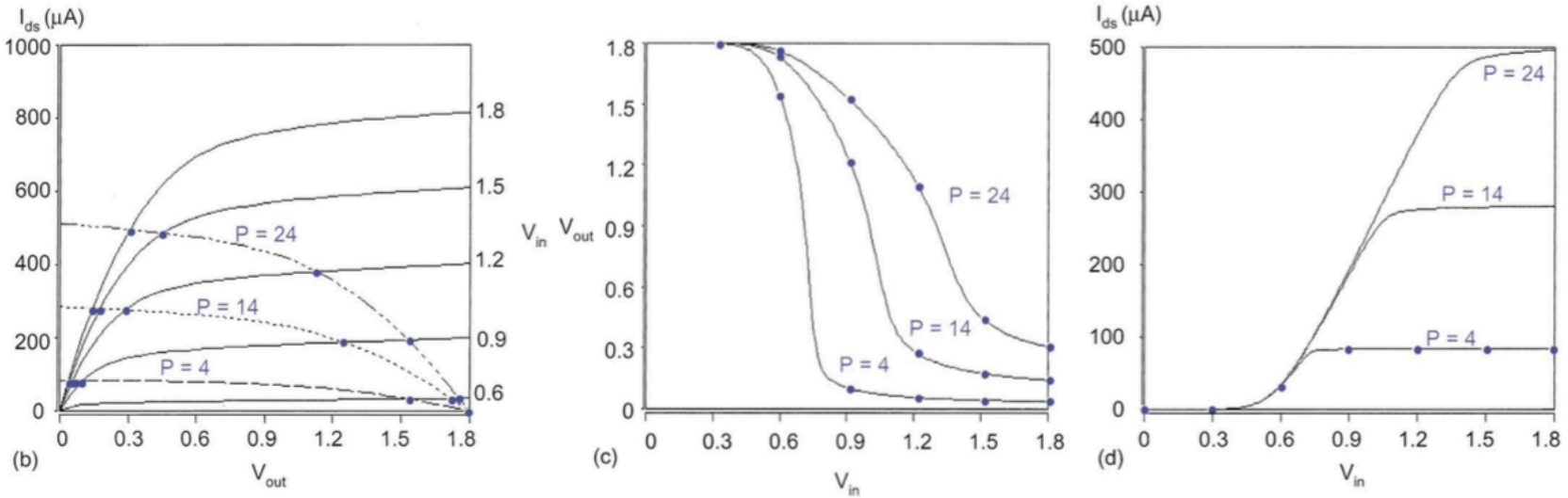
- NMOS inverters with resistive or constant current-source load
  - Transfer function depends on the ratio of pull-down to the pull-up transistor (static load)



Ratioed Inverter Transfer Function (II)

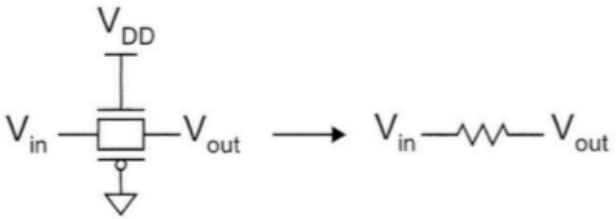
- NMOS inverters with turn-ON PMOS as load
  - Turn-ON PMOS is made by a depletion mode NMOS in pure NMOS process
  - Dissipating static power when V_{out} = LOW
  - Poor NM but smaller area and input capacitance loading

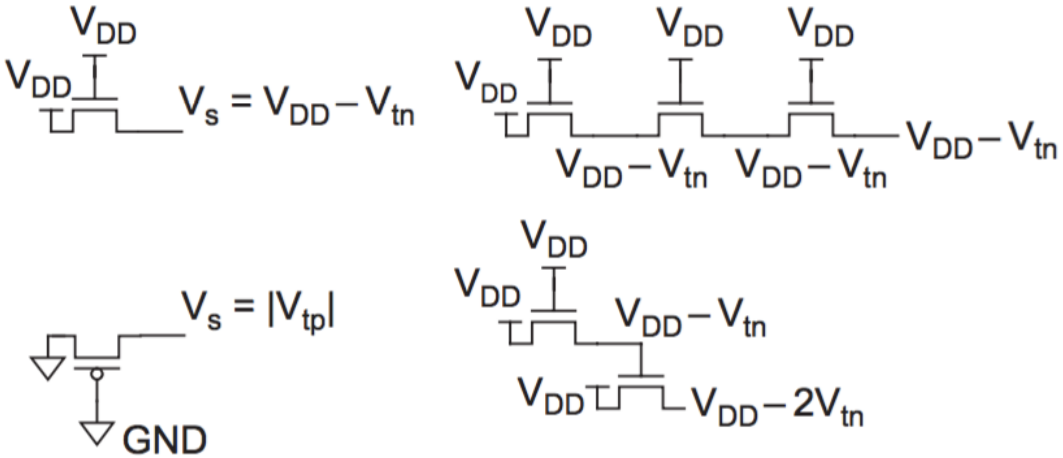


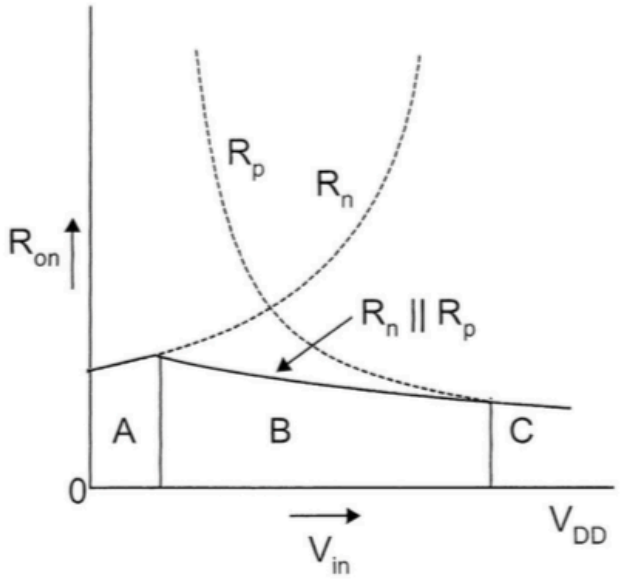


Pass Transistor DC Characteristics

- Due to V_{th}
  - NMOS cannot pass "1"
  - PMOS cannot pass "0"
  - Need to consider **body effect**
- ON-resistance depends on V_{in}
  - Need to boost gate voltage with small V_{DD}

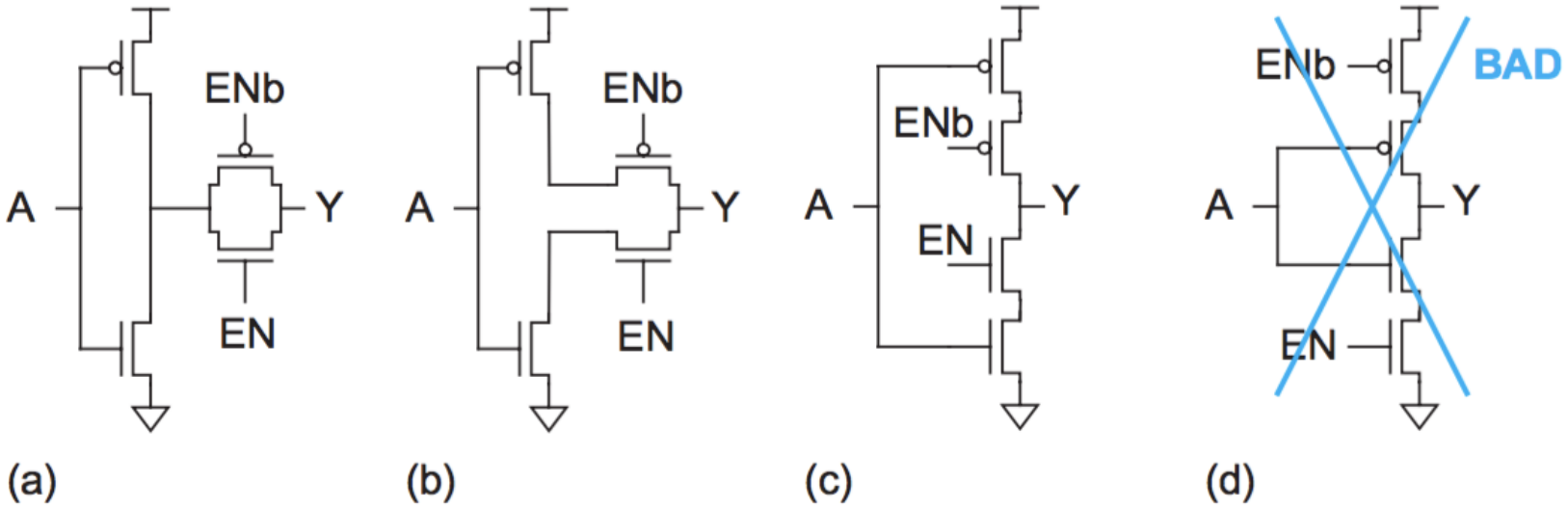






Tri-state Inverter

- Inverter + transmission gate
  - Approximately half the speed of CMOS inverter for the same n and p device sizes
  - The structure in (d) suffer from A's toggling in tristate
  - Need to consider **body effect**



Outline

- Introduction
- Ideal I-V characteristics
- Nonideal Effects
- C-V characteristics
- DC transfer characteristics
- **Switch-level RC delay models**

Effective Resistance *R*

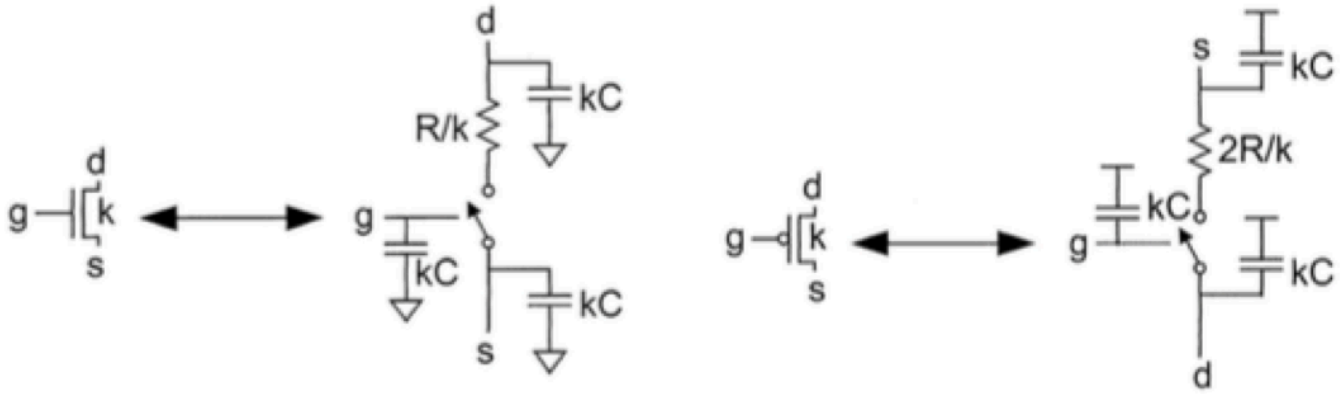
- ***R*: effective resistance** of unit NMOS (W_{min} and L_{min})
  - Unit PMOS has ***2R*** (or ***3R***) due to lower mobility
  - **In linear region**, inversely proportional to W/L and V_{gs}

$$R = \left(\frac{\partial I_{ds}}{\partial V_{ds}} \right)^{-1} = \frac{1}{\beta \left(V_{gs} - V_t \right)} = \frac{1}{\mu C_{ox}} \frac{L}{W} \frac{1}{\left(V_{gs} - V_t \right)}$$

- ***C*: gate capacitance** of unit transistor (NMOS and PMOS)
  - Proportional to gate area W*L
- ***C*: S/D junction capacitance** of unit transistor
  - Proportional to gate width W

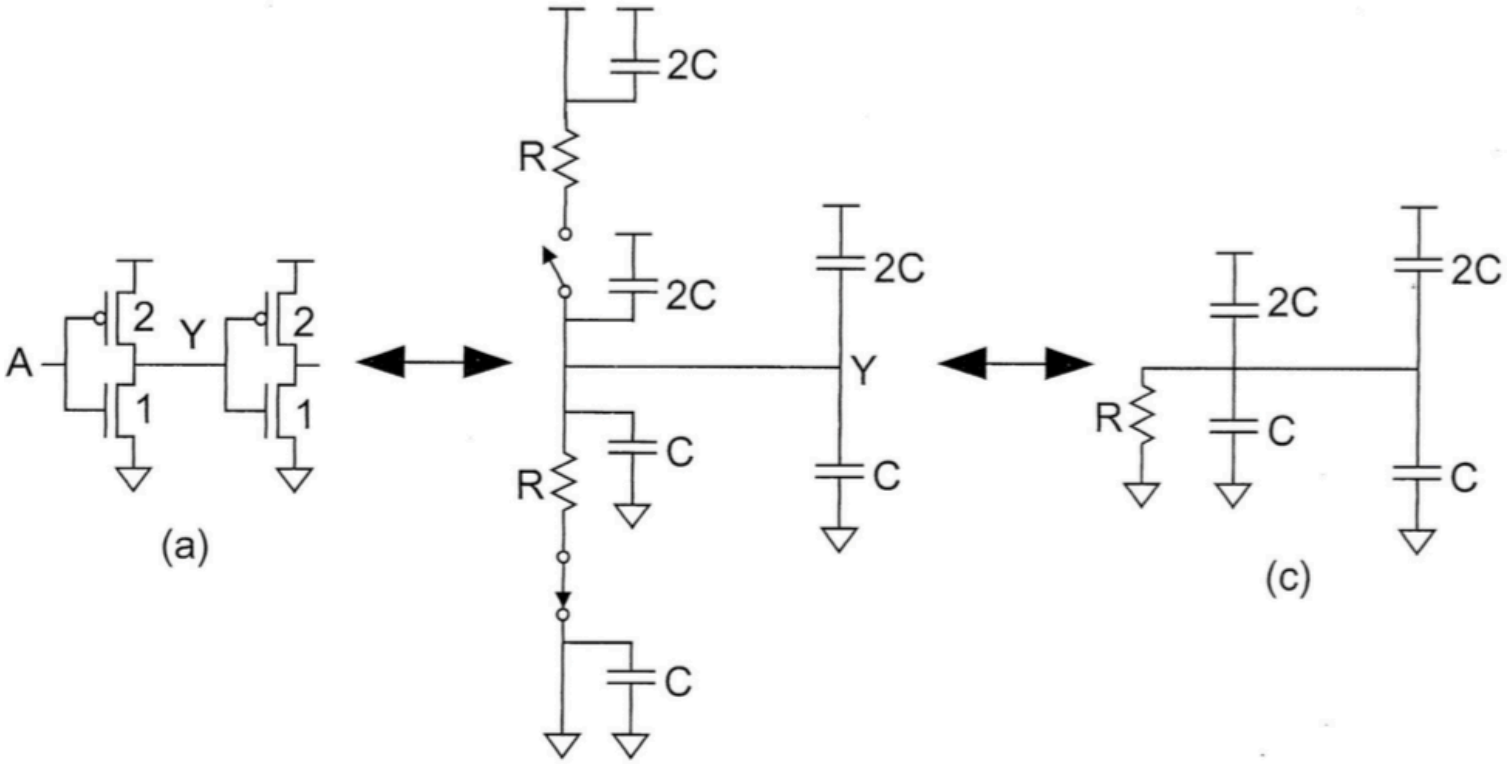
RC Circuit Model

- NMOS of k times unit width has resistance of ***R/k***, gate capacitance of ***kC***, and S/D capacitance of ***kC***
  - NMOS parasitic capacitance referenced to GND (p-sub)
- PMOS of k times unit width has resistance of ***2R/k***, gate capacitance of ***kC***, and S/D capacitance of ***kC***
  - PMOS parasitic capacitance referenced to V_{DD} (n-well)



Inverter Propagation Delay

- Fanout-of-1 inverter
  - Choose PMOS width to be 2x~3x of NMOS width
  - $t_{pd} = R(6C) = 6RC$



R of Transmission Gate

- Parallel combination of NMOS and PMOS
  - Depend on signal to pass
  - PMOS pass 0 weakly with larger resistance ***4R***
  - NMOS pass 1 weakly with larger resistance ***2R***
  - Usually the same size for NMOS and PMOS
  - Increase size → R ↓ C ↑ → need to check the trade-off