Introduction to Semiconductor Manufacturing Technology

Chapter 1, Introduction

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Objective

After taking this course, you will able to

- Use common semiconductor terminology
- Describe a basic IC fabrication sequence
- Briefly explain each process step
- Relate your job or products to semiconductor manufacturing process

Topics

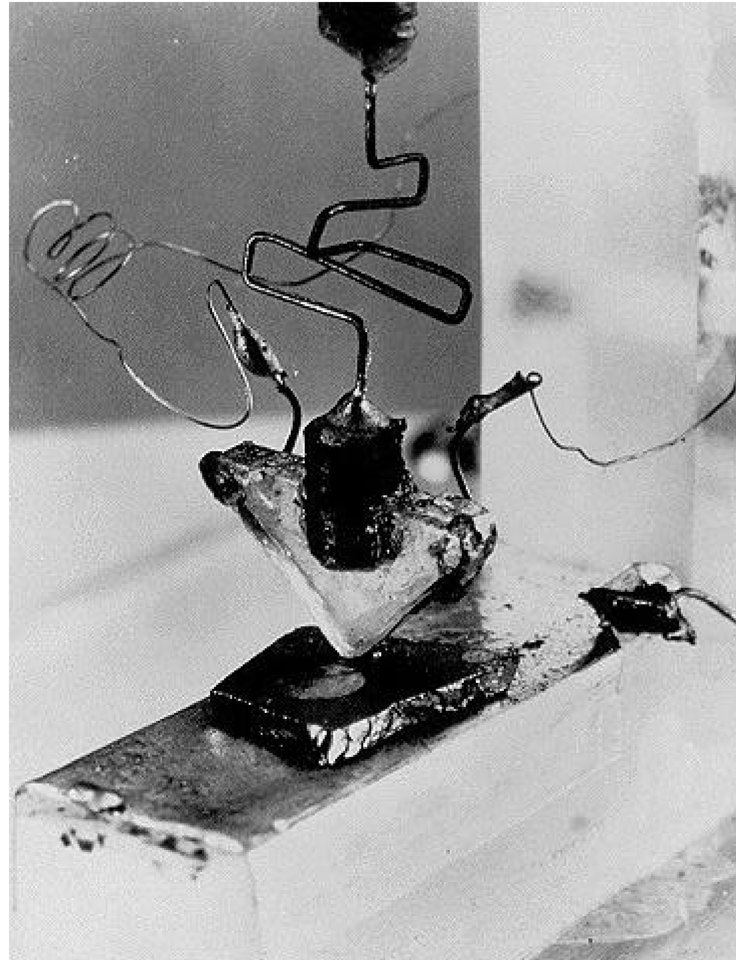
- Introduction
- IC Device and Design
- Semiconductor Manufacturing Processes
- Future Trends

Introduction

- First Transistor, AT&T Bell Labs, 1947
- First Single Crystal Germanium, 1952
- First Single Crystal Silicon, 1954
- First IC device, TI, 1958
- First IC product, Fairchild Camera, 1961

First Transistor, Bell Lab, 1947

Photo courtesy:
AT&T Archive



First Transistor and Its Inventors

John Bardeen, William Shockley and Walter Brattain

Photo courtesy: Lucent Technologies Inc.

First IC Device Made by Jack Kilby of Texas Instrument in 1958

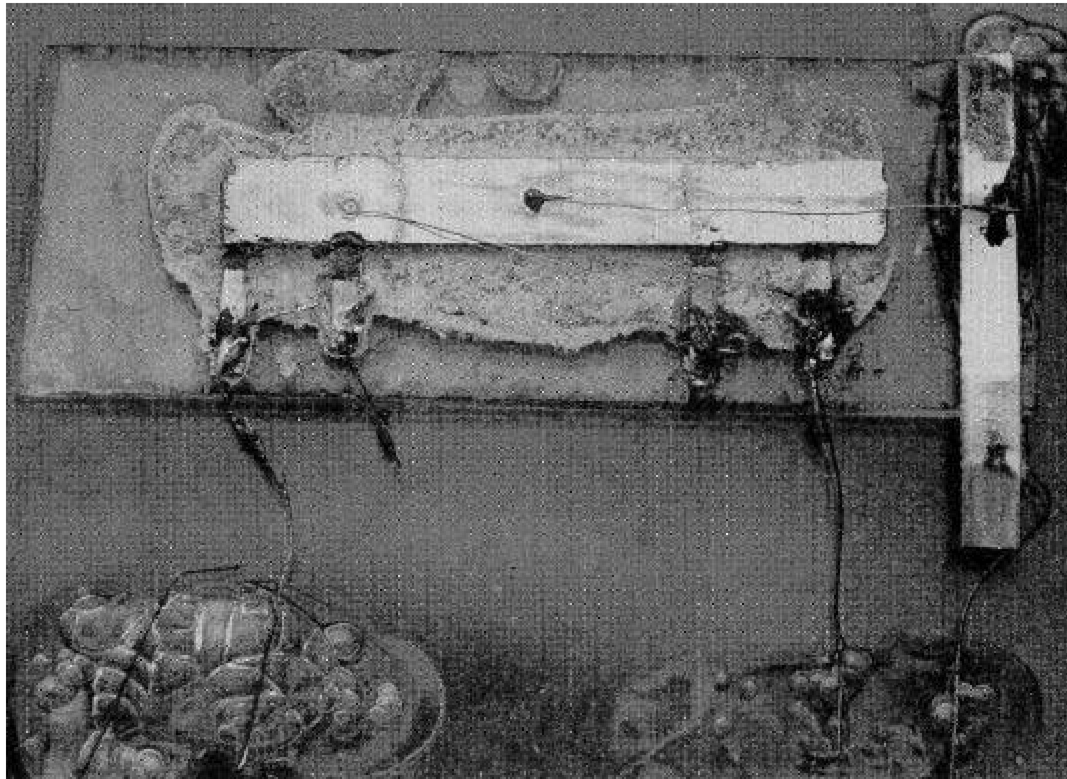


Photo courtesy: Texas Instruments

First Silicon IC Chip Made by Robert Noyce of Fairchild Camera in 1961

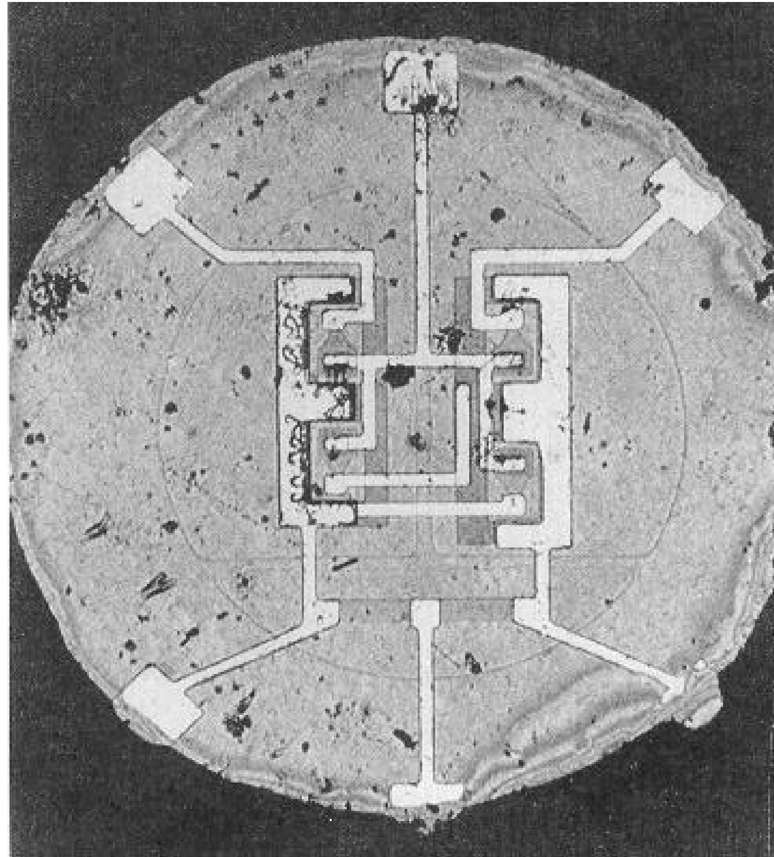
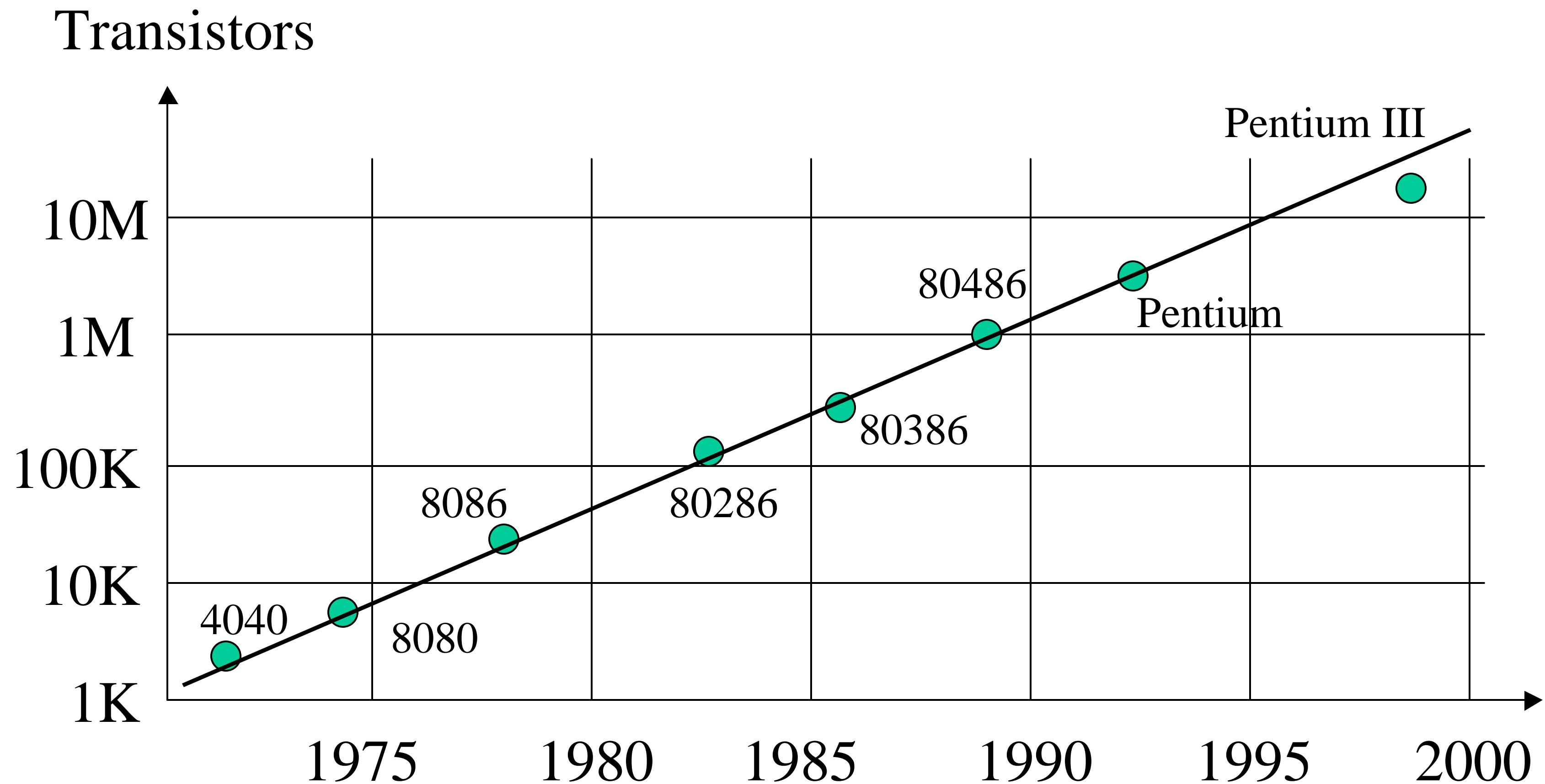


Photo courtesy: Fairchild Semiconductor International

Moore's Law

- Intel co-founder Gorden Moore notice in 1964
- Number of transistors doubled ever 12 months while price keeping unchanged
- Slowed down in the 1980s to every 18 months
- Amazingly still correct, likely to keep until 2010.

Moore's Law, Intel's Version



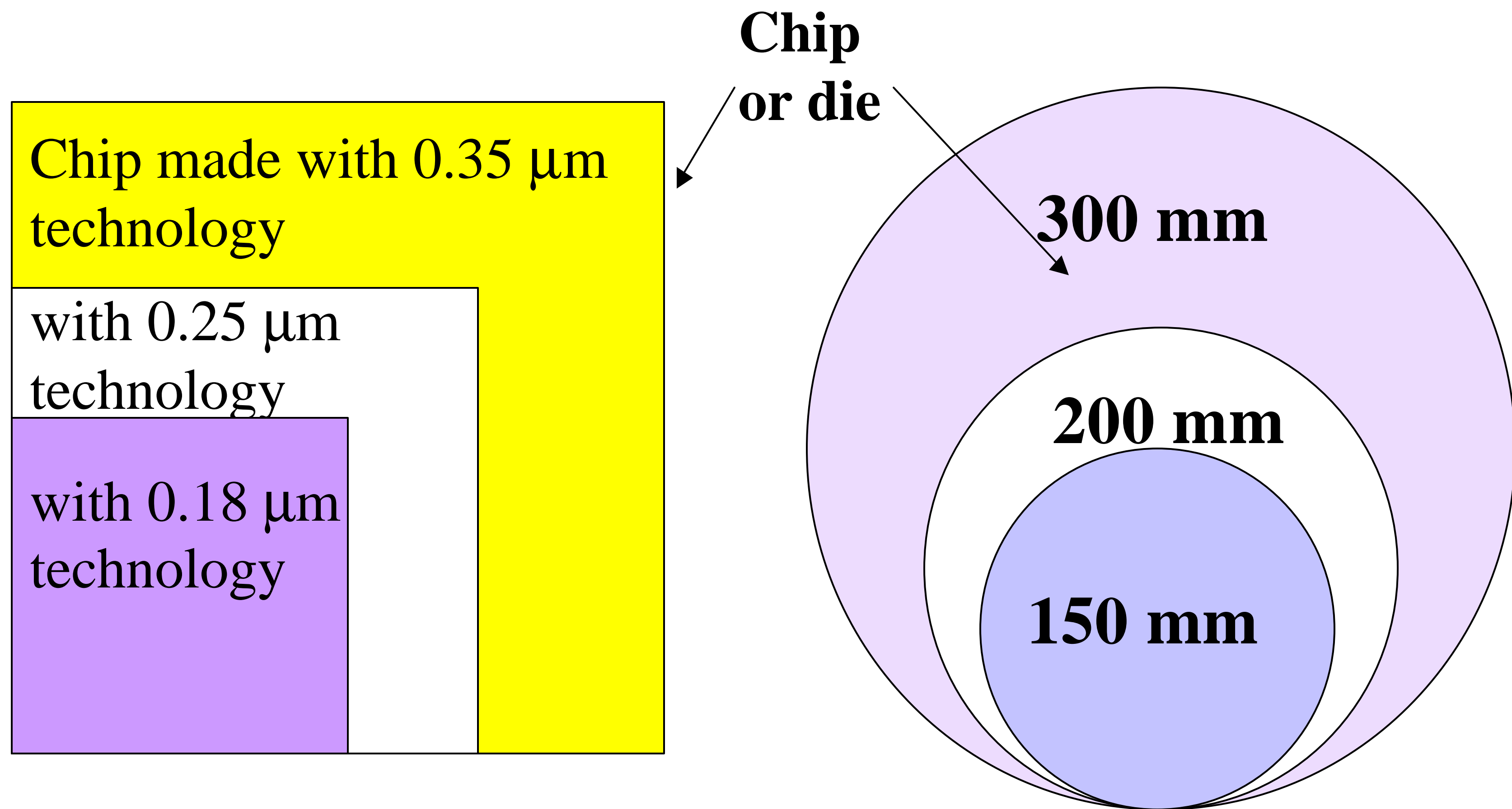
IC Scales

Integration level	Abbreviation	Number of devices on a chip
Small Scale Integration	SSI	2 to 50
Medium Scale Integration	MSI	50 to 5,000
Large Scale Integration	LSI	5,000 to 100,000
Very Large Scale Integration	VLSI	100,000 to 10,000,000
Ultra Large Scale Integration	ULSI	10,000,000 to 1,000,000,000
Super Large Scale Integration	SLSI	over 1,000,000,000

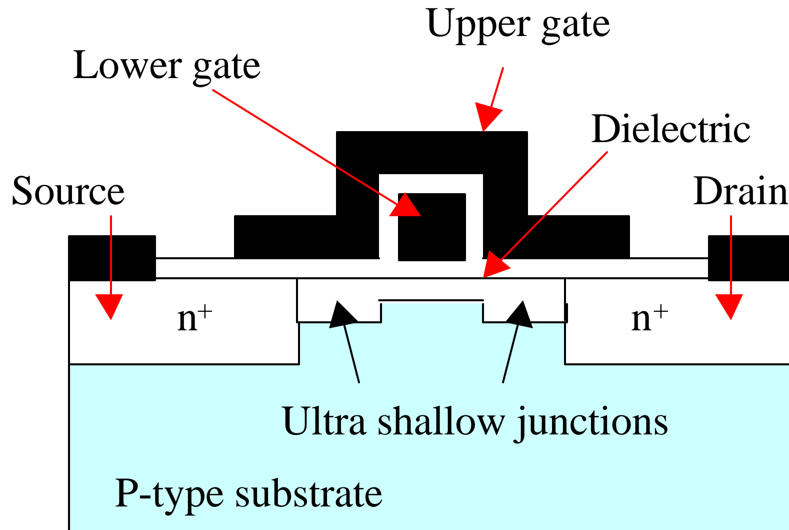
Road Map Semiconductor Industry

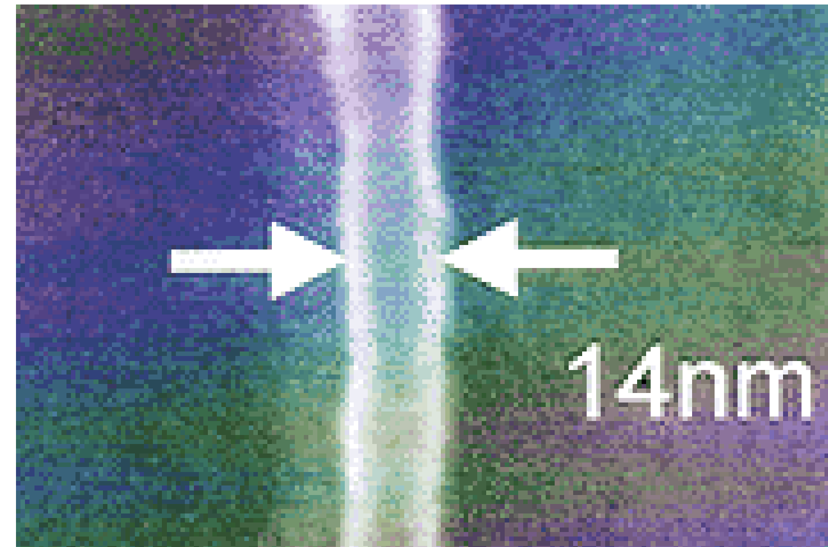
	1995	1997	1999	2001	2004	2007
Minimum feature size (μm)	**0.35**	**0.25**	**0.18**	**0.13**	**0.10**	**0.07**
DRAM Bits/chip Cost/bits @ volume (millicents)	 64 M 0.017	 256 M 0.007	 1 G 0.003	 4 G 0.001	 16 G 0.0005	 64 G 0.0002
Microprocessor Transistors/cm^2 Cost/Transistor @ volume (millicents)	 4 M 1	 7 M 0.5	 13 M 0.2	 25 M 0.1	 50 M 0.05	 90 M 0.02
ASIC Transistors/cm^2 Cost/Transistor @ volume (millicents)	 2 M 0.3	 4 M 0.1	 7 M 0.05	 13 M 0.03	 25 M 0.02	 40 M 0.01
Wafer size (mm)	200	200	200 - 300	300	300	300 – 400 (?)

Feature Size and Wafer Size



Smallest Known Transistor Made by NEC in 1997



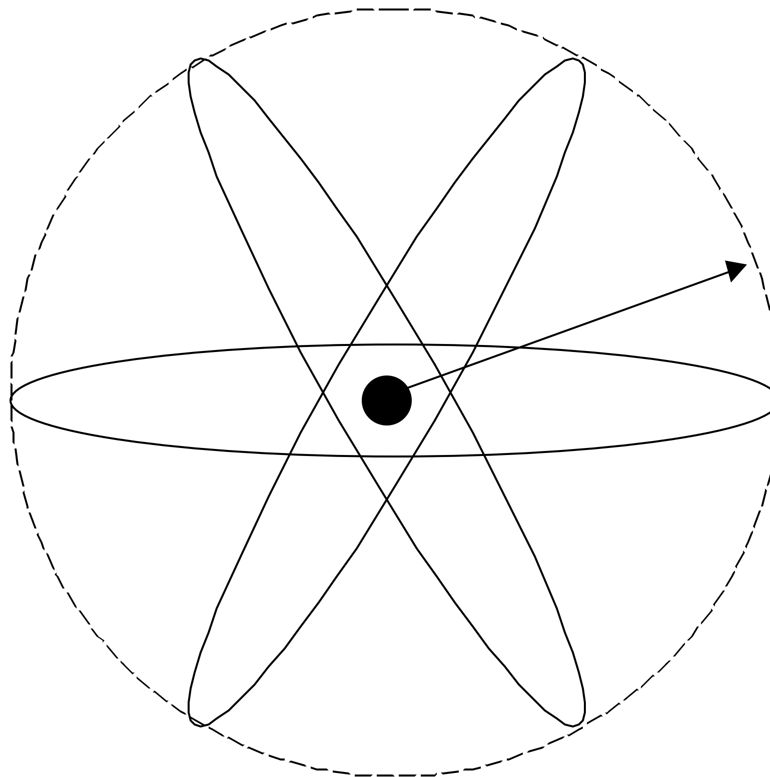


0.014 micron lower gate width

Photo courtesy: NEC Corporation

Limit of the IC Geometry

Size of the atom



Limit of the IC device

- Atom size: several Å
- Need some atoms to form a device
- Likely the final limit is around 100 Å or 0.01 micron.
- About 30 silicon atoms

IC Design: First IC

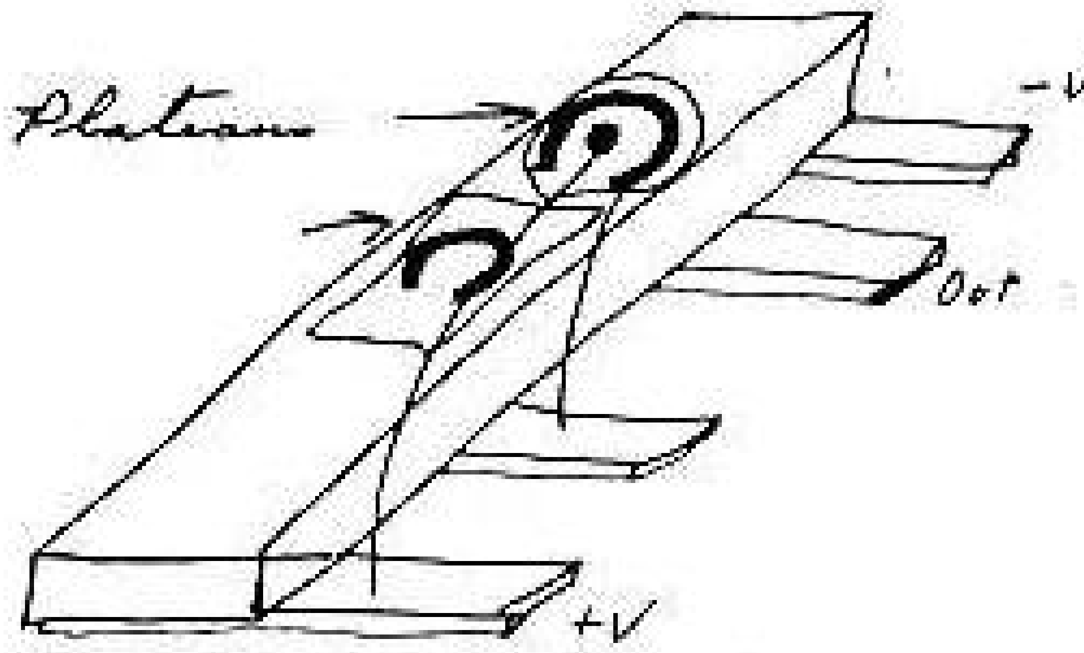
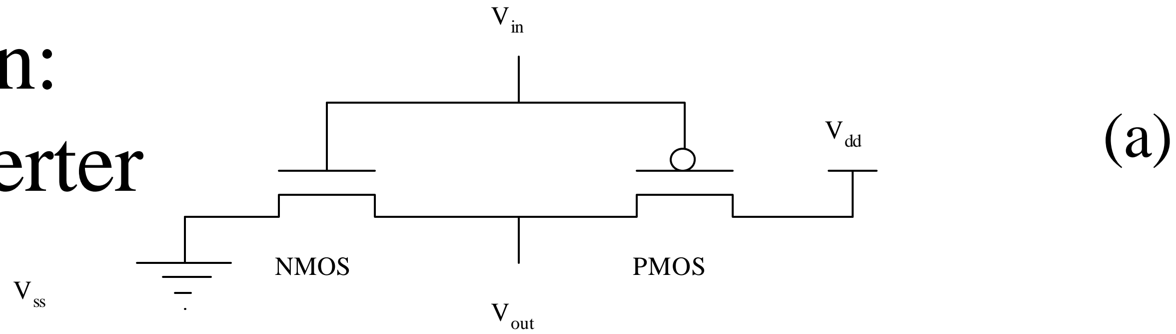


Photo courtesy: Texas Instruments

IC Design: CMOS Inverter

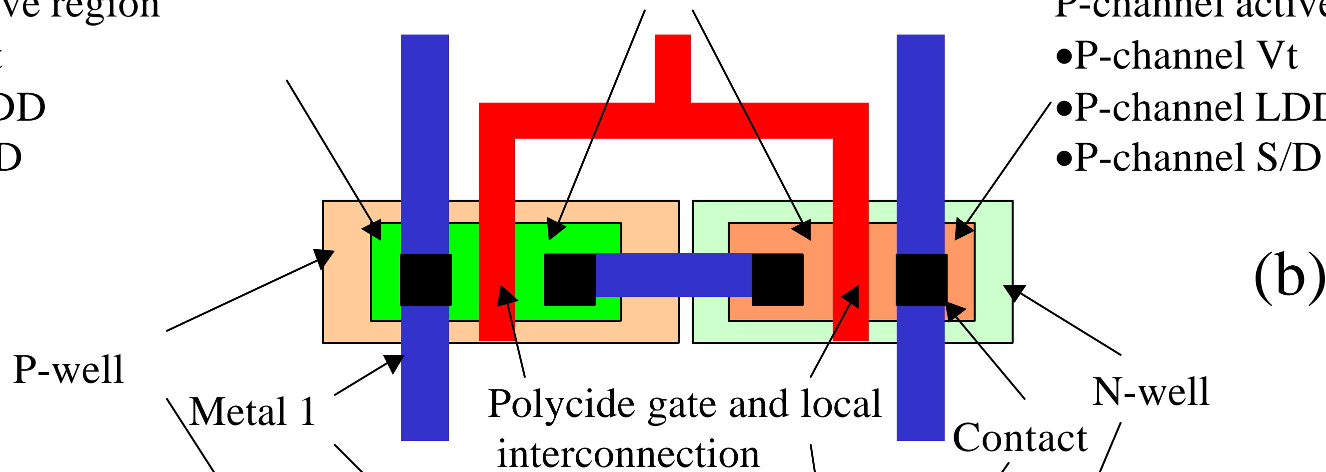


(a)

Shallow trench isolation (STI)

N-channel active region
- N-channel Vt
- N-channel LDD
- N-channel S/D

P-channel active region
- P-channel Vt
- P-channel LDD
- P-channel S/D



(b)

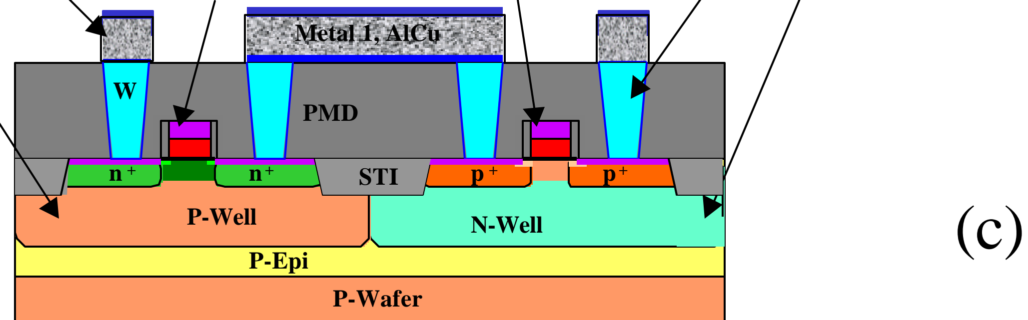
P-well

Metal 1

Polycide gate and local interconnection

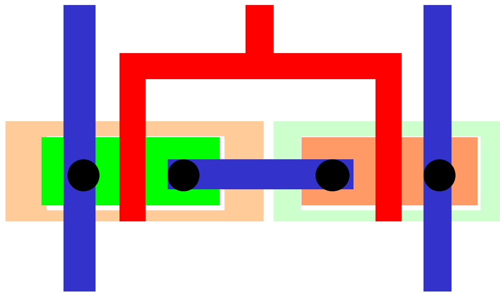
Contact

N-well



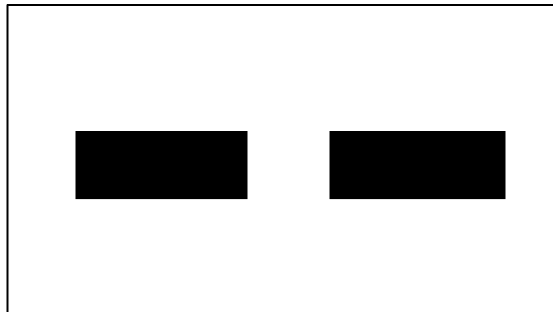
(c)

IC Design: Layout and Masks of CMOS Inverter


CMOS inverter layout

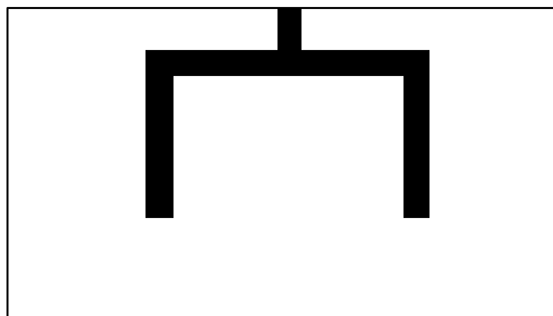
Mask 1, N-well

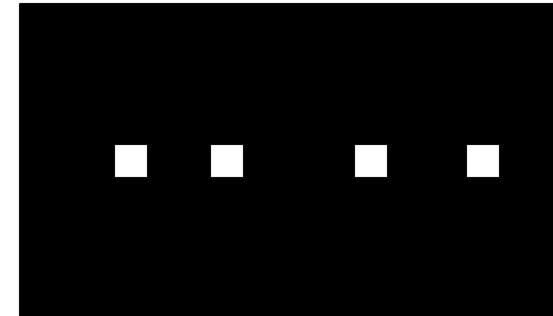
Mask 2, P-well

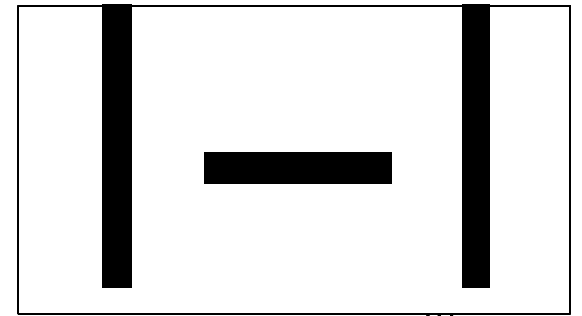

Mask 3, shallow trench isolation

Mask 4, 7, 9, N-Vt, LDD, S/D

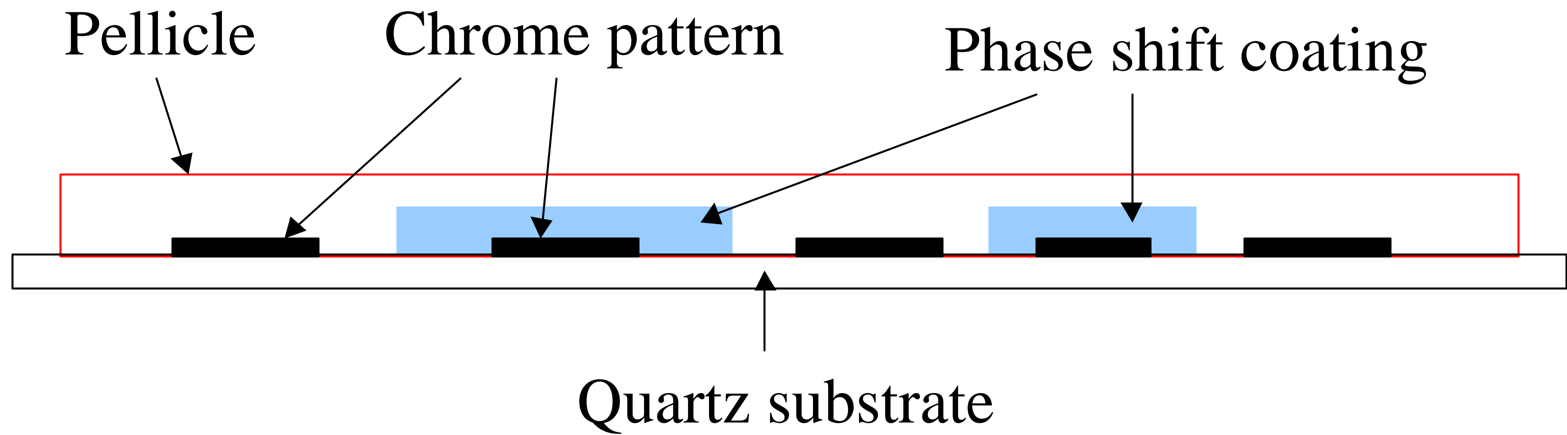
Mask 5, 8, 10, P-Vt, LDD, S/D


Mask 6, gate/local interconnection

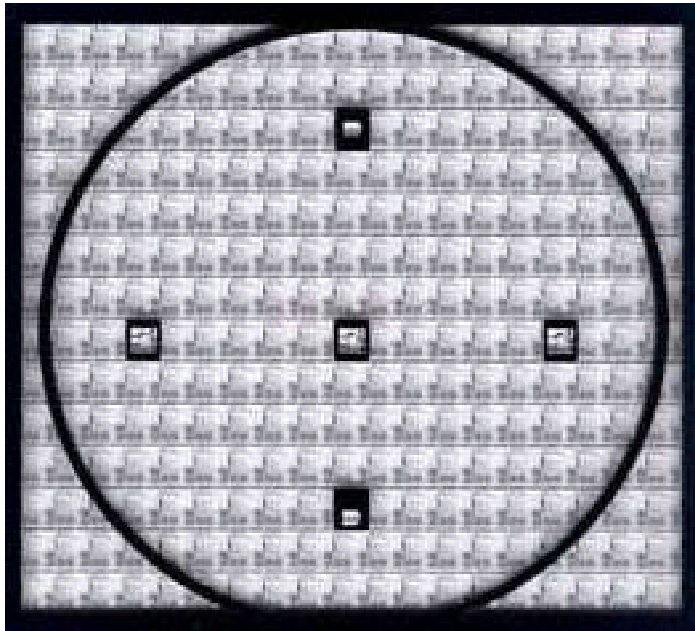

Mask 11, contact


Mask 12, metal 1

Mask/Reticle



A Mast and a Reticle



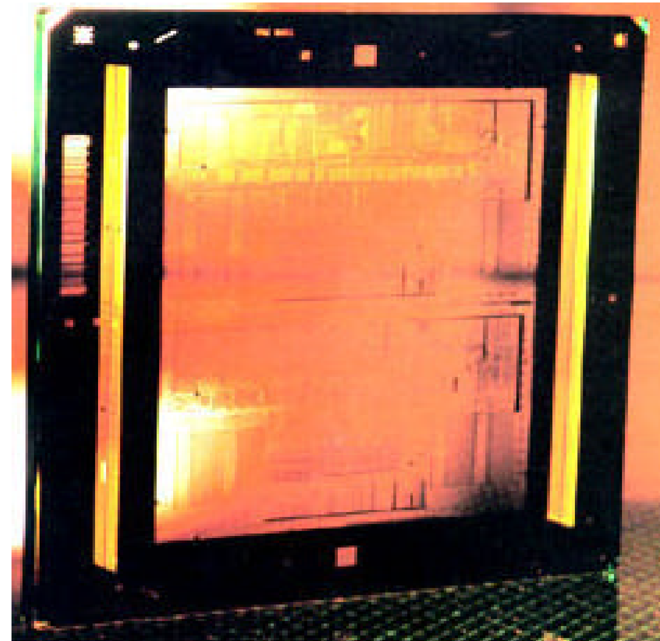
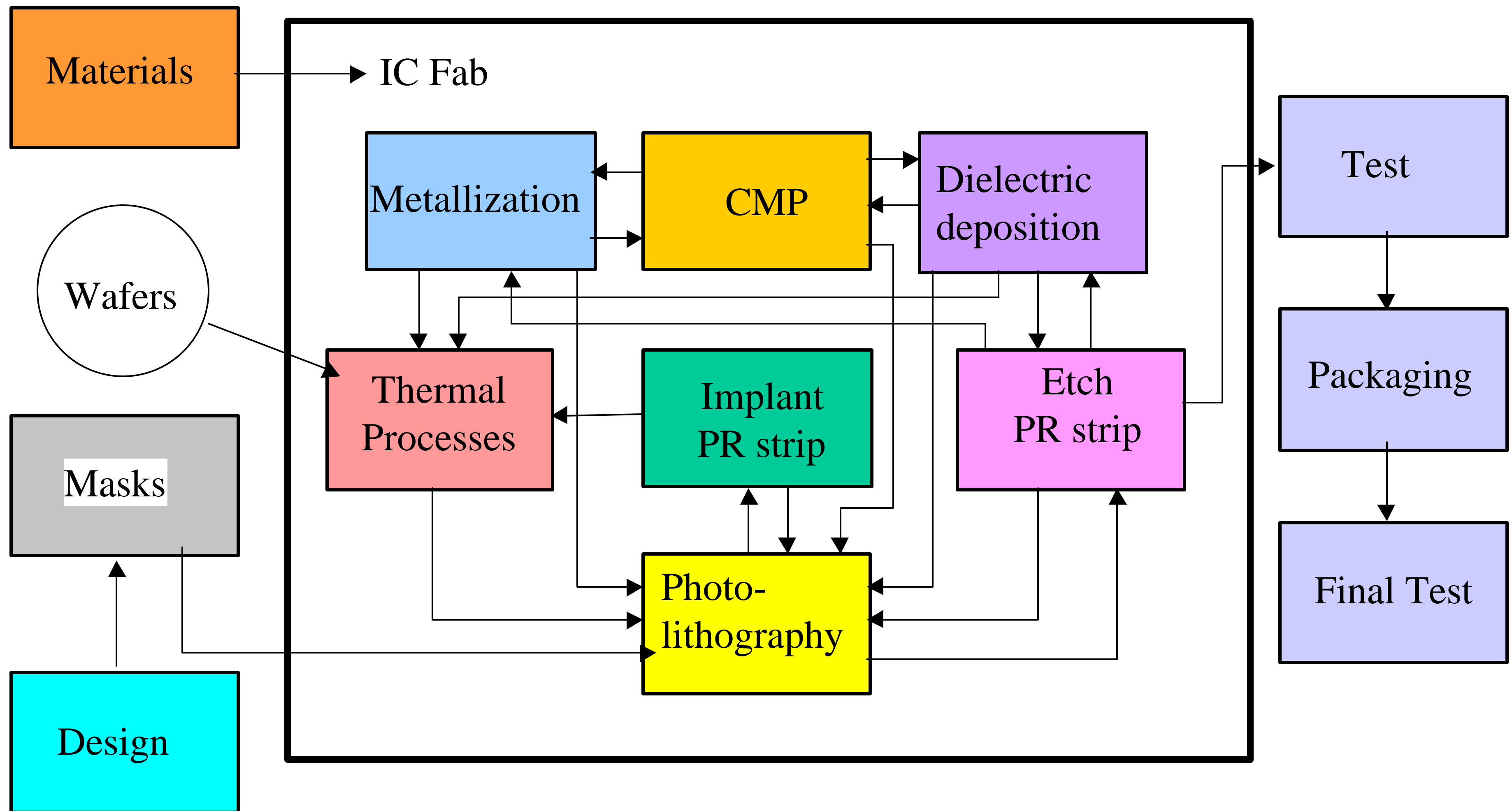


Photo courtesy: SGS Thompson

Wafer Process Flow



Chapter 2
Introduction of IC Fabrication

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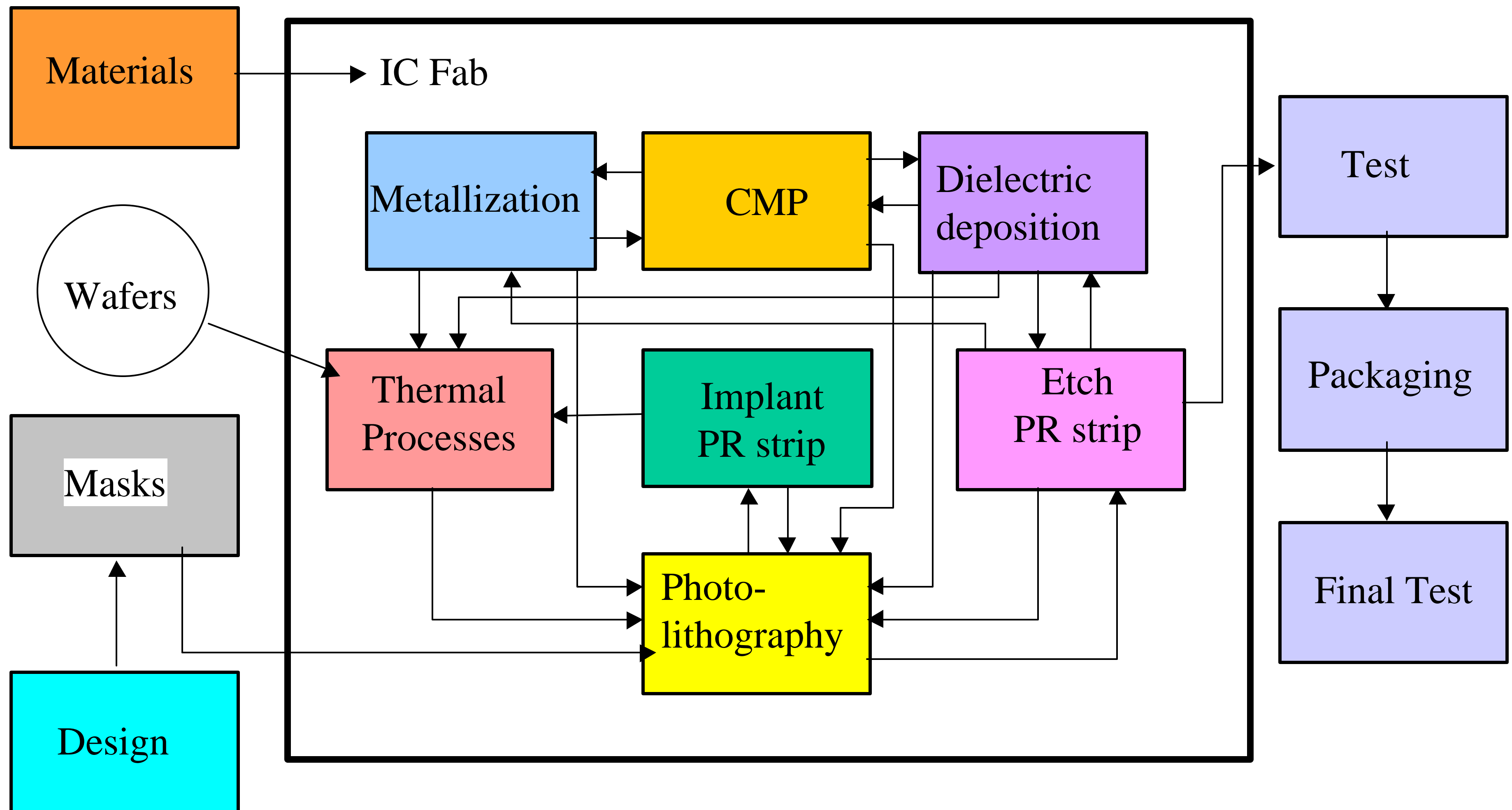
Objectives

- Define yield and explain its importance
- Describe the basic structure of a cleanroom.
- Explain the importance of cleanroom protocols
- List four basic operations of IC processing
- Name at least six process bays in an IC fab
- Explain the purposes of chip packaging
- Describe the standard wire bonding and flip-chip bump bonding processes

Wafer Process Flow



Fab Cost

- Fab cost is very high, > $1B for 8” fab
- Clean room
- Equipment, >$1M per tool
- Materials, high purity, ultra high purity
- Facilities
- People, training and pay

Wafer Yield

$$Y_W = \frac{Wafers_{good}}{Wafers_{total}}$$

Die Yield

$$Y_D = \frac{Dies_{good}}{Dies_{total}}$$

Packaging Yield

$$Y_C = \frac{Chips_{good}}{Chips_{total}}$$

Overall Yield

$$Y_T = Y_W \times Y_D \times Y_C$$

Overall Yield determines whether a fab is making profit or losing money

How Does Fab Make Money

- Cost:
  - Wafer (8”): ~$150/wafer*
  - Processing: ~$200 (1$/wafer, 200 process steps)
  - Packing: ~$1/chip
- Sale:
  - ~100 chips/wafer
  - ~$50/chip (low-end microprocessor in 2000)

*Cost of wafer and price of chip are changing daily, numbers are choosing randomly based on general information.

How Does a Fab Make (*Loss*) Money

Cost:

- **100% yield: 150+200+100 = $450/wafer**
- 50% yield: 150+200+50 = $400/wafer
- *0% yield: 150+200 = $350/wafer*

Sale:

- **100% yield: 100´50 = $5,000/wafer**
- 50% yield: 50×50 = $2,500/wafer
- *0% yield: 0 ´50 = $0.00/wafer*

Profit Margin:

- **100% yield: 5000 - 450 = $4550/wafer**
- 50% yield : 2500 - 400 = $2100/wafer
- *0% yield : 0 - 350 = - $350/wafer*

Throughput

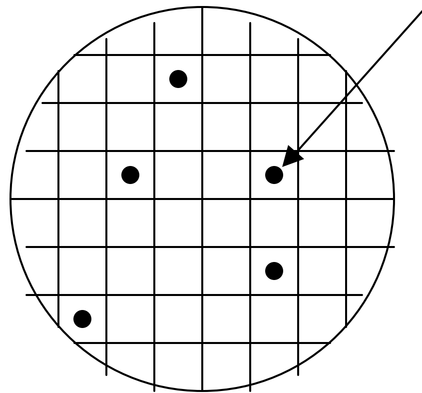
- Number of wafers able to process
  - Fab: wafers/month (typically 10,000)
  - Tool: wafers/hour (typically 60)
- At high yield, high throughput brought

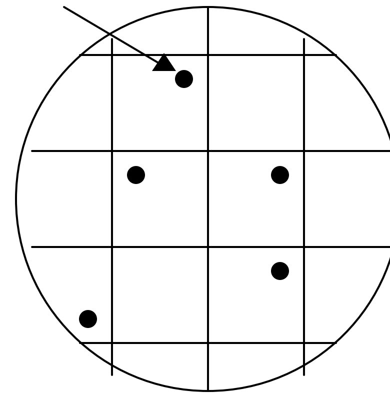
Defects and Yield

$$Y \propto \frac{1}{(1+DA)^n}$$

Yield and Die Size

Killer Defects





$Y = 28/32 = 87.5\%$ $Y = 2/6 = 33.3\%$

Illustration of a Production Wafer

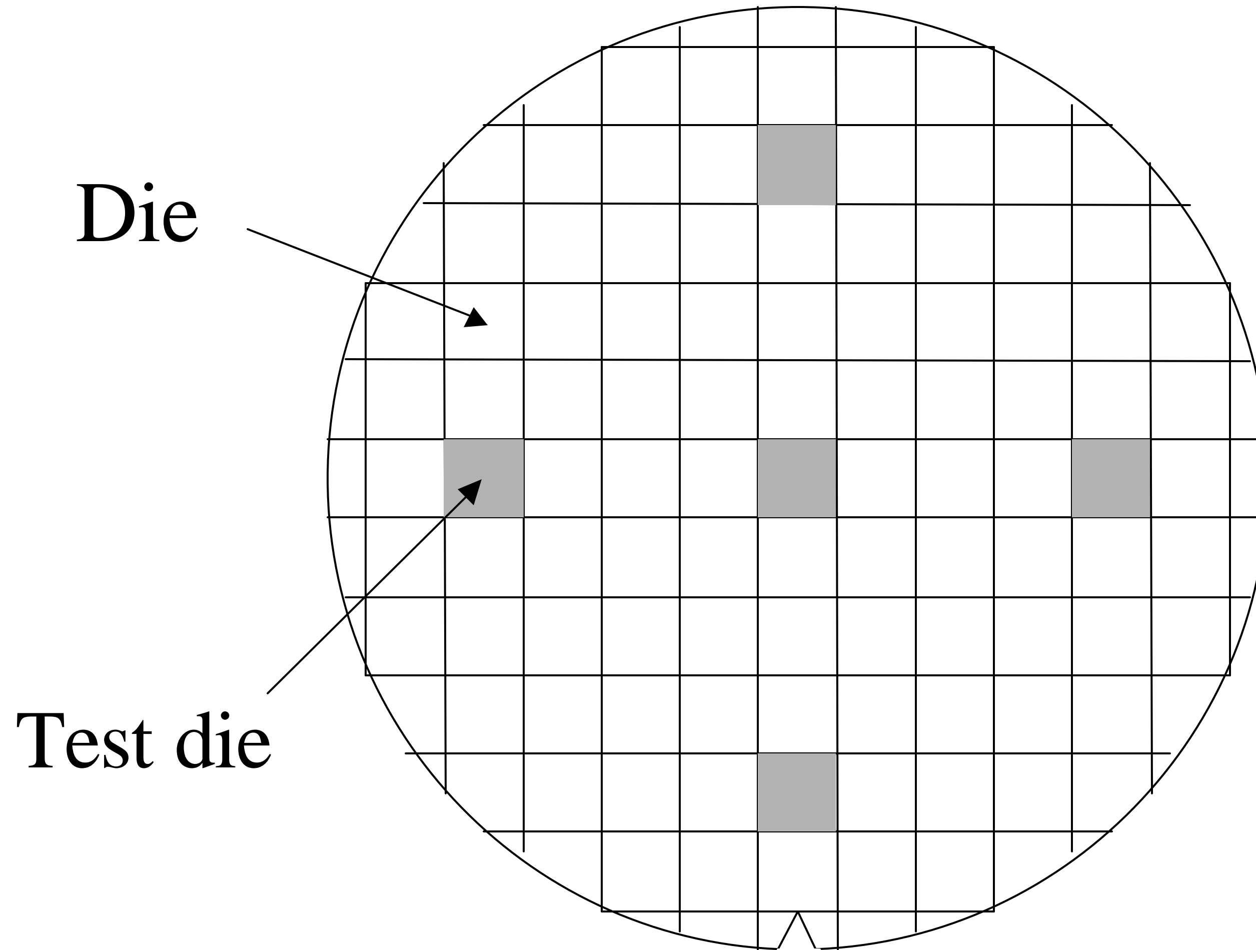
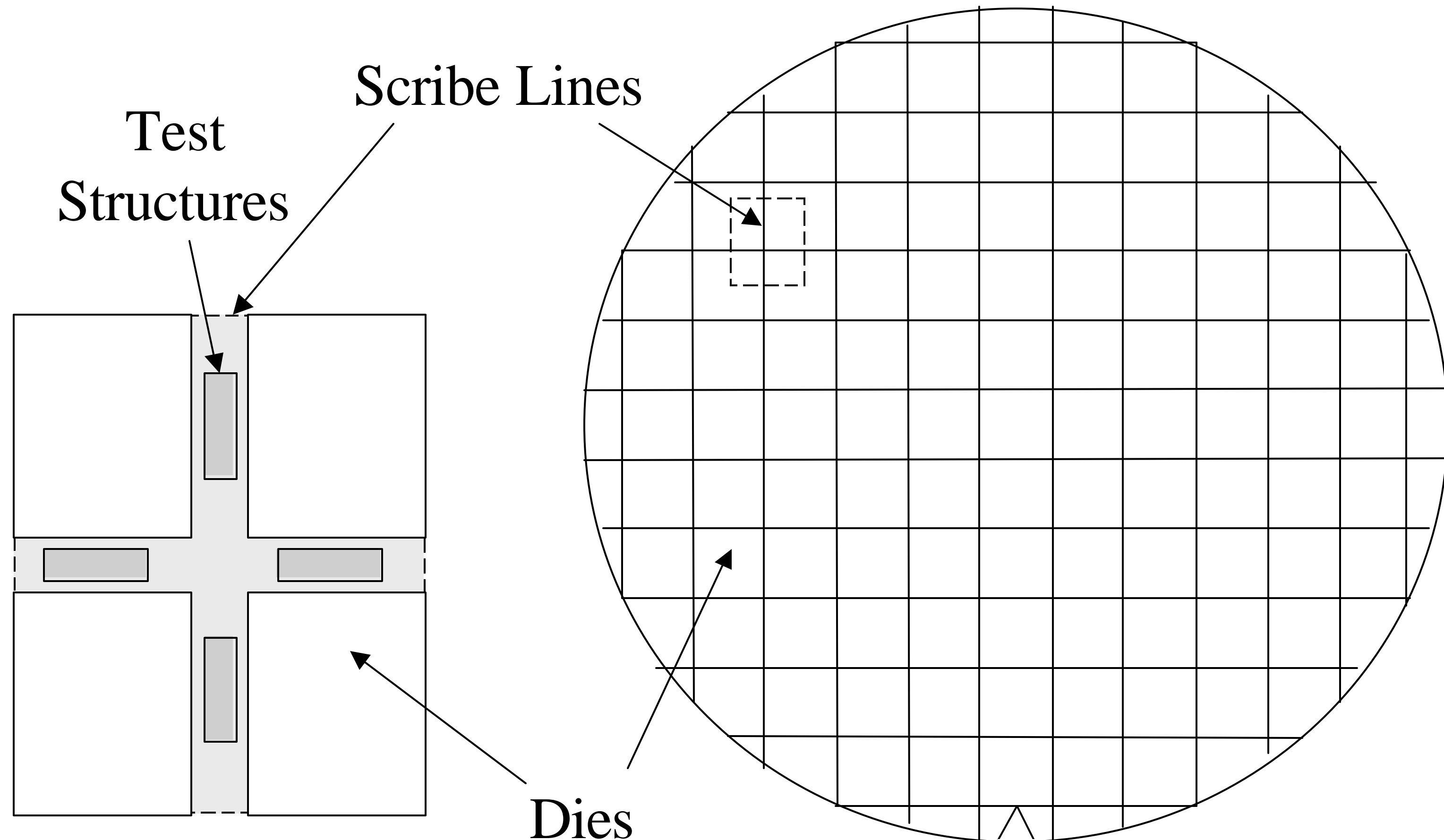


Illustration of a Production Wafer



Clean Room

- Particles kills yield
- IC fabrication must in a clean room
- Artificial environment with low particle counts

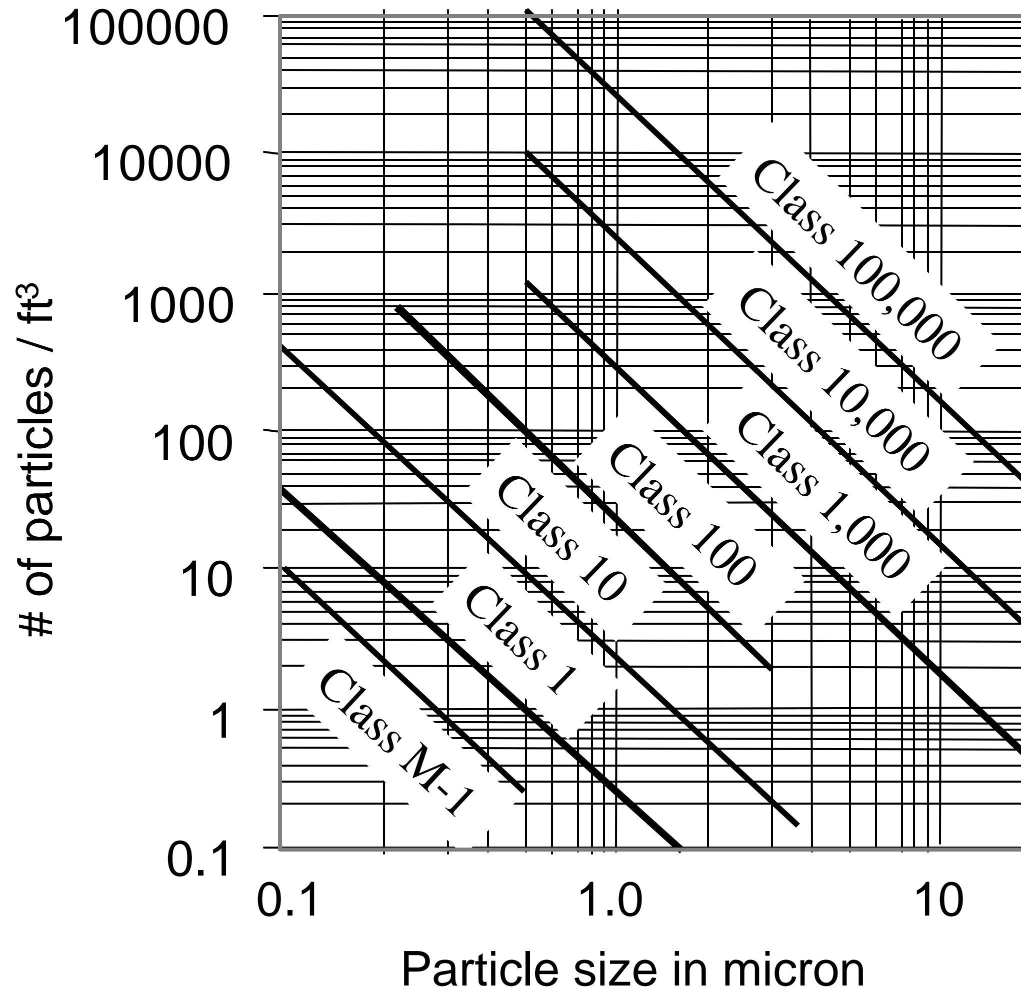
Clean Room

- First used for surgery room to avoid bacteria contamination
- Adopted in semiconductor industry in 1950
- Smaller device needs higher grade clean room
- Less particle, more expensive to build

Clean Room Class

- Class 10 is defined as less than 10 particles with diameter larger than 0.5 μm per cubic foot.
- Class 1 is defined as less than 1 such particles per cubic foot.
- 0.18 mm device require higher than Class 1 grade clean room.

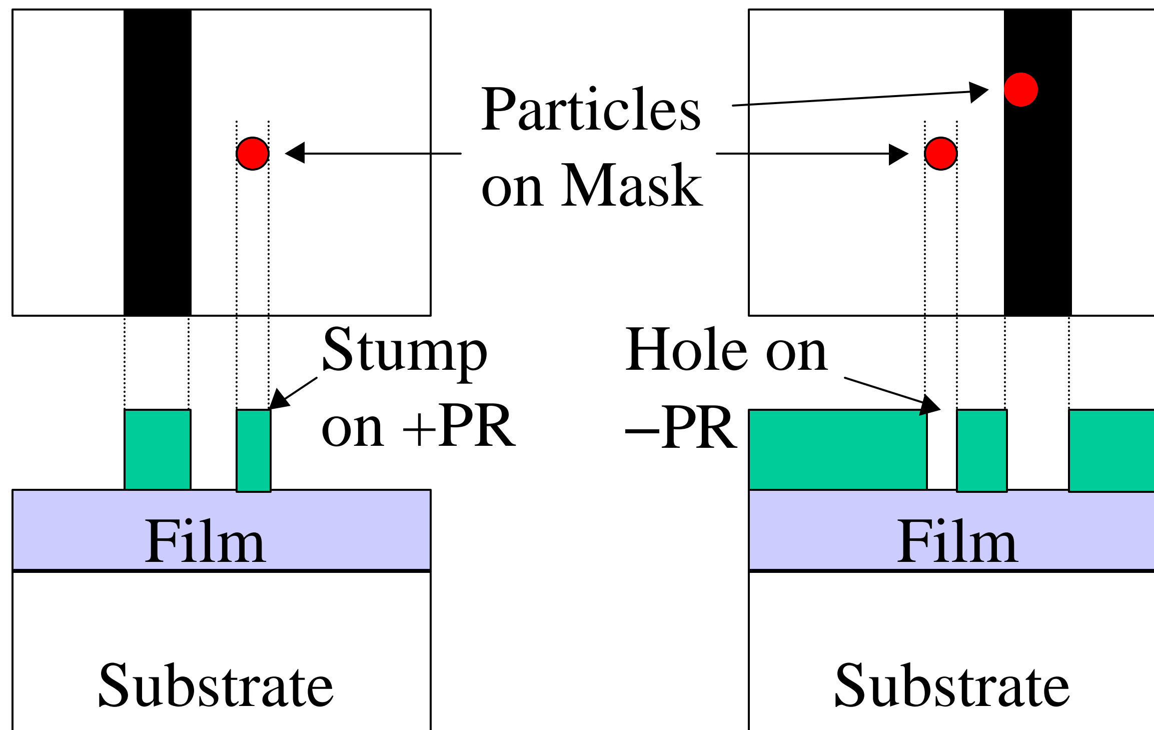
Cleanroom Classes



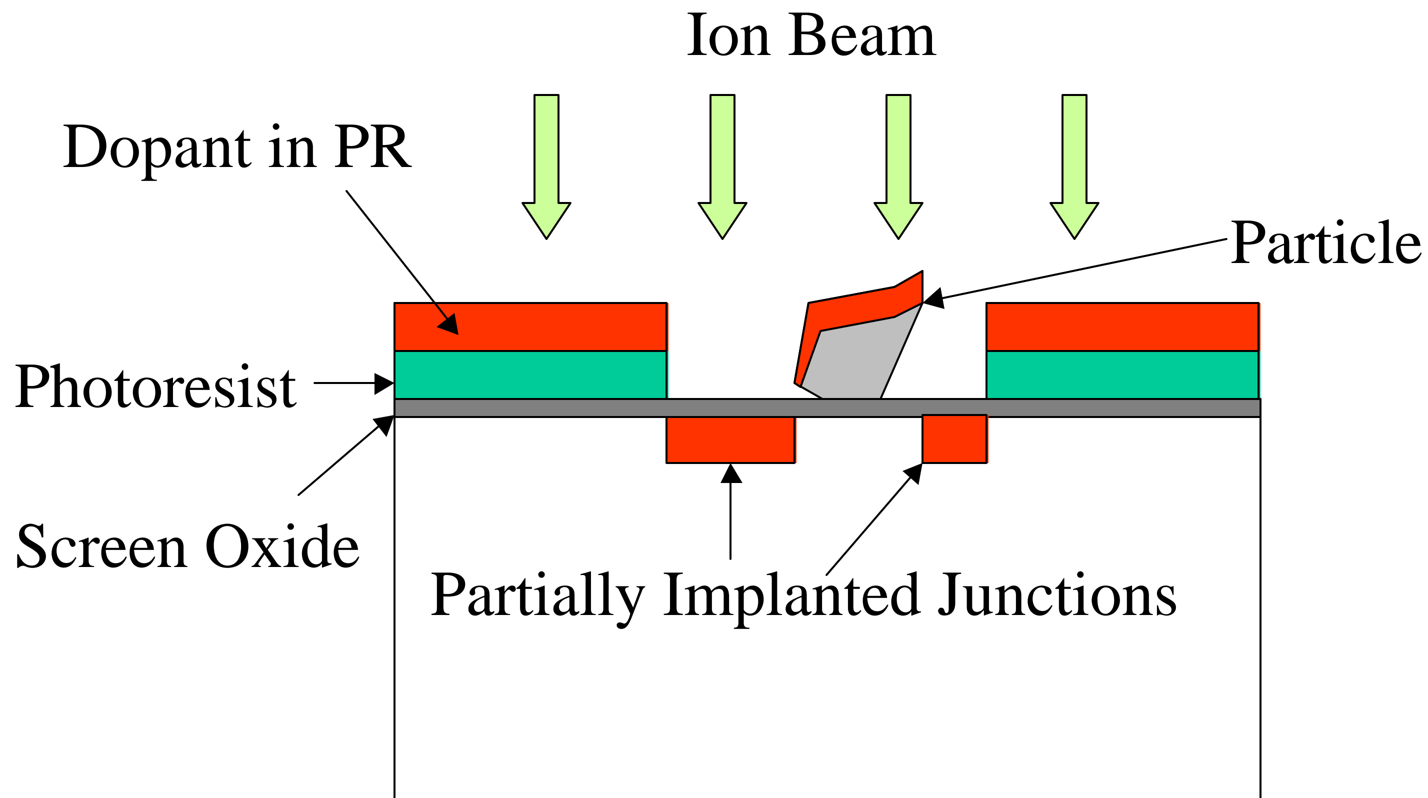
Definition of Airborne Particulate Cleanliness Class per Fed. Std. 209E

Class	Particles/ft^3				
	0.1 μm	0.2 μm	0.3 μm	0.5 μm	5 μm
M-1	9.8	2.12	0.865	0.28	
1	35	7.5	3	1	
10	350	75	30	10	
100		750	300	100	
1000				1000	7
10000				10000	70

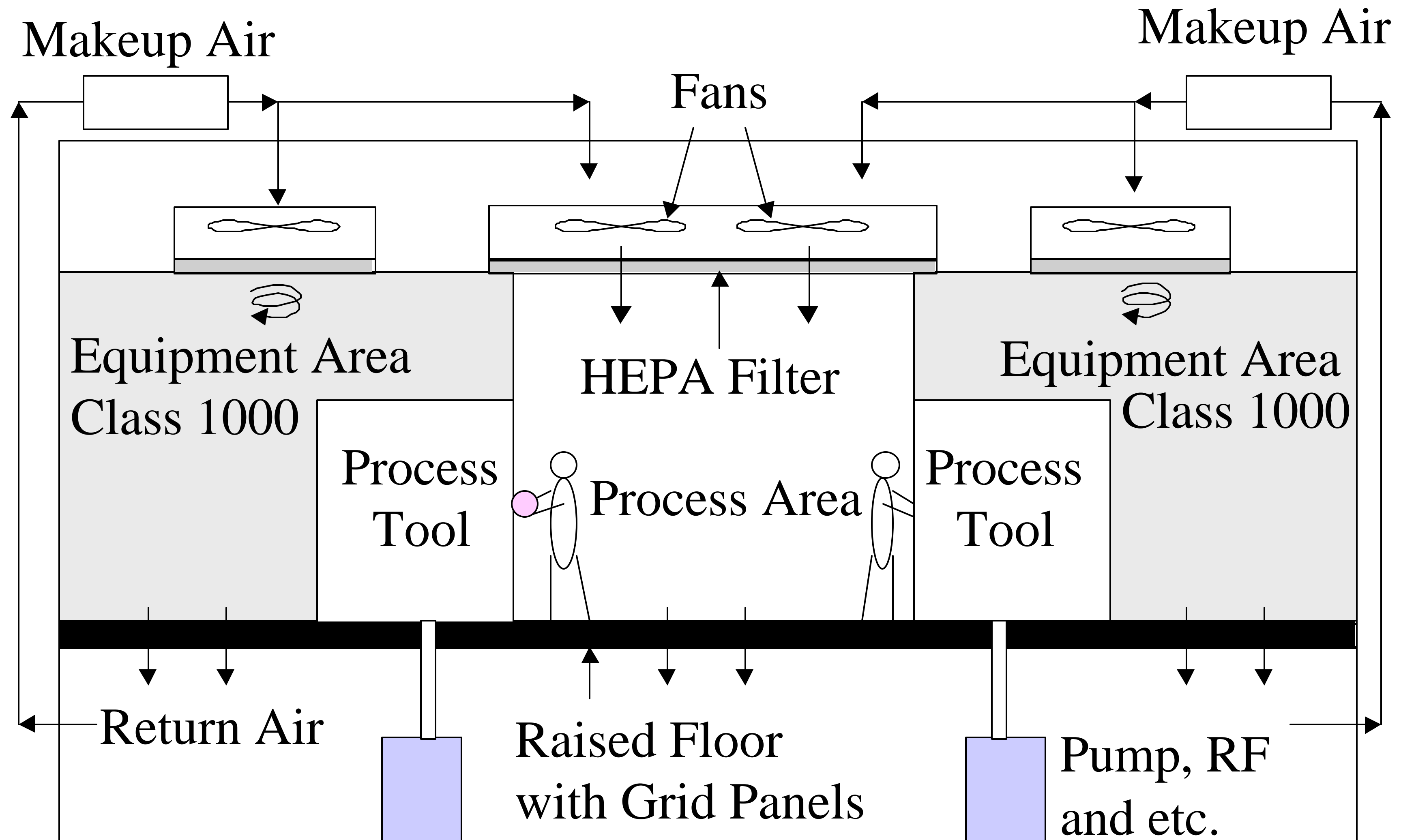
Effect of Particles on Masks



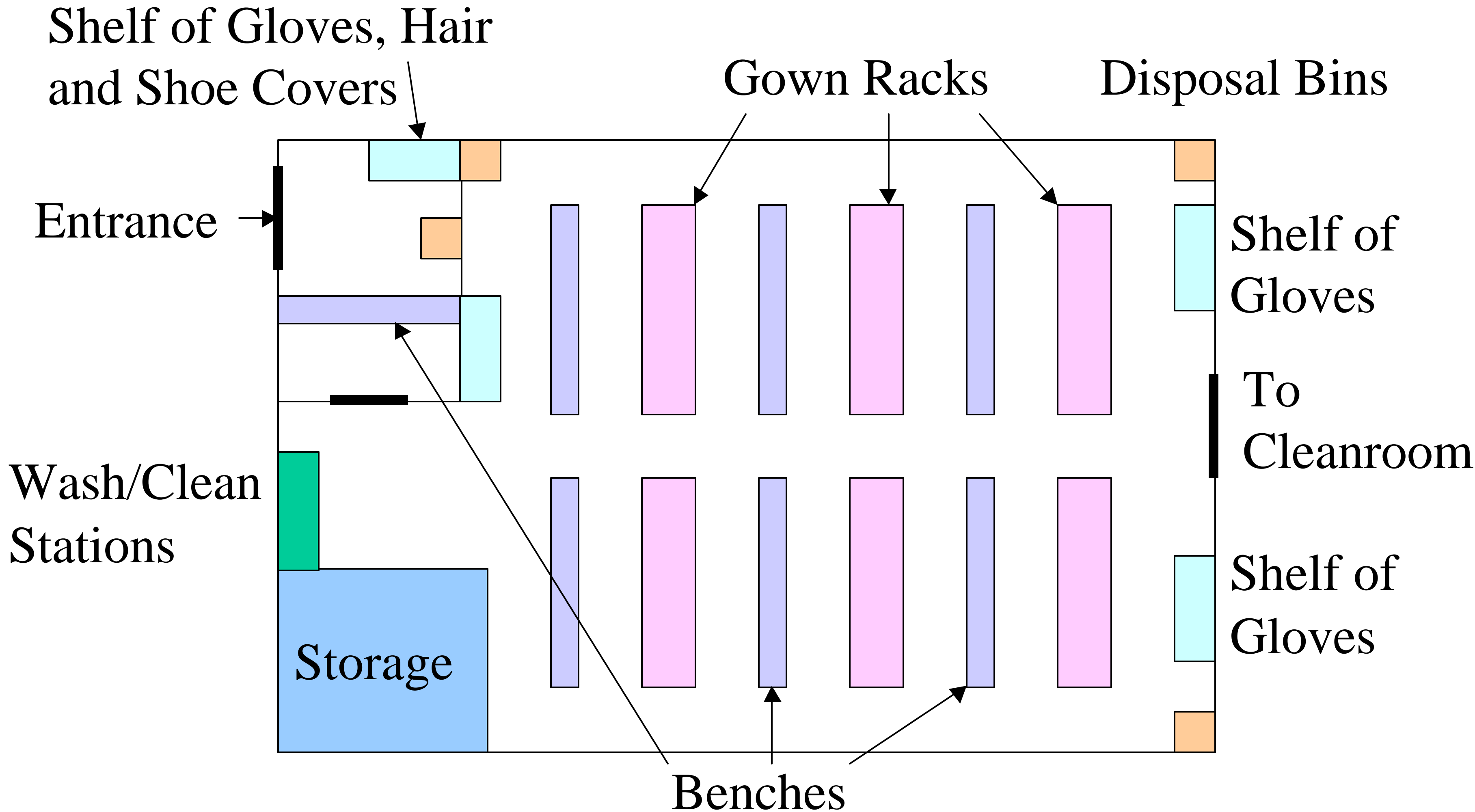
Effect of Particle Contamination



Cleanroom Structure



Gowning Area



IC Fabrication Process Module

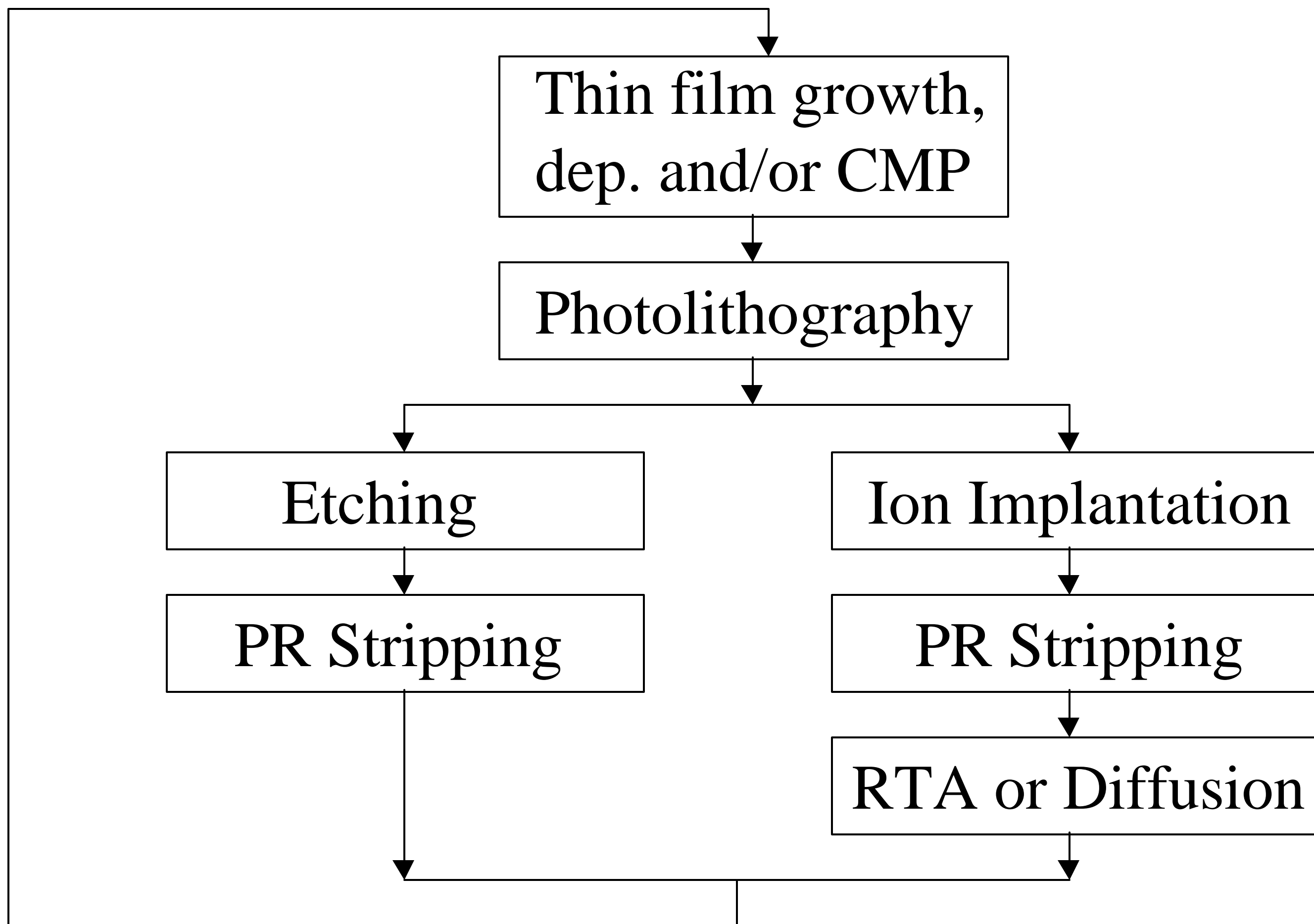
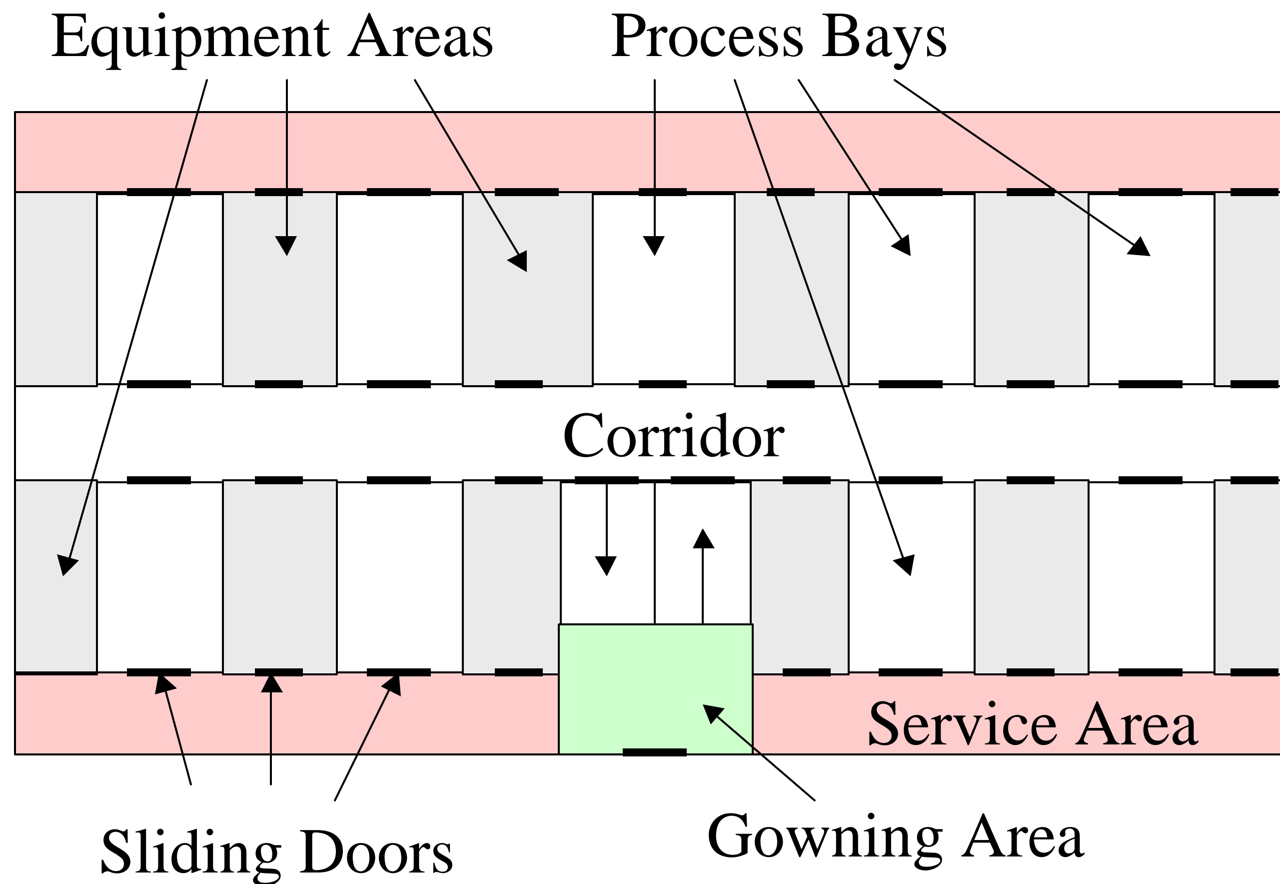
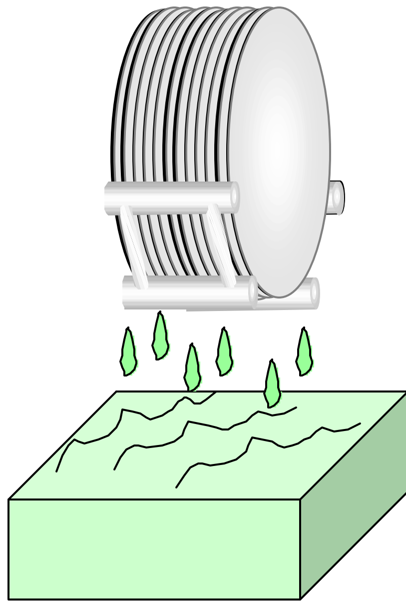
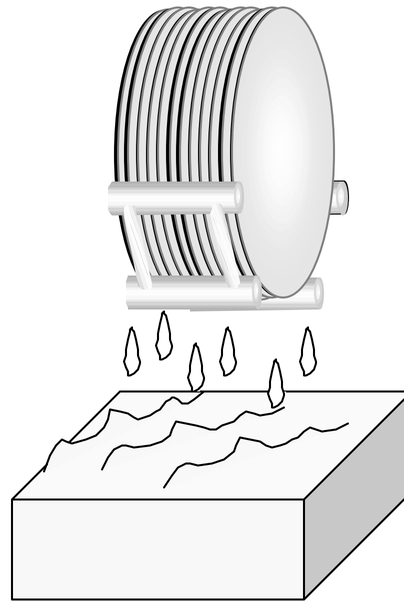


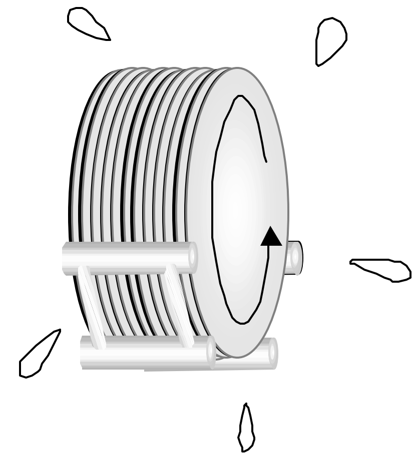
Illustration of Fab Floor



Wet Processes





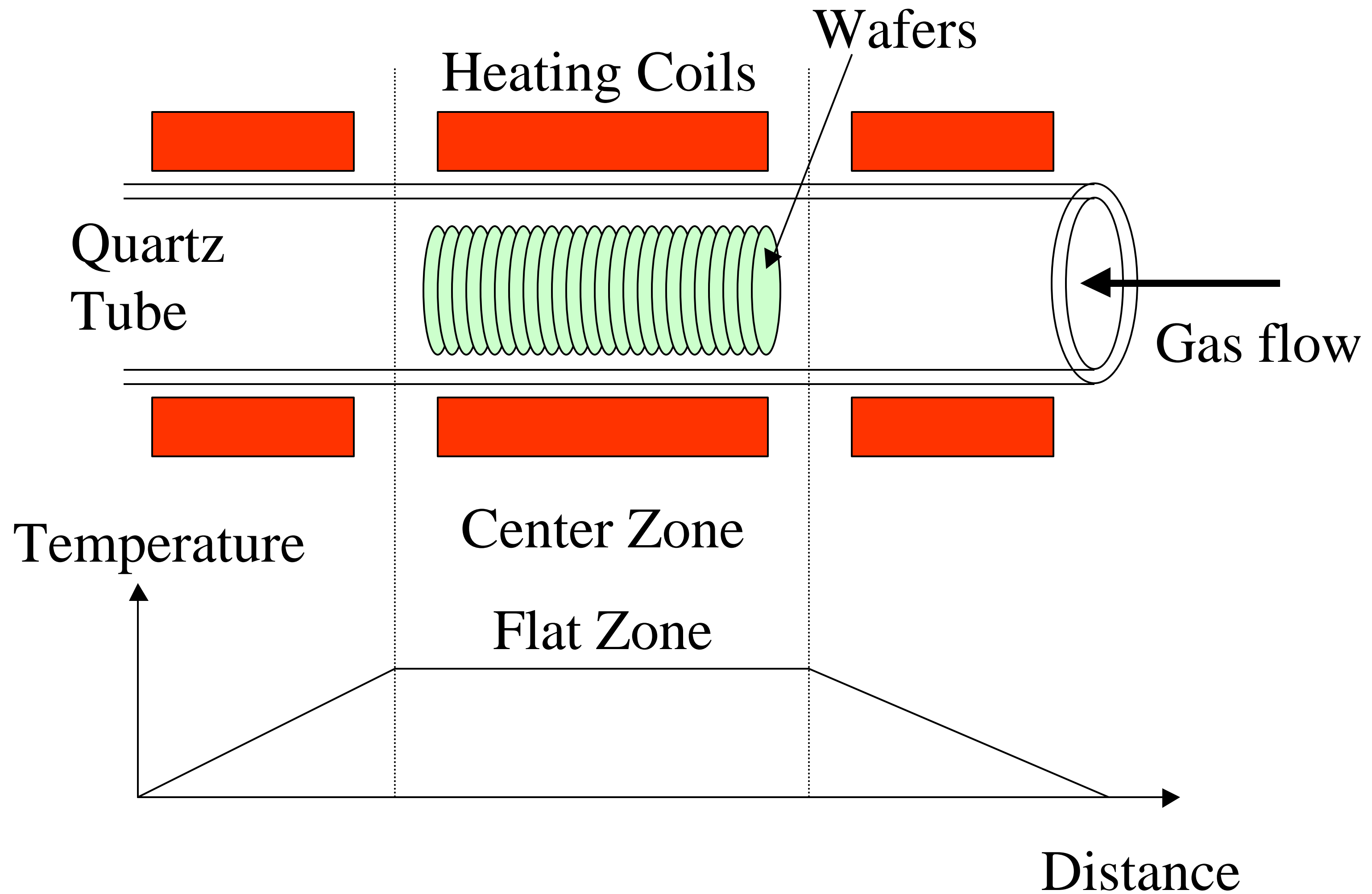


Etch, PR strip, or clean

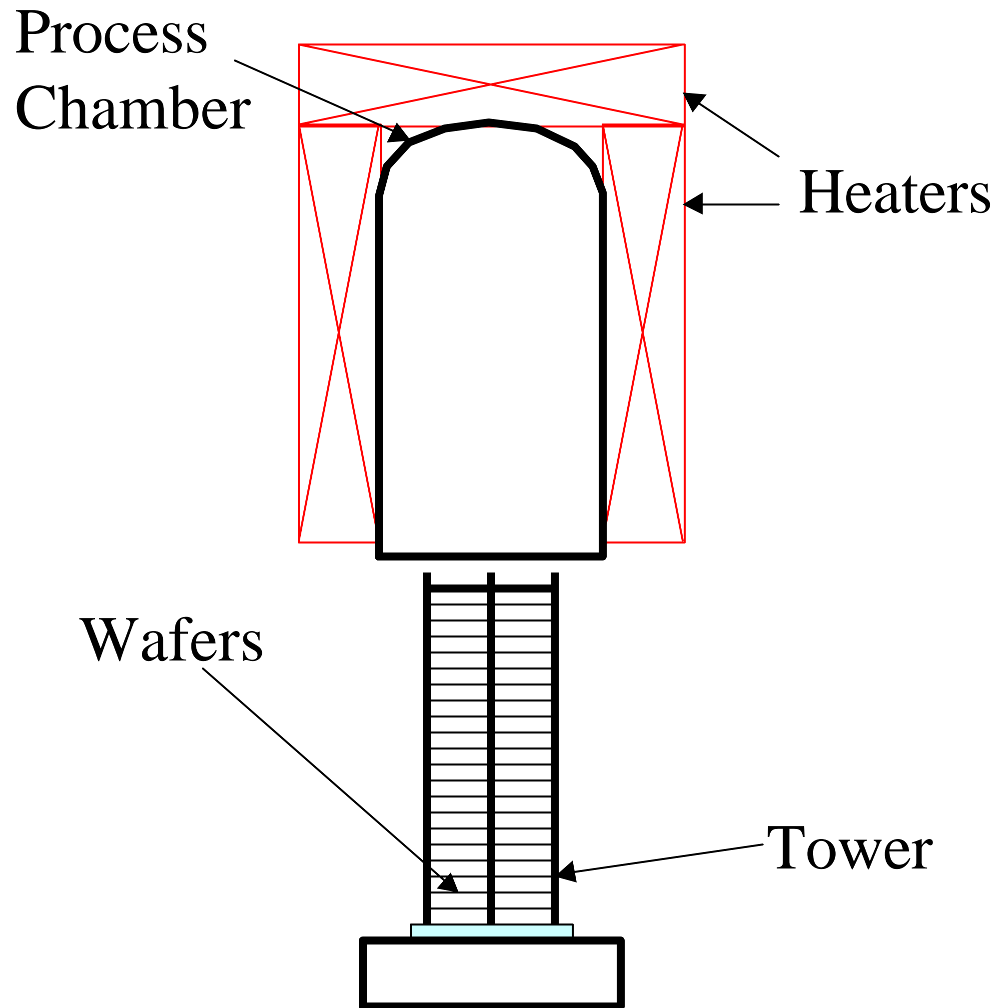
Rinse

Dry

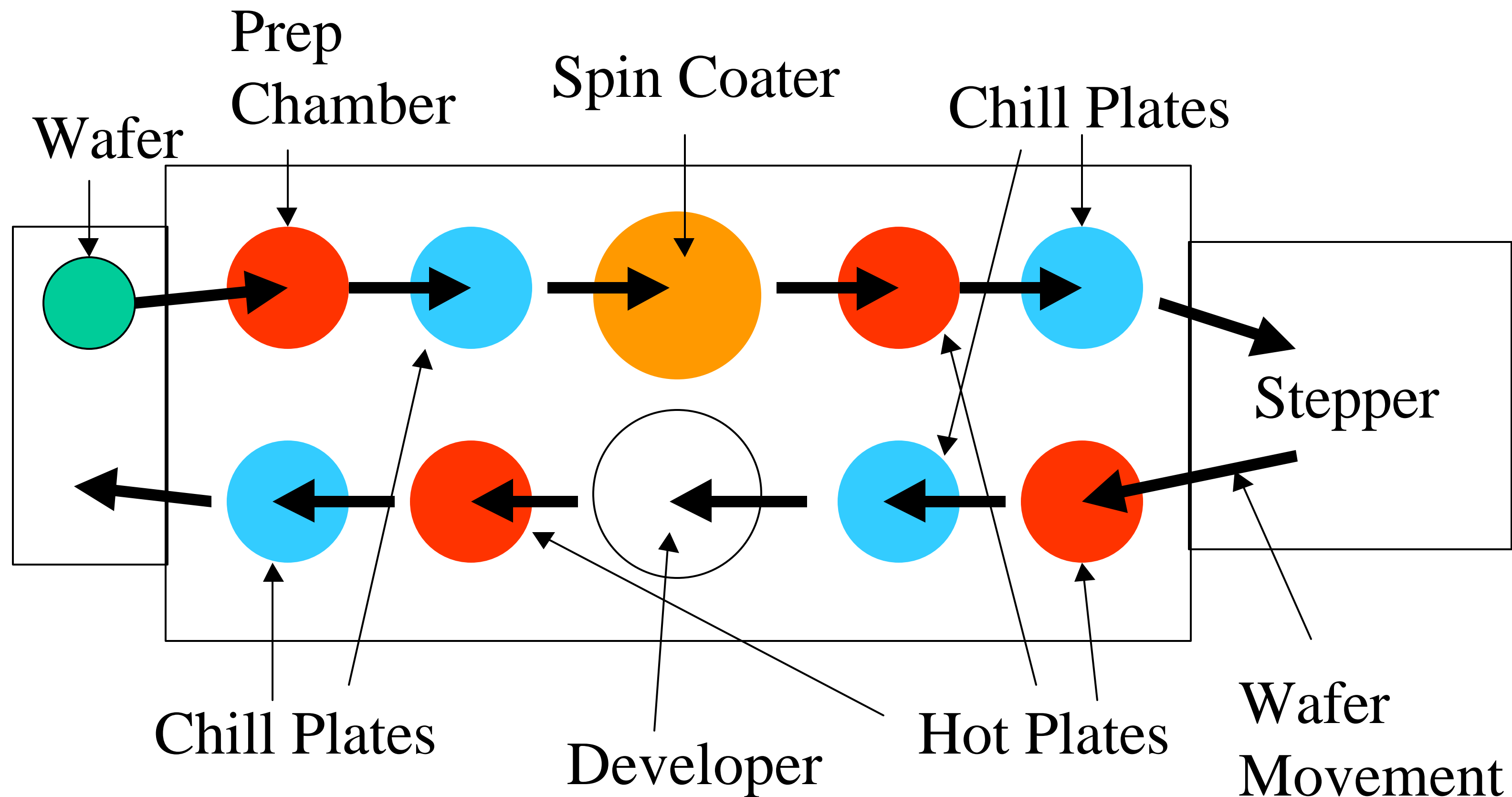
Horizontal Furnace



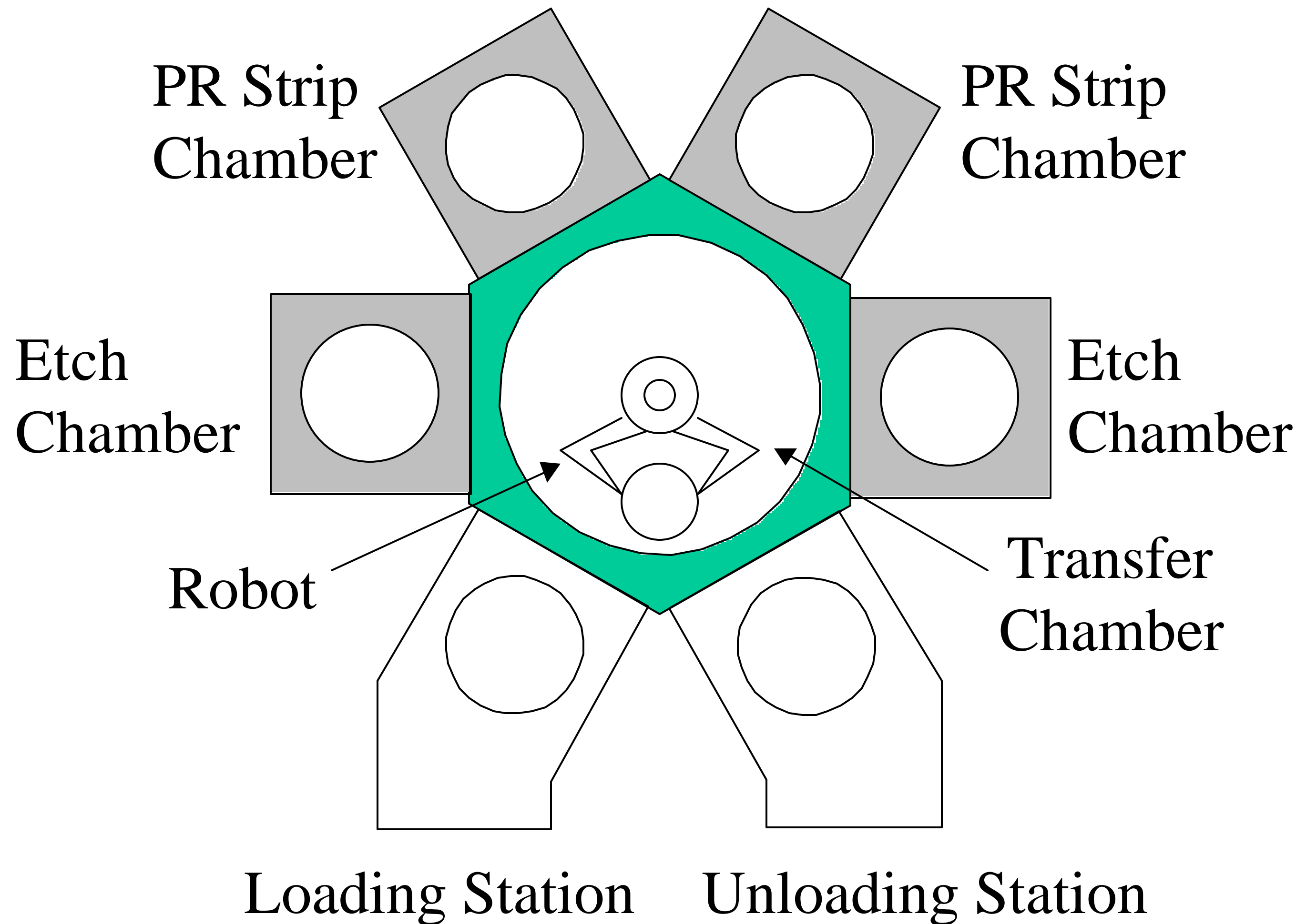
Vertical Furnace



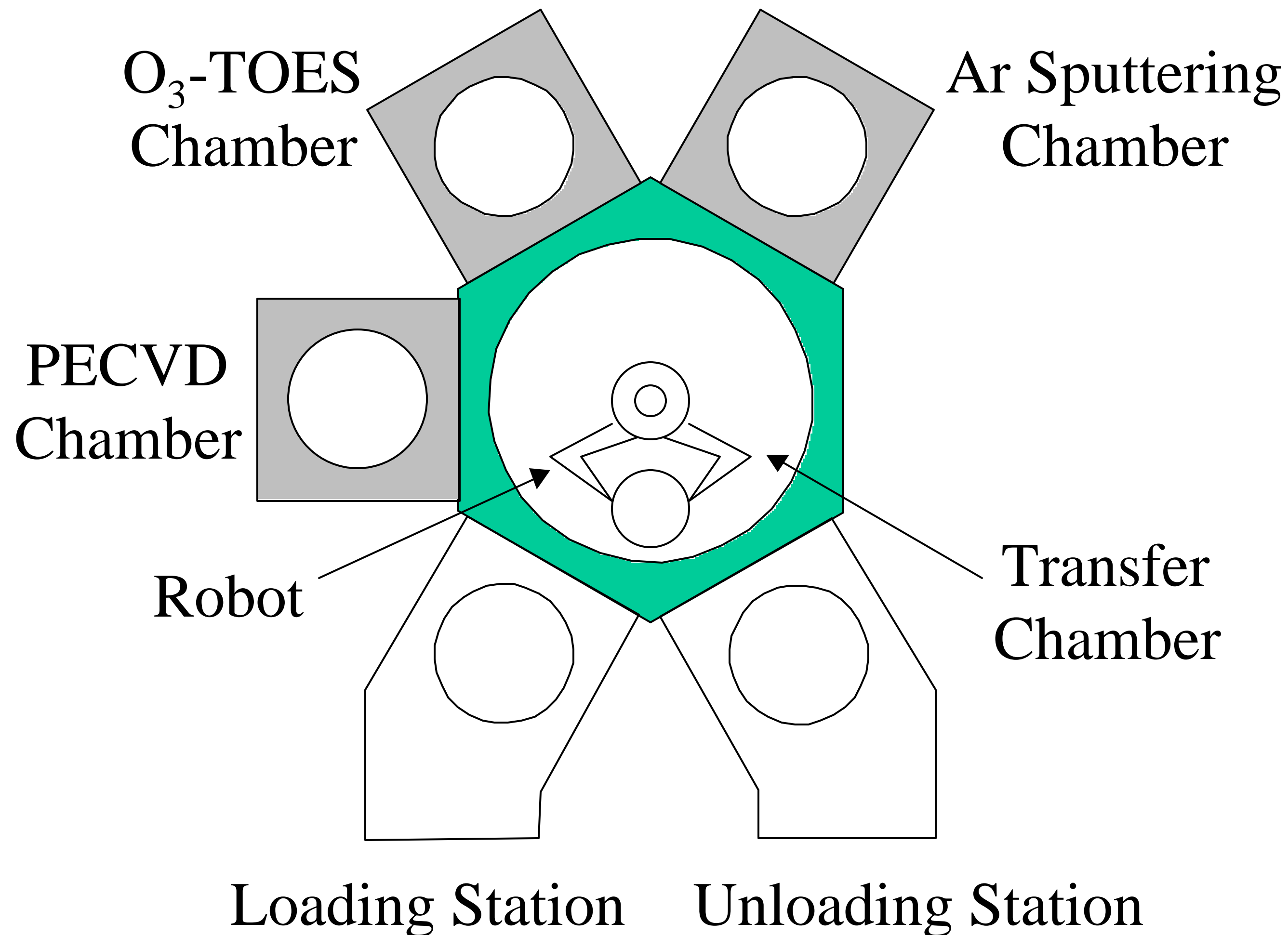
Schematic of a Track Stepper Integrated System



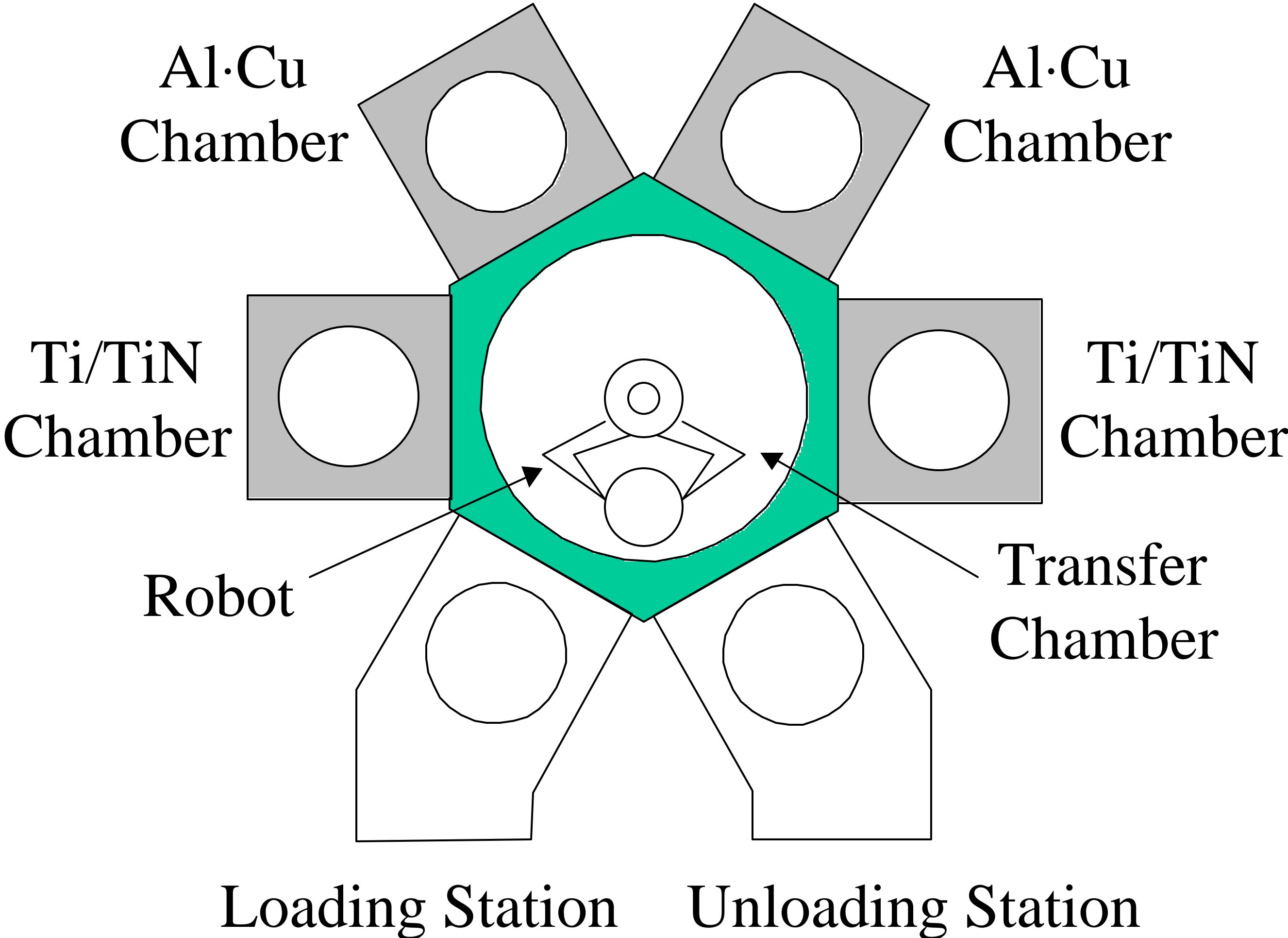
Cluster Tool with Etch and Strip Chambers



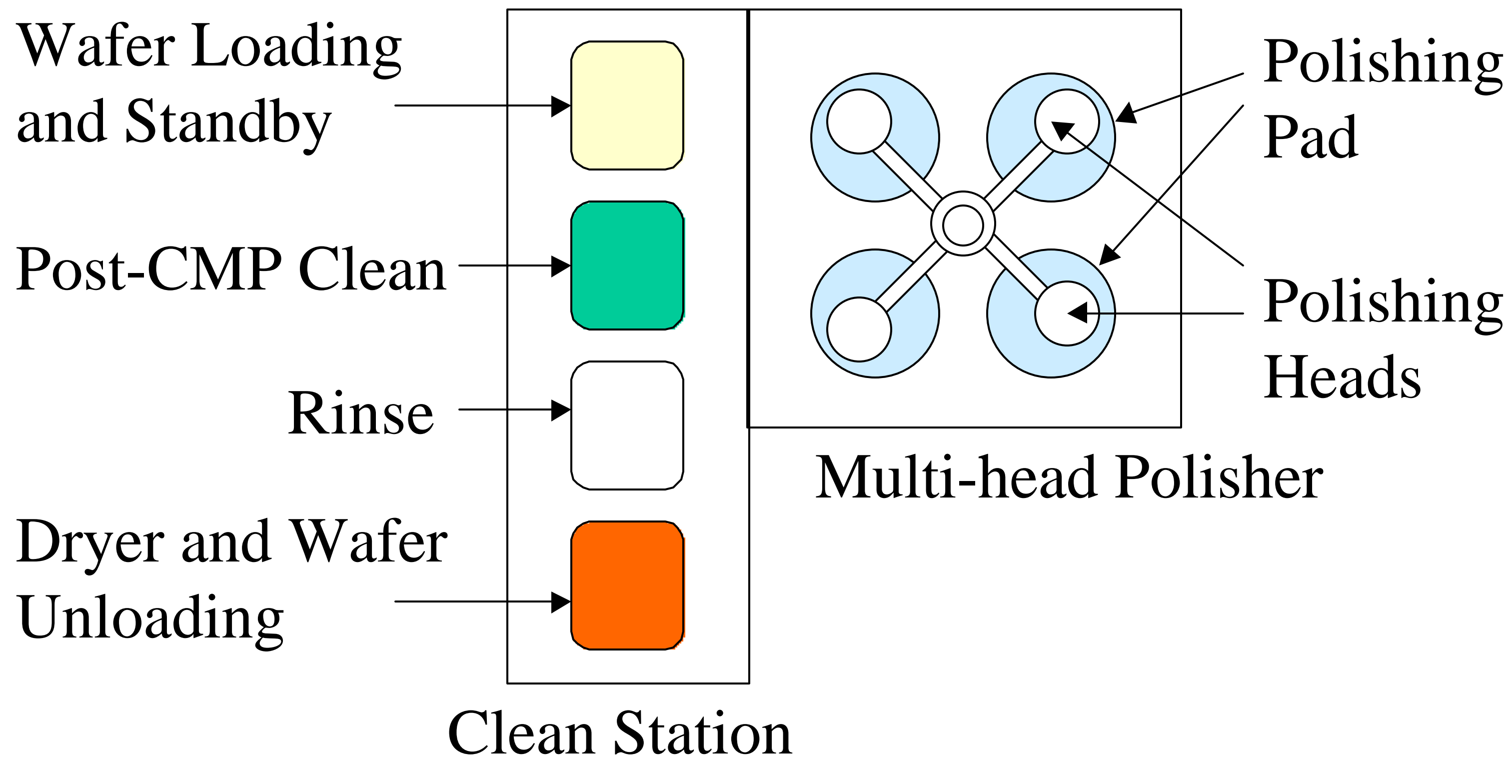
Cluster Tool with Dielectric CVD and Etchback Chambers



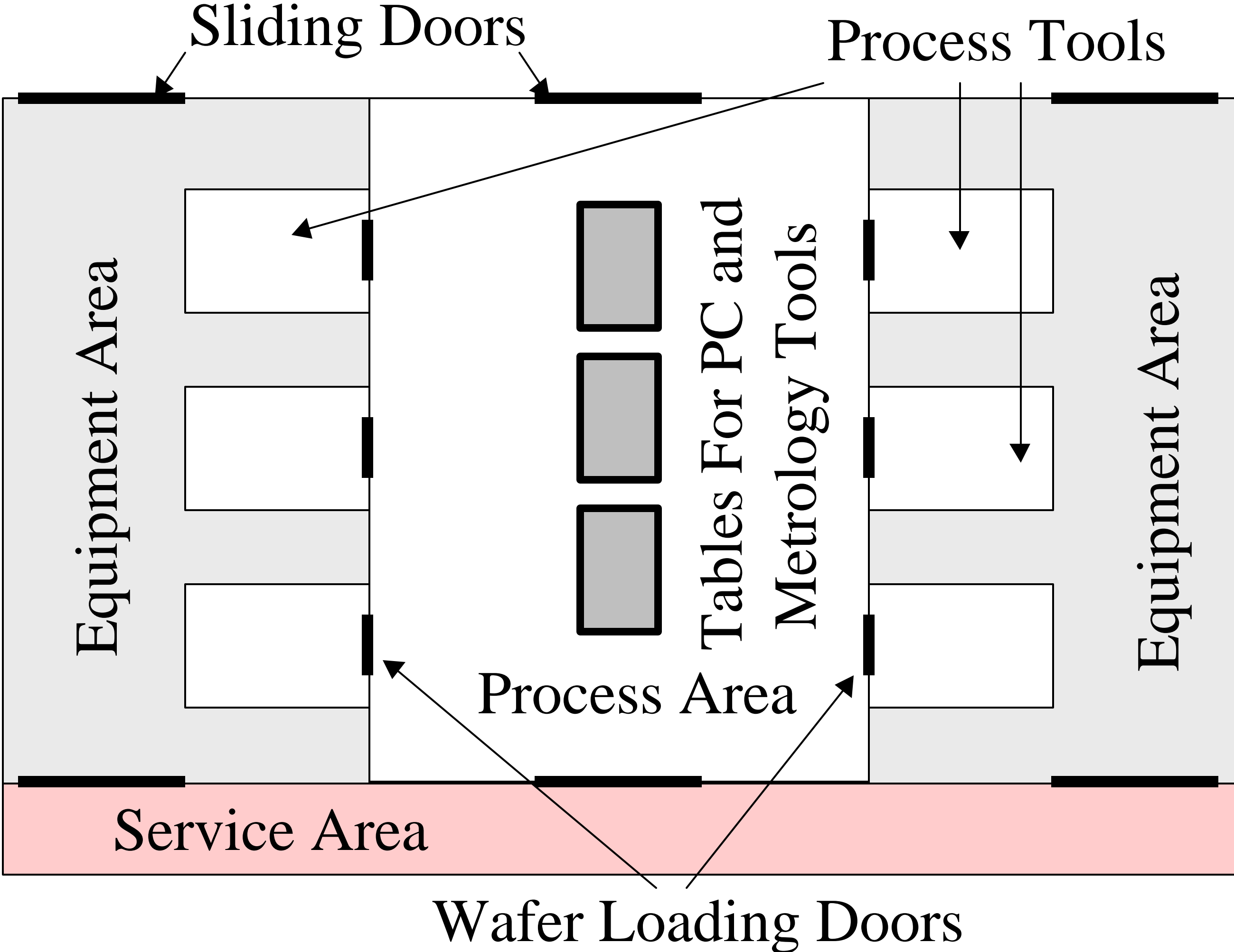
Cluster Tool with PVD Chambers



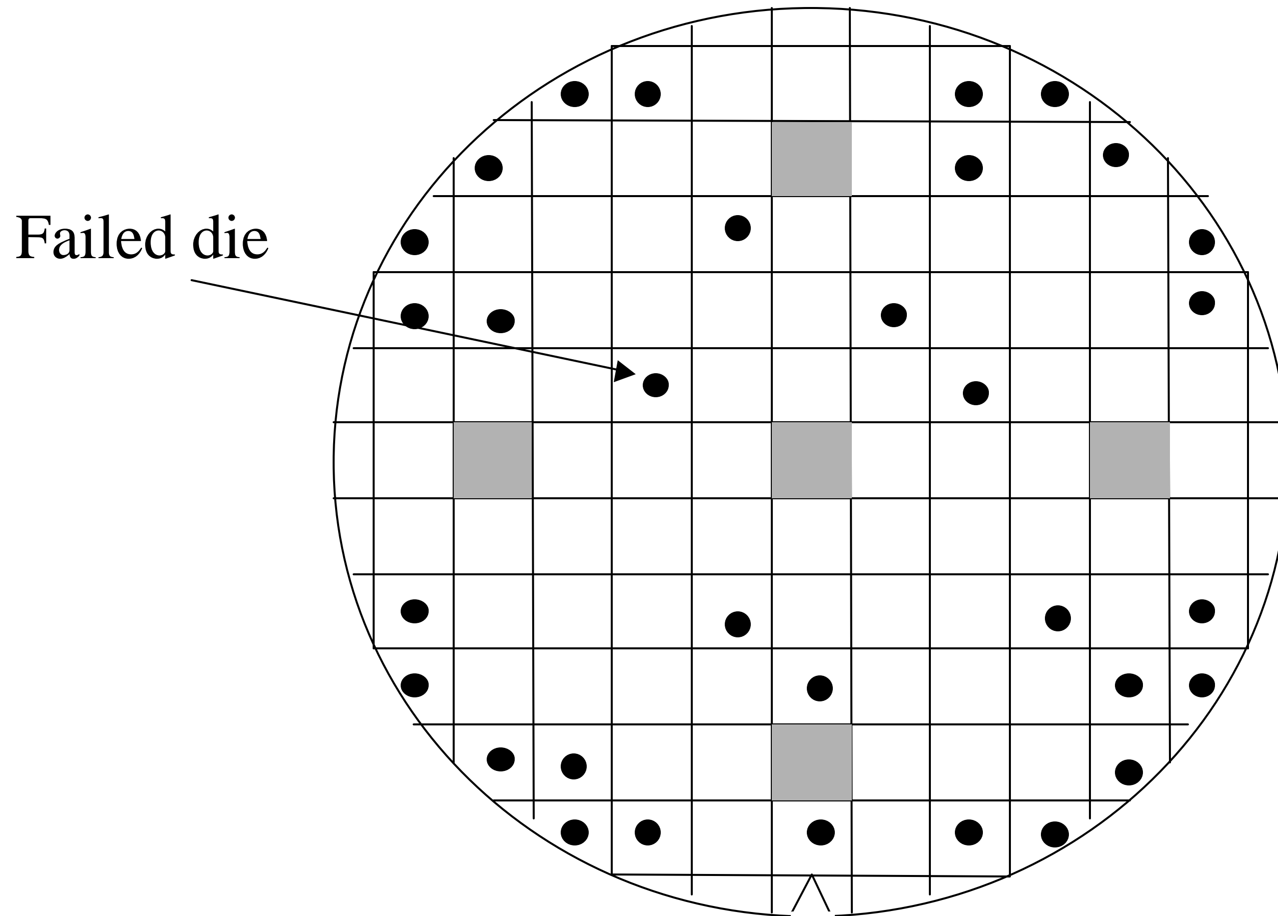
Dry-in Dry-out CMP System



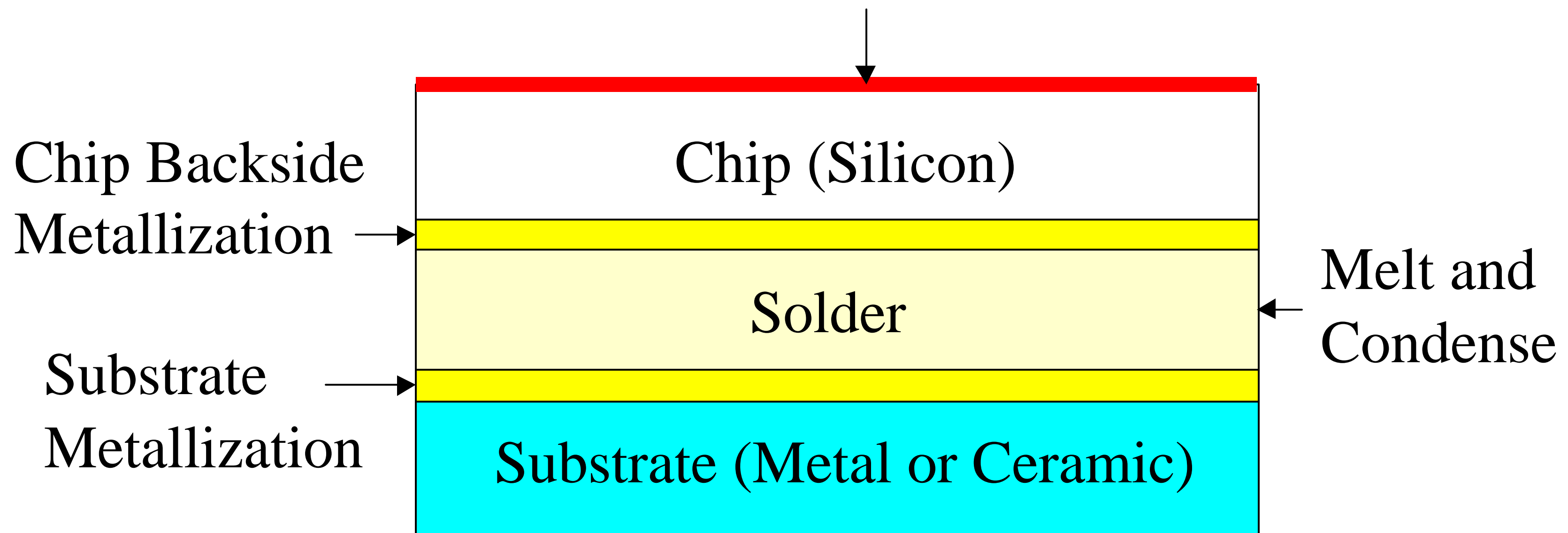
Process Bay and Equipment Areas



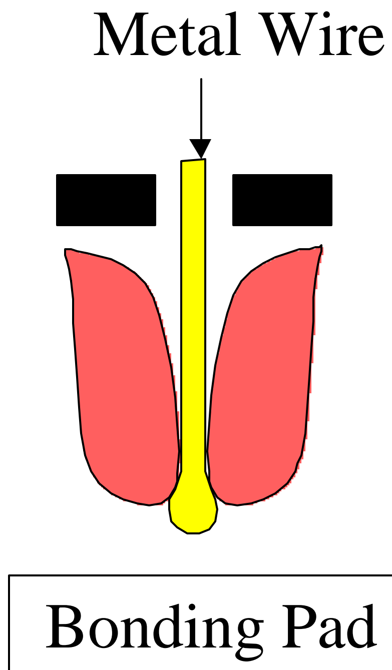
Test Results



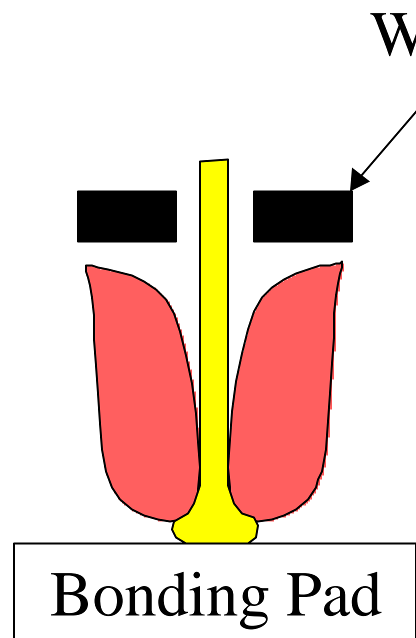
Chip-Bond Structure



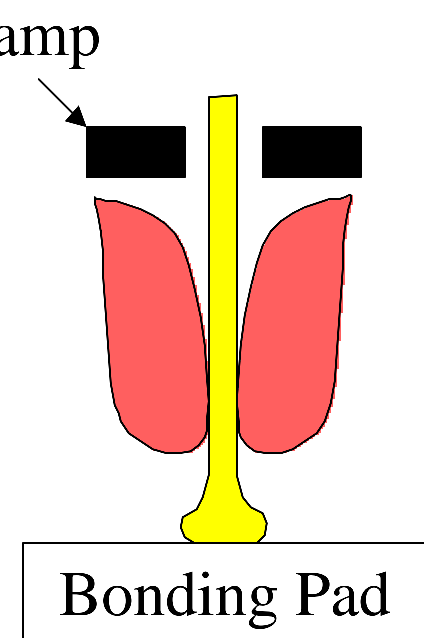
Wire Bonding



Formation of molten metal ball

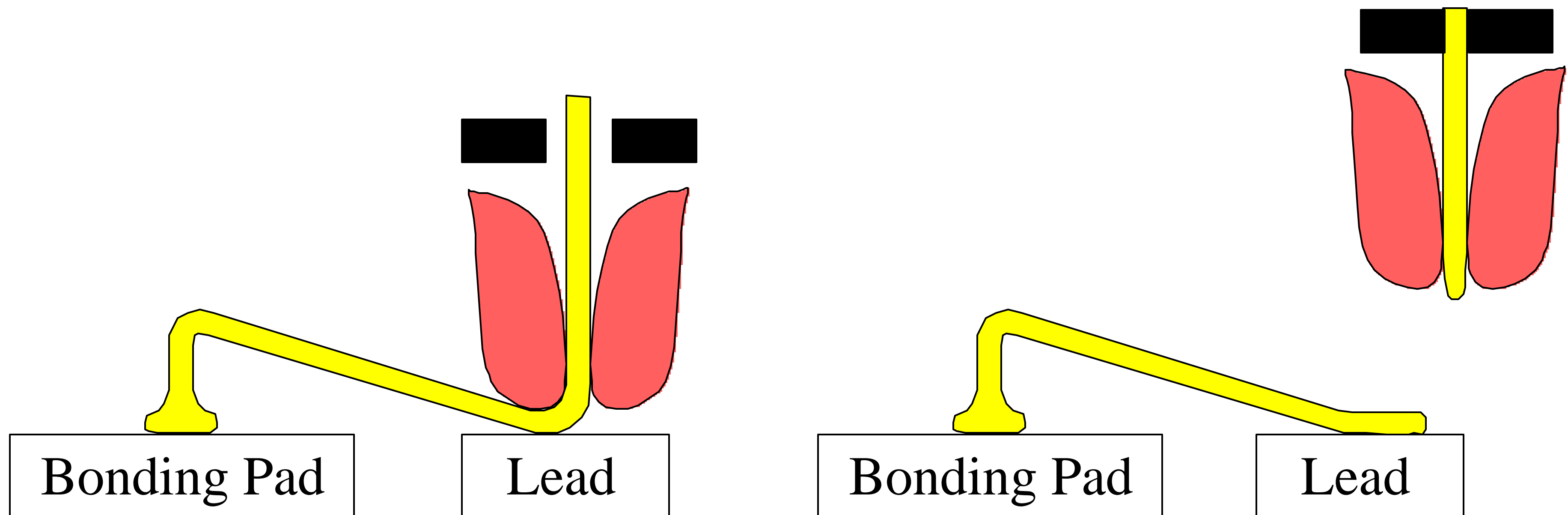


Press to make contact



Head retreat

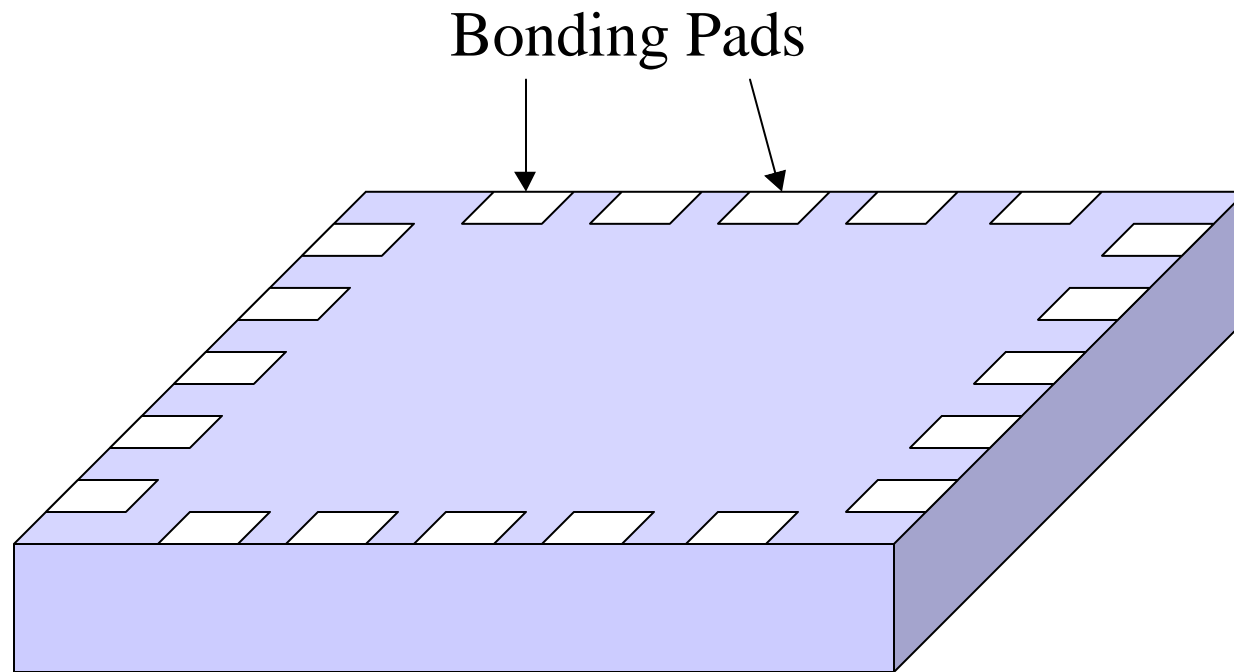
Wire Bonding



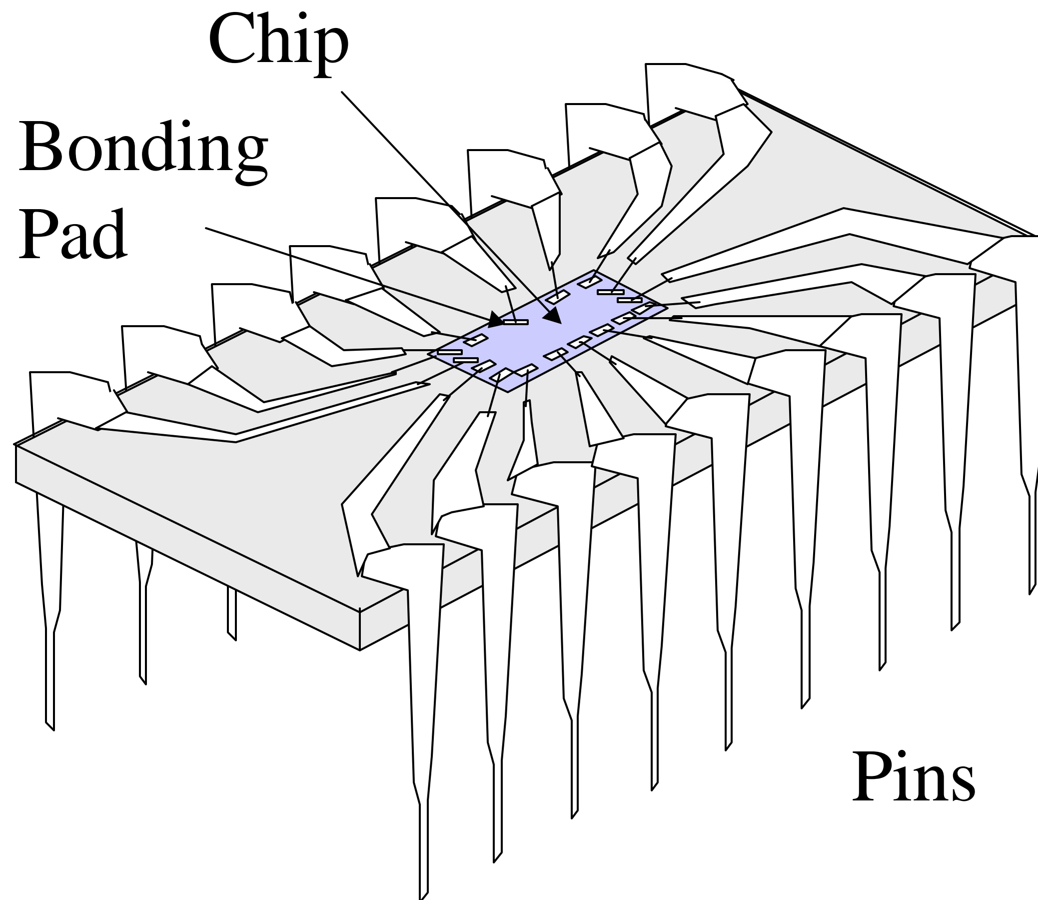
Lead contact with pressure and heat

Clamp closed with heat on to break the wire

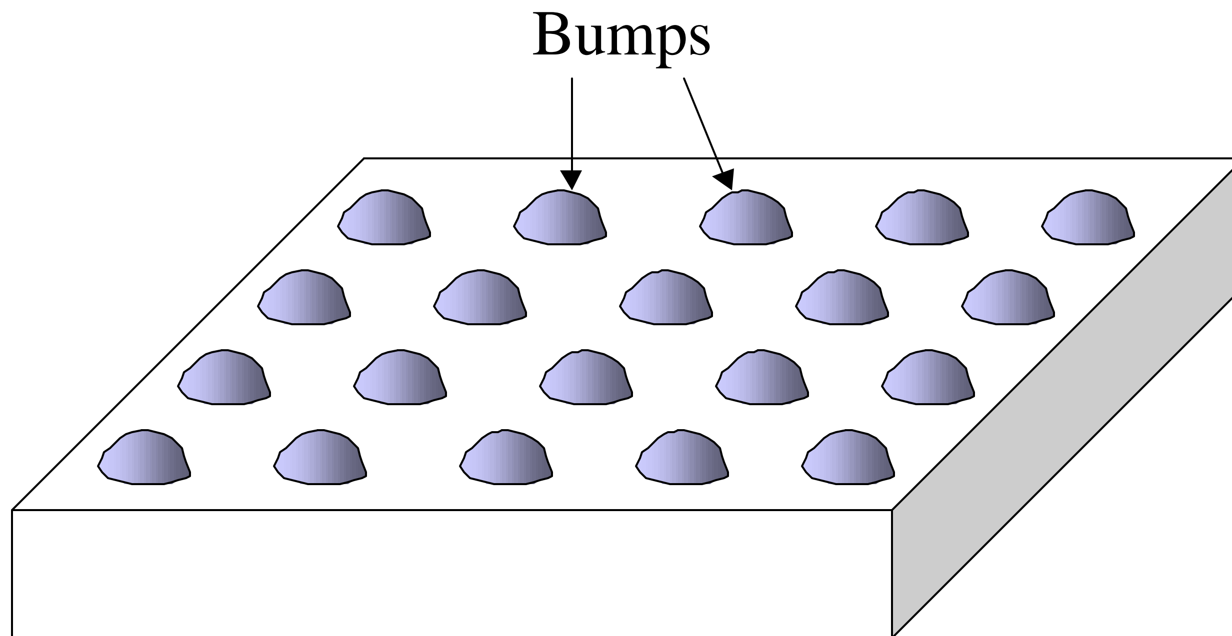
IC Chip with Bonding Pads



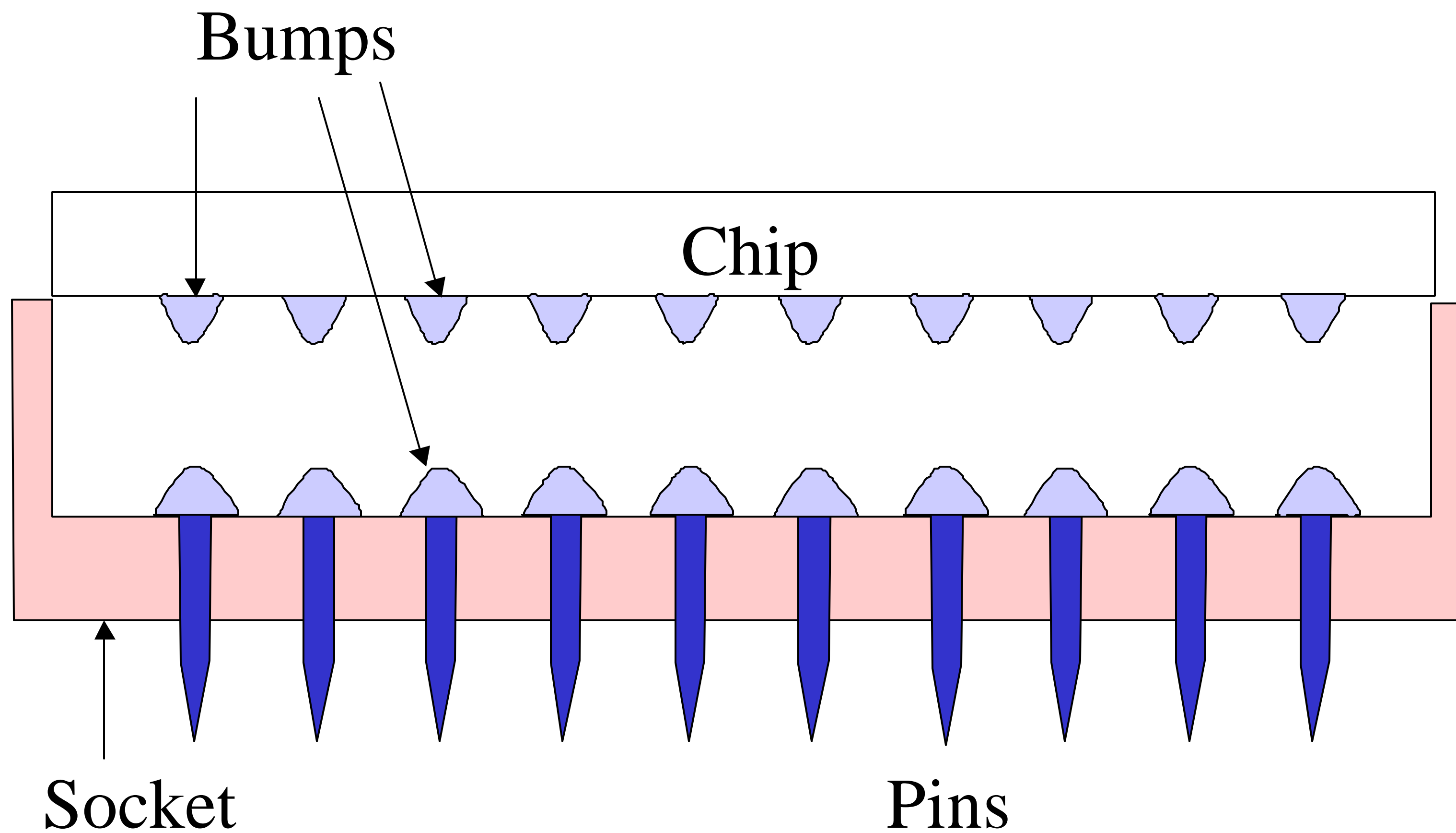
IC Chip Packaging



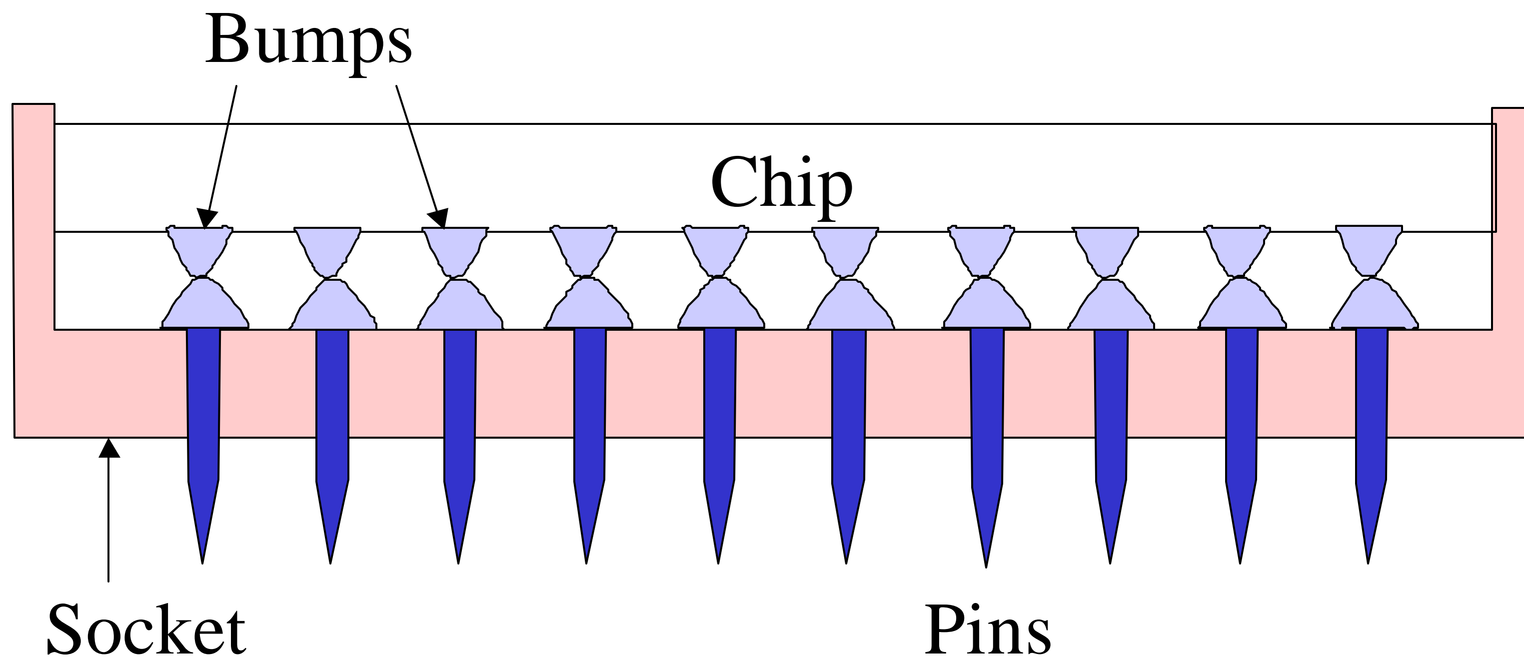
Chip with Bumps



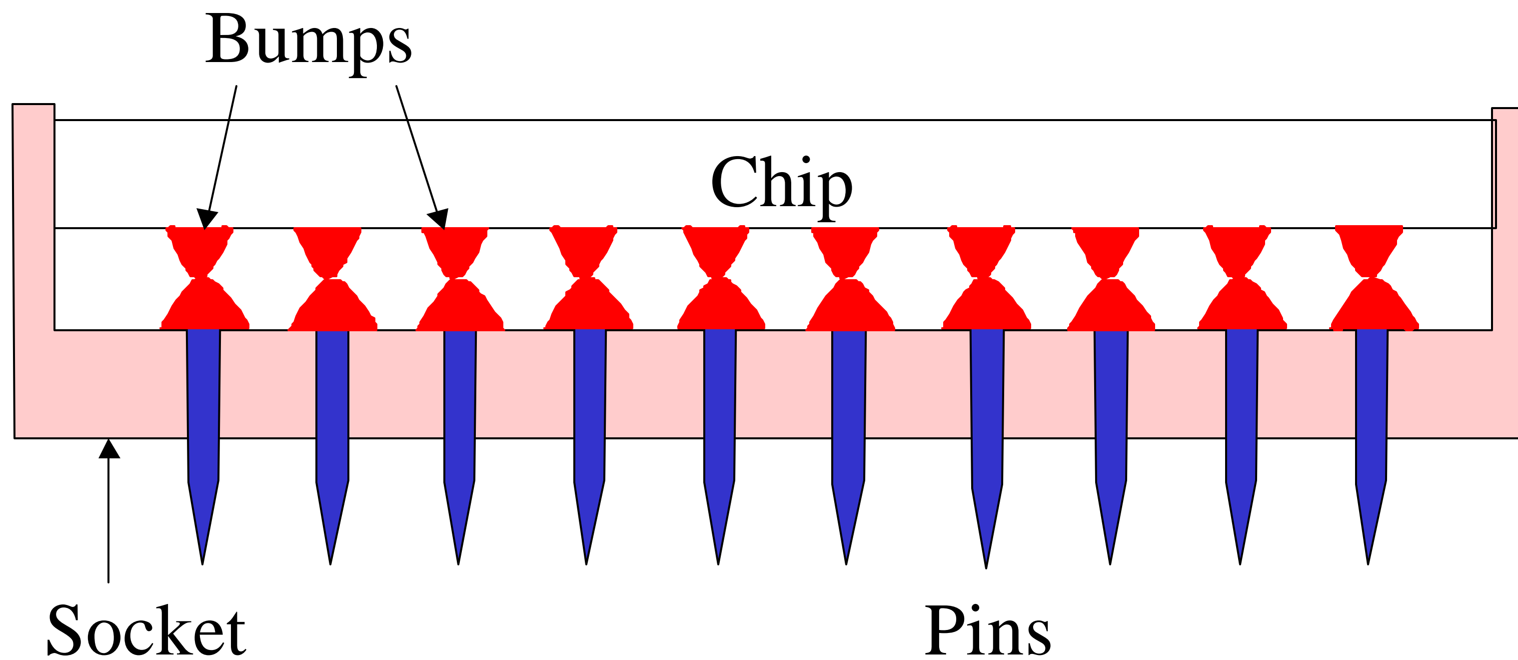
Flip Chip Packaging



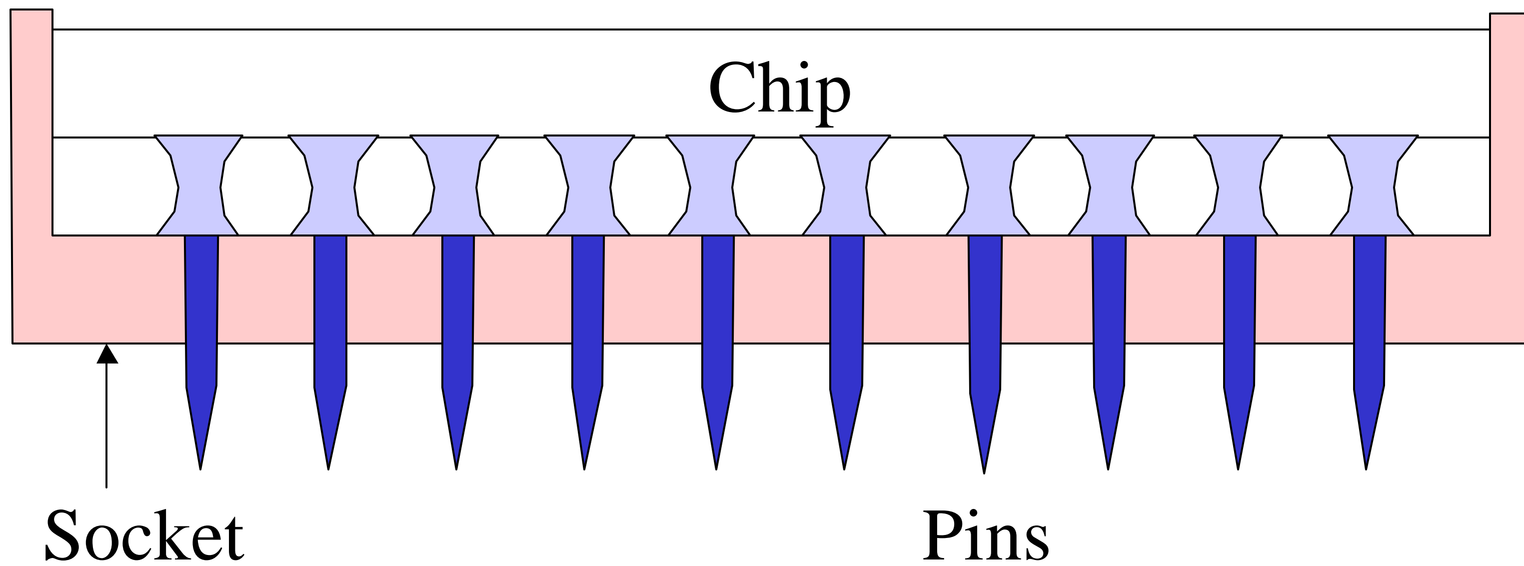
Bump Contact



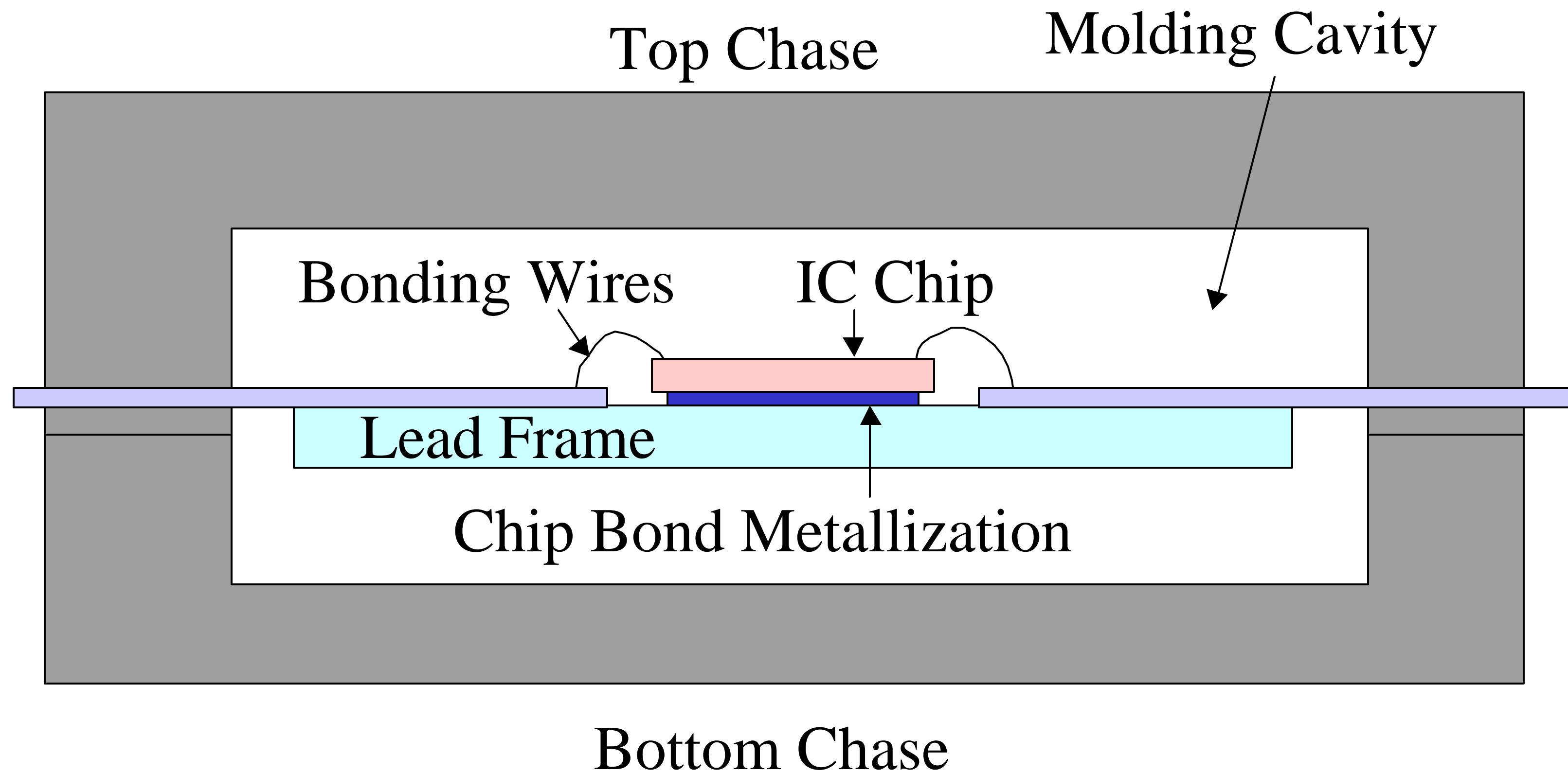
Heating and Bumps Melt



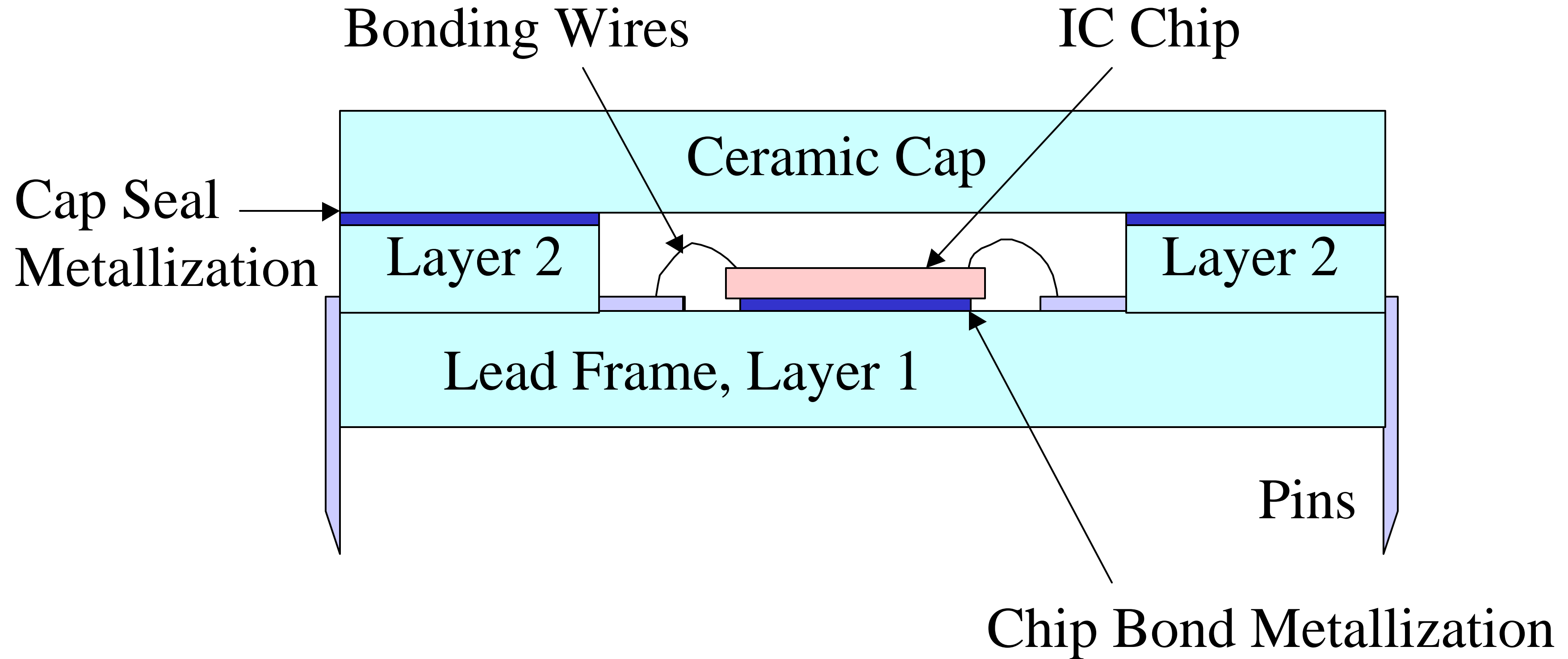
Flip Chip Packaging



Molding Cavity for Plastic Packaging



Ceramic Seal



Summary

- Overall yield
- Yield determines losing money or making profit
- Cleanroom and cleanroom protocols
- Process bays
- Process, equipment, and facility areas
- Die test, wafer thinning, die separation, chip packaging, and final test

Chapter 3
Basics Semiconductor Devices and Processing

Hong Xiao, Ph. D.

www2.austin.cc.tx.us/HongXiao/Book.htm

Objectives

- Identify at least two semiconductor materials from the periodic table of elements
- List n-type and p-type dopants
- Describe a diode and a MOS transistor
- List three kinds of chips made in the semiconductor industry
- List at least four basic processes required for a chip manufacturing

Topics

- What is semiconductor
- Basic semiconductor devices
- Basics of IC processing

What is Semiconductor

- Conductivity between conductor and insulator
- Conductivity can be controlled by dopant
- Silicon and germanium
- Compound semiconductors
  - SiGe, SiC
  - GaAs, InP, etc.

Periodic Table of the Elements

	IA	IIA	IIIB	IVB	VB	VIB	VIIB	VII			IB	IIB	IIIA	IVA	VA	VIA	VIIA	0
1	1 H																	2 He
2	3 Li	4 Be											5 B	6 C	7 N	8 O	9 F	10 Ne
3	11 Na	12 Mg											13 Al	14 Si	15 P	16 S	17 Cl	18 Ar
4	19 K	20 Ca	21 Sc	22 Ti	23 V	24 Cr	25 Mn	26 Fe	27 Co	28 Ni	29 Cu	30 Zn	31 Ga	32 Ge	33 As	34 Se	35 Br	36 Kr
5	37 Rb	38 Sr	39 Y	40 Zr	41 Nb	42 Mo	43 Tc	44 Ru	45 Rh	46 Pd	47 Ag	48 Cd	49 In	50 Sn	51 Sb	52 Te	53 I	54 Xe
6	55 Cs	56 Ba	57 *La	72 Hf	73 Ta	74 W	75 Re	76 Os	77 Ir	78 Pt	79 Au	80 Hg	81 Tl	82 Pb	83 Bi	84 Po	85 At	86 Rn
7	87 Fr	88 Ra	89 +Ac	104 Rf	105 Ha	106 Sg	107 Ns	108 Hs	109 Mt	110 110	111 111	112 112	113 113					

* Lanthanide Series	58 Ce	59 Pr	60 Nd	61 Pm	62 Sm	63 Eu	64 Gd	65 Tb	66 Dy	67 Ho	68 Er	69 Tm	70 Yb	71 Lu
+ Actinide Series	90 Th	91 Pa	92 U	93 Np	94 Pu	95 Am	96 Cm	97 Bk	98 Cf	99 Es	100 Fm	101 Md	102 No	103 Lr

Semiconductor Substrate and Dopants

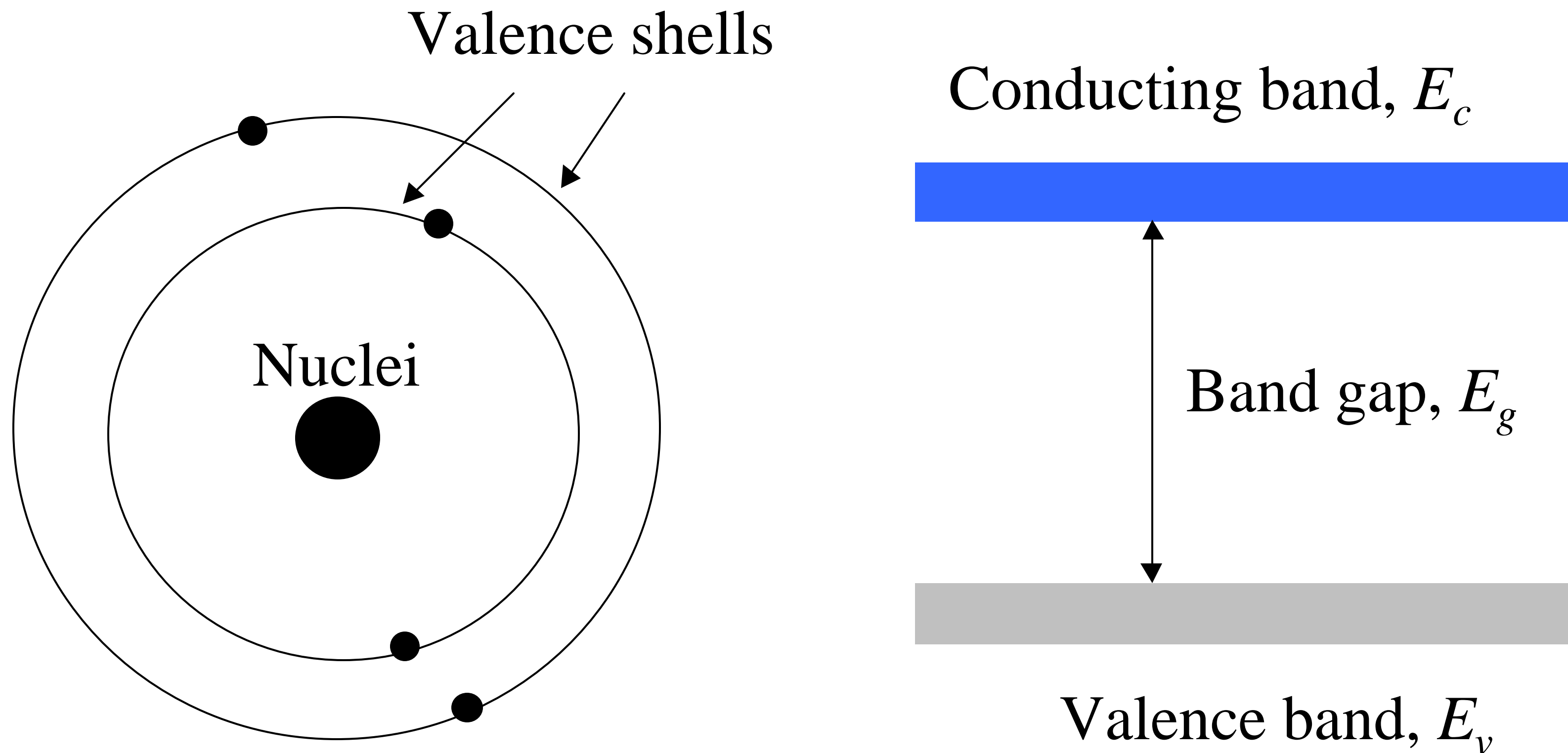
Substrate

P-type Dopant

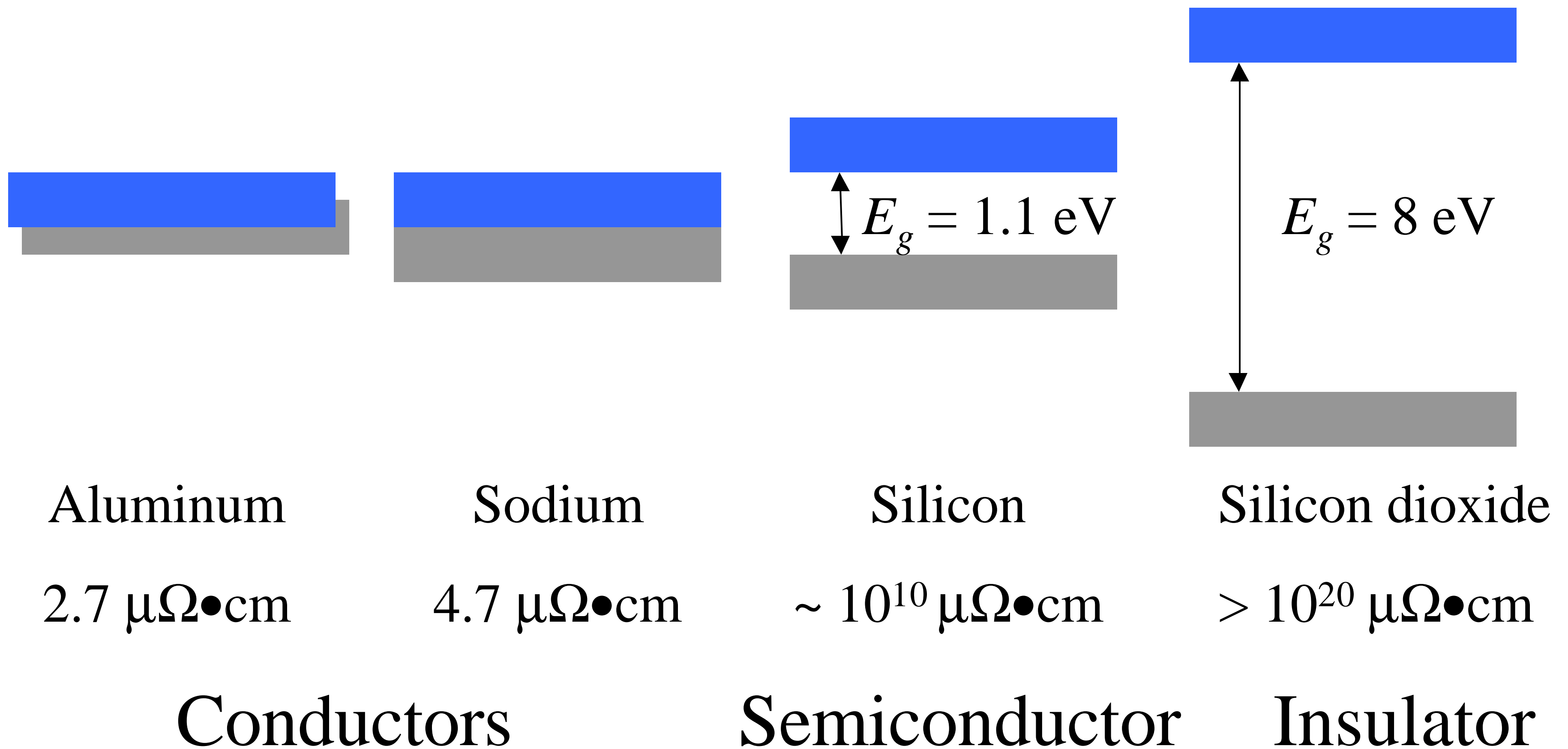
IIIA	IVA	VA	VIA	VIIA
	6 C	7 N	8 O	9 F
13 Al			16 S	17 Cl
31 Ga	32 Ge		34 Se	35 Br

N-type Dopants

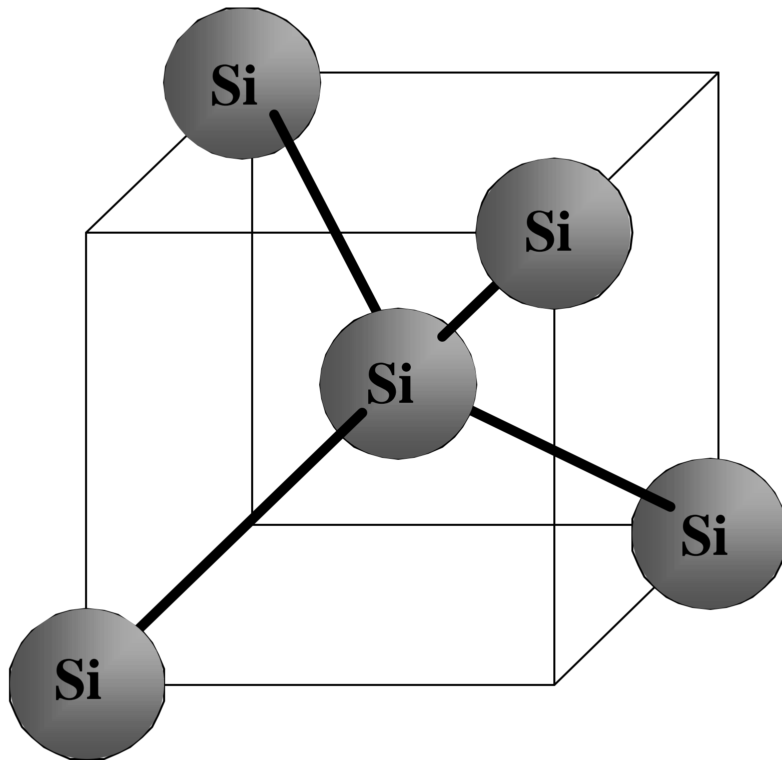
Orbital and Energy Band Structure of an Atom

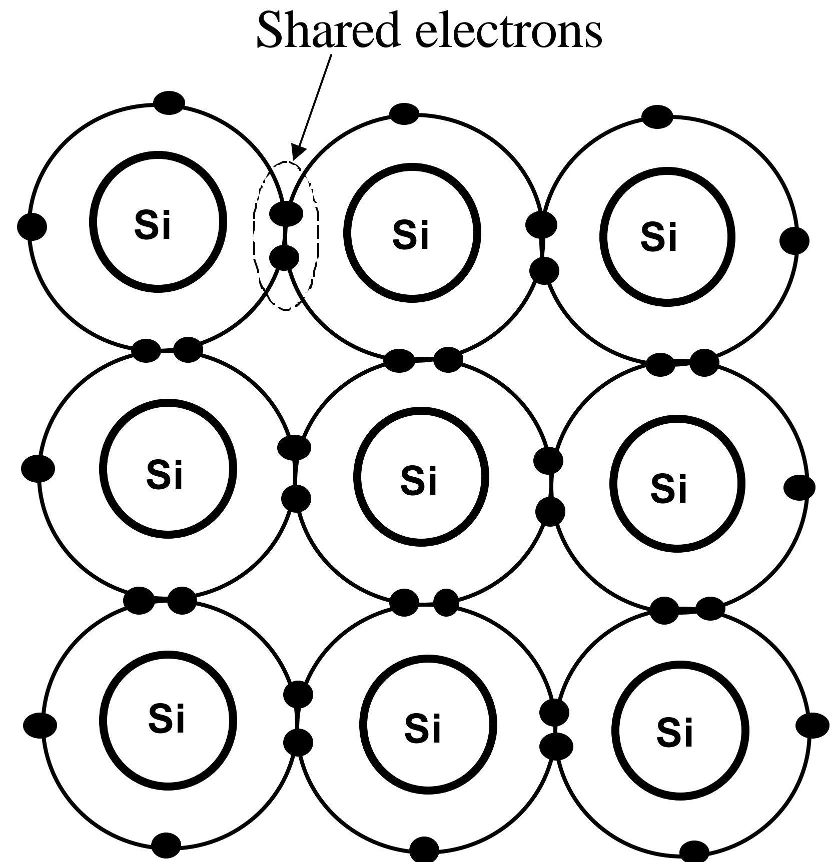


Band Gap and Resistivity



Crystal Structure of Single Crystal Silicon

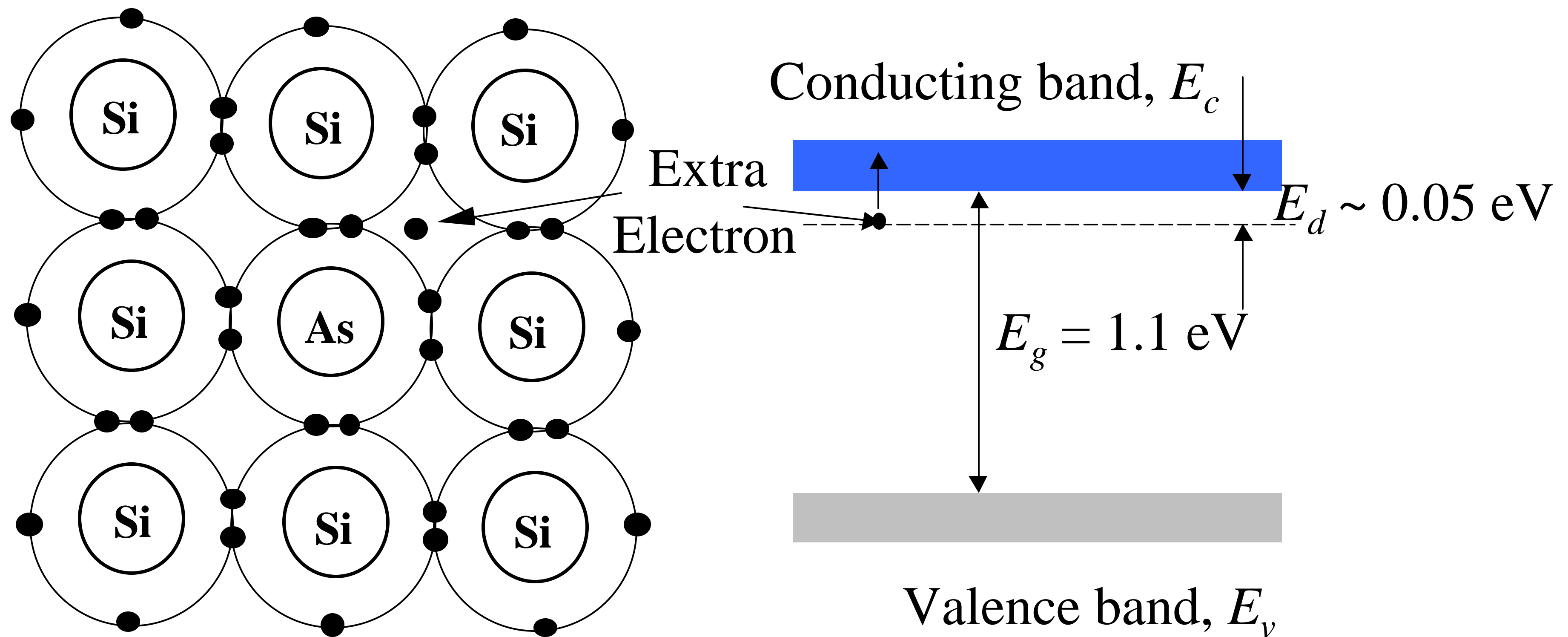




Why Silicon

- Abundant, inexpensive
- Thermal stability
- Silicon dioxide is a strong dielectric and relatively easy to form
- Silicon dioxide can be used as diffusion doping mask

N-type (Arsenic) Doped Silicon and Its Donor Energy Band



P-type (Boron) Doped Silicon and Its Donor Energy Band

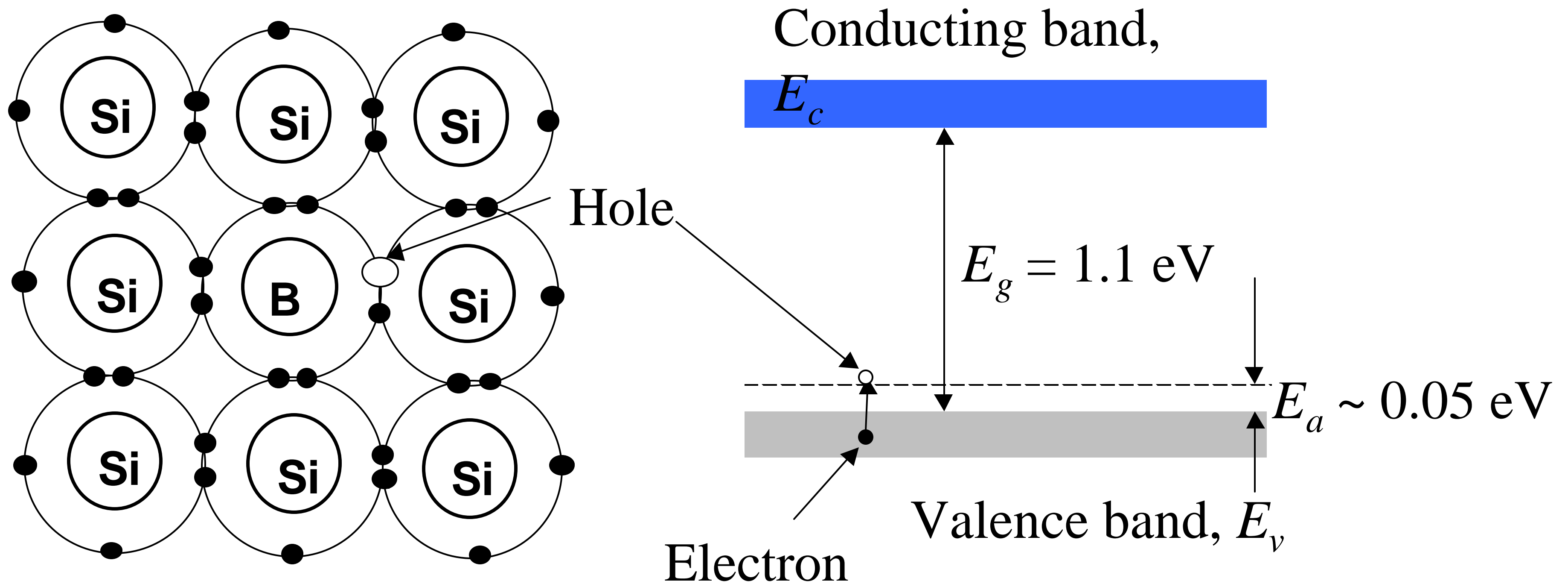
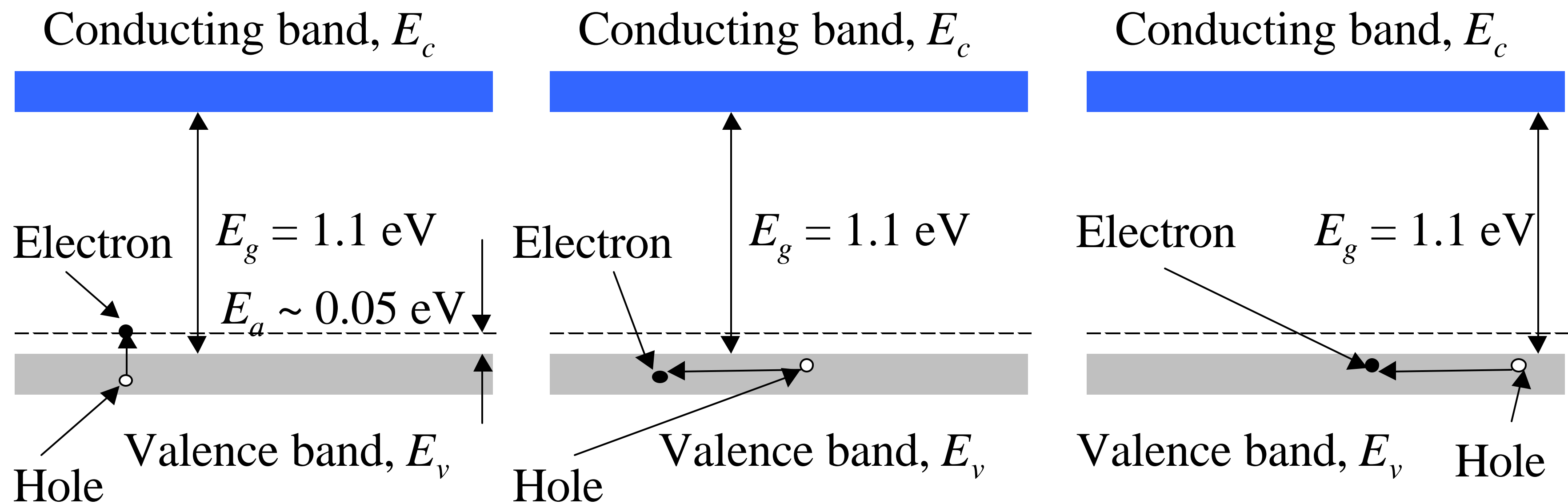
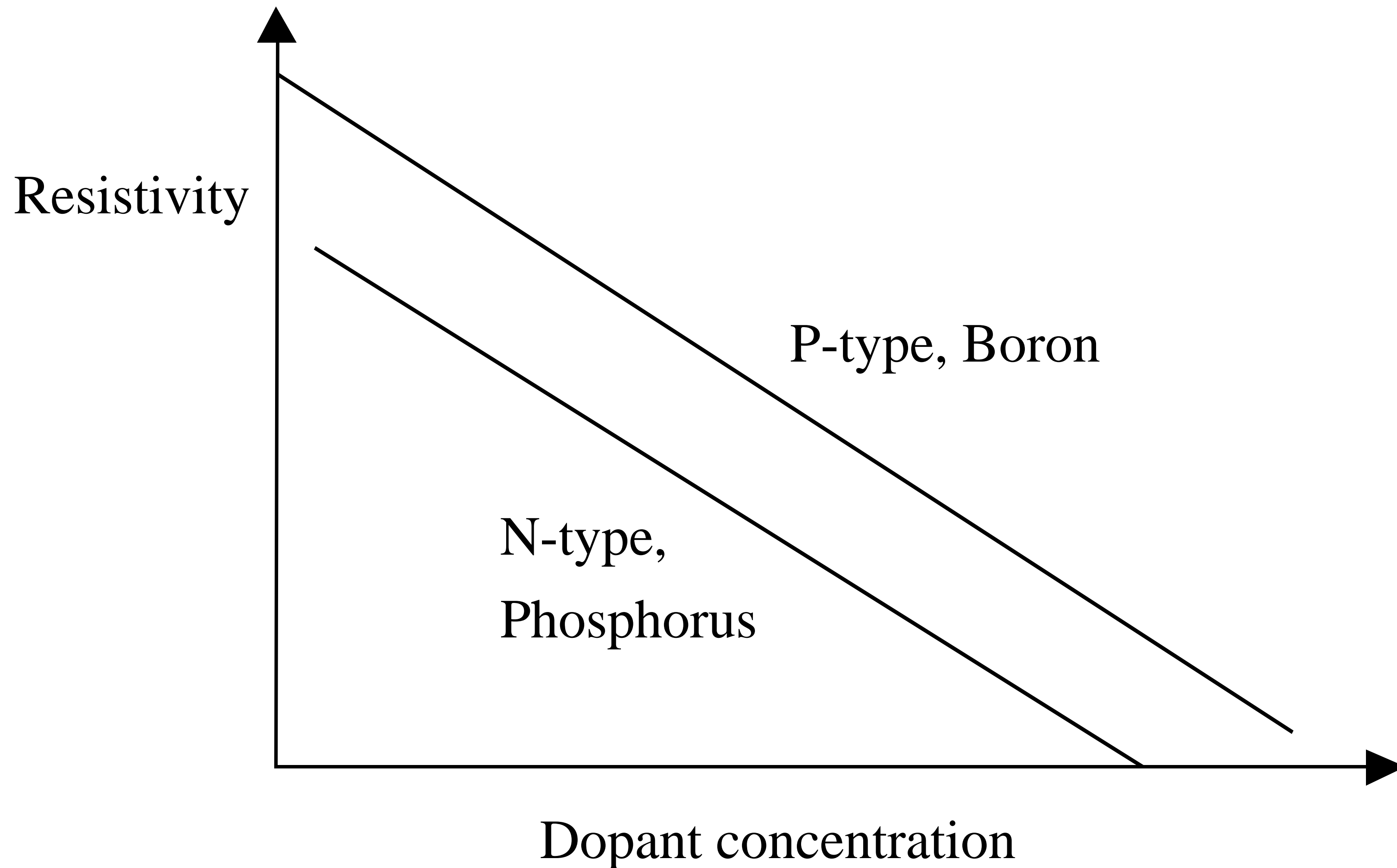


Illustration of Hole Movement



Dopant Concentration and Resistivity



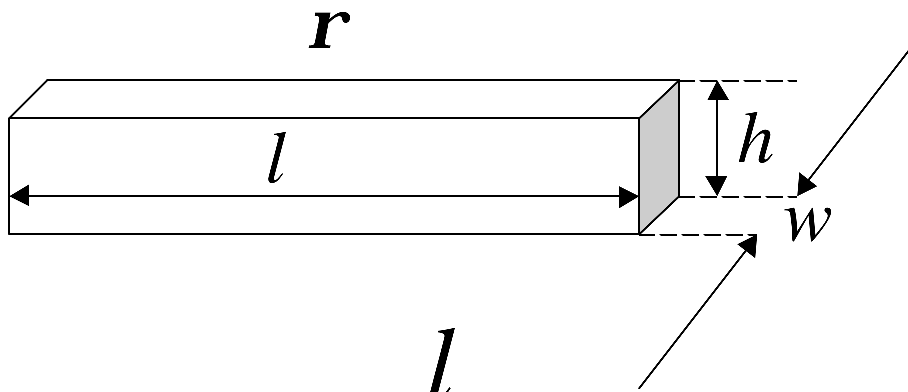
Dopant Concentration and Resistivity

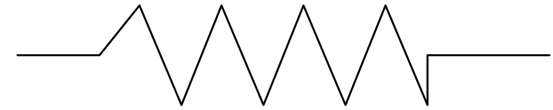
- Higher dopant concentration, more carriers (electrons or holes)
- Higher conductivity, lower resistivity
- Electrons move faster than holes
- N-type silicon has lower resistivity than p-type silicon at the same dopant concentration

Basic Devices

- Resistor
- Capacitor
- Diode
- Bipolar Transistor
- MOS Transistor

Resistor





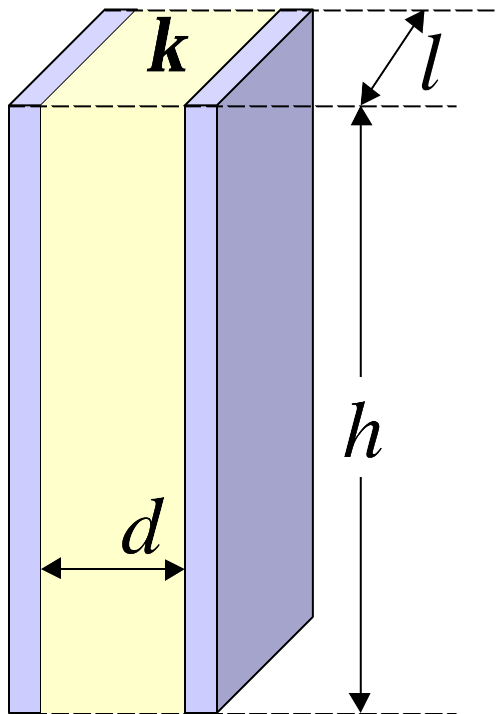
$$R = \rho \frac{l}{wh}$$

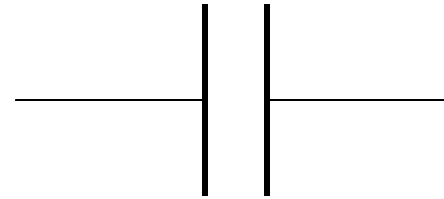
ρ: Resistivity

Resistor

- Resistors are made by doped silicon or polysilicon on an IC chip
- Resistance is determined by length, line width, height, and dopant concentration

Capacitors





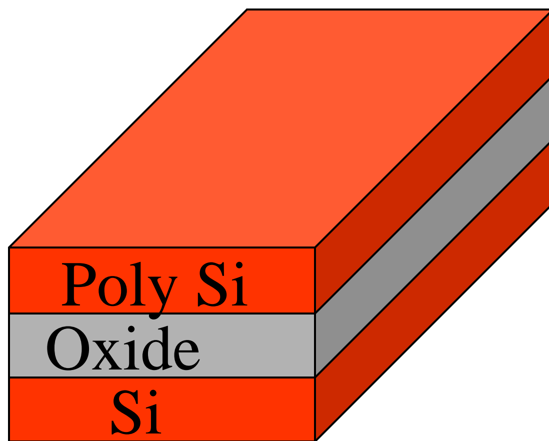
$$C = \boldsymbol{k}\frac{hl}{d}$$

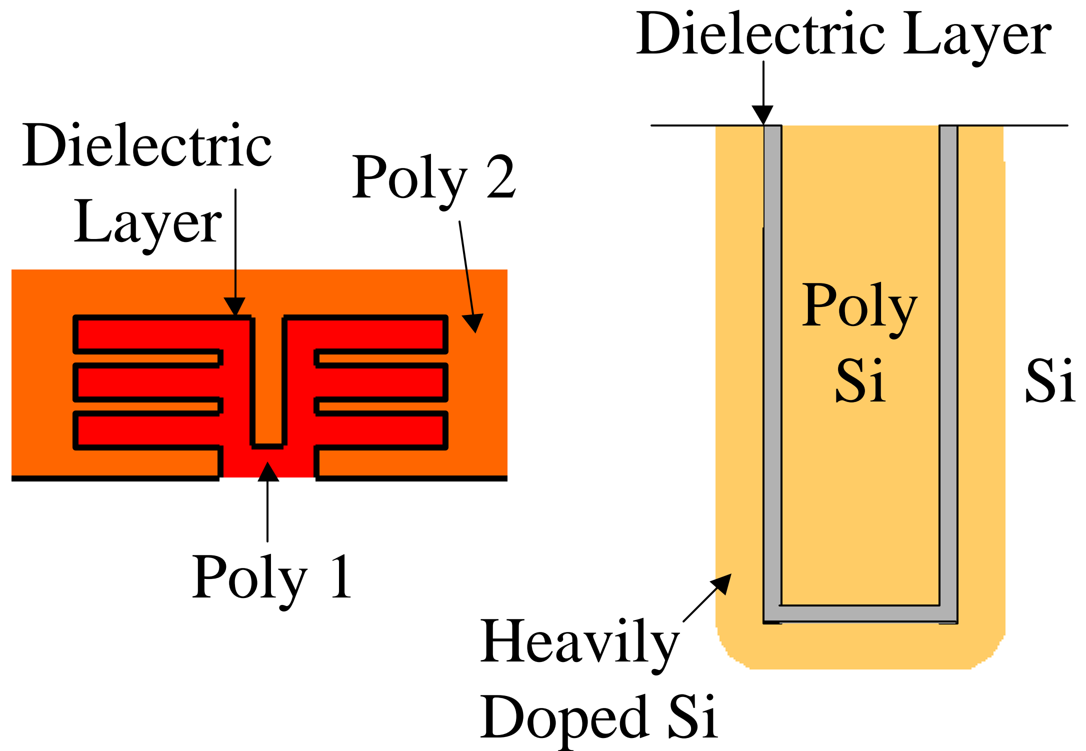
k: Dielectric Constant

Capacitors

- Charge storage device
- Memory Devices, esp. DRAM
- Challenge: reduce capacitor size while keeping the capacitance
- High-κ dielectric materials

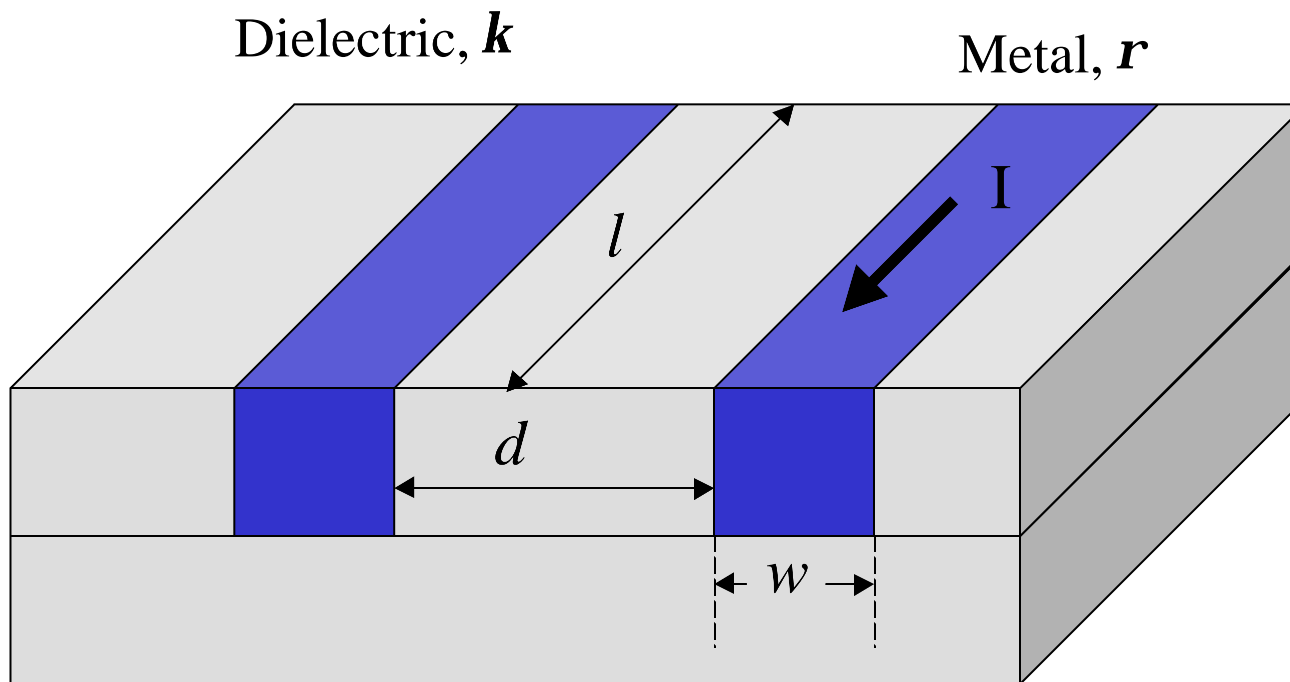
Capacitors





Parallel plate | Stacked | Deep Trench

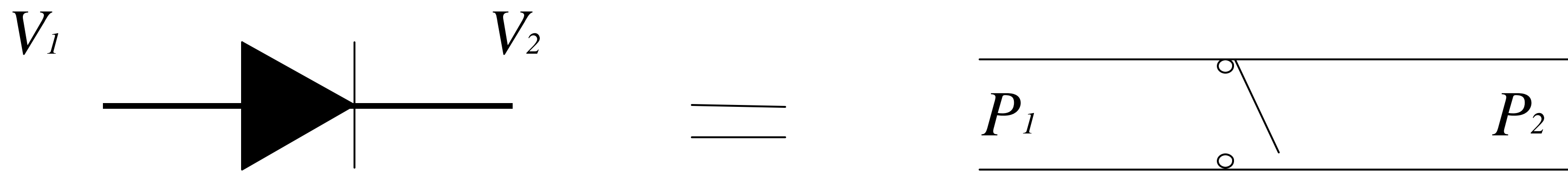
Metal Interconnection and RC Delay



Diode

- P-N Junction
- Allows electric current go through only when it is positively biased.

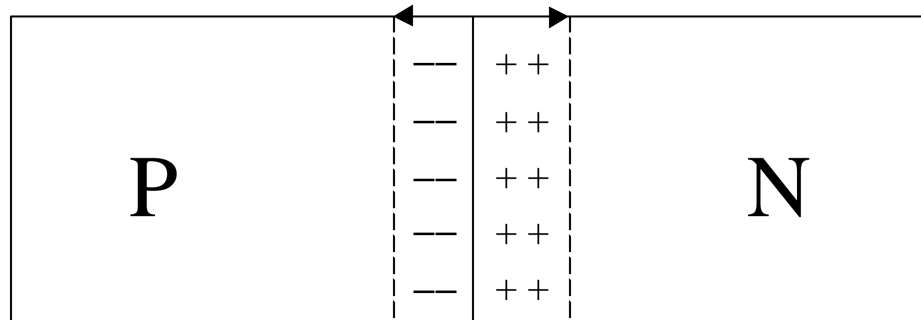
Diode

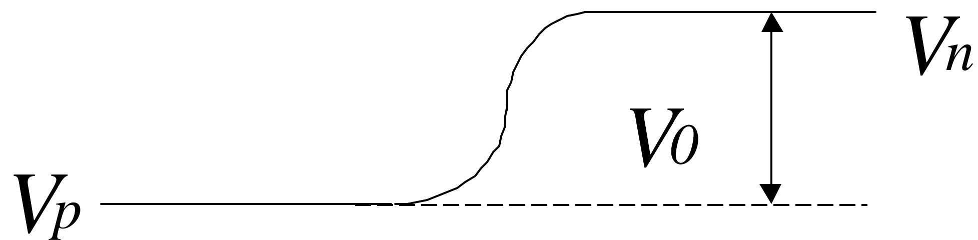


- $V_1 > V_2$, current →
- $V_1 < V_2$, no current

- $P_1 > P_2$, current →
- $P_1 < P_2$, no current

Figure 3.14



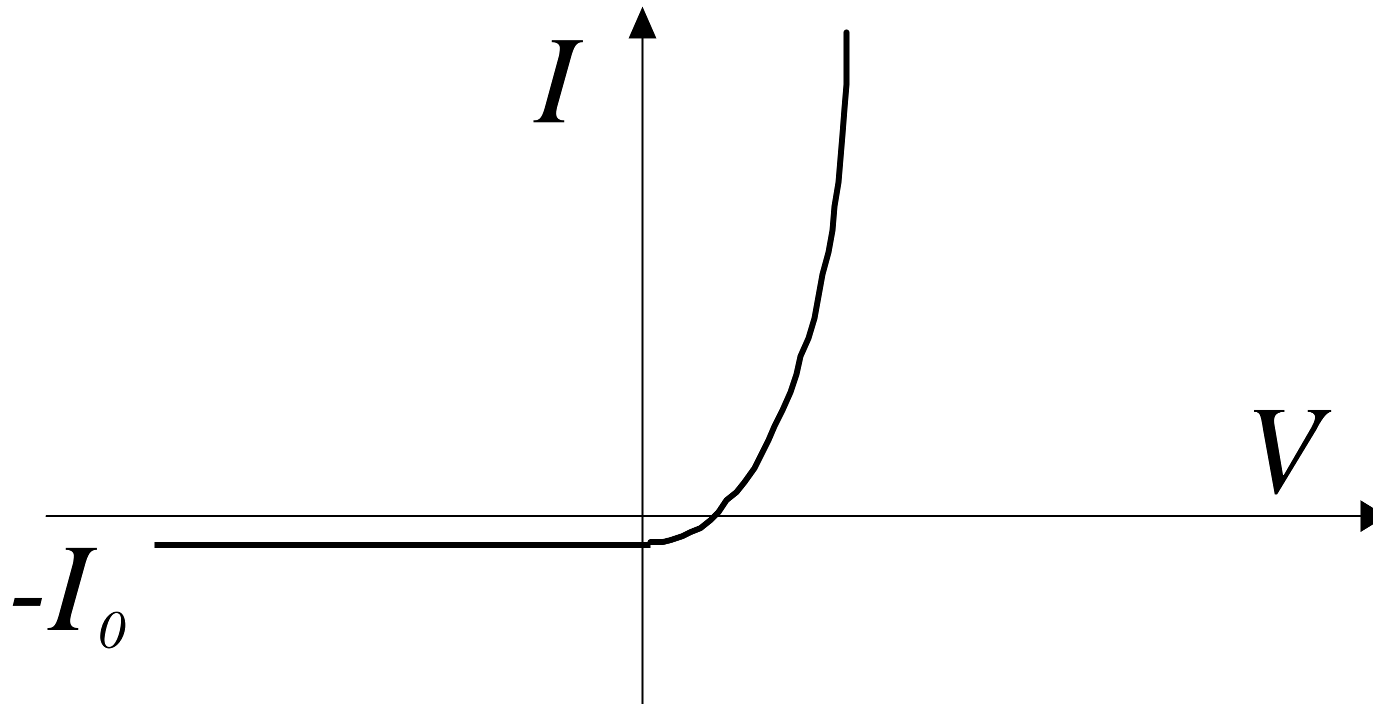


Intrinsic Potential

$$V_0 = \frac{kT}{q} \ln \frac{N_a N_d}{n_i^2}$$

- For silicon $V_0 \sim 0.7$ V

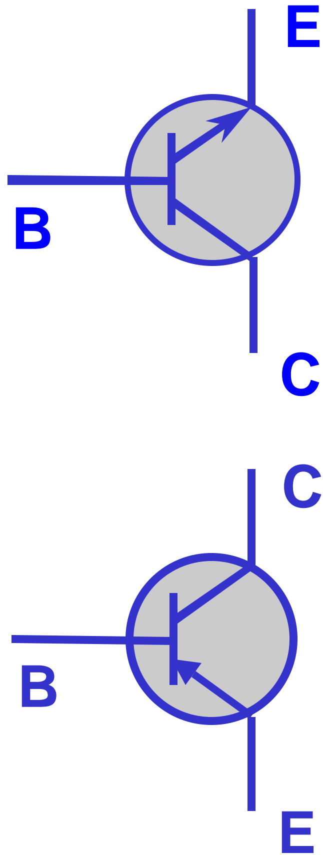
I-V Curve of Diode

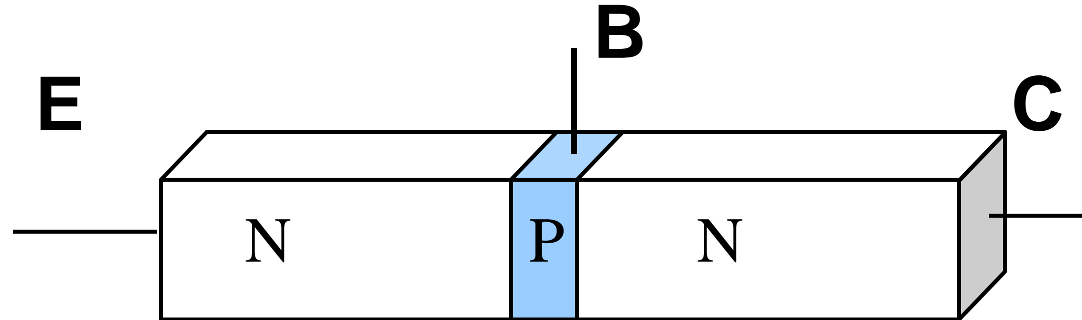


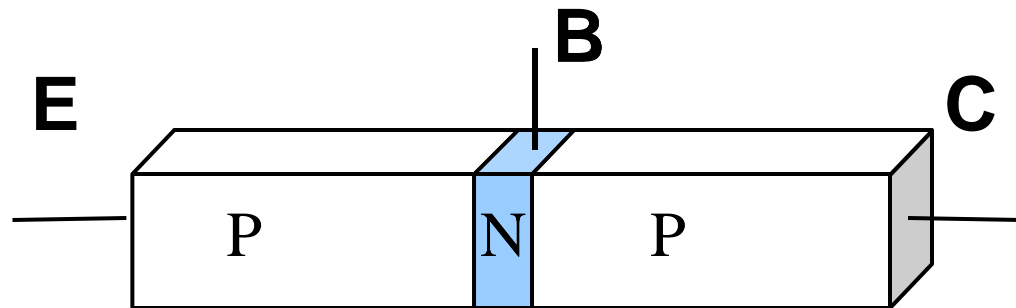
Bipolar Transistor

- PNP or NPN
- Switch
- Amplifier
- Analog circuit
- Fast, high power device

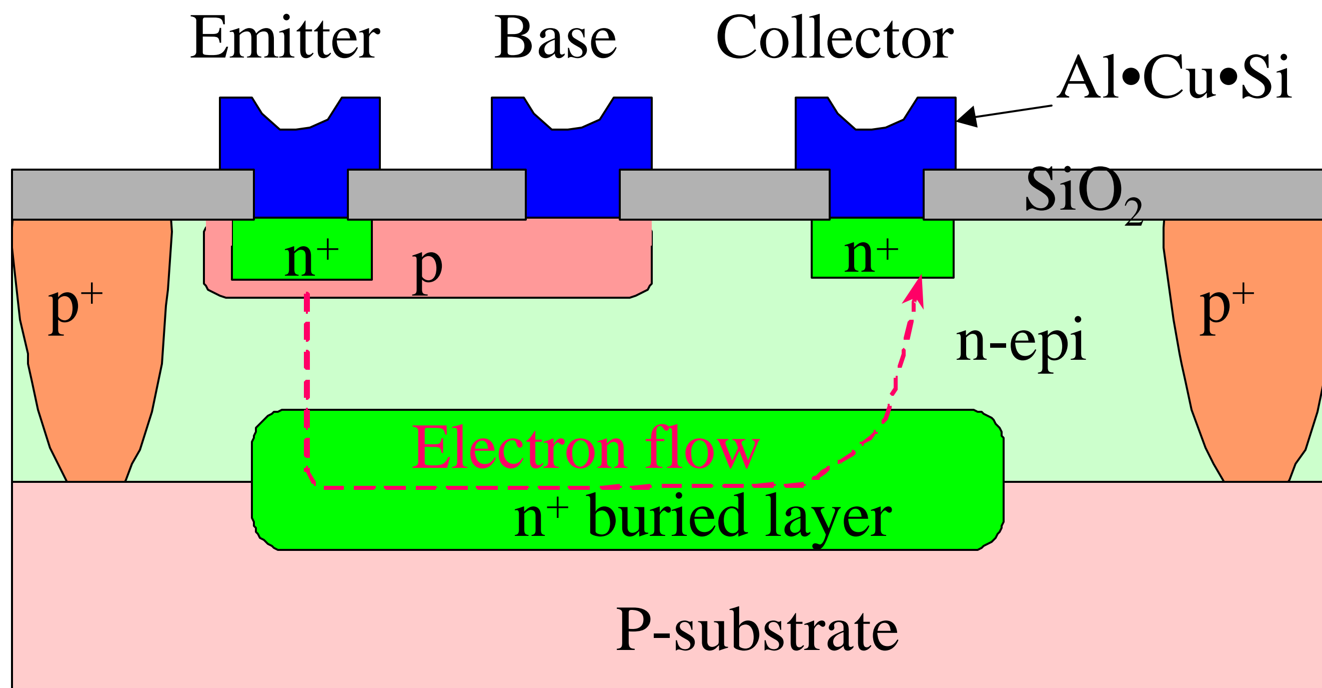
NPN and PNP Transistors







NPN Bipolar Transistor



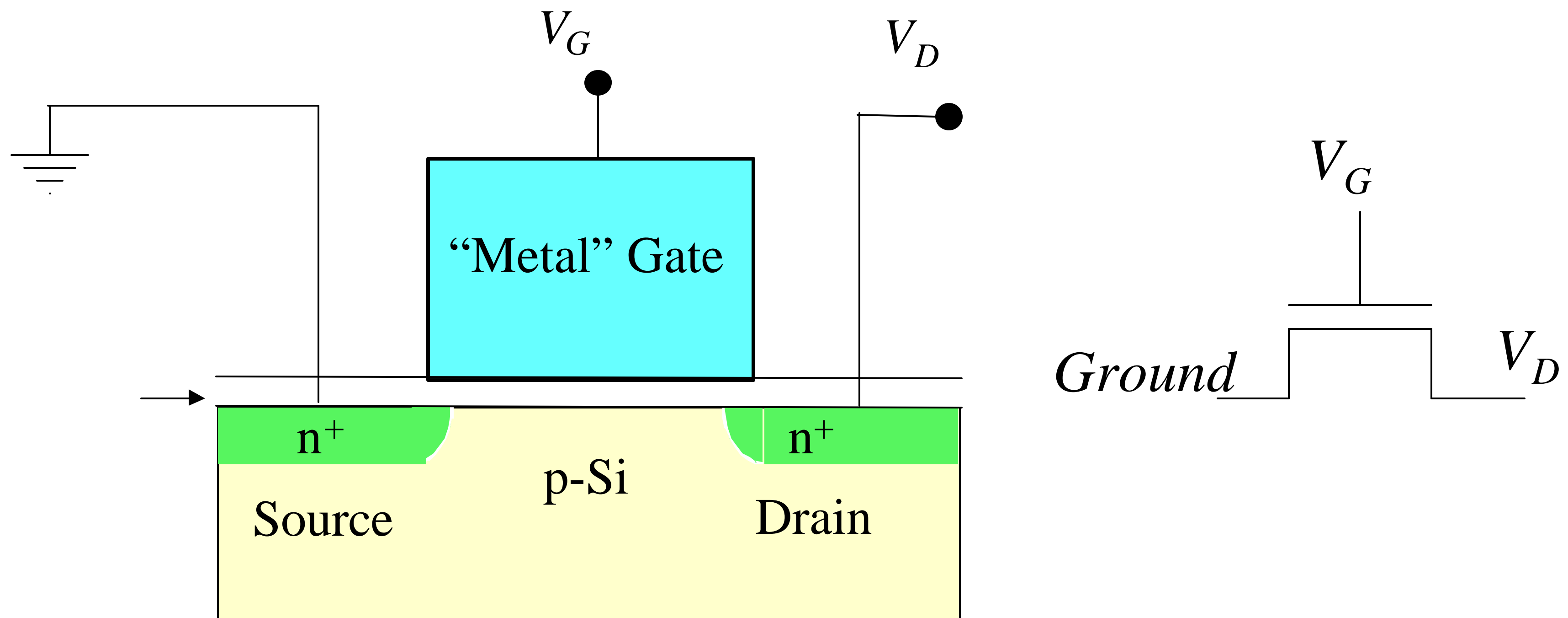
Sidewall Base Contact NPN Bipolar Transistor

Metal
CVD oxide
Base
Emitter
CVD oxide
CVD oxide
Collector
Poly
p
n^+
p
Field oxide
n Epi
Field oxide
n^+
Field oxide
n^+ Buried Layer
P-substrate

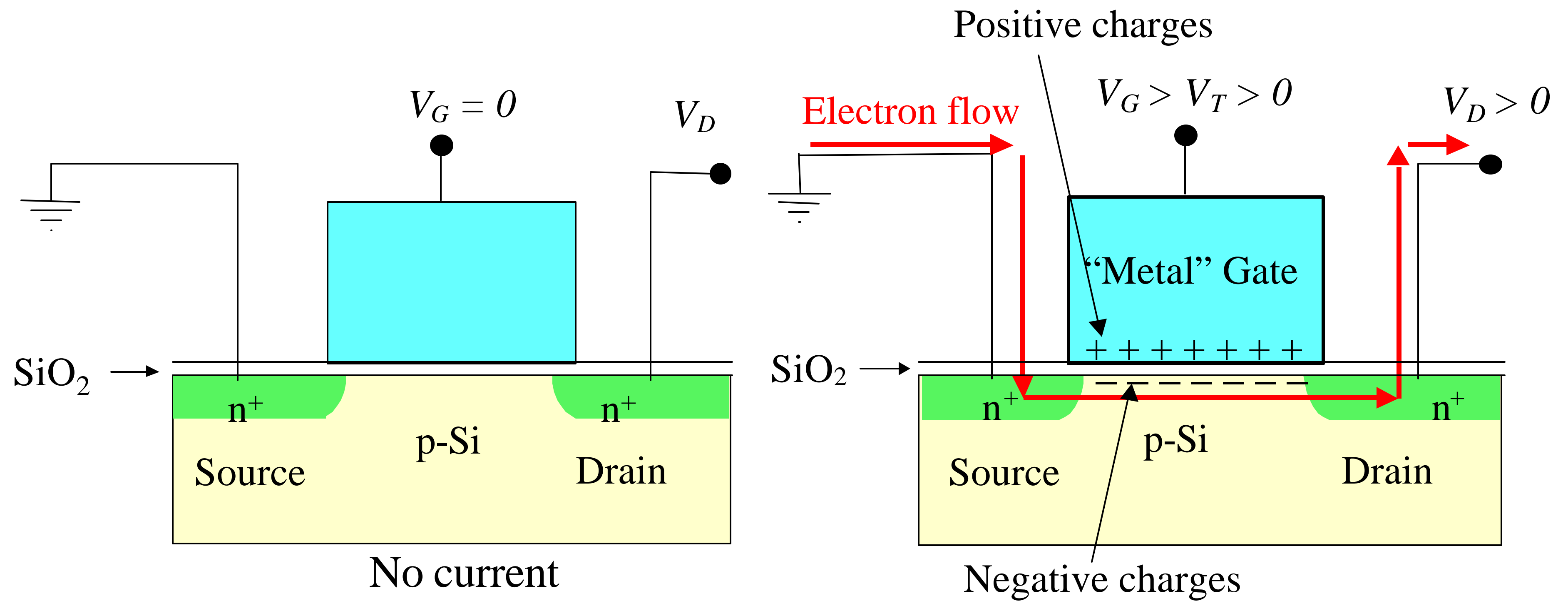
MOS Transistor

- Metal-oxide-semiconductor
- Also called MOSFET (MOS Field Effect Transistor)
- Simple, symmetric structure
- Switch, good for digital, logic circuit
- Most commonly used devices in the semiconductor industry

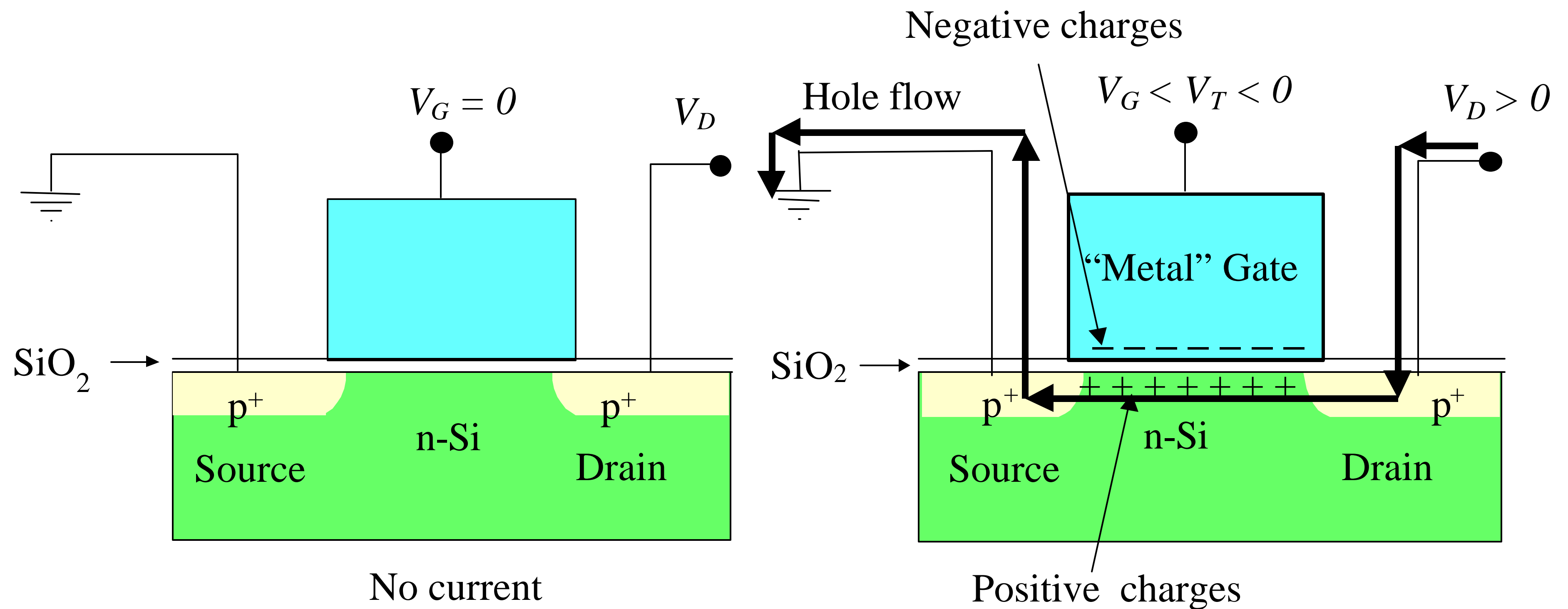
NMOS Device
Basic Structure



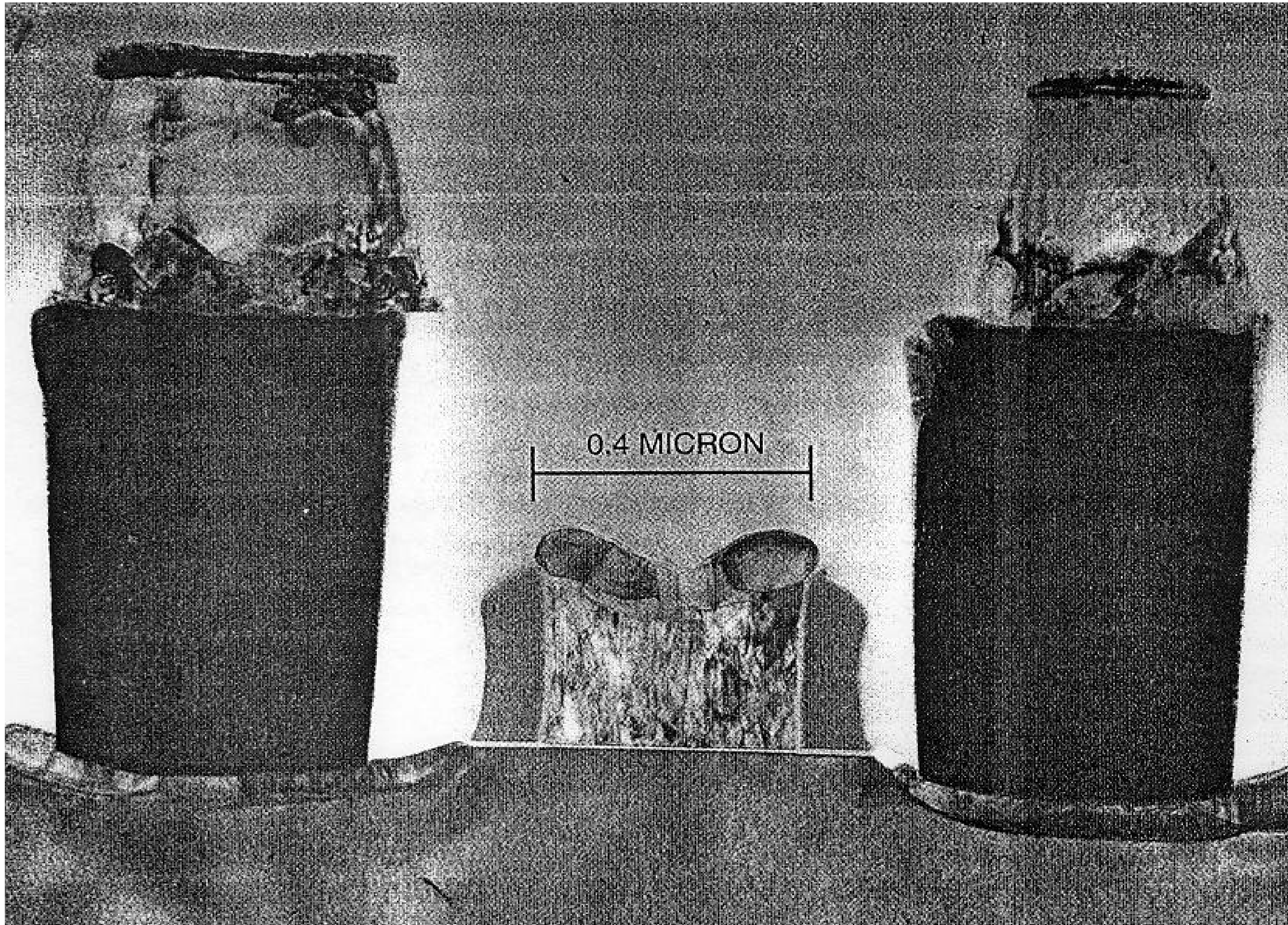
NMOS Device



PMOS Device



MOSFET



MOSFET and Drinking Fountain

MOSFET	**Drinking Fountain**
• Source, drain, gate	• Source, drain, gate valve
• Source/drain biased	• Pressurized source
• Voltage on gate to turn-on	• Pressure on gate (button) to turn-on
• Current flow between source and drain	• Current flow between source and drain

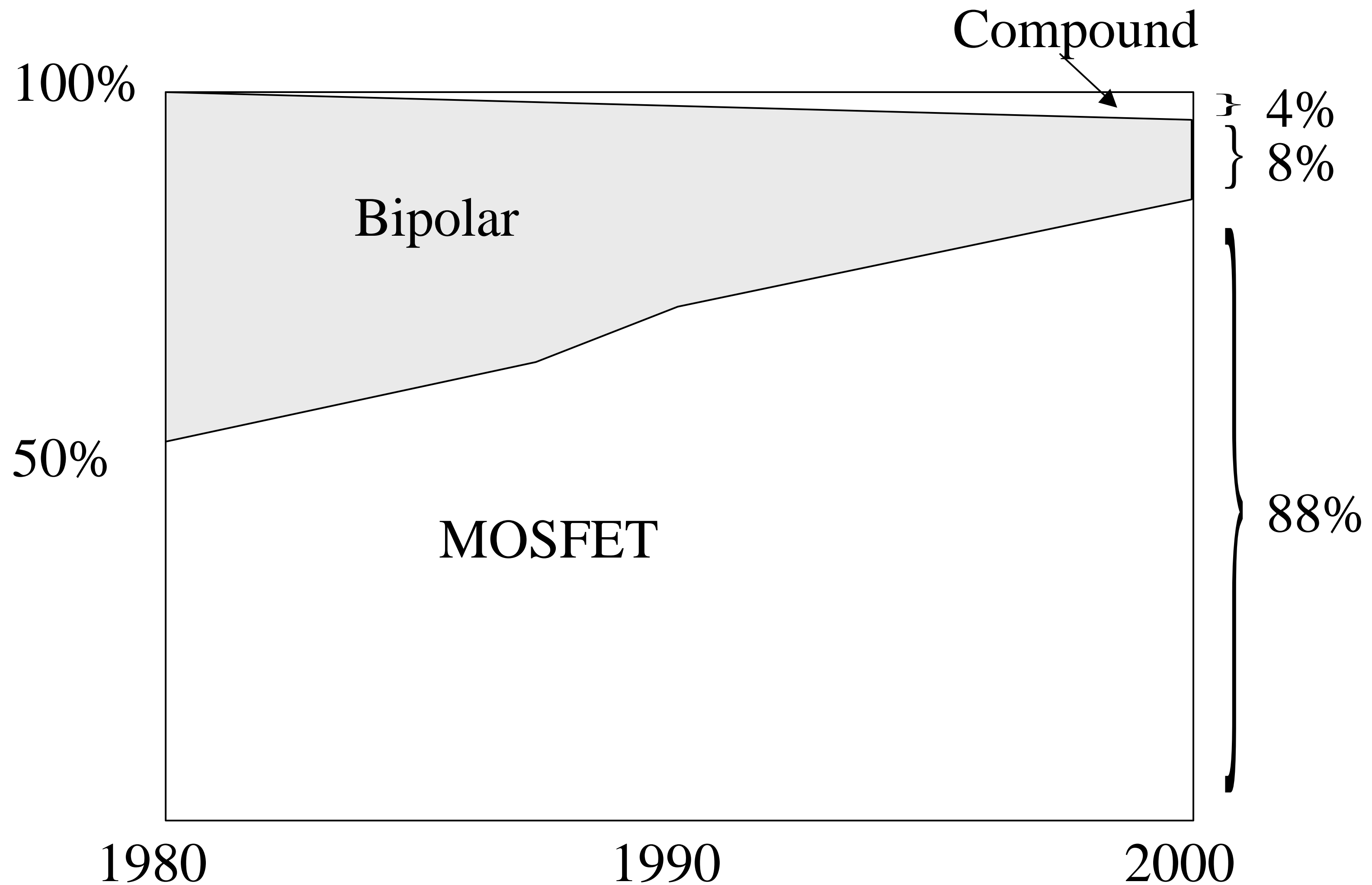
Basic Circuits

- Bipolar
- PMOS
- NMOS
- **CMOS**
- BiCMOS

Devices with Different Substrates

Silicon	• Bipolar • MOSFET • BiCMOS	Dominate IC industry
Germanium	• Bipolar: high speed devices	
Compound	• GaAs: up to 20 GHz device • Light emission diode (LED)	

Market of Semiconductor Products



Bipolar IC

- Earliest IC chip
- 1961, four bipolar transistors, $150.00
- Market share reducing rapidly
- Still used for analog systems and power devices
- TV, VCR, Cellar phone, etc.

PMOS

- First MOS field effect transistor, 1960
- Used for digital logic devices in the 1960s
- Replaced by NMOS after the mid-1970s

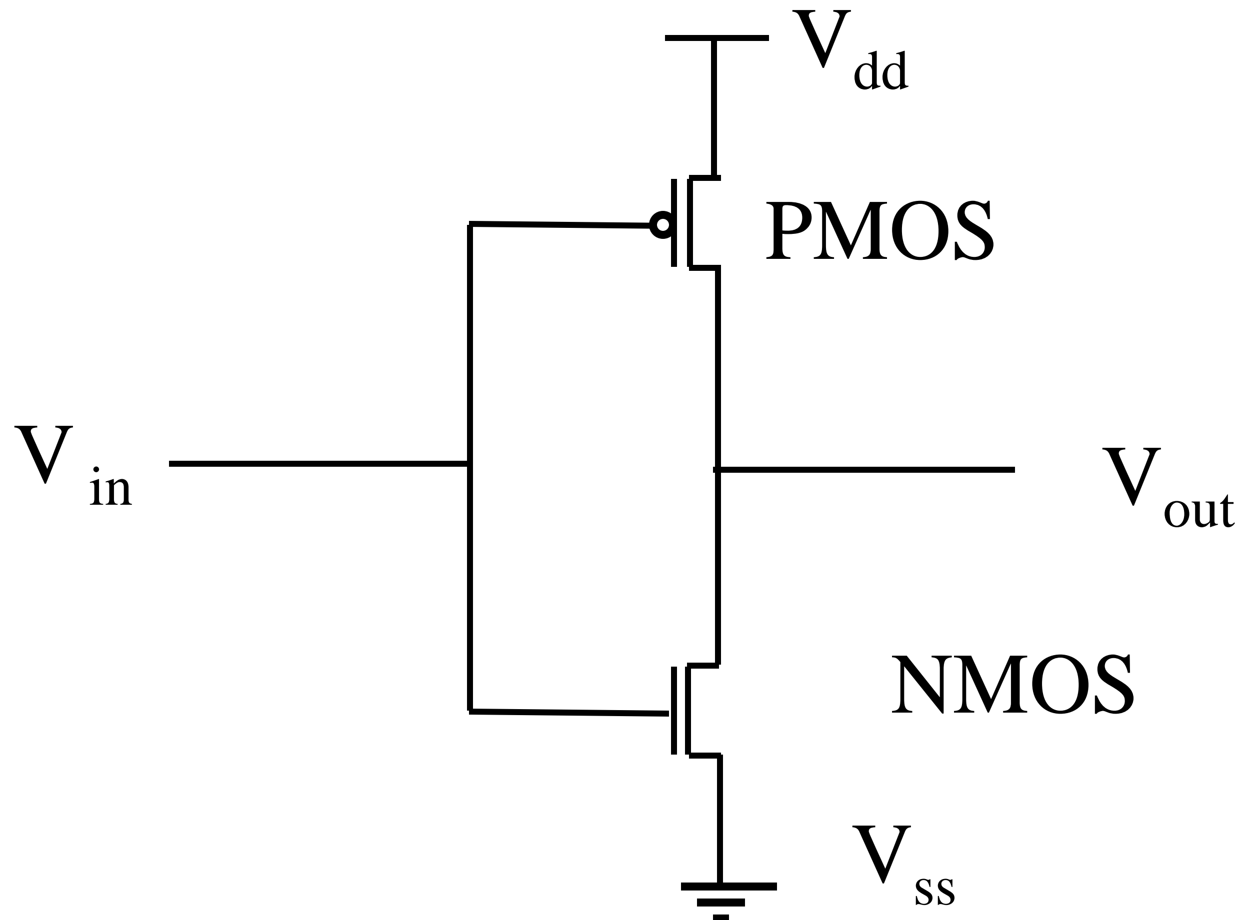
NMOS

- Faster than PMOS
- Used for digital logic devices in 1970s and 1980s
- Electronic watches and hand-hold calculators
- Replaced by CMOS after the 1980s

CMOS

- Most commonly used circuit in IC chip since 1980s
- Low power consumption
- High temperature stability
- High noise immunity
- Symmetric design

CMOS Inverter



CMOS IC

n+ Source/Drain
Gate Oxide
p+ Source/Drain
Polysilicon
p-Si
STI
n-Si
USG
Balk Si

BiCMOS

- Combination of CMOS and bipolar circuits
- Mainly in 1990s
- CMOS as logic circuit
- Bipolar for input/output
- Faster than CMOS
- Higher power consumption
- Likely will have problem when power supply voltage dropping below one volt

IC Chips

- Memory
- Microprocessor
- Application specific IC (ASIC)

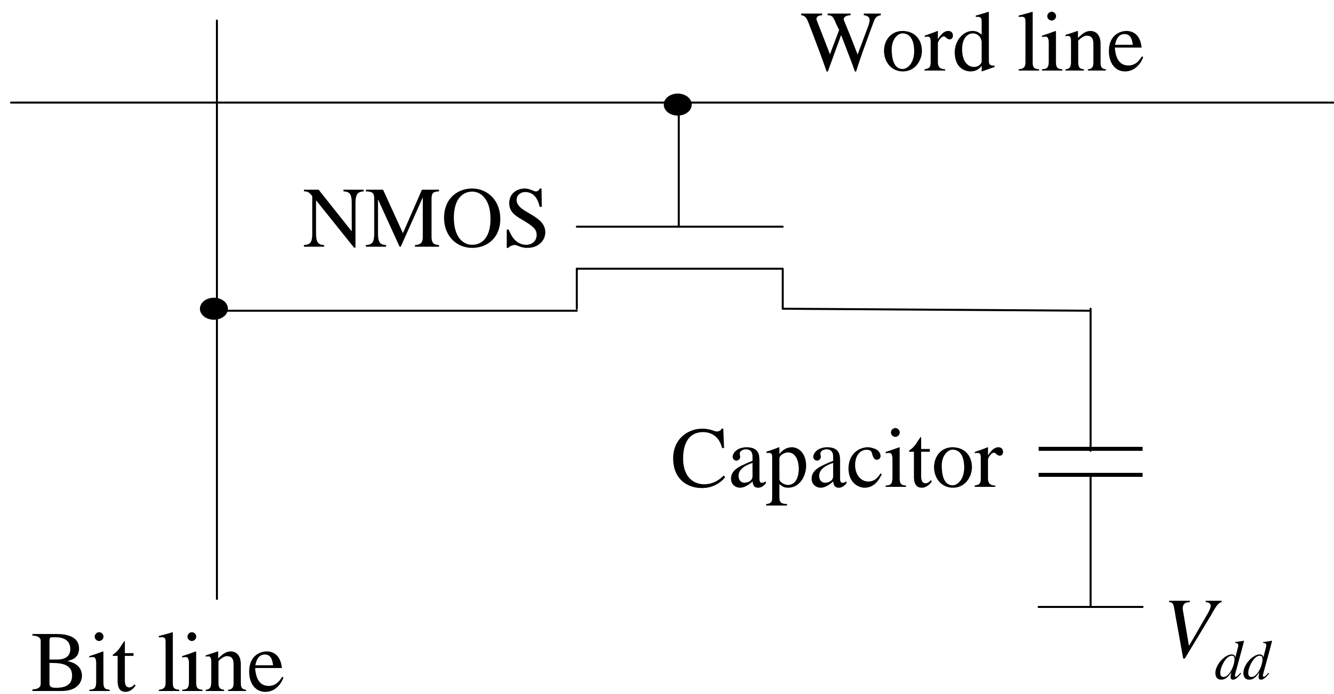
Memory Chips

- Devices store data in the form of electric charge
- Volatile memory
  - Dynamic random access memory (DRAM)
  - S random access memory (SRAM)
- Non-volatile memory
  - Erasable programmable read only memory (EPROM)
  - FLASH

DRAM

- Major component of computer and other electronic instruments for data storage
- Main driving force of IC processing development
- One transistor, one capacitor

Basic DRAM Memory Cell



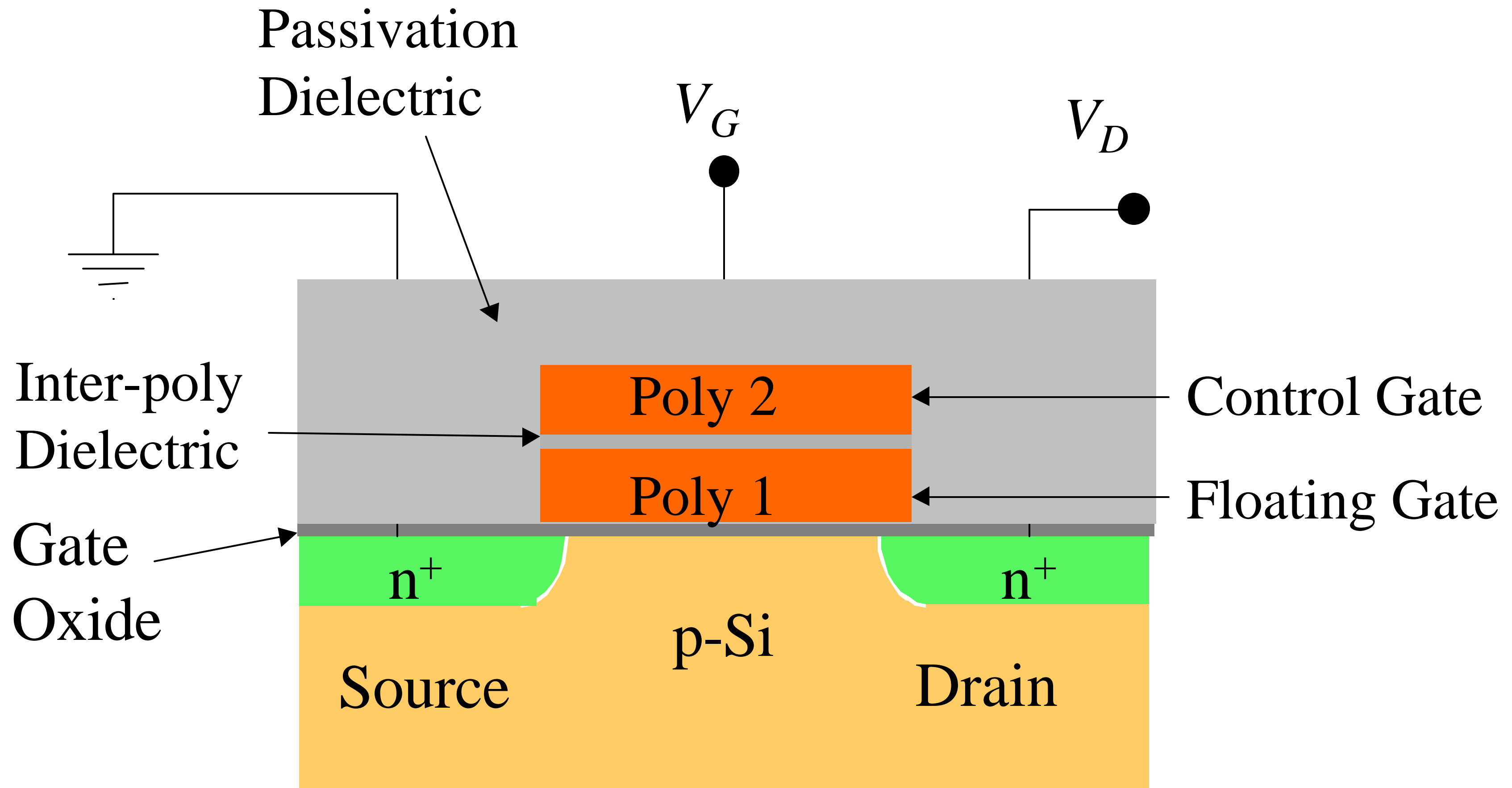
SRAM

- Fast memory application such as computer cache memory to store commonly used instructions
- Unit memory cell consists of six transistors
- Much faster than DRAM
- More complicated processing, more expensive

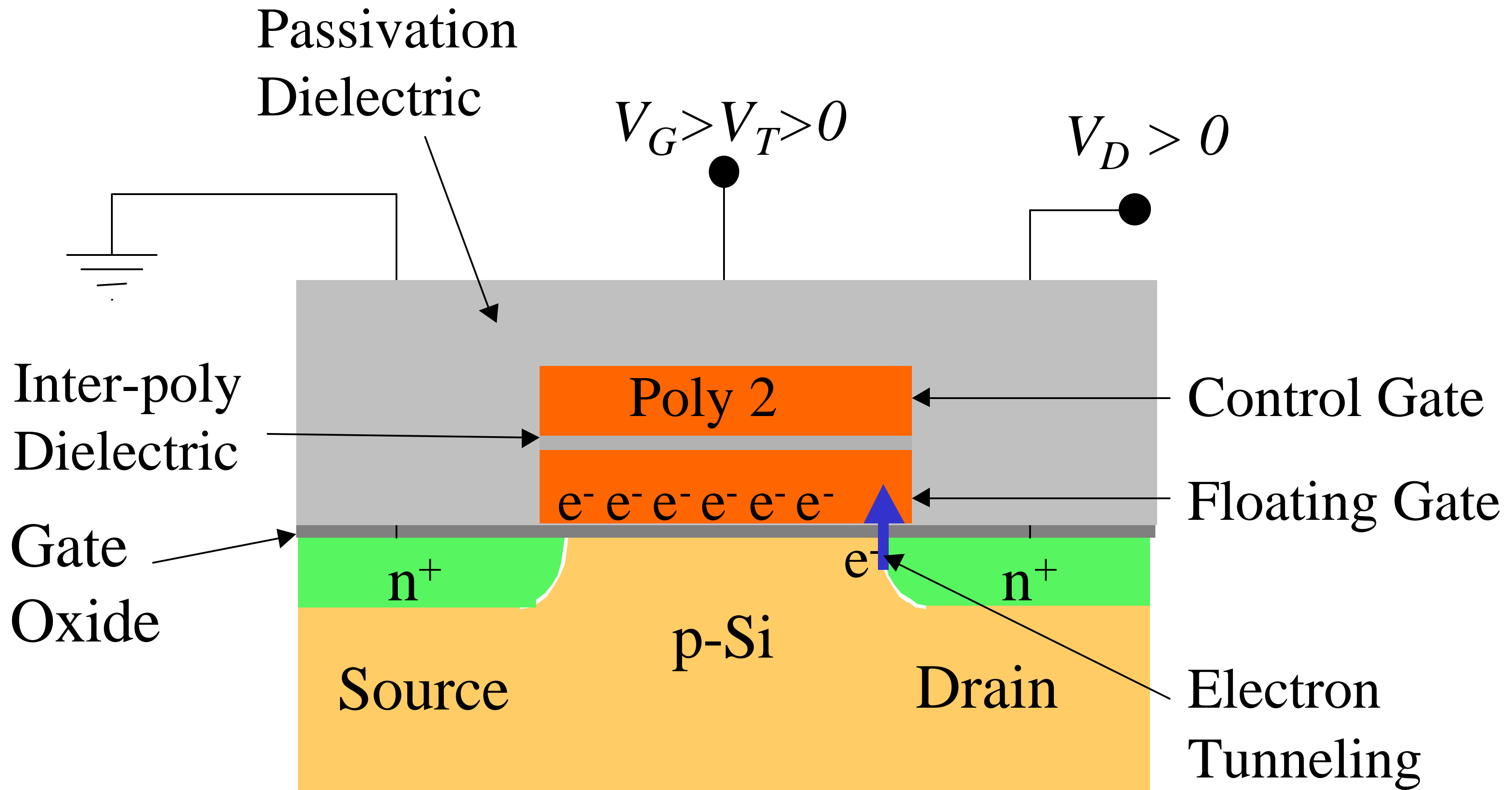
EPROM

- Non-volatile memory
- Keeping data ever without power supply
- Computer bios memory which keeps boot up instructions
- Floating gate
- UV light memory erase

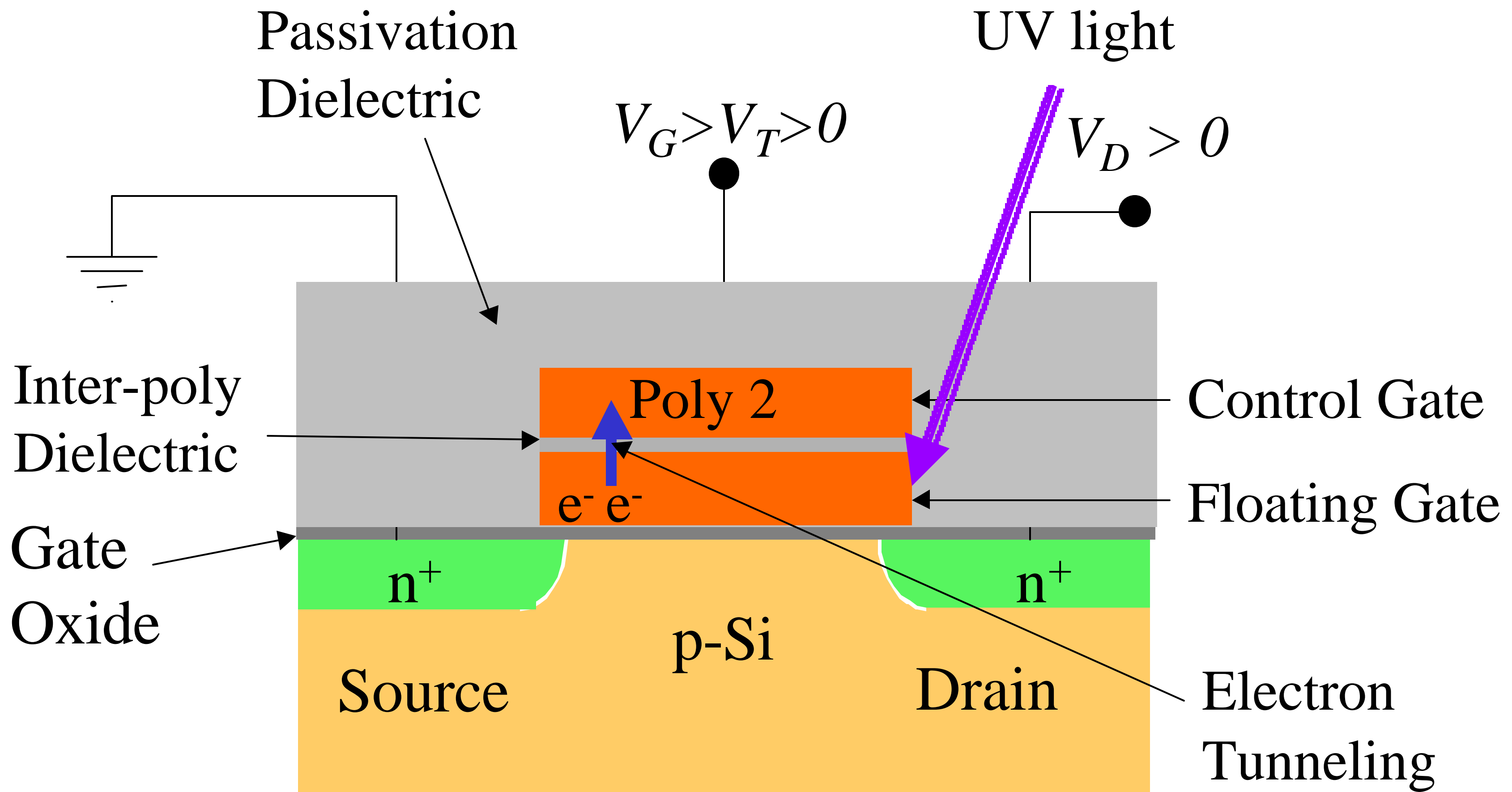
EPROM



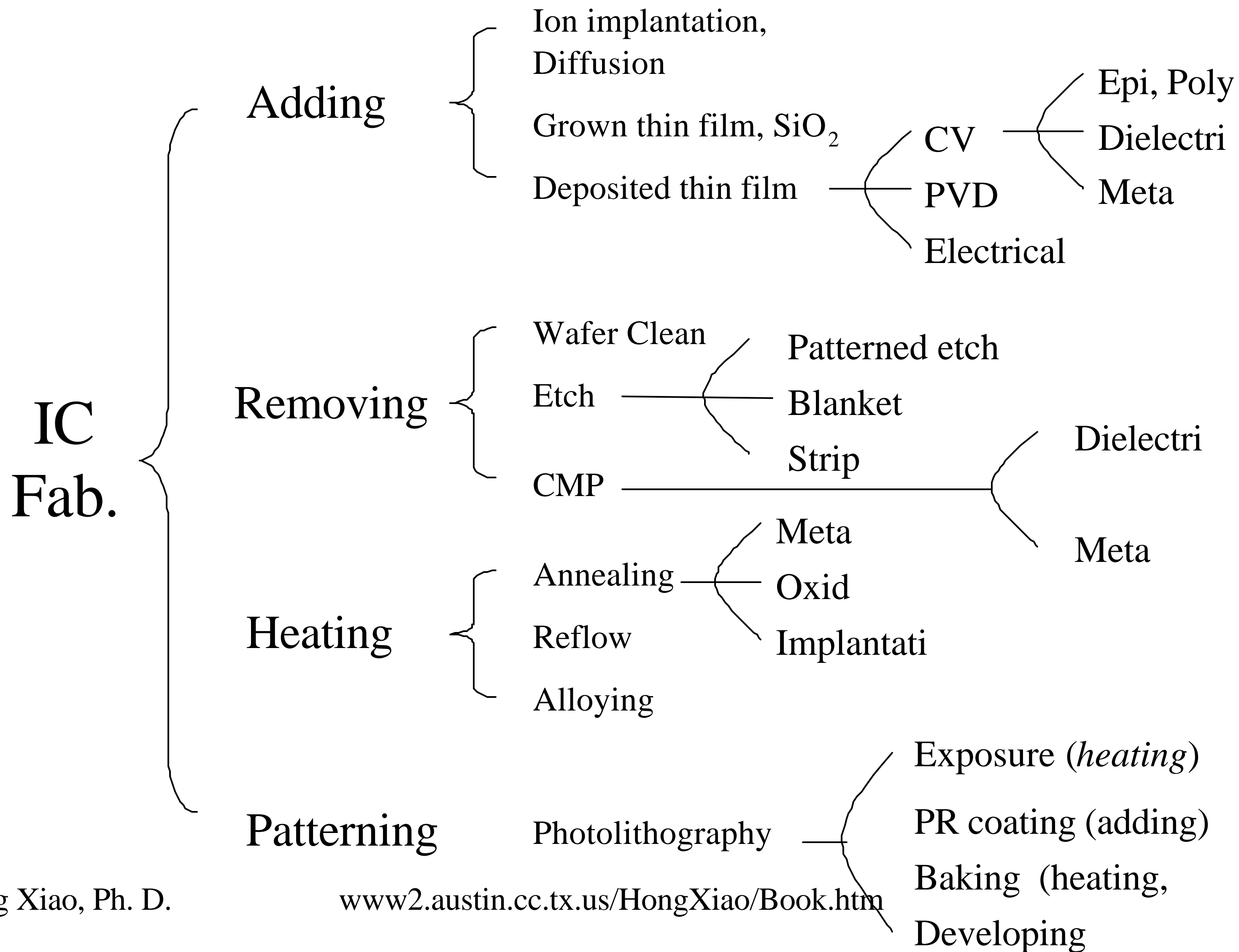
EPROM Programming



EPROM Programming



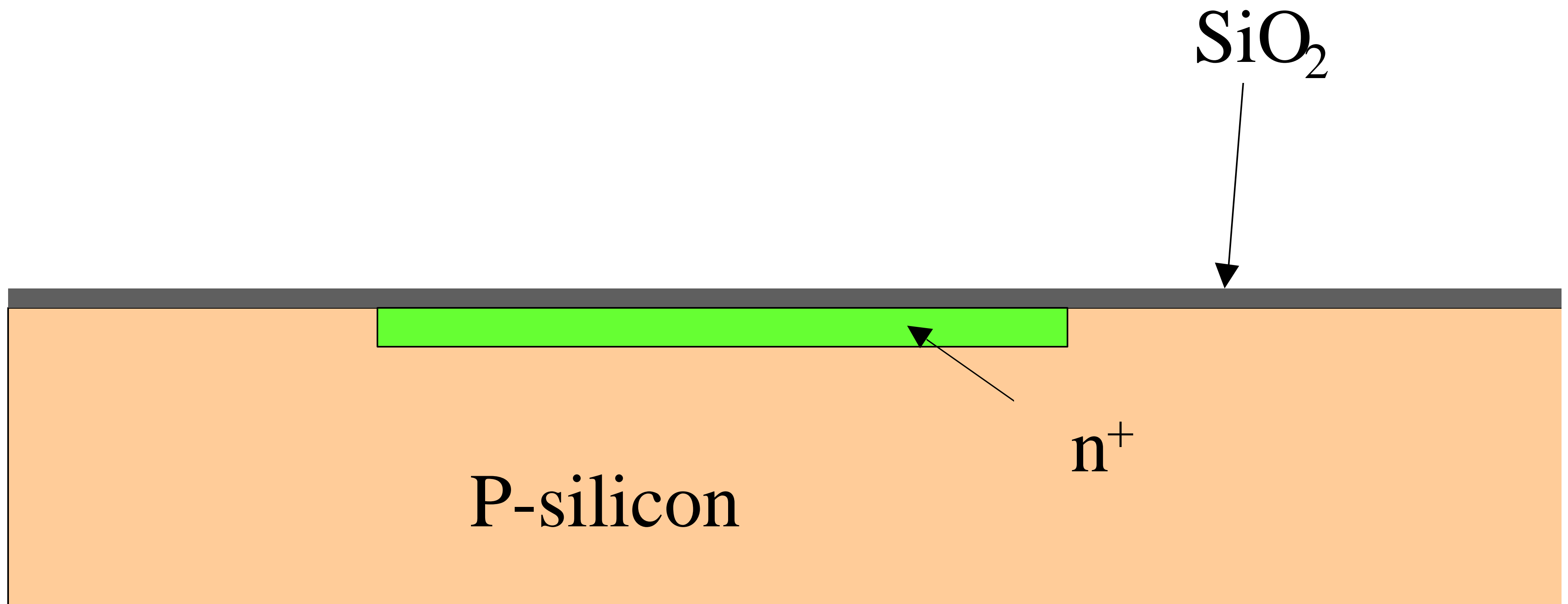
IC Fabrication Processes



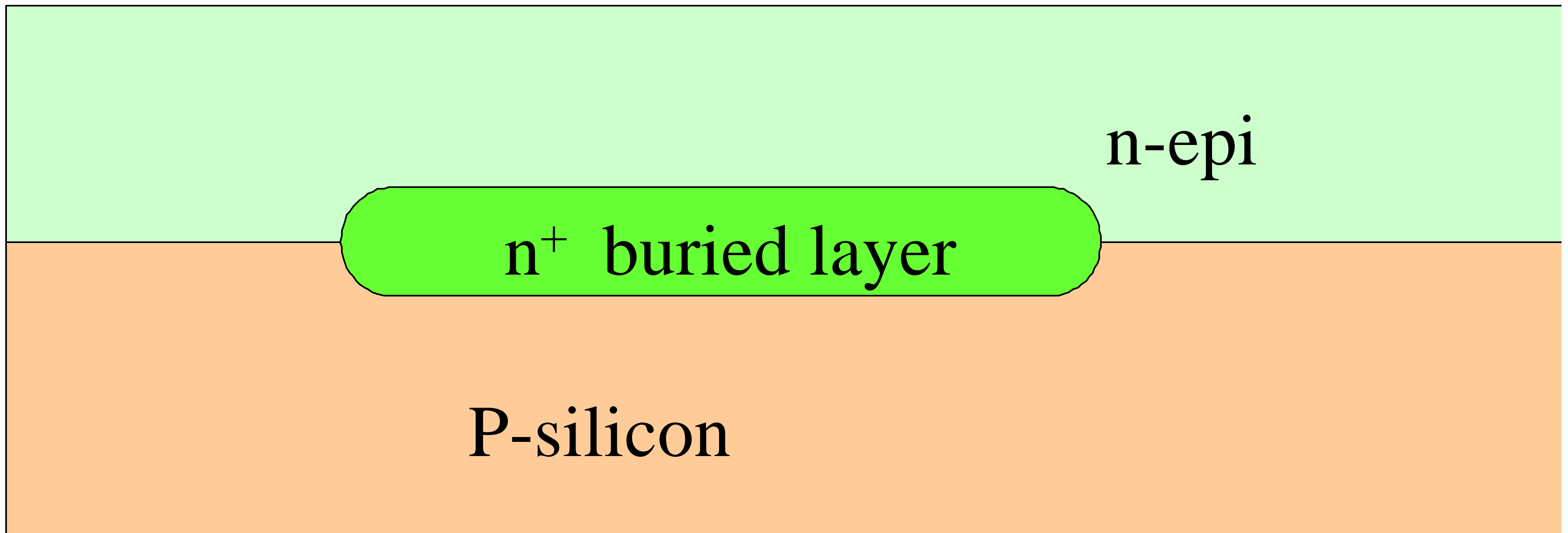
Basic Bipolar Process Steps

- Buried layer doping
- Epitaxial silicon growth
- Isolation and transistor doping
- Interconnection
- Passivation

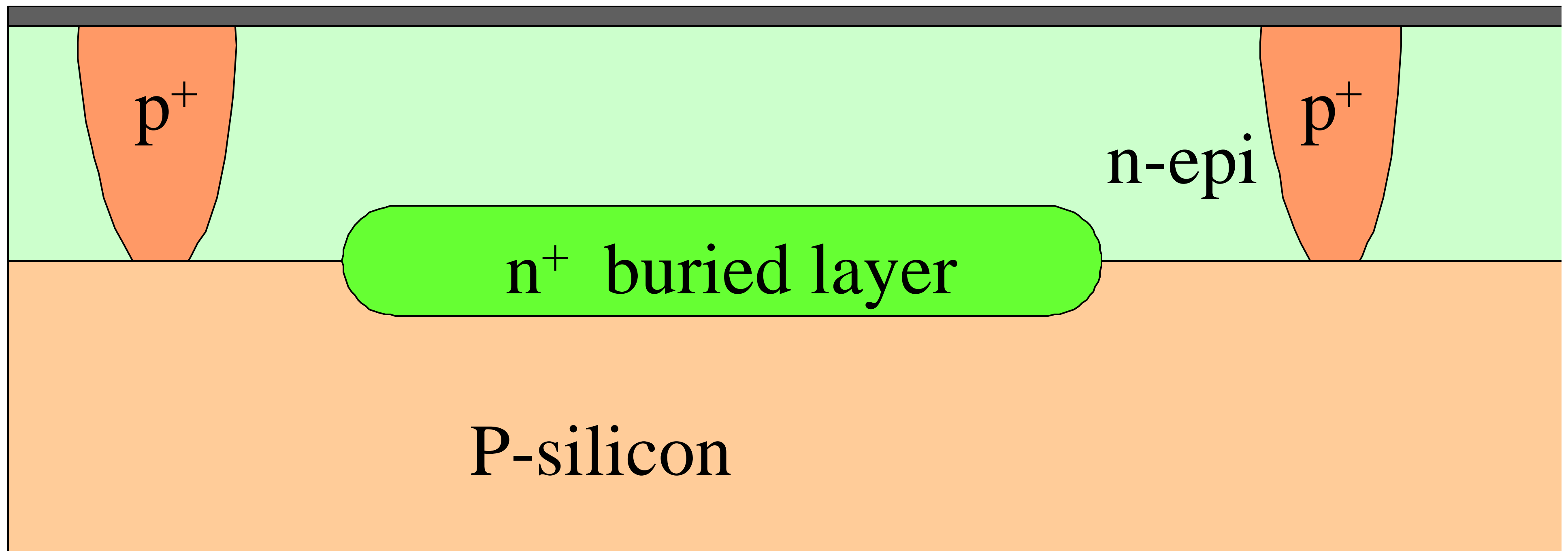
Buried Layer Implantation



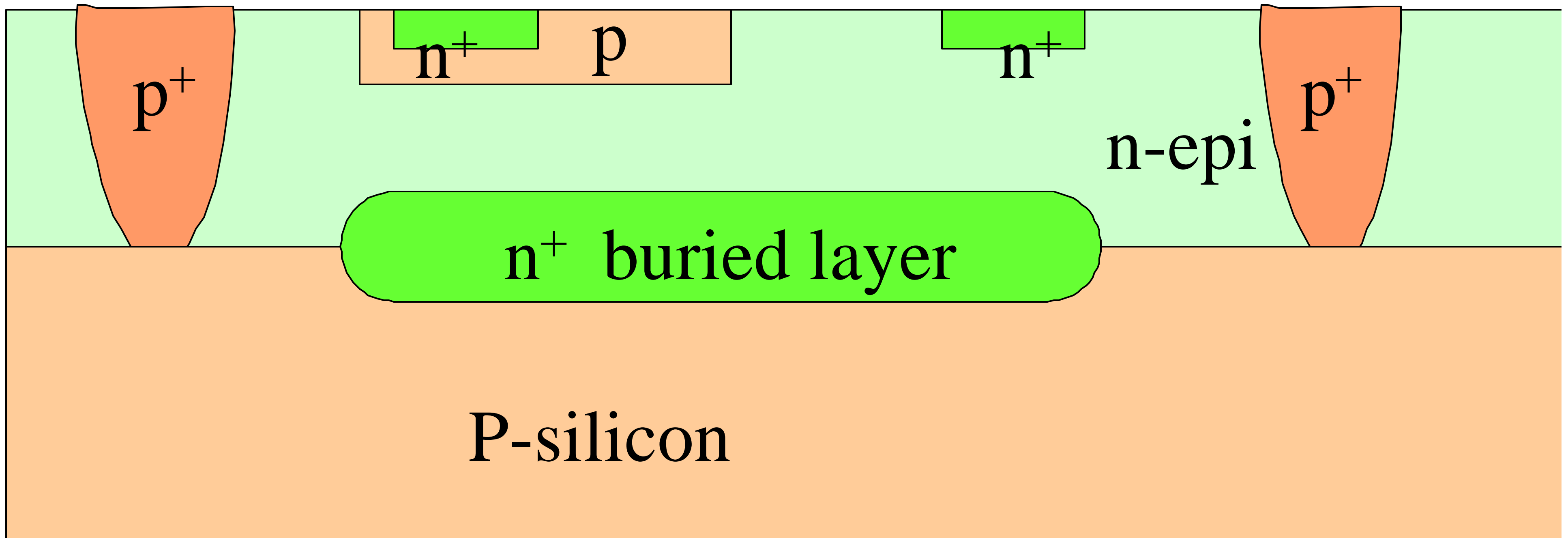
Epitaxy Grow



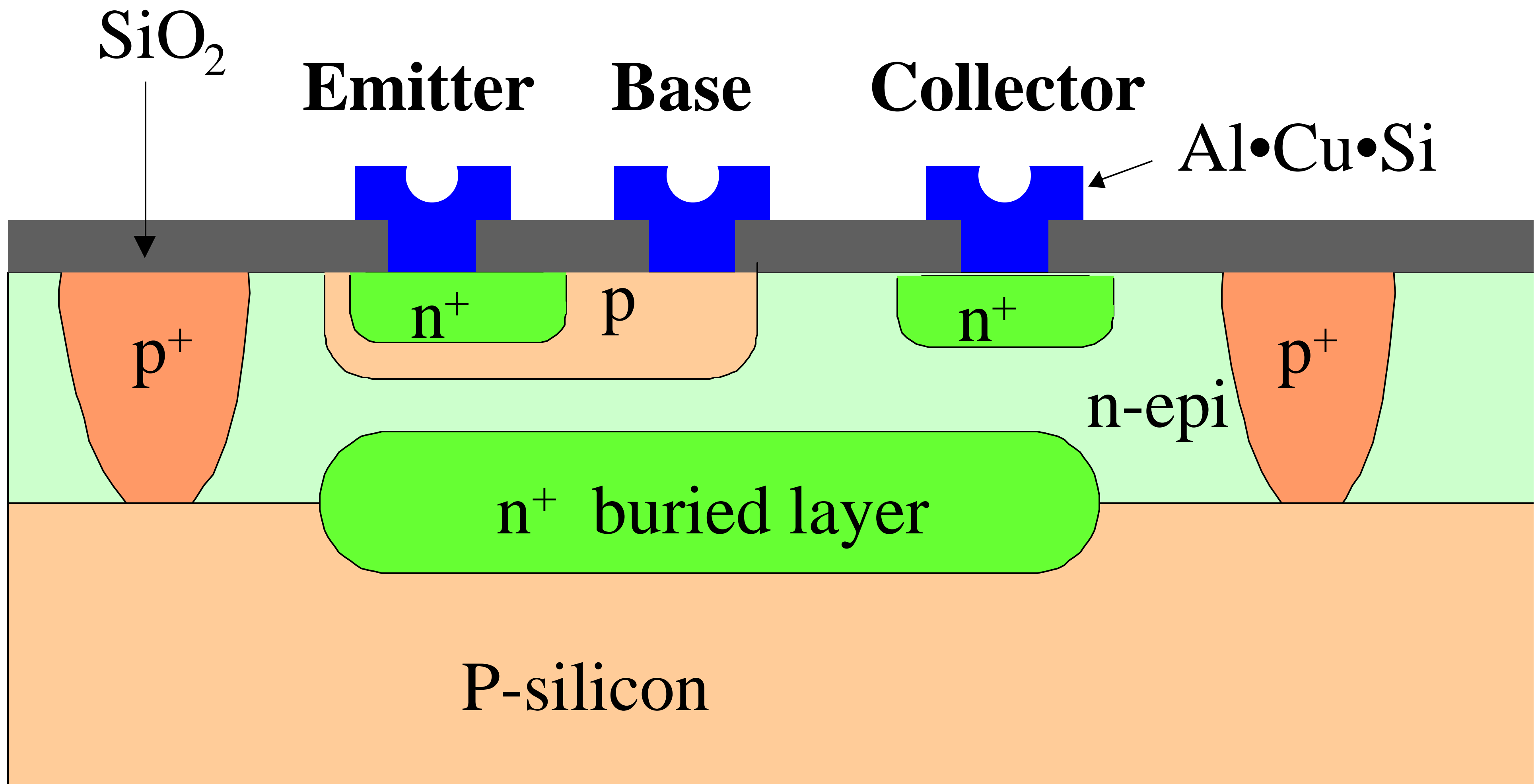
Isolation Implantation



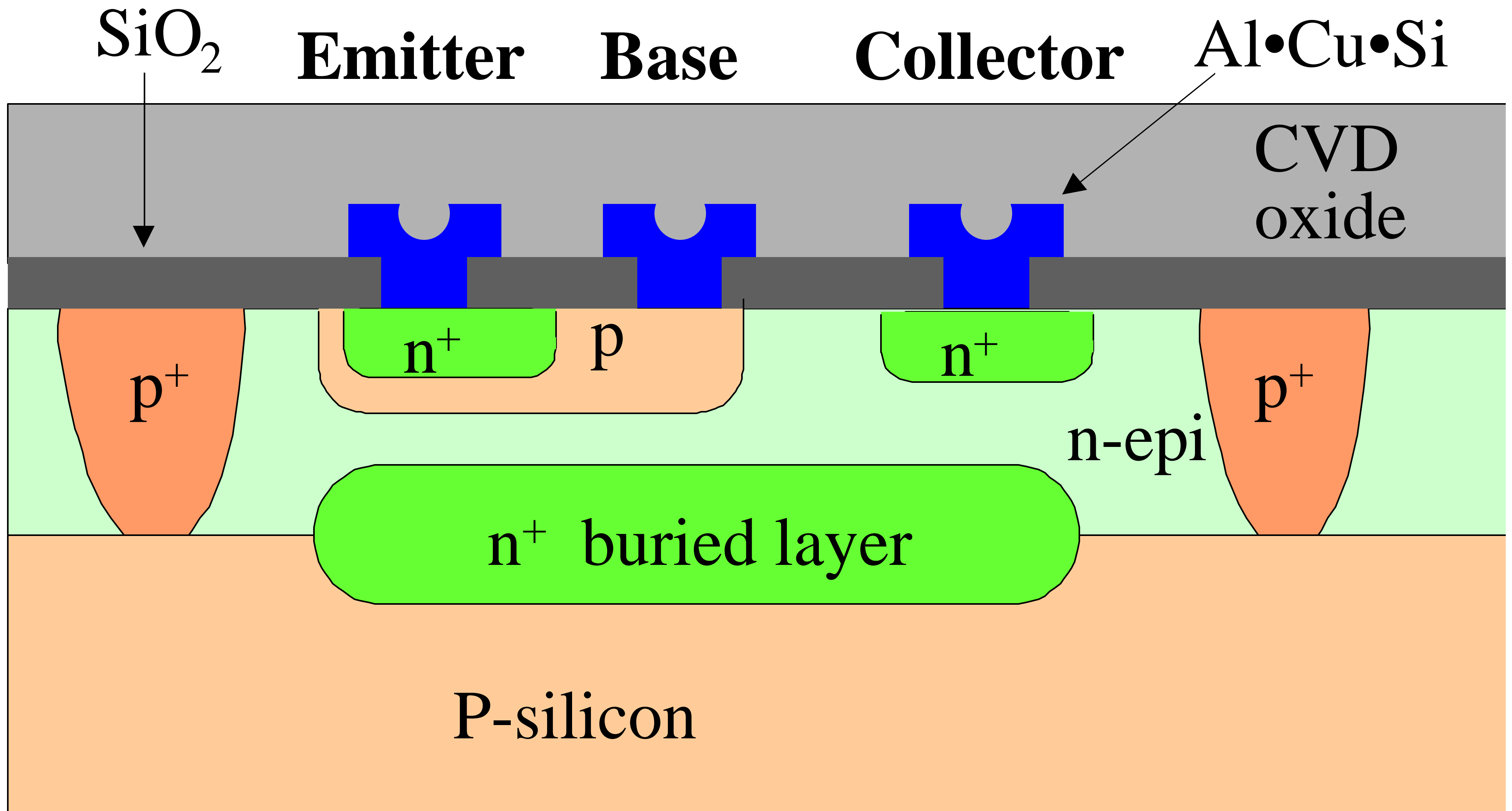
Emitter/Collector and Base Implantation



Metal Etch



Passivation Oxide Deposition



MOSFET

- Good for digital electronics
- Major driving forces:
  - Watches
  - Calculators
  - PC
  - Internet
  - Telecommunication

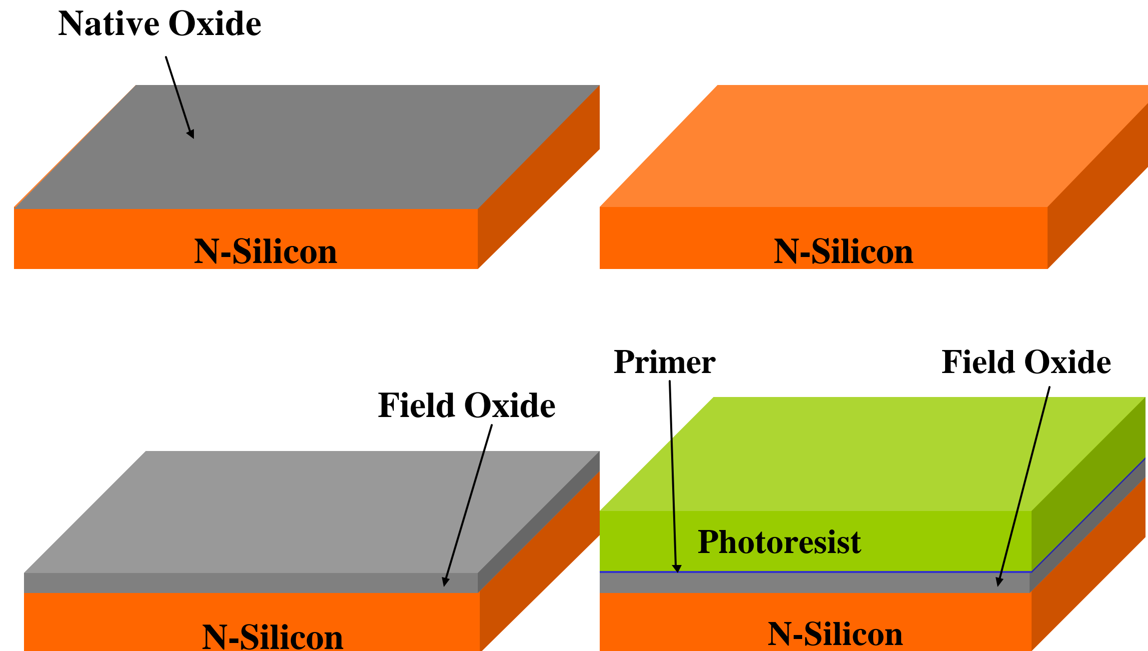
1960s: PMOS Process

- Bipolar dominated
- First MOSFET made in Bell Labs
- Silicon substrate
- Diffusion for doping
  - Boron diffuses faster in silicon
  - PMOS

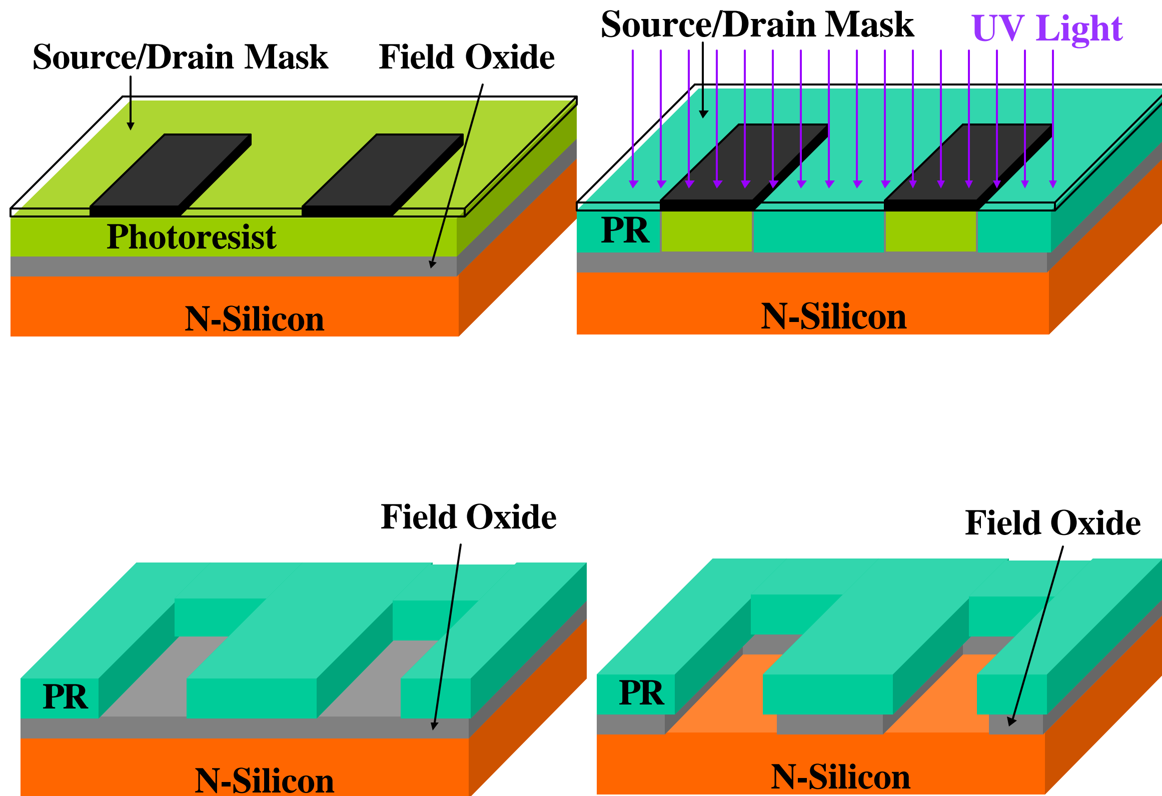
PMOS Process Sequence (1960s)

Wafer clean	(R)	Etch oxide	(R)
Field oxidation	(A)	Strip photo resist	(R)
Mask 1. (Source/Drain)	(P)	Al deposition	(A)
Etch oxide	(R)	**Mask 4.** (Metal)	(P)
Strip photo resist/Clean	(R)	Etch Aluminum	(R)
S/D diffusion (B)/Oxidation	(A)	Strip photo resist	(R)
Mask 2. (Gate)	(P)	Metal Anneal	(H)
Etch oxide	(R)	CVD oxide	(A)
Strip photo resist/Clean	(R)	**Mask 5.** (Bonding pad)	(P)
Gate oxidation	(A)	Etch oxide	(R)
Mask 3. (Contact)	(P)	*Test and packaging*	

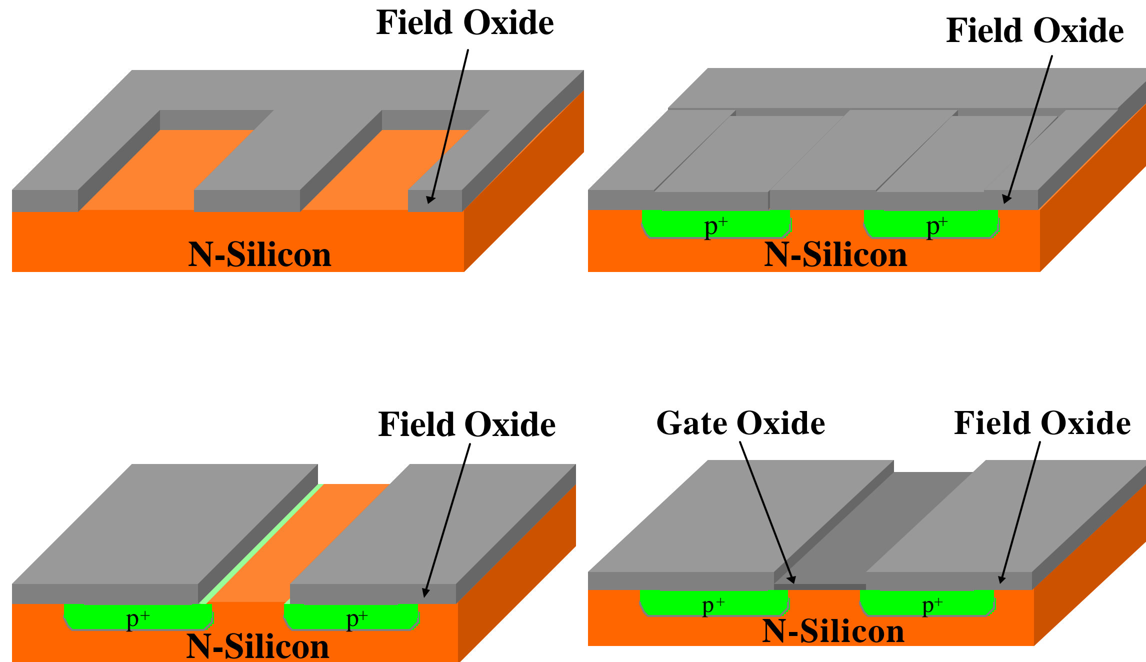
Wafer clean, field oxidation, and photoresist coating



Photolithography and etch



Source/drain doping and gate oxidation



Contact, Metallization, and Passivation

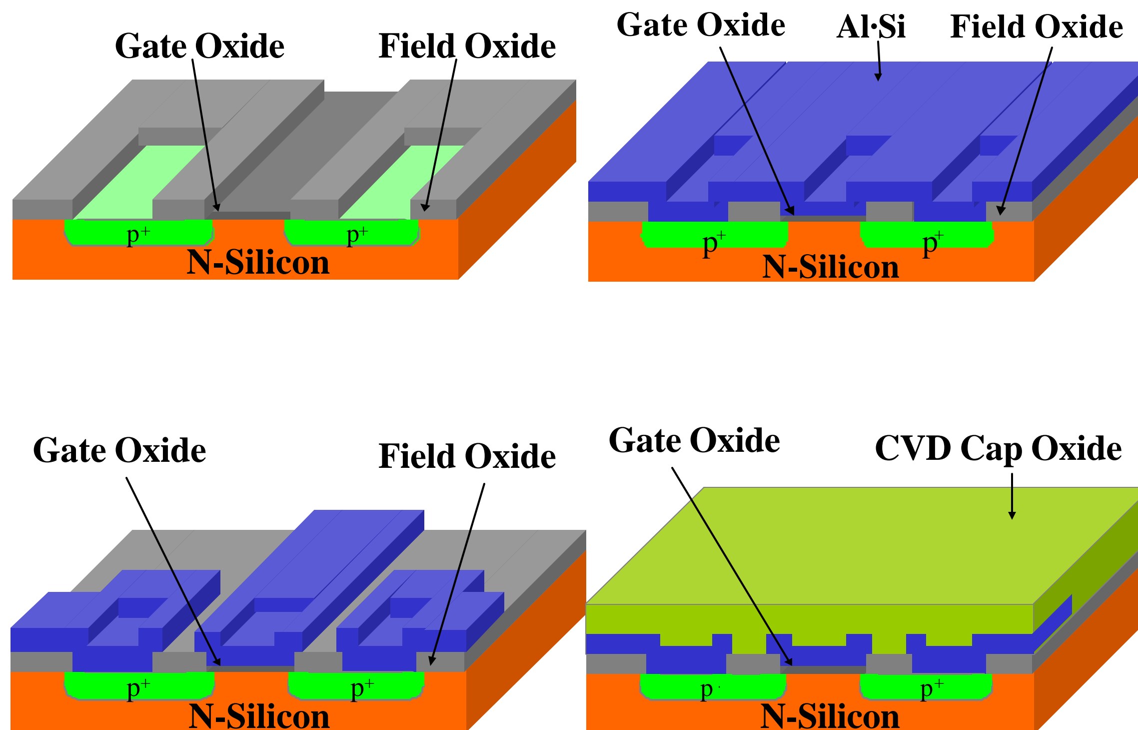
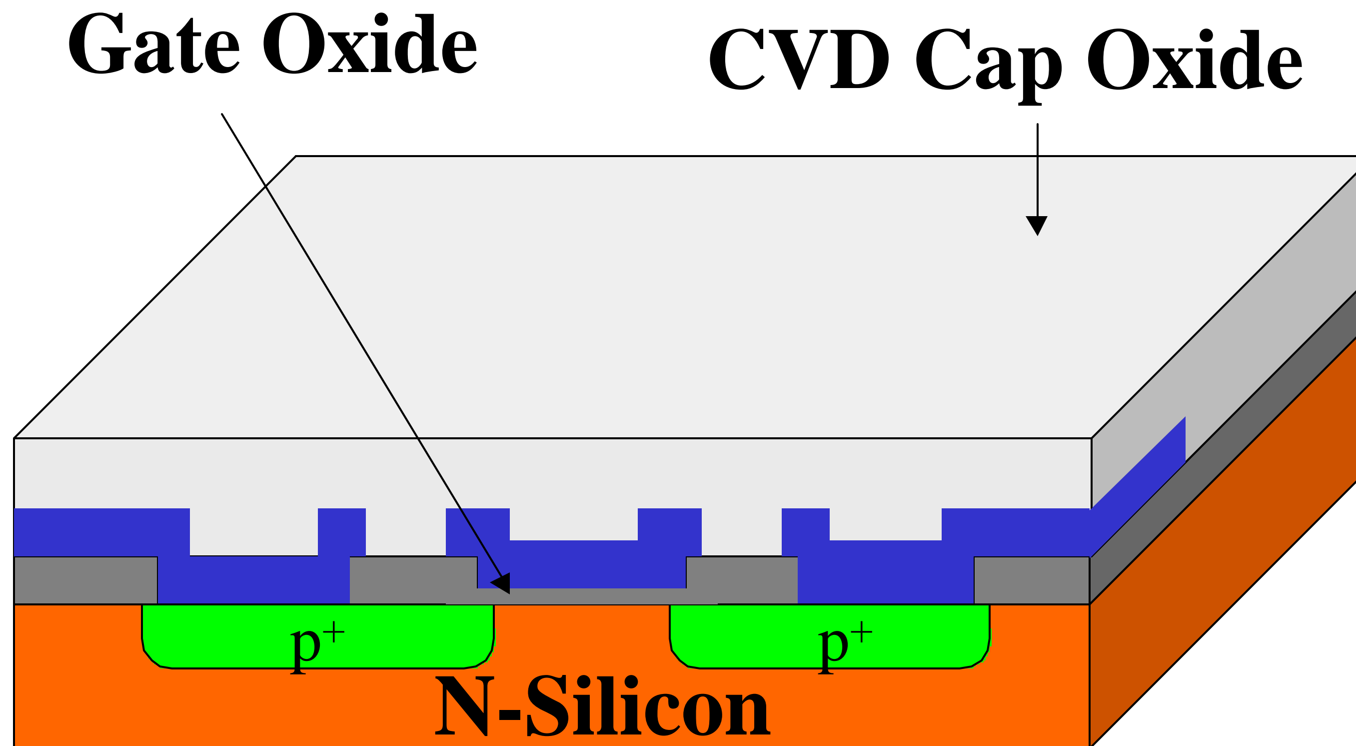


Illustration of a PMOS

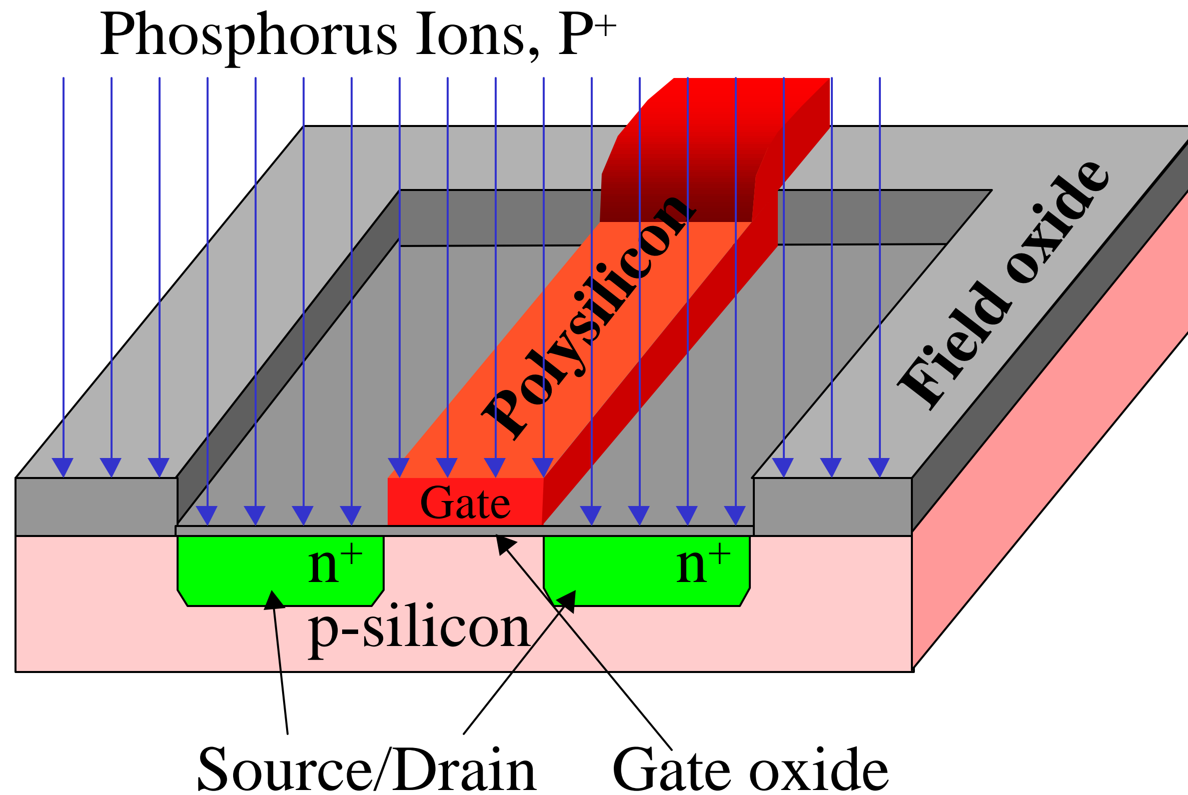


NMOS Process after mid-1970s

- Doping: ion implantation replaced diffusion
- NMOS replaced PMOS
  - NMOS is faster than PMOS
- Self-aligned source/drain

- Main driving force: watches and calculators

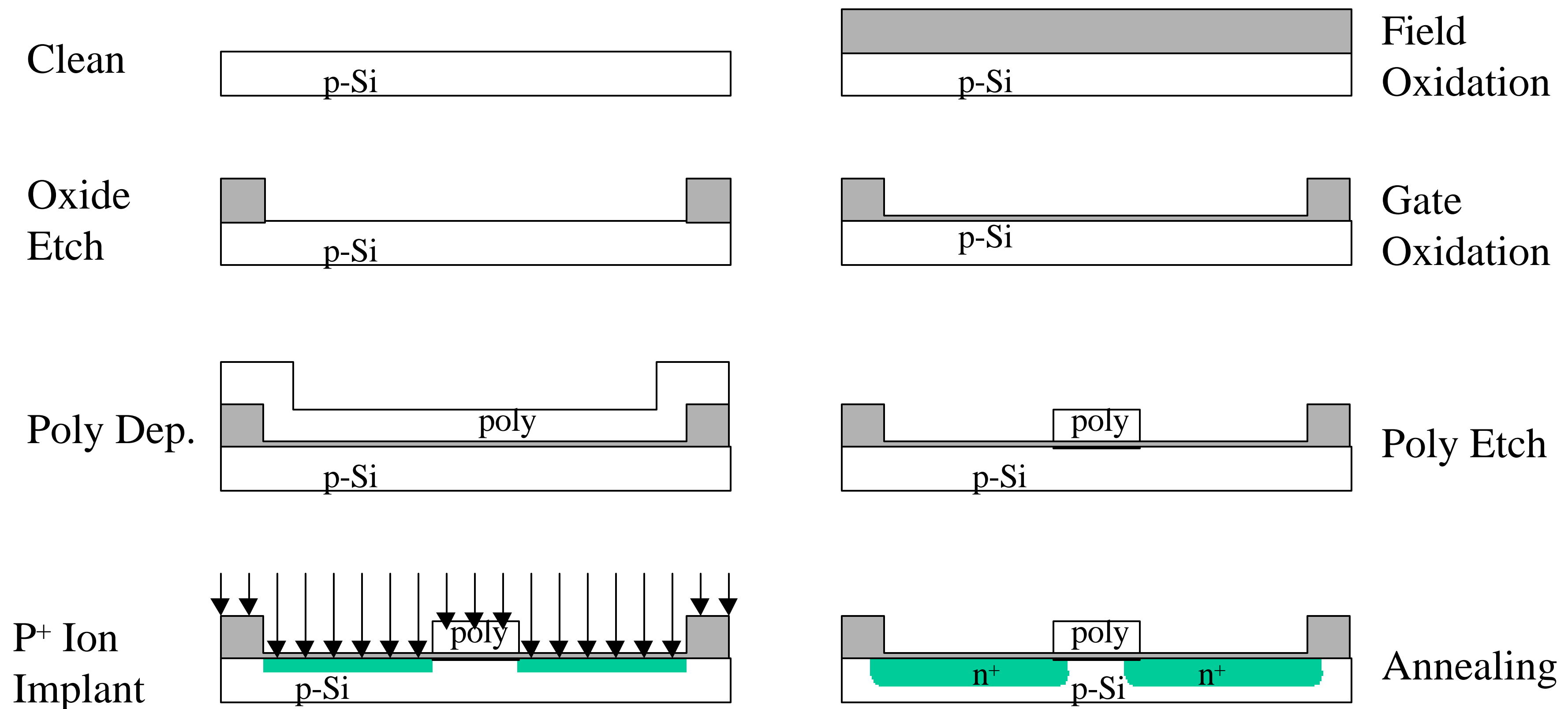
Self-aligned S/D Implantation



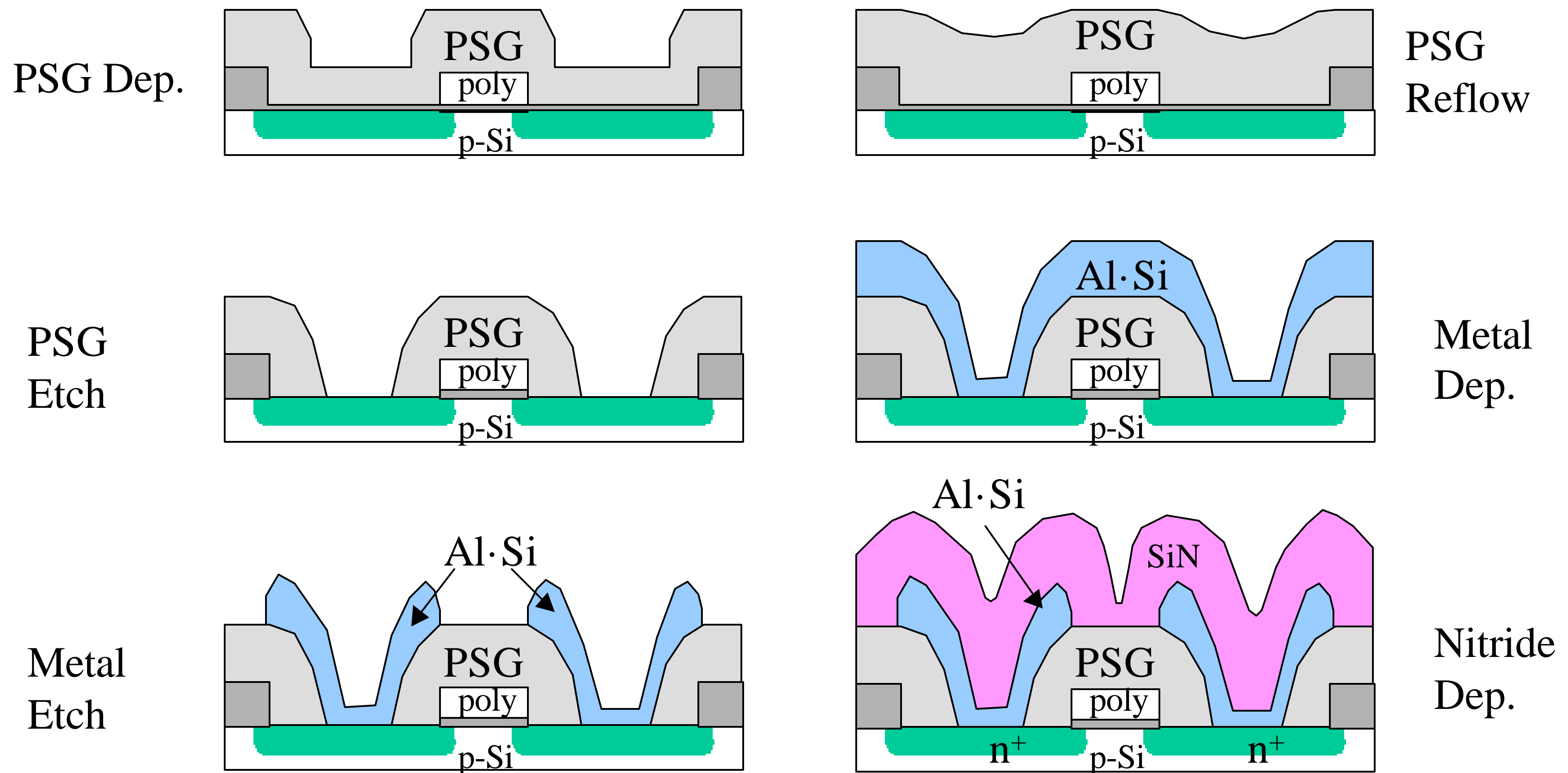
NMOS Process Sequence (1970s)

Wafer clean
Grow field oxide
Mask 1. Active Area
Etch oxide
Strip photo resist/Clean
Grow gate oxide
Deposit polysilicon
Mask 2. Gate
Etch polysilicon
Strip photo resist/Clean
S/D and poly dope implant
Anneal and poly reoxidation
CVD USG/PSG
PSG reflow
Mask 3. Contact
Etch PSG/USG
Strip photo resist/Clean
Al deposition
Mask 4. Metal
Etch Aluminum
Strip photo resist
Metal anneal
CVD oxide
Mask 5. Bonding pad
Etch oxide
Test and packaging

NMOS Process Sequence



NMOS Process Sequence



CMOS

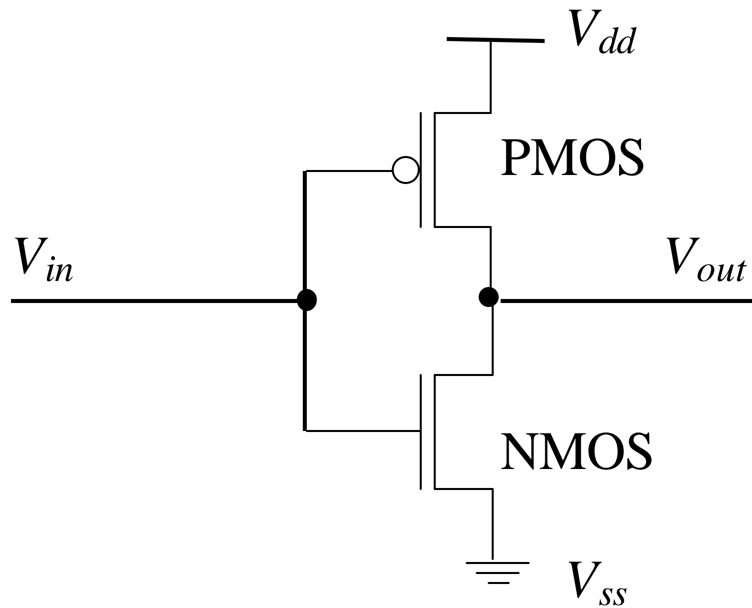
- In the 1980s MOSFET IC surpassed bipolar
- LCD replaced LED
- Power consumption of circuit
- CMOS replaced NMOS
- Still dominates the IC market

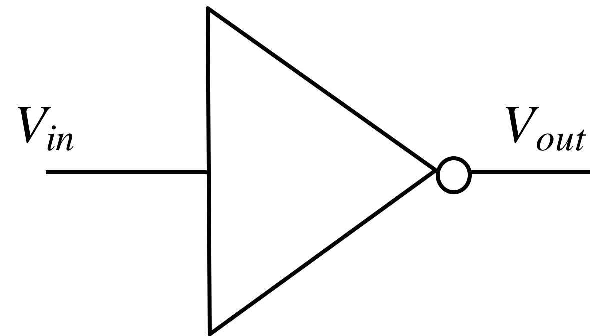
- Backbone of information revolution

Advantages of CMOS

- Low power consumption
- High temperature stability
- High noise immunity

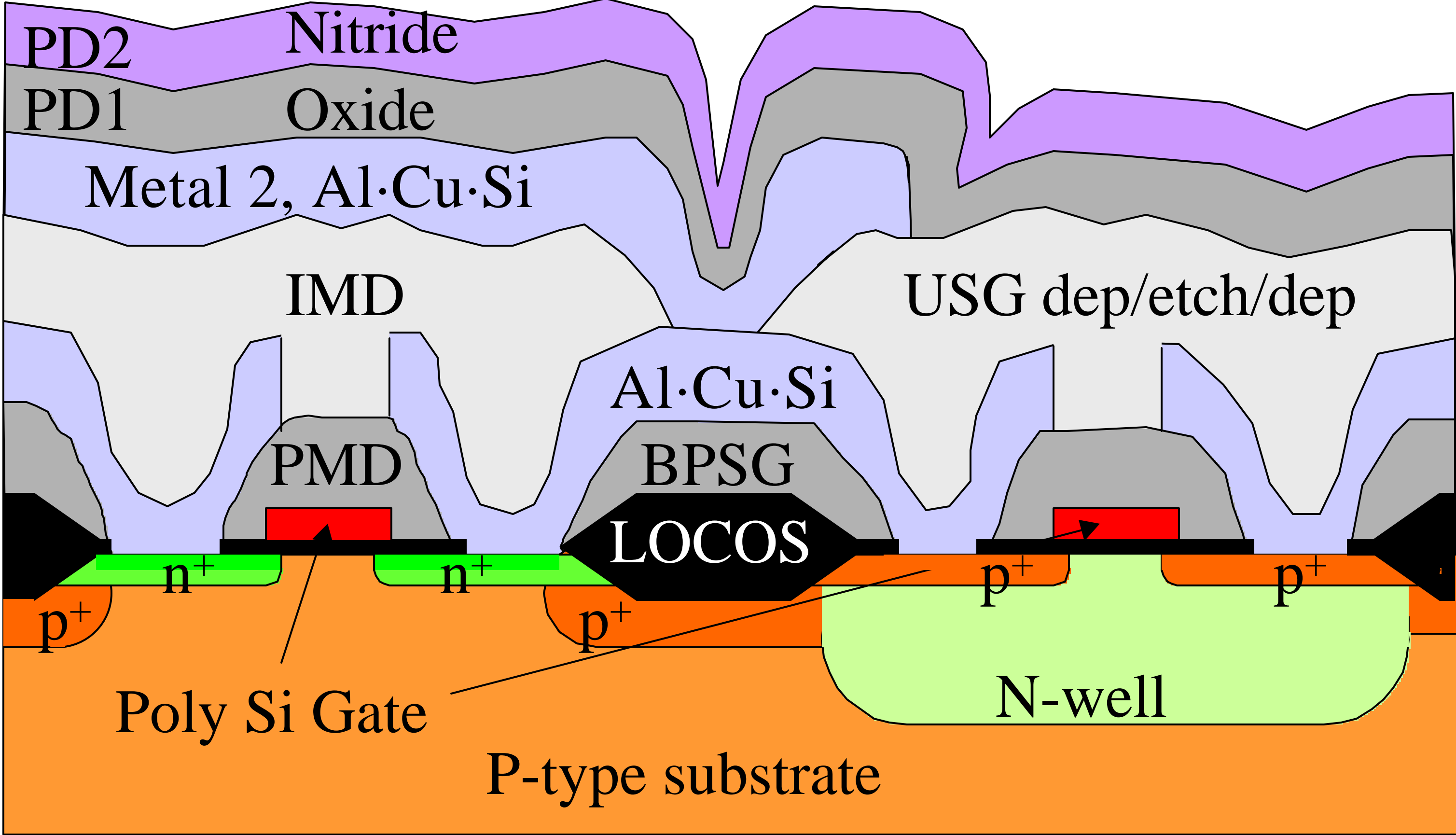
CMOS Inverter, Its Logic Symbol and Logic Table



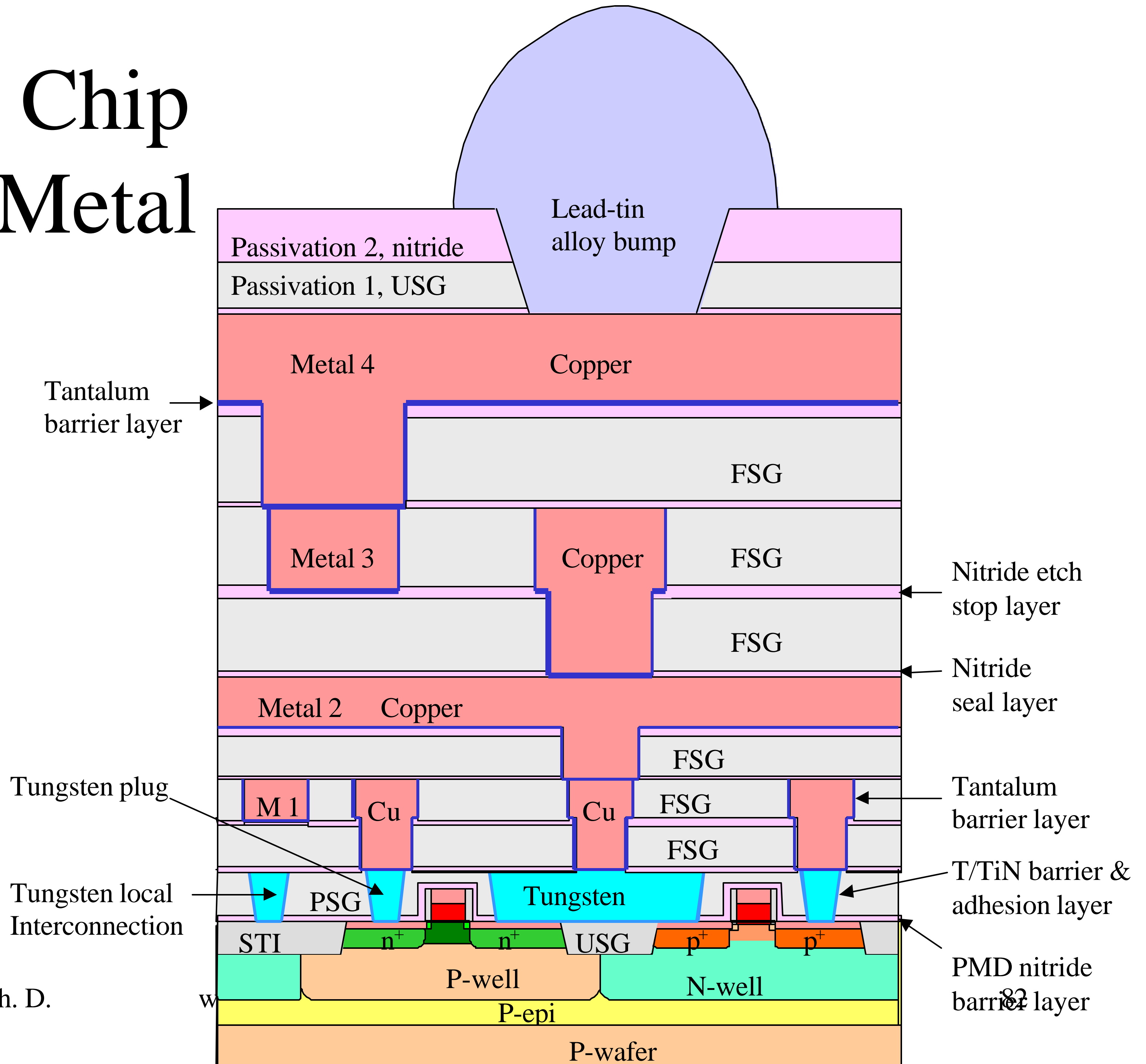


In	Out
0	1
1	0

CMOS Chip with 2 Metal Layers



CMOS Chip with 4 Metal Layers



Summary

- Semiconductors are the materials with conductivity between conductor and insulator
- Its conductivity can be controlled by dopant concentration and applied voltage
- Silicon, germanium, and gallium arsenate
- Silicon most popular: abundant and stable oxide

Summary

- Boron doped semiconductor is p-type, majority carriers are holes
- P, As, or Sb doped semiconductor is p-type, the majority carriers are electrons
- Higher dopant concentration, lower resistivity
- At the same dopant concentration, n-type has lower resistivity than p-type

Summary

- $R = \mathbf{r}\, l/A$
- $C = \mathbf{k}\, A/d$
- Capacitors are mainly used in DRAM
- Bipolar transistors can amplify electric signal, mainly used for analog systems
- MOSFET electric controlled switch, mainly used for digital systems

Summary

- MOSFETs dominated IC industry since 1980s
- Three kinds IC chips microprocessor, memory, and ASIC
- Advantages of CMOS: low power, high temperature stability, high noise immunity, and clocking simplicity

Summary

- The basic CMOS process steps are transistor making (front-end) and interconnection/passivation (back-end)
- The most basic semiconductor processes are adding, removing, heating, and patterning processes.

Chapter 4
Wafer Manufacturing and Epitaxy Growing

Hong Xiao, Ph. D.
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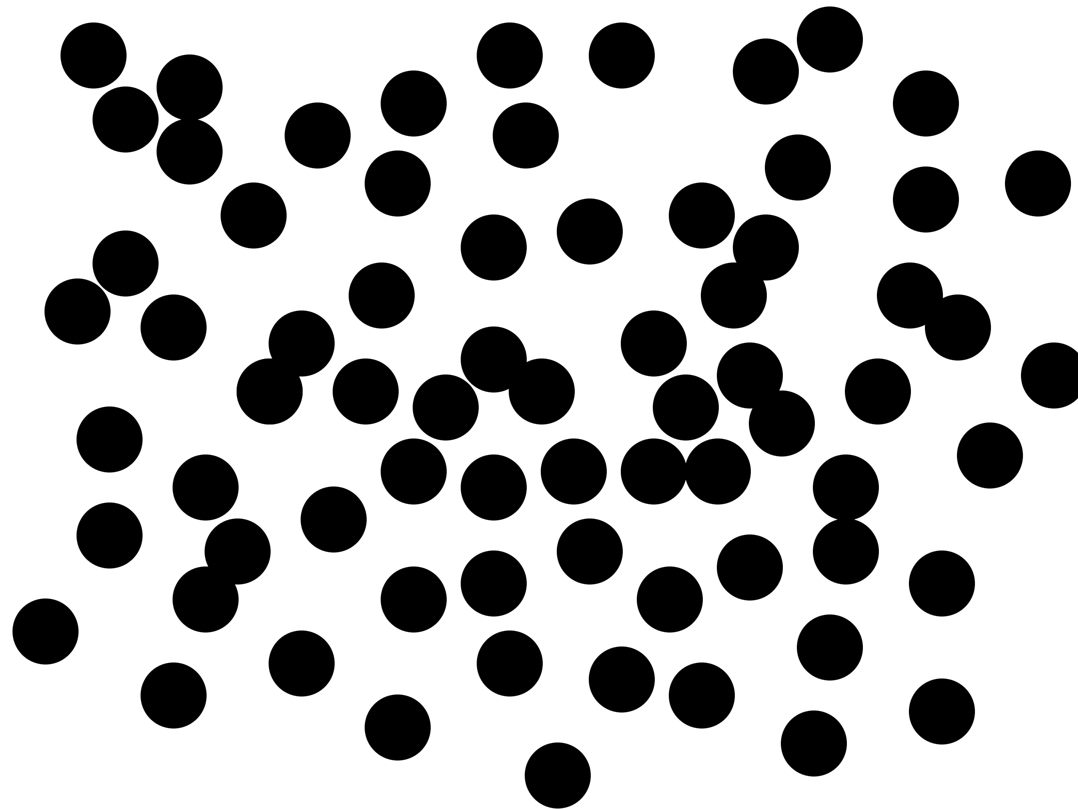
Objectives

- Give two reasons why silicon dominate
- List at least two wafer orientations
- List the basic steps from sand to wafer
- Describe the CZ and FZ methods
- Explain the purpose of epitaxial silicon
- Describe the epi-silicon deposition process.

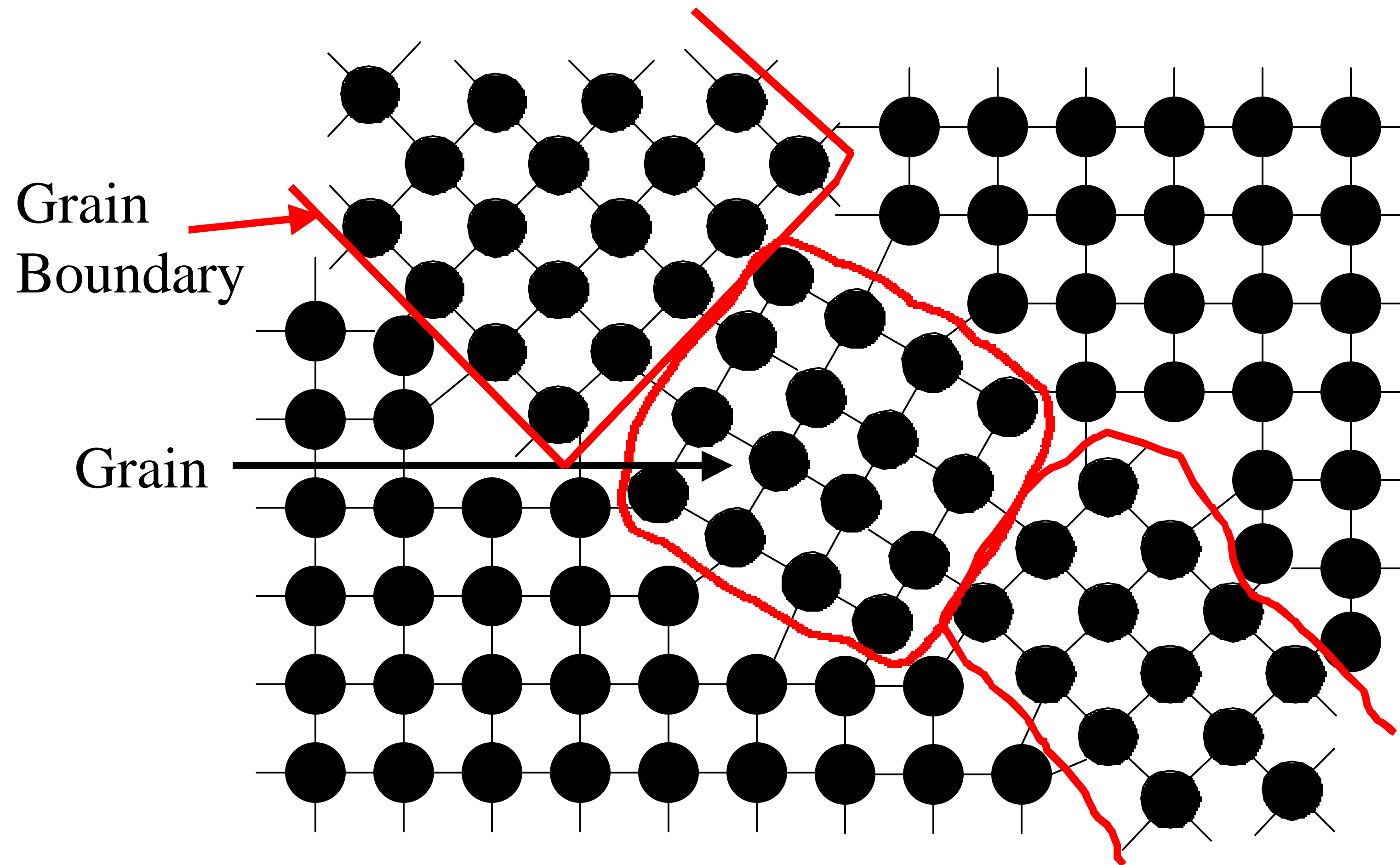
Crystal Structures

- Amorphous
  - No repeated structure at all
- Polycrystalline
  - Some repeated structures
- Single crystal
  - One repeated structure

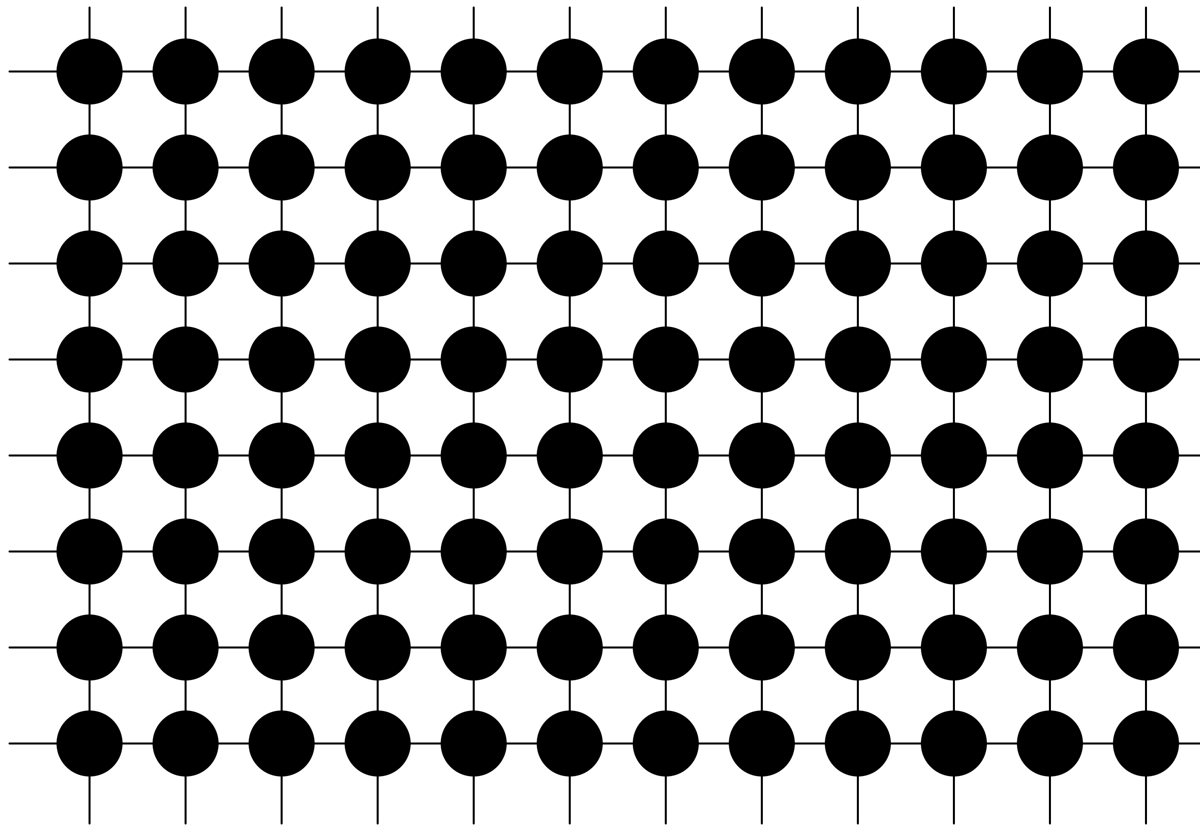
Amorphous Structure



Polycrystalline Structure



Single Crystal Structure



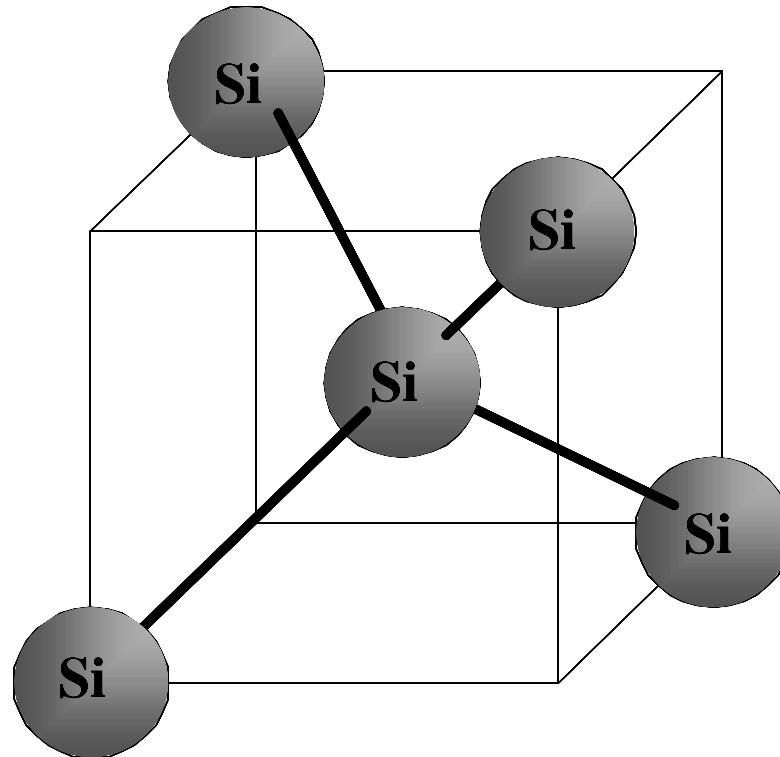
Why Silicon?

- Abundant, cheap
- Silicon dioxide is very stable, strong dielectric, and it is easy to grow in thermal process.
- Large band gap, wide operation temperature range.

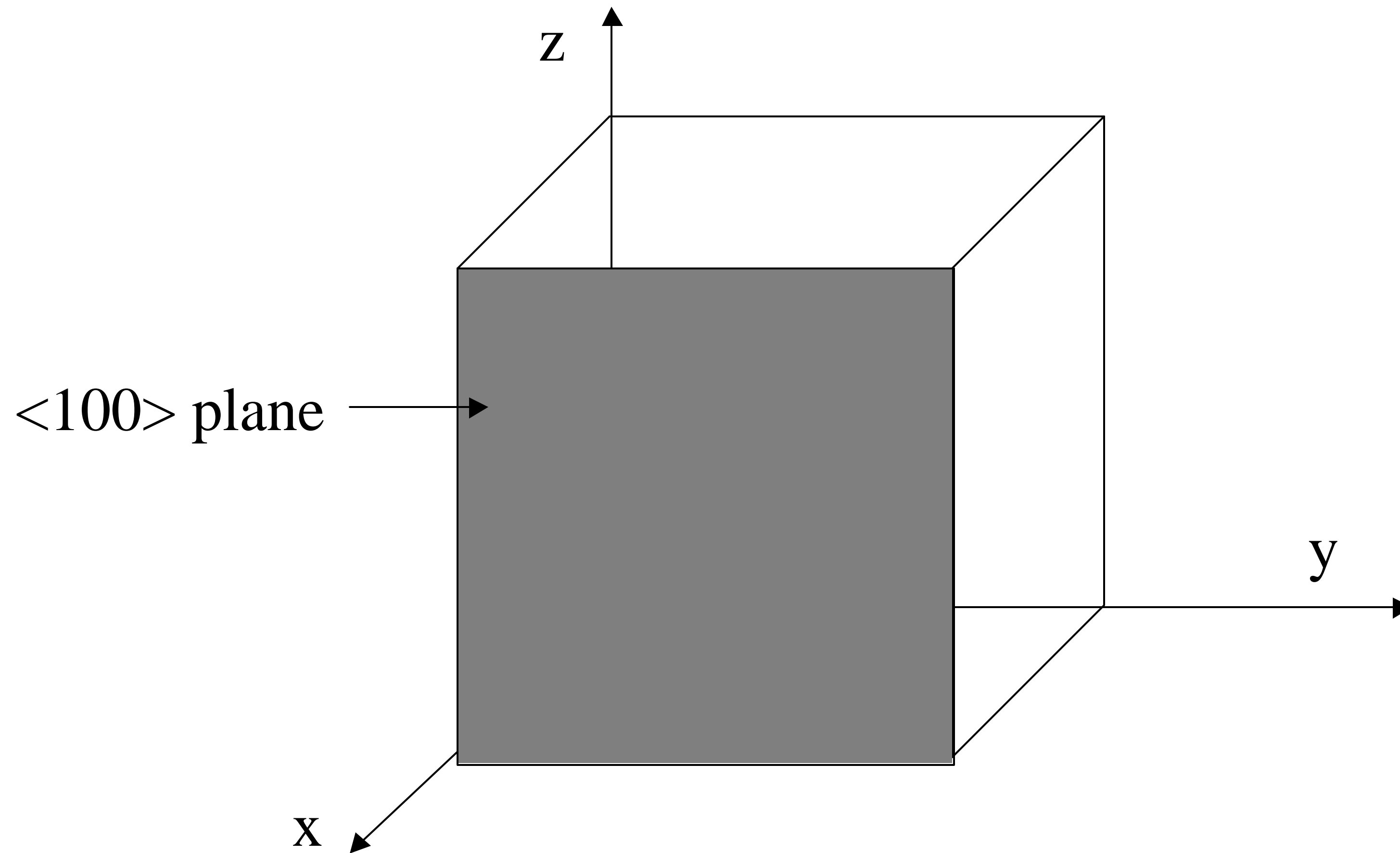
Name	Silicon
Symbal	Si
Atomic number	14
Atomic weight	28.0855
Discoverer	Jöns Jacob Berzelius
Discovered at	Sweden
Discovery date	1824
Origin of name	From the Latin word "silicis" meaning "flint"
Bond length in single crystal Si	2.352 Å
Density of solid	2.33 g/cm^3
Molar volume	12.06 cm^3
Velocity of sound	2200 m/sec
Electrical resistivity	100,000 μΩ·cm
Reflectivity	28%
Melting point	1414 °C
Boiling point	2900 °C

Source: http://www.shef.ac.uk/chemistry/web-elements/nofr-key/Si.html

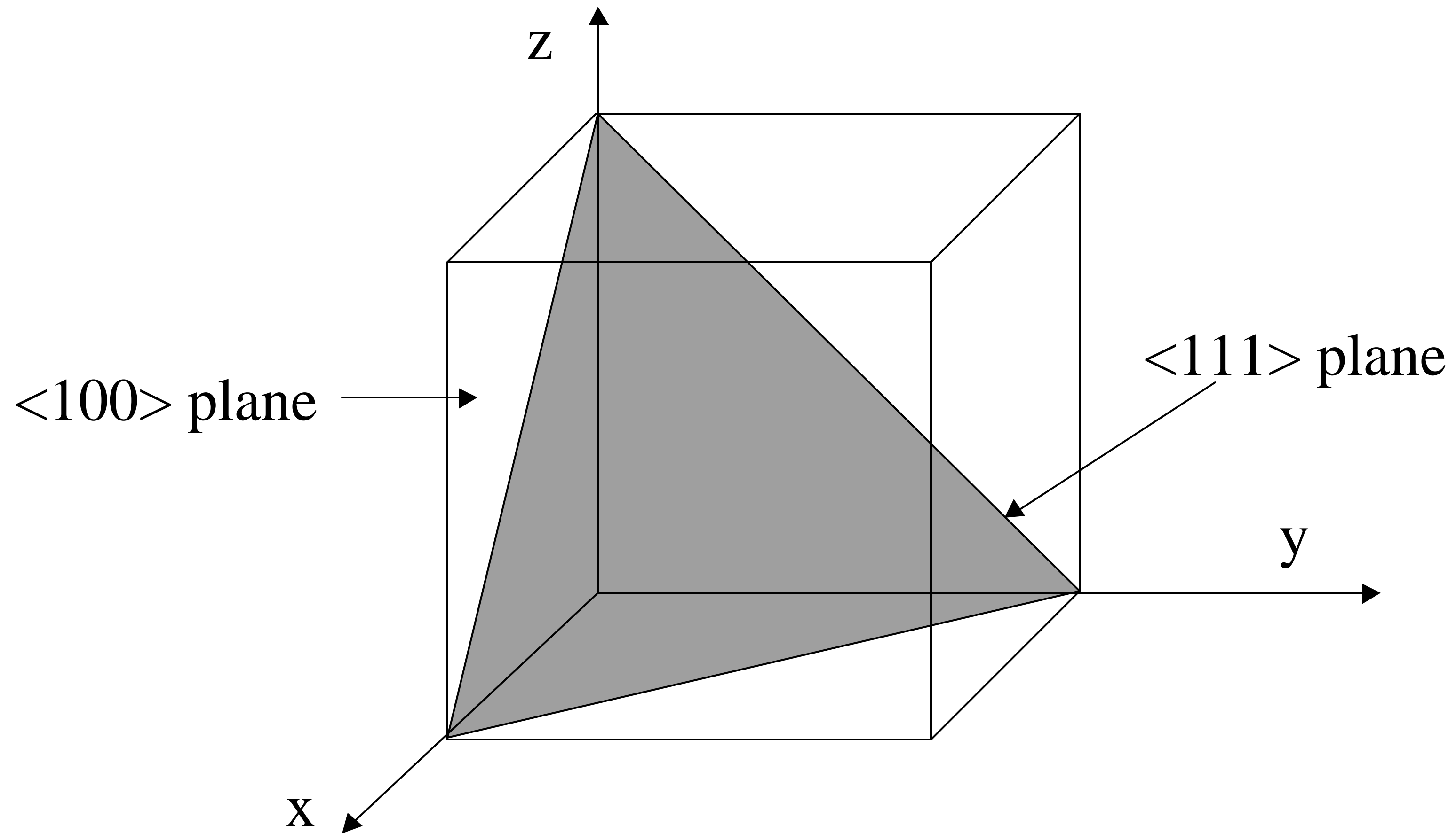
Unit Cell of Single Crystal Silicon



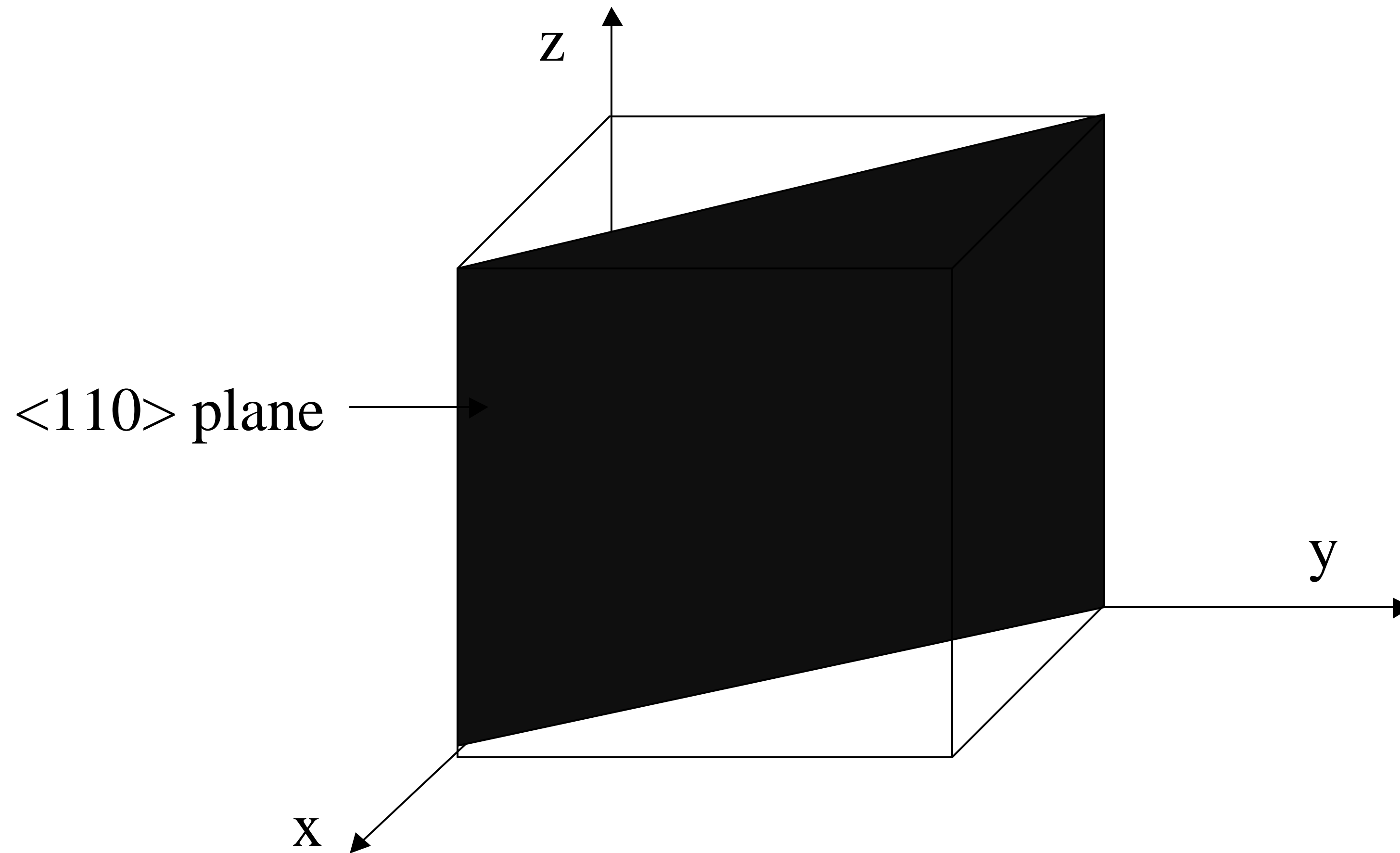
Crystal Orientations: <100>



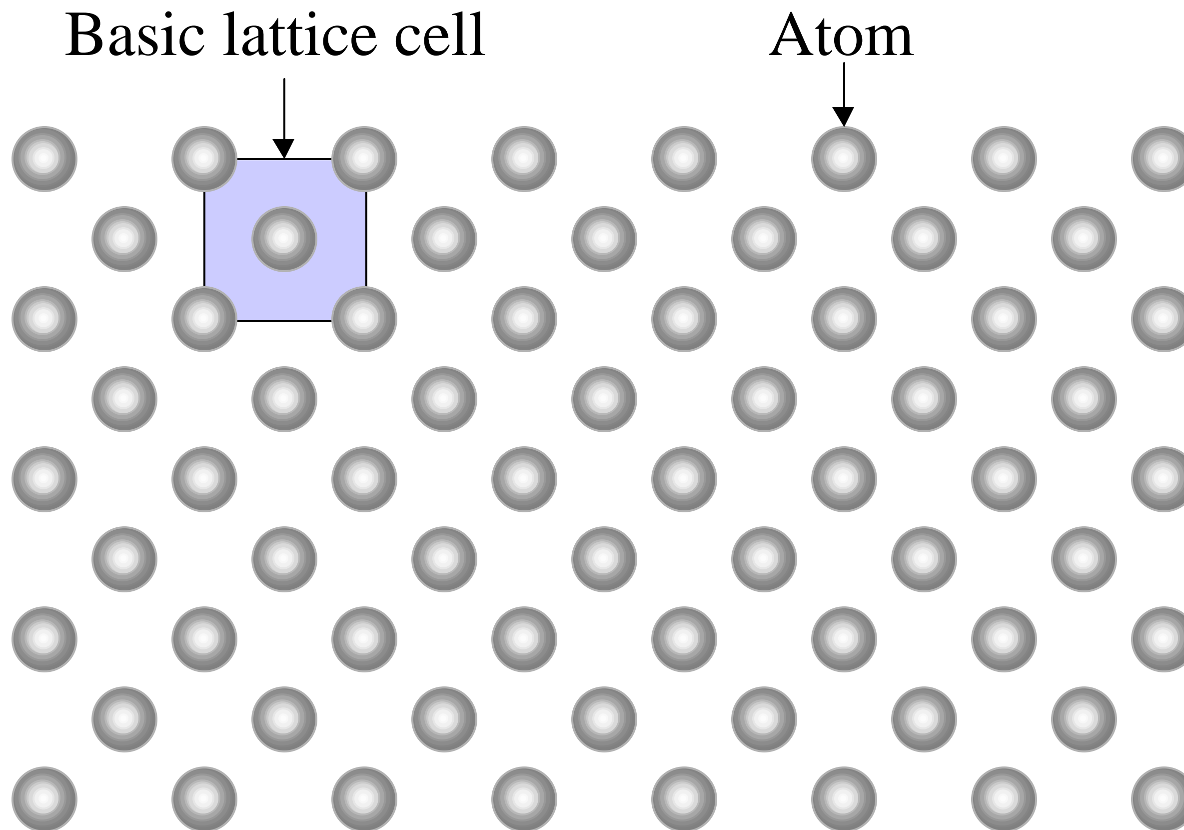
Crystal Orientations: <111>



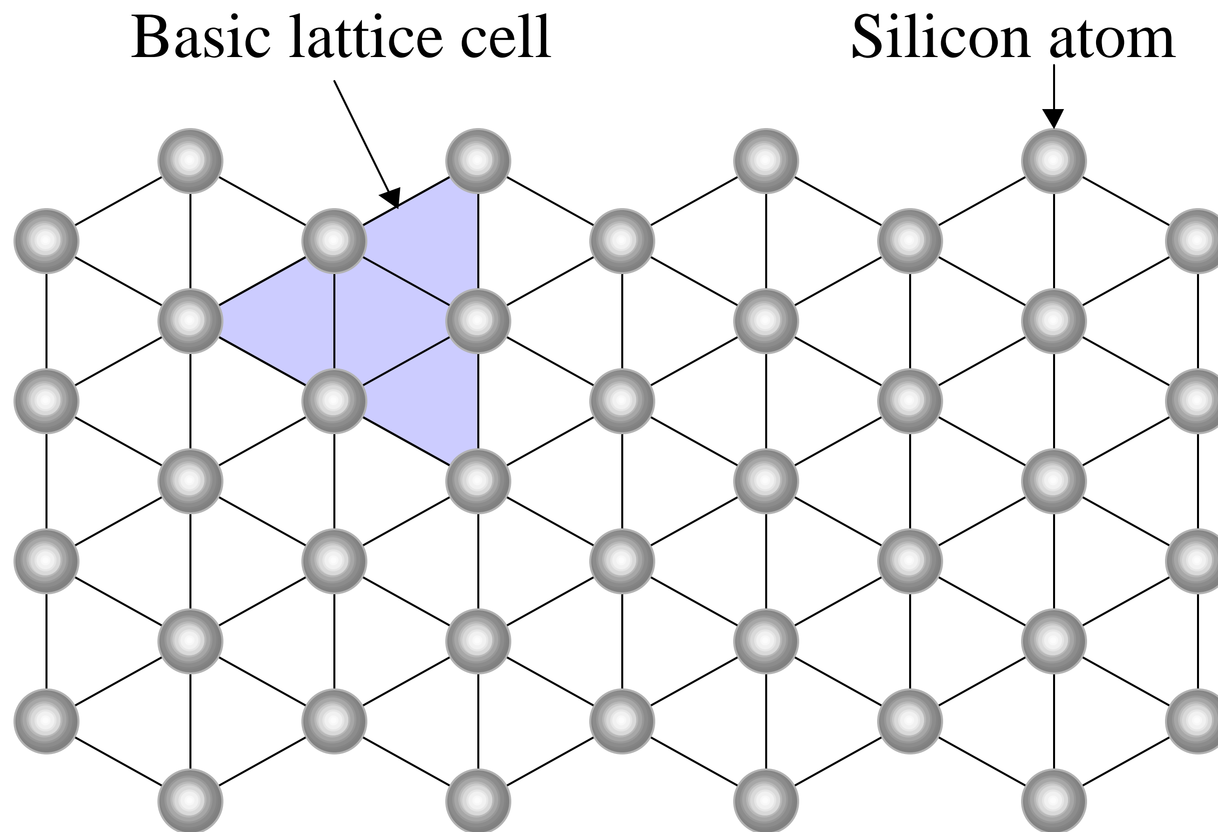
Crystal Orientations: <110>



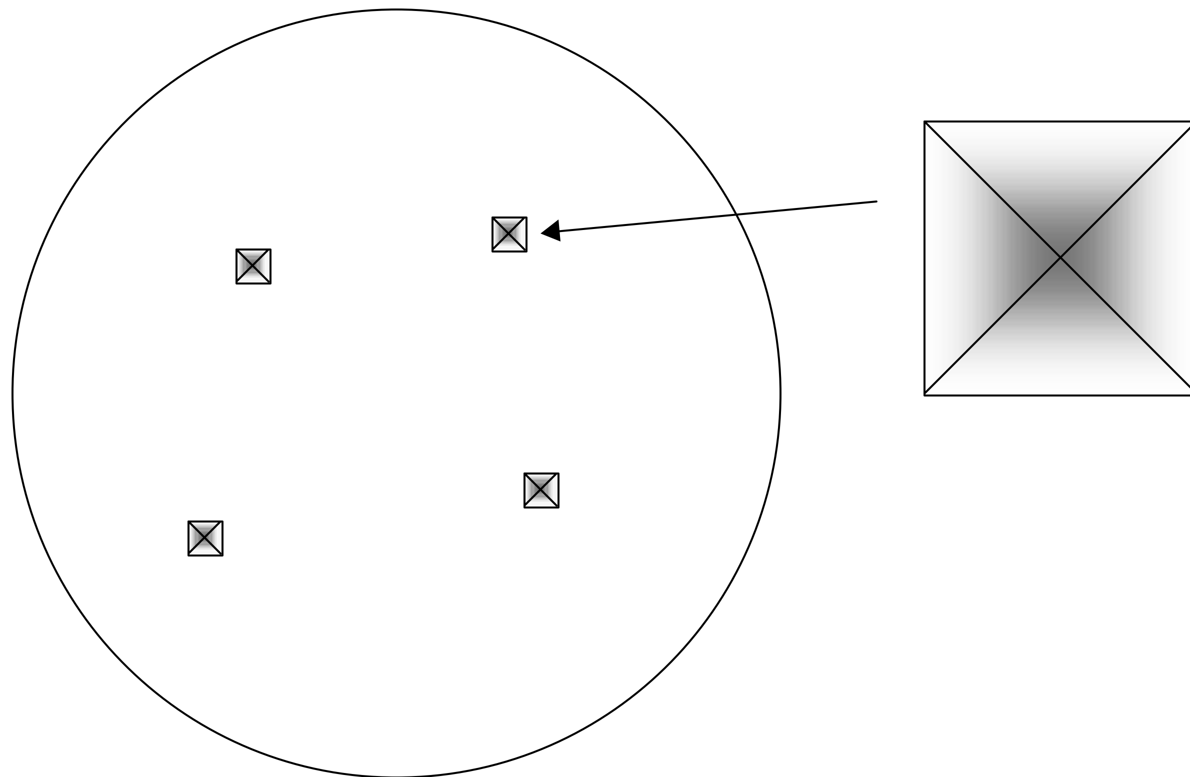
<100> Orientation Plane



<111> Orientation Plane



<100> Wafer Etch Pits



<111> Wafer Etch Pits

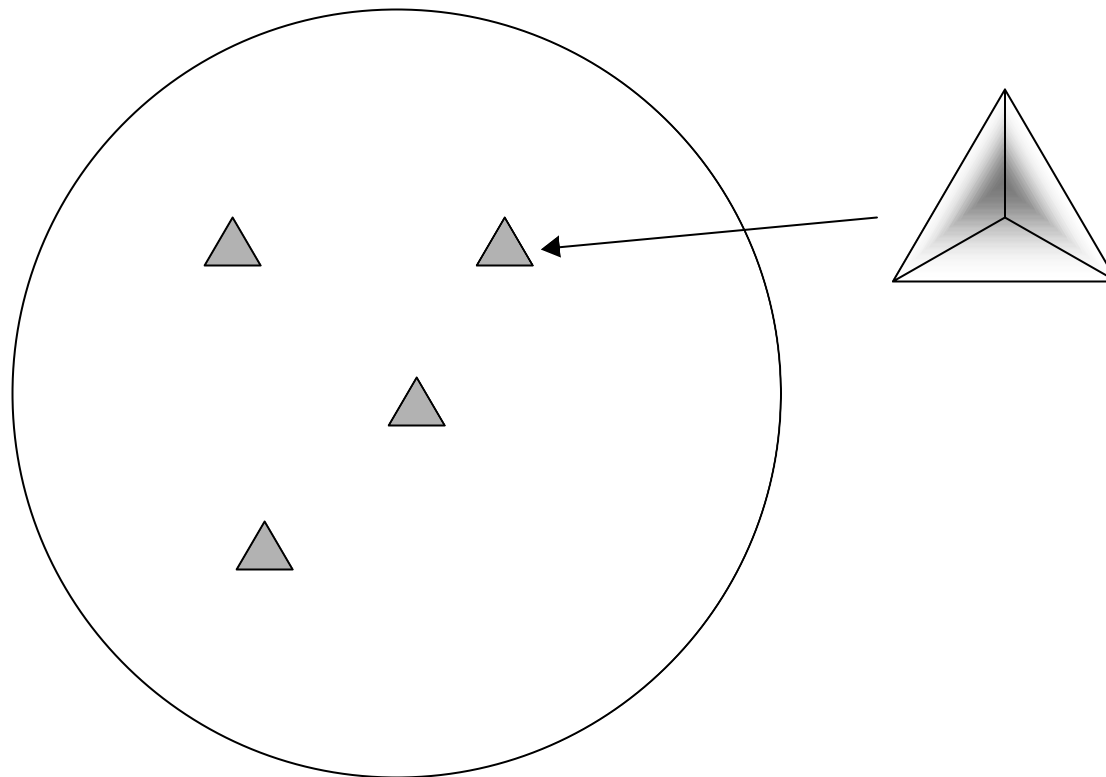
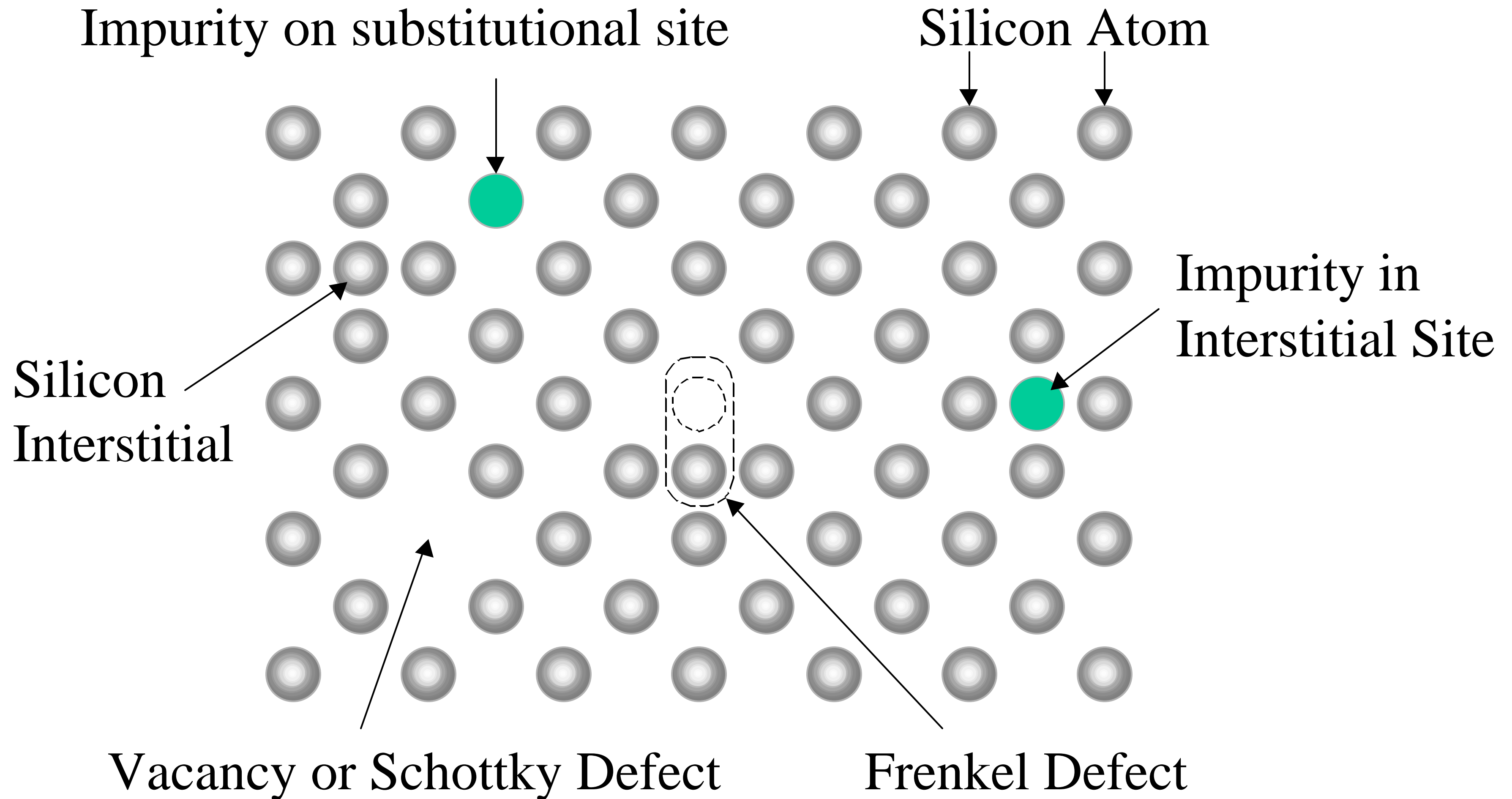
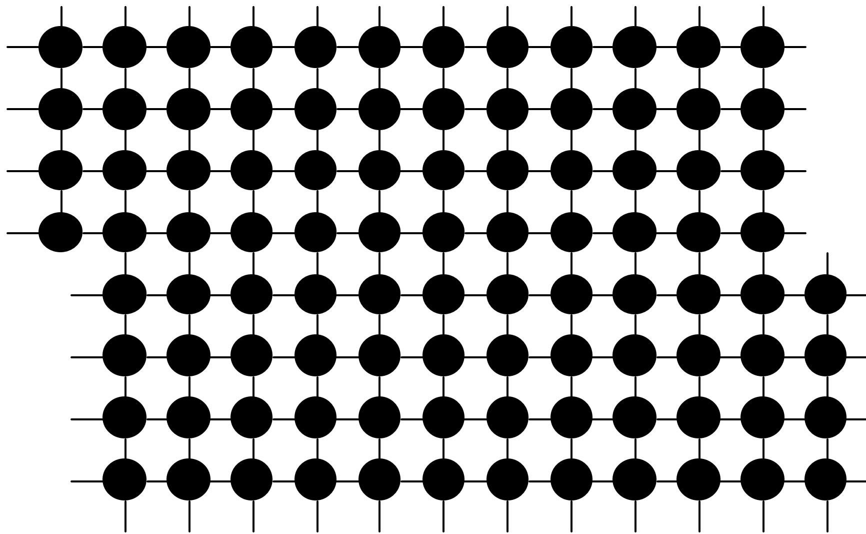
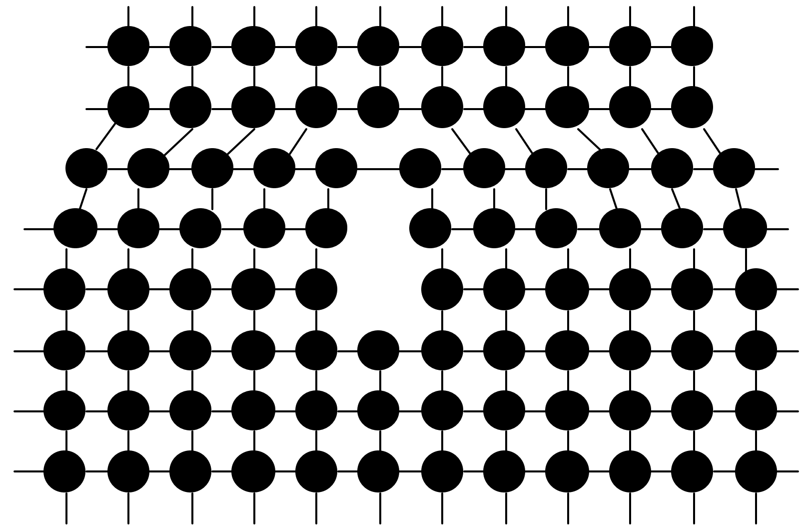


Illustration of the Defects



Dislocation Defects





From Sand to Wafer

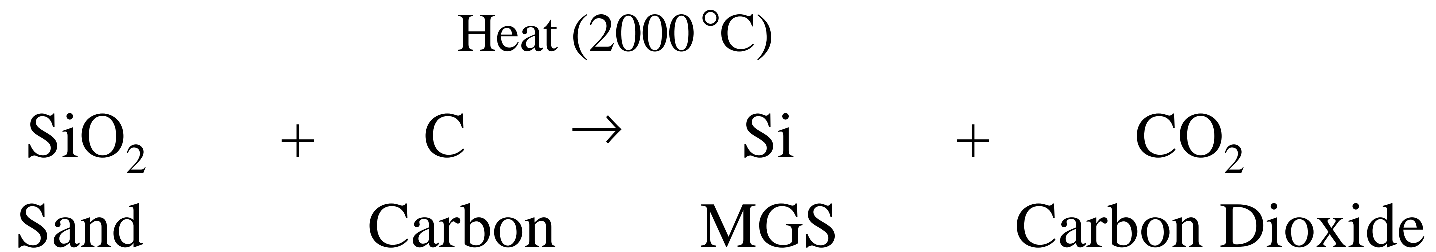
- Quartz sand: silicon dioxide
- Sand to metallic grade silicon (MGS)
- React MGS powder with HCl to form TCS
- Purify TCS by vaporization and condensation
- React TCS to H_2 to form polysilicon (EGS)
- Melt EGS and pull single crystal ingot

From Sand to Wafer (cont.)

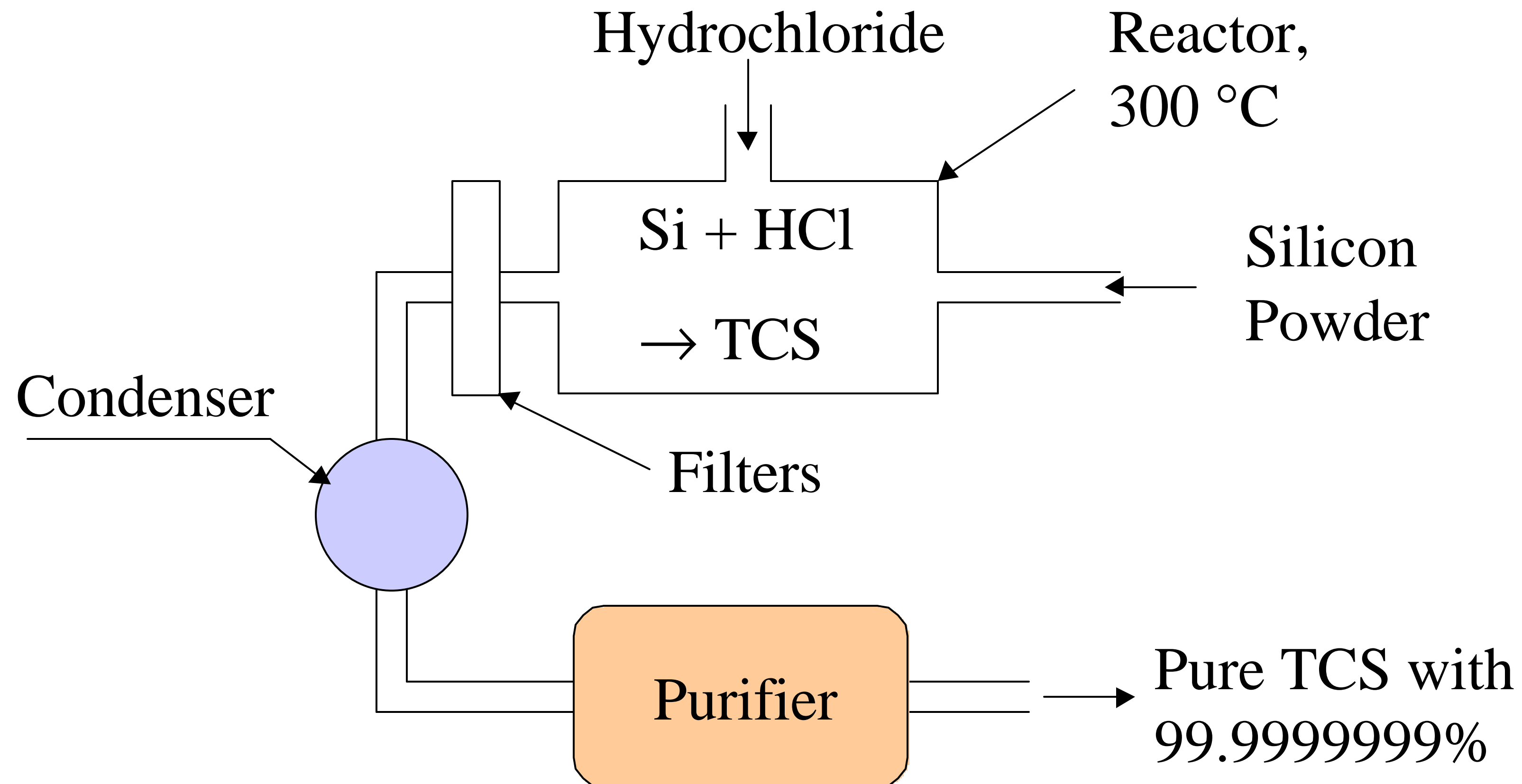
- Cut end, polish side, and make notch or flat
- Saw ingot into wafers
- Edge rounding, lap, wet etch, and CMP
- Laser scribe

- Epitaxy deposition

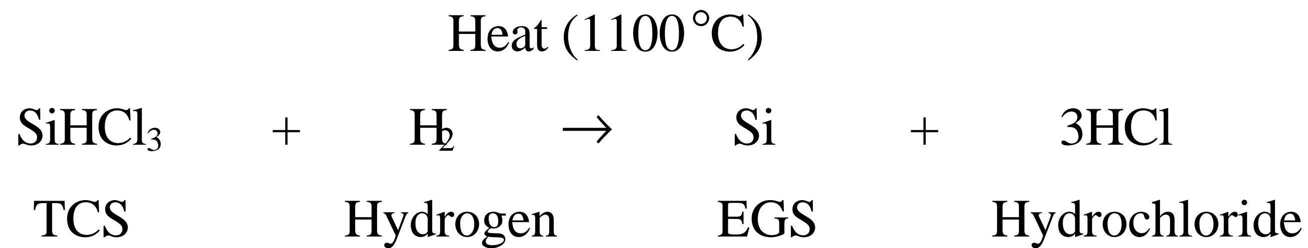
From Sand to Silicon



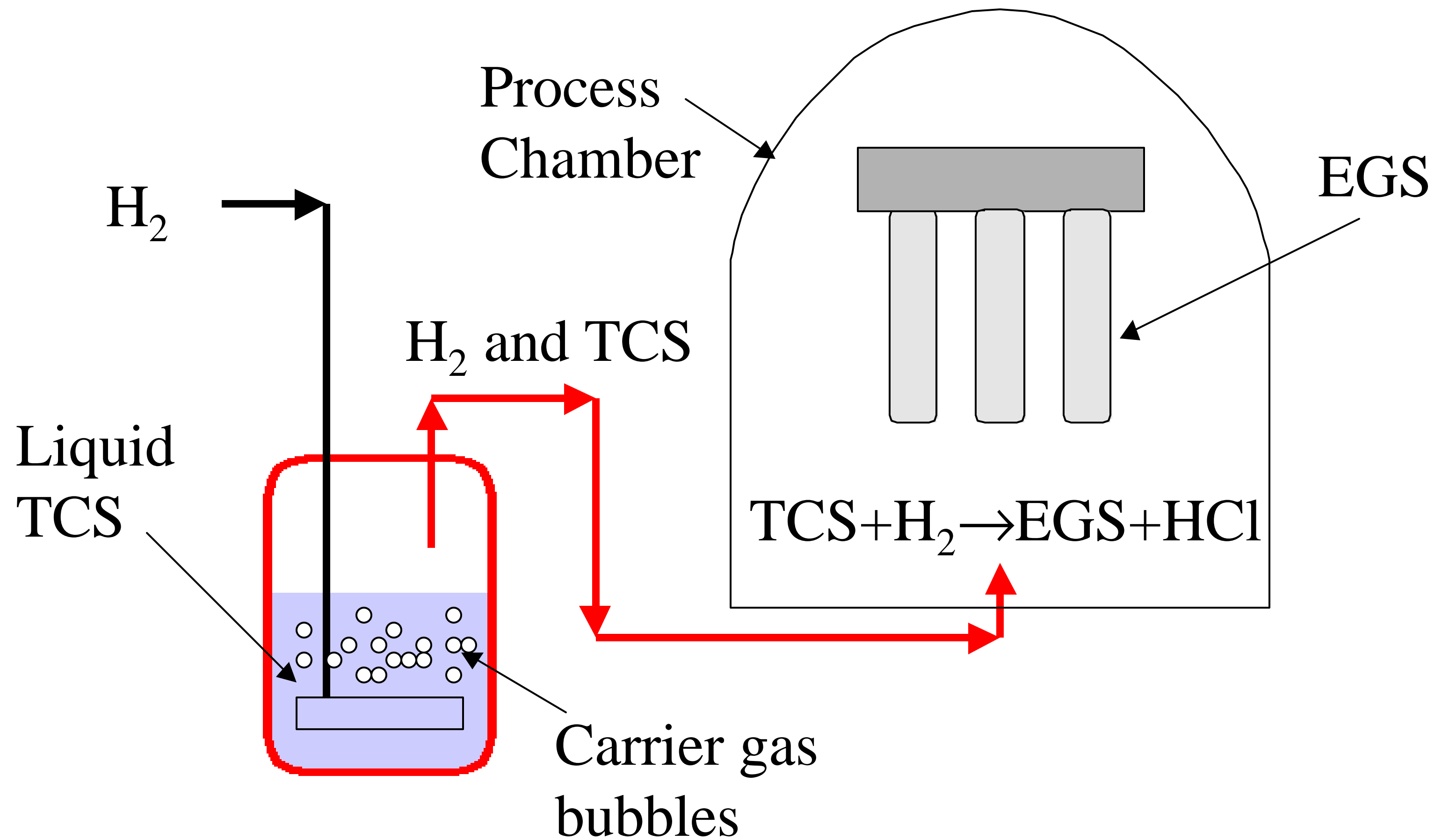
Silicon Purification I



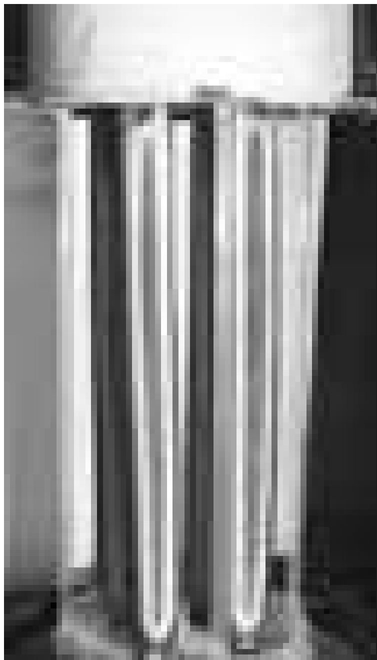
Polysilicon Deposition, EGS



Silicon Purification II

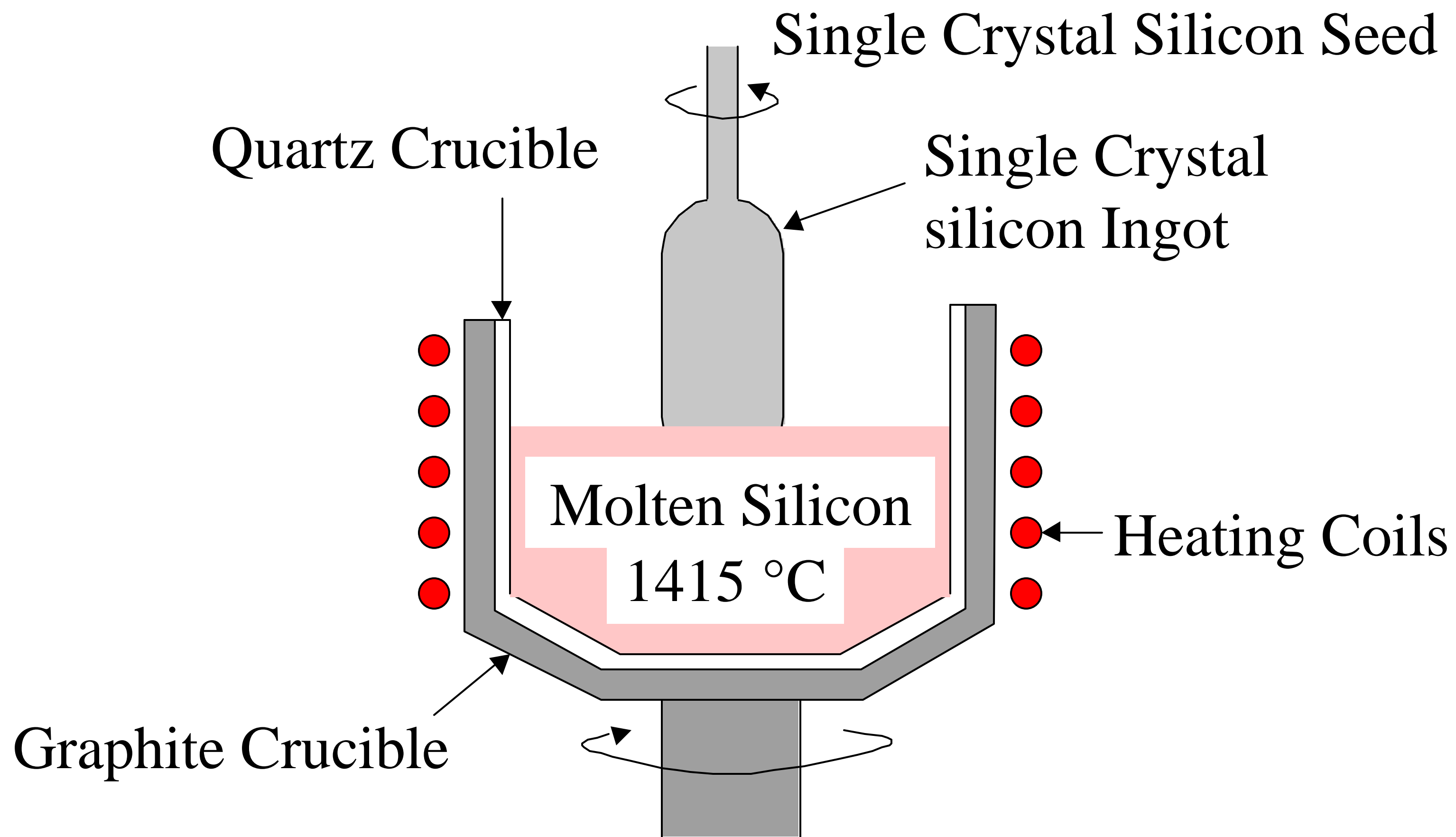


Electronic Grade Silicon



Source: http://www.fullman.com/semiconductors/_polysilicon.html

Crystal Pulling: CZ method

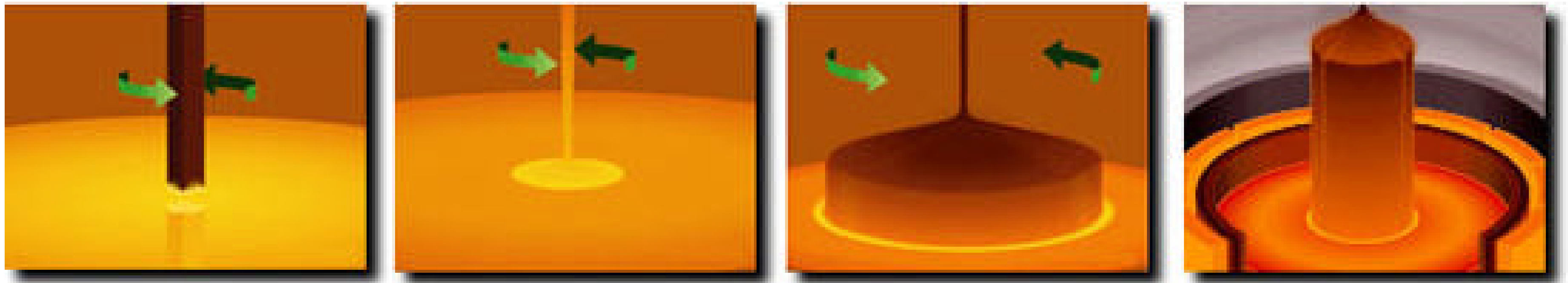


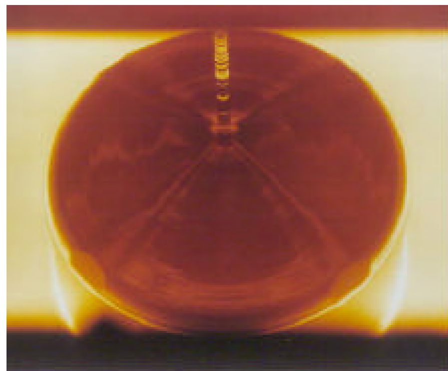
CZ Crystal Pullers

Mitsubish Materials Silicon

Source: http://www.fullman.com/semiconductors/_crystalgrowing.html

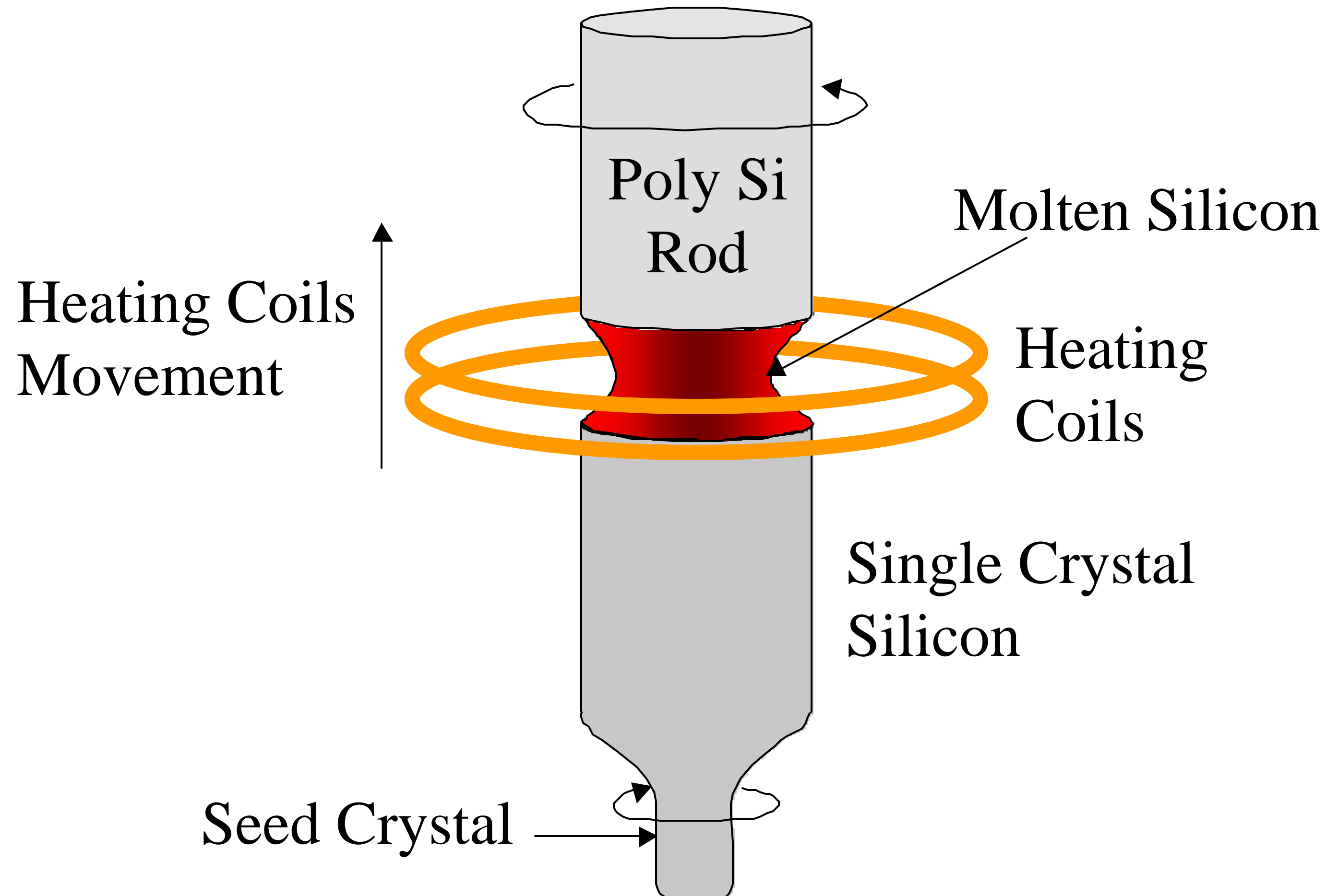
CZ Crystal Pulling





Source: http://www.fullman.com/semiconductors/_crystalgrowing.html

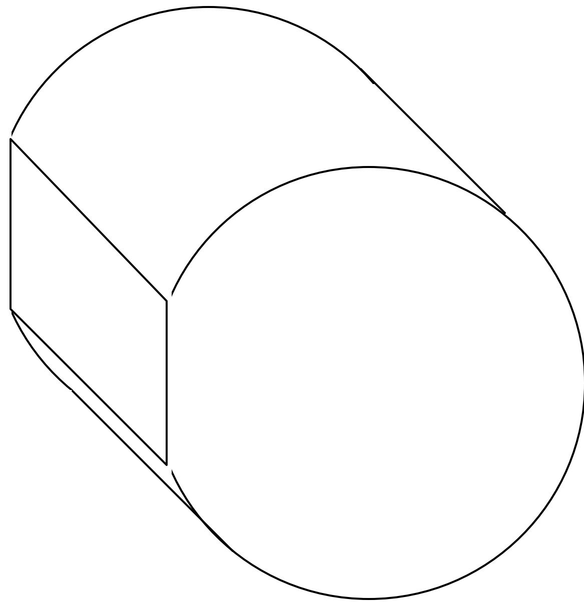
Floating Zone Method



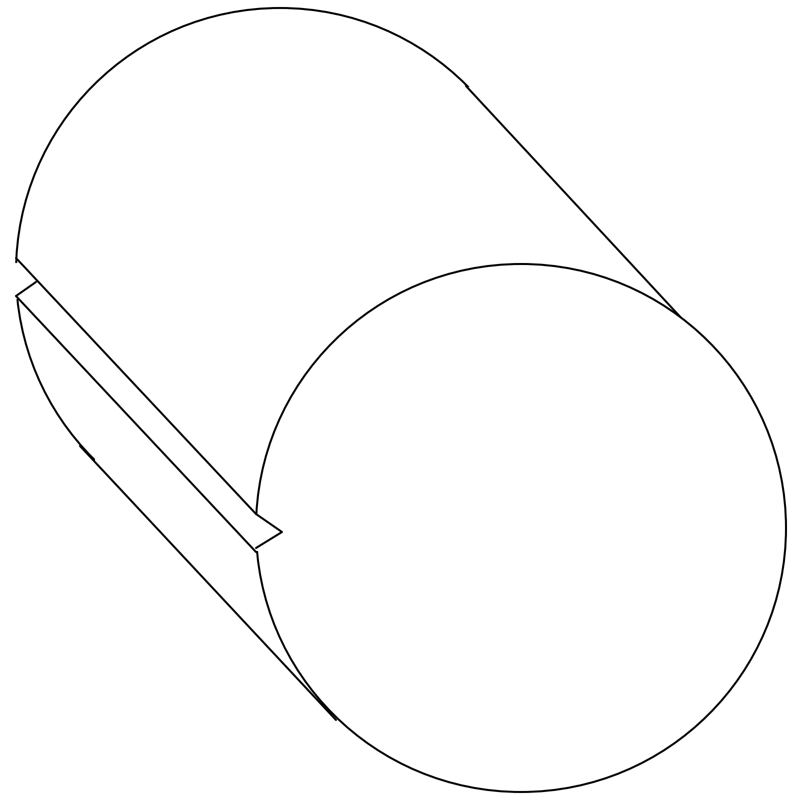
Comparison of the Two Methods

- CZ method is more popular
  - Cheaper
  - Larger wafer size (300 mm in production)
  - Reusable materials
- Floating Zone
  - Pure silicon crystal (no crucible)
  - More expensive, smaller wafer size (150 mm)
  - Mainly for power devices.

Ingot Polishing, Flat, or Notch

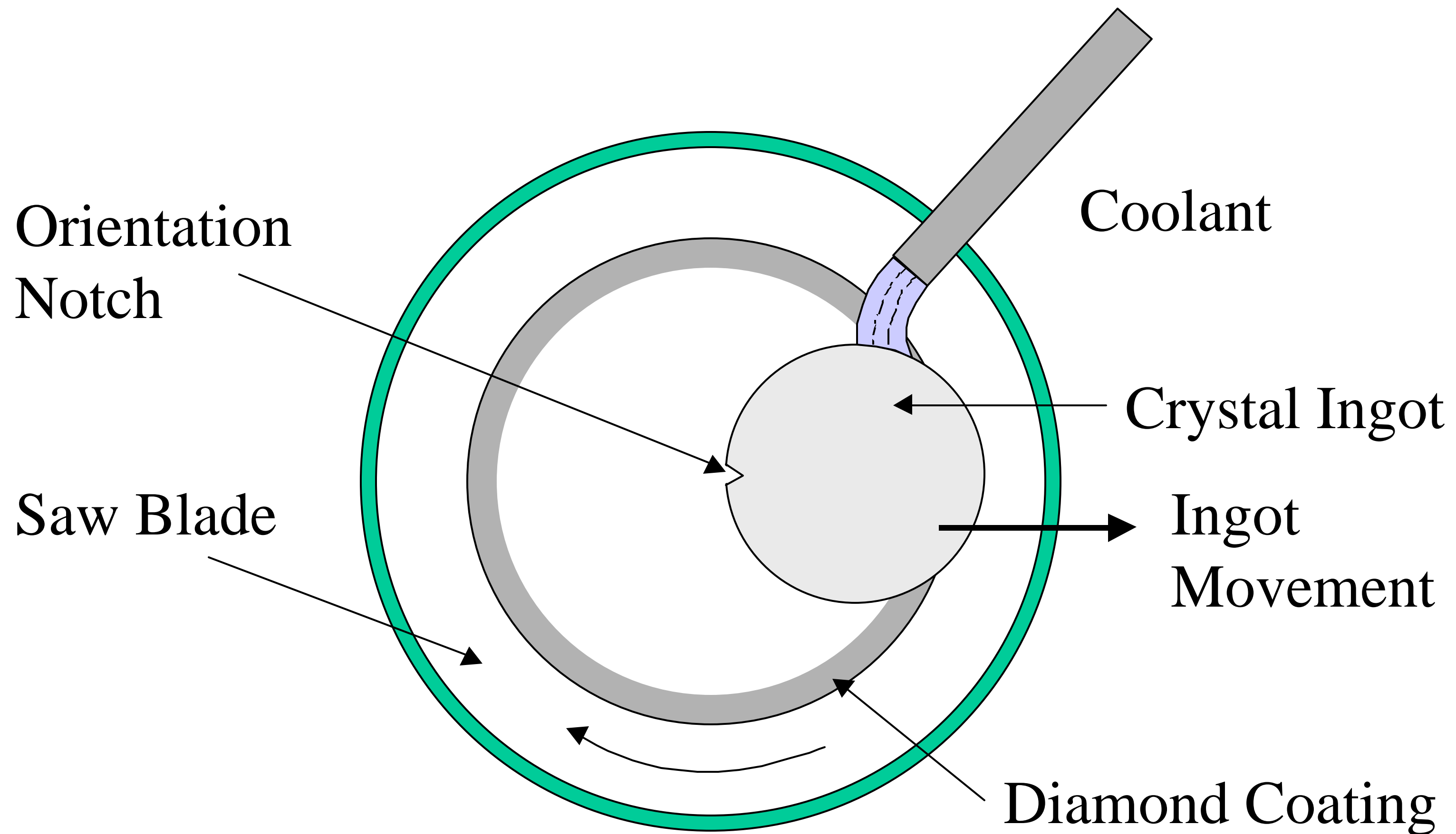


Flat, 150 mm and smaller



Notch, 200 mm and larger

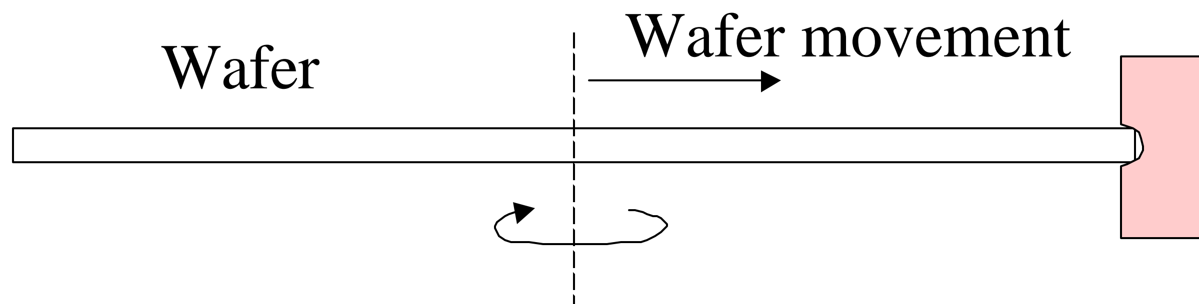
Wafer Sawing



Parameters of Silicon Wafer

Wafer Size (mm)	**Thickness** (μm)	**Area** (cm^2)	**Weight** (grams)
50.8 (2 in) 76.2 (3in)	279 381	20.26 45.61	1.32 4.05
100	525	78.65	9.67
125	625	112.72	17.87
150	675	176.72	27.82
200	725	314.16	52,98
300	775	706.21	127.62

Wafer Edge Rounding



Wafer Before Edge Rounding

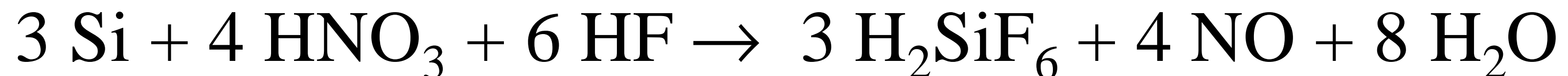
Wafer After Edge Rounding

Wafer Lapping

- Rough polished
- conventional, abrasive, slurry-lapping
- To remove majority of surface damage
- To create a flat surface

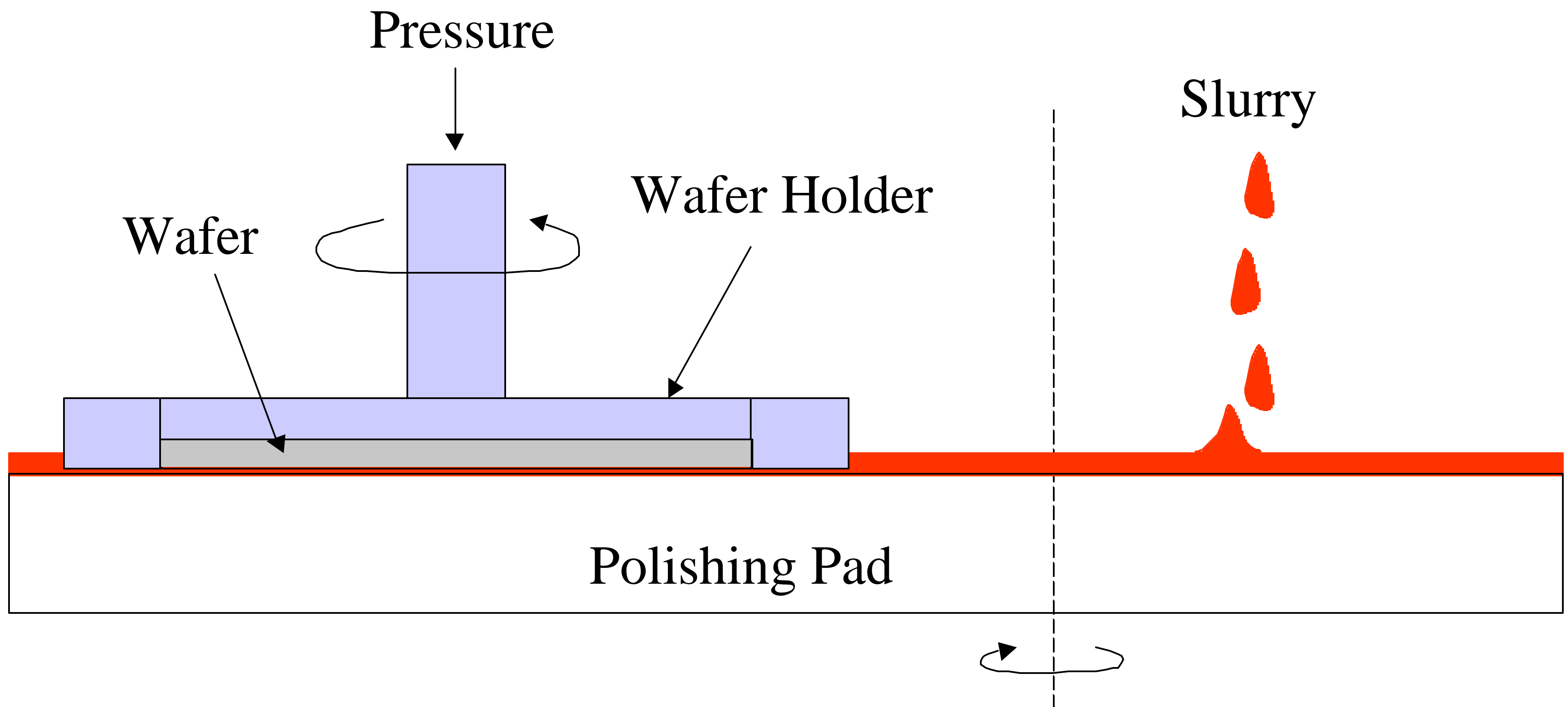
Wet Etch

- Remove defects from wafer surface
- 4:1:3 mixture of HNO_3 (79 wt% in H_2O), HF (49 wt% in H_2O), and pure CH_3COOH.
- Chemical reaction:

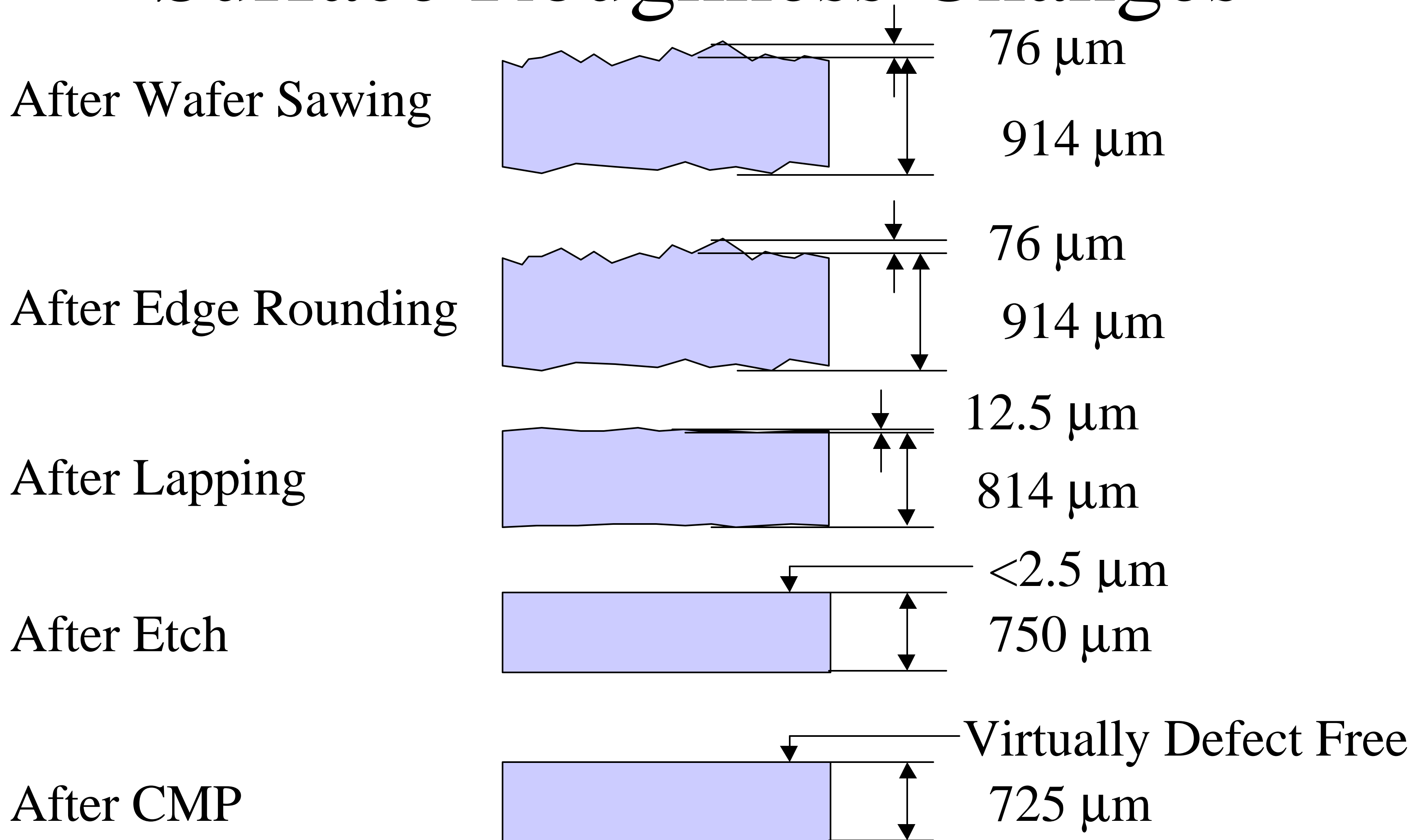


$$3\ Si + 4\ HNO_3 + 6\ HF \rightarrow 3\ H_2SiF_6 + 4\ NO + 8\ H_2O$$

Chemical Mechanical Polishing



200 mm Wafer Thickness and Surface Roughness Changes



Epitaxy Grow

- Definition
- Purposes
- Epitaxy Reactors
- Epitaxy Process

Epitaxy: Definition

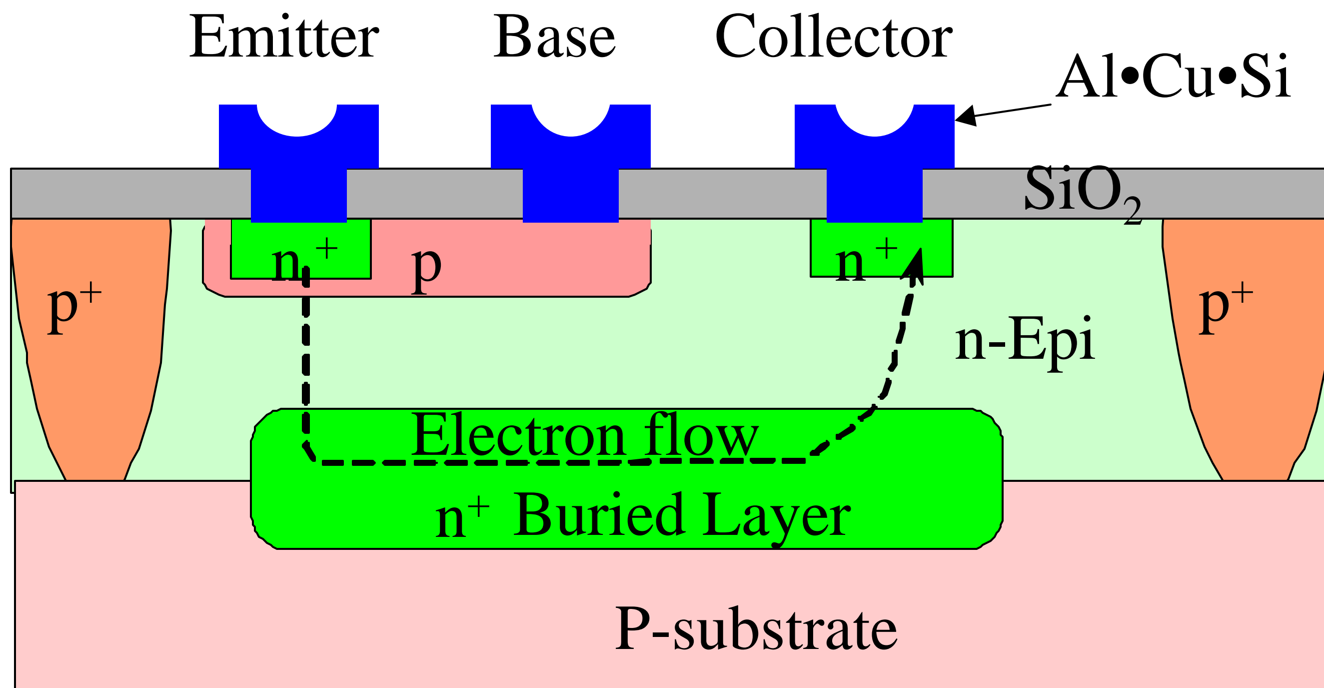
- Greek origin
- *epi*: upon
- *taxy*: orderly, arranged

- Epitaxial layer is a single crystal layer on a single crystal substrate.

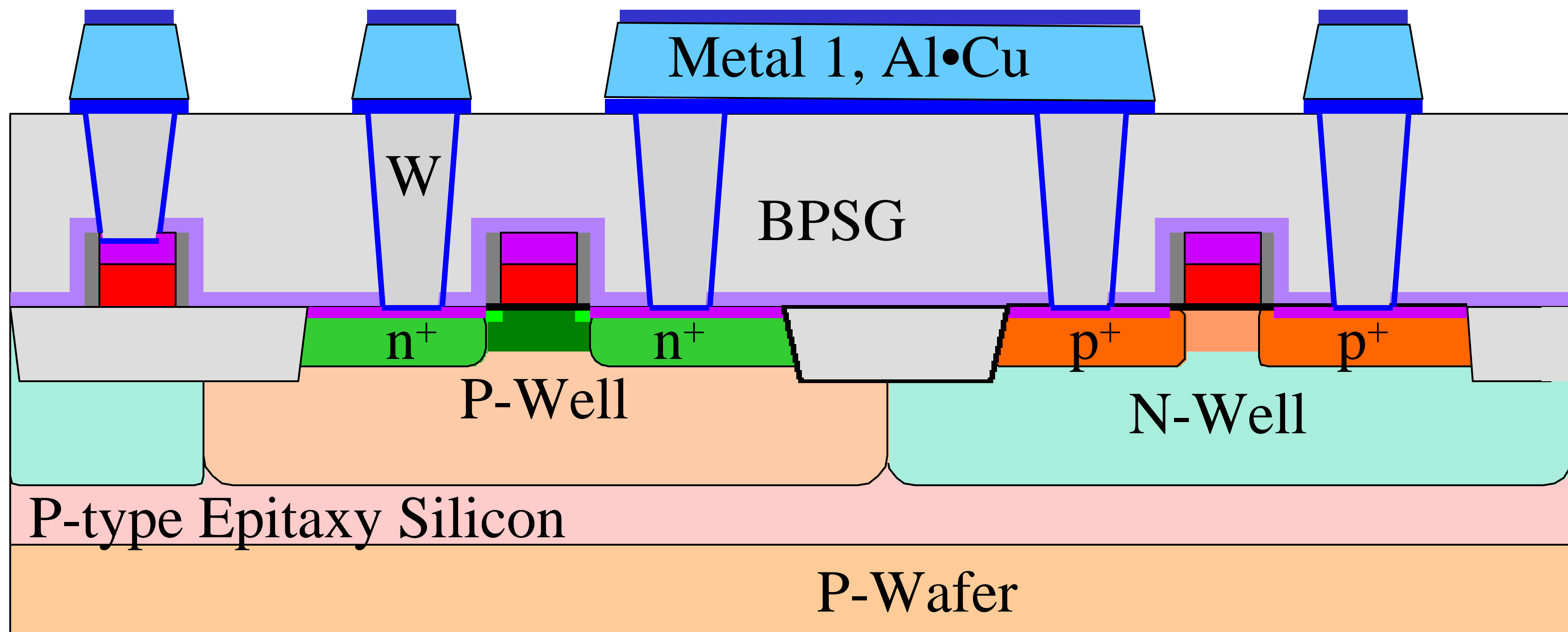
Epitaxy: Purpose

- Barrier layer for bipolar transistor
  - Reduce collector resistance while keep high breakdown voltage.
  - Only available with epitaxy layer.
- Improve device performance for CMOS and DRAM because much lower oxygen, carbon concentration than the wafer crystal.

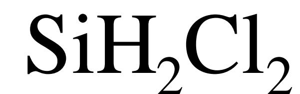
Epitaxy Application, Bipolar Transistor



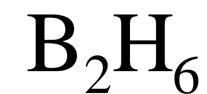
Epitaxy Application: CMOS



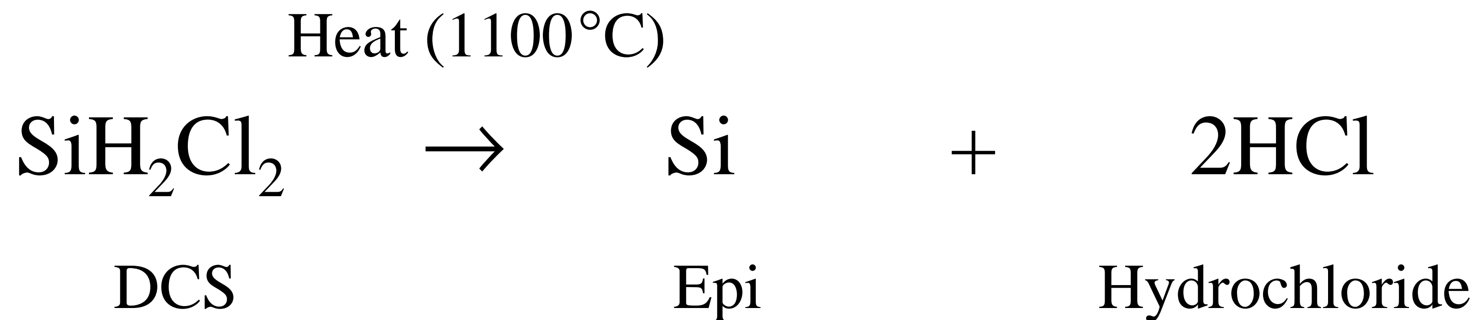
Silicon Source Gases

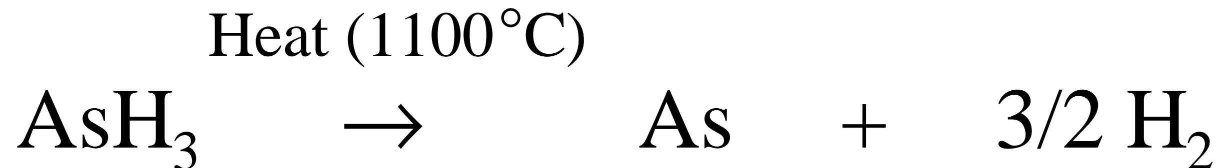
Silane		SiH_4
Dichlorosilane	DCS	 SiH_2Cl_2
Trichlorosilane	TCS	$SiHCl_3$
Tetrachlorosilane		$SiCl_4$

Dopant Source Gases

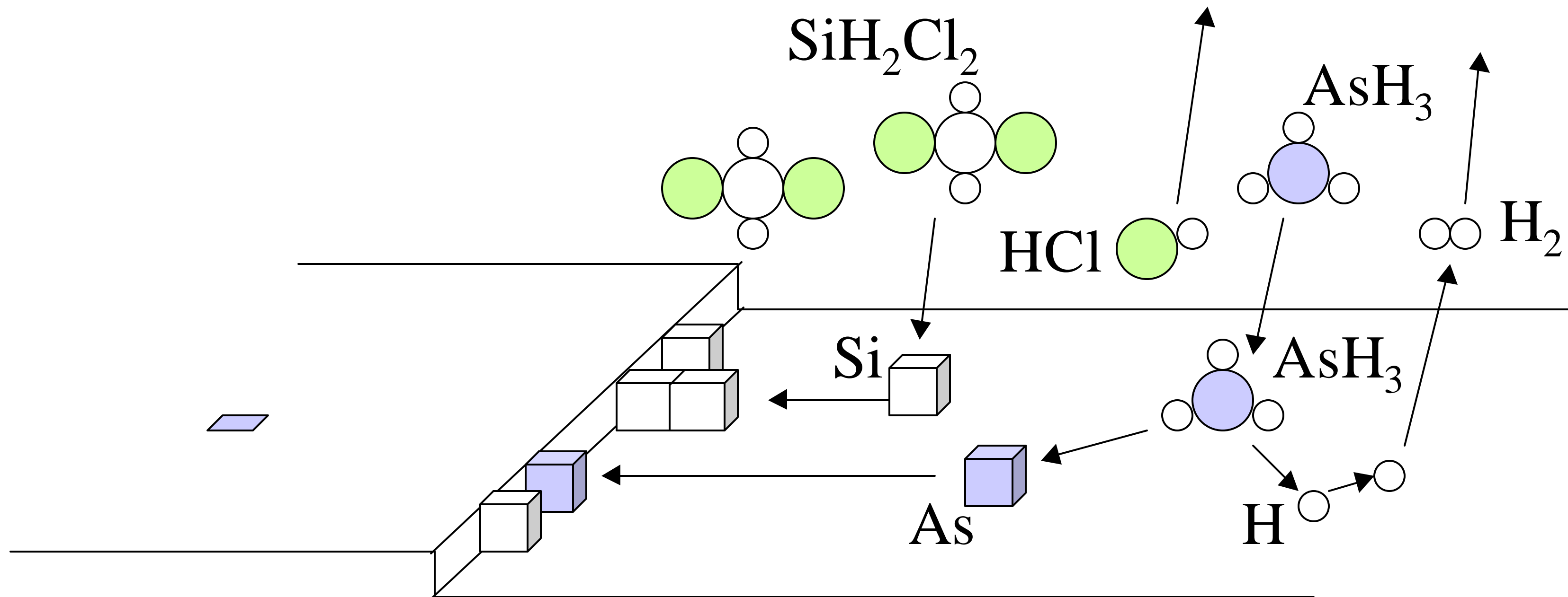
Diborane	 B_2H_6
Phosphine	PH_3
Arsine	AsH_3

DCS Epitaxy Grow, Arsenic Doping

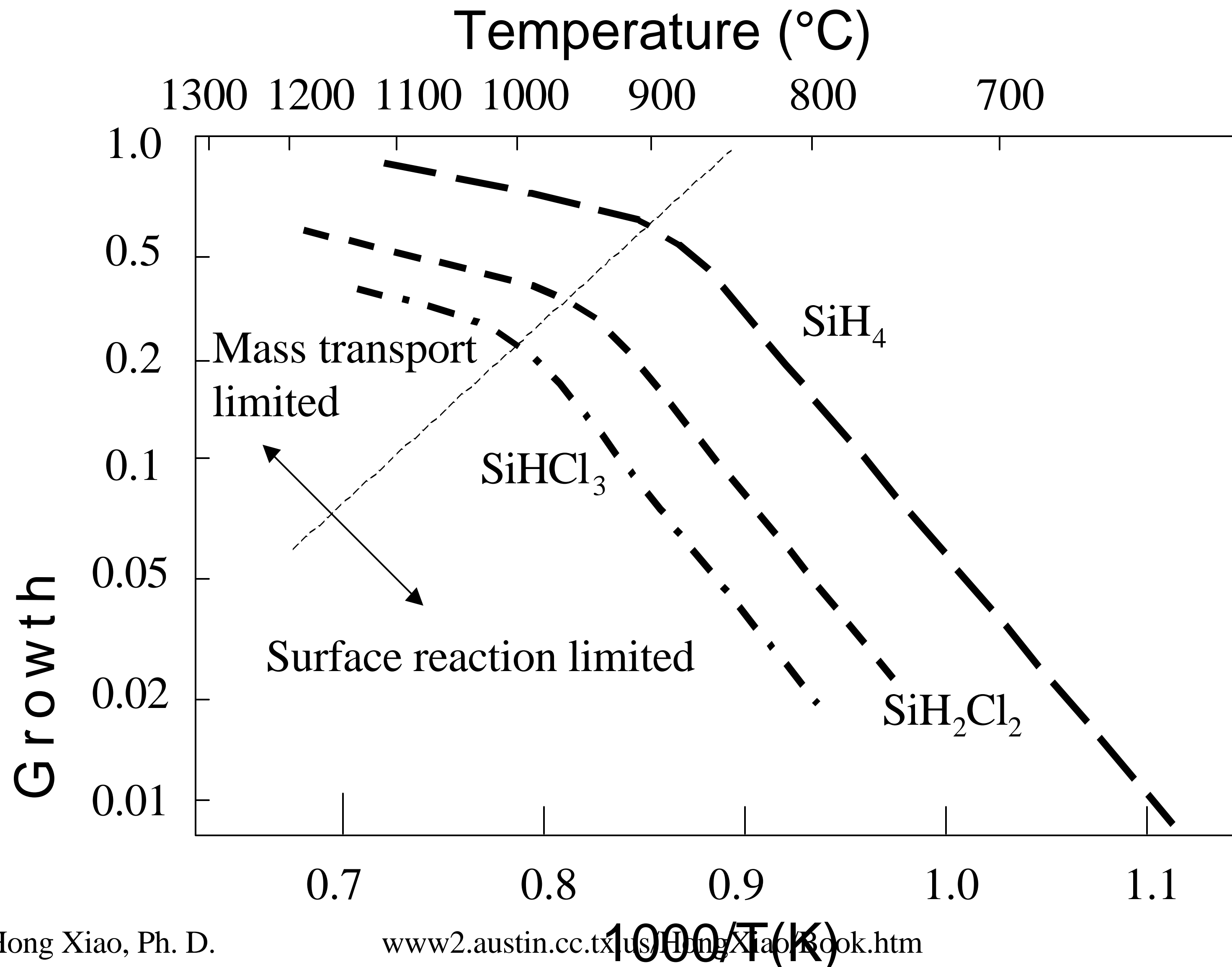




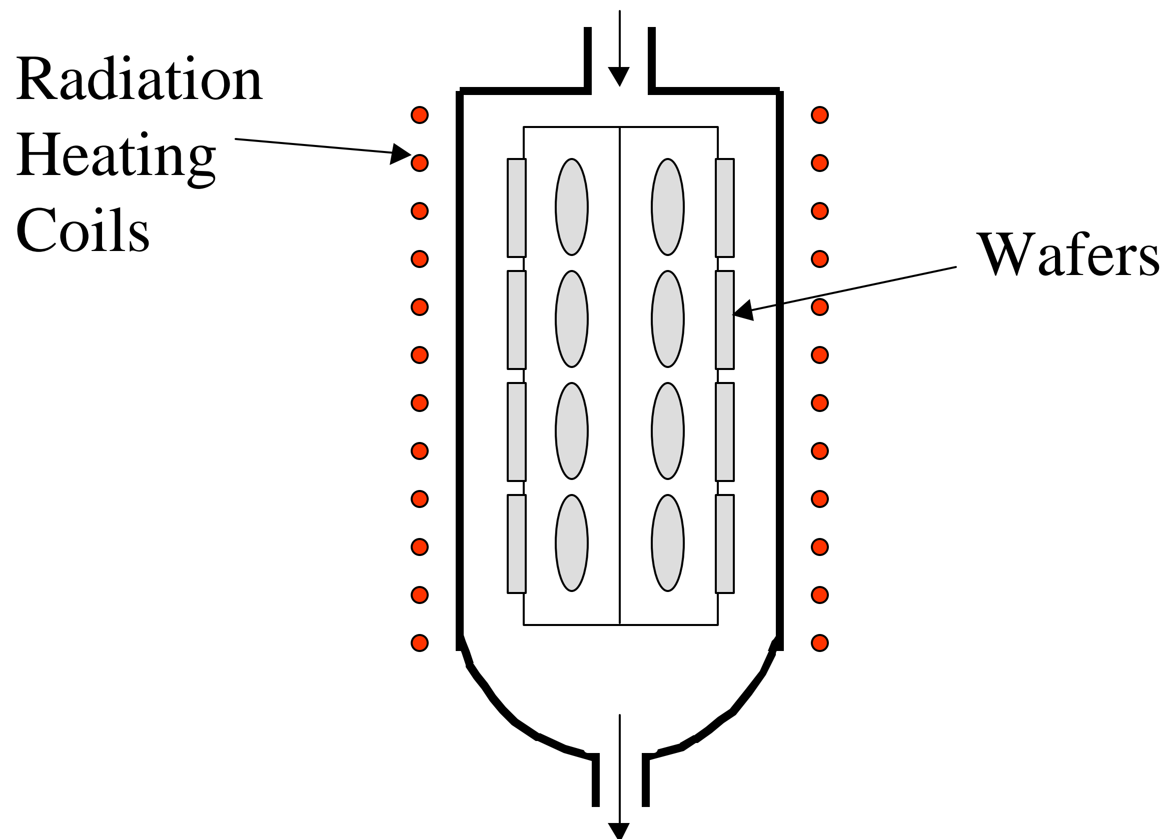
Schematic of DCS Epi Grow and Arsenic Doping Process



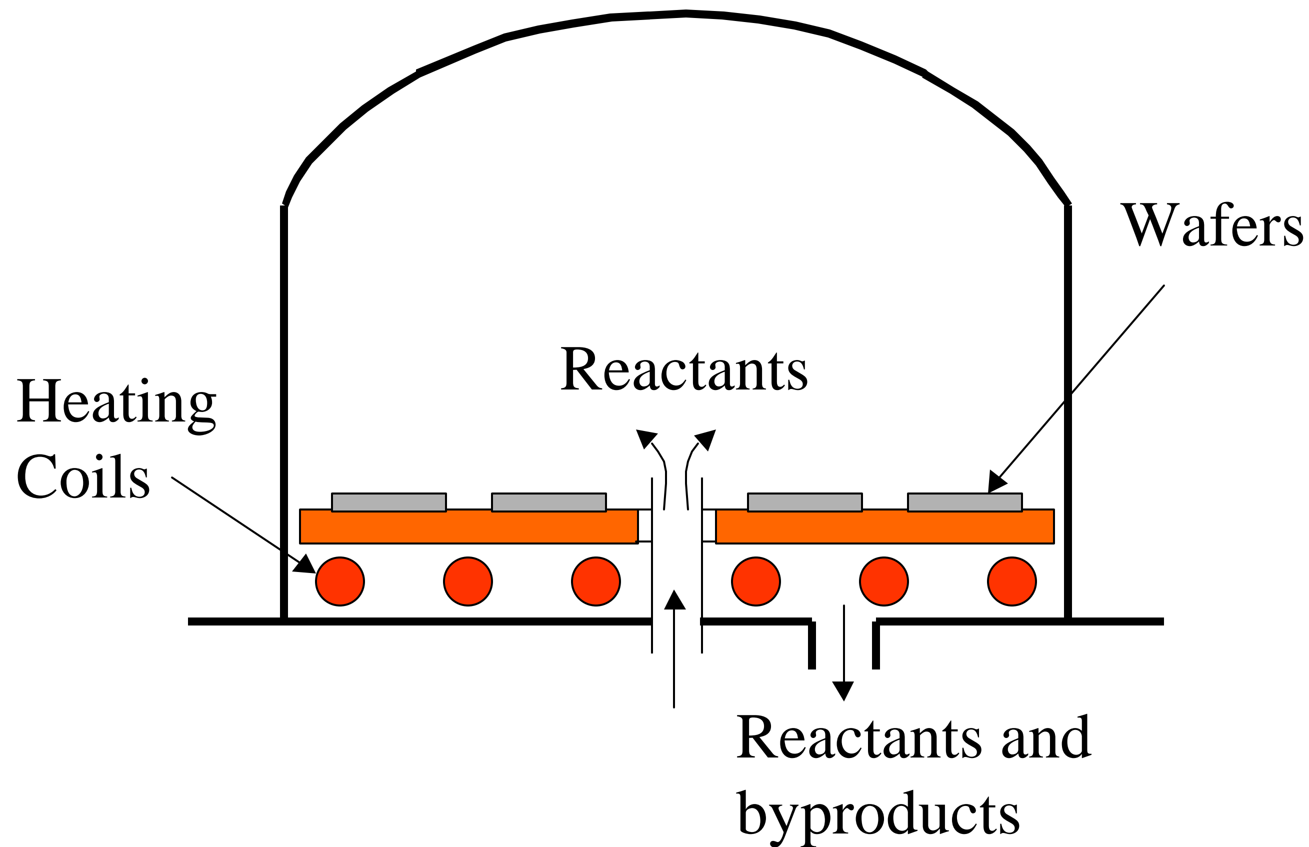
Epitaxial Silicon Growth Rate Trends



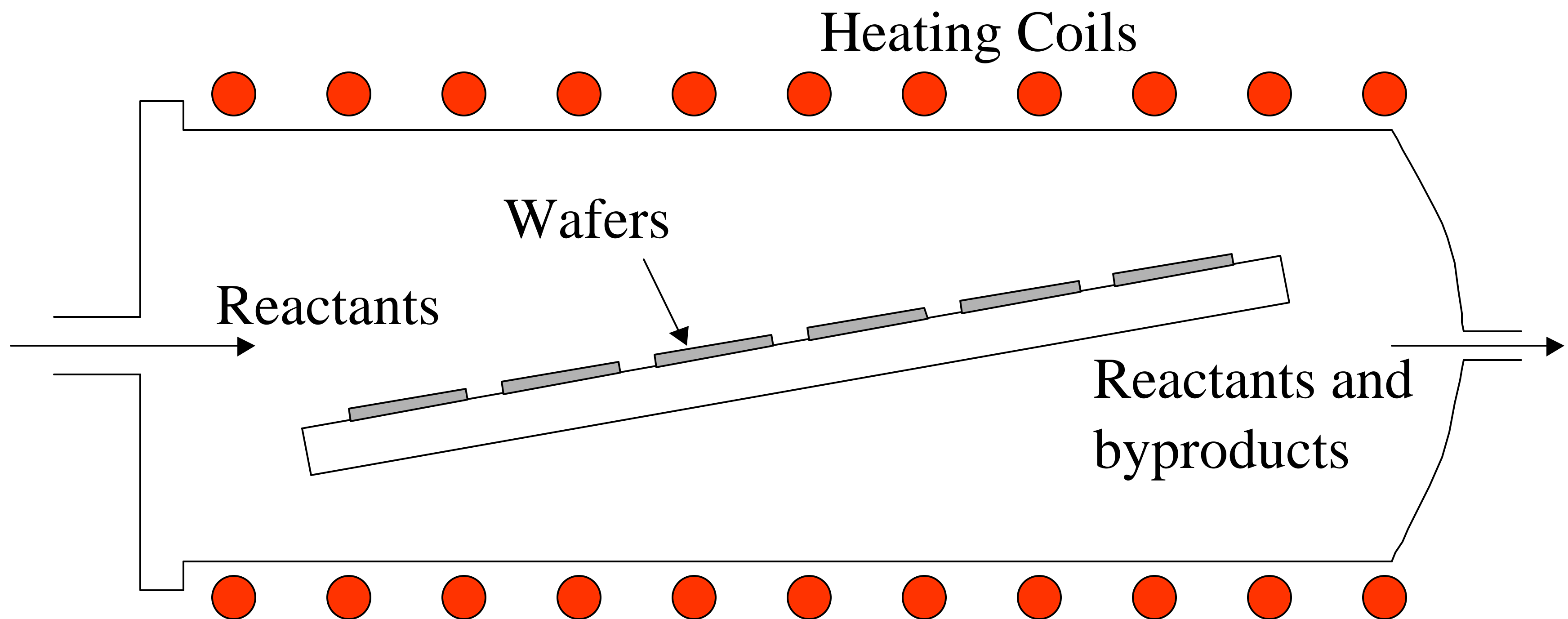
Barrel Reactor



Vertical Reactor



Horizontal Reactor



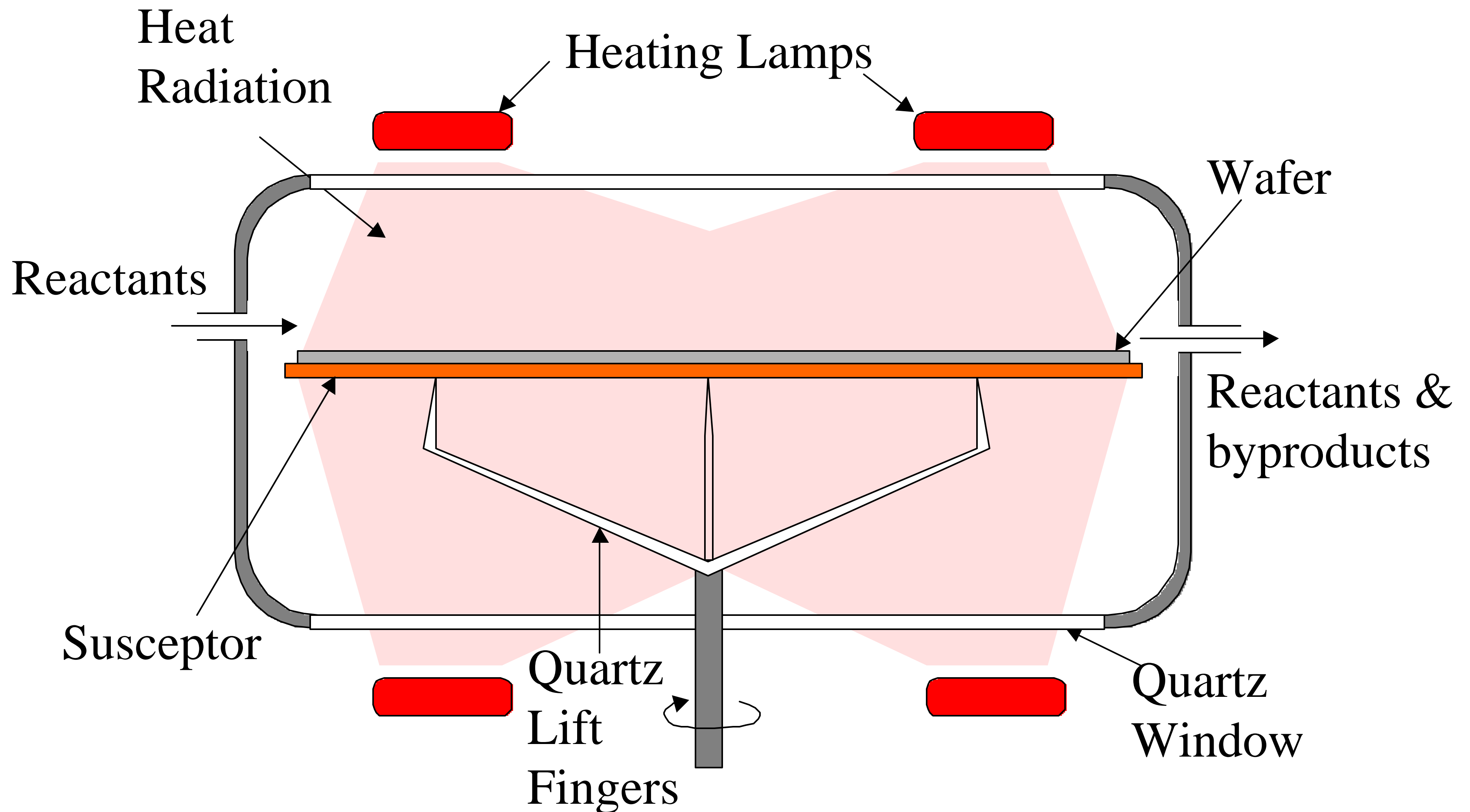
Epitaxy Process, Batch System

- Hydrogen purge, temperature ramp up
- HCl clean
- Epitaxial layer grow
- Hydrogen purge, temperature cool down
- Nitrogen purge
- Open Chamber, wafer unloading, reloading

Single Wafer Reactor

- Sealed chamber, hydrogen ambient
- Capable for multiple chambers on a mainframe
- Large wafer size (to 300 mm)
- Better uniformity control

Single Wafer Reactor



Epitaxy Process, Single Wafer System

- Hydrogen purge, clean, temperature ramp up
- Epitaxial layer grow
- Hydrogen purge, heating power off
- Wafer unloading, reloading

- In-situ HCl clean,

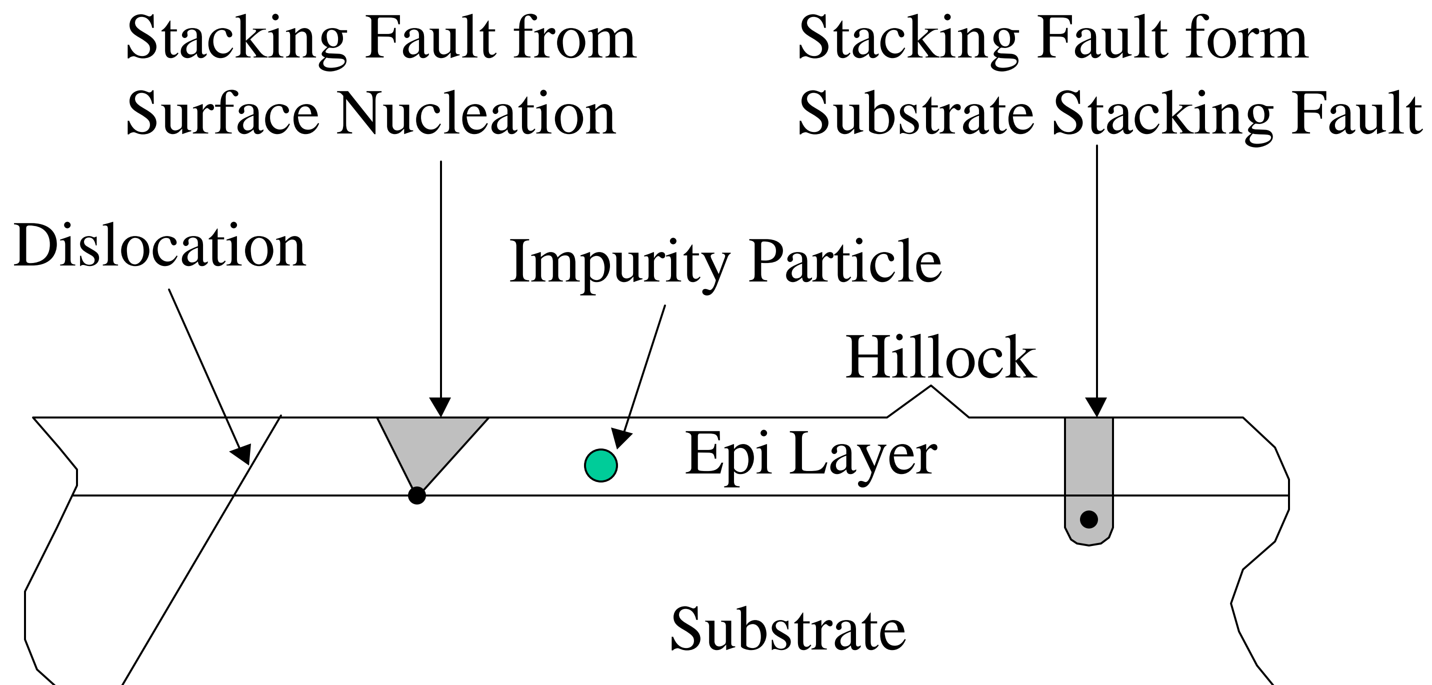
Why Hydrogen Purge

- Most systems use nitrogen as purge gas
- Nitrogen is a very stable abundant
- At > 1000 °C, N_2 can react with silicon
- SiN on wafer surface affects epi deposition
- H_2 is used for epitaxy chamber purge
- Clean wafer surface by hydrides formation

Properties of Hydrogen

Name	Hydrogen
Symbol	H
Atomic number	1
Atomic weight	1.00794
Discoverer	Henry Cavendish
Discovered at	England
Discovery date	1766
Origin of name	From the Greek words "hydro" and "genes" meaning "water" and "generator"
Molar volume	11.42 cm^3
Velocity of sound	1270 m/sec
Refractive index	1.000132
Melting point	-258.99 C
Boiling point	-252.72 C
Thermal conductivity	0.1805 W m^{-1} K^{-1}

Defects in Epitaxy Layer



After S.M. Zse's *VLSI Technology*

Future Trends

- Larger wafer size
- Single wafer epitaxial grow
- Low temperature epitaxy
- Ultra high vacuum (UHV, to 10^{-9} Torr)
- Selective epitaxy

Summary

- Silicon is abundant, cheap and has strong, stable and easy grown oxide.
- <100> and <111>
- CZ and floating zone, CZ is more popular
- Sawing, edging, lapping, etching and CMP

Summary

- Epitaxy: single crystal on single crystal
- Needed for bipolar and high performance CMOS, DRAM.
- Silane, DCS, TCS as silicon precursors
- B_2H_6 as P-type dopant
- PH_3 and AsH_3 as N-type dopants
- Batch and single wafer systems

Chapter 5
Thermal Processes

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Objective

- List four thermal processes
- Describe thermal process in IC fabrication
- Describe thermal oxidation process
- Explain the advantage of RTP over furnace
- Relate your job or products to the processes

Topics

- Introduction
- Hardware
- Oxidation
- Diffusion
- Annealing
  - Post-Implantation
  - Alloying
  - Reflow
- High Temp CVD
  - Epi
  - Poly
  - Silicon Nitride
- RTP
  - RTA
  - RTP
- Future Trends

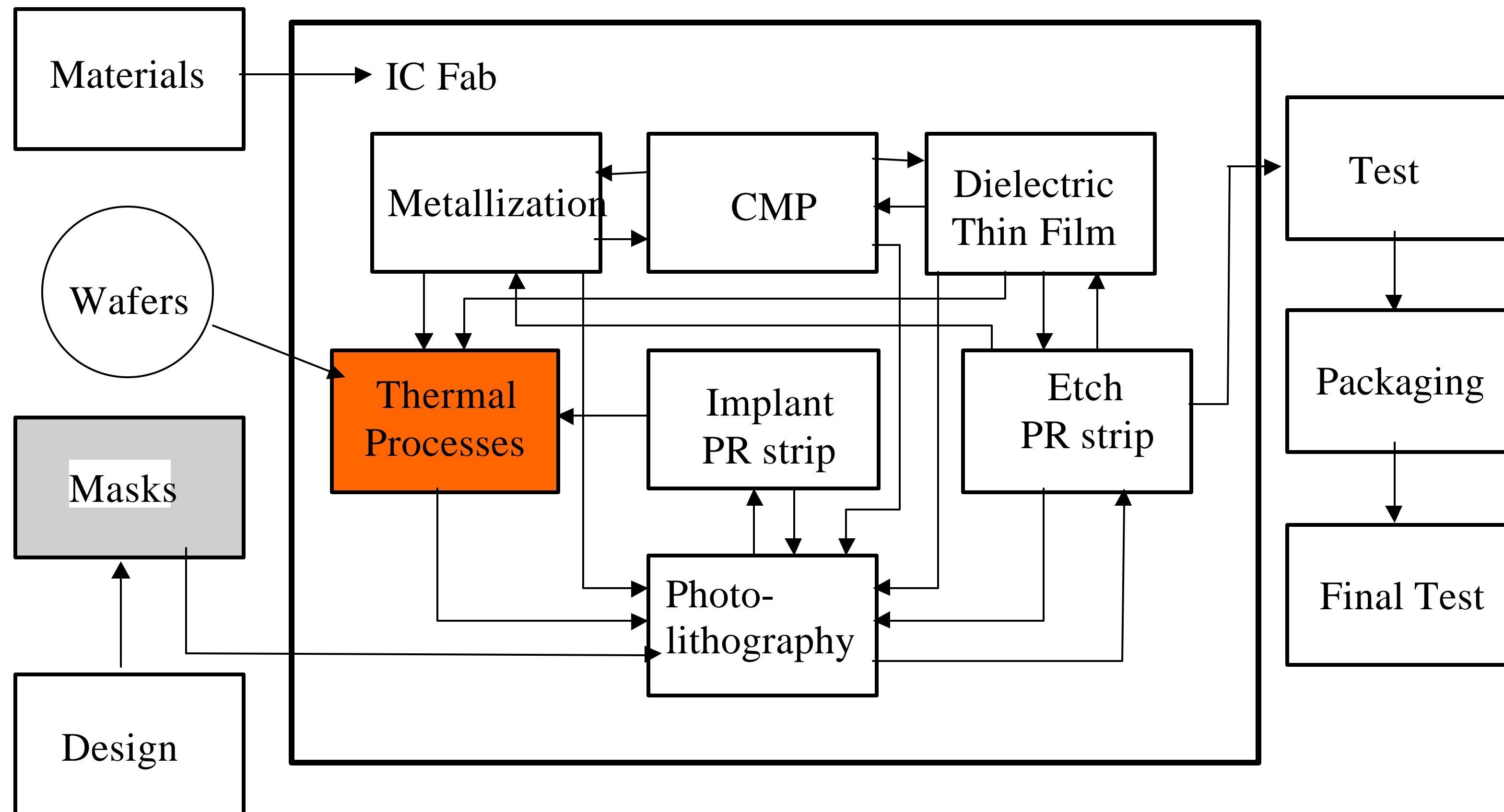
Definition

- Thermal processes are the processes operate at high temperature, which is usually higher than melting point of aluminum.
- They are performed in the front-end of the semiconductor process, usually in high temperature furnace commonly called diffusion furnace.

Introduction

- Advantages of Silicon
  - Abundant, cheap
  - Stable and useful oxide
- Oxidation and Diffusion are the backbone processes in early IC fabrications

Thermal Processes in IC Fabrication

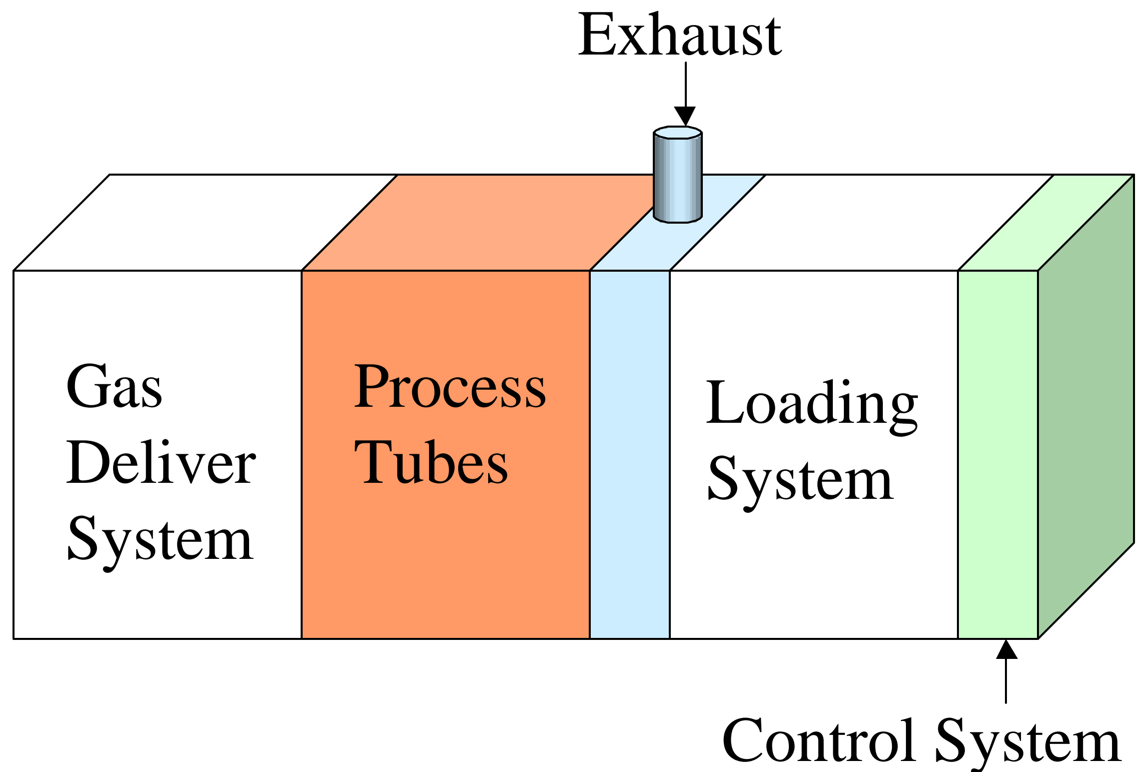


Hardware Overview

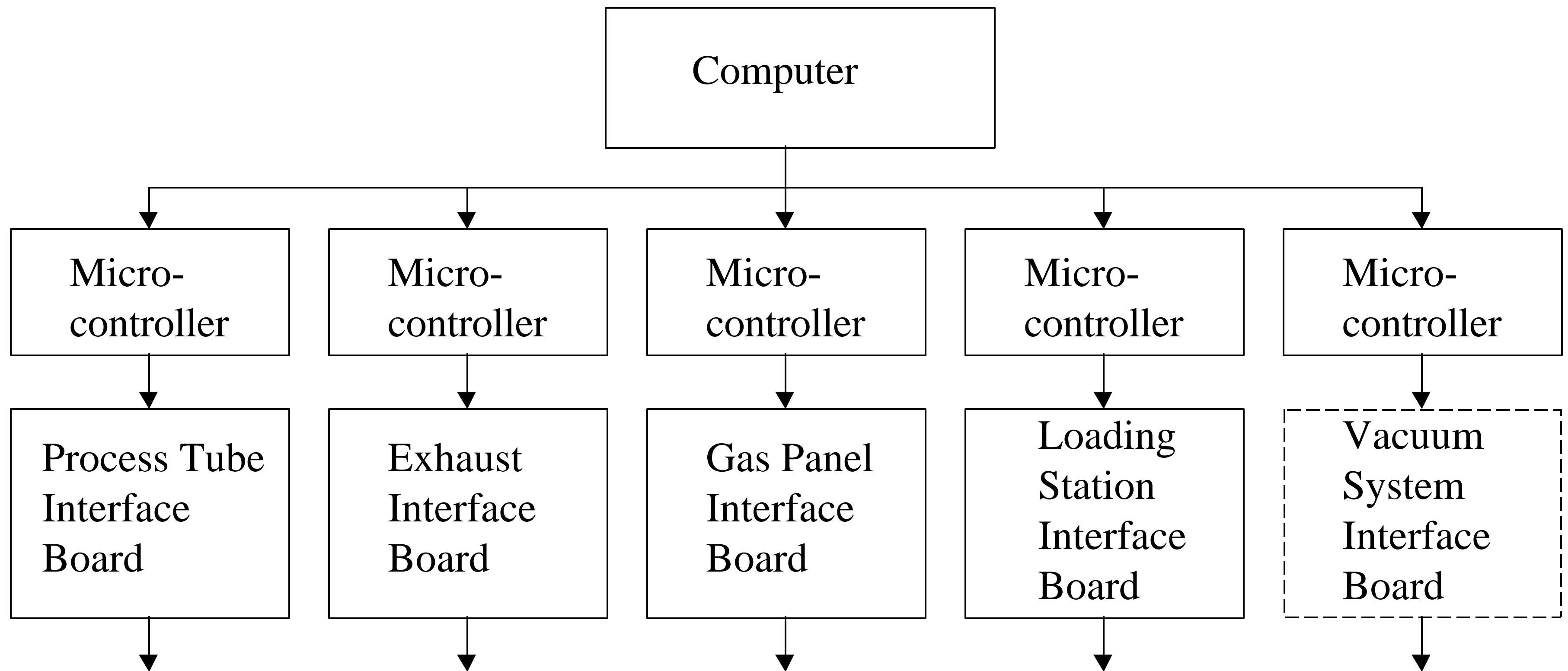
Horizontal Furnace

- Commonly used tool for thermal processes
- Often be called as *diffusion furnace*
- Quartz tube inside a ceramic liner called muffle
- Multi-tube system

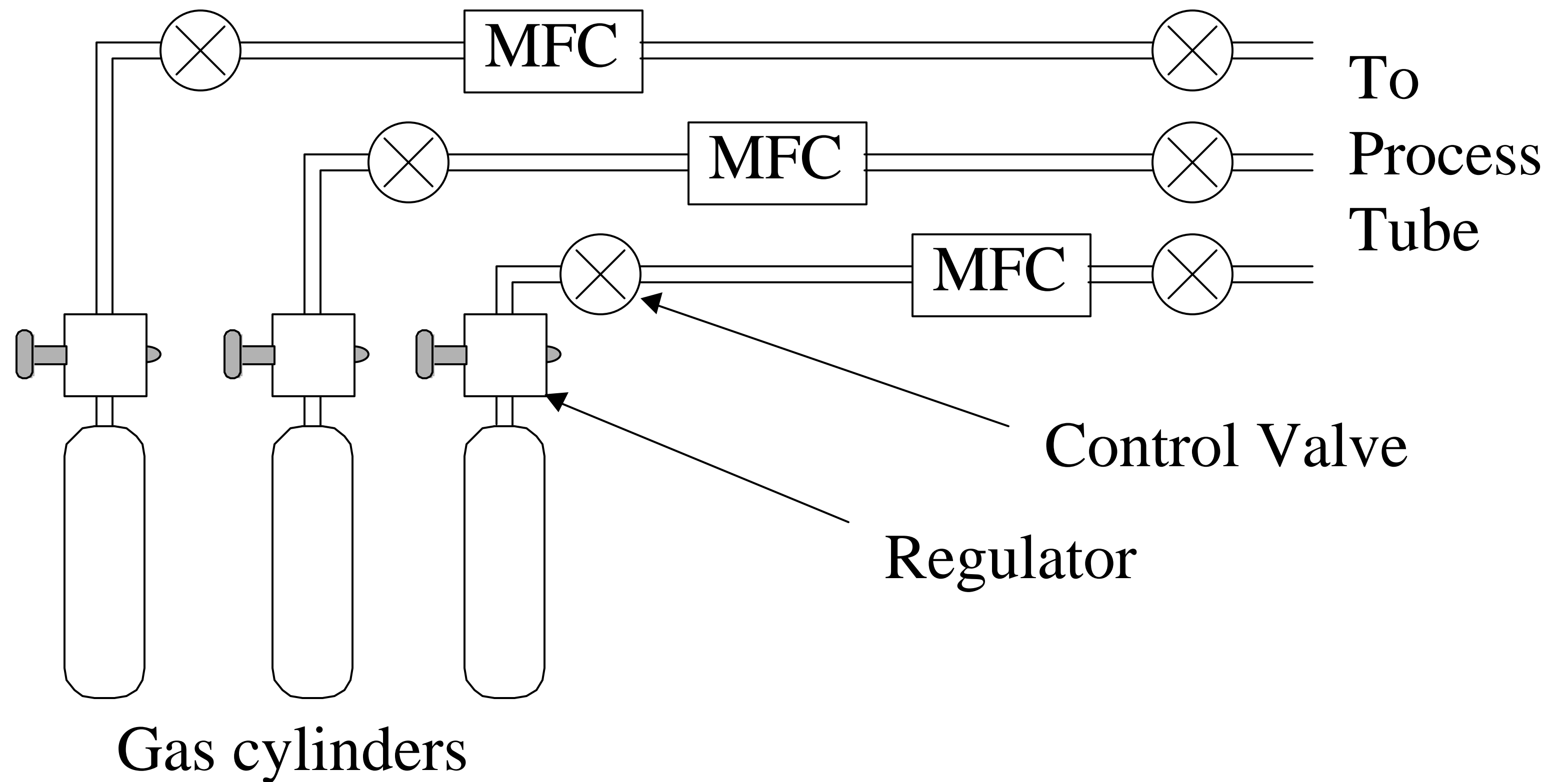
Layout of a Horizontal Furnace



Control System



Gas Deliver System



Source Cabinet

- Source Gases
  - Oxygen
  - Water Vapor
  - Nitrogen
  - Hydrogen
- Gas control panel
- Gas flow controller
- Gas flow meter

Oxidation Sources

- Dry Oxygen
- Water vapor sources
  - Bubblers
  - Flash systems
- Hydrogen and oxygen, $H_2 + O_2 \rightarrow H_2O$
- Chlorine sources, for minimized mobile ions in gate oxidation
  - Anhydrous hydrogen chloride HCl
  - Trichloroethylene (TCE), Trichloroethane (TCA)

Diffusion Sources

- P-type dopant
  - B_2H_6, burnt chocolate, sickly sweet odor
  - Poisonous, flammable, and explosive
- N-type dopants
  - PH_3, rotten fish smell
  - AsH_3, garlic smell
  - Poisonous, flammable, and explosive
- Purge gas
  - N_2

Deposition Sources

- Silicon source for poly and nitride deposition:
  - Silane, SiH_4, pyrophoric, toxic and explosive
  - DCS, SiH_2Cl_2, extremely flammable
- Nitrogen source for nitride deposition:
  - NH_3, pungent, irritating odor, corrosive
- Dopants for polysilicon deposition
  - B_2H_6, PH_3 and AsH_3
- Purge gas
  - N_2

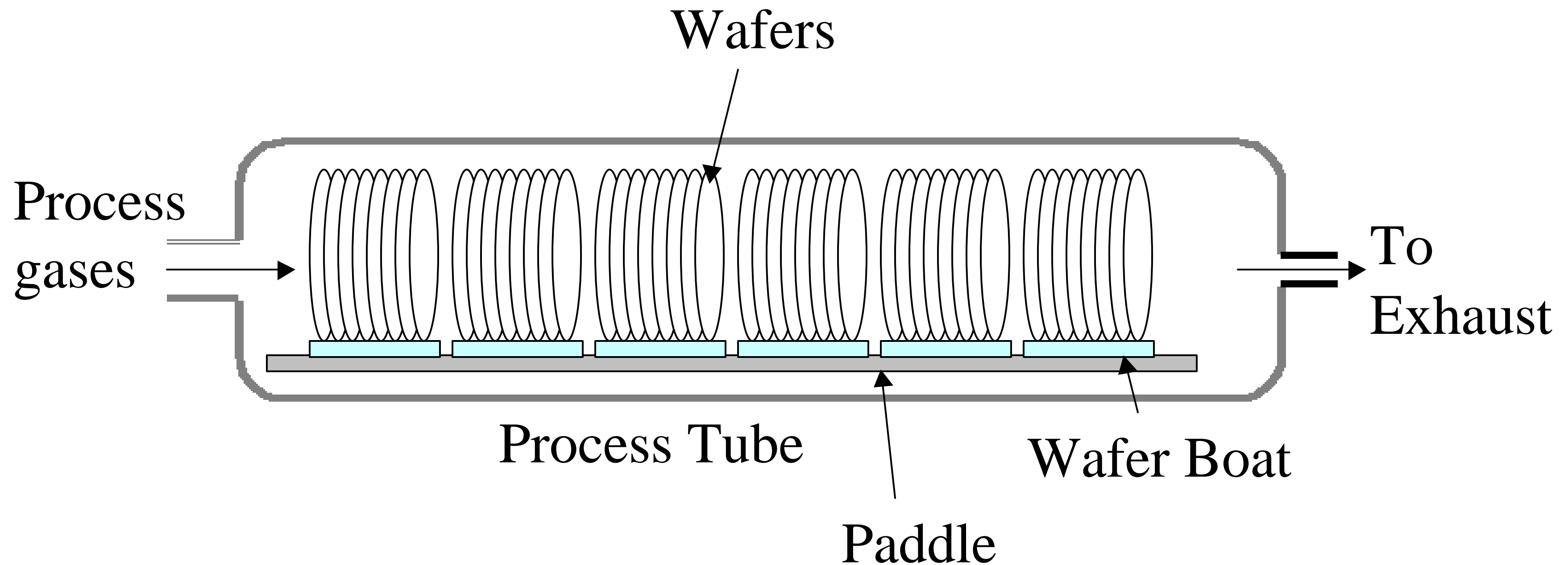
Anneal Sources

- High purity N_2, is used for most anneal processes.
- H_2O sometimes used as ambient for PSG or BPSG reflow.
- O_2 is used for USG anneal after USG CMP in STI formation process.
- Lower grade N_2 is used for idle purge.

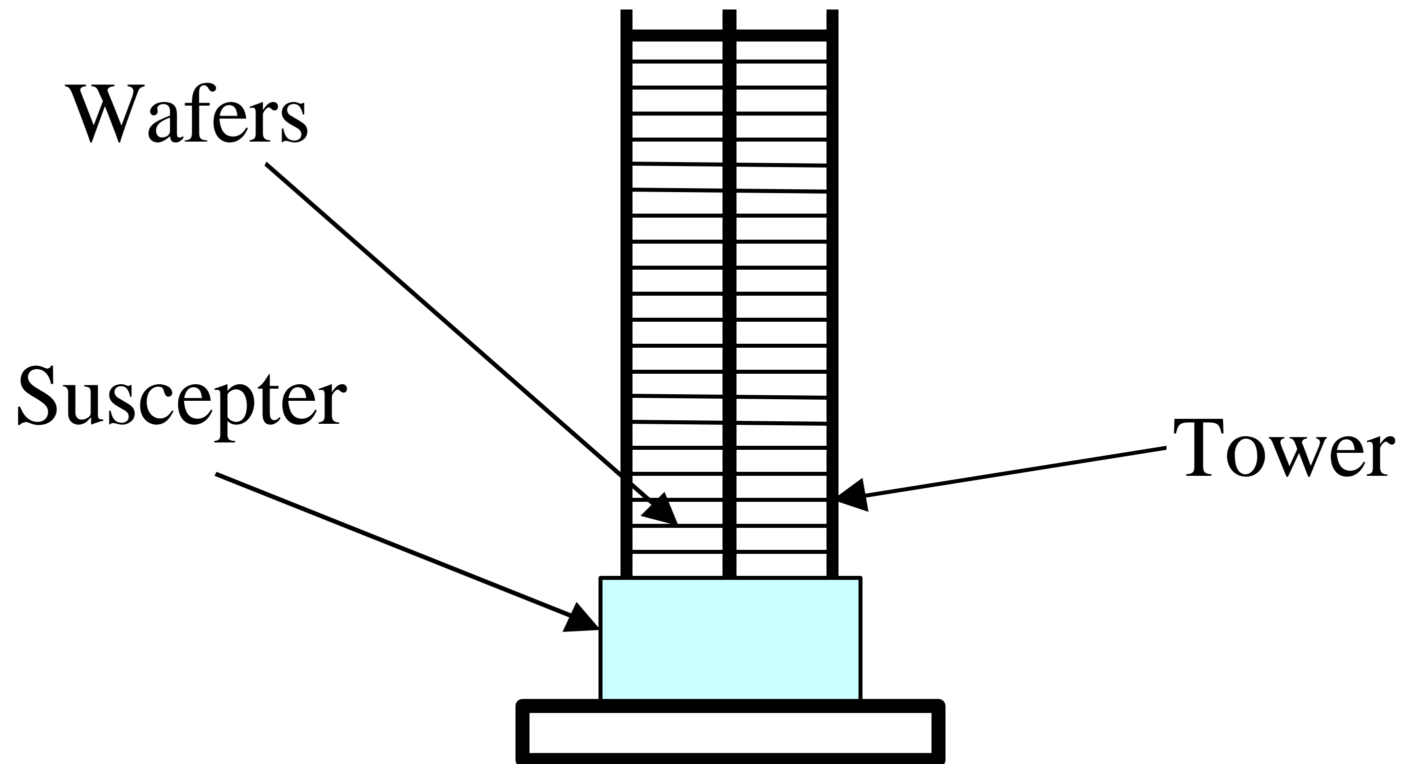
Exhaust System

- Removal of hazardous gases before release
- Poisonous, flammable, explosive and corrosive gases.
- Burn box removes most poisonous, flammable and explosive gases
- Scrubber removes burned oxide and corrosive gases with water.
- Treated gases exhaust to the atmosphere.

Wafer Loading, Horizontal System



Wafer Loading, Vertical System



Temperature Control

- Thermal processes are very sensitive to the temperature
- Precisely temperature control is vital
- ±0.5 °C at central zone
- ±0.05% at 1000 °C!

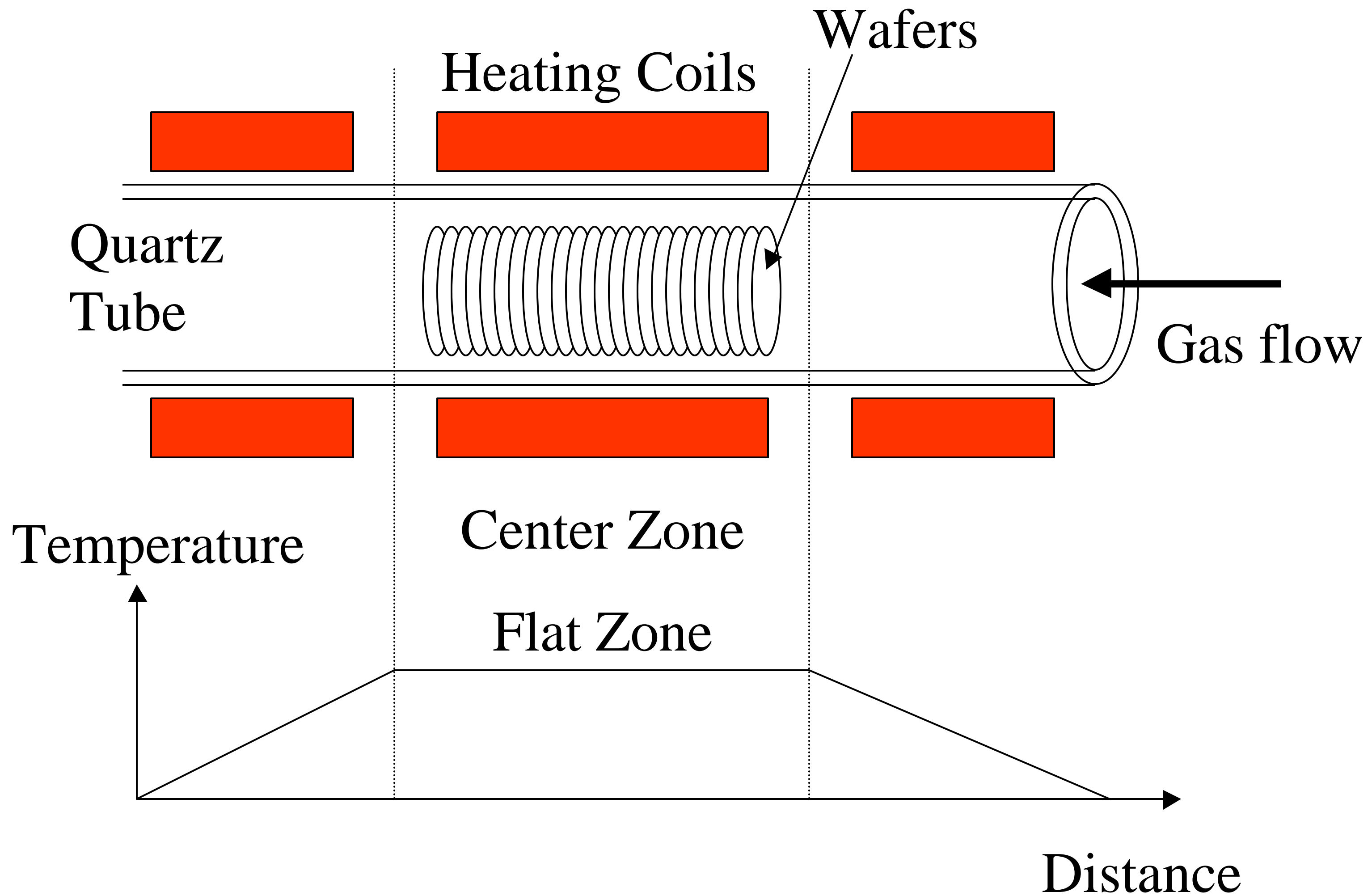
Temperature Control System

- Thermocouples touching the reaction tube
- Proportional band controllers feed the power to the heating coils
- The heating power is proportional to difference between setting point and measured value

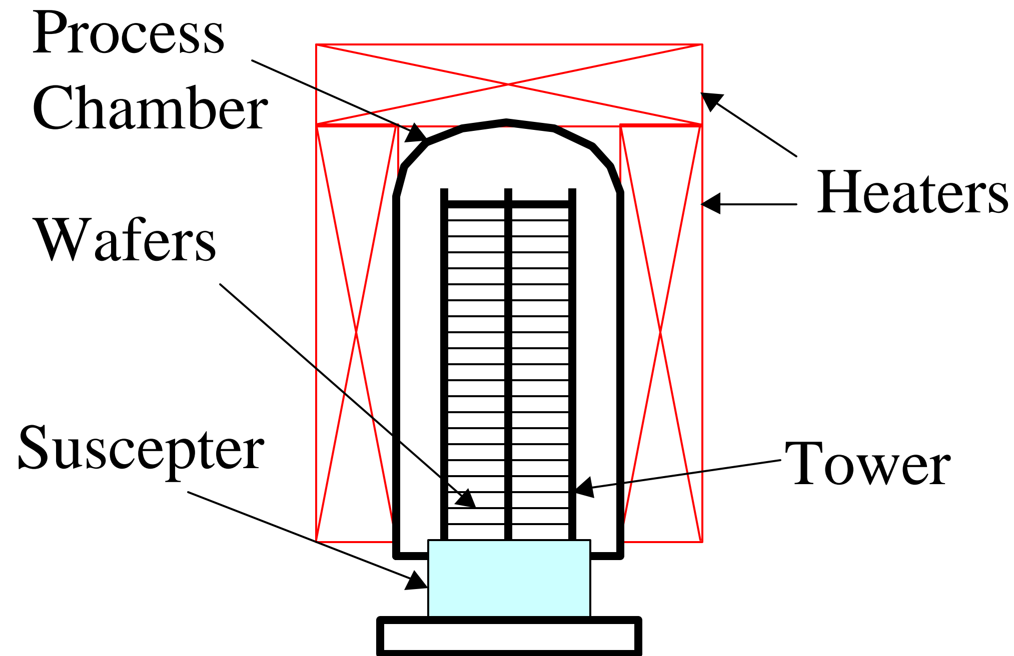
Reaction Chamber

- High-purity Quartz
  - Stability at high temperature
  - Basic Cleanliness
- Drawback
  - Fragility
  - Some metallic ions
  - Not a sodium barrier
  - Small flakes at > 1200 °C, *devitrification*

Horizontal Furnace



Vertical Furnace, Process Position



Quartz Tube

- Electric Fused
- Flame Fused
- Both of them as trace amount of metals
- Flame-fused tubes produced devices have better characteristics.

Quartz Tube Clean

- Very important especially for deposition furnace to prevent particle contamination
- Out side fab, ex-situ
  - Hydrofluoric acid (HF) tank
  - Remove a thin layer of quartz every time
  - limited tube lifetime
- In-situ clean
  - Plasma generator inside tube
  - Free fluorine from NF_3 etch away contaminant

Silicon Carbide Tube

- Pro
  - Higher thermal stability
  - Better metallic ion barrier
- Con
  - Heavier
  - More expensive

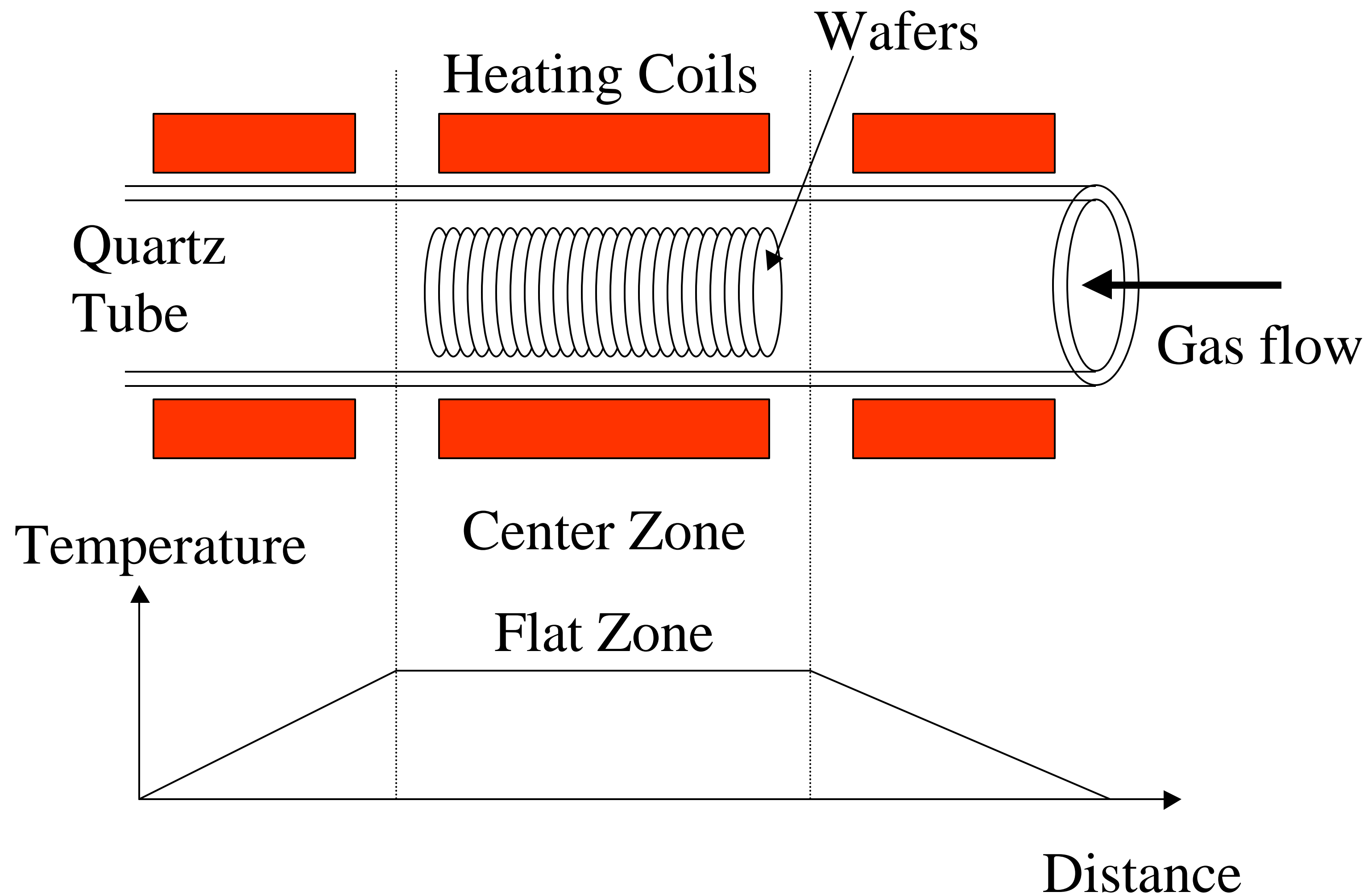
Temperature Control Anti-Warp Methods

- Ramping
  - Load wafer slowly at a lower temperature (idle temperature, ~ 800 °C)
  - Ramp temperature to process point after a short stabilization period
- Slow loading
  - 1 inch/min
  - thermal capacity of 200 six-inch wafers can drop temperature as much as 50 °C

Horizontal Furnace

- Contain 3 or 4 tubes (reaction chambers)
- Separate temperature control system for each tube

Horizontal Furnace



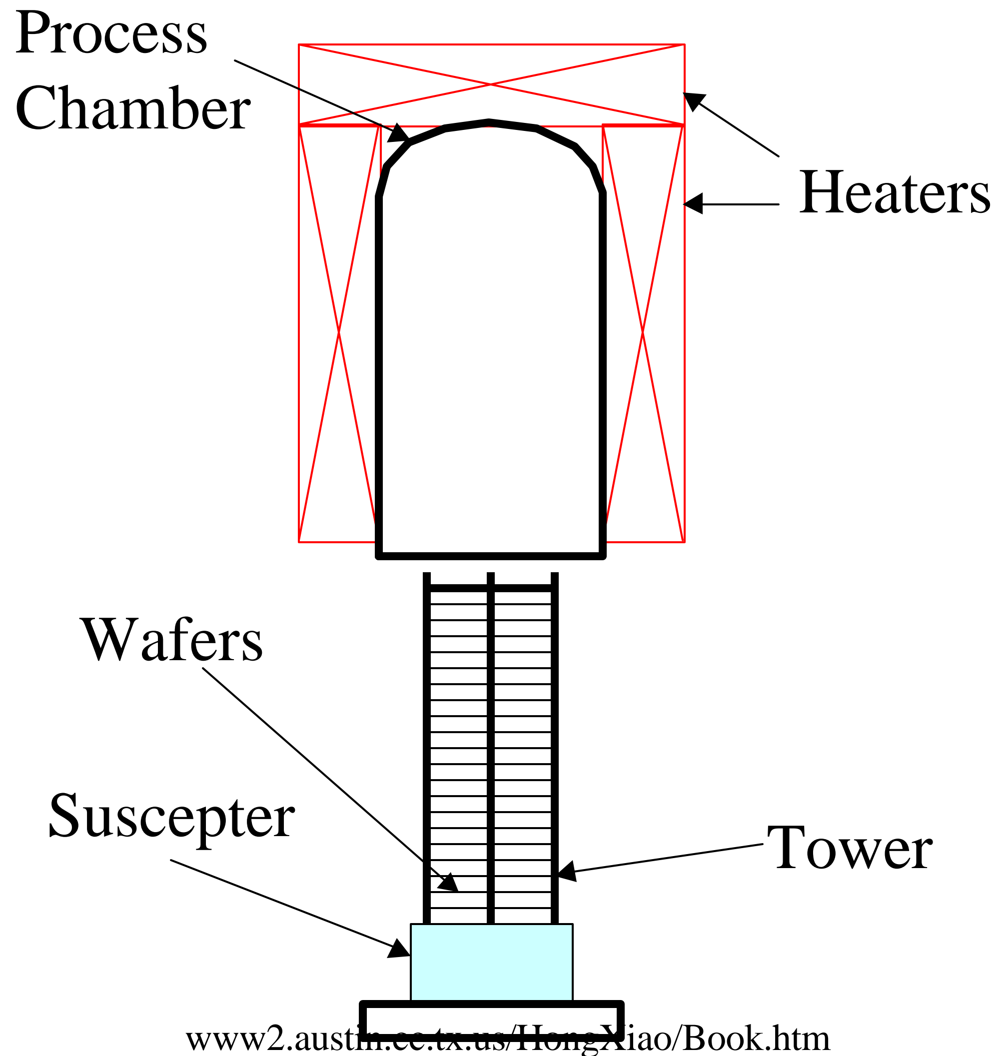
Furnace

- Wafer Clean Station
- Wafer Loading Station
  - Manual wafer loading
  - Automatic wafer loading
- Oxidation Process Automation

Vertical Furnaces

- Place the process tube in vertical direction
- Smaller footprint
- Better contamination control
- Better wafer handling
- Lower maintenance cost and higher uptime

Vertical Furnace, Loading and Unloading Position



Smaller Footprint

- Clean room footage becomes very expensive
- Small footprint reduces cost of ownership (COO)

Better Contamination Control

- Gas flow from top to bottom
- Better uniformity for Laminar gas flow control
- Particles has less chance to fall at the center of the wafers

Better Wafer Handling

- High torque on paddle of horizontal when it handle large amount of large diameter wafers
- Zero torque for wafer tower in vertical system

Summery of Hardware

- Furnaces are commonly used in thermal processes
- Furnaces usually consist with control system, gas delivery system, process tube or chamber, wafer loading system, and exhaust system.
- Vertical furnace is more widely used due to it smaller footprint, better contamination control, and lower maintenance.
- Precise temperature and its uniformity is vital for the success of the thermal processes.

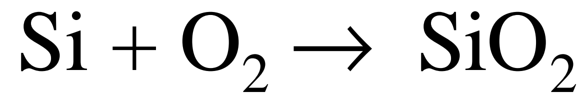
Oxidation

Oxidation

- Introduction
- Applications
- Mechanism
- Process
- System
- RTO

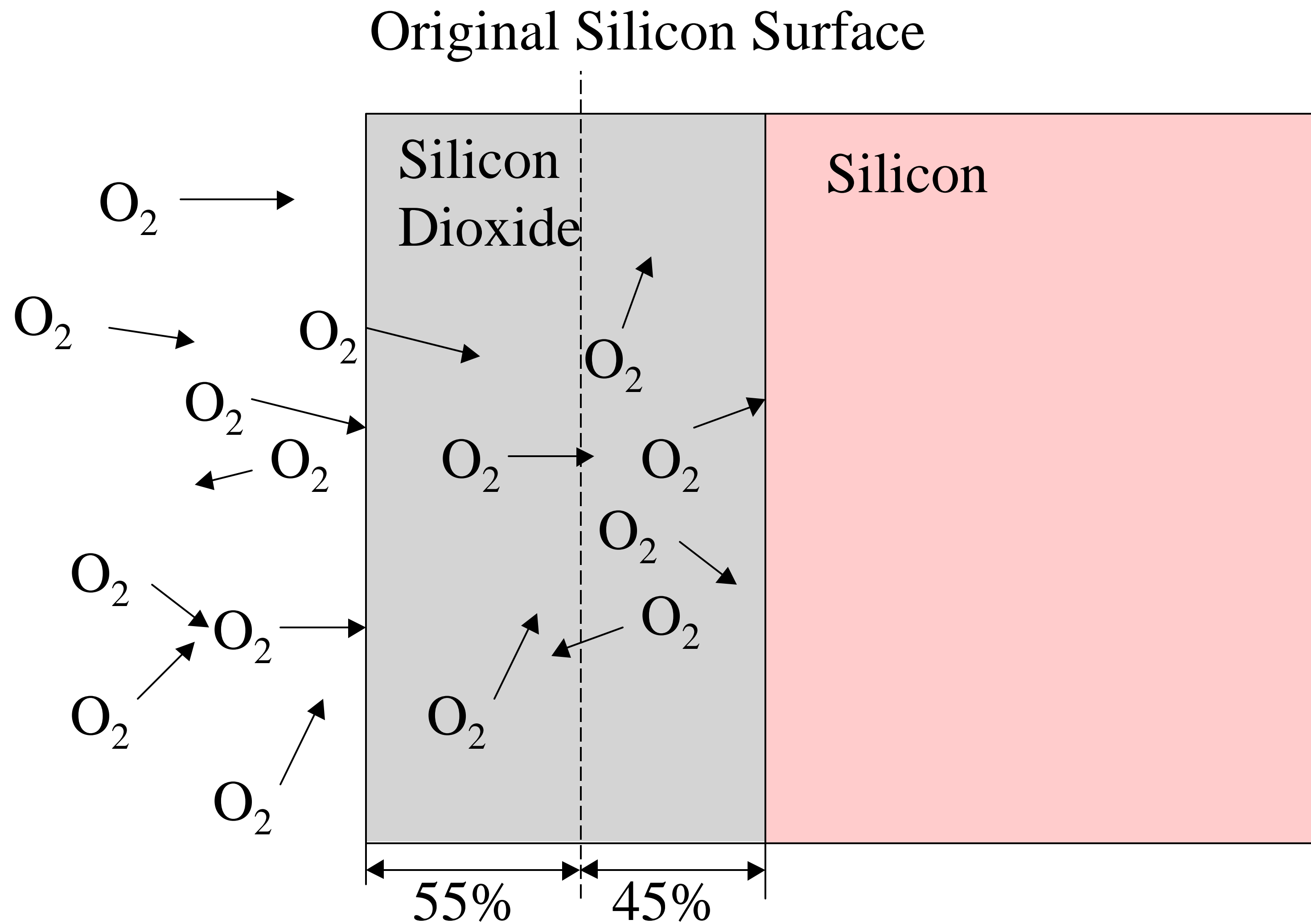
Introduction

- Silicon reacts with oxygen
- Stable oxide compound
- Widely used in IC manufacturing



$$Si + O_2 \rightarrow SiO_2$$

Oxidation



Some Facts About Silicon

Name	Silicon
Symbol	Si
Atomic number	14
Atomic weight	28.0855
Discoverer	Jöns Jacob Berzelius
Discovered at	Sweden
Discovery date	1824
Origin of name	From the Latin word "silicis" meaning "flint"
Bond length in single crystal Si	2.352 Å
Density of solid	2.33 g/cm^3
Molar volume	12.06 cm^3
Velocity of sound	2200 m/sec
Hardness	6.5
Electrical resistivity	100,000 μΩ·cm
Reflectivity	28%
Melting point	1414 °C
Boiling point	2900 °C
Thermal conductivity	150 W m^{-1} K^{-1}
Coefficient of linear thermal expansion	2.6×10^{-6} K^{-1}
Etchants (wet)	HNO_4 and HF, KOH, etc.
Etchants (dry)	HBr, Cl_2, NF_3, etc.
CVD Precursor	SiH_4, SiH_2Cl_2, $SiHCl_3$, and $SiCl_4$

Fact About Oxygen

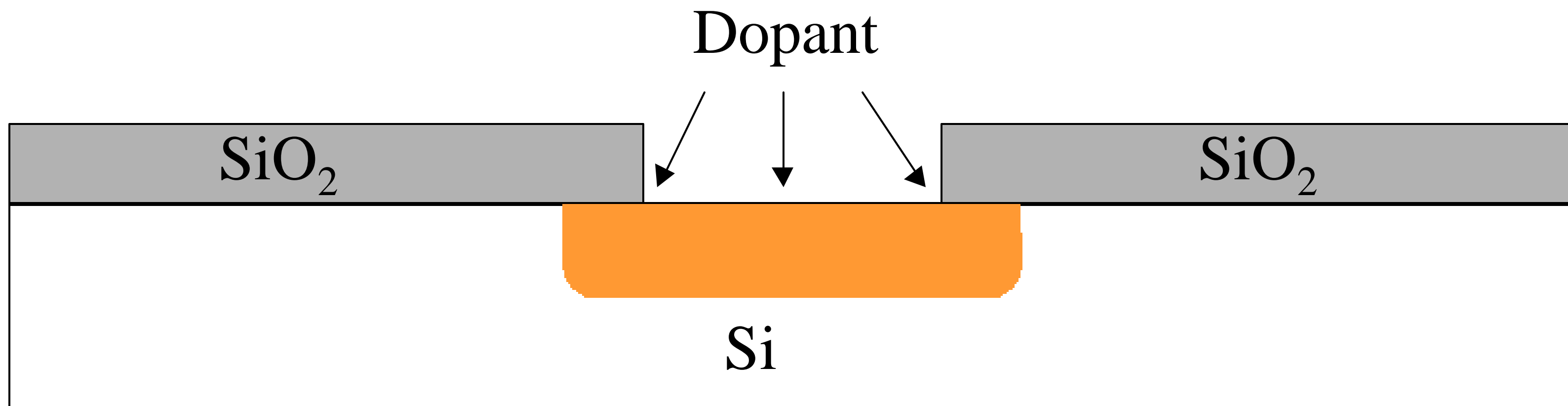
Name	Oxygen
Symbol	O
Atomic number	8
Atomic weight	15.9994
Discoverer	Joseph Priestley, Carl Scheele
Discovered at	England, Sweden
Discovery date	1774
Origin of name	From the Greek words "oxy genes" meaning "acid" (sharp) and "forming" (acid former)
Molar volume	17.36 cm^3
Velocity of sound	317.5 m/sec
Refractivity	1.000271
Melting point	54.8 K = -218.35 °C
Boiling point	90.2 K = -182.95 °C
Thermal conductivity	0.02658 $W\ m^{-1}\ K^{-1}$
Applications	Thermal oxidation, oxide CVD, reactive sputtering and photoresist stripping
Main sources	O_2, H_2O, N_2O, O_3

Application of Oxidation

- Diffusion Masking Layer
- Surface Passivation
  - Screen oxide, pad oxide, barrier oxide
- Isolation
  - Field oxide and LOCOS
- Gate oxide

Diffusion Barrier

- Much lower B and P diffusion rates in SiO_2 than that in Si
- SiO_2 can be used as diffusion mask



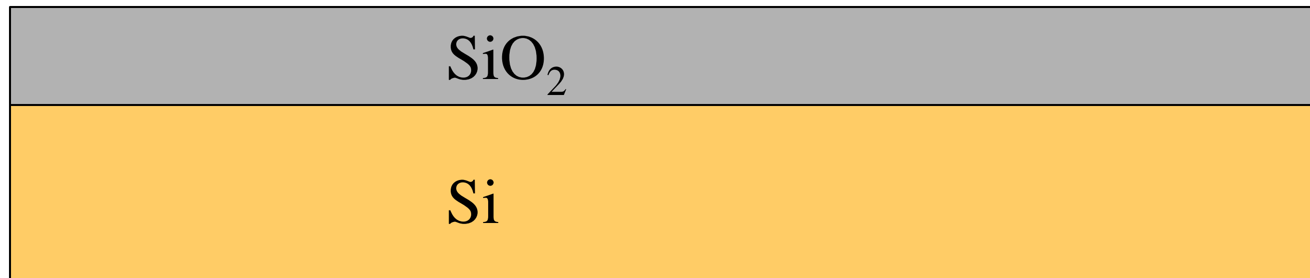
Application, Surface Passivation

Pad Oxide

Screen Oxide

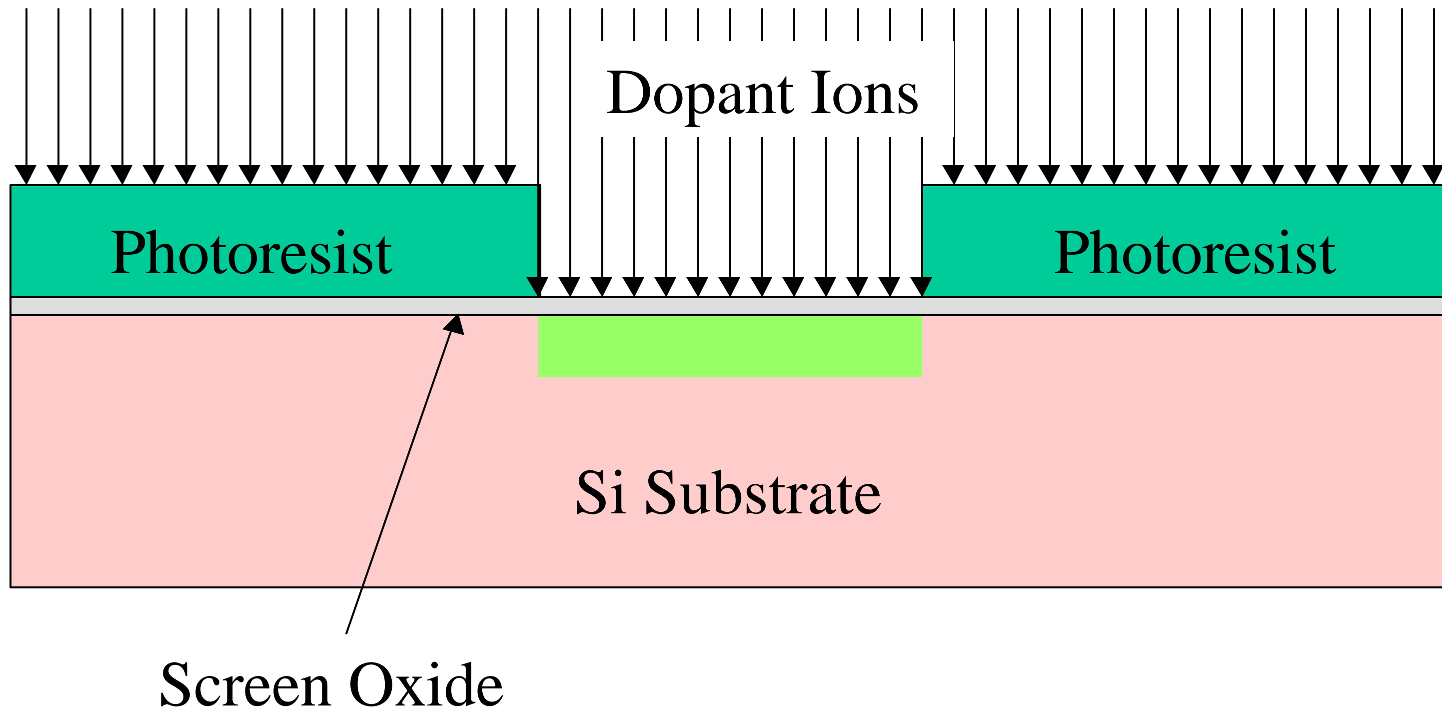
Sacrificial Oxide

Barrier Oxide

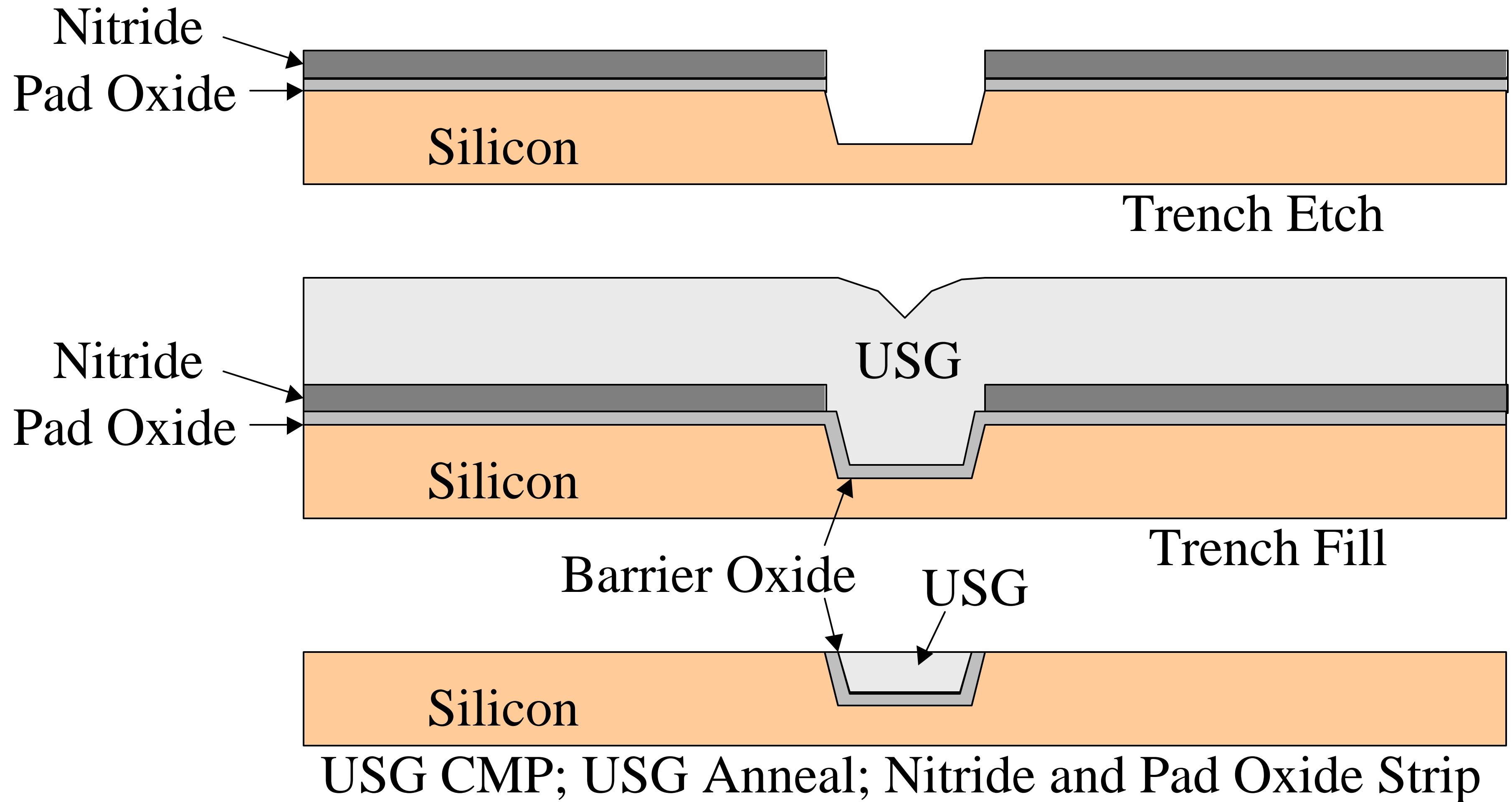


Normally thin oxide layer (~150Å) to protect silicon defects from contamination and over-stress.

Screen Oxide

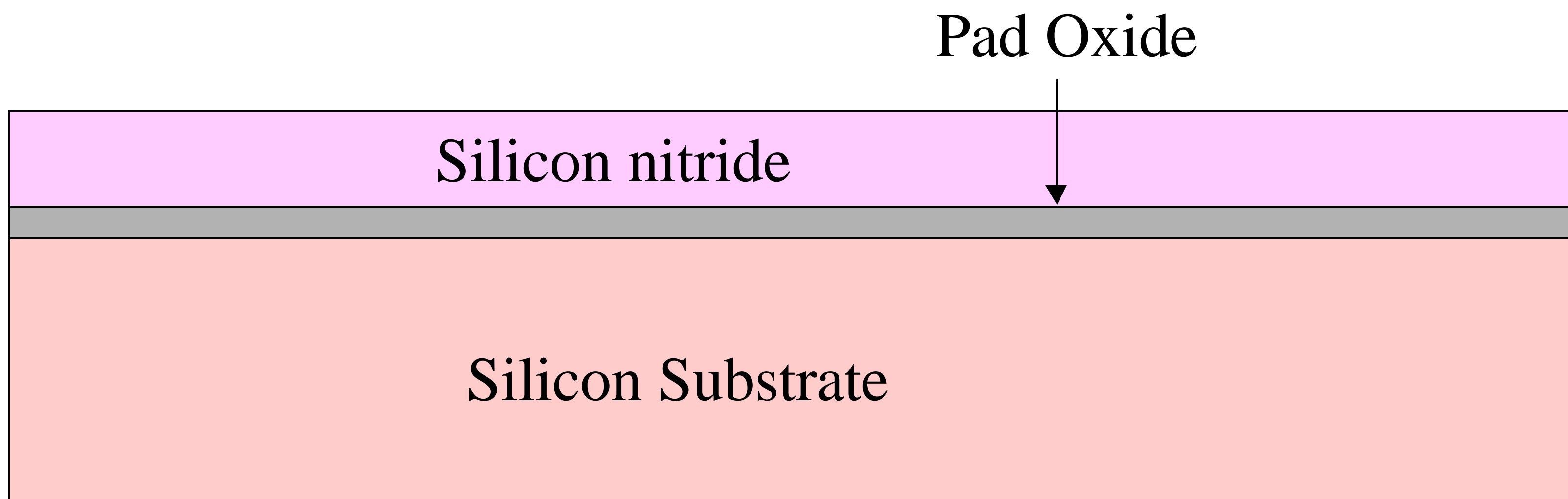


Pad and Barrier Oxides in STI Process



Application, Pad Oxide

- Relieve strong tensile stress of the nitride
- Prevent stress induced silicon defects



Application, Device Isolation

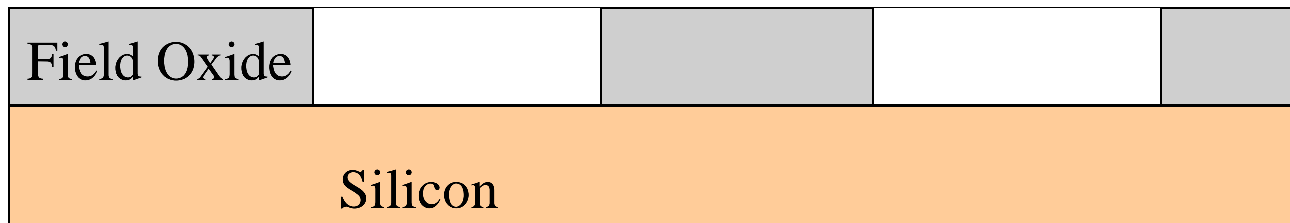
- Electronic isolation of neighboring devices
- Blanket field oxide
- Local oxidation of silicon (LOCOS)
- Thick oxide, usually 3,000 to 10,000 Å

Blanket Field Oxide Isolation

Wafer Clean

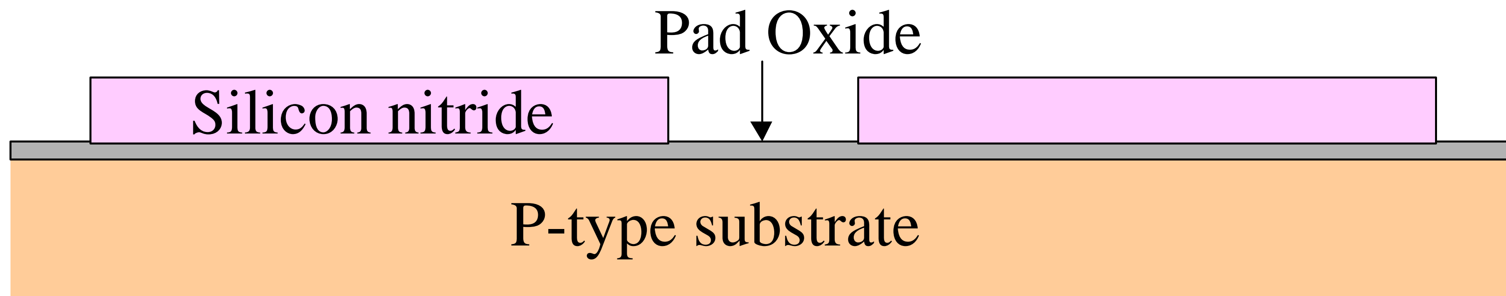
Activation Area

Field Oxidation

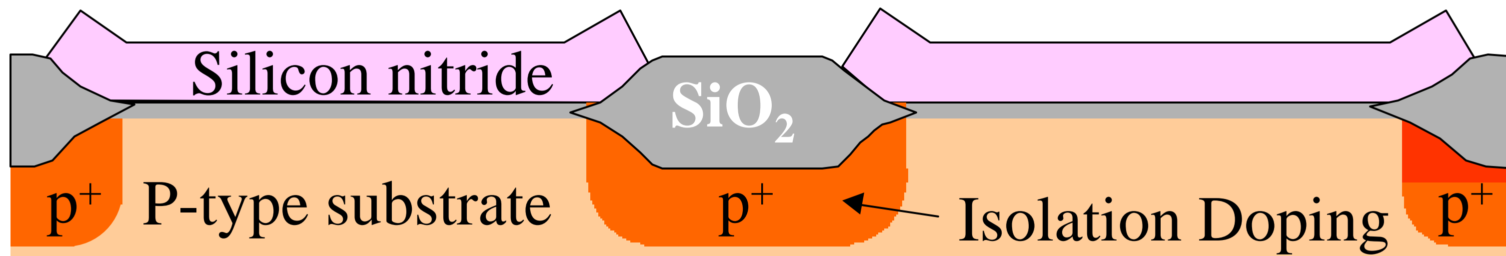


Oxide Etch

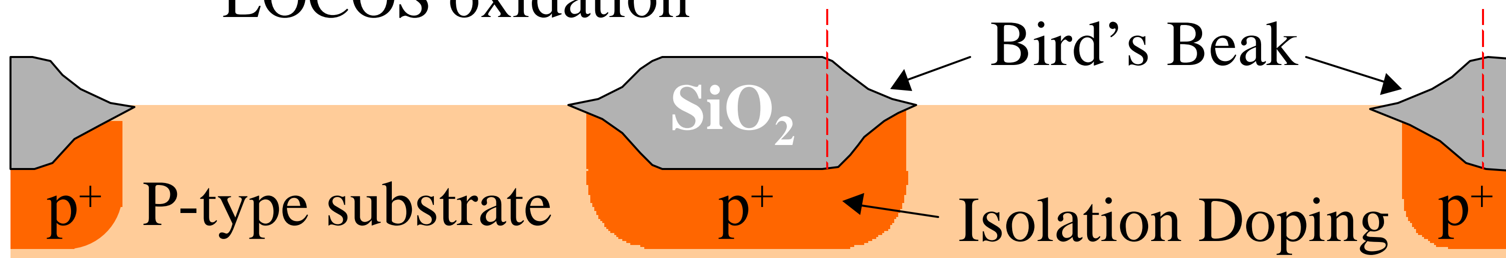
LOCOS Process



Pad oxidation, nitride deposition and patterning



LOCOS oxidation



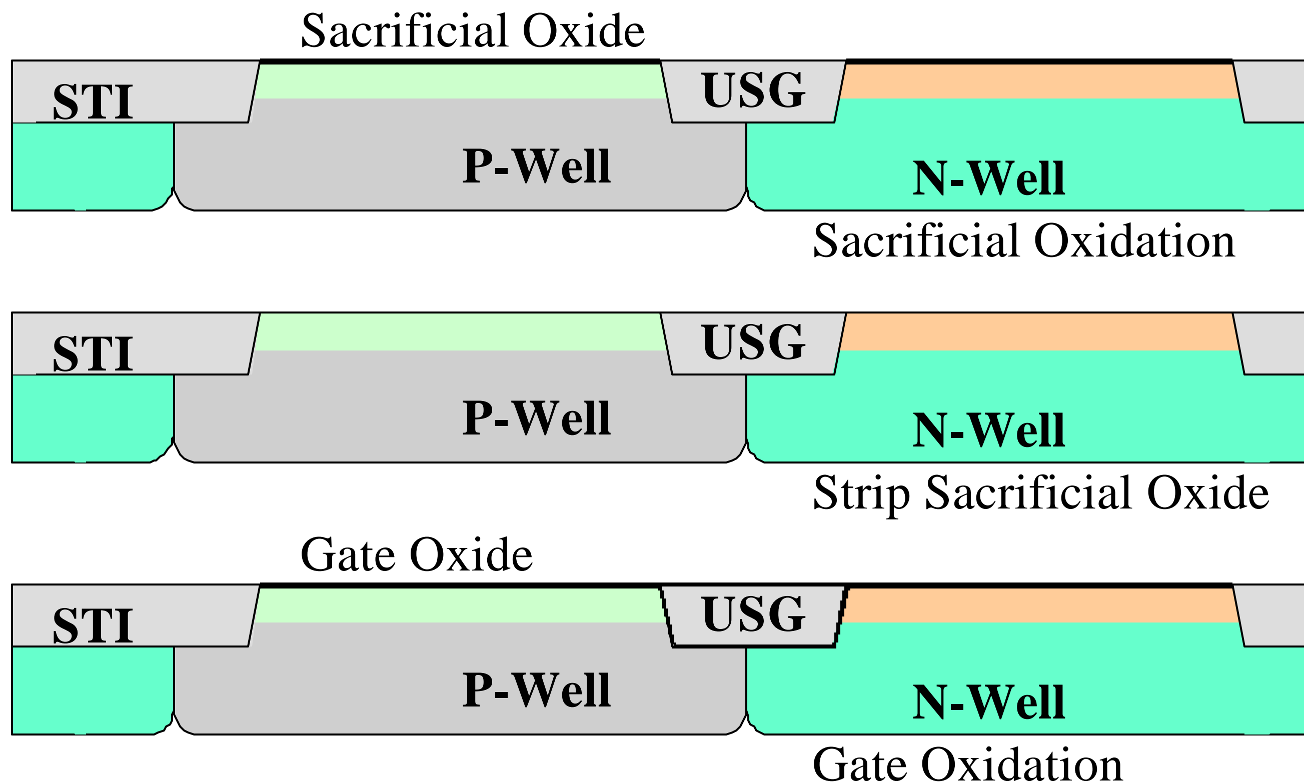
Nitride and pad oxide strip

LOCOS

- Compare with blanket field oxide
  - Better isolation
  - Lower step height
  - Less steep sidewall
- Disadvantage
  - rough surface topography
  - Bird's beak
- Replacing by shallow trench isolation (STI)

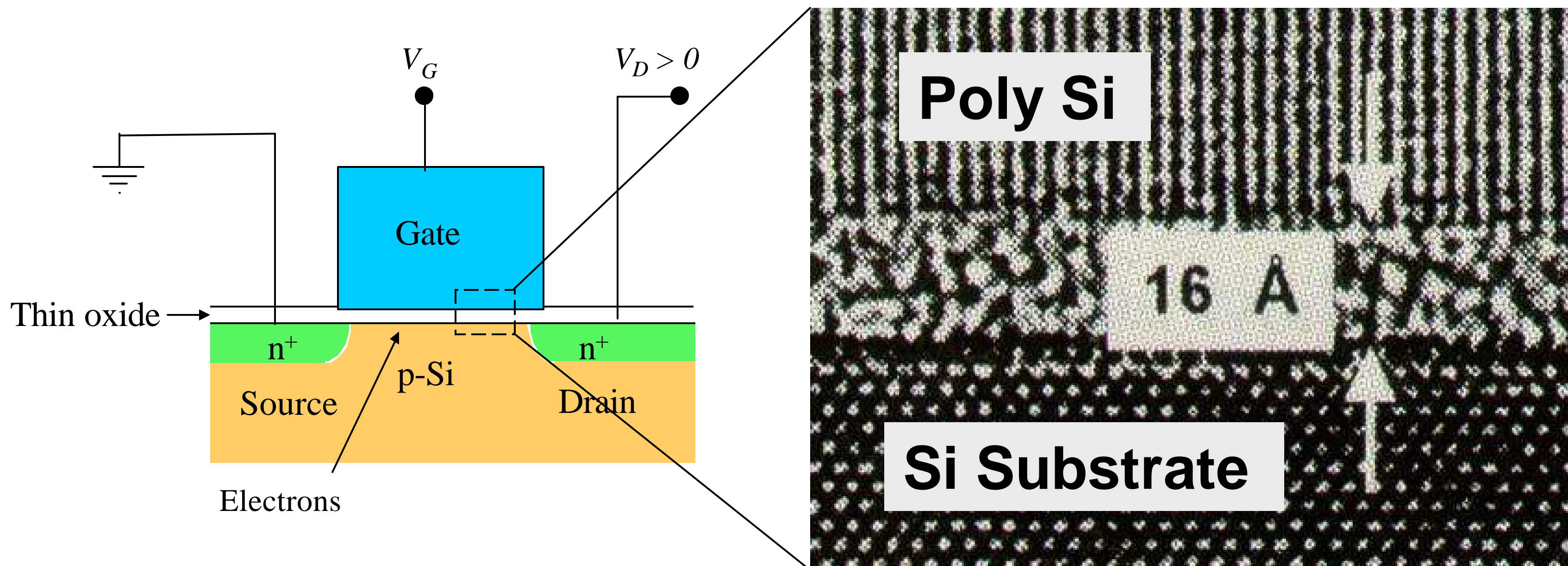
Application, Sacrificial Oxide

- Defects removal from silicon surface



Application, Device Dielectric

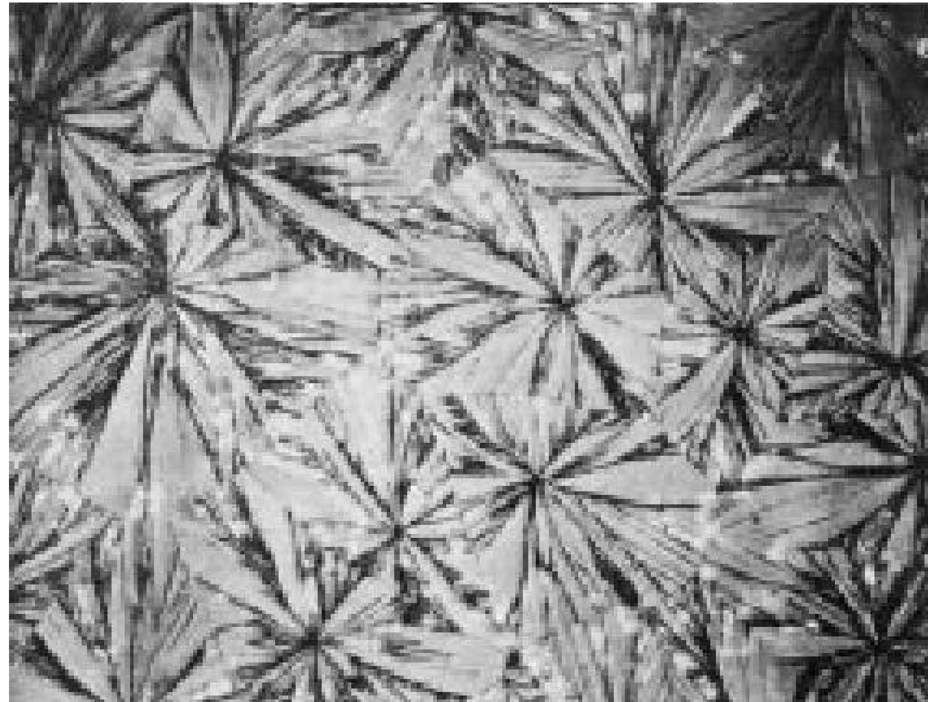
- Gate oxide: thinnest and most critical layer
- Capacitor dielectric



Oxide and Applications

Name of the Oxide	Thickness	Application	Time in application
Native	15 - 20 Å	undesirable	-
Screen	~ 200 Å	Implantation	Mid-70s to present
Masking	~ 5000 Å	Diffusion	1960s to mid-1970s
Field and LOCOS	3000 - 5000 Å	Isolation	1960s to 1990s
Pad	100 - 200 Å	Nitride stress buffer	1960s to present
Sacrificial	<1000 Å	Defect removal	1970s to present
Gate	30 - 120 Å	Gate dielectric	1960s to present
Barrier	100 - 200 Å	STI	1980s to present

Silicon Dioxide Grown on Improperly Cleaned Silicon Surface



Pre-oxidation Wafer Clean

- Particulates
- Organic residues
- Inorganic residues
- Native oxide layers

RCA Clean

- Developed by Kern and Puotinen in 1960 at RCA
- Most commonly used clean processes in IC fabs
- SC-1-- $NH_4OH:H_2O_2:H_2O$ with 1:1:5 to 1:2:7 ratio at 70 to 80 °C to remove organic contaminants.
- SC-2-- $HCl:H_2O_2:H_2O$with 1:1:6 to 1:2:8 ratio at 70 to 80 °C to remove inorganic contaminates.
- DI water rinse
- HF dip or HF vapor etch to remove native oxide.

Pre-oxidation Wafer Clean Particulate Removal

- High purity deionized (DI) water or $H_2SO_4:H_2O_2$ followed by DI H_2O rinse.
- High pressure scrub or immersion in heated dunk tank followed by rinse, spin dry and/or dry bake (100 to 125 °C).

Pre-oxidation Wafer Clean
Organic Removal

- Strong oxidants remove organic residues.
- H_2SO_4:H_2O_2 or NH_3OH:H_2O_2 followed by DI H_2O rinse.
- High pressure scrub or immersion in heated dunk tank followed by rinse, spin dry and/or dry bake (100 to 125 °C).

Pre-oxidation Wafer Clean Inorganic Removal

- HCl:H_2O.
- Immersion in dunk tank followed by rinse, spin dry and/or dry bake (100 to 125 °C).

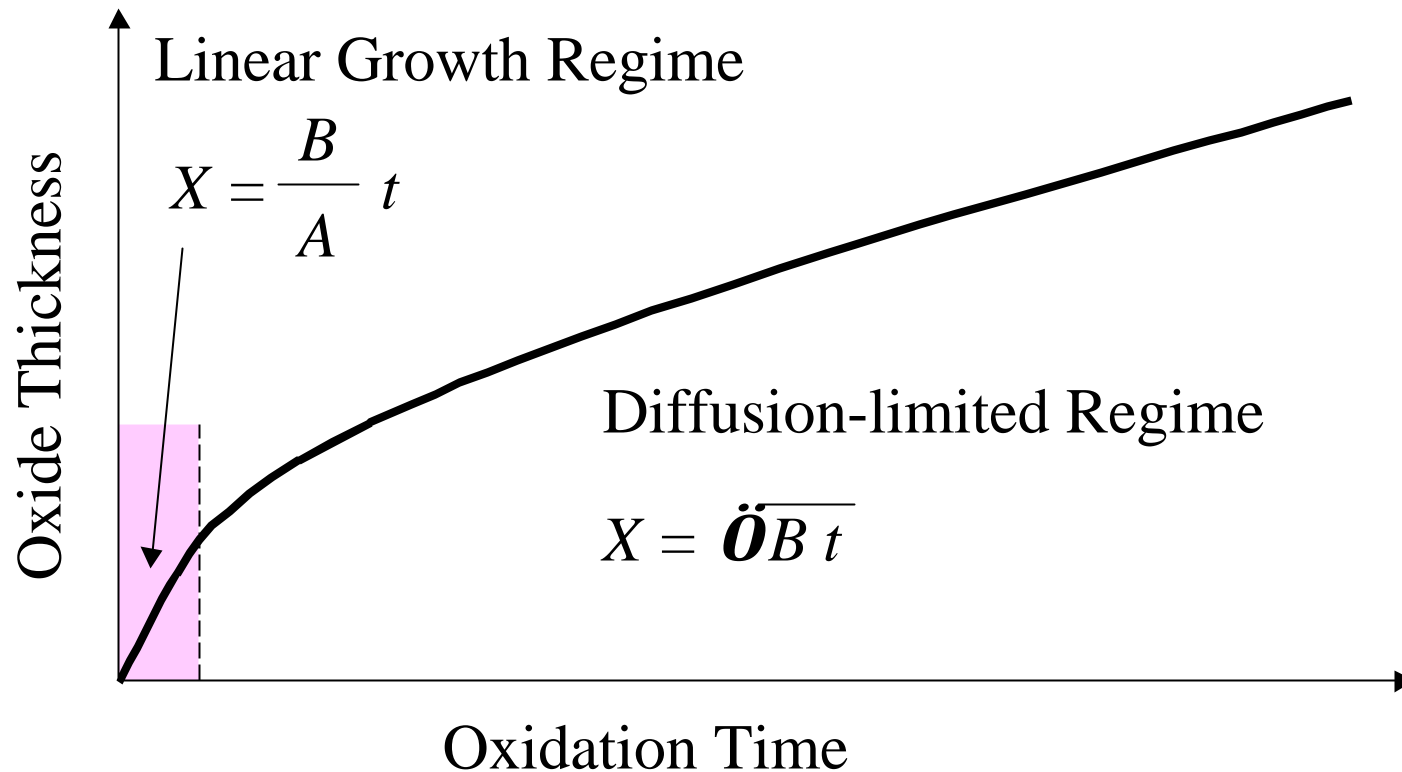
Pre-oxidation Wafer Clean
Native Oxide Removal

- HF:H_2O.
- Immersion in dunk tank or single wafer vapor etcher followed by rinse, spin dry and/or dry bake (100 to 125 °C).

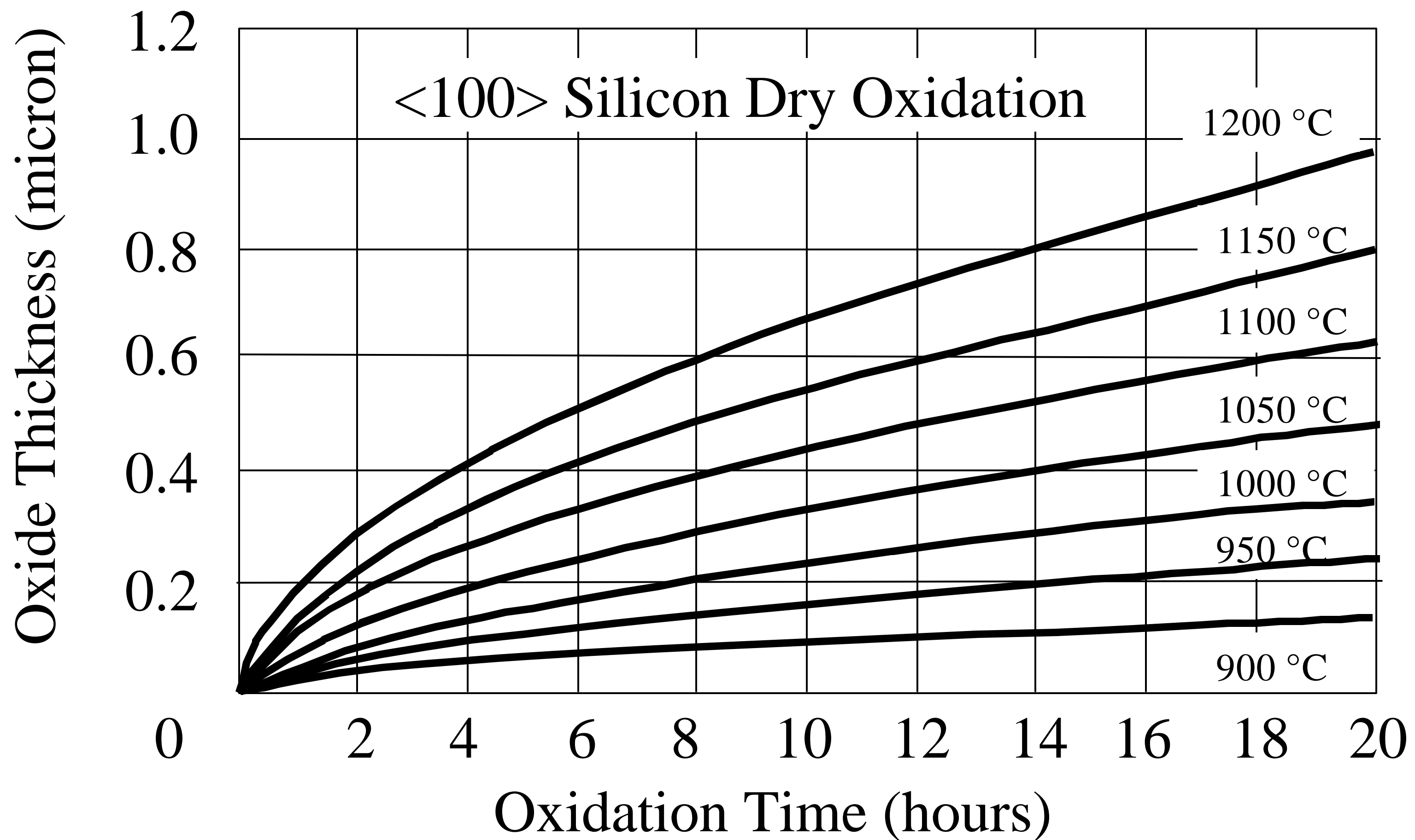
Oxidation Mechanism

- $Si + O_2 \longrightarrow SiO_2$
- Oxygen comes from gas
- Silicon comes from substrate
- Oxygen diffuse cross existing silicon dioxide layer and react with silicon
- The thicker of the film, the lower of the growth rate

Oxide Growth Rate Regime



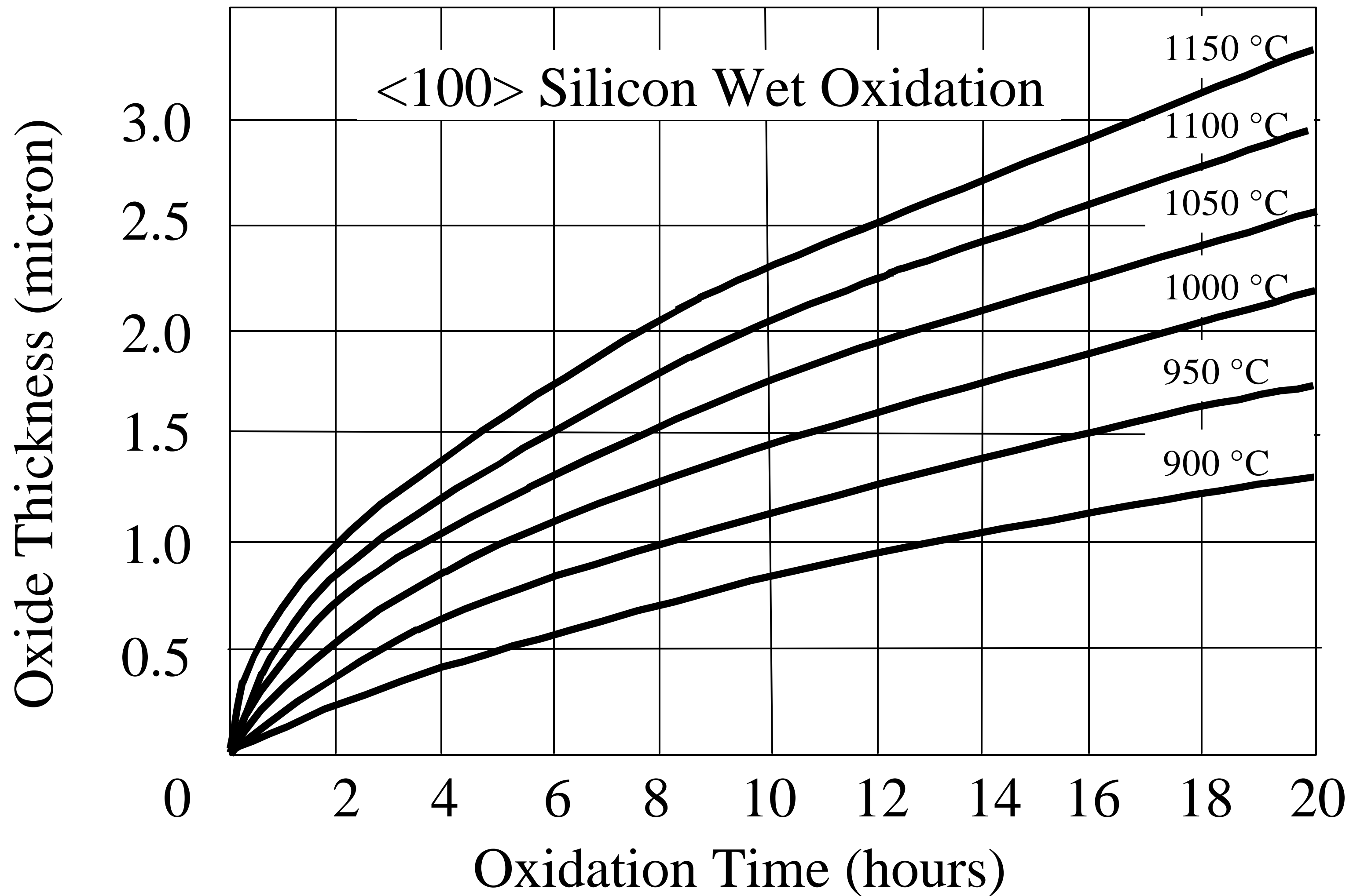
<100> Silicon Dry Oxidation



Wet (Steam) Oxidation

- $Si + 2H_2O \longrightarrow SiO_2 + 2H_2$
- At high temperature H_2O is dissociated to H and H-O
- H-O diffuses faster in SiO_2 than O_2
- Wet oxidation has higher growth rate than dry oxidation.

<100> Silicon Wet Oxidation Rate



Oxidation Rate

- Temperature
- Chemistry, wet or dry oxidation
- Thickness
- Pressure
- Wafer orientation (<100> vs. <111>)
- Silicon dopant

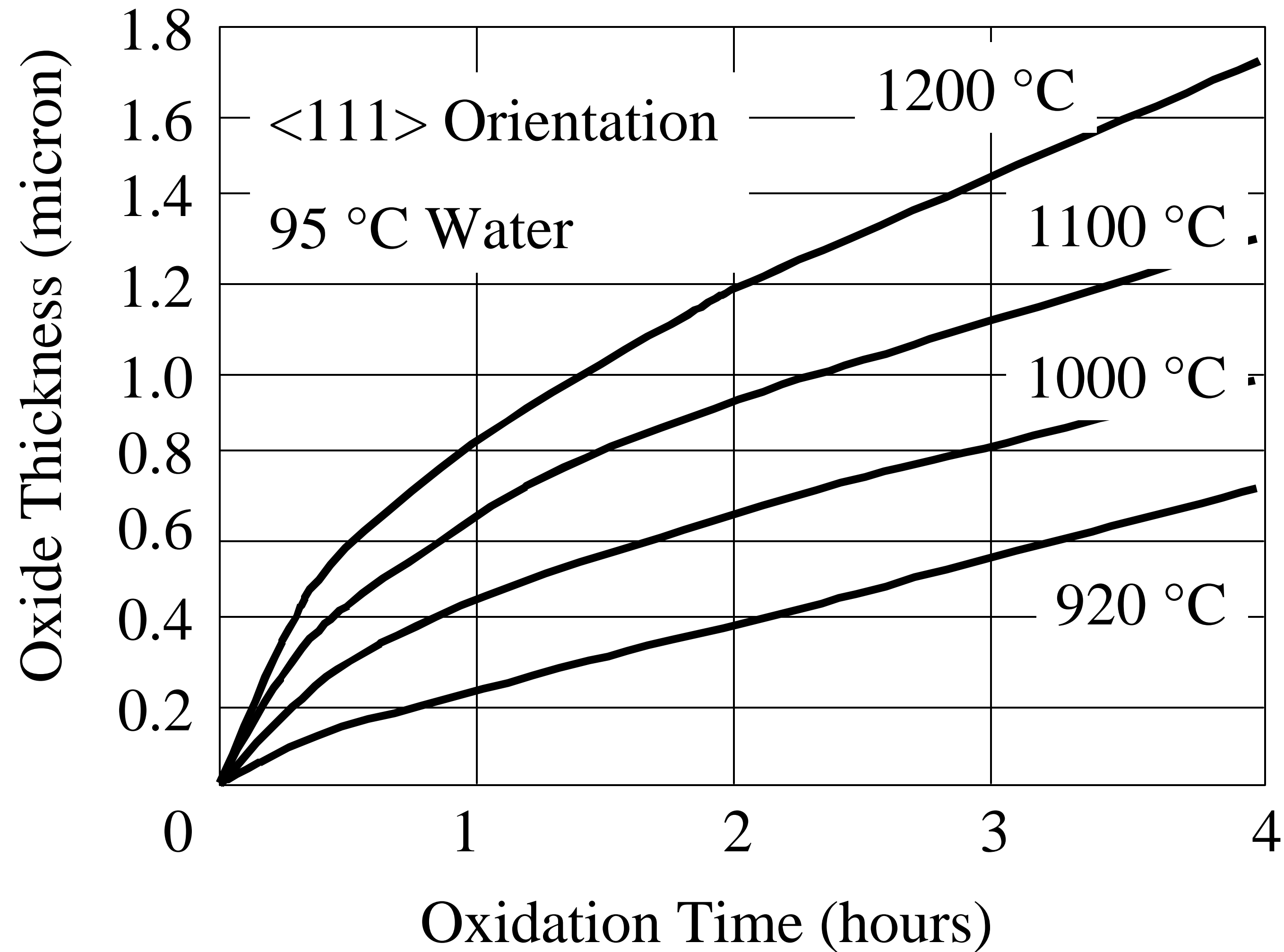
Oxidation Rate Temperature

- Oxidation rate is very sensitive (exponentially related) to temperature
- Higher temperature will have much higher oxidation rate.
- The higher of temperature is, the higher of the chemical reaction rate between oxygen and silicon is and the higher diffusion rate of oxygen in silicon dioxide is.

Oxidation Rate Wafer Orientation

- <111> surface has higher oxidation rate than <100> surface.
- More silicon atoms on the surface.

Wet Oxidation Rate



Oxidation Rate
Dopant Concentration

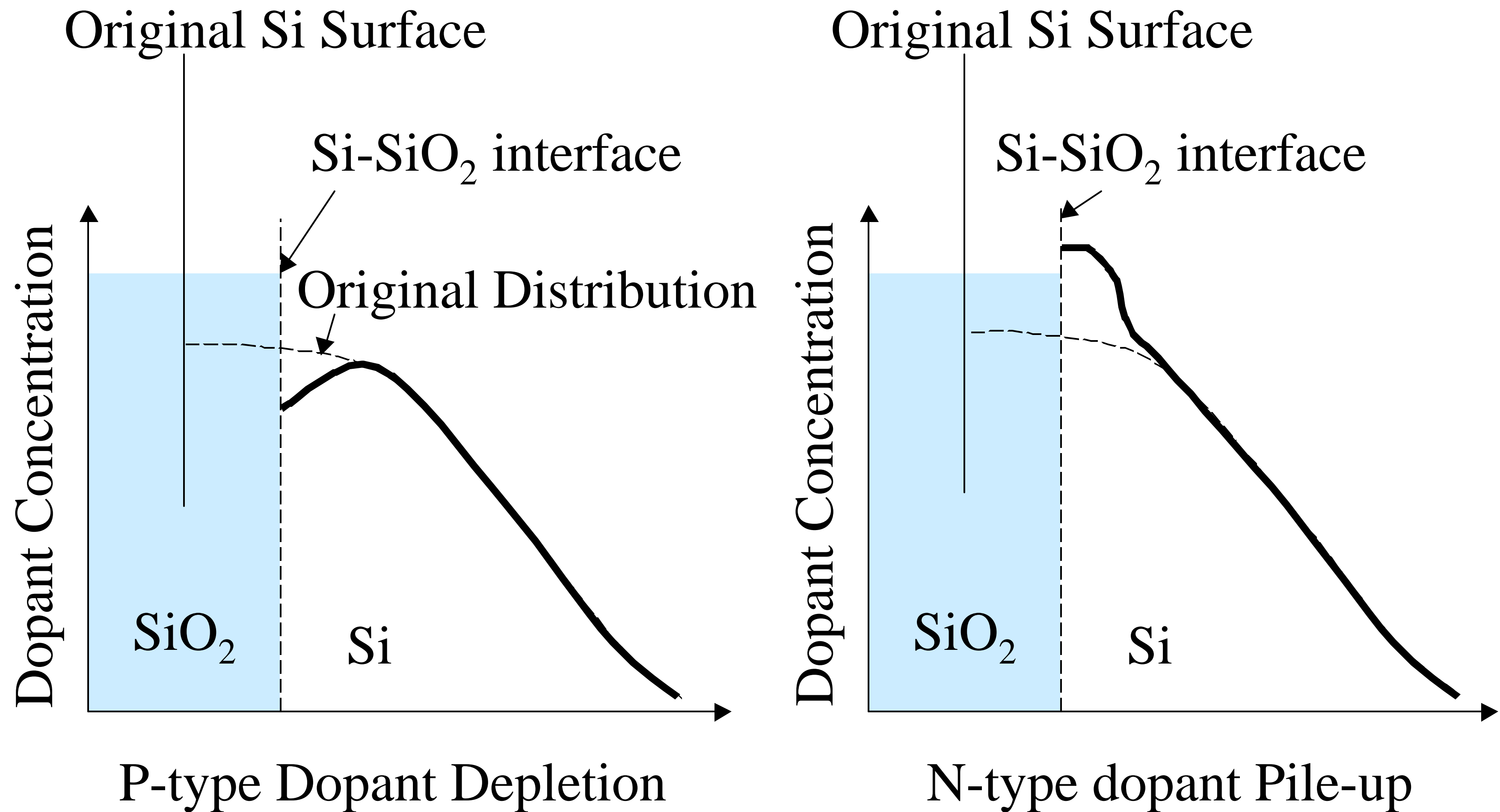
- Dopant elements and concentration
- Highly phosphorus doped silicon has higher growth rate, less dense film and etch faster.
- Generally highly doped region has higher grow rate than lightly doped region.
- More pronounced in the linear stage (thin oxides) of oxidation.

Oxidation: Dopants Pile-up and Depletion Effects

- N-type dopants (P, As, Sb) have higher solubility in Si than in SiO_2, when SiO_2 grow they move into silicon, it is call pile-up or snowplow effect.

- Boron tends to go to SiO_2, it is called depletion effect.

Depletion and Pile-up Effects



Oxidation Rate
Doped oxidation (HCl)

- HCl is used to reduce mobile ion contamination.
- Widely used for gate oxidation process.
- Growth rate can increase from 1 to 5 percent.

Oxidation Rate
Differential Oxidation

- The thicker of the oxide film is, the slower of the oxidation rate is.
- Oxygen need more time to diffuse cross the existing oxide layer to react with substrate silicon.

Pre-oxidation Clean

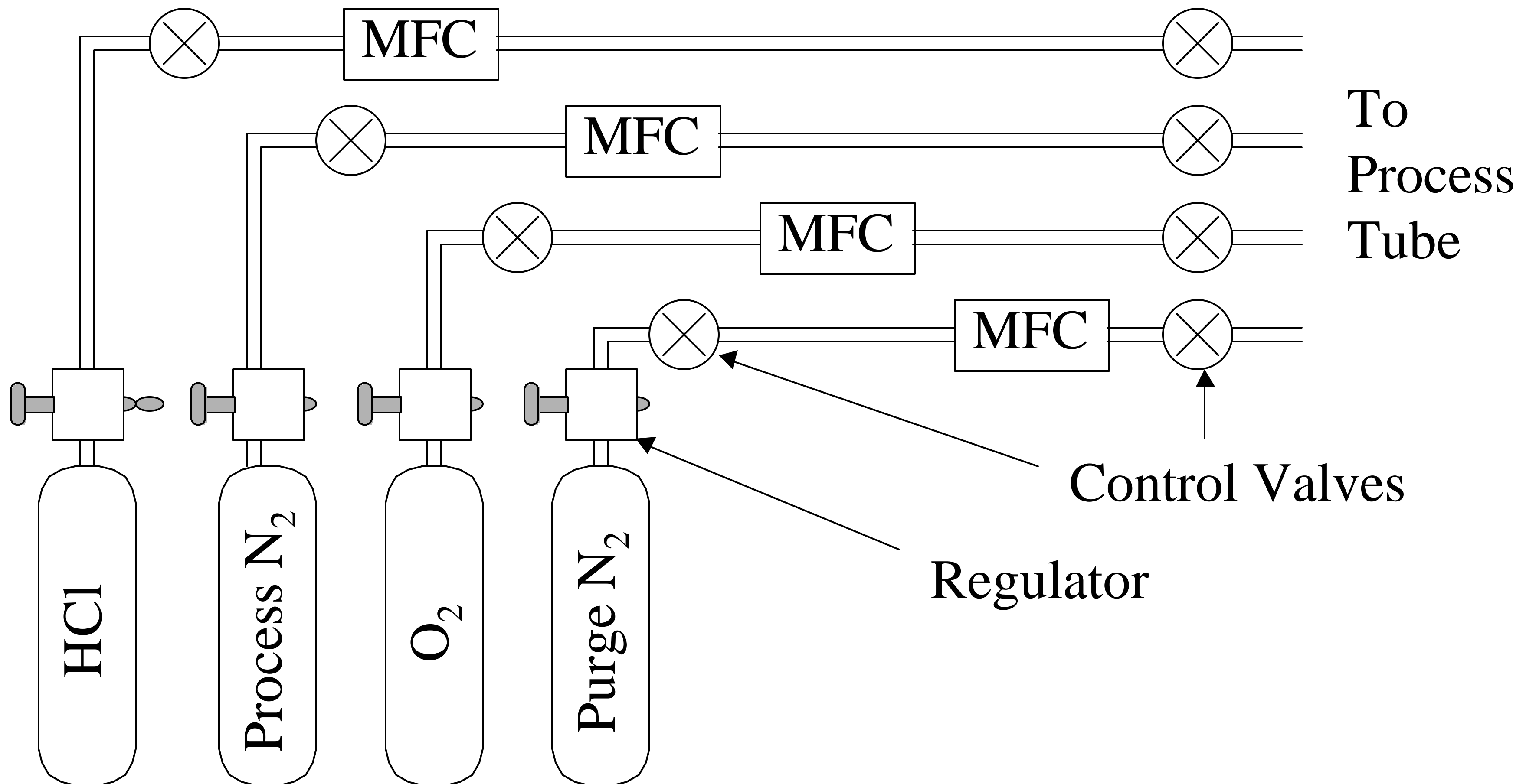
- Thermally grown SiO_2 is amorphous.
- Tends to cross-link to form a crystal
- In nature, SiO_2 exists as quartz and sand
- Defects and particles can be the nucleation sites
- Crystallized SiO_2 with poor barrier capability.

- Need clean silicon surface before oxidation.

Oxidation Process

- Dry Oxidation, thin oxide
  - Gate oxide
  - Pad oxide, screen oxide, sacrificial oxide, etc.
- Wet Oxidation, thick oxide
  - Field oxide
  - Diffusion masking oxide

Dry Oxidation System



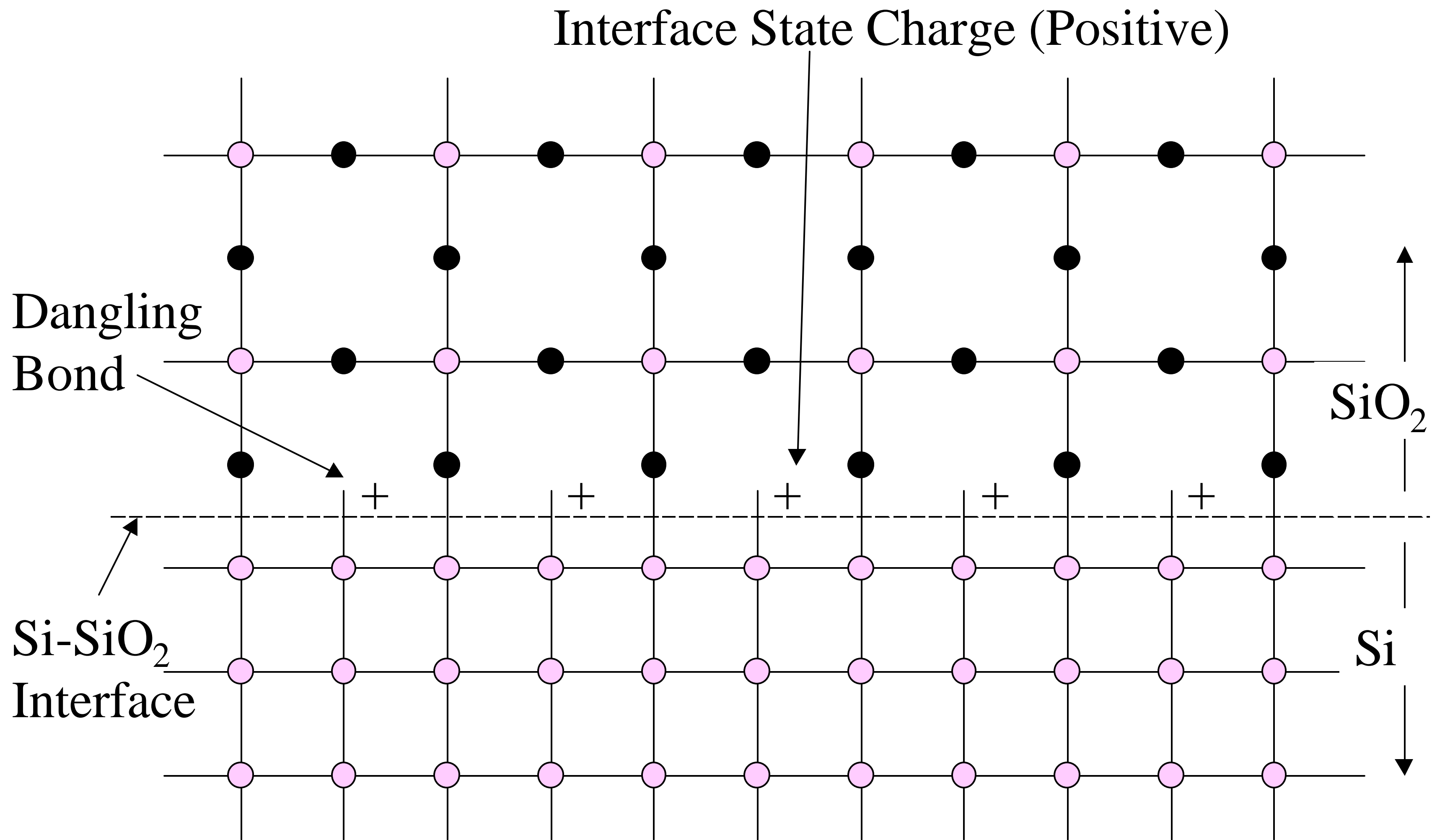
Dry Oxidation

- Dry O_2 as the main process gas
- HCl is used to remove mobile ions for gate oxidation
- High purity N_2 as process purge gas
- Lower grade N_2 as idle purge gas

Gate Oxidation Steps

- Idle with purge N_2 flow
- Idle with process N_2 flow
- Wafer boats push-in with process N_2 flow
- Temperature ramp-up with process N_2 flow
- Temperature stabilization with process N_2 flow
- Oxidation with O_2, HCl, stop N_2 flow

Dangling Bonds and Interface Charge



Gate Oxidation Steps, Continue

- Oxide annealing, stop O_2, start process flow N_2
- Temperature cool-down with process N_2 flow
- Wafer boats pull-out with process N_2 flow
- Idle with process N_2 flow
- Next boats and repeat process
- Idle with purge N_2 flow

Wet Oxidation Process

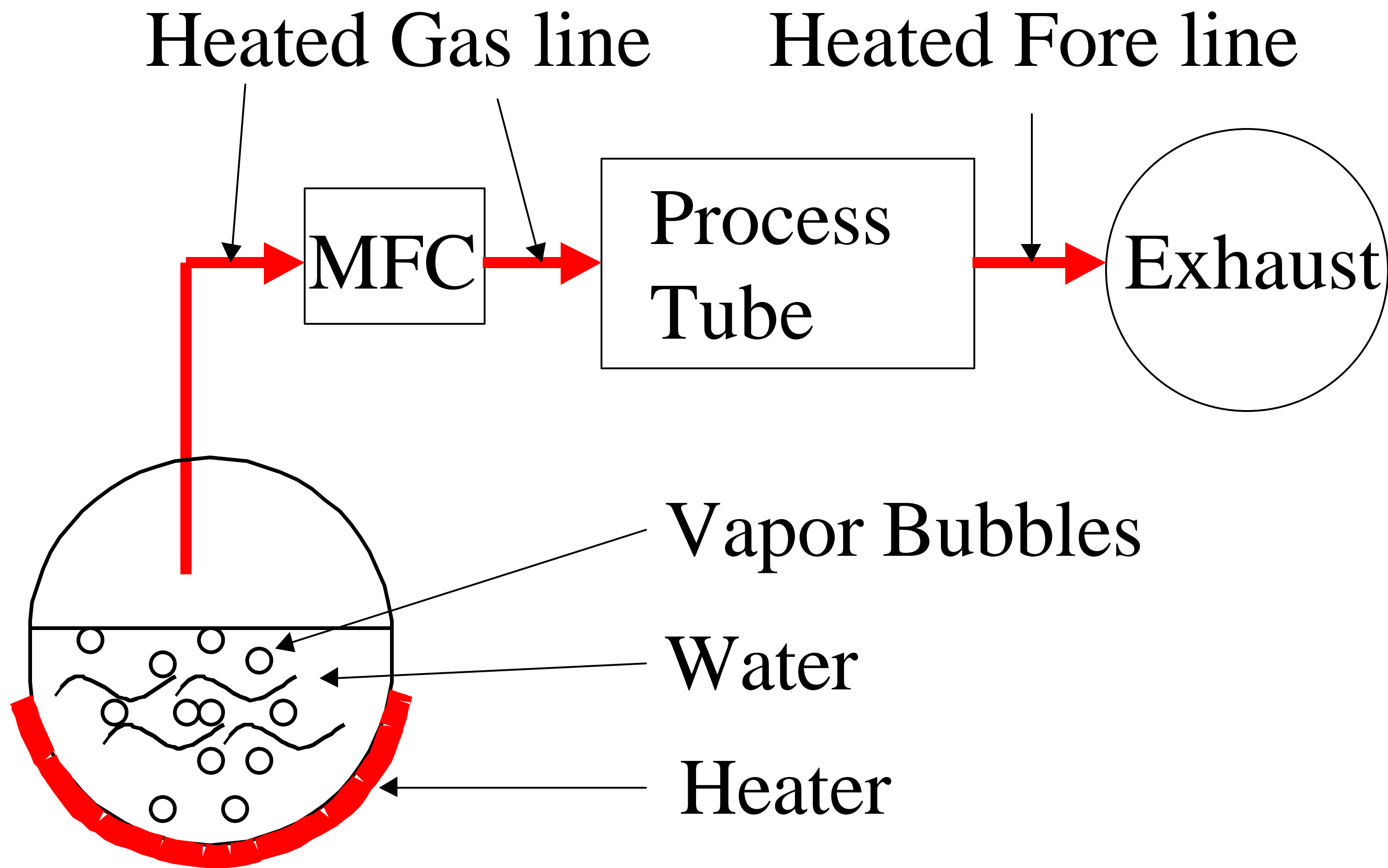
- Faster, higher throughput
- Thick oxide, such as LOCOS
- Dry oxide has better quality

Process	Temperature	Film Thickness	Oxidation Time
Dry oxidation	1000 °C	1000 Å	~ 2 hours
Wet oxidation	1000 °C	1000 Å	~ 12 minutes

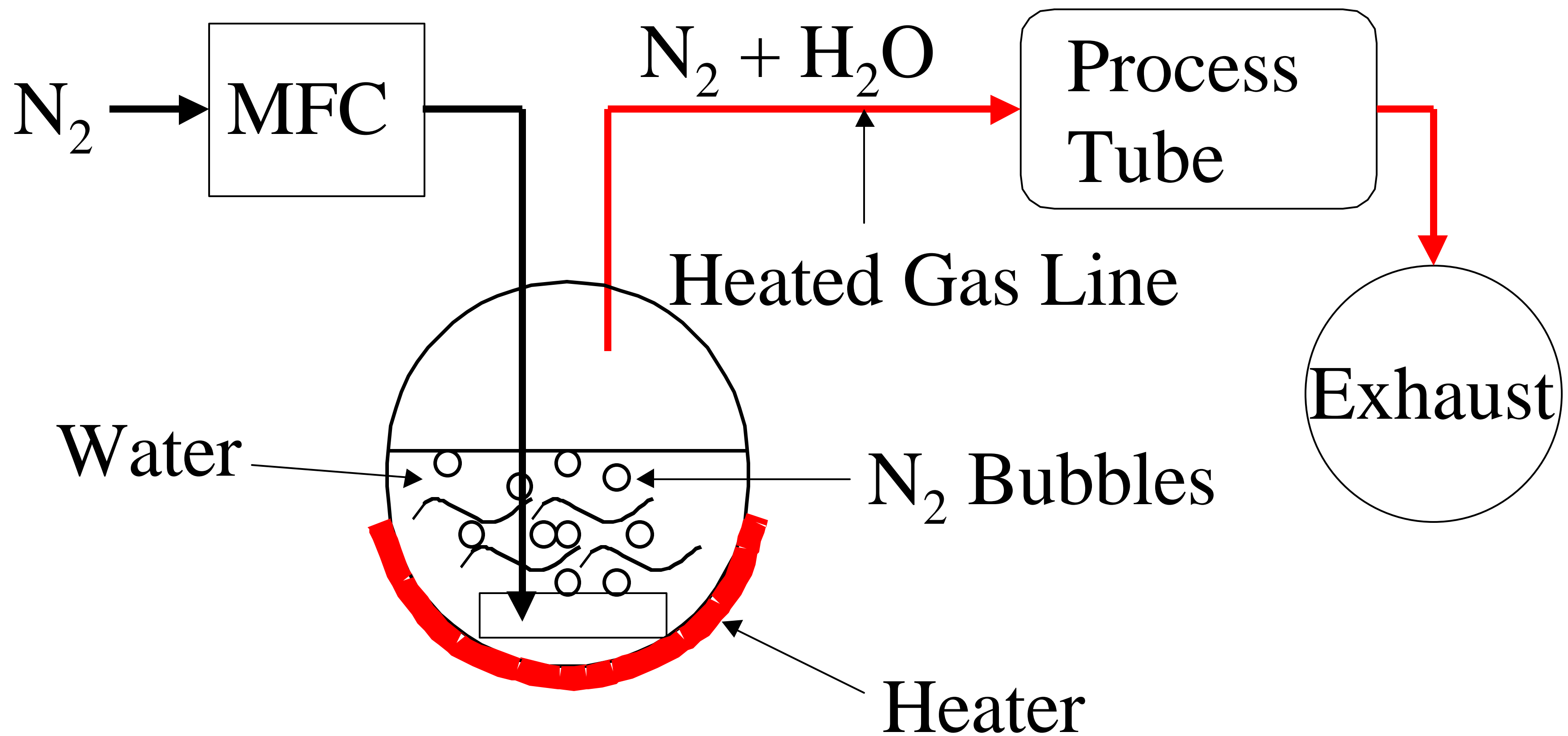
Water Vapor Sources

- Boiler
- Bubbler
- Flush
- Pyrogenic

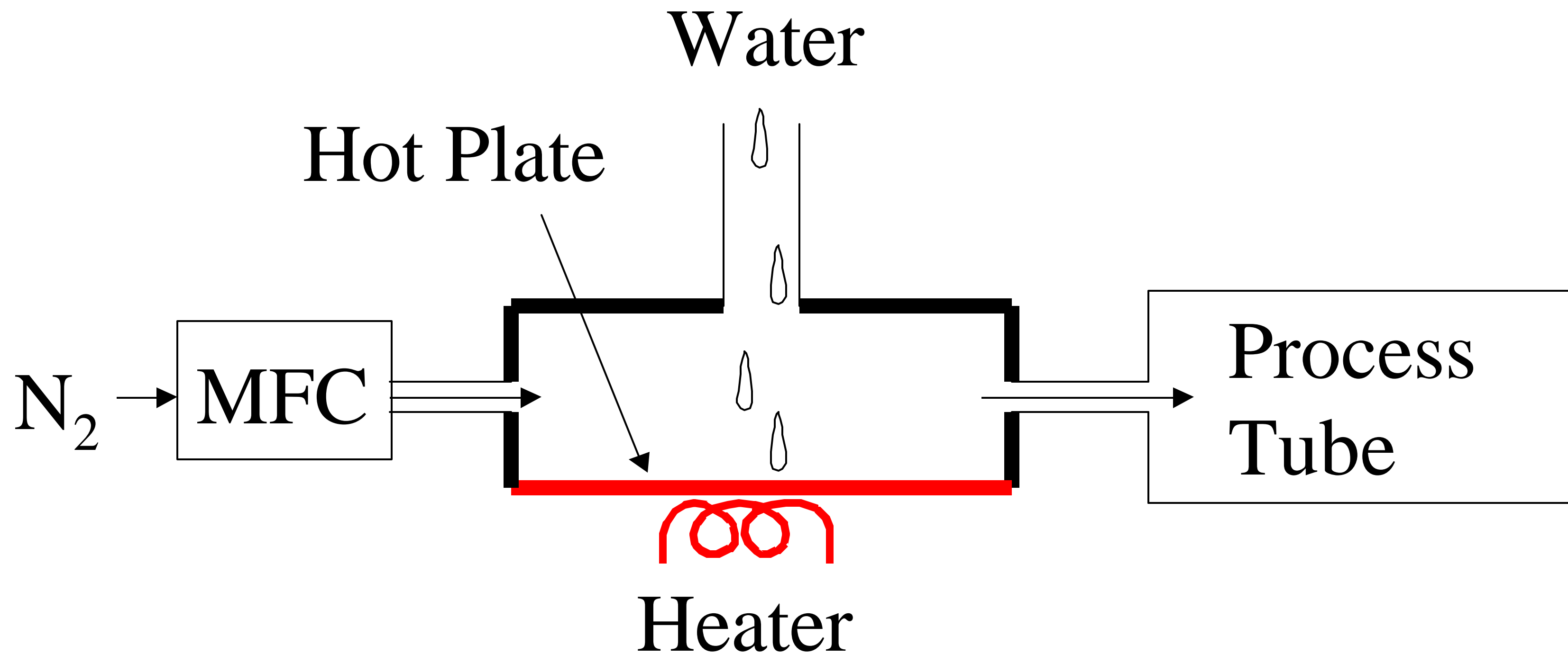
Boiler System



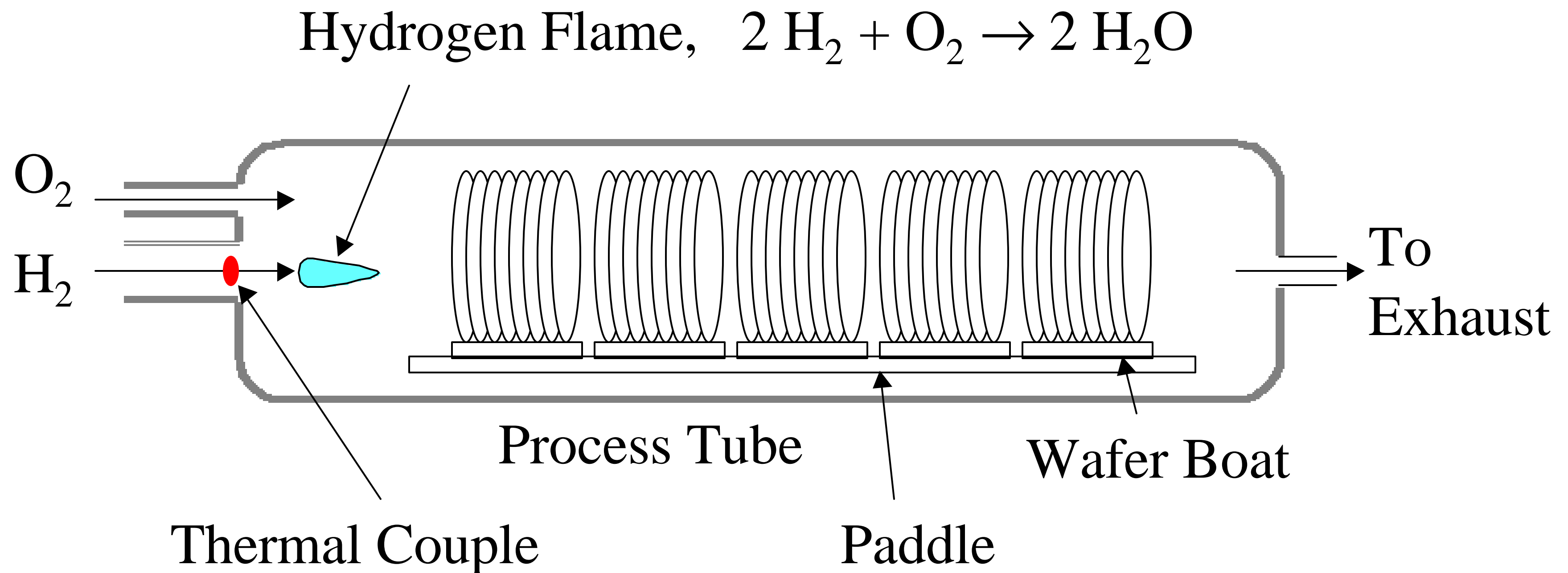
Bubbler System



Flush System



Pyrogenic Steam System

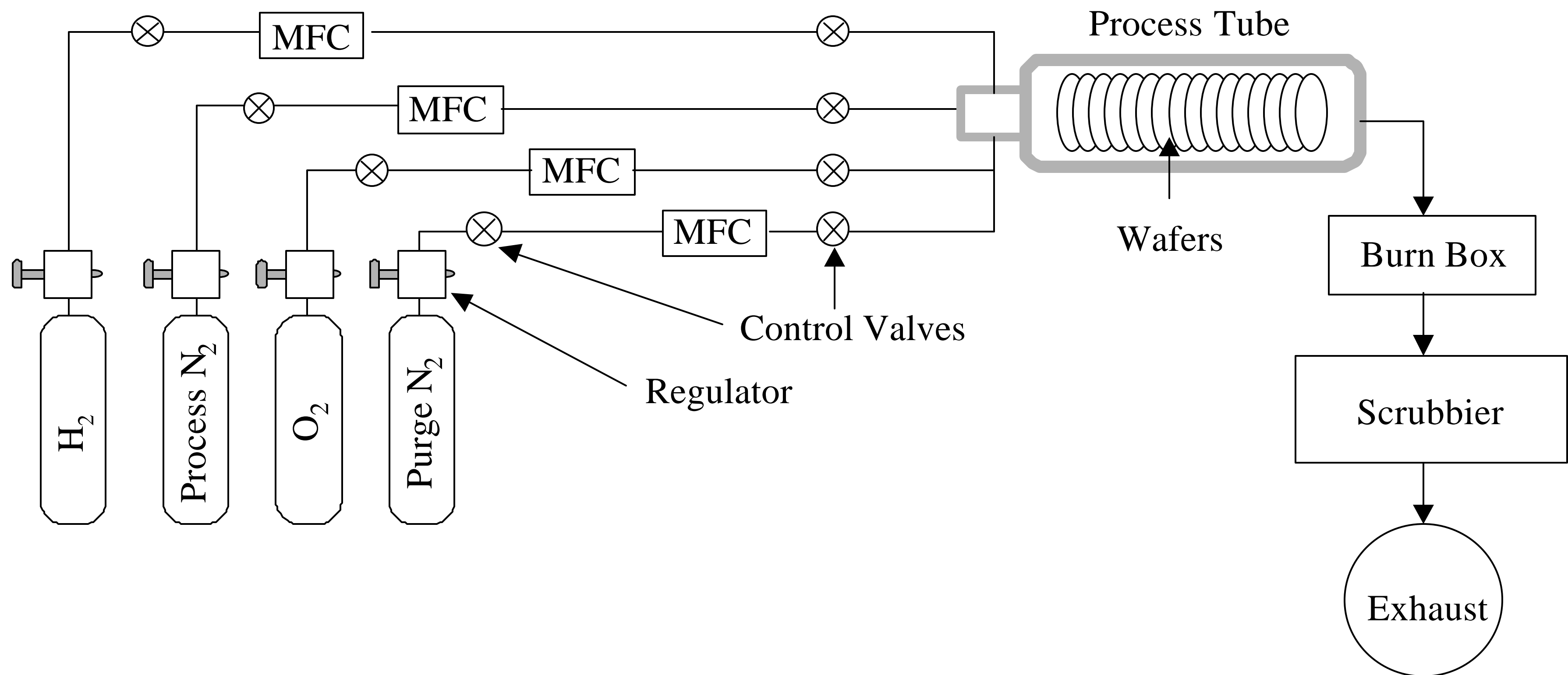


Pyrogenic System

- Advantage
  - All gas system
  - Precisely control of flow rate
- Disadvantage
  - Introducing of flammable, explosive hydrogen

- Typical $H_2:O_2$ ratio is between 1.8:1 to 1.9:1.

Pyrogenic Wet Oxidation System



Wet Oxidation Process Steps

- Idle with purge N_2 flow
- Idle with process N_2 flow
- Ramp O_2 with process N_2 flow
- Wafer boat push-in with process N_2 and O_2 flows
- Temperature ramp-up with process N_2 and O_2 flows
- Temperature stabilization with process N_2 and O_2 flows
- Ramp O_2, turn-off N_2 flow
- Stabilize the O_2 flow

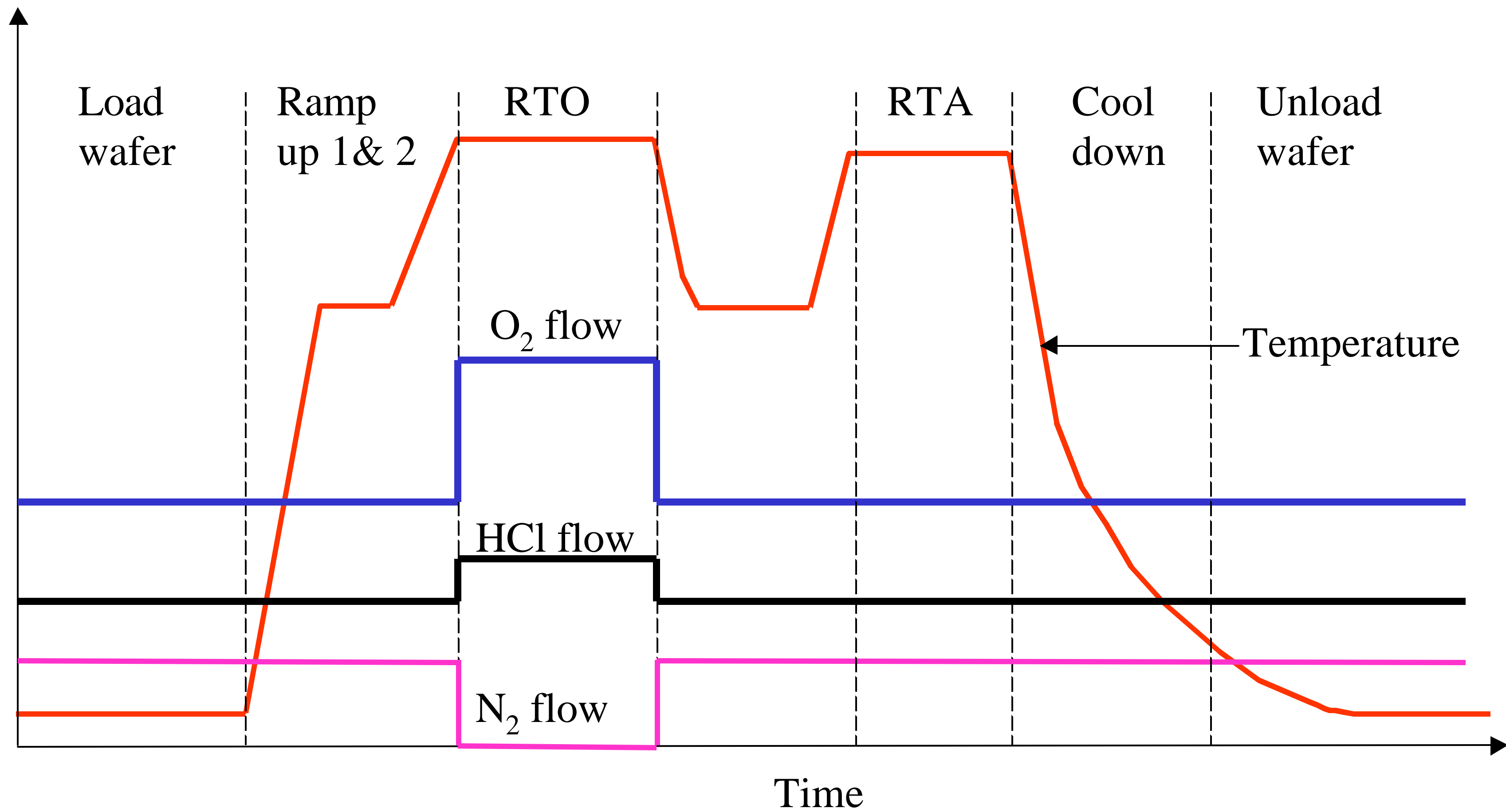
Wet Oxidation Process Steps

- Turn-on H_2 flow, ignition and H_2 flow stabilization
- Steam oxidation with O_2 and H_2 flow
- Hydrogen termination, turn-off H_2 while keeping O_2 flow
- Oxygen termination, turn-off O_2 start process N_2 flow
- Temperature ramp-down with process N_2 flow
- Wafer boat pull-out with process N_2 flow
- Idle with process N_2 flow
- Next boats and repeat process
- Idle with purge N_2 flow

Rapid Thermal Oxidation

- For gate oxidation of deep sub-micron device
- Very thin oxide film, < 30 Å
- Need very good control of temperature uniformity, WIW and WTW.
- RTO will be used to achieve the device requirement.

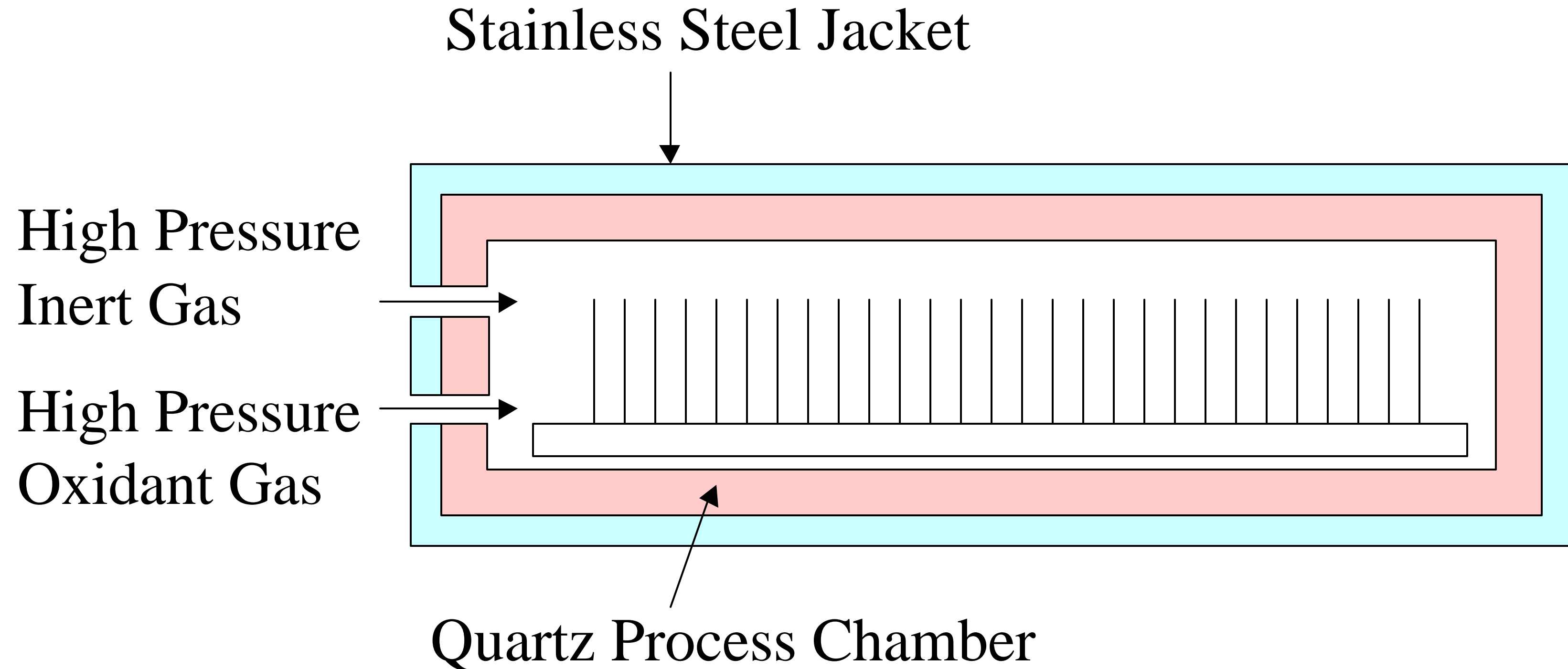
RTP Process Diagram



High Pressure Oxidation

- Faster growth rate
- Reducing oxidation temperature:
  - 1 amt. = –30 °C
- Higher dielectric strength

High Pressure Oxidation



High Pressure Oxidation

Oxidation time to grow 10,000 Å wet oxide

Temperature	Pressure	Time
1000 °C	1 atmosphere	5 hours
	5 atmosphere	1 hour
	25 atmosphere	12 minutes

High Pressure Oxidation

Oxidation temperature to grow 10,000 Å wet oxide in 5 hours

<table>
<tr><th>Time</th><th>Pressure</th><th>Temperature</th></tr>
<tr><td rowspan="2">5 hours</td><td>1 atmosphere</td><td>1000 °C</td></tr>
<tr><td>10 atmosphere</td><td>700 °C</td></tr>
</table>

High Pressure Oxidation

- Complex system
- Safety issues

- Not widely used in IC production

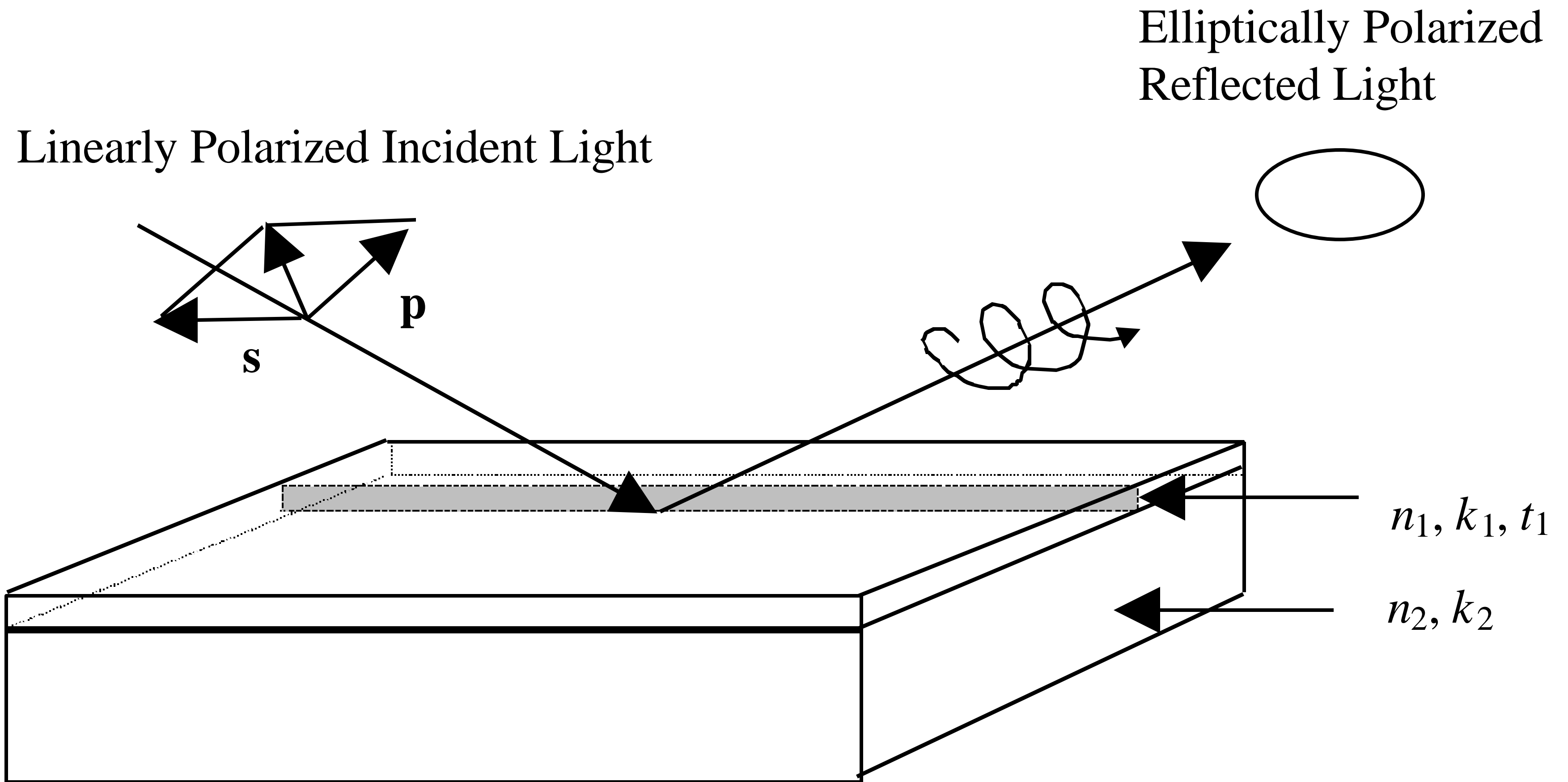
Oxide Measurement

- Thickness
- Uniformity

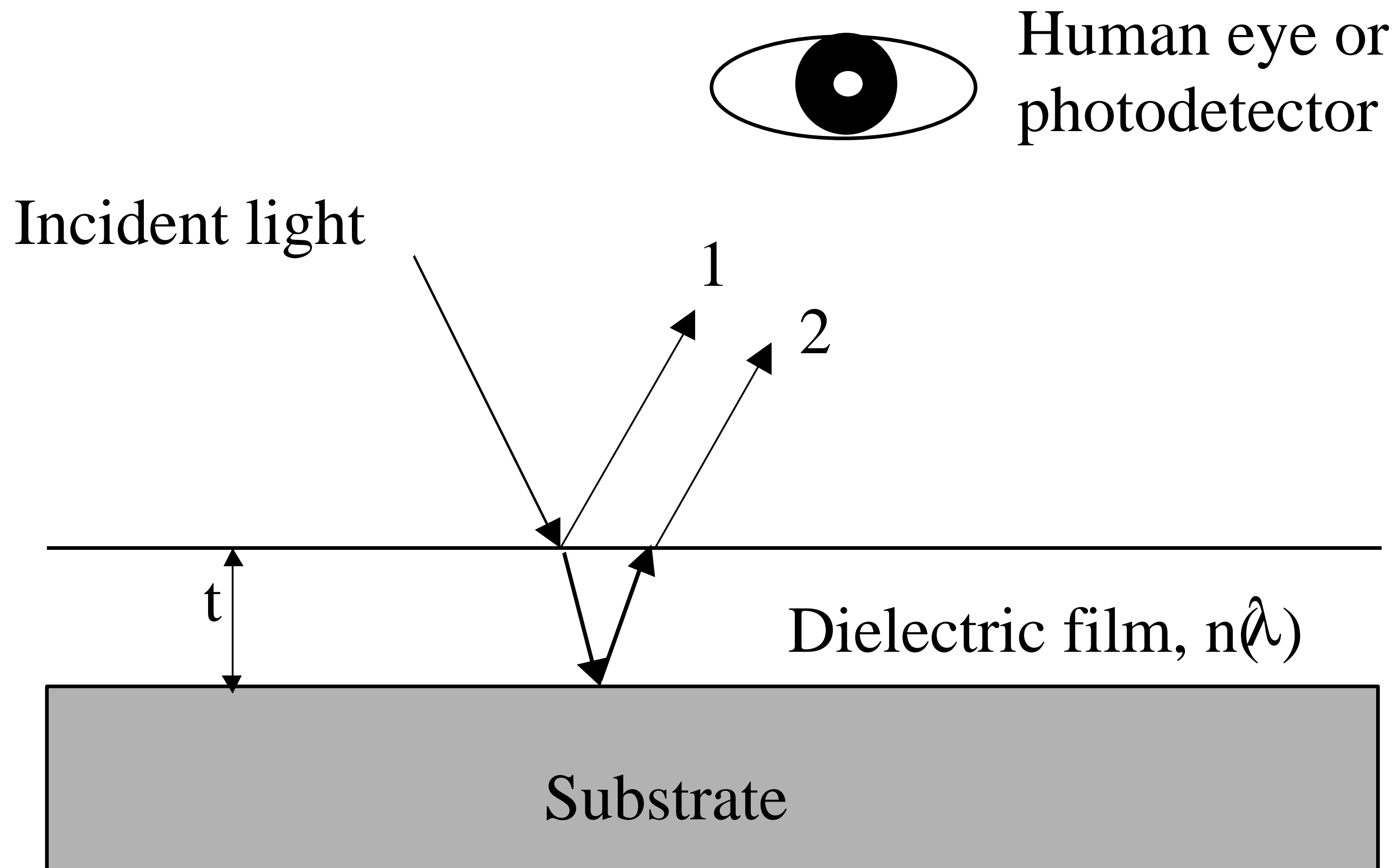
- Color chart
- Ellipsometry
- Reflectometry

- Gate oxide
- Break down voltage
- C-V characteristics

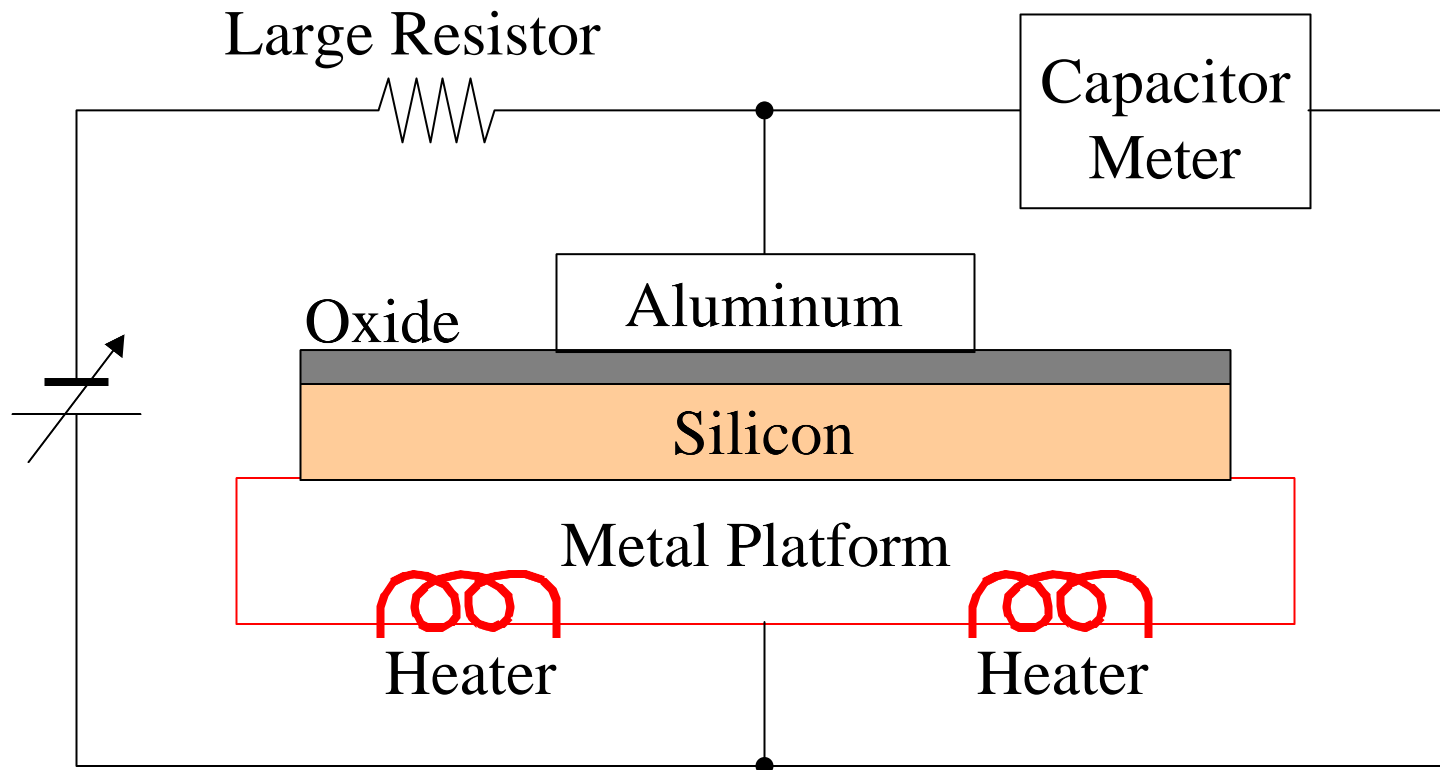
Ellipsometry



Reflectometry



C-V Test Configuration



Summary of Oxidation

- Oxidation of silicon
- High stability and relatively easy to get.
- Application
  - Isolation, masking, pad, barrier, gate, and etc.
- Wet and Dry
- More dry processes for advanced IC chips
- Rapid thermal oxidation and annealing for ultra-thin gate oxide

Diffusion

Diffusion

- Most common physics phenomena
- Materials disperse from higher concentration to lower concentration region
- Silicon dioxide as diffusion mask
- Was widely used for semiconductor doping
- “Diffusion Furnace” and “Diffusion Bay”

Illustration of Diffusion Doping

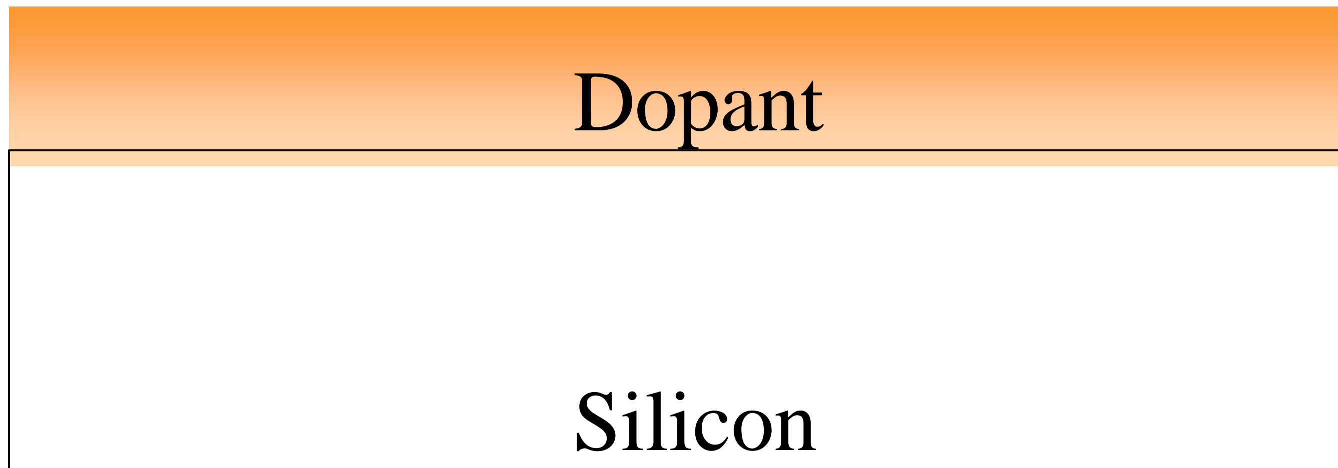
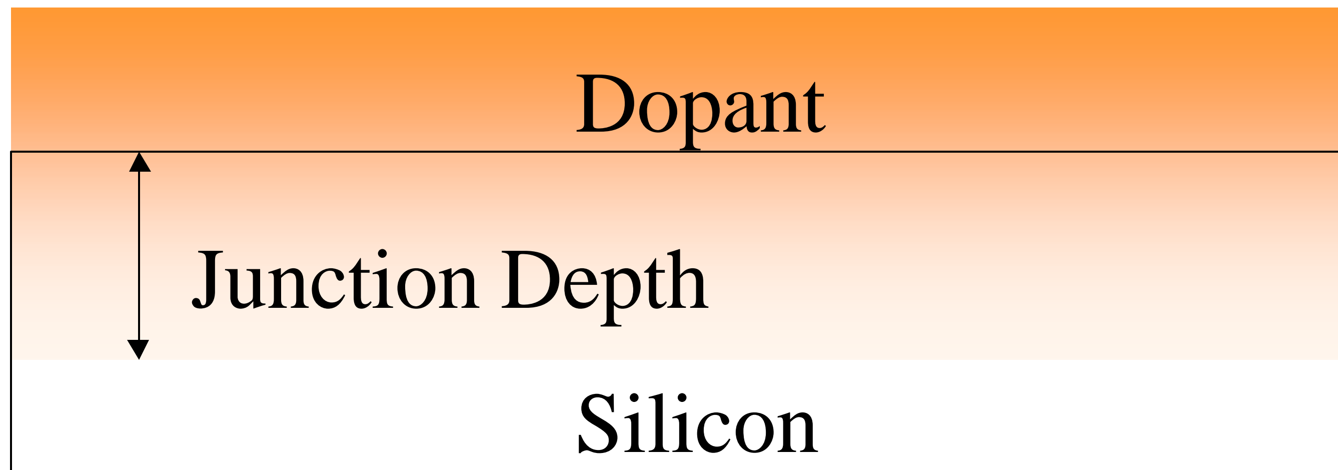
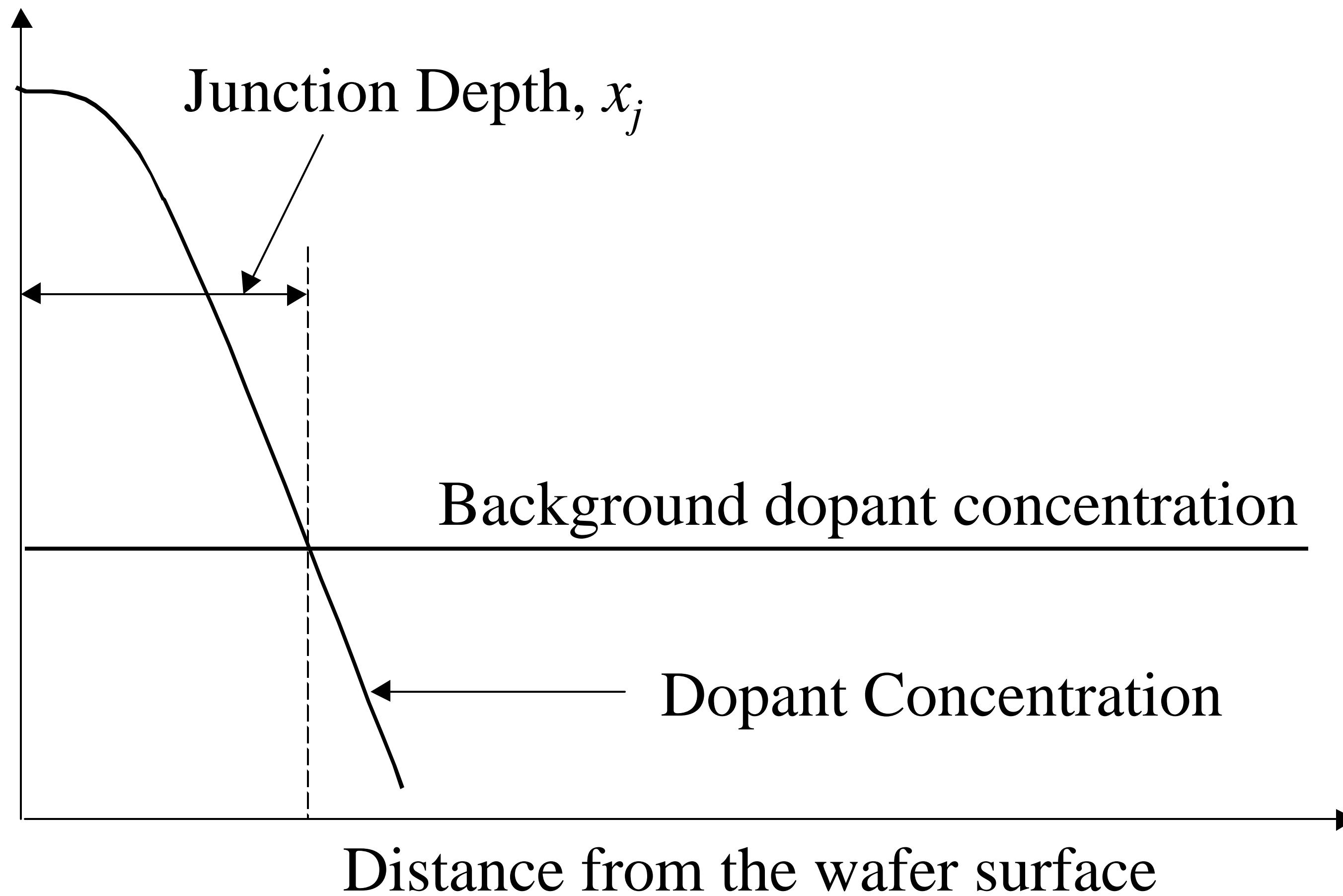


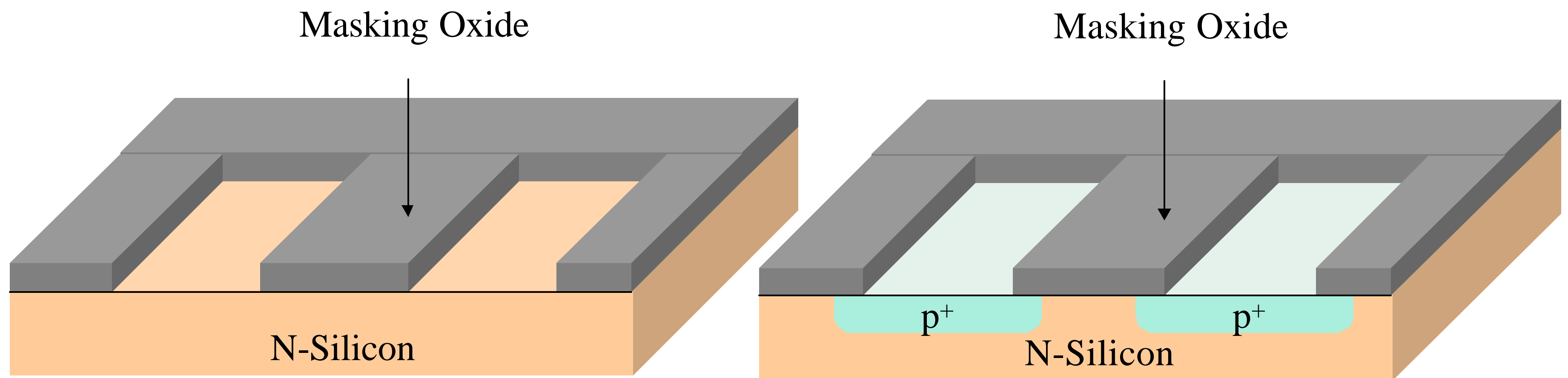
Illustration of Diffusion Doping



Definition of Junction depth



Diffusion



Diffusion

- Replaced by ion implantation due to the less process control
- Still being used in drive-in for well formation

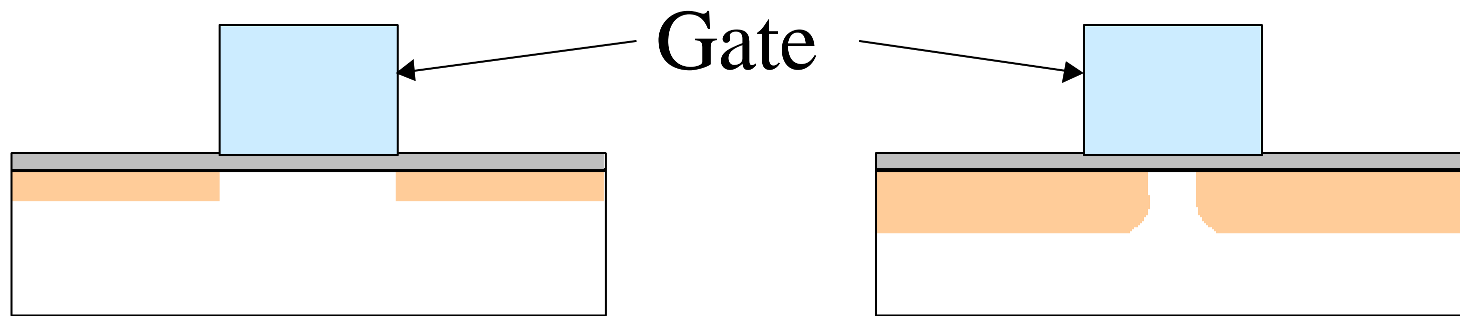
Thermal Budget

- Dopant atoms diffuse fast at high temperature

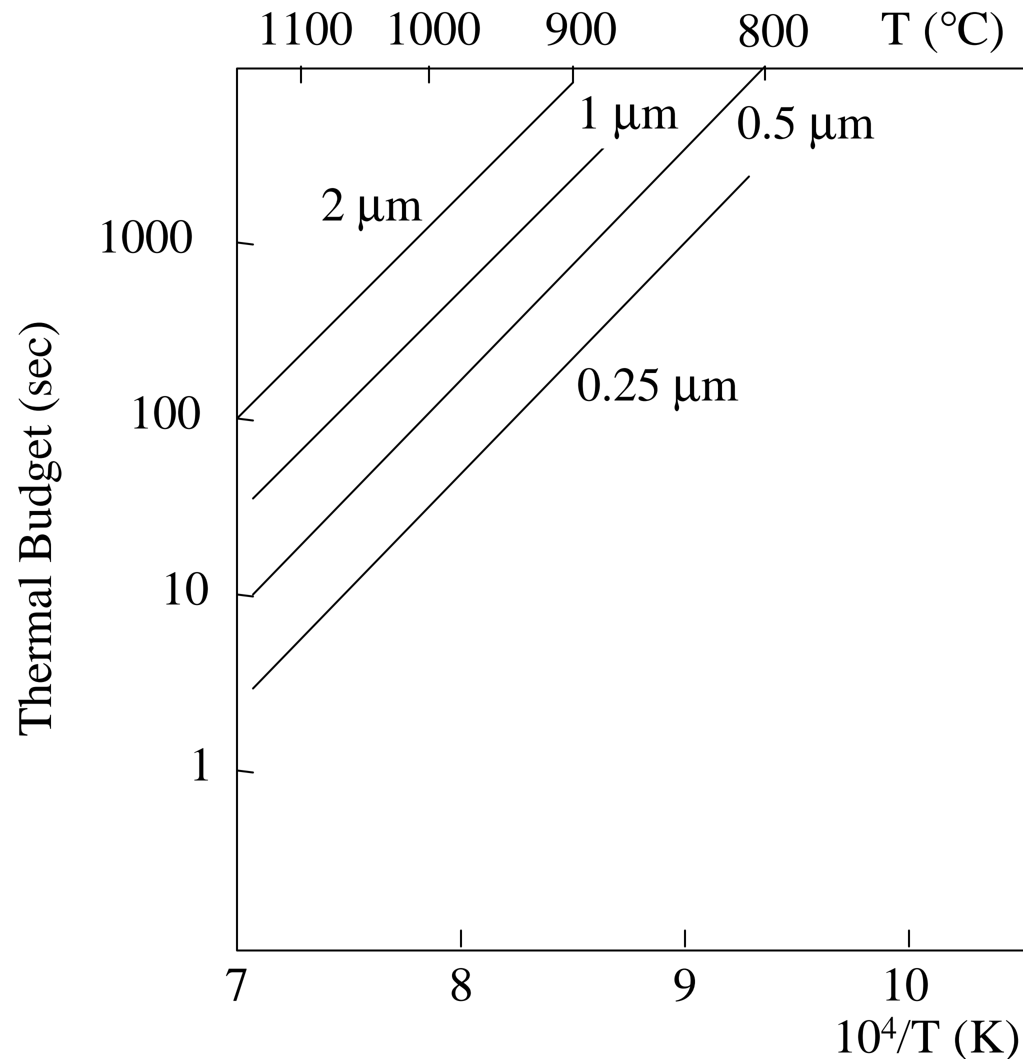
$$D = D_0 \exp(-E_A/kT)$$

- Smaller device geometry, less room for dopant thermal diffusion, less thermal budget
- Thermal budget determines the time and temperature of the post-implantation thermal processes

Illustration of Thermal Budget



Thermal Budget



Source: Chang and Sze, *ULSI Technology*

Diffusion Doping Process

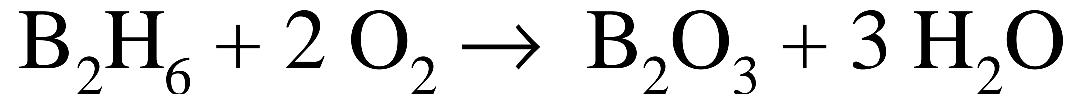
- Both dopant concentration and junction depth are related to temperature.
- No way to independently to control both factor
- Isotropic dopant profile
- Replaced by ion implantation after the mid-1970s.

Diffusion Doping Process

- Silicon dioxide as hard mask
- Deposit dopant oxide
- Cap oxidation
  - prevent dopant diffusion into gas phase
- Drive-in

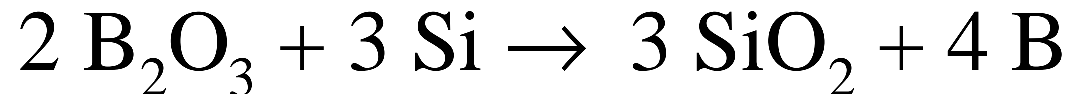
Diffusion Doping Process

- Oxidation, photolithography and oxide etch
- Pre-deposition:

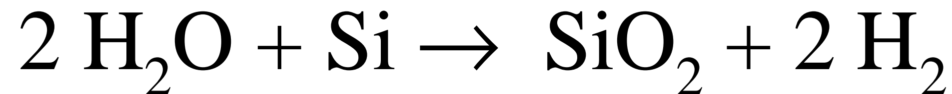


$$B_2H_6 + 2\ O_2 \rightarrow B_2O_3 + 3\ H_2O$$

- Cap oxidation:



$$2\ B_2O_3 + 3\ Si \rightarrow 3\ SiO_2 + 4\ B$$

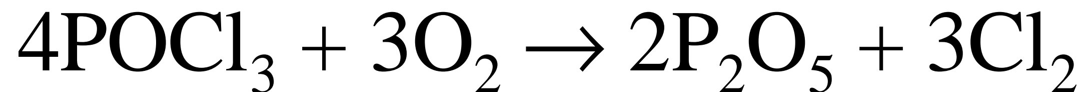


$$2\ H_2O + Si \rightarrow SiO_2 + 2\ H_2$$

- Drive-in
  - Boron diffuses into silicon substrate

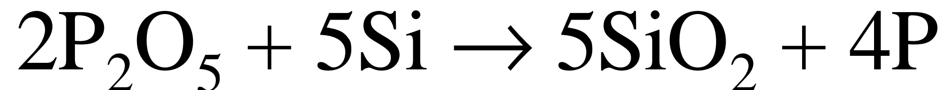
Diffusion Doping Process

- Oxidation, photolithography and oxide etch
- Deposit dopant oxide:



$$4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 3Cl_2$$

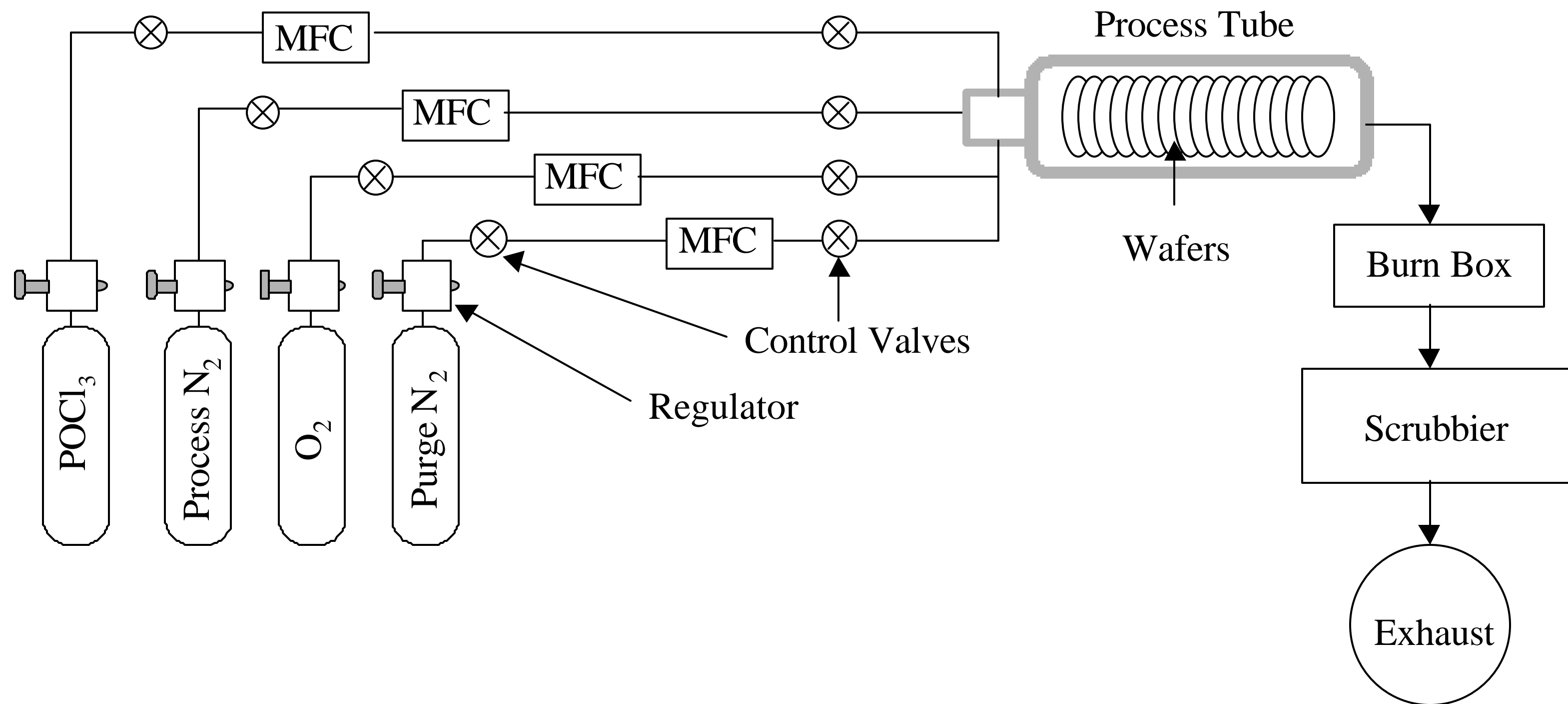
- Cap oxidation



$$2P_2O_5 + 5Si \rightarrow 5SiO_2 + 4P$$

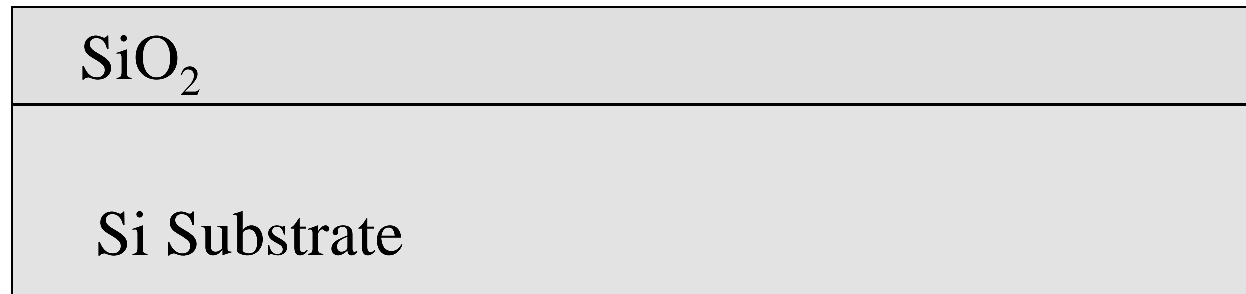
  – Phosphorus concentrates on silicon surface
- Drive-in
  – Phosphorus diffuses into silicon substrate

Phosphorus Diffusion System

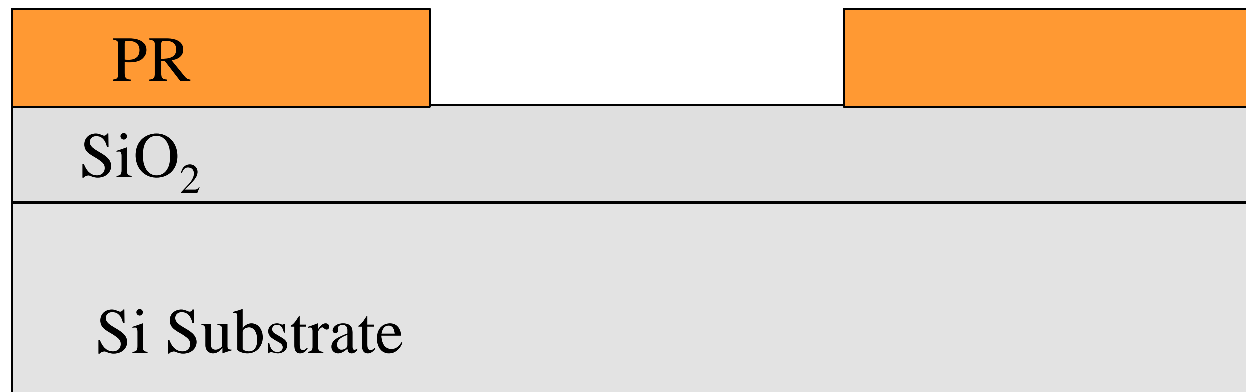


Wafer Clean

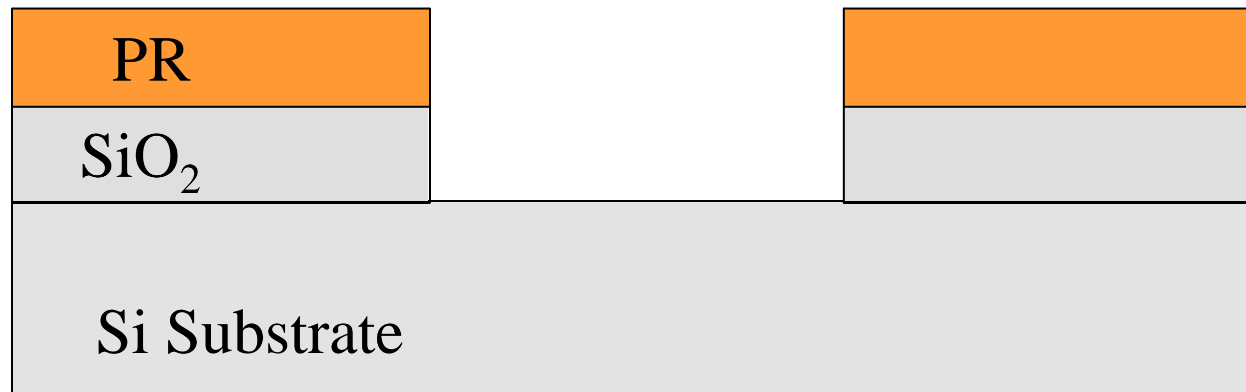
Oxidation



Doped Area Patterning



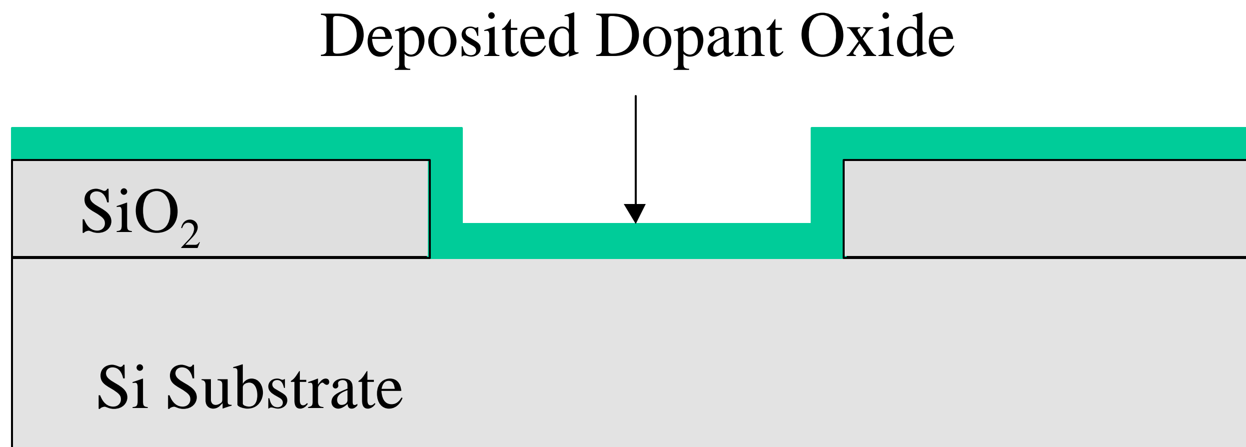
Etch Silicon Dioxide



Strip Photoresist

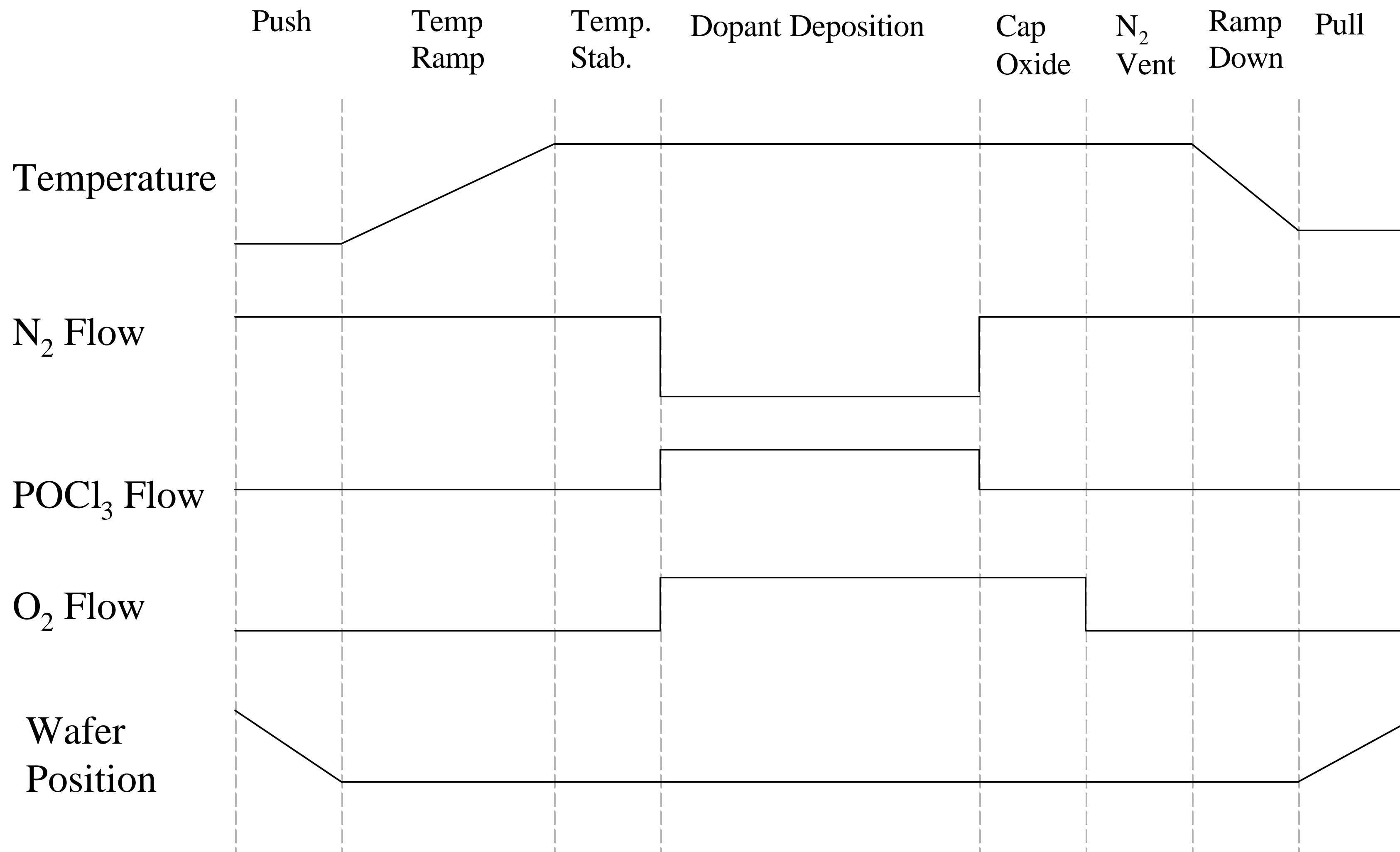
Wafer Clean

Dopant Oxide Deposition

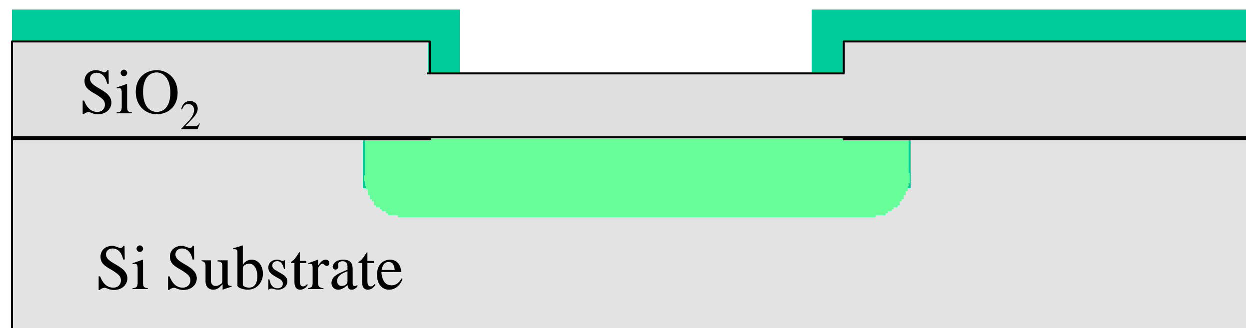


Cap Oxidation

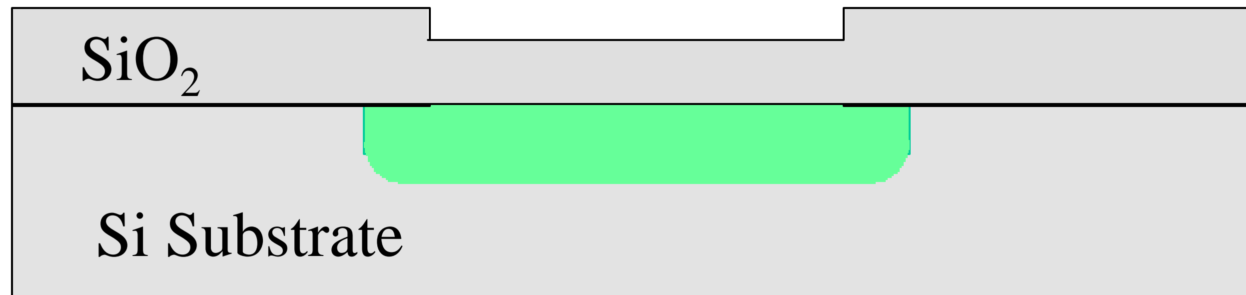
Phosphoric Oxide Deposition and Cap Oxidation



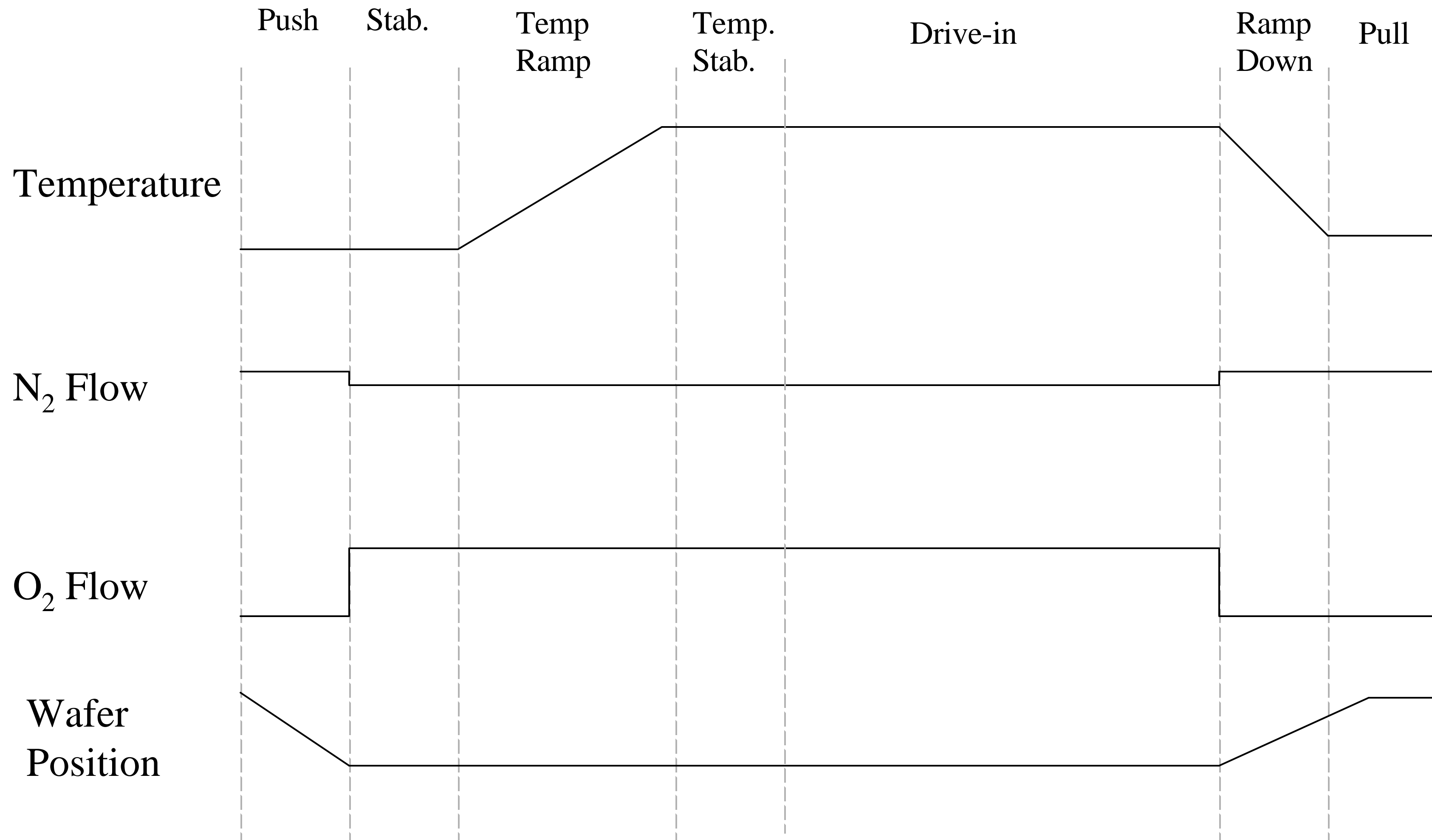
Drive-in



Strip Oxide, Ready for Next Step



Phosphorus Drive-in



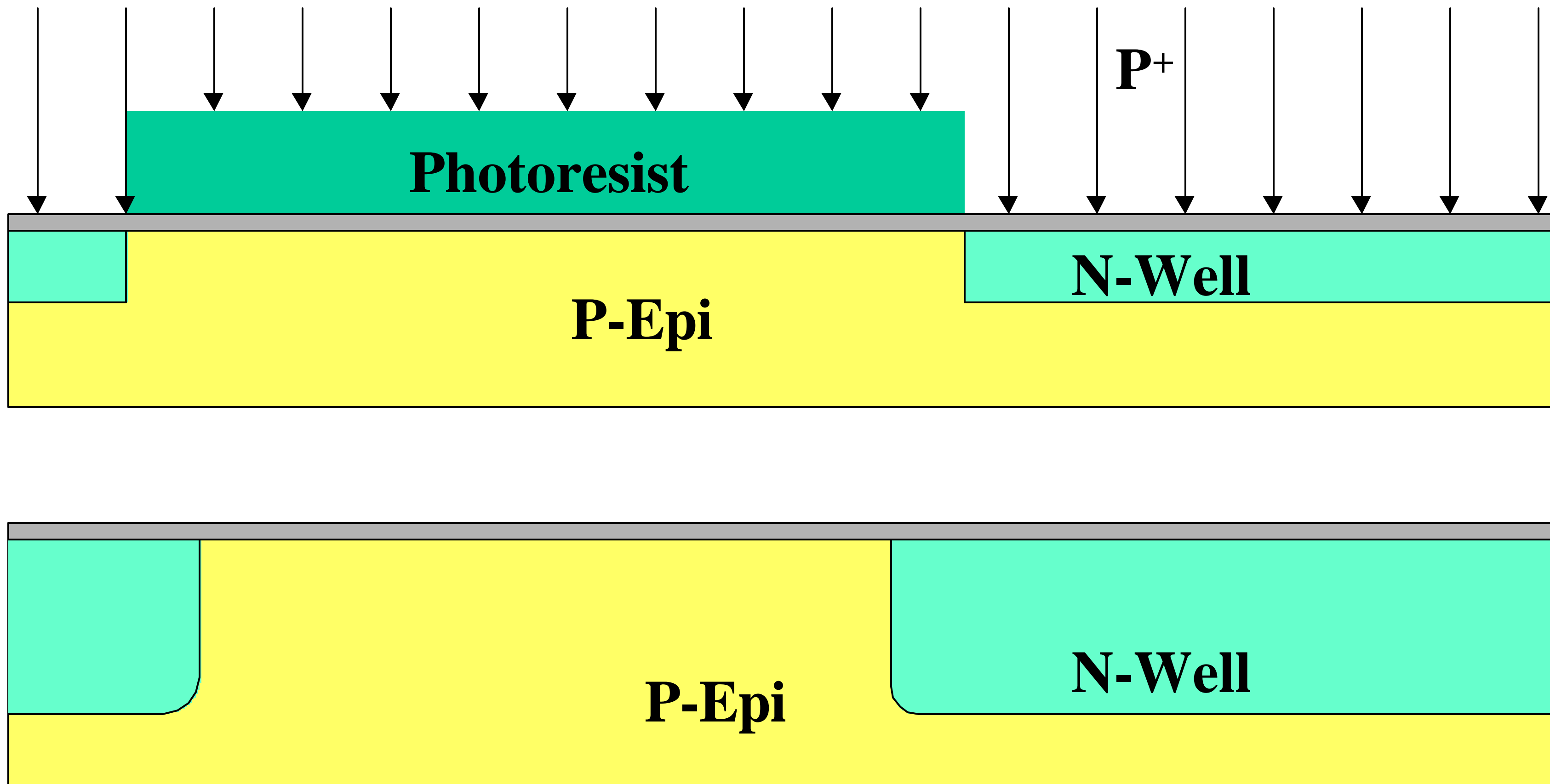
Limitations and Applications

- Diffusion is isotropic process and always dope underneath masking oxide
- Can't independently control junction depth and dopant concentration
- Used for well implantation drive-in
- R&D for ultra shallow junction (USJ) formation

Application of Diffusion: Drive-in

- Wells have the deepest junction depth
- Need very high ion implantation energy
- Cost of MeV ion implanters is very high
- Diffusion can help to drive dopant to the desired junction depth while annealing

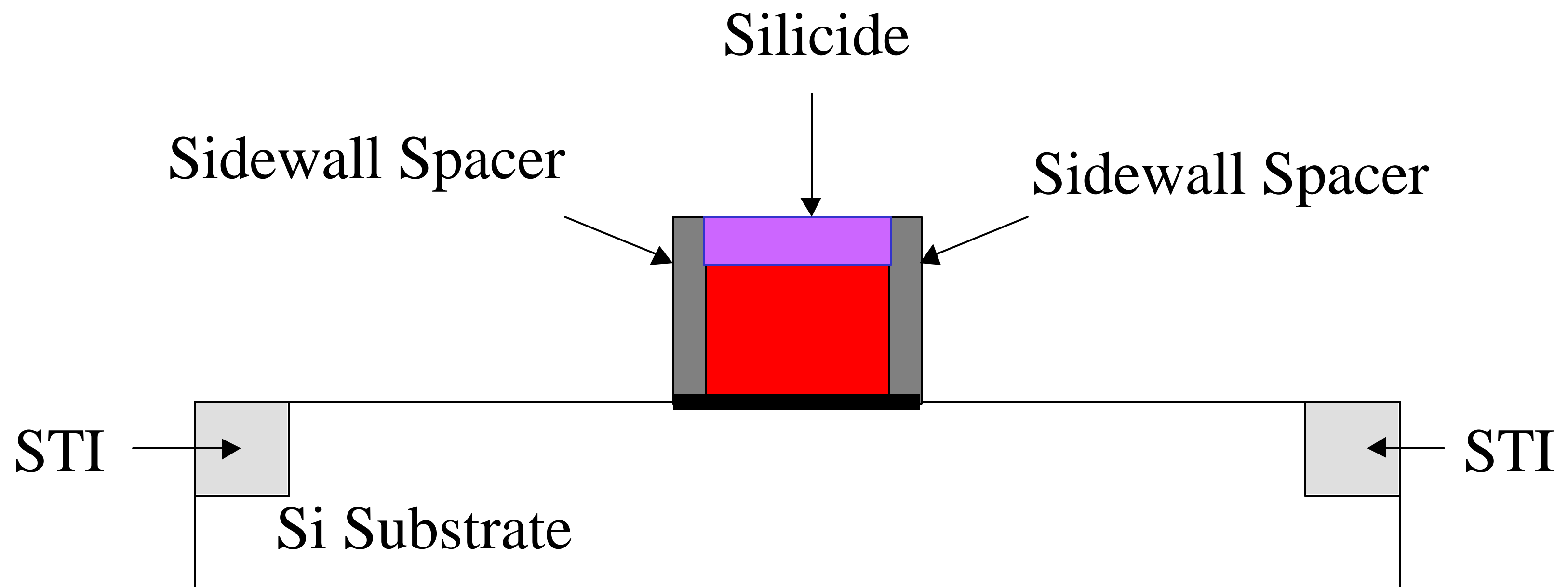
Well Implantation and Drive-in



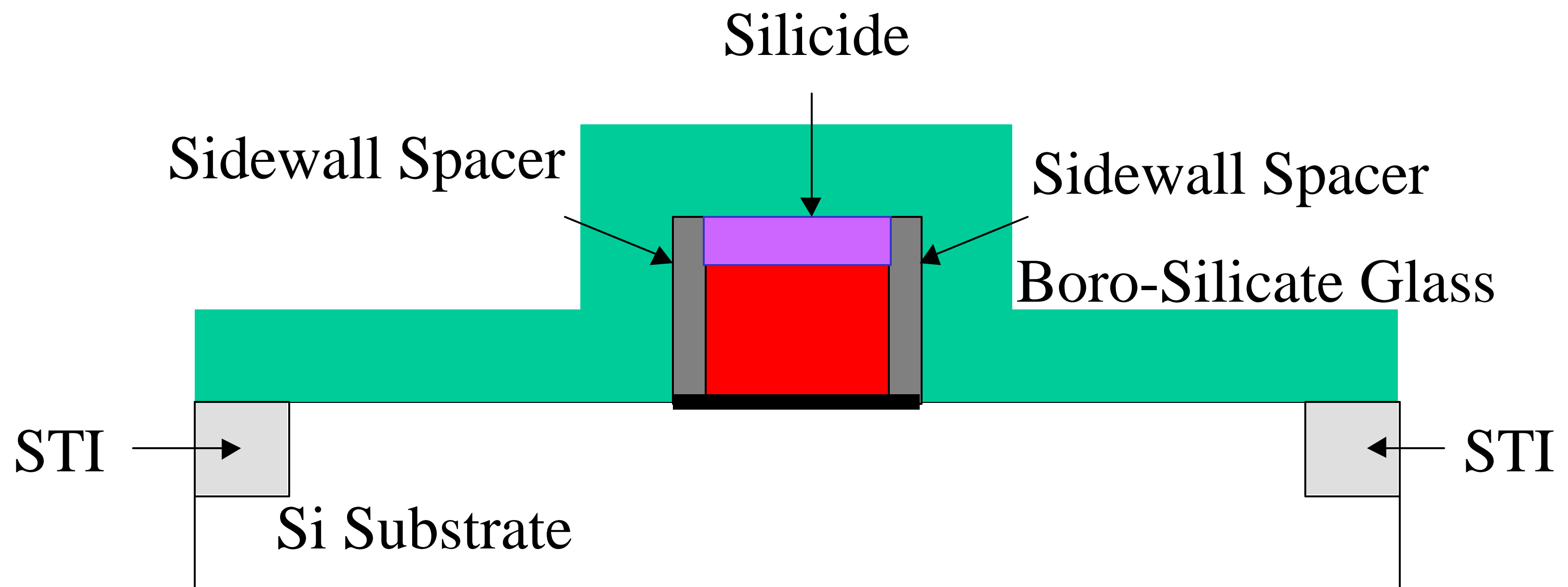
Diffusion for Boron USJ Formation

- Small devices needs ultra shallow junction
- Boron is small and light, implanter energy could be too high for it goes too deep
- Controlled thermal diffusion is used in R&D for shallow junction formation

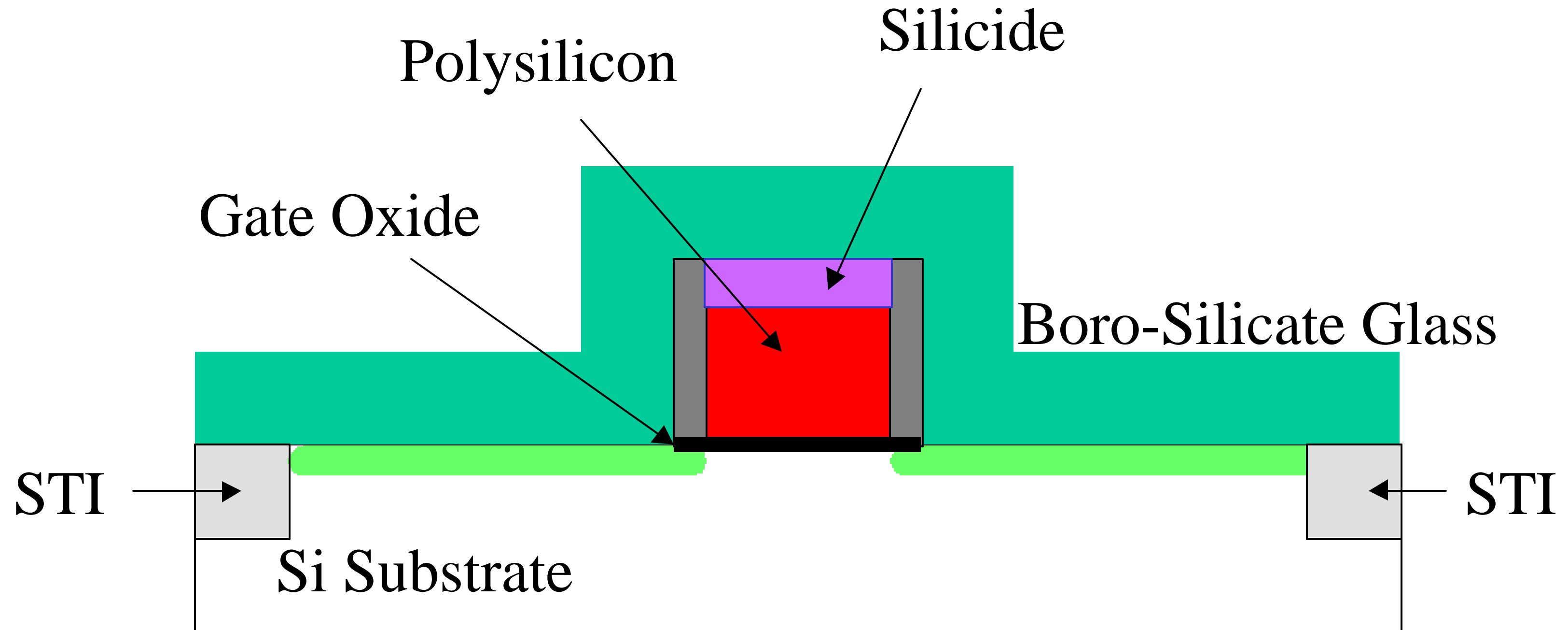
Surface Clean



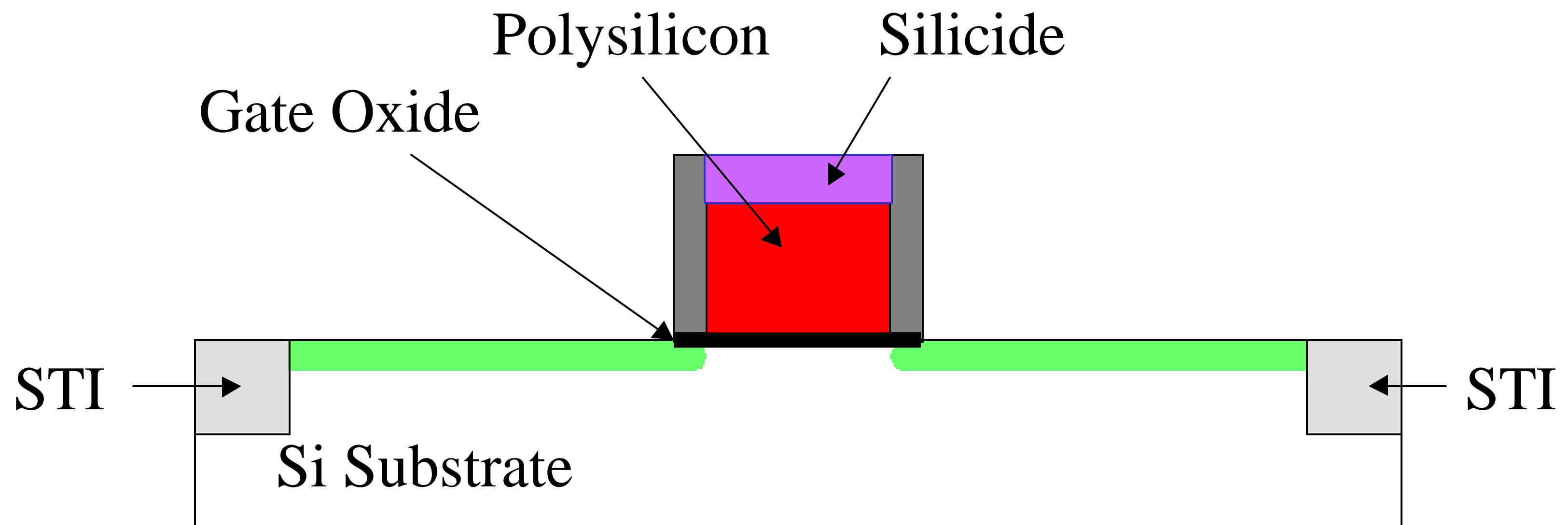
BSG CVD



RTP Dopant Drive-in



Strip BSG

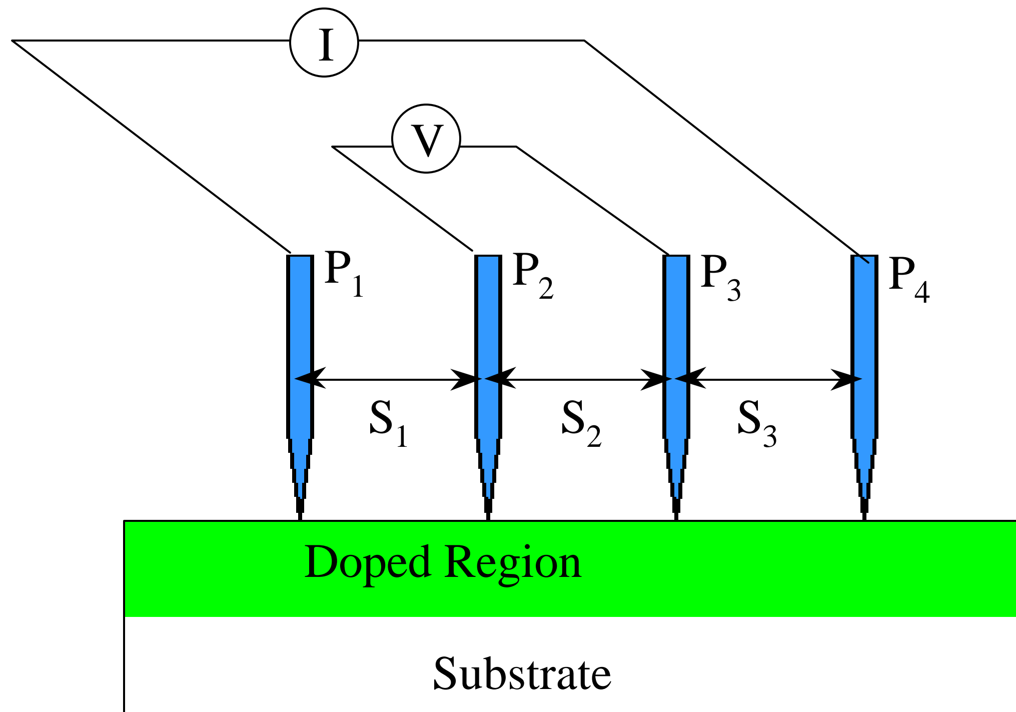


Doping Measurement

- Four-point probe

$$R_s = \boldsymbol{r}/t$$

Four-Point Probe Measurement



Summary of Diffusion

- Physics of diffusion is well understood
- Diffusion was widely used in doping processes in early IC manufacturing
- Replaced by ion implantation since the mid-1970s

Annealing and RTP Processes

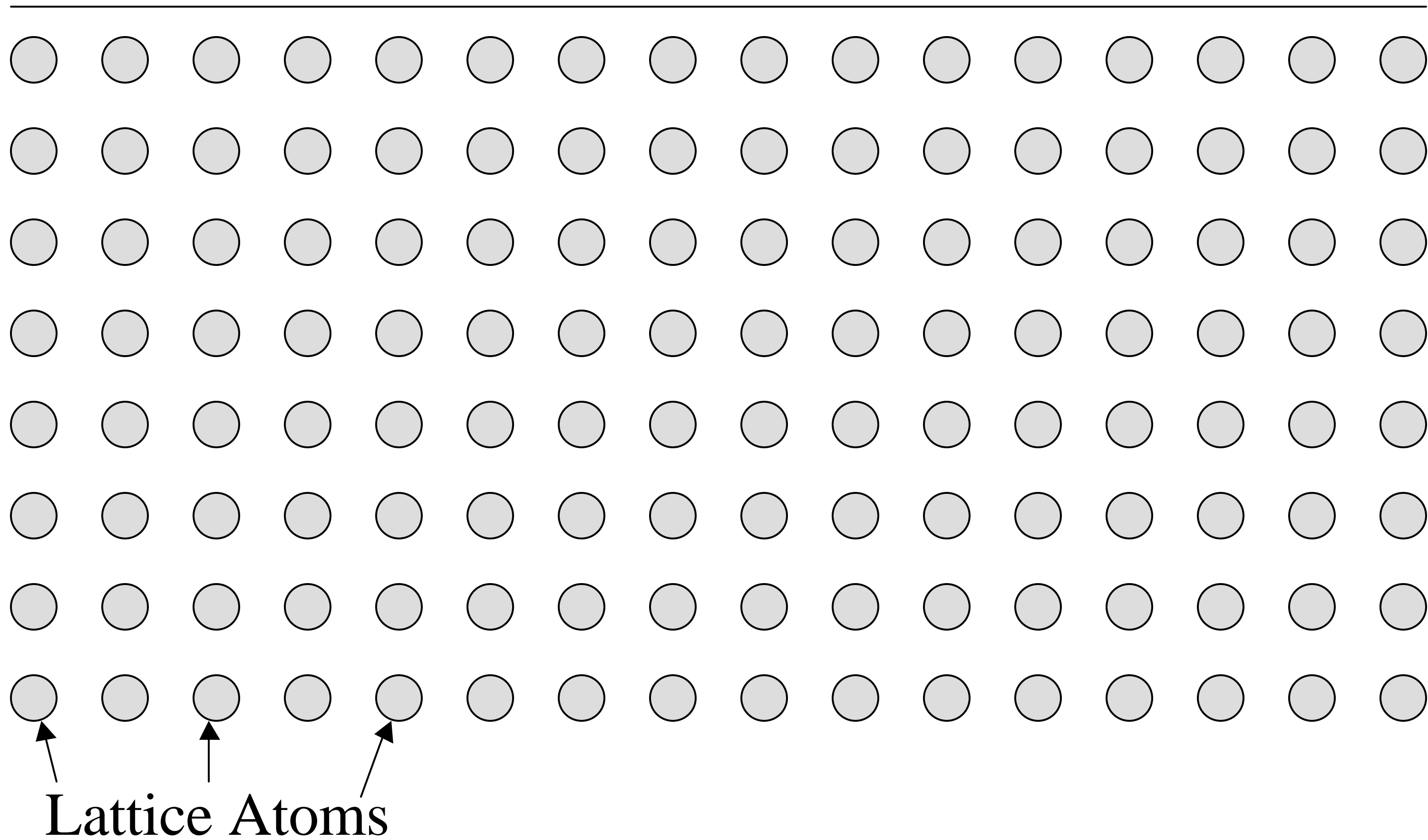
Post-implantation Annealing

- Energetic ions damage crystal structure
- Amorphous silicon has high resistivity
- Need external energy such as heat for atoms to recover single crystal structure
- Only in single crystal structure dopants can be activated

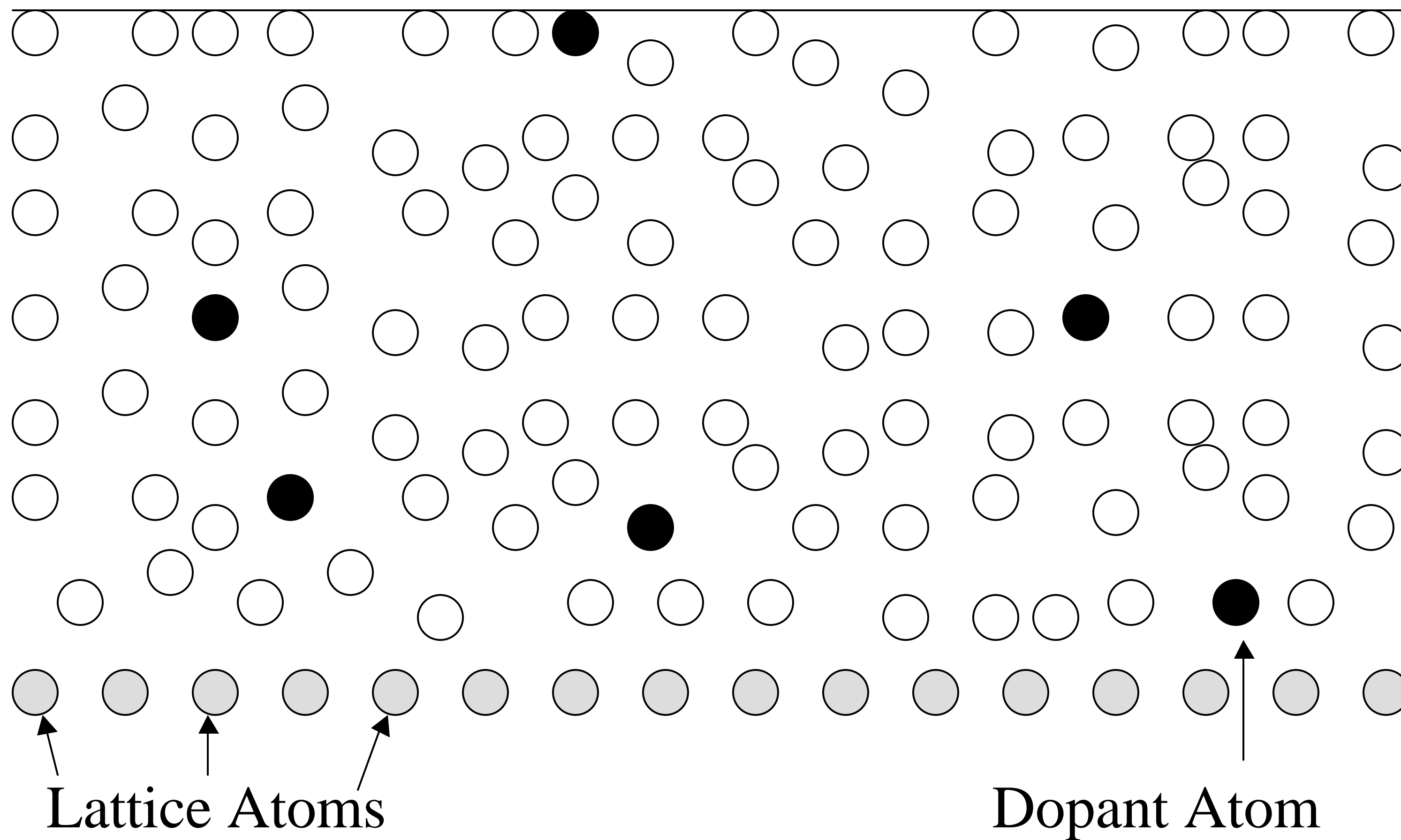
Post-implantation Annealing

- Single crystal structure has lowest potential energy
- Atoms tend to stop on lattice grid
- Heat can provide energy to atoms for fast thermal motion
- Atoms will find and settle at the lattice grid where has the lowest potential energy position
- Higher temperature, faster annealing

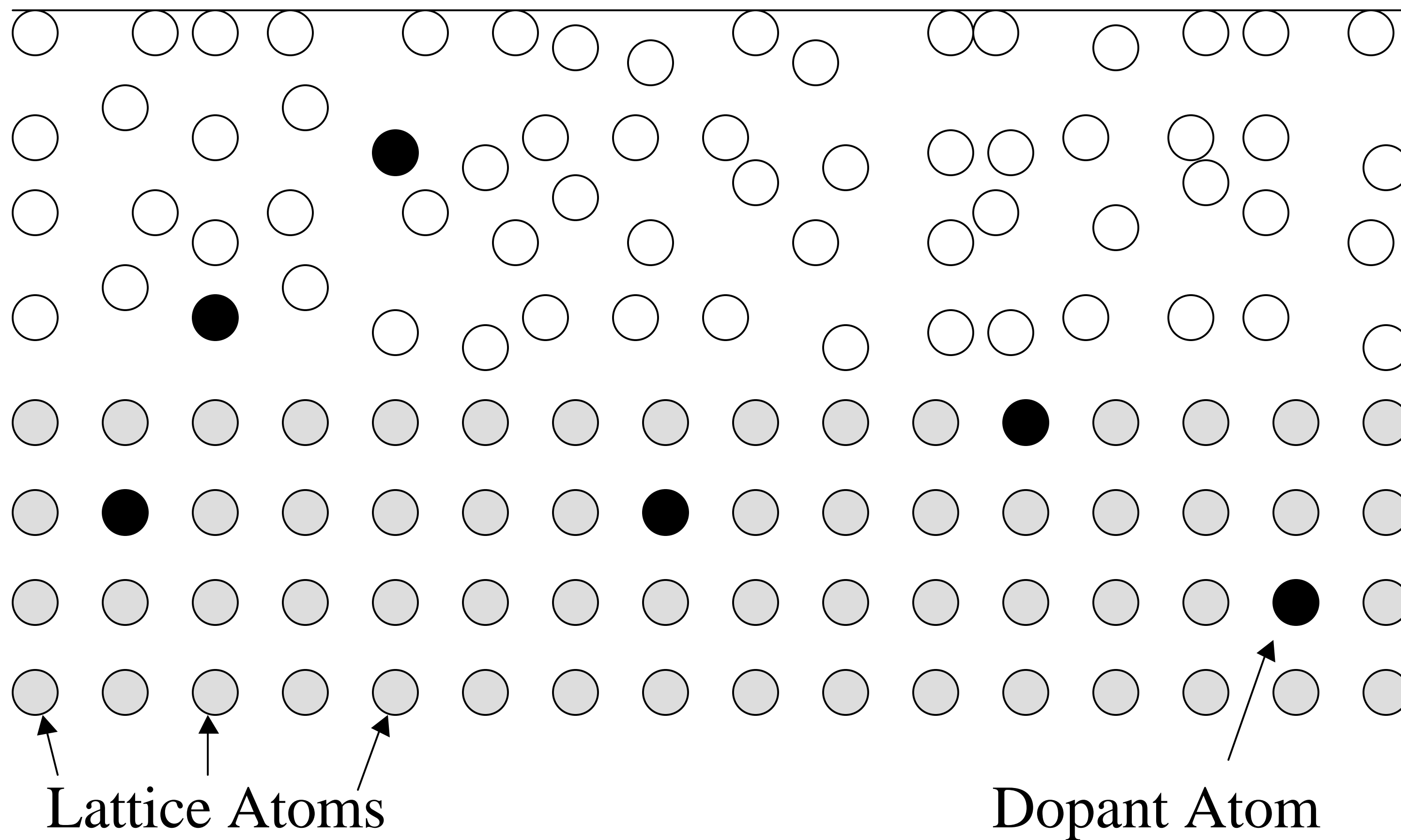
Before Ion Implantation



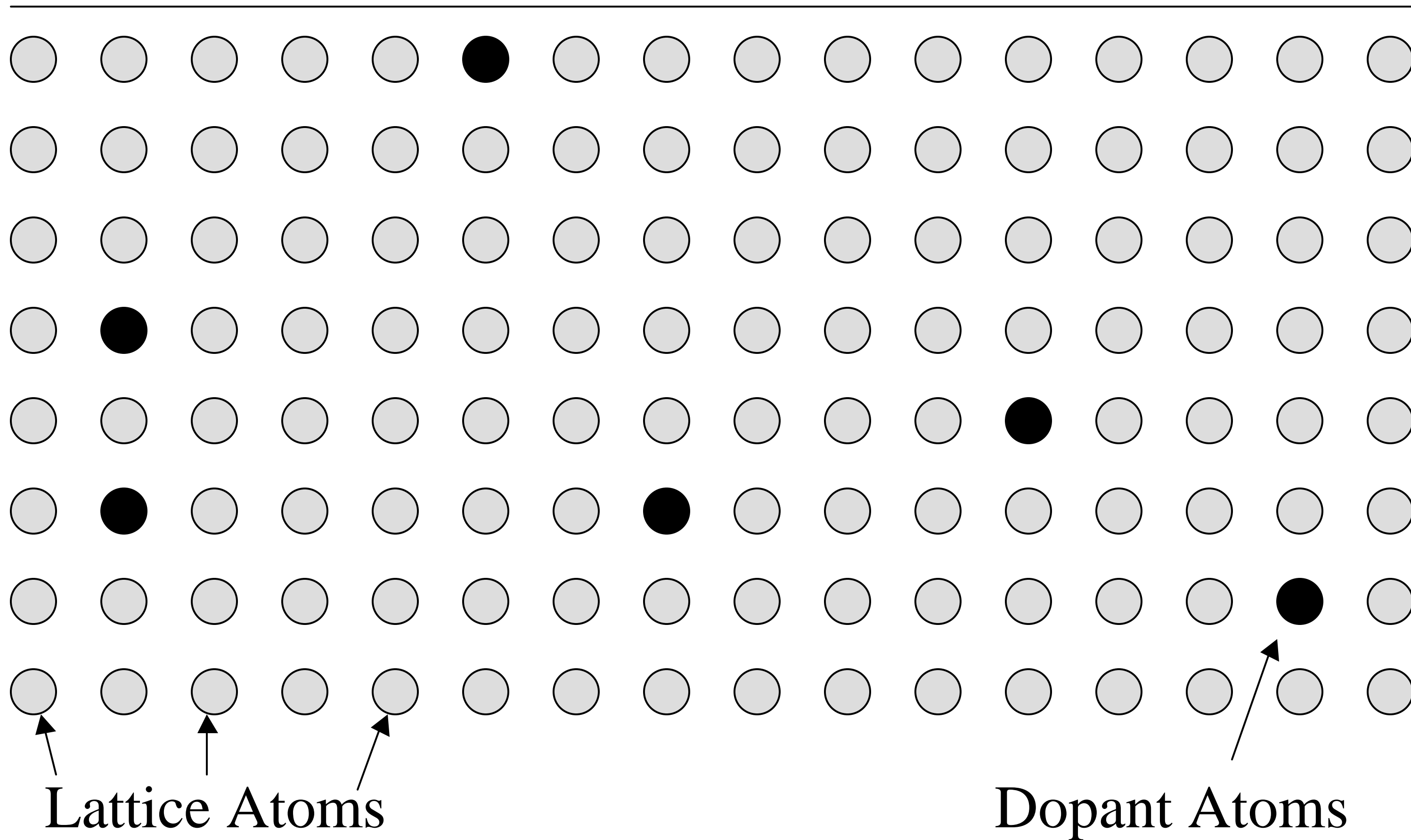
After Ion Implantation



Thermal Annealing



Thermal Annealing



Annoy Annealing

- A thermal process in which different atoms chemically bond with each other to form a metal alloy.
- Widely used in silicide formation
- Self aligned silicide (salicide)
  - Titanium silicide, $TiSi_2$
  - Cobalt silicide, $CoSi_2$
- Furnace and RTP

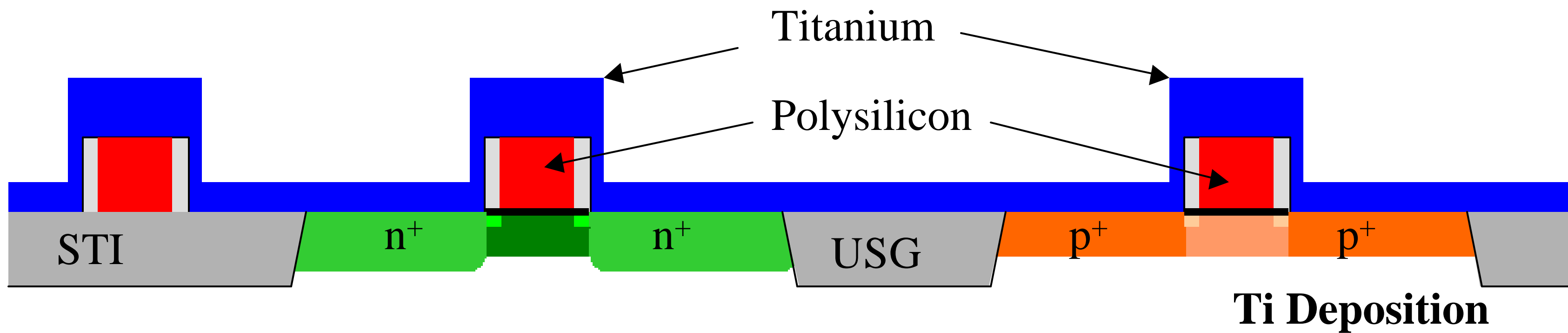
Silicide

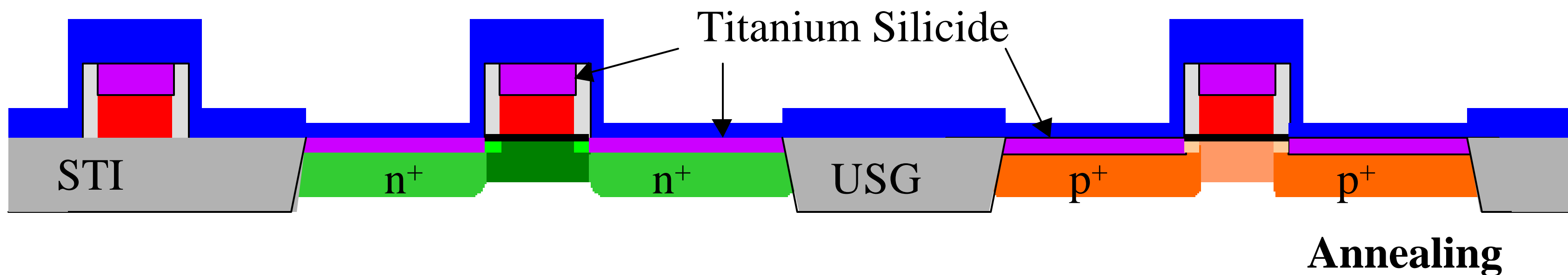
- Much lower resistivity than polysilicon
- Used as gate and local interconnection
- Used as capacitor electrodes
- Improving device speed and reduce heat generation
- $TiSi_2$, WSi_2 are the most commonly used silicide
- $CoSi_2$, $MoSi_2$, and etc are also used

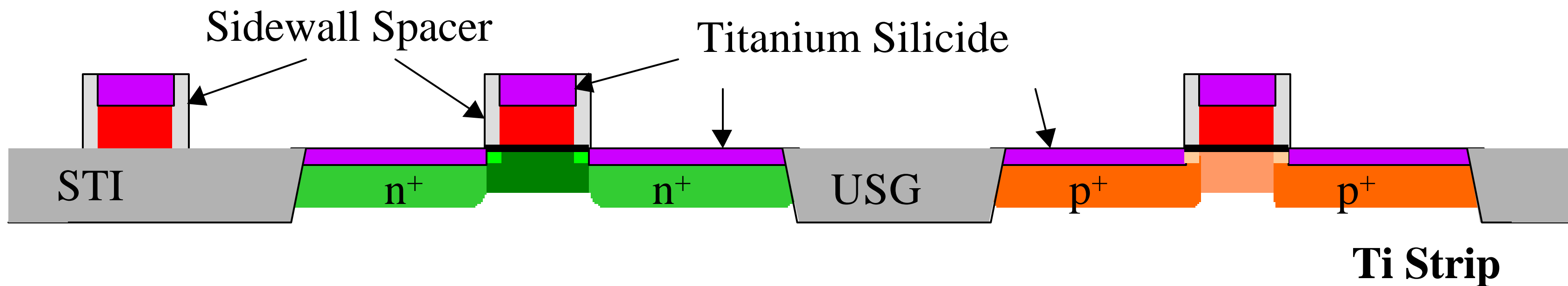
Titanium Silicide Process

- Argon sputtering clean
- Titanium PVD
- RTP Anneal, ~700 °C
- Strip titanium, H_2O_2:H_2SO_2

Titanium Silicide Process







Aluminum-silicon Alloy

- Form on silicon surface
- Prevent junction spiking due to silicon dissolving in aluminum

Junction Spike

Al

Al

Al

SiO_2

p^+

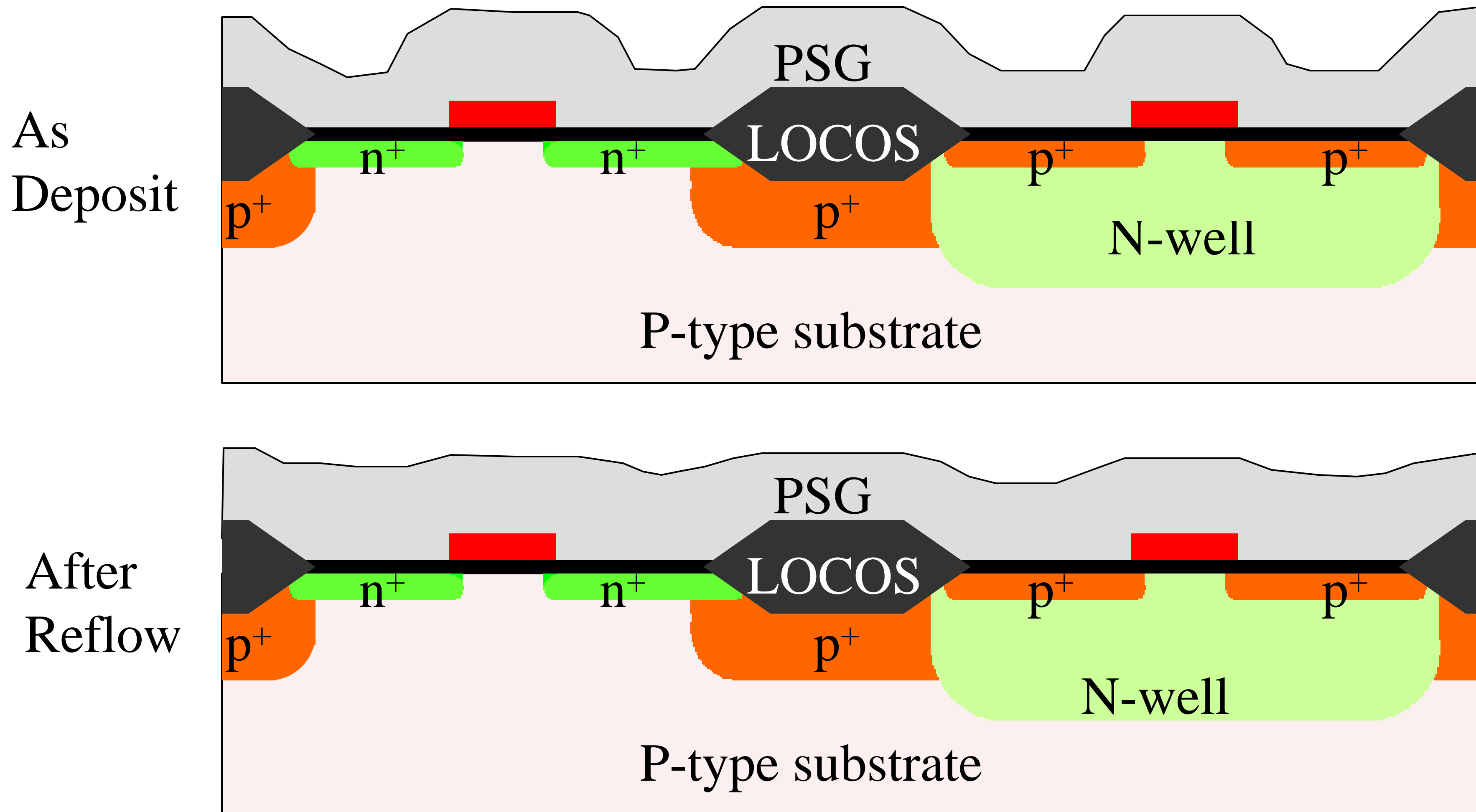
p^+

n-type Silicon

Reflow

- Flowed surface is smoother and flatter
- Easier for photolithography and metallization
- Higher temperature, better flow result
- Reflow time and temperature are determined by the thermal budget
- Higher dopant concentration requires lower flow temperature

Illustration of BPSG Reflow



Reflow

- Undoped silicate glass (USG) becomes soften at very high temperature T > 1500 °C, will flow due to the surface tension
- PSG and BPSG become soften at significant lower temperature (< 1100 °C down to 850 °C)
- Phosphorus also can trap sodium
- PSG and BPSG is commonly used as pre-metal dielectric (PMD)

Reflow Process

- Wafer loading
- Temperature rump-up
- Temperature stabilization
- Reflow
- Temperature rump-down
- Wafer unloading

Reflow Process

- Reflow usually used N_2 ambient
- Sometimes H_2O vapor is also used
- H_2O helps to filly oxidize dopant atoms

Reflow Process

- Smaller device, less thermal budget
- No enough thermal budget for reflow for sub-0.25 μm devices
- PSG anneal (~750 °C) instead of reflow

Summary of Anneal

- The most commonly used anneal processes are post-implantation annealing, alloy annealing and reflow
- Thermal anneal is required after ion implantation for recover crystal structure and activation dopant atoms
- Thermal anneal helps metal to react with silicon to form silicides

Summary of Anneal

- Metal anneal helps to form larger grain size and reduces the resistivity
- PSG or BPSG reflow smoothens and flattens the dielectric surface and helps photolithography and metallization processes
- RTP becomes more commonly used in annealing processes

Summary of Anneal

- Advantages of RTP
  - Much faster ramp rate (75 to 150 °C/sec)
  - Higher temperature (up to 1200 °C)
  - Faster process
  - Minimize the dopant diffusion
  - Better control of thermal budget
  - Better wafer to wafer uniformity control

High Temperature Deposition Processes

What is CVD

Chemical Vapor Deposition

- Gas(es) or vapor(s) chemically react on substrate surface and form solid byproduct on the surface as deposited thin film.
- Other byproducts are gases and leave the surface.
- Widely used in IC processing for metal, dielectric and silicon thin film deposition.

High Temperature CVD

- Epitaxy
- Polysilicon
- Silicon Nitride

Epitaxy

- Monocrystralline layer
- Epitaxy silicon
- Epitaxy silicon-germanium
- Epitaxy GaAs

Epitaxy Silicon

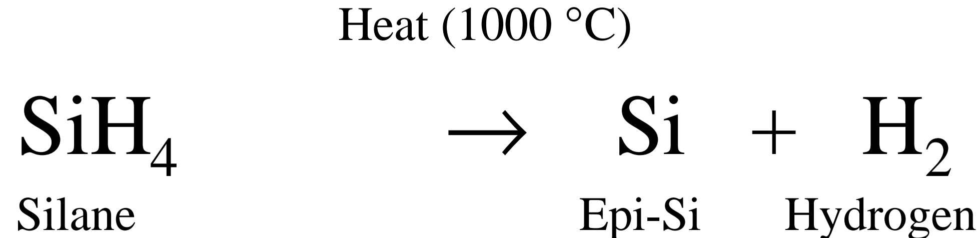
- Provide high quality silicon substrate without trace amount of oxygen and carbon.
- Required for bipolar devices.
- Needed for high performance CMOS devices.

Epitaxy Silicon

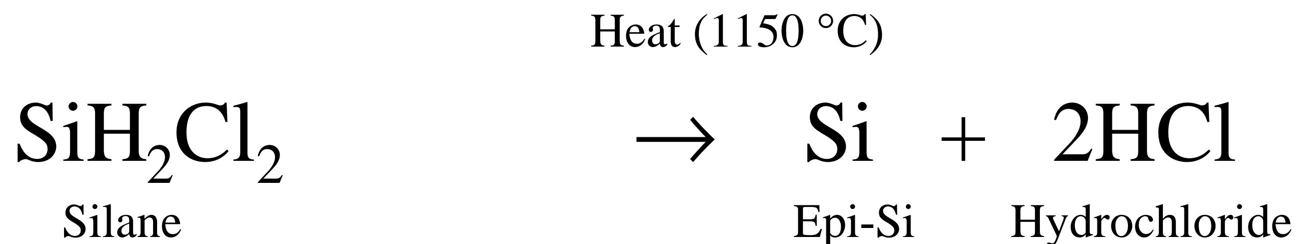
- High temperature (~1000 °C) processes.
- Silane (SiH_4), DCS (SiH_2Cl_2) or TCS ($SiHCl_3$) as silicon source gases.
- Hydrogen as process gas and purge gas
- Arsine (AsH_3), Phosphine (PH_3), and Diborane (B_2H_6) are used as dopant gases.

Epitaxy Silicon Deposition

- Silane process

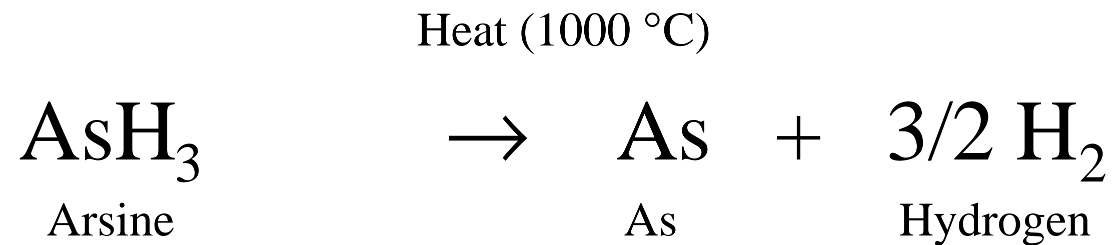


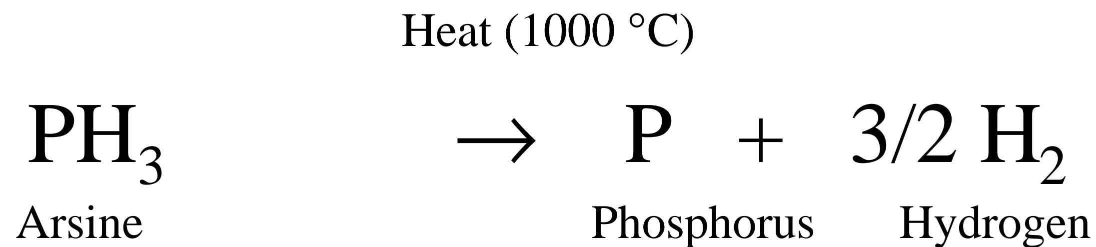
- DCS process



Epitaxy Silicon Doping

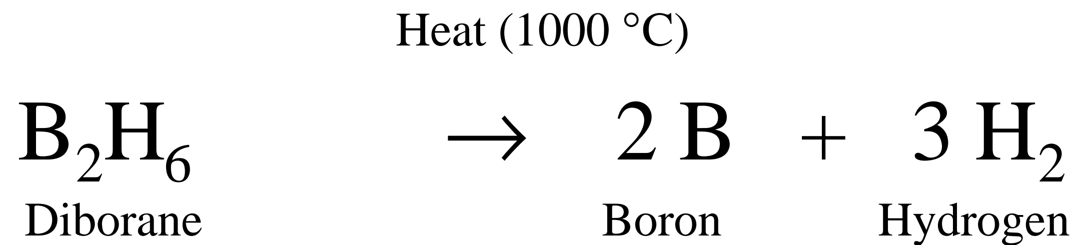
- N-type Dopant





Epitaxy Silicon Doping

- P-type Dopant



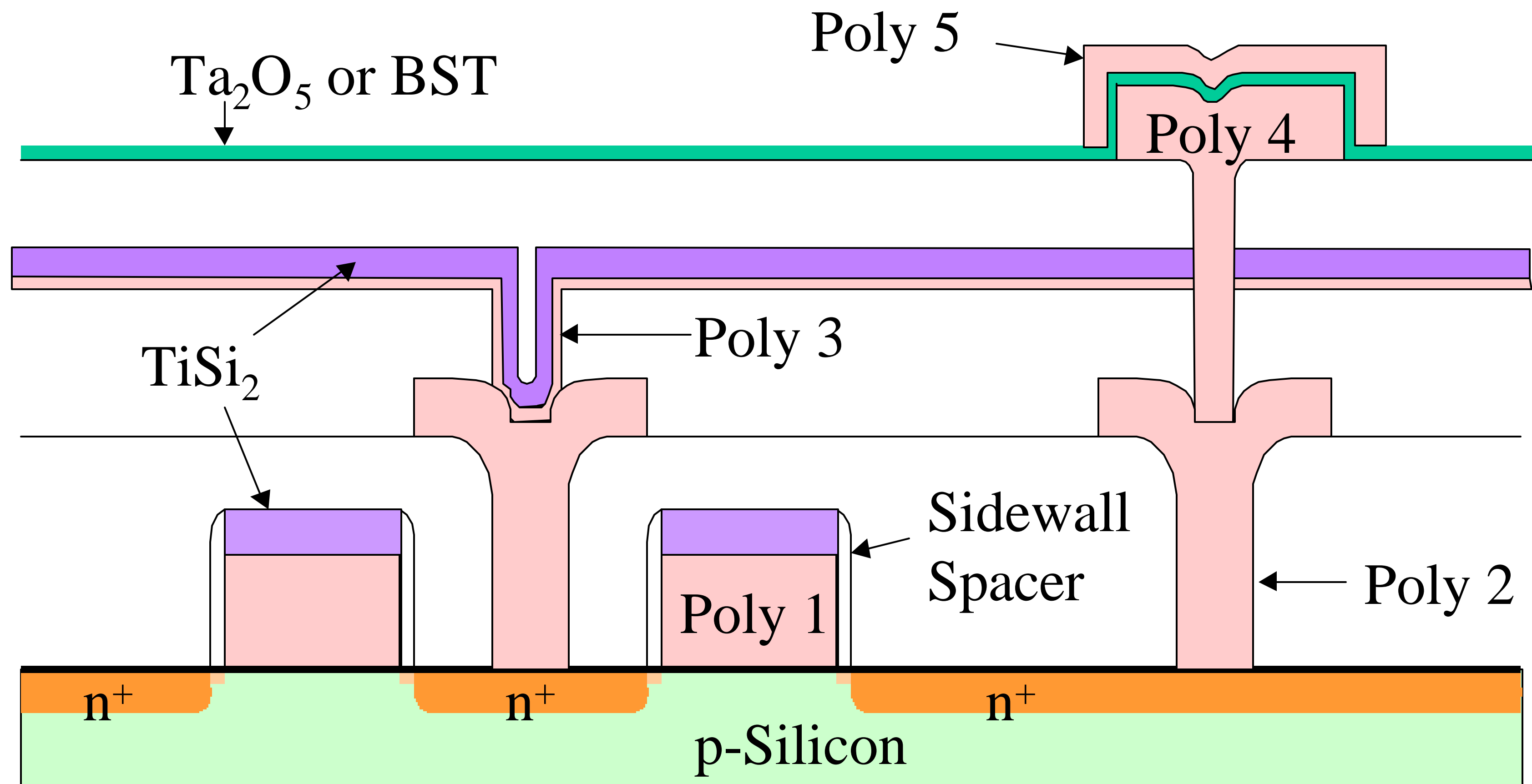
Epitaxy Silicon

- Usually deposited ("grown") by wafer manufacturer instead by IC fab.
- In fab epi process: special needs such as usually dopant concentration and epi thickness.
- Selective epi for raised source/drain.
- Single wafer epitaxy process.

Polysilicon

- High temperature stability.
- Reasonable good conductivity.
- Widely used for the gate and local interconnection in MOS devices.
- Also widely used as the capacitor electrodes in memory devices, especially DRAM.

Polysilicon Applications in DRAM

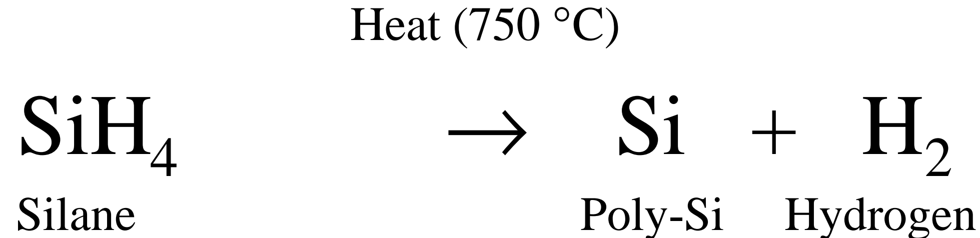


Polysilicon

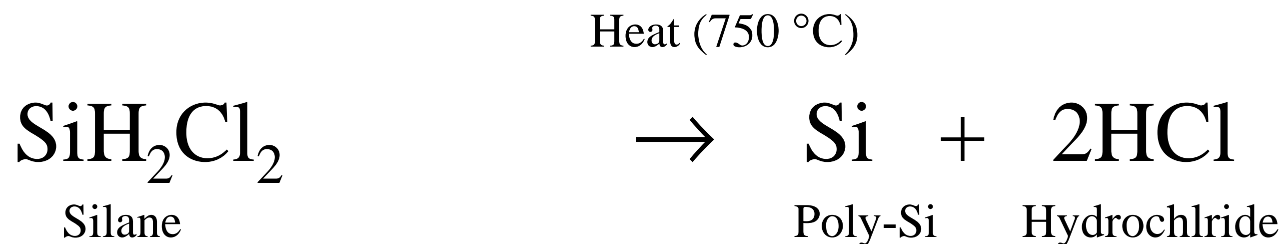
- High temperature (~700 °C) furnace LPCVD processes.
- Silane (SiH_4) or DCS (SiH_2Cl_2) as silicon source gases.
- Nitrogen as purge gas
- Arsine (AsH_3), Phosphine (PH_3), and Diborane (B_2H_6) are used as dopant gases.

Polysilicon Deposition

- Silane process

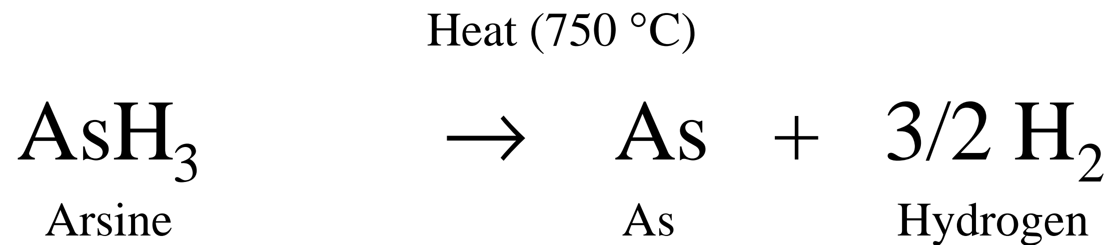


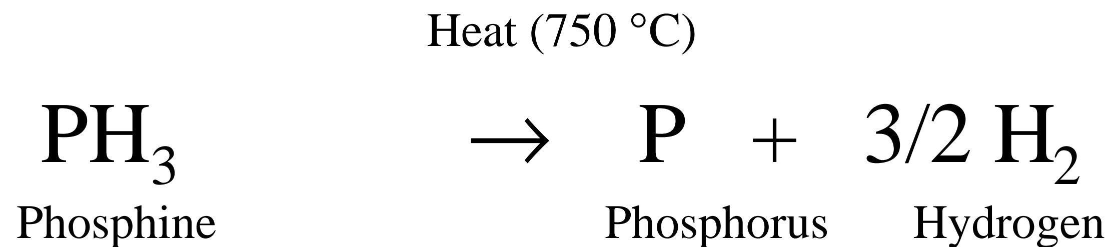
- DCS process



Polysilicon Doping

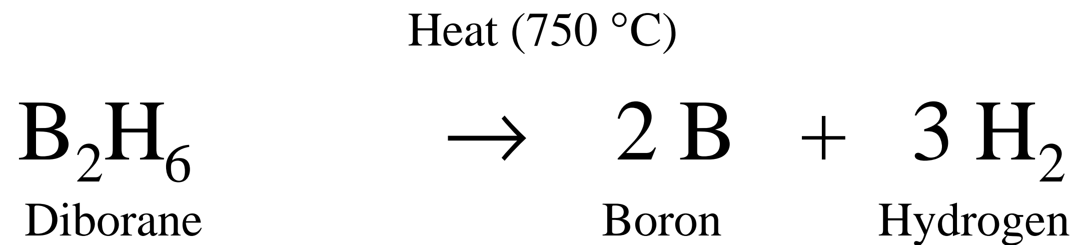
- N-type Dopant





Polysilicon Doping

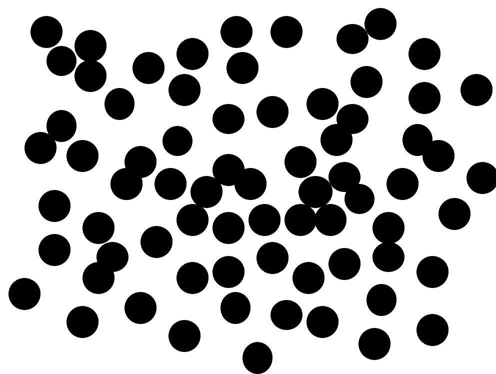
- P-type Dopant



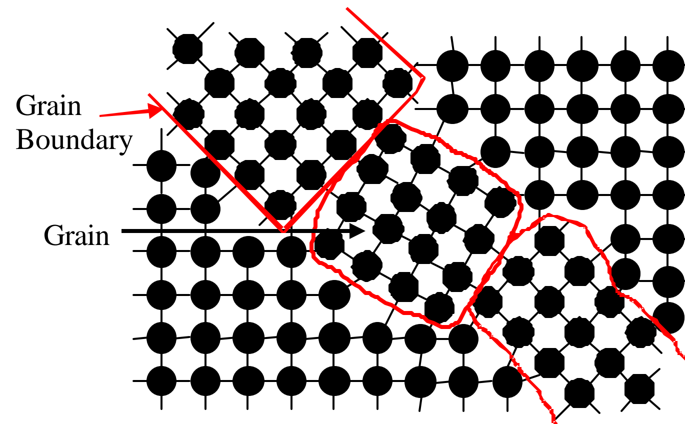
Temperature Relationship of Silane Process

- On single crystal silicon substrate
- Silane as source gases
- T > 900 °C deposit *single crystal silicon*
- 900 °C > T > 550 °C deposit *polysilicon*
- T < 550 °C deposit *amorphous silicon*

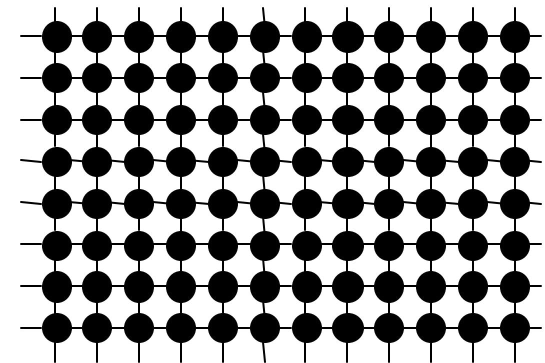
Temperature and Crystal Structure for Silane Processes



T<550 °C
Amorphous Si

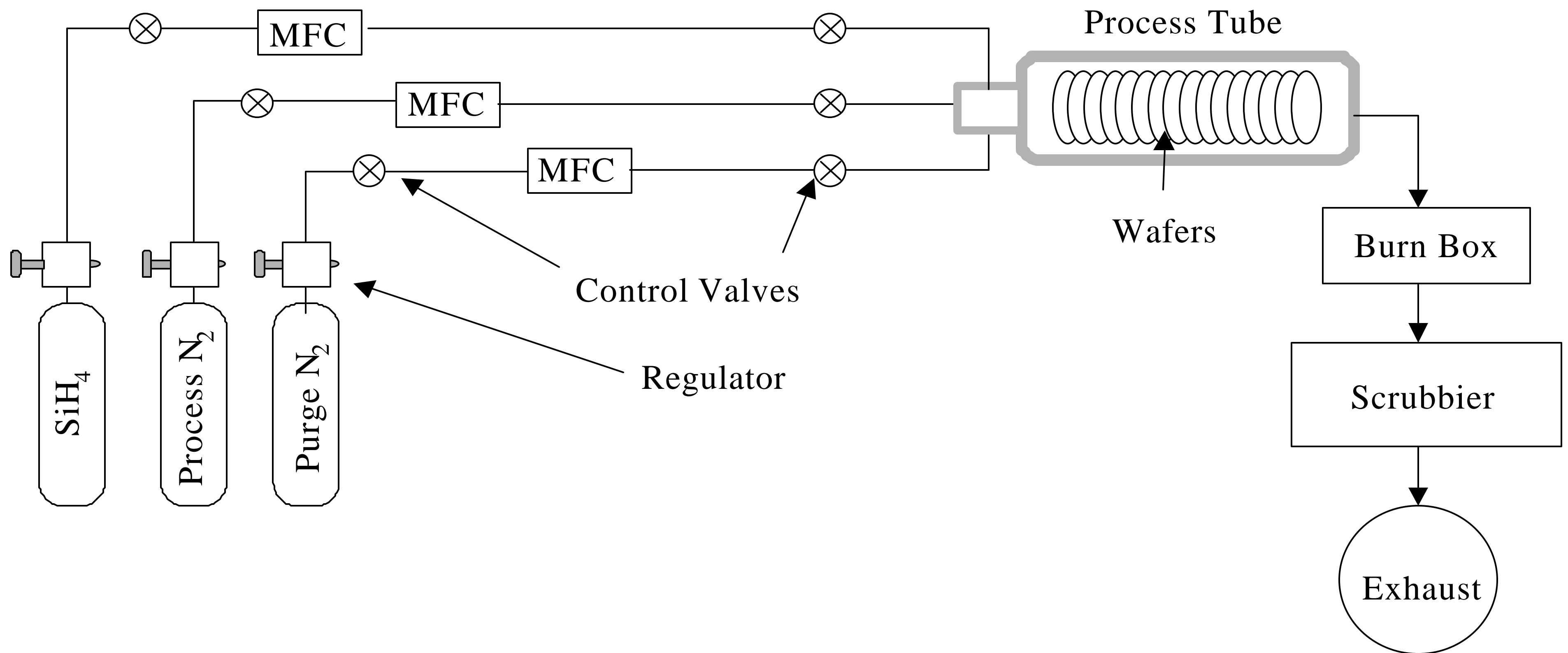


550 °C <T< 900 °C
Polysilicon



T > 900 °C
Single Crystal Si

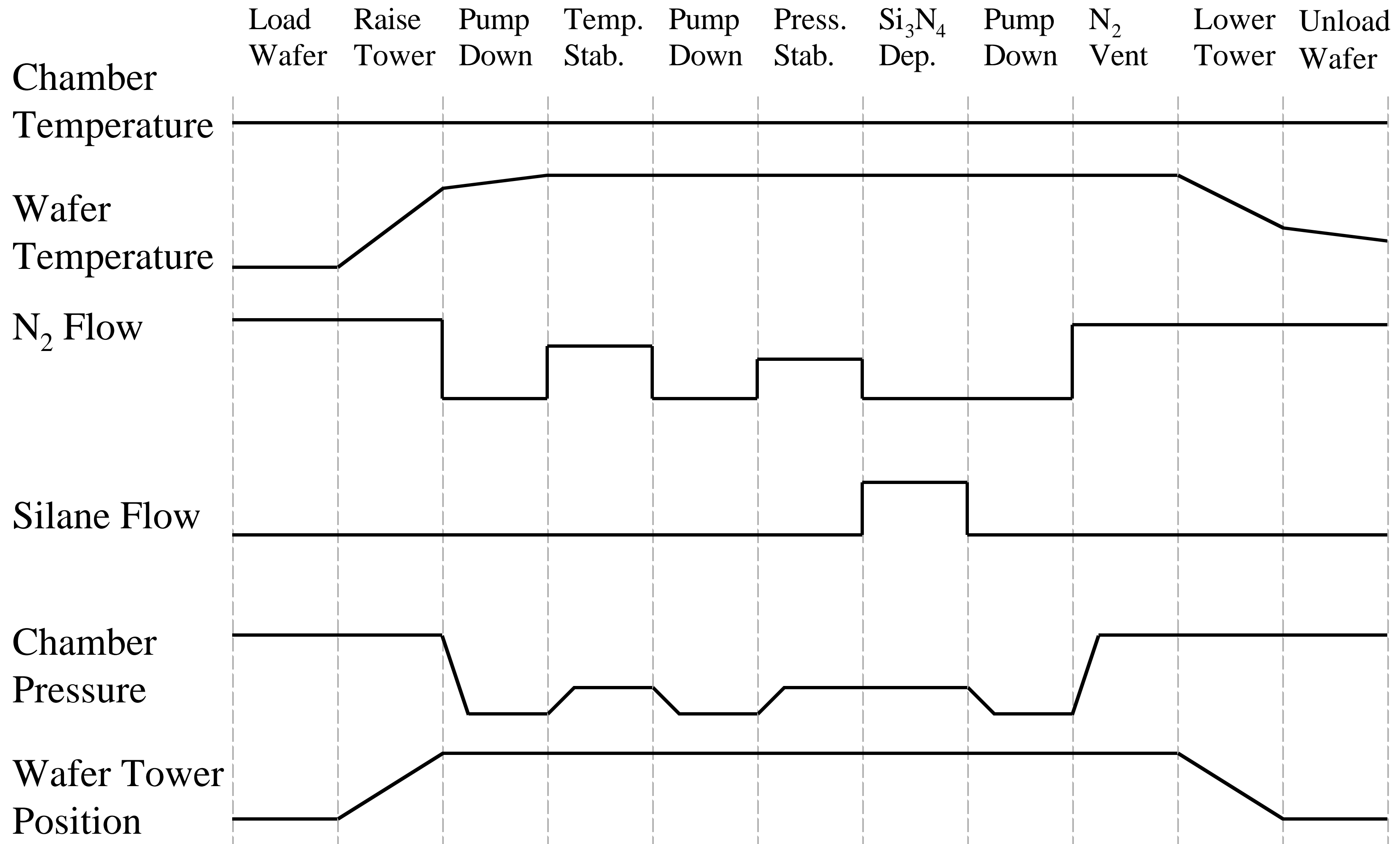
Polysilicon LPCVD System



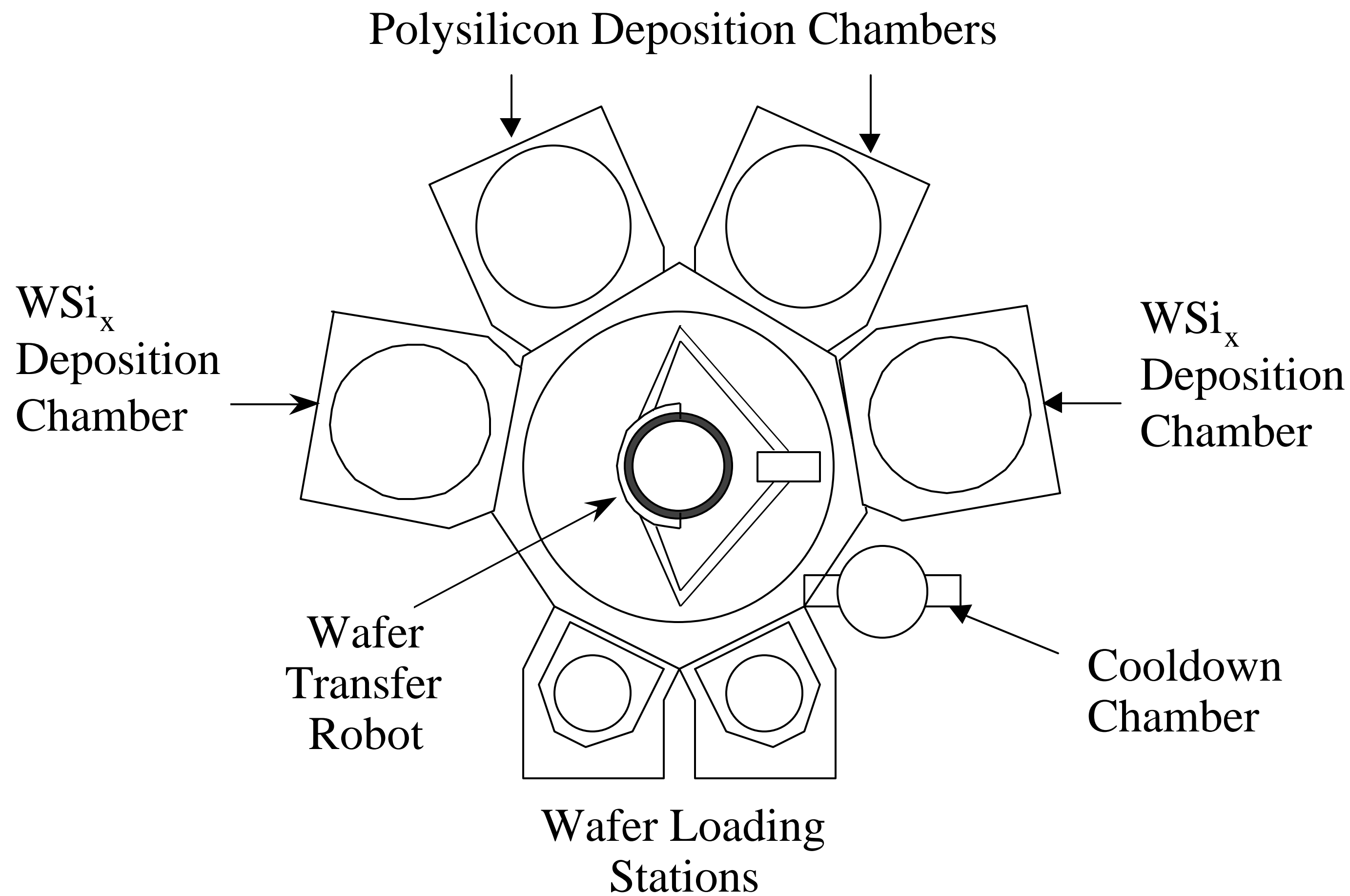
Polysilicon Deposition Process

- Idle with purge N_2 flow
- Idle with process N_2 flow
- Wafer load into tower with process N_2 flow
- Tower raises into process chamber (bell jar) with process N_2 flow
- Pump down chamber to base pressure (< 2 mTorr) by turning-off N_2 flow
- Stabilize wafer temperature with N_2 flow and leak check
- Set up process pressure (~250 mTorr) and with N_2 flow
- Turn-on SiH_4 flow and turn-off N_2, start deposition
- Close gate valve, fill N_2 and ramp-up pressure to atmospheric pressure
- Tower lowed and wafer temperature cooled down, with process N_2 flow
- Unload wafer with process N_2 flow
- Idle with purge N_2 flow

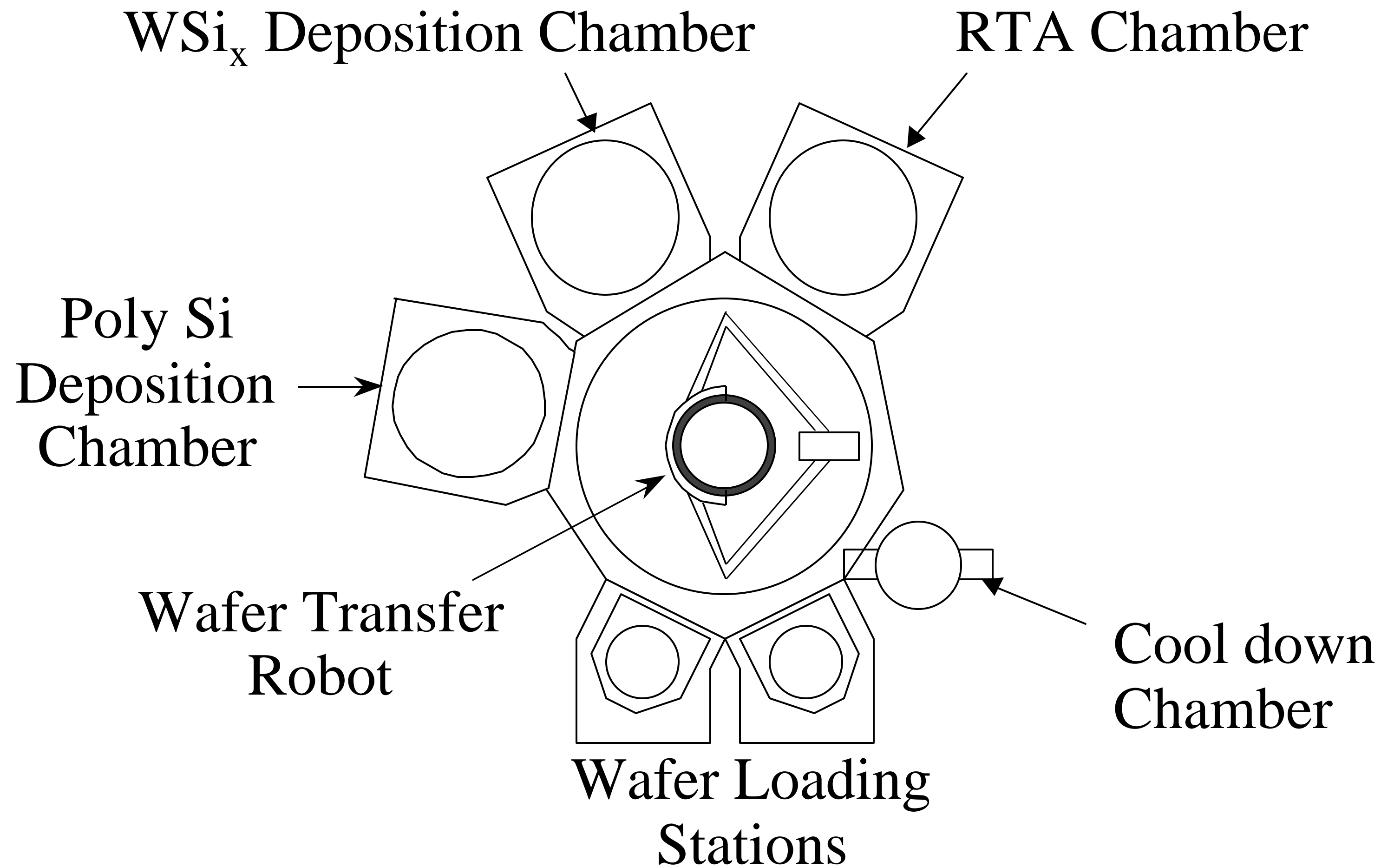
Polysilicon Deposition Process



Polycide Deposition System



Polycide Deposition System



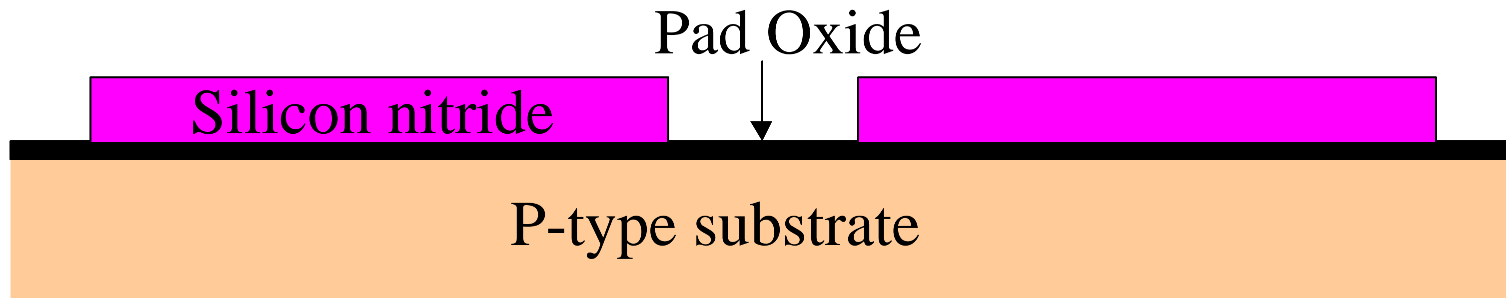
Silicon Nitride

- Dense material
- Widely used as diffusion barrier layer and passivation layer
- LPCVD (front-end) and PECVD (back-end)
- LPCVD nitride usually is deposited in a furnace

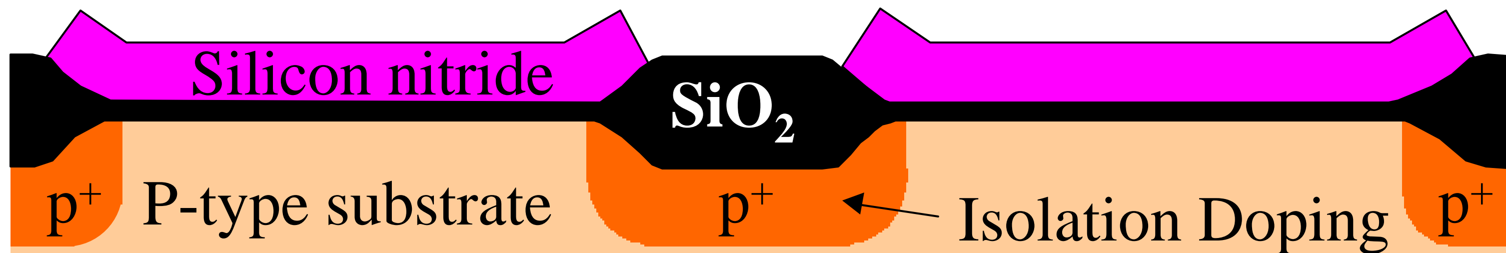
Application of Silicon Nitride

- LOCOS formation as oxygen diffusion barrier
- STI formation as oxide CMP stop
- PMD barrier layer
- Etch stop layer

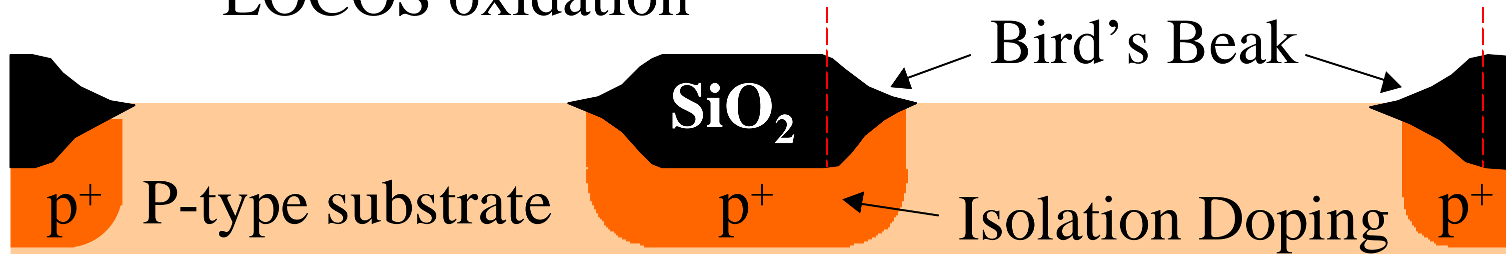
LOCOS Process



Pad oxidation, nitride deposition and patterning

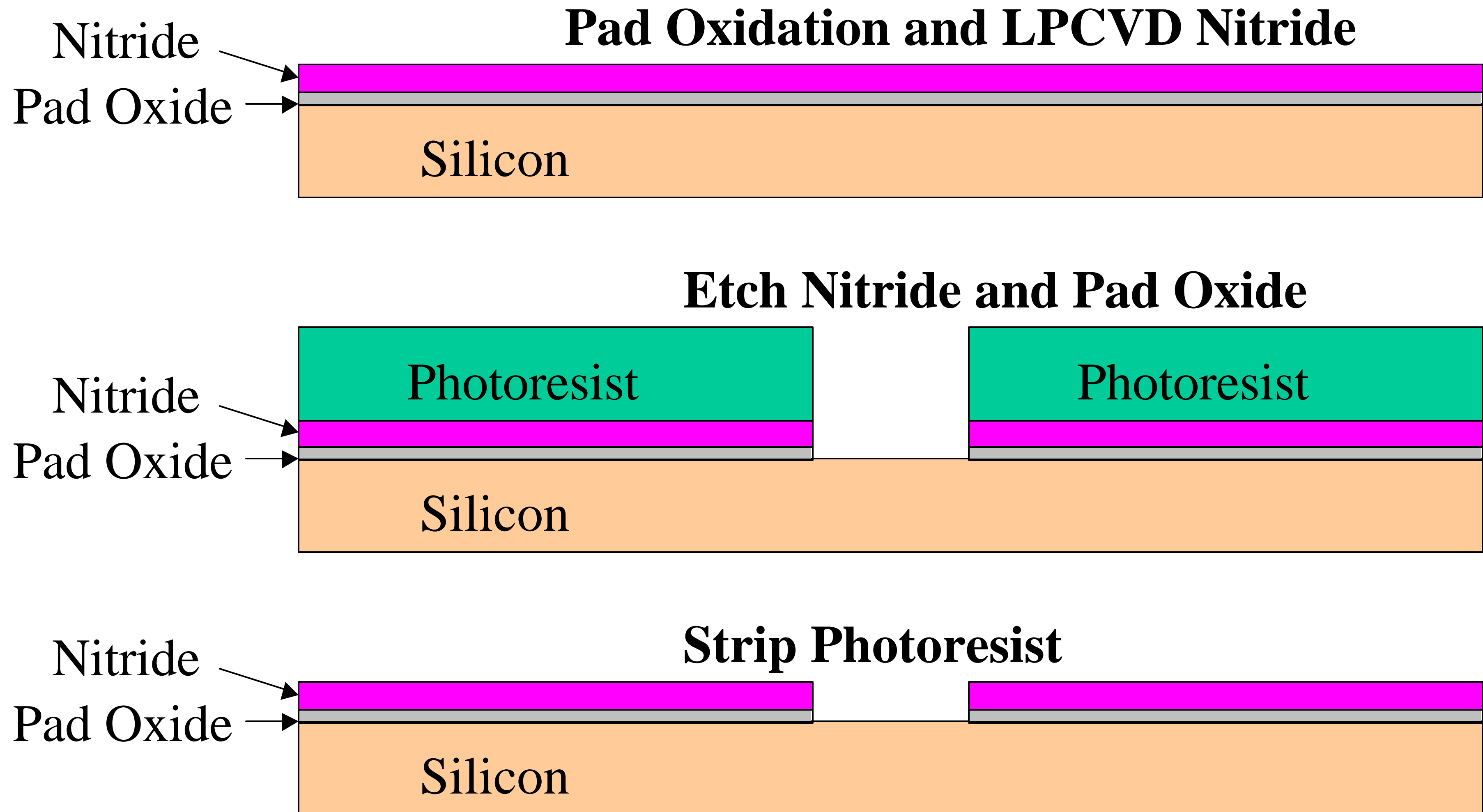


LOCOS oxidation

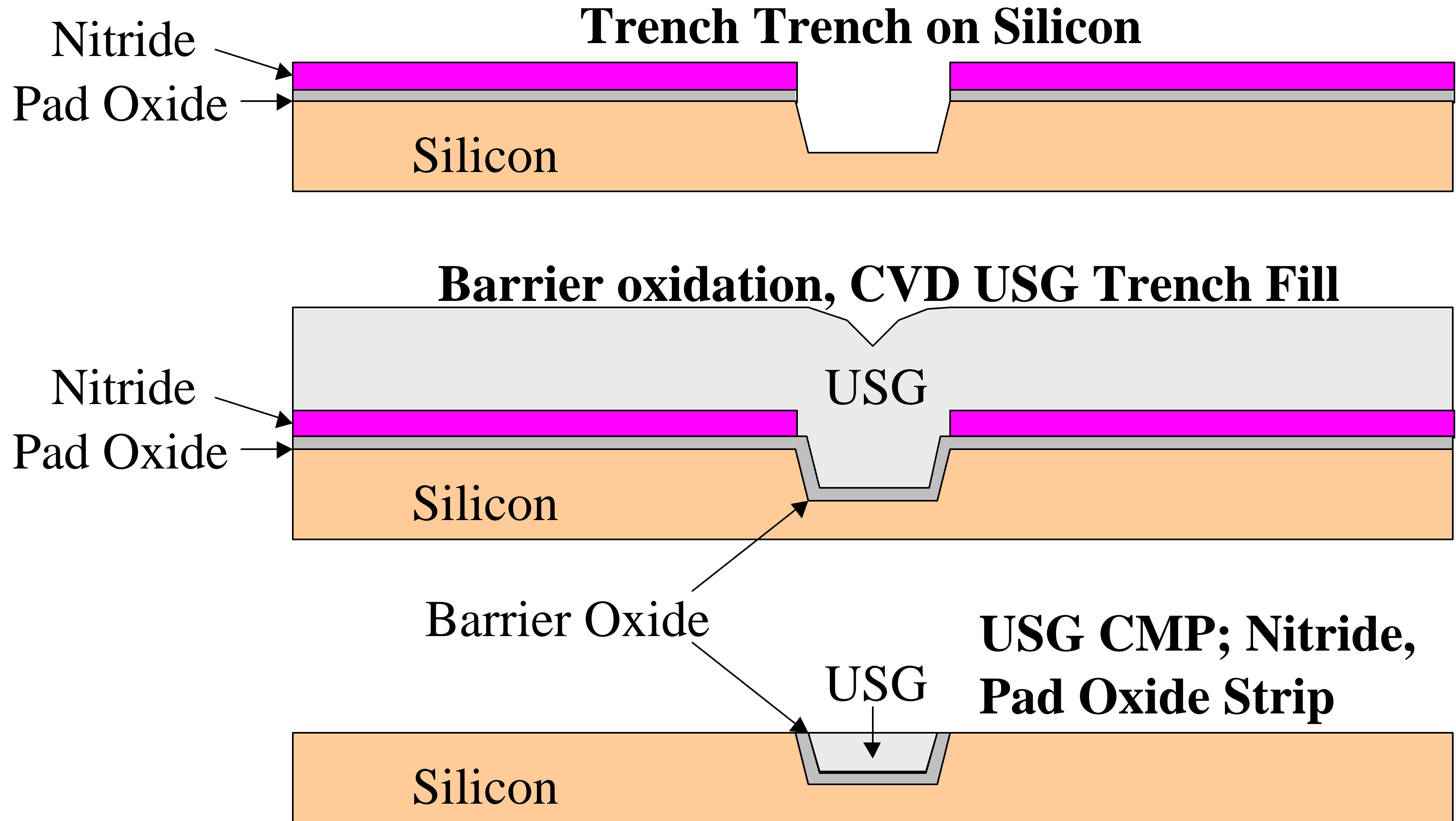


Nitride and pad oxide strip

STI Process



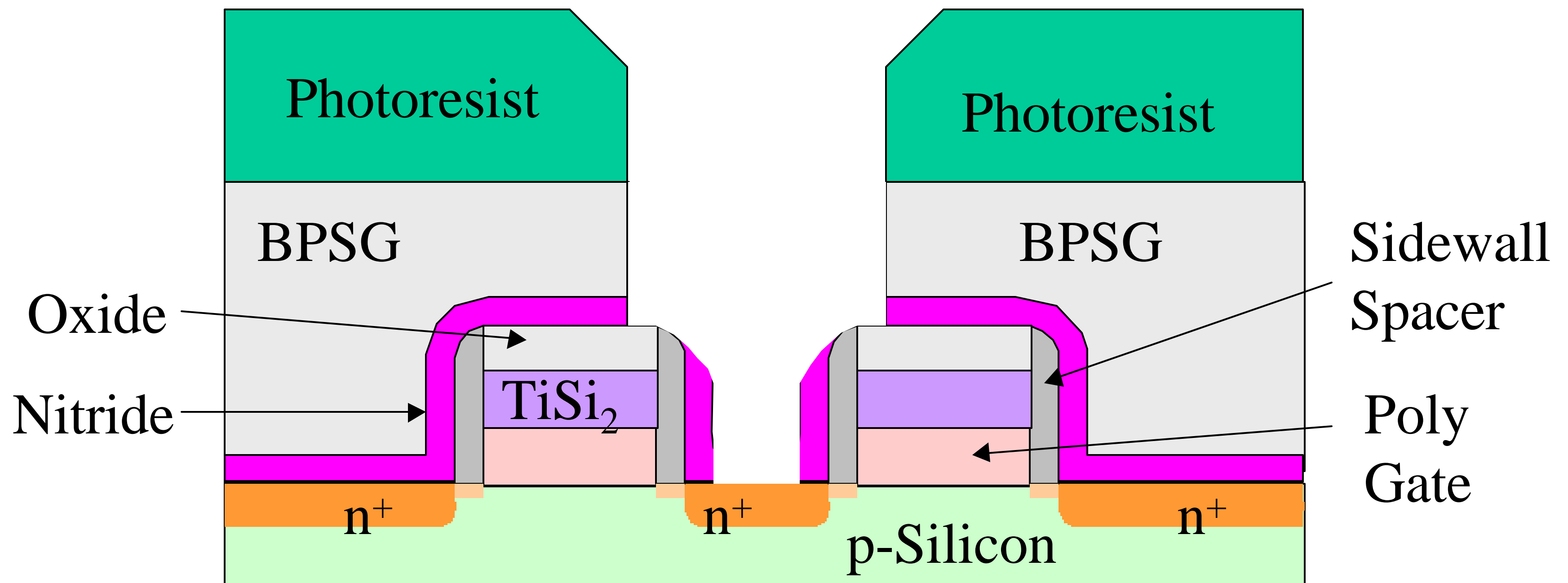
STI Process



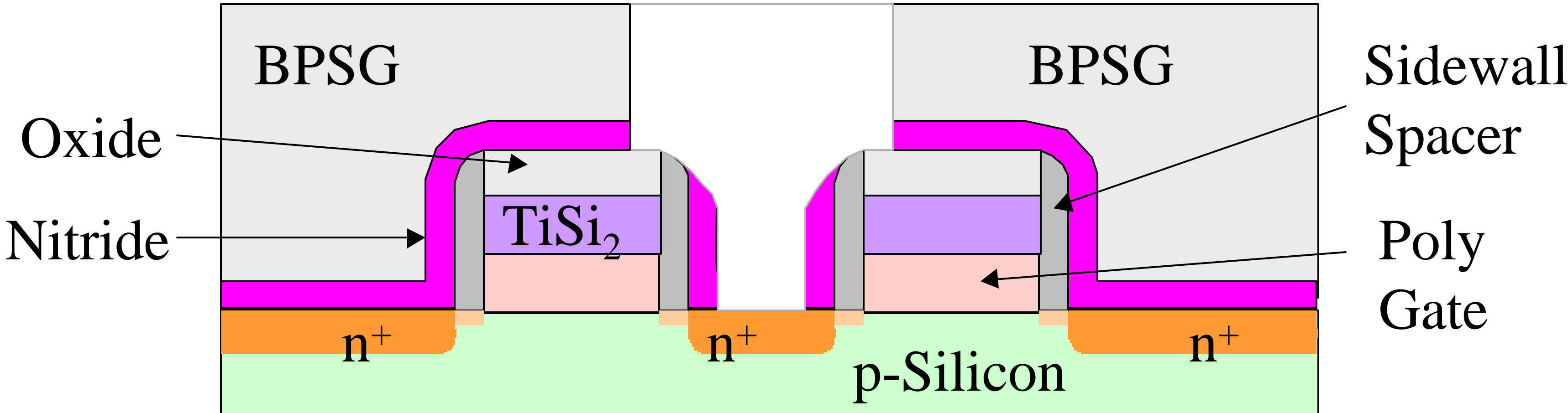
Self-aligned Contact Etch Stop

Photoresist
Photoresist
BPSG
BPSG
Oxide
Nitride
$TiSi_2$
Sidewall Spacer
Poly Gate
n^+
n^+
n^+
p-Silicon

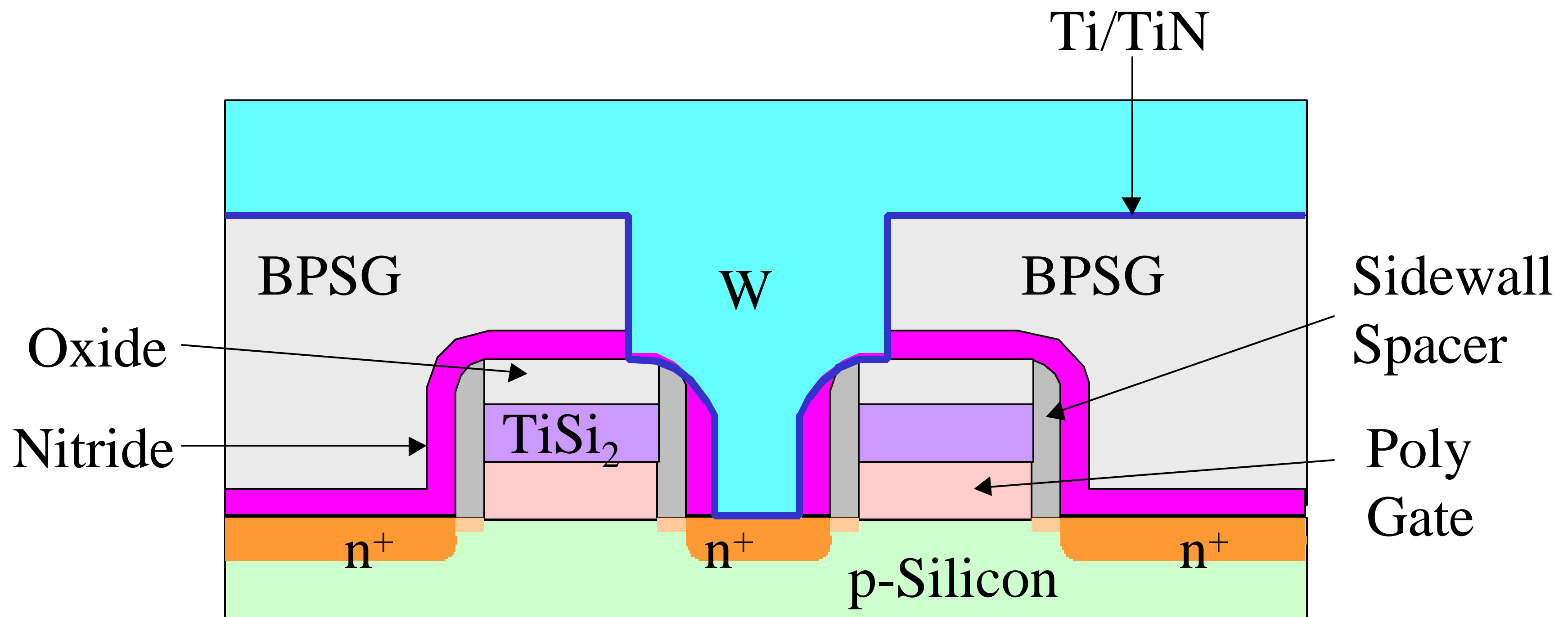
Nitride Breakthrough



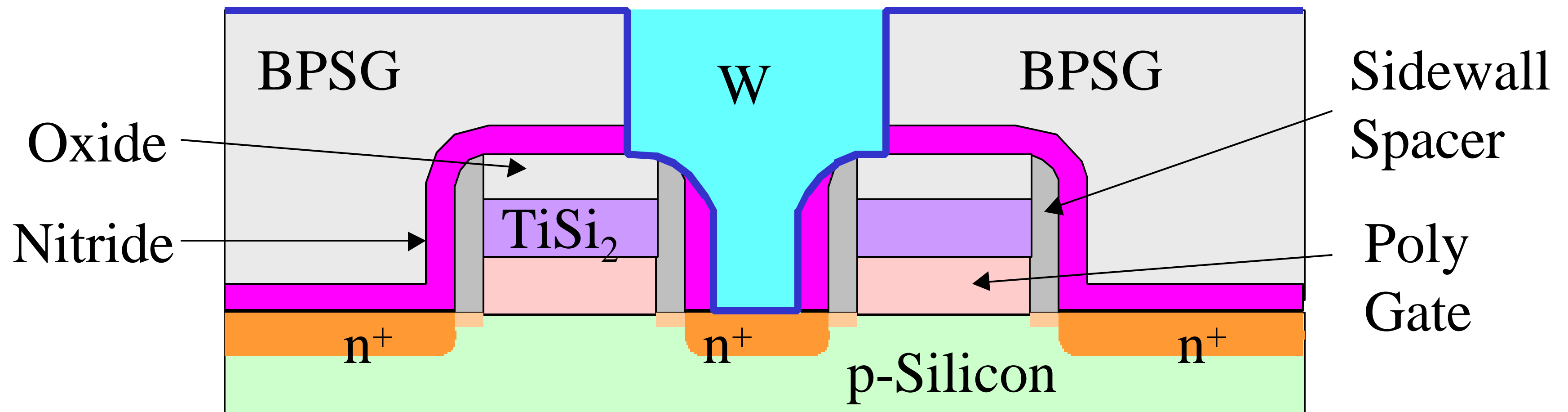
Strip Photoresist



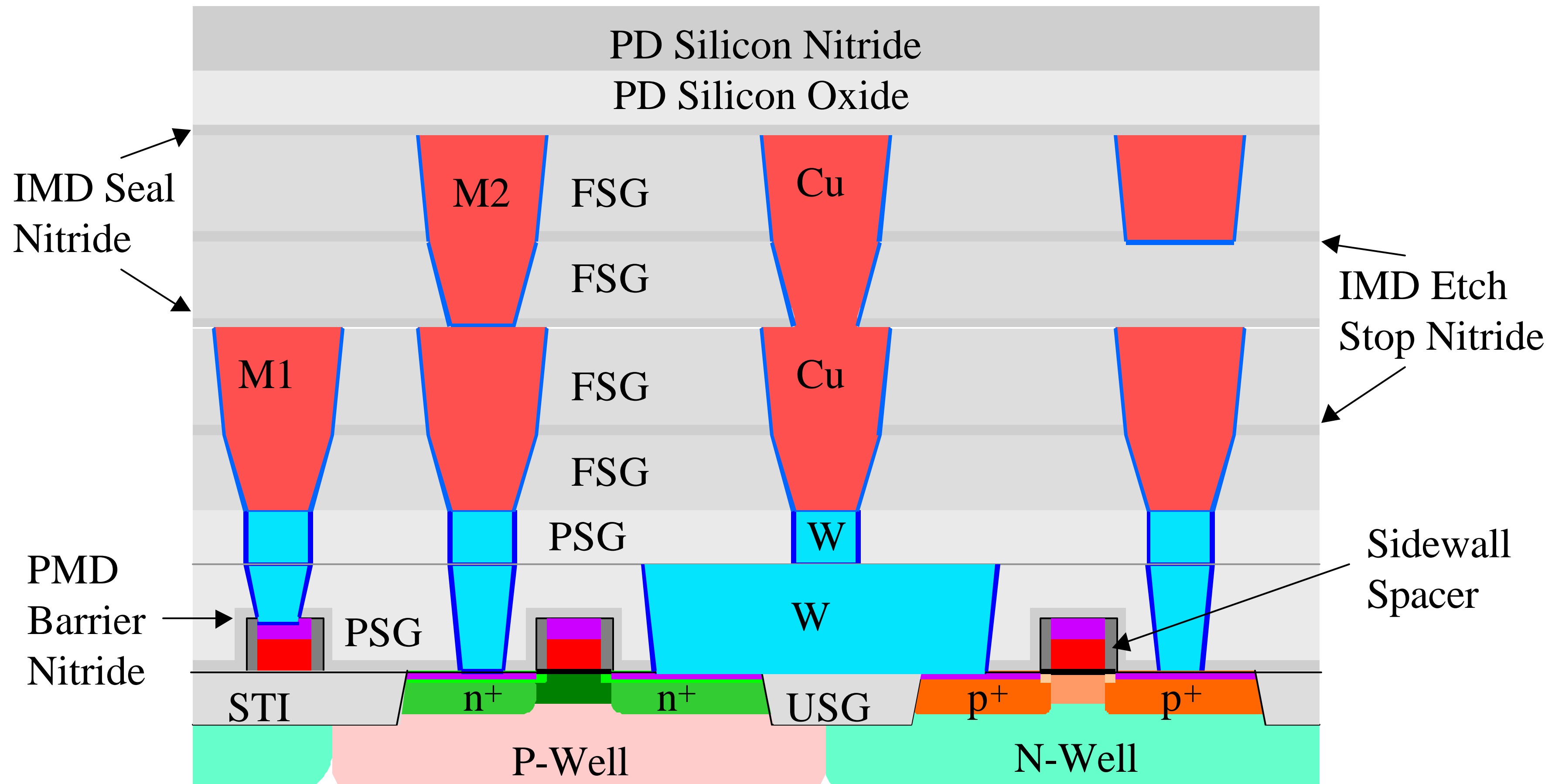
Deposit Ti/TiN and Tungsten



CMP Tungsten and TiN/Ti

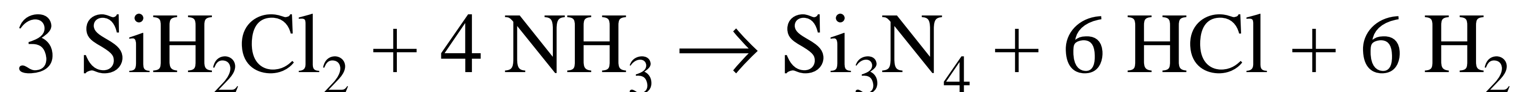


Silicon Nitride Applications



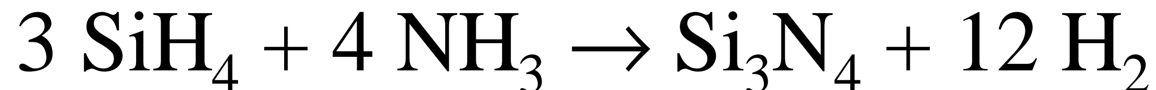
Silicon Nitride Deposition

- Silane or DCS as silicon source
- NH_3 as nitrogen source
- N_2 as purge gas



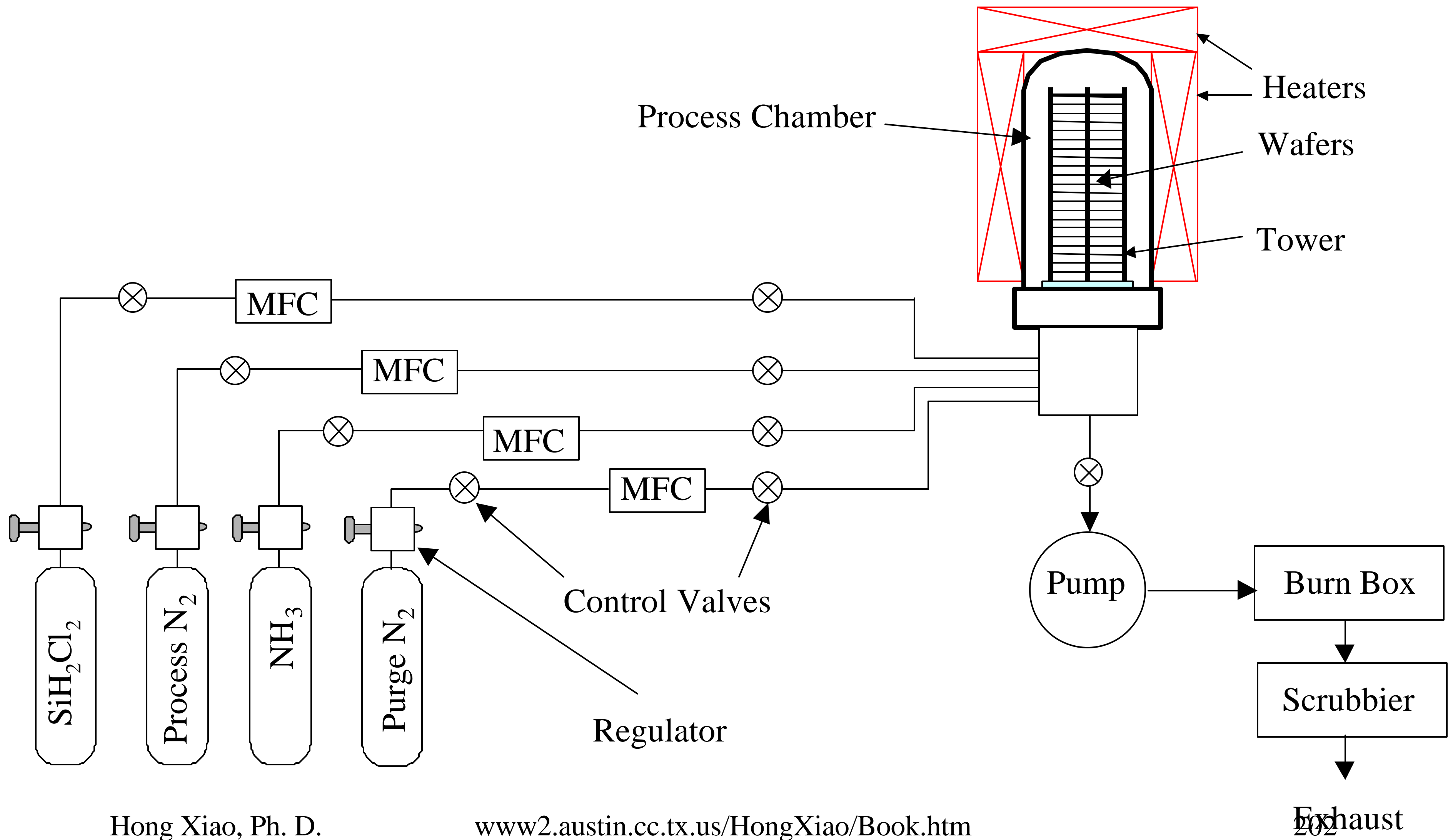
$$3\ SiH_2Cl_2 + 4\ NH_3 \rightarrow Si_3N_4 + 6\ HCl + 6\ H_2$$

or

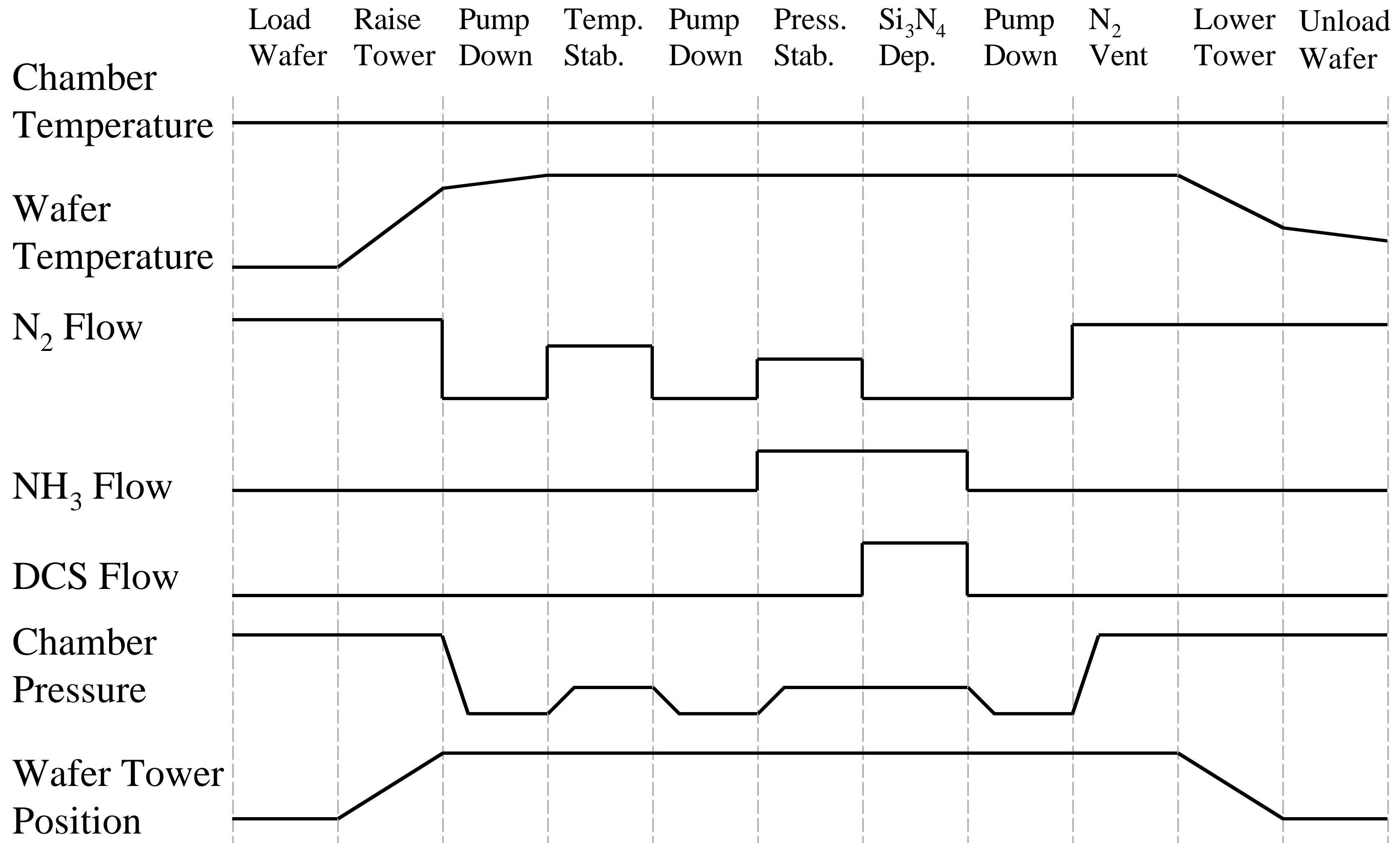


$$3\ SiH_4 + 4\ NH_3 \rightarrow Si_3N_4 + 12\ H_2$$

Silicon Nitride LPCVD System



Nitride Deposition Process Sequence



Future Trends of HT-CVD

- More single wafer rapid thermal CVD
- Integrated processes in cluster tools

Summary of Furnace Deposition

- Polysilicon and silicon nitride are the two most commonly film deposited in high temperature furnace
- Silane and DCS are the two most commonly used silicon sources.
- Polysilicon can be doped while deposition by flowing phosphine, arsine or diborane

Rapid Thermal Process

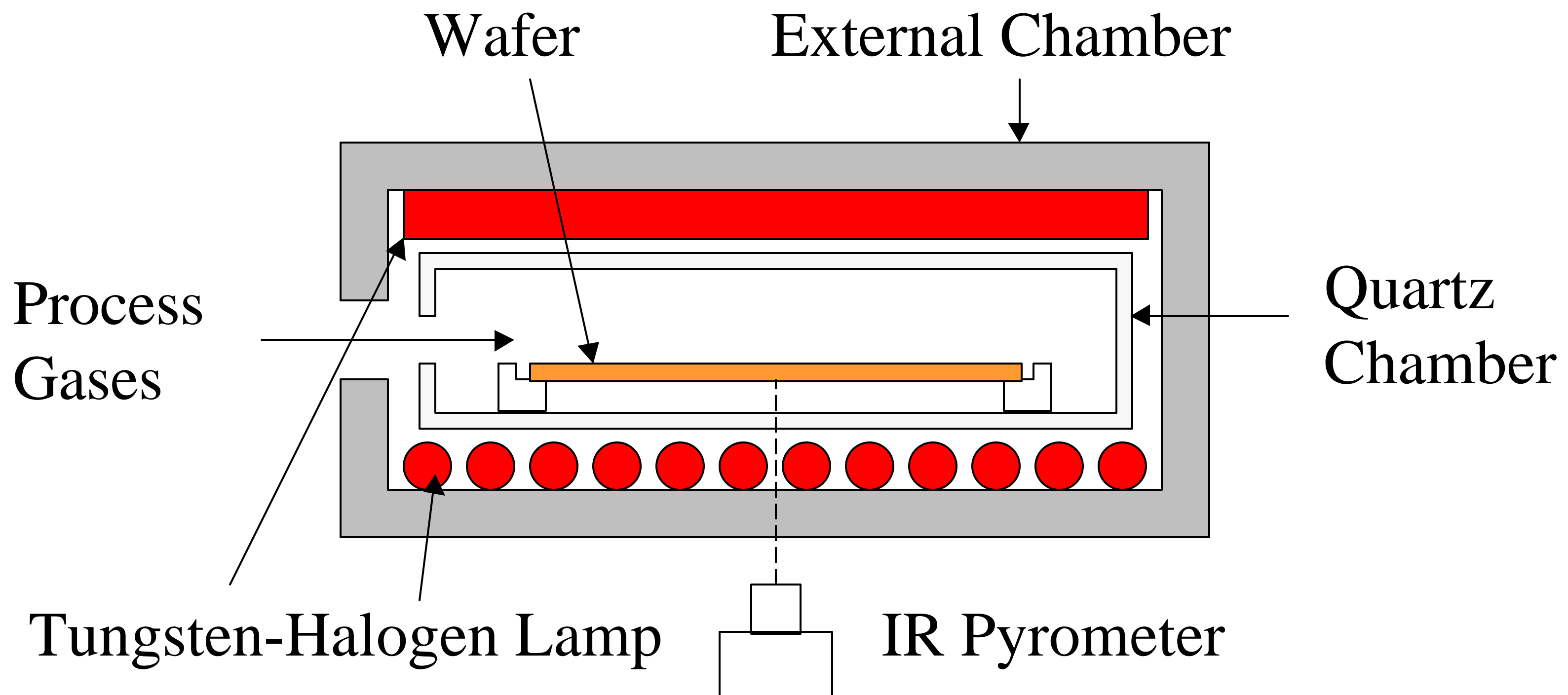
Rapid Thermal Processing (RTP)

- Mainly used for post-implantation rapid thermal anneal (RTA) process.
- Fast temperature ramp-up, 100 to 150 °C/sec compare with 15 °C/min in horizontal furnace.
- Reduce thermal budge and easier process control.

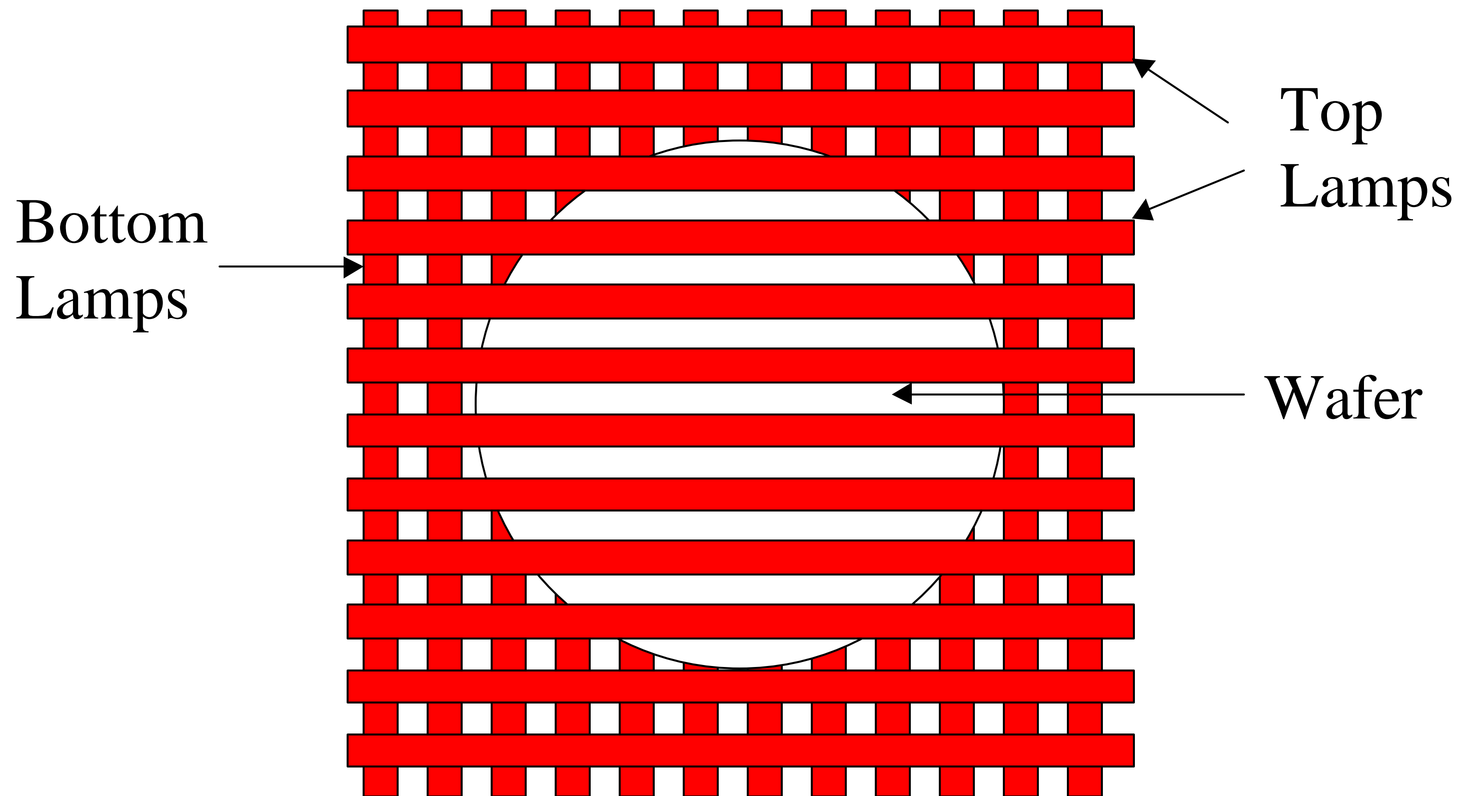
Rapid Thermal Processing (RTP)

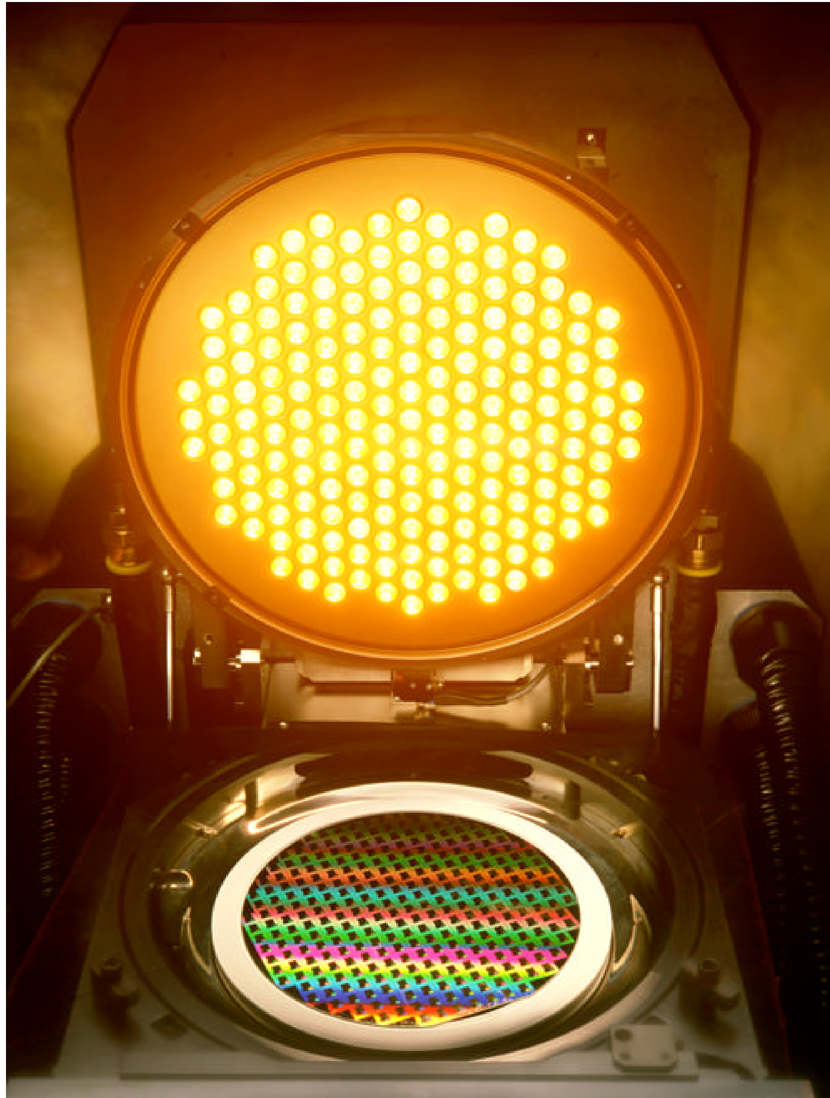
- Single wafer rapid thermal CVD (RTCVD) chamber can be used to deposit polysilicon and silicon nitride.
- RTCVD chamber can be integrated with other process chamber in a cluster tool for in-line process.
- Thin oxide layer (< 40 Å) is likely to be grown with RTO for WTW uniformity control.

Schematic of RTP Chamber



Lamp Array





RTP Chamber

Photo courtesy of Applied Materials, Inc

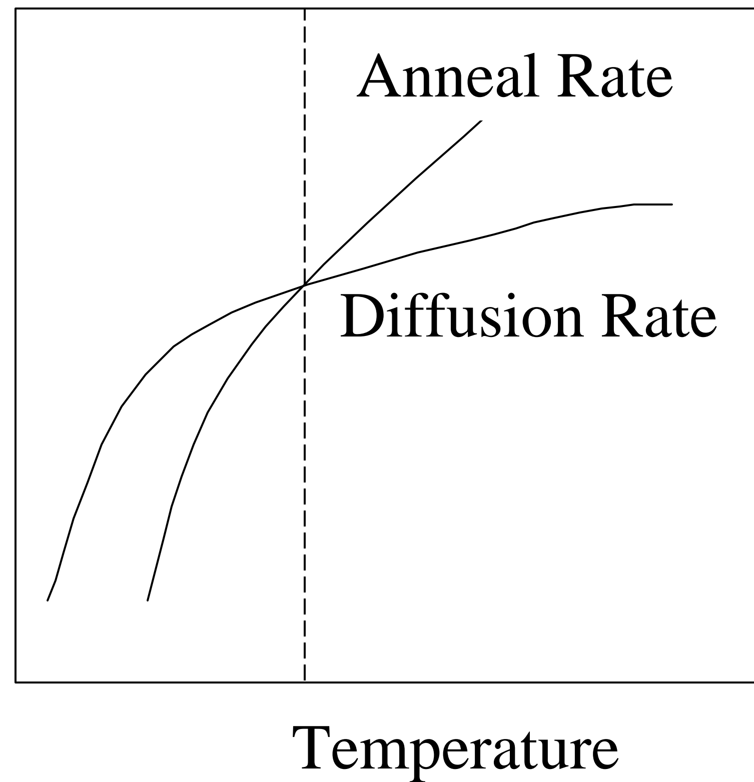
Annealing and Dopant Diffusion

- At higher temperature >1100 °C anneal is faster than diffusion
- Post implantation prefer high temperature and high temperature ramp rate.
- Single wafer rapid thermal process tool has been developed initially for this application

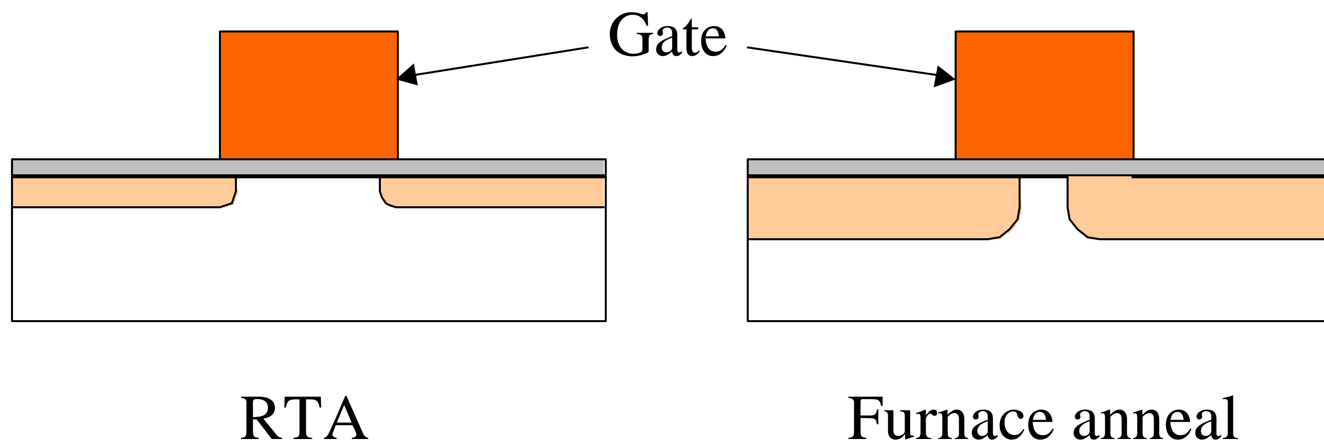
Annealing and Dopant Diffusion

- Dopant atoms diffuse at high temperature
- Furnace has low temperature ramp rate (~10 °C/min) due to large thermal capacity
- Furnace annealing is a long process which causes more dopant diffusion
- Wafer at one end gets more anneal than wafer at another end

Anneal Rate and Diffusion Rate



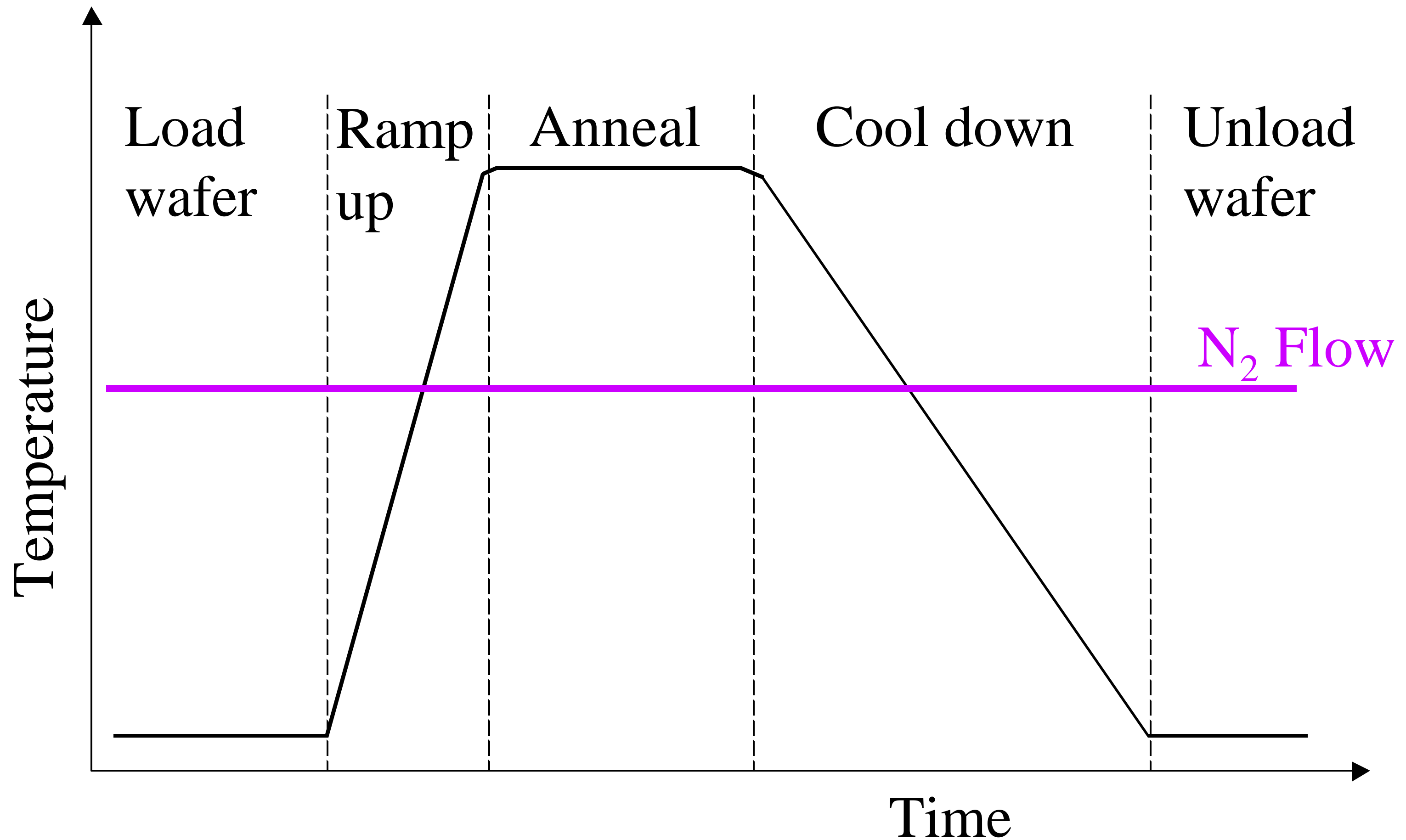
Dopant Diffusion After Anneal



Advantage of RTP over Furnace

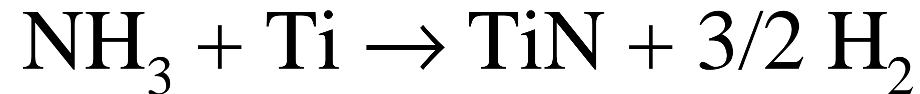
- Much faster ramp rate (75 to 150 °C/sec)
- Higher temperature (up to 1200 °C)
- Faster process
- Minimize the dopant diffusion
- Better control of thermal budget
- Better wafer to wafer uniformity control

RTP Temperature Change



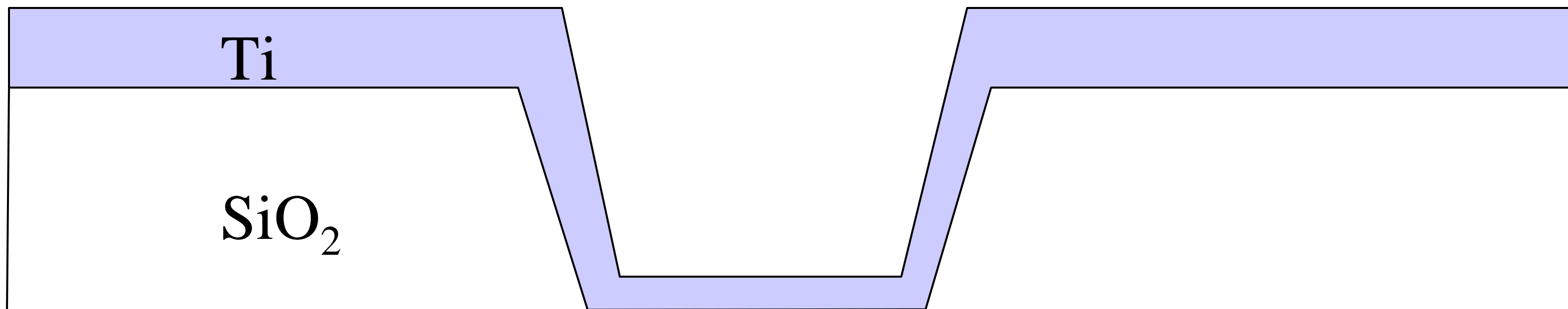
Thermal Nitridization

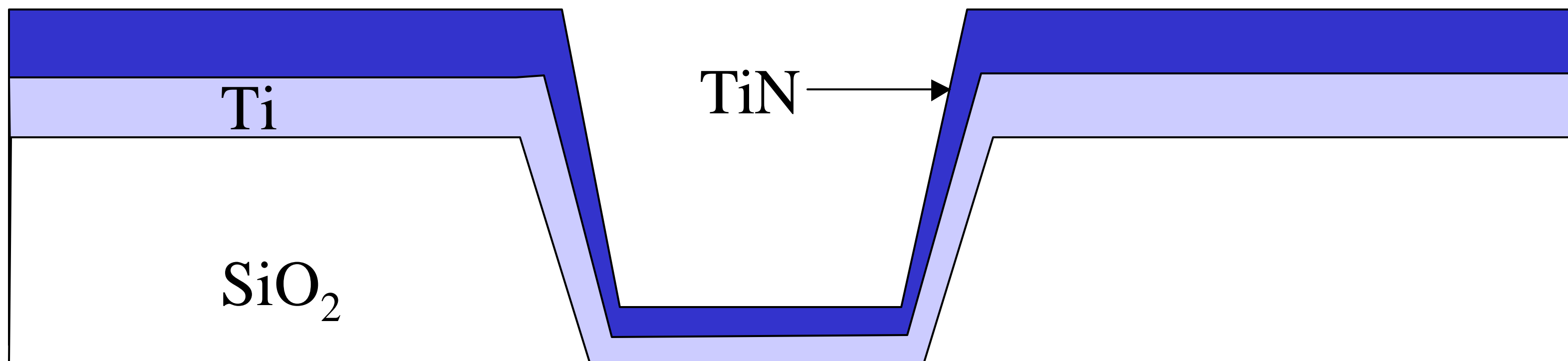
- Titanium PVD
- Thermal nitridization with NH_3



$$NH_3 + Ti \rightarrow TiN + 3/2\ H_2$$

Titanium Nitridization

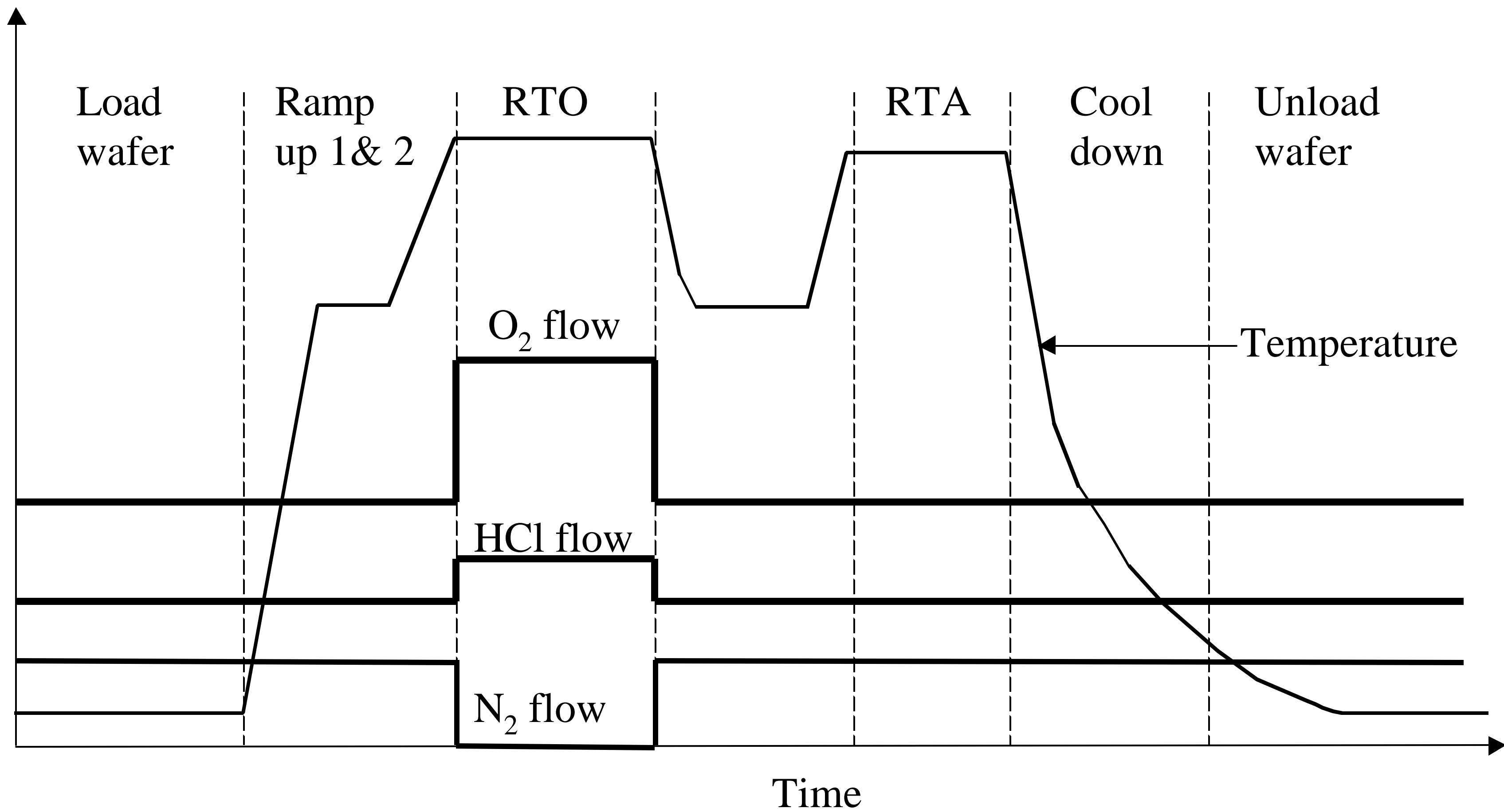




RTO Process

- Ultra thin silicon dioxide layer < 30Å
- Better WTW uniformity
- Better thermal budget control

RTP Process Diagram

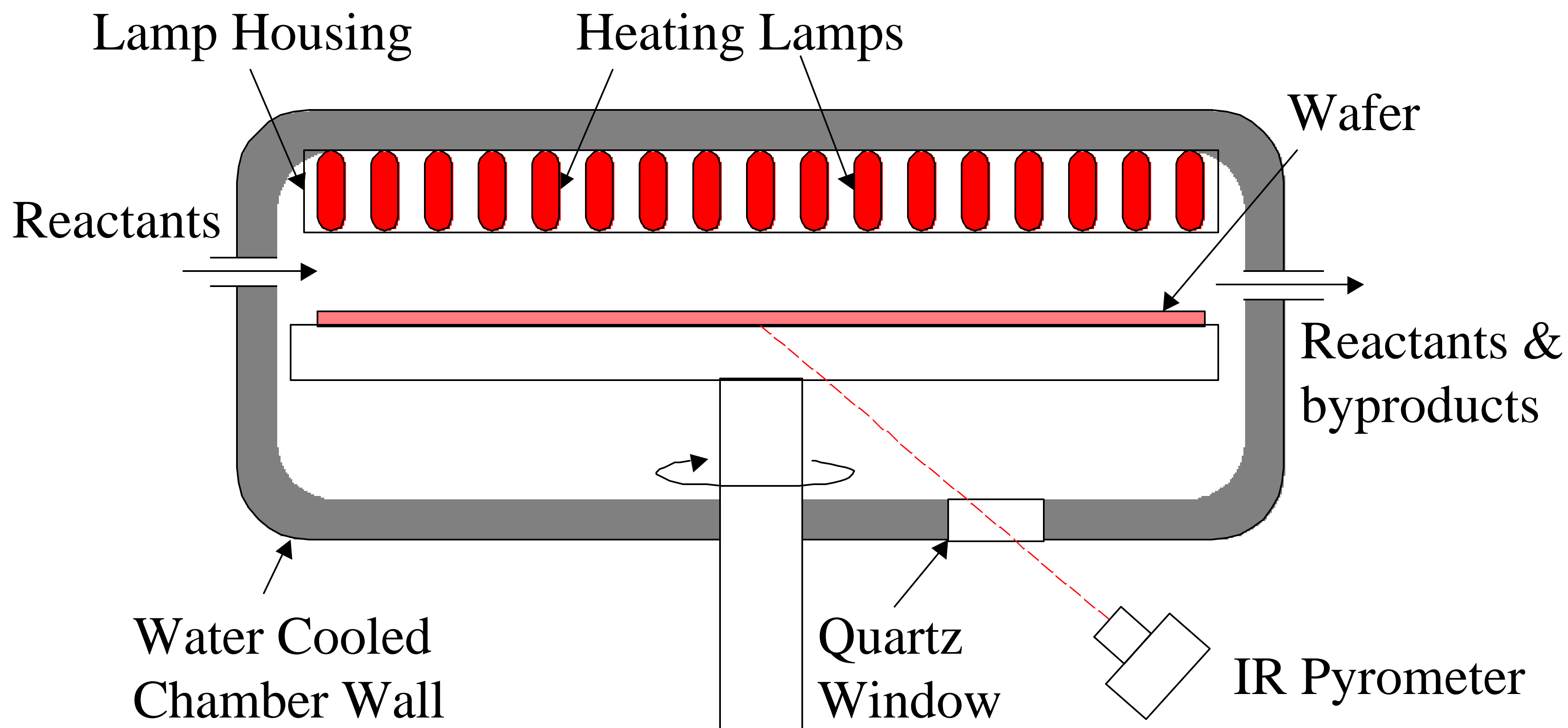


Future Tends

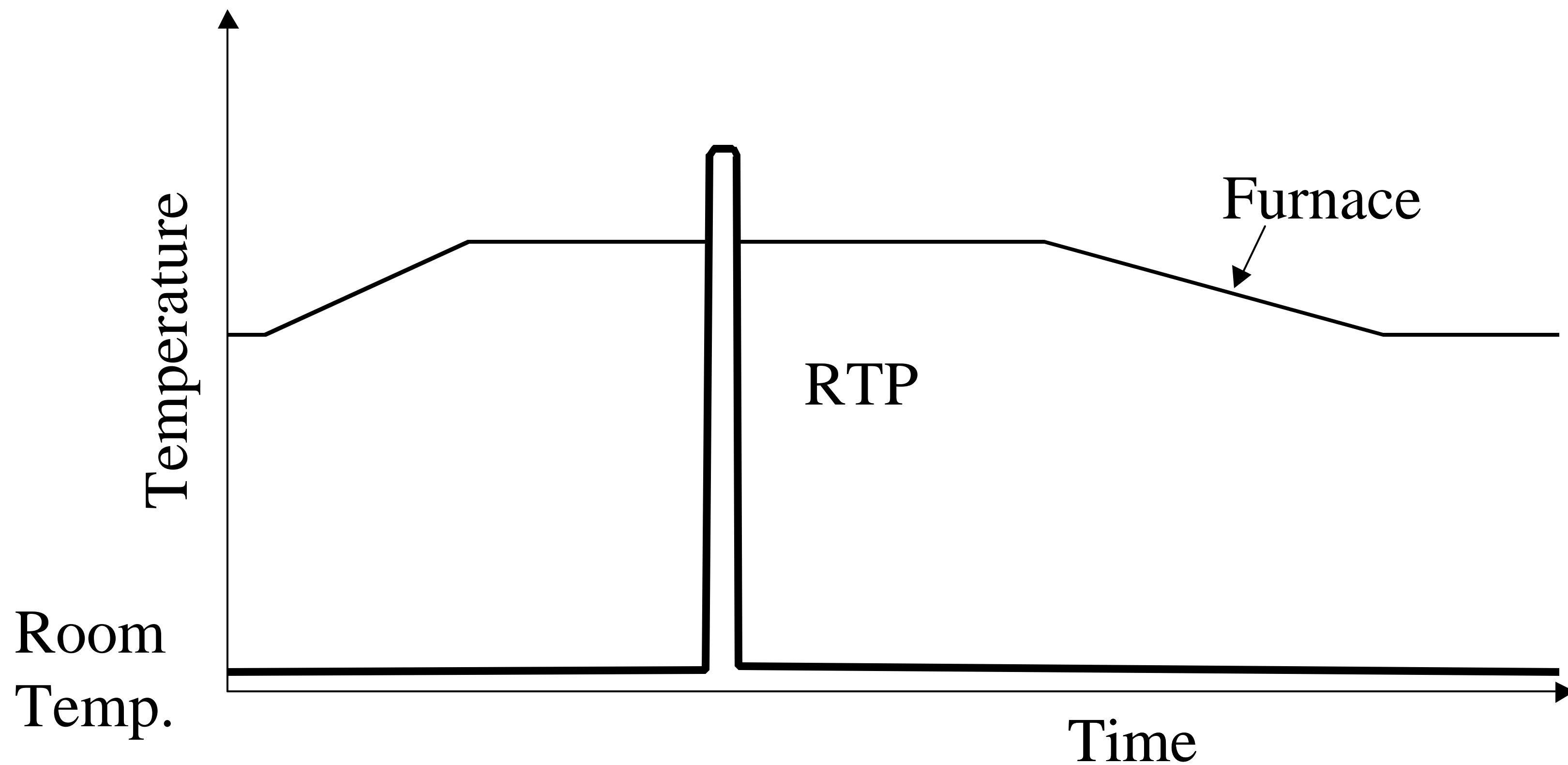
- Rapid thermal process (RTP)
- In-situ process monitoring
- Cluster tools

- Furnace will still be used

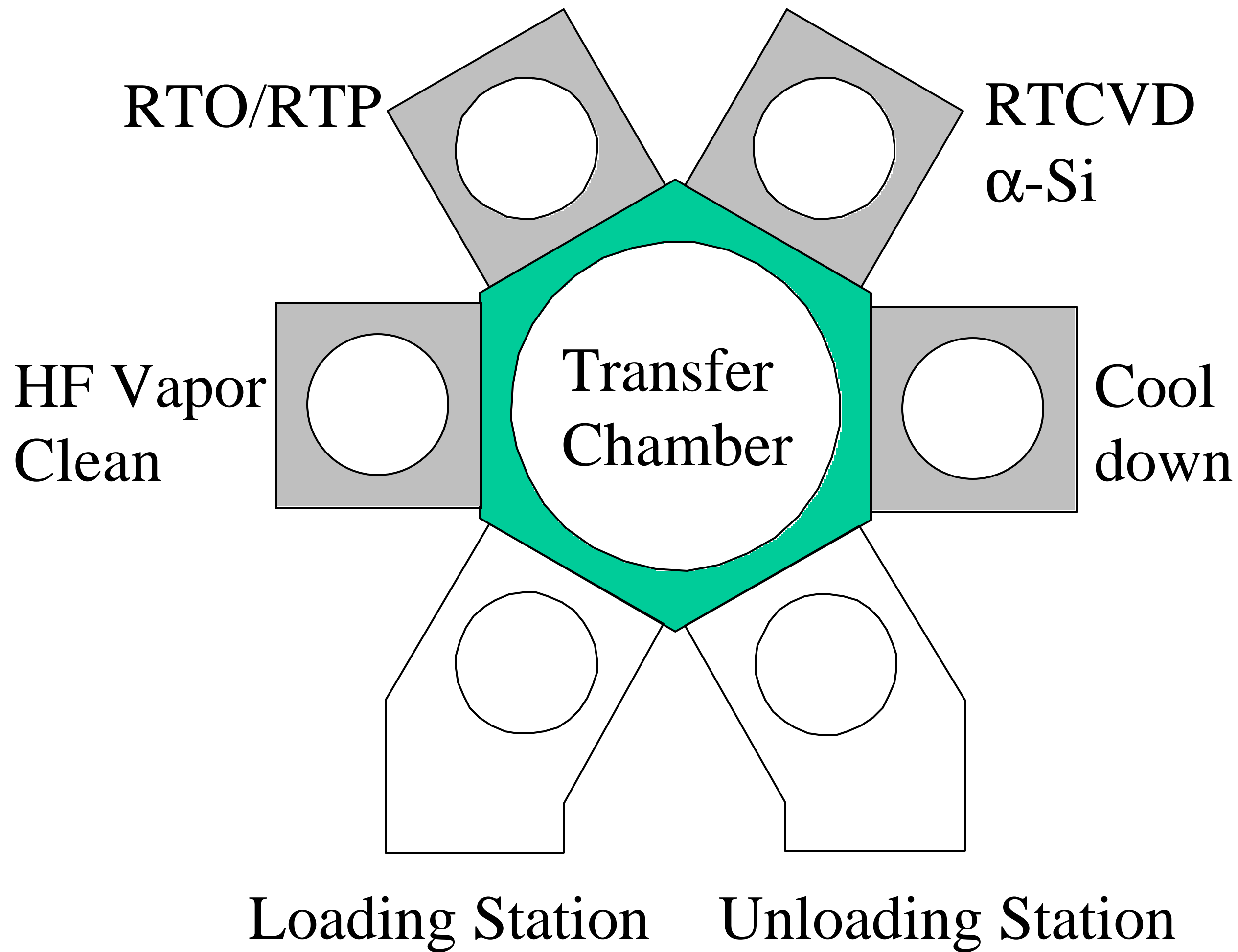
RTCVD Chamber



Temperature of RTP & Furnace



Cluster Tool



Summary of RTP

- Fast
- Better process control
  - Thermal budget
  - Wafer to wafer uniformity
- Minimized dopant diffusion
- Cluster tool, easy process integration

Summary of Thermal Process

- Oxidation, diffusion, annealing, and deposition
- Wet oxidation is faster, dry oxidation has better film quality. Advanced fab: mainly dry oxidation.
- Diffusion doping with oxide mask, used in lab
- LPCVD polysilicon and front-end silicon nitride
- Annealing recovers crystal and activates dopants
- RTP: better control, faster and less diffusion
- Furnaces: high throughput and low cost, will continue to be used in the future fabs

Chapter 6
Photolithography

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www2.austin.cc.tx.us/HongXiao/Book.htm

Objectives

- List the four components of the photoresist
- Describe the difference between +PR and −PR
- Describe a photolithography process sequence
- List four alignment and exposure systems
- Describe the wafer movement in a track-stepper integrated system.
- Explain relationships of resolution and depth of focus to wavelength and numerical aperture.

Introduction

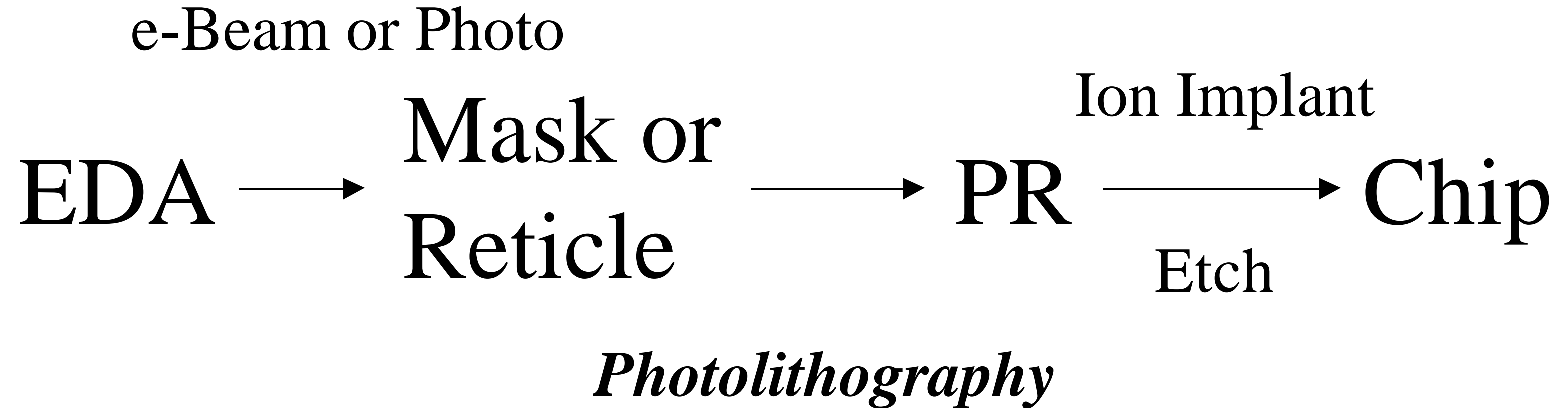
Photolithography

- Temporarily coat photoresist on wafer
- Transfers designed pattern to photoresist
- Most important process in IC fabrication
- 40 to 50% total wafer process time
- Determines the minimum feature size

Applications of Photolithography

- Main application: IC patterning process
- Other applications: Printed electronic board, nameplate, printer plate, and *et al*.

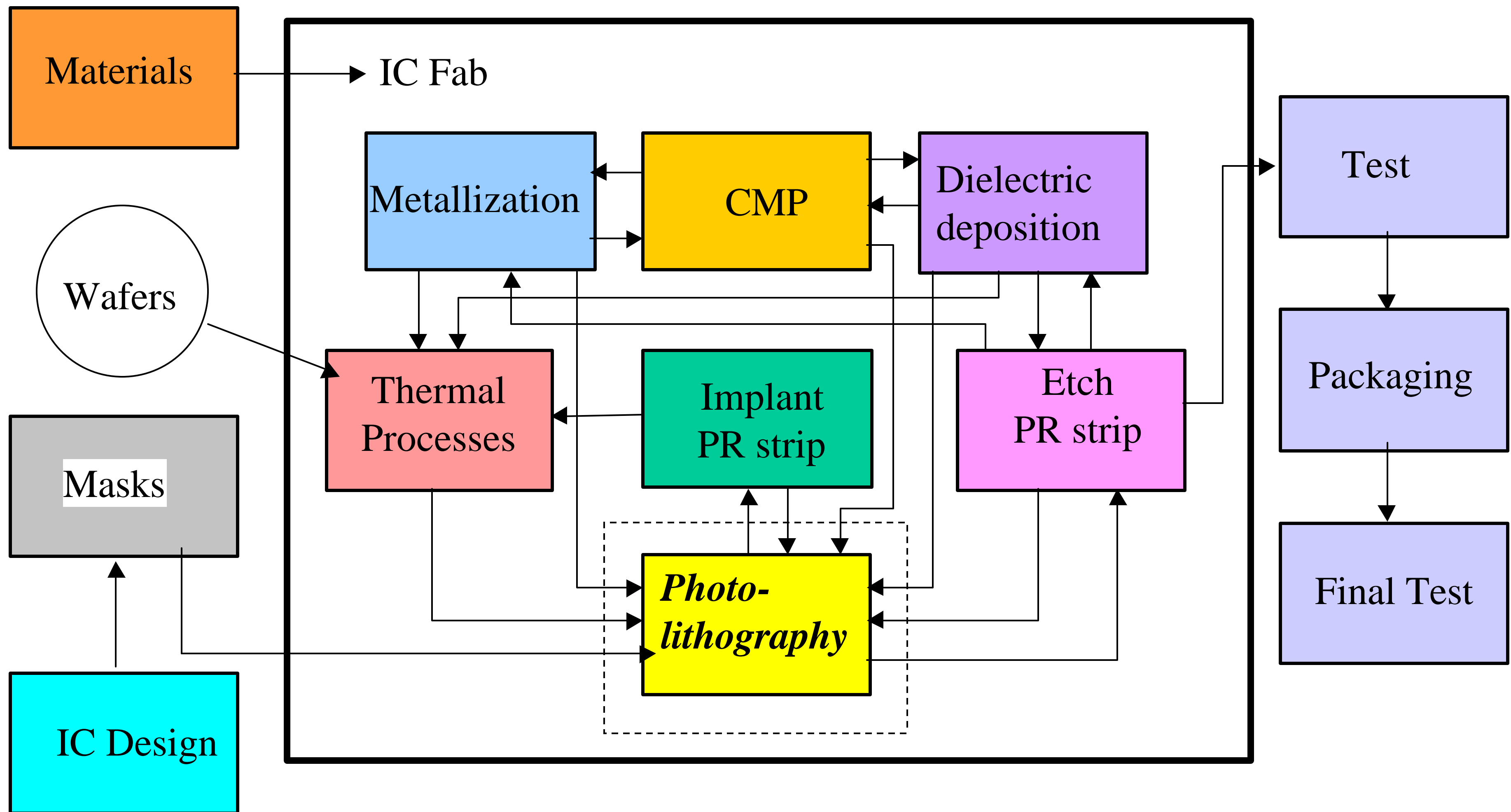
IC Fabrication



EDA: Electronic Design Automation

PR: Photoresist

IC Processing Flow



Photolithography Requirements

- High Resolution
- High PR Sensitivity
- Precision Alignment
- Precise Process Parameters Control
- Low Defect Density

Photoresist

- Photo sensitive material
- Temporarily coated on wafer surface
- Transfer design image on it through exposure
- Very similar to the photo sensitive coating on the film for camera

Photoresist

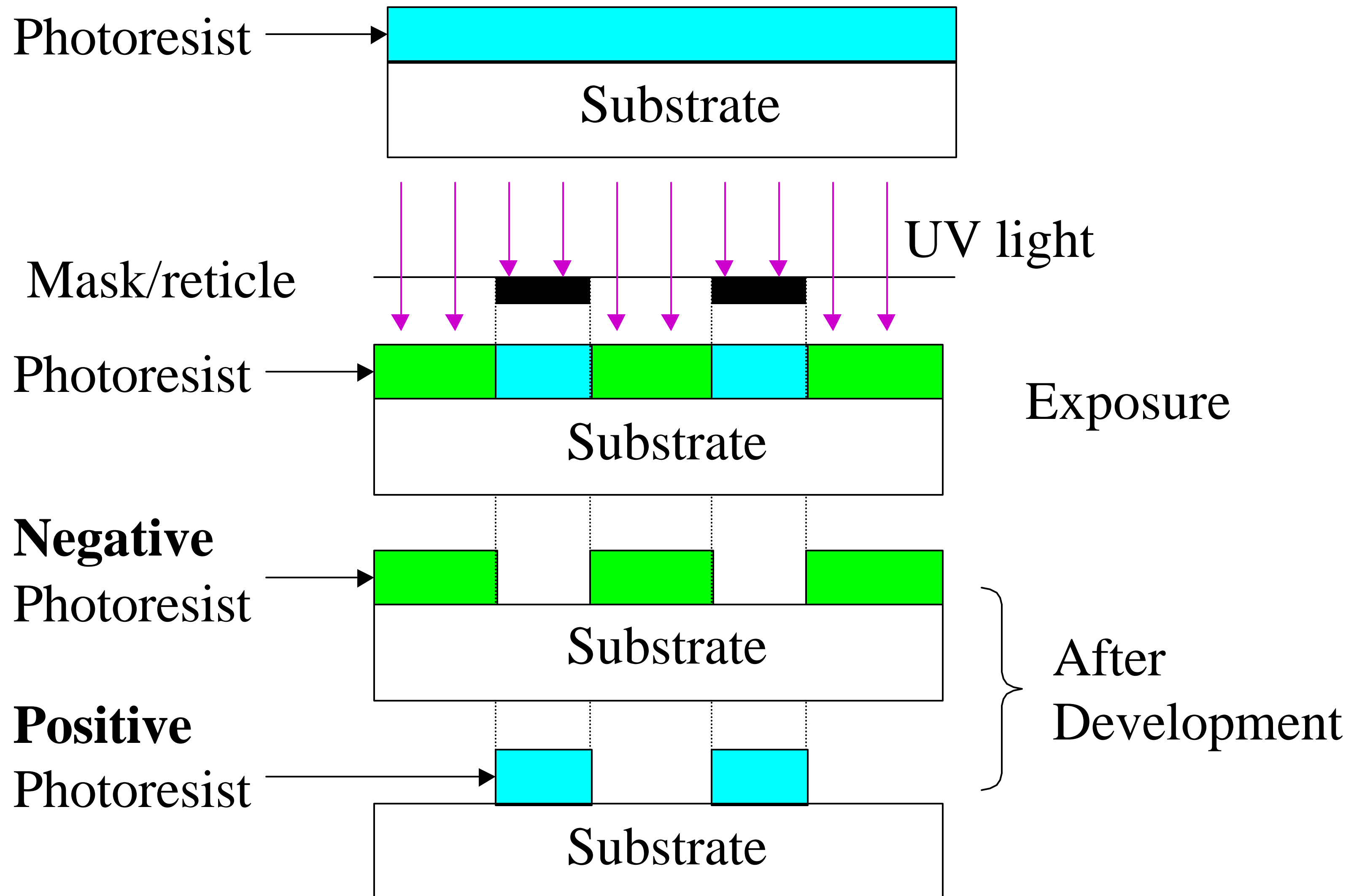
Negative Photoresist

- Becomes insoluble after exposure
- When developed, the unexposed parts dissolved.
- Cheaper

Positive Photoresist

- Becomes soluble after exposure
- When developed, the exposed parts dissolved
- Better resolution

Negative and Positive Photoresists



Photoresist Chemistry

- Start with printed circuit
- Adapted in 1950 in semiconductor industry
- Critical to the patterning process
- Negative and positive photoresist

Photoresist Composition

- Polymer
- Solvents
- Sensitizers
- Additives

Polymer

- Solid organic material
- Transfers designed pattern to wafer surface
- Changes solubility due to photochemical reaction when exposed to UV light.
- Positive PR: from insoluble to soluble
- Negative PR: from soluble to insoluble

Solvent

- Dissolves polymers into liquid
- Allow application of thin PR layers by spinning.

Sensitizers

- Controls and/or modifies photochemical reaction of resist during exposure.
- Determines exposure time and intensity

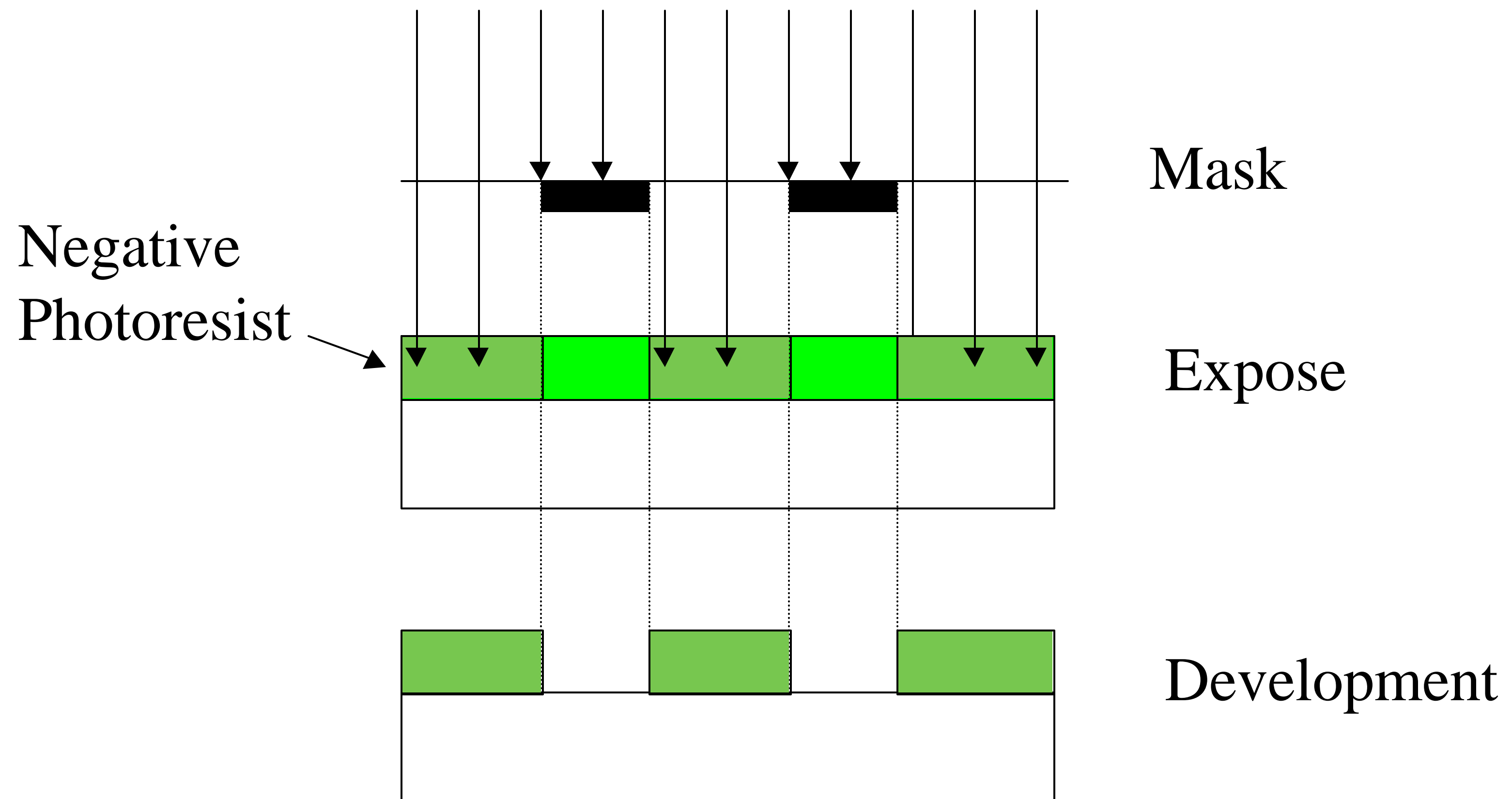
Additives

- Various added chemical to achieve desired process results, such as dyes to reduce reflection.

Negative Resist

- Most negative PR are polyisoprene type
- Exposed PR becomes cross-linked polymer
- Cross-linked polymer has higher chemical etch resistance.
- Unexposed part will be dissolved in development solution.

Negative Photoresist

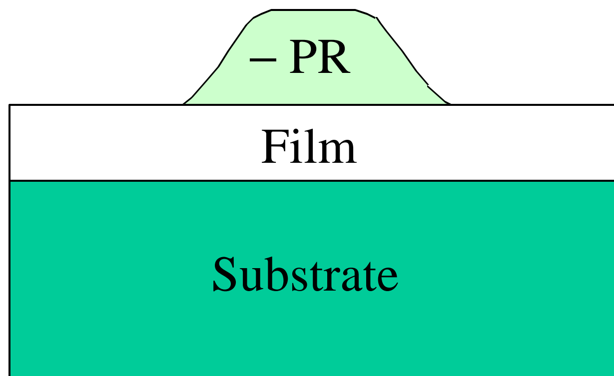


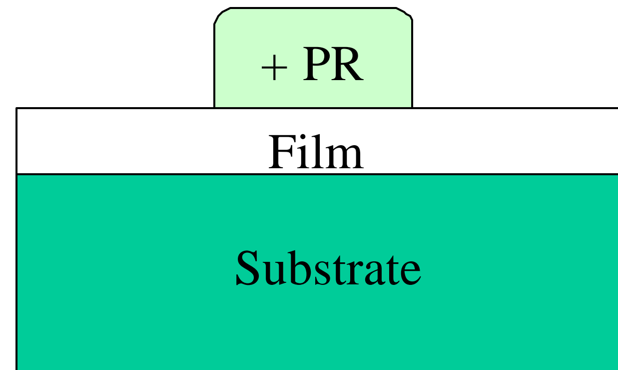
Negative Photoresist

Disadvantages

- Polymer absorbs the development solvent
- Poor resolution due to PR swelling
- Environmental and safety issues due to the main solvents xylene.

Comparison of Photoresists





Positive Photoresist

- Exposed part dissolve in developer solution
- Image the same that on the mask
- Higher resolution
- Commonly used in IC fabs

Positive Photoresist

- Novolac resin polymer
- Acetate type solvents
- Sensitizer cross-linked within the resin
- Energy from the light dissociates the sensitizer and breaks down the cross-links
- Resin becomes more soluble in base solution

Question

- Positive photoresist can achieve much higher resolution than negative photoresist, why didn't people use it before the 1980s?

- Positive photoresist is much more expensive therefore negative photoresist was used until it had to be replaced when the minimum feature size was shrunk to smaller than 3 μm.

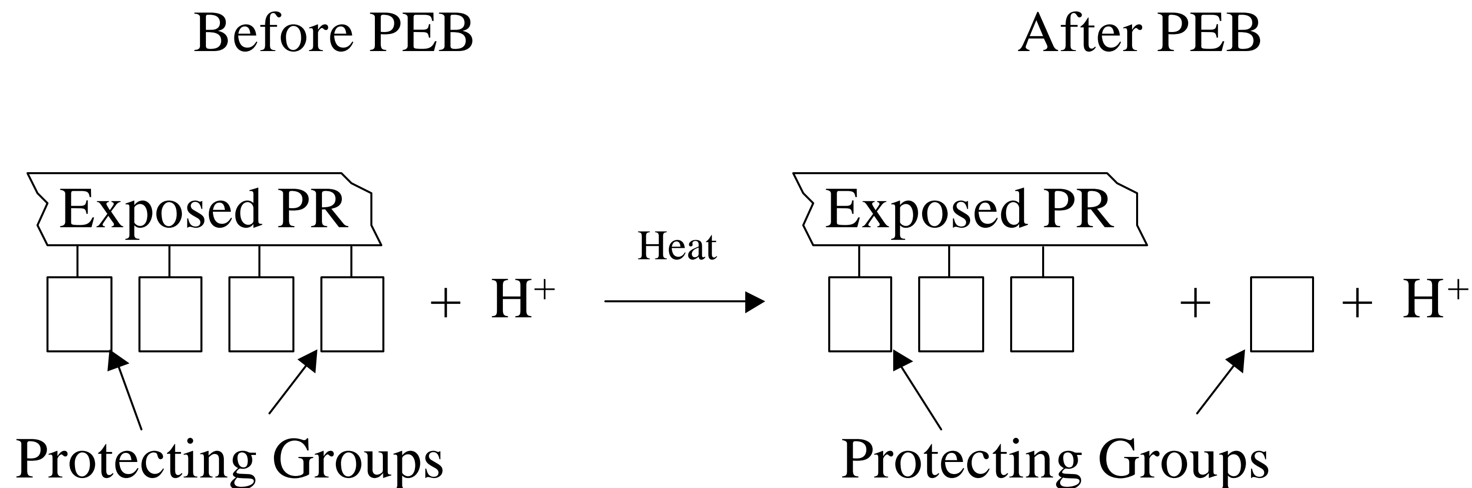
Chemically Amplified Photoresists

- Deep ultraviolet (DUV), $\lambda \leq 248$ nm
- Light source: excimer lasers
- Light intensity is lower than I-line (365 nm) from high-pressure mercury lamp
- Need different kind of photoresist

Chemically Amplified Photoresists

- Catalysis effect is used to increase the effective sensitivity of the photoresist
- A photo-acid is created in PR when it exposes to DUV light
- During PEB, head-induced acid diffusion causes amplification in a catalytic reaction
- Acid removes protection groups
- Exposed part will be removed by developer

Chemically Amplified Photoresist



Requirement of Photoresist

- High resolution
  - Thinner PR film has higher the resolution
  - Thinner PR film, the lower the etching and ion implantation resistance
- High etch resistance
- Good adhesion
- Wider process latitude
  - Higher tolerance to process condition change

Photoresist Physical Properties

- Photoresist must be able to withstand process conditions
  - Coating, spinning, baking, developing.
  - Etch resistance
  - Ion implantation blocking

Photoresist Performance Factor

- Resolution
- Adhesion
- Expose rate, Sensitivity and Exposure Source
- Process latitude
- Pinholes
- Particle and Contamination Levels
- Step Coverage
- Thermal Flow

Resolution Capability

- The smallest opening or space that can produced in a photoresist layer.
- Related to particular processes including expose source and developing process.
- Thinner layer has better resolution.
- Etch and implantation barrier and pinhole-free require thicker layer
- Positive resist has better resolution due to the smaller size of polymer.

Photoresist Characteristics Summary

Parameter	Negative	Positive
Polymer	Polyisoprene	Novolac Resin
Photo-reaction	Polymerization	Photo-solubilization
Sensitizer	Provide free radicals for polymer cross-link	Changes film to base soluble
Additives	Dyes	Dyes

Photolithography Process

Basic Steps of Photolithography

- Photoresist coating
- Alignment and exposure
- Development

Basic Steps, Old Technology

- Wafer clean
- Dehydration bake
- Spin coating primer and PR
- Soft bake
- Alignment and exposure
- Development
- Pattern inspection
- Hard bake

(Wafer clean through Soft bake: PR coating)

(Development through Hard bake: Development)

Basic Steps, Advanced Technology

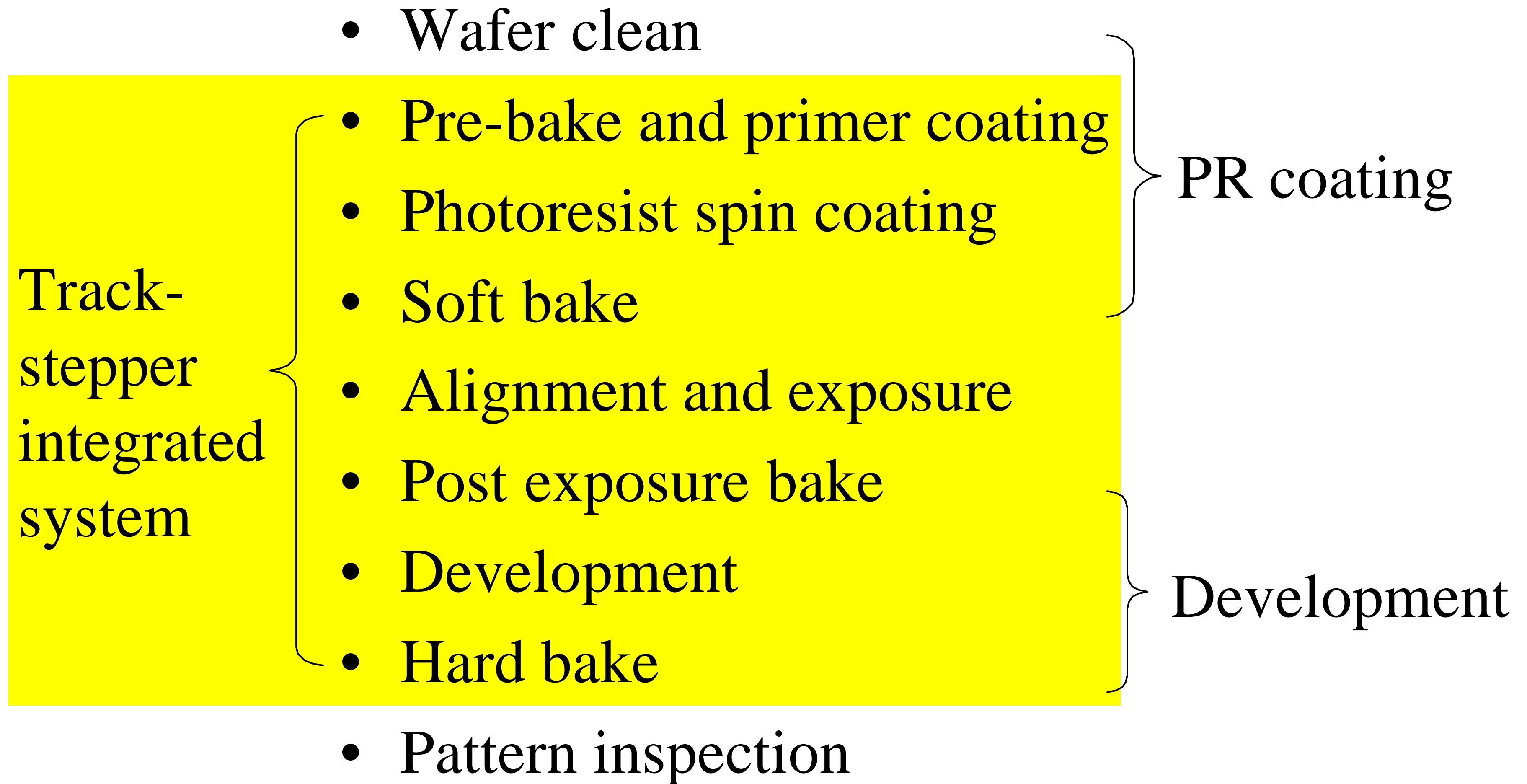
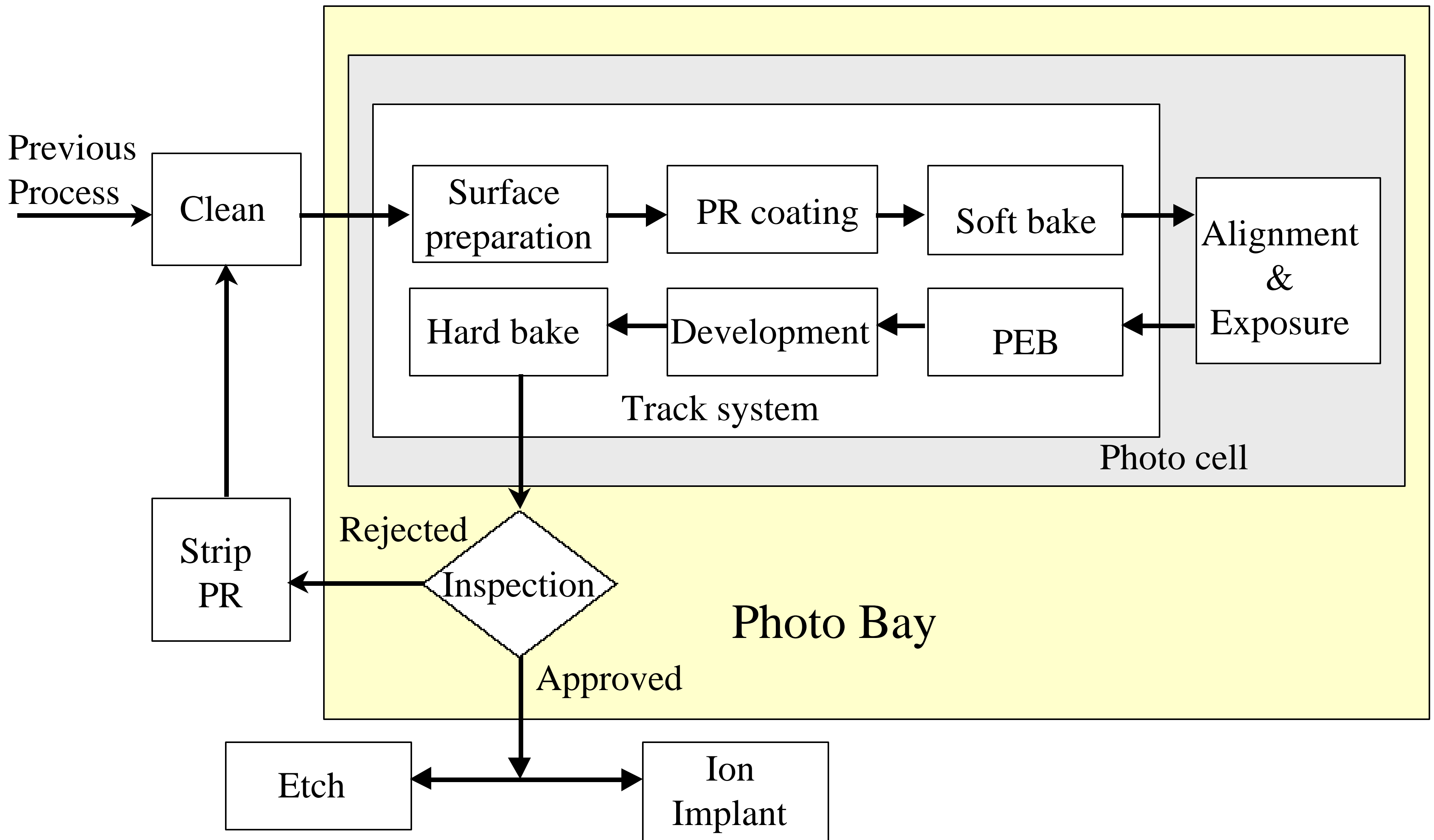
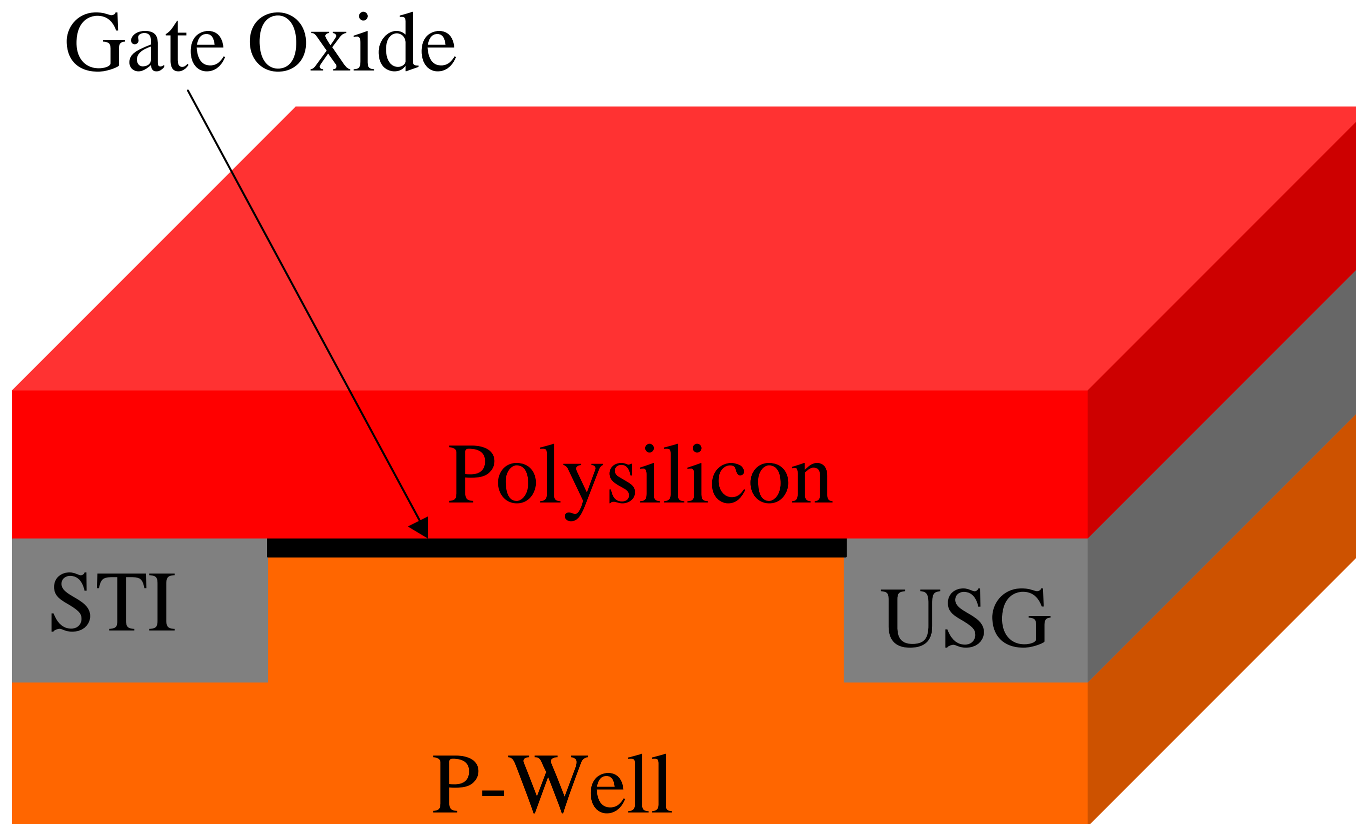


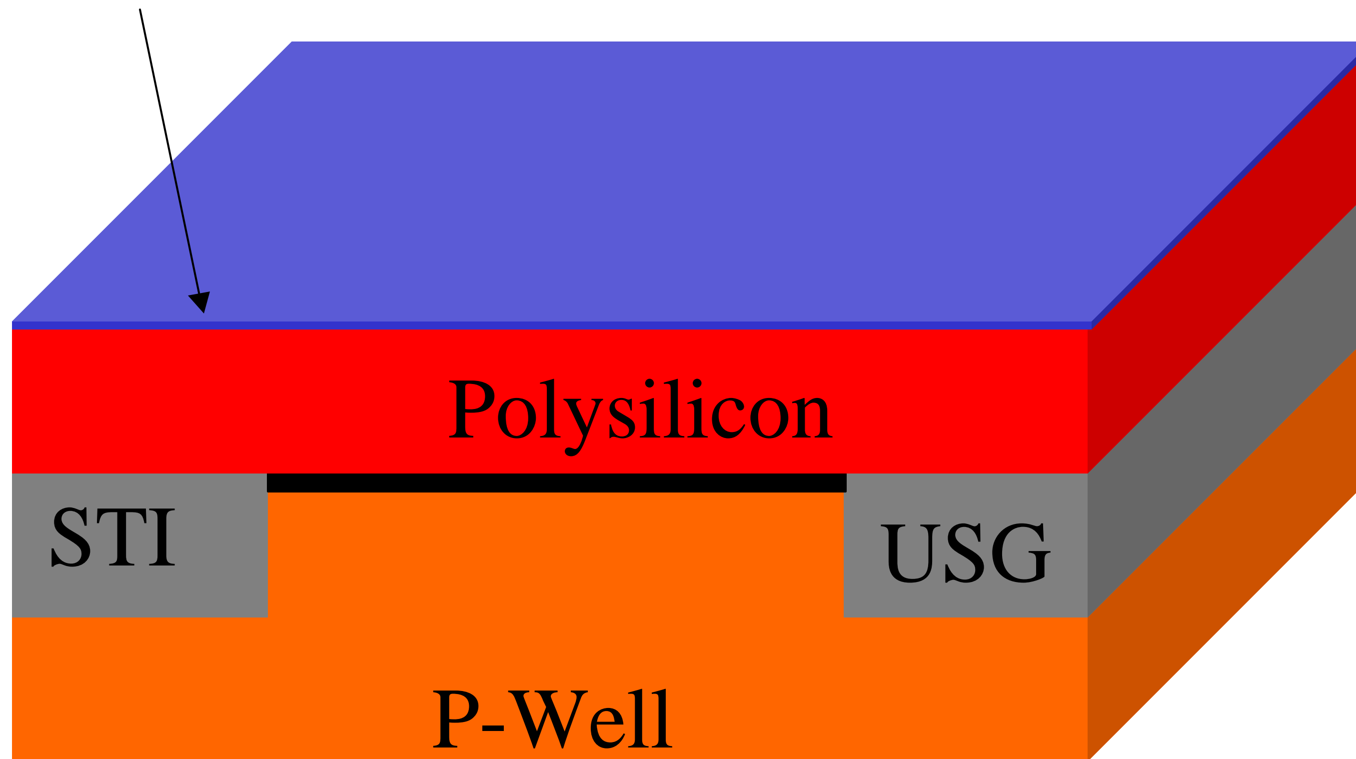
Figure 6.5



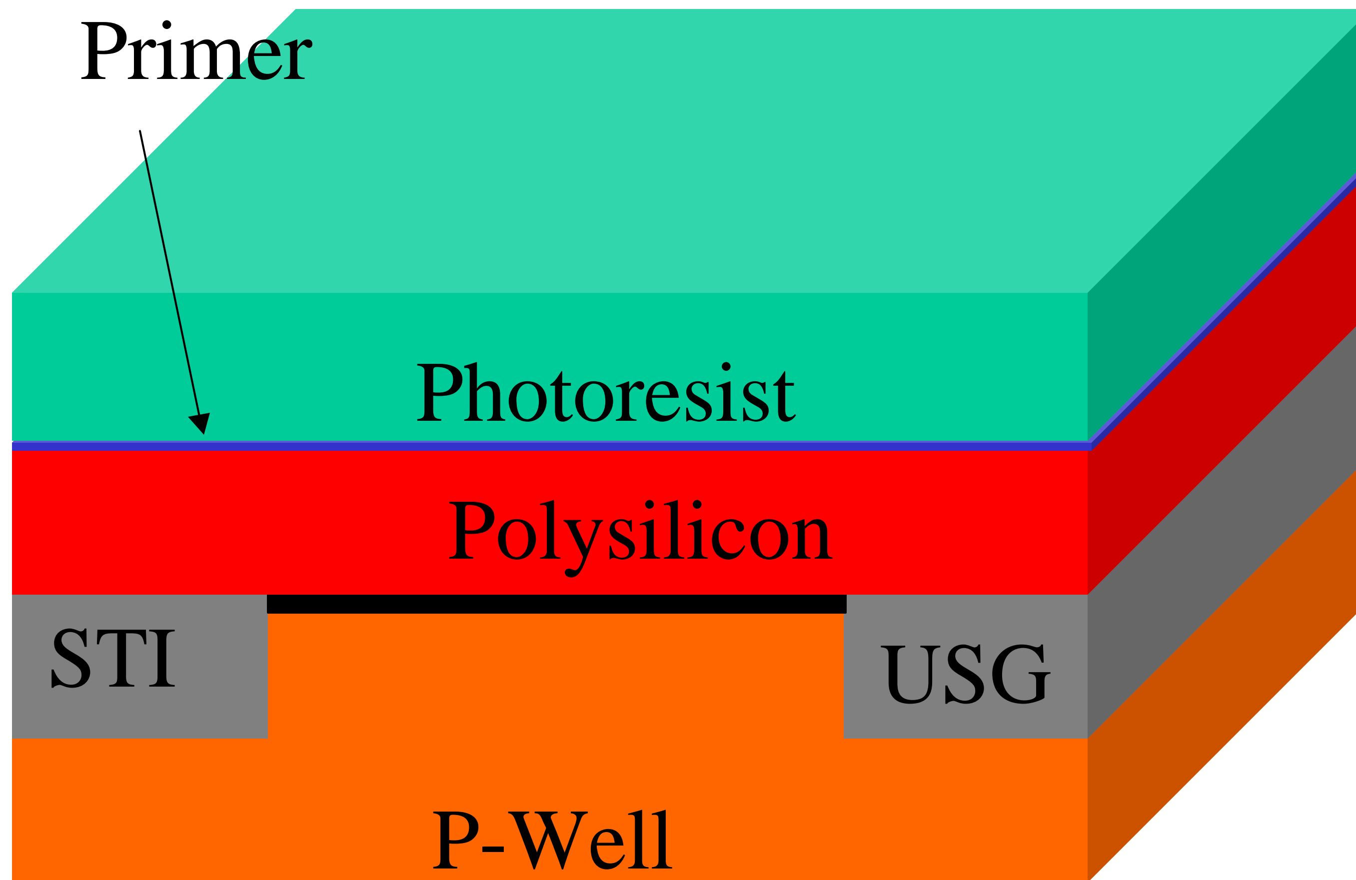
Wafer Clean



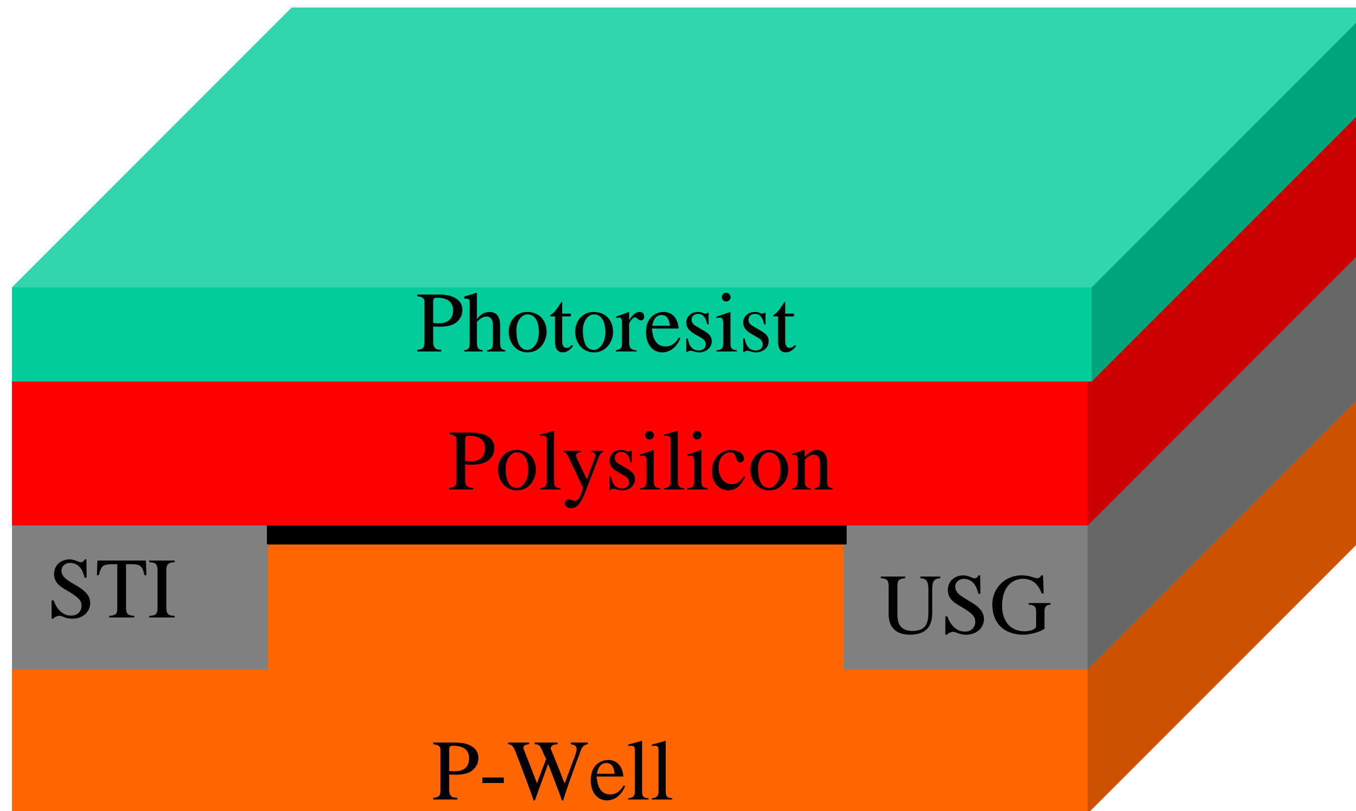
Pre-bake and Primer Vapor



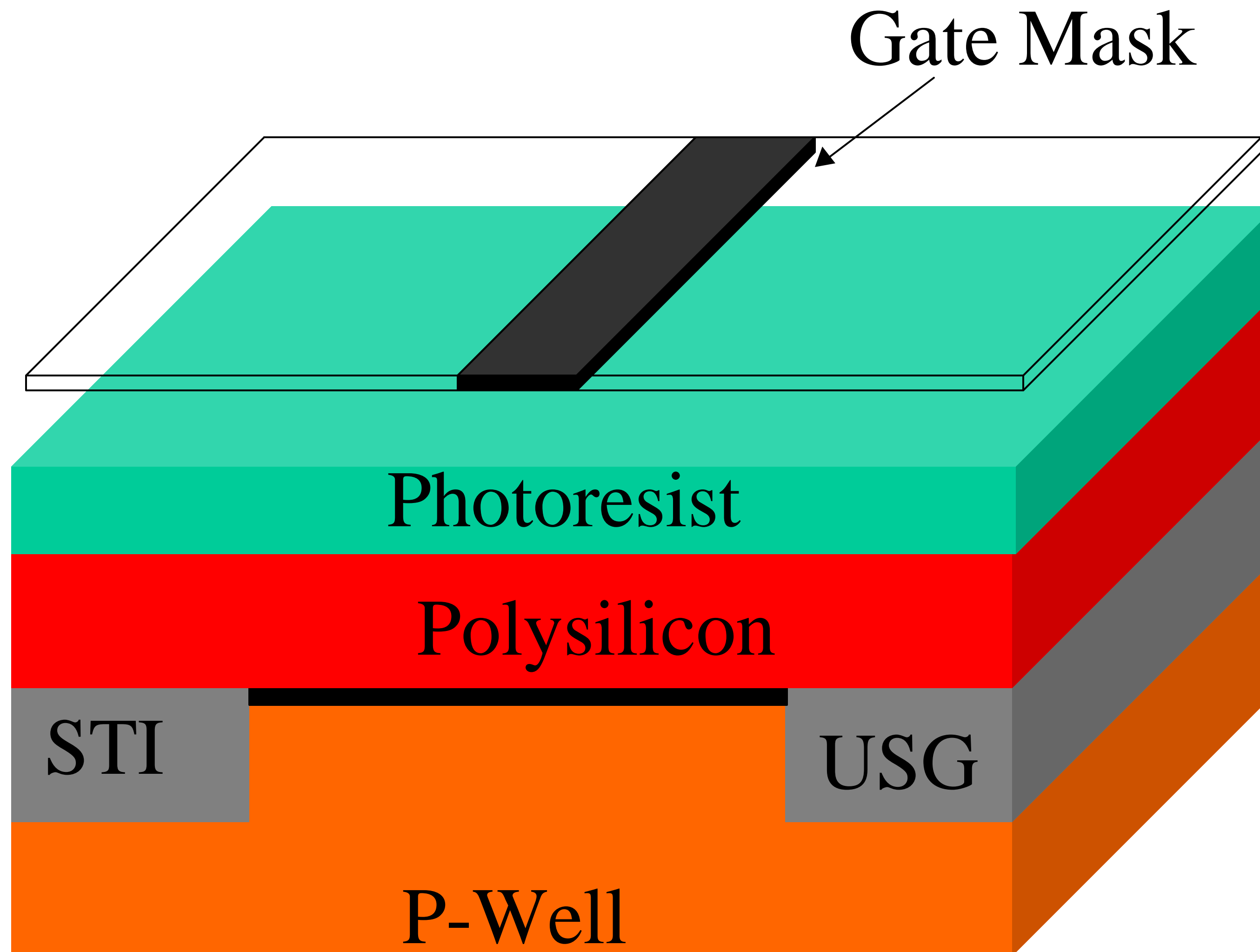
Photoresist Coating



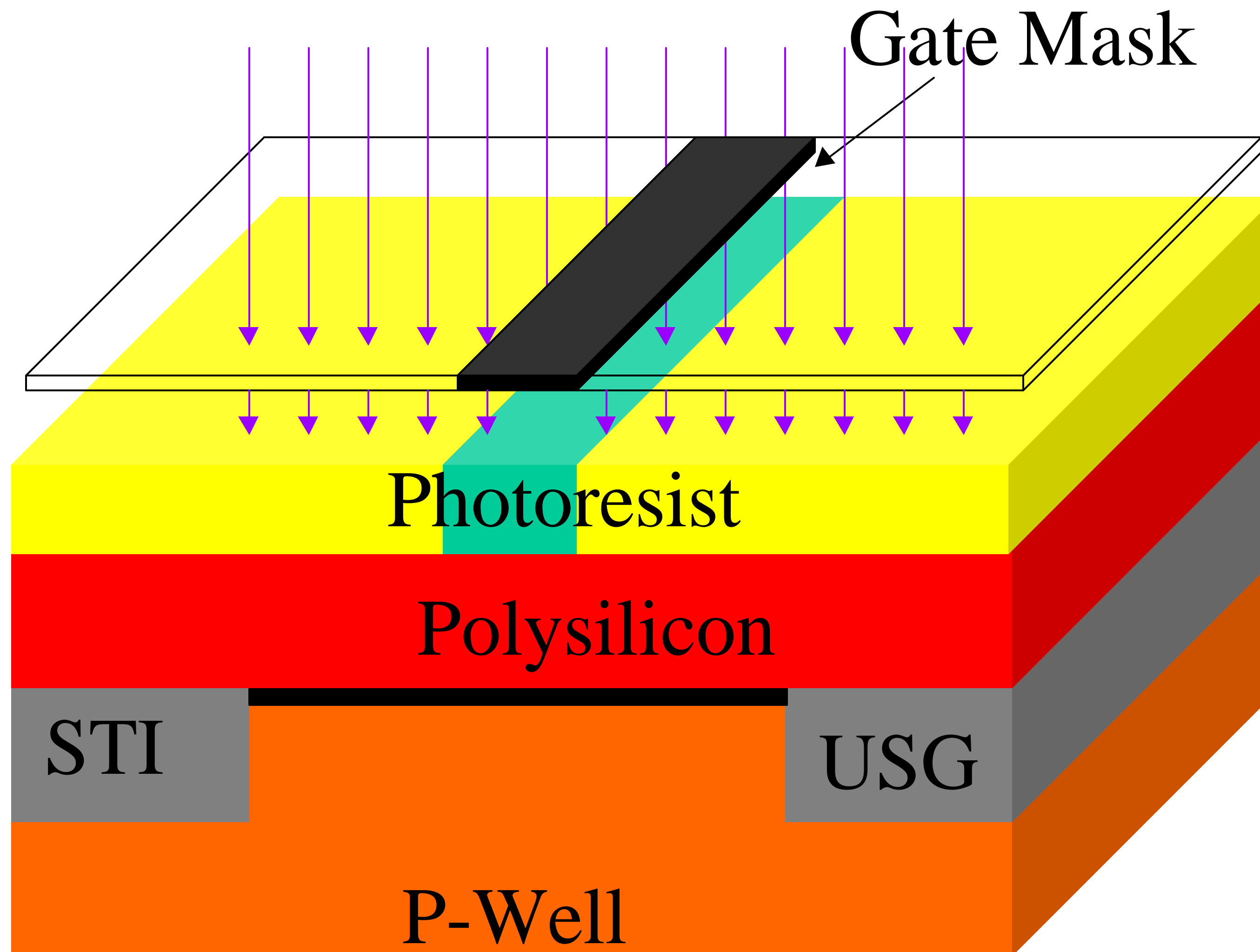
Soft Bake



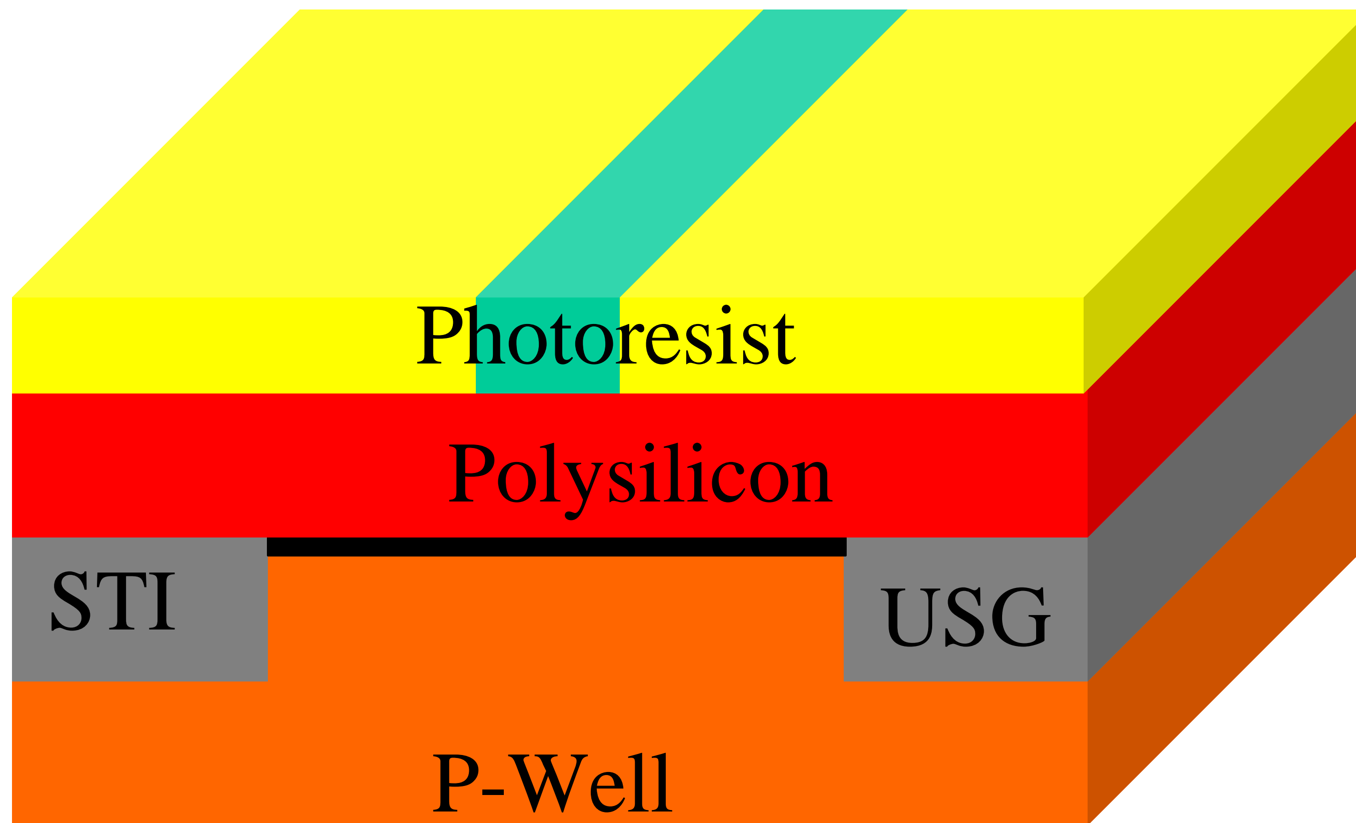
Alignment and Exposure



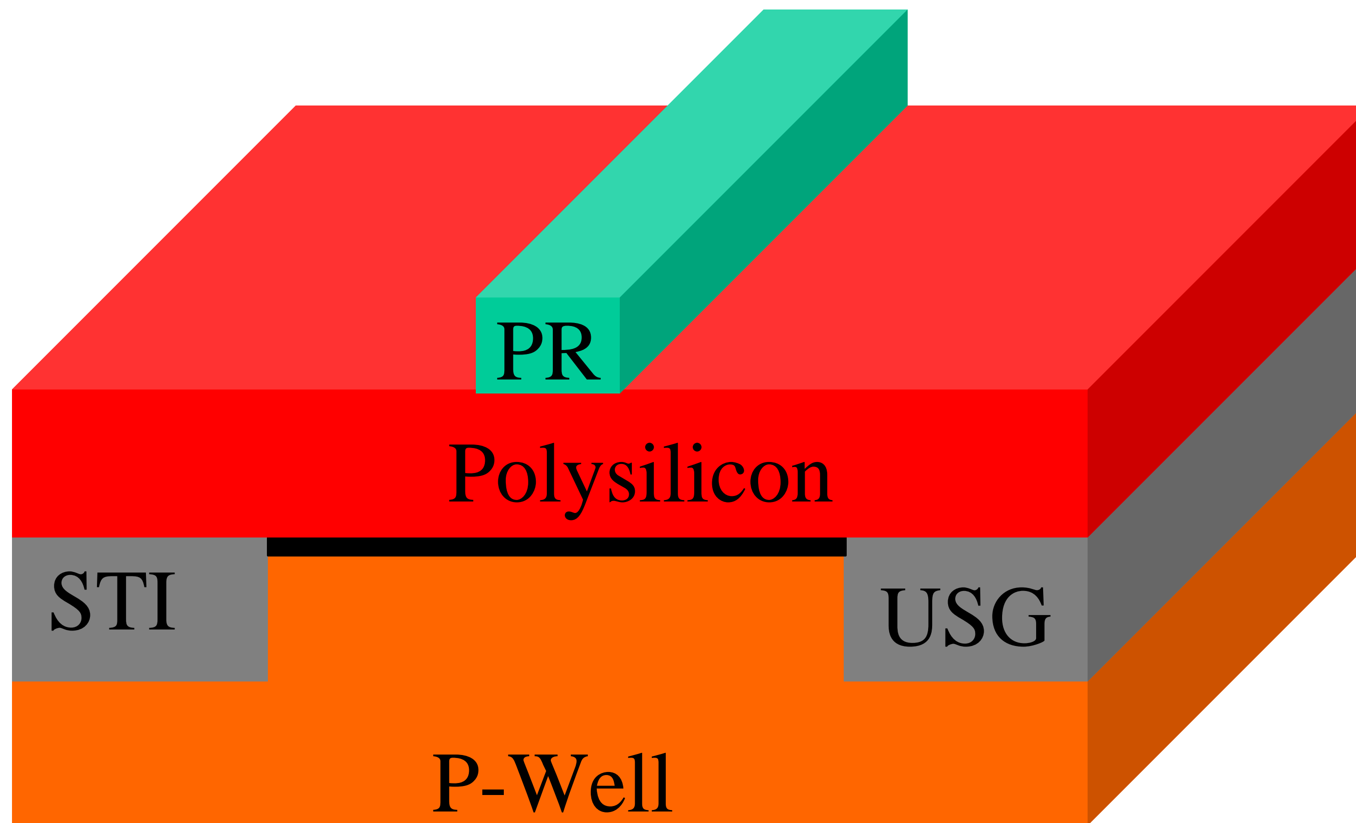
Alignment and Exposure



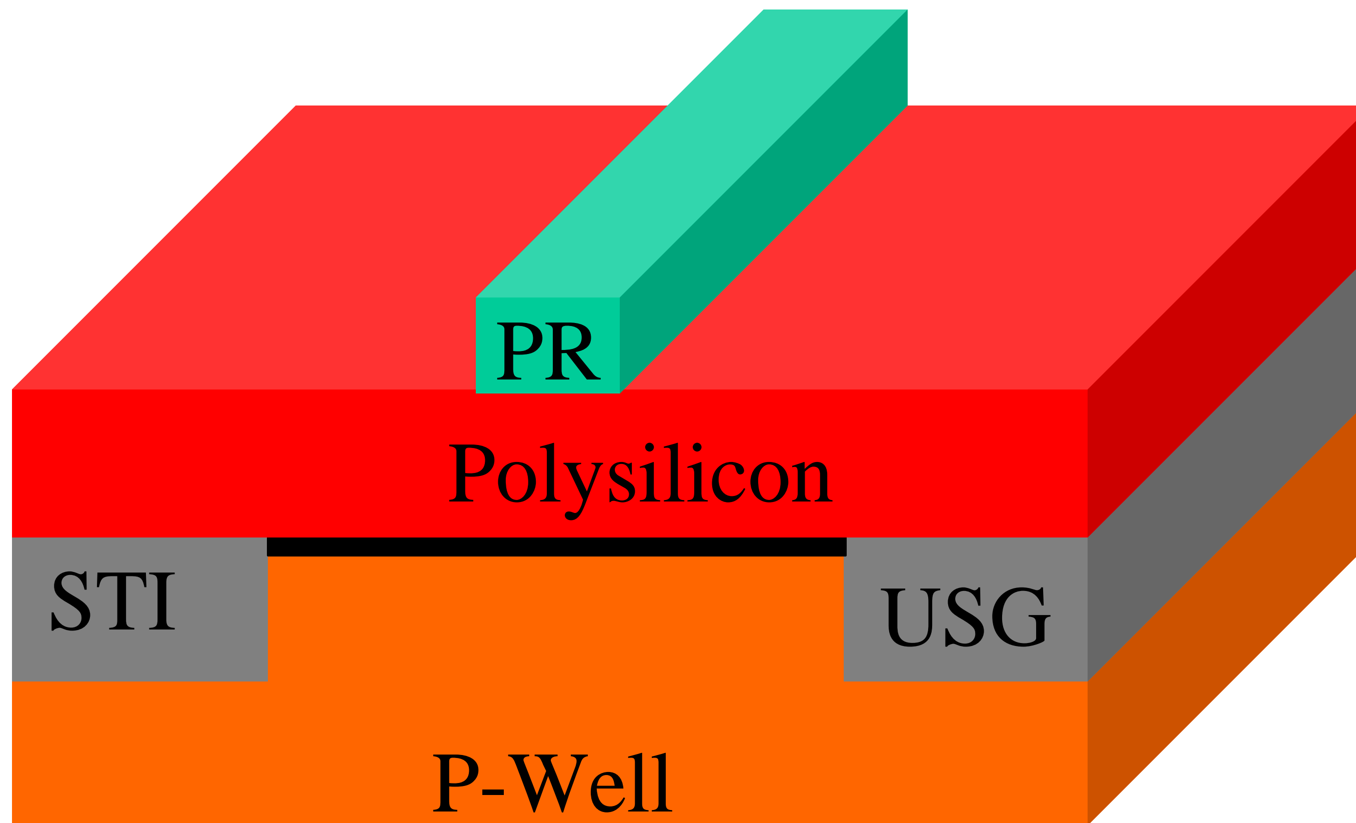
Post Exposure Bake



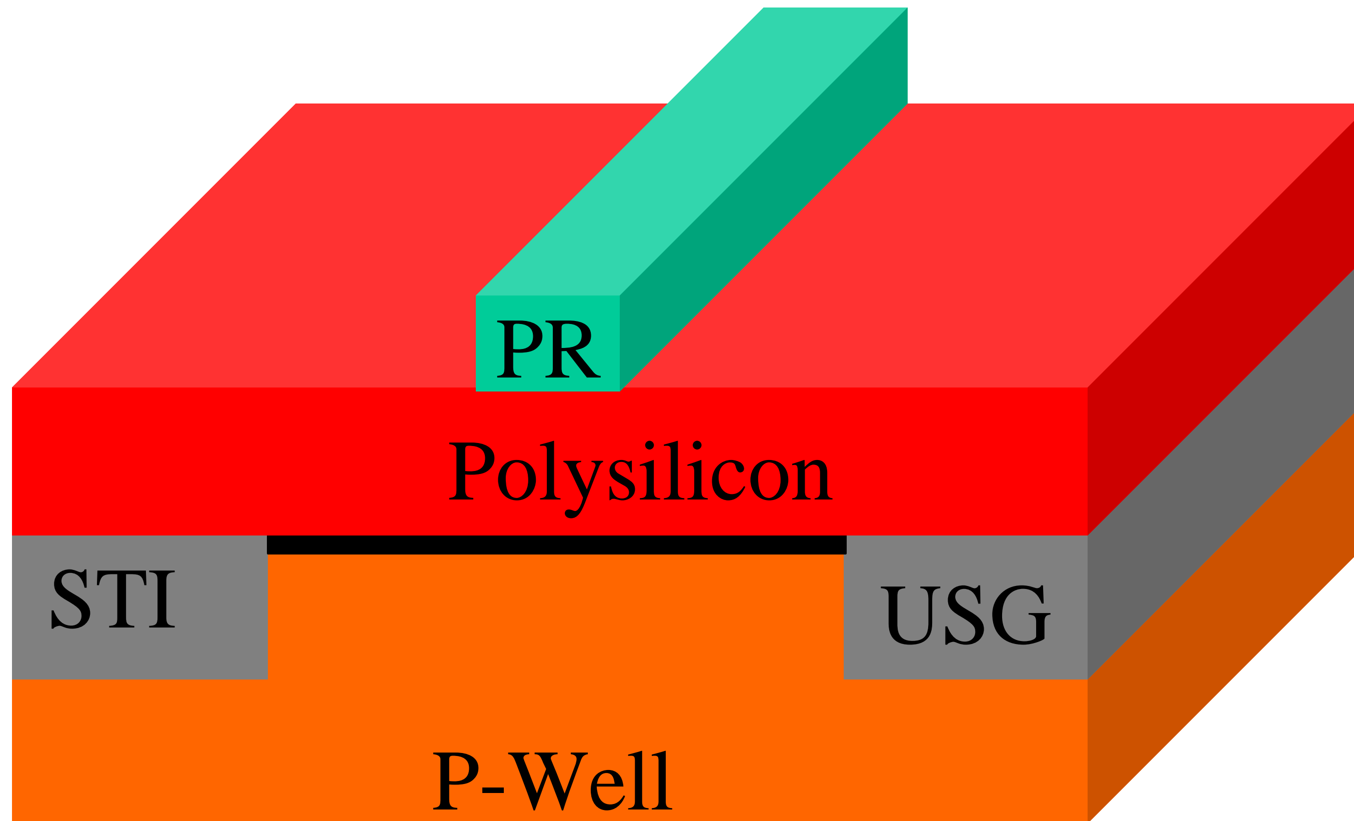
Development



Hard Bake



Pattern Inspection



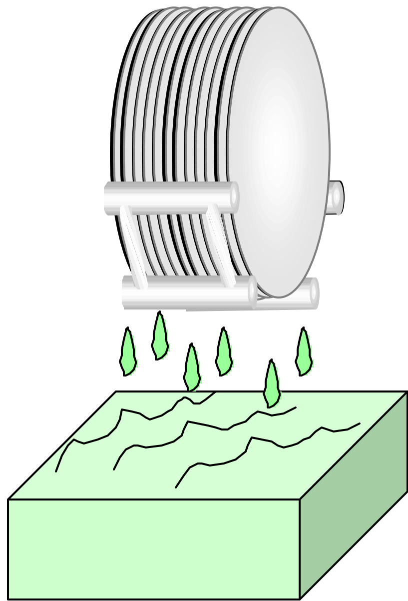
Wafer Clean

- Remove contaminants
- Remove particulate
- Reduce pinholes and other defects
- Improve photoresist adhesion
- Basic steps
  - Chemical clean
  - Rinse
  - Dry

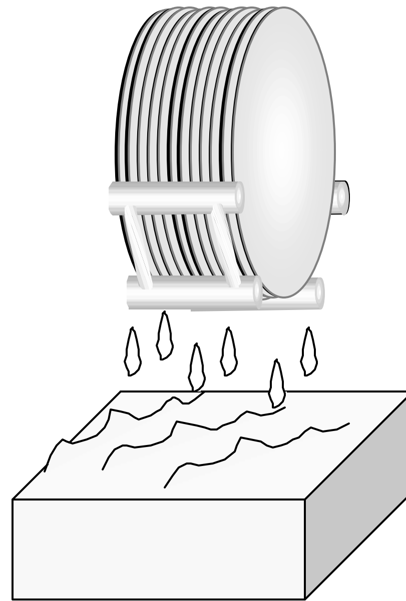
Photolithography Process, Clean

- Older ways
  - High-pressure nitrogen blow-off
  - Rotating brush scrubber
  - High-pressure water stream

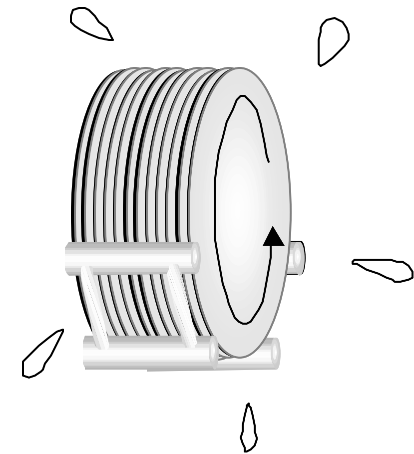
Wafer Clean Process



Chemical Clean



Rinse



Dry

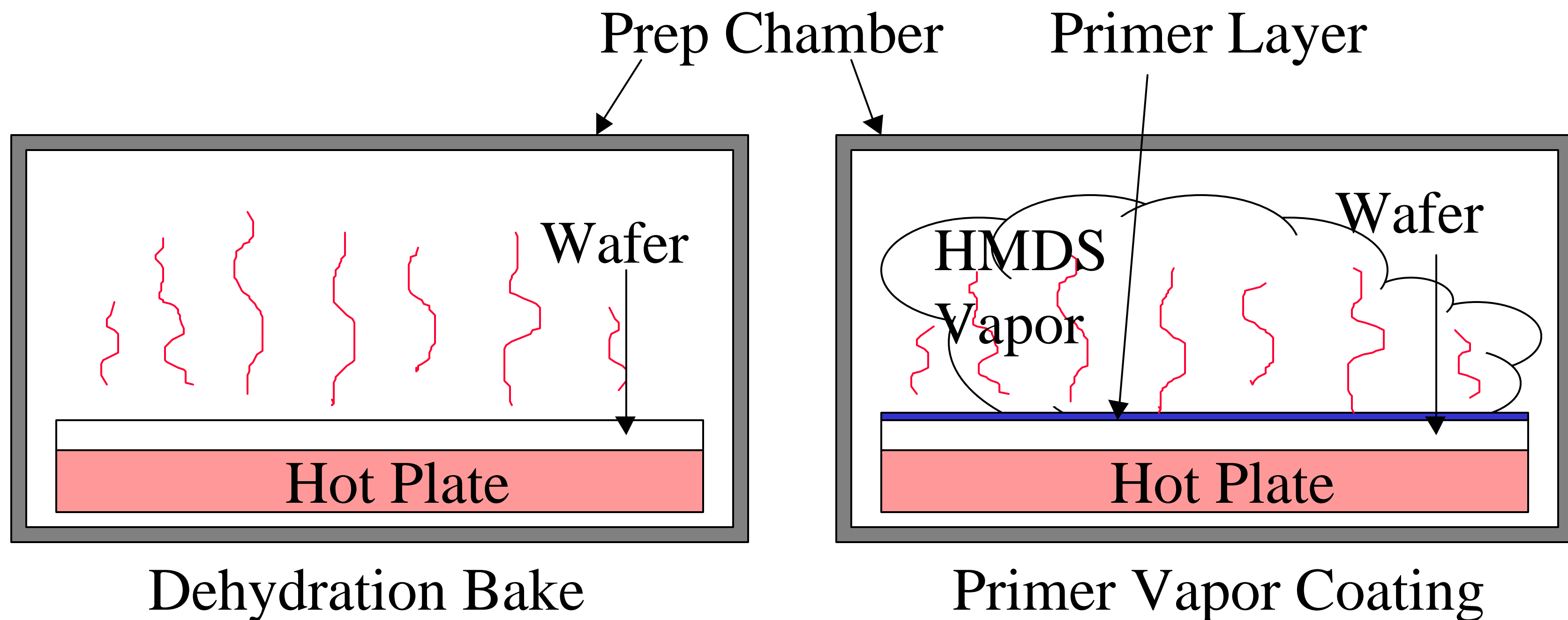
Photolithography Process, Prebake

- Dehydration bake
- Remove moisture from wafer surface
- Promote adhesion between PR and surface
- Usually around 100 °C
- Integration with primer coating

Photolithography Process, Primer

- Promotes adhesion of PR to wafer surface
- Wildly used: Hexamethyldisilazane (HMDS)
- HMDS vapor coating prior to PR spin coating
- Usually performed in-situ with pre-bake
- Chill plate to cool down wafer before PR coating

Pre-bake and Primer Vapor Coating



Wafer Cooling

- Wafer need to cool down
- Water-cooled chill plate
- Temperature can affect PR viscosity
  - Affect PR spin coating thickness

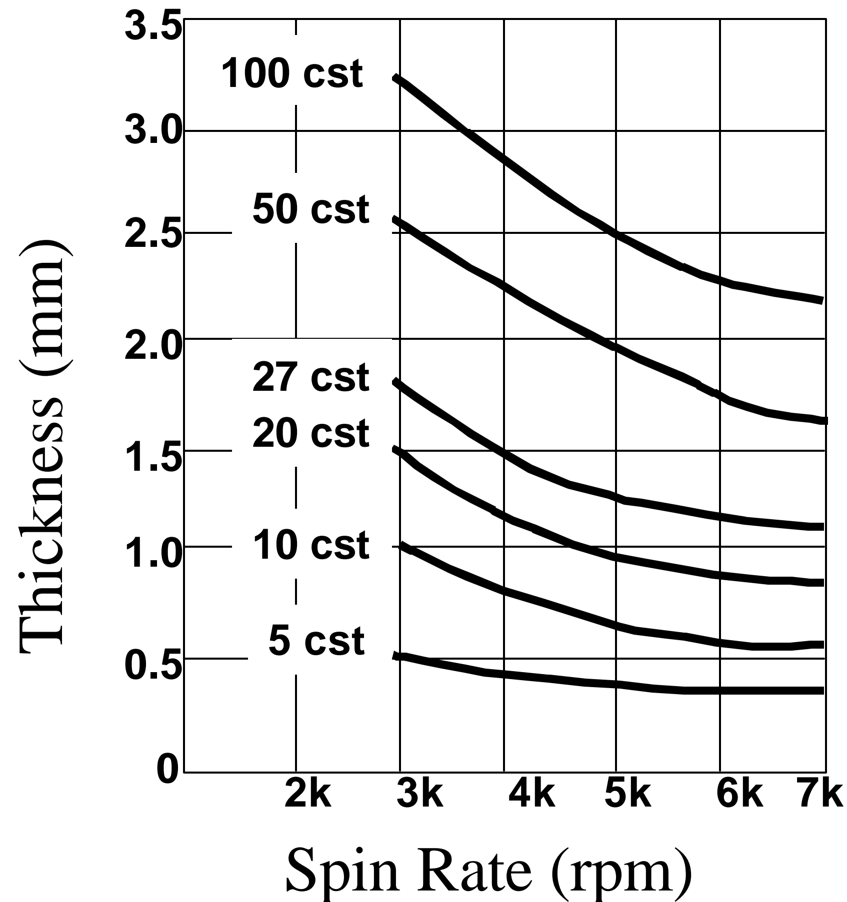
Spin Coating

- Wafer sit on a vacuum chuck
- Rotate at high speed
- Liquid photoresist applied at center of wafer
- Photoresist spread by centrifugal force
- Evenly coat on wafer surface

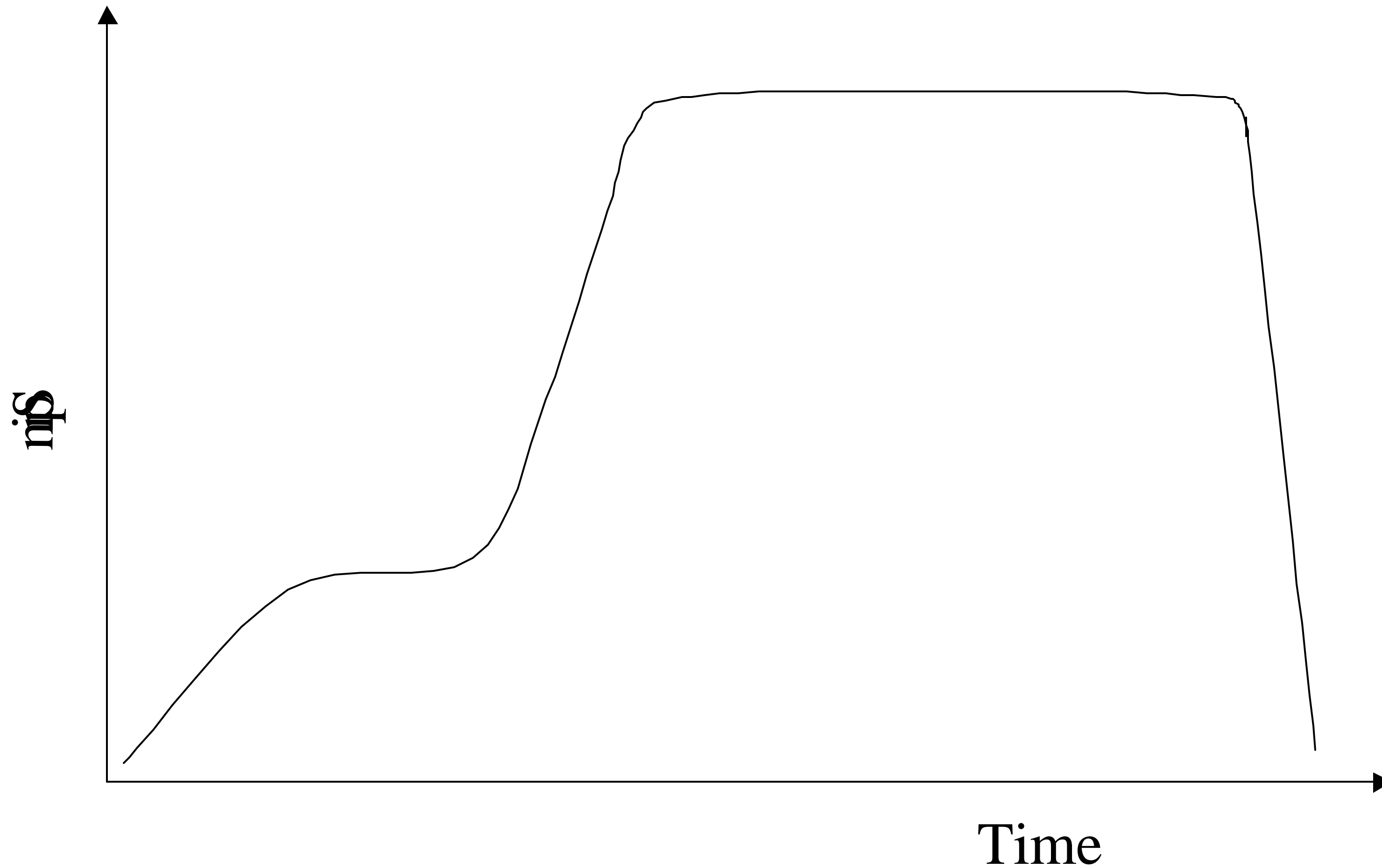
Viscosity

- Fluids stick on the solid surface
- Affect PR thickness in spin coating
- Related to PR type and temperature
- Need high spin rate for uniform coating

Relationship of Photoresist Thickness to Spin Rate and Viscosity



Dynamic Spin Rate



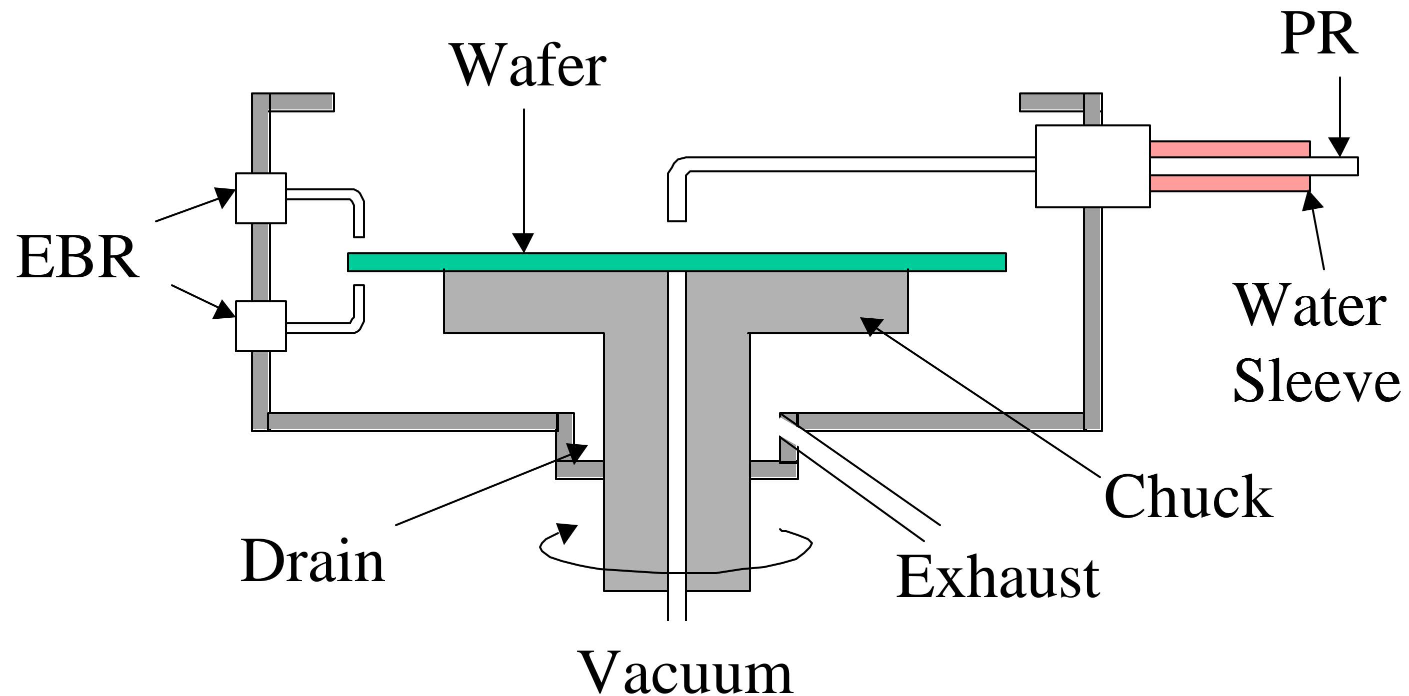
PR Spin Coater

- Photoresist spread on spinning wafer surface
- Wafer held on a vacuum chuck
- Slow spin ~ 500 rpm
- Ramp up to ~ 3000 - 7000 rpm

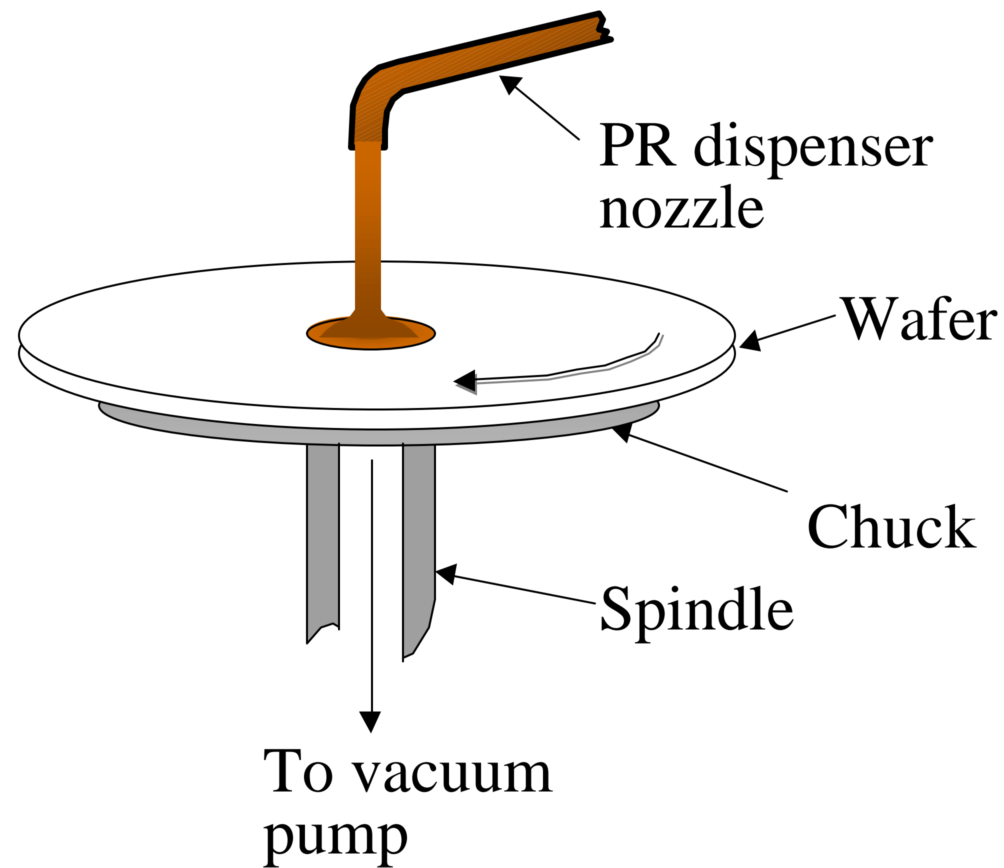
Spin Coater

- Automatic wafer loading system from robot of track system
- Vacuum chuck to hold wafer
- Resist containment and drain
- Exhaust features
- Controllable spin motor
- Dispenser and dispenser pump
- Edge bead removal

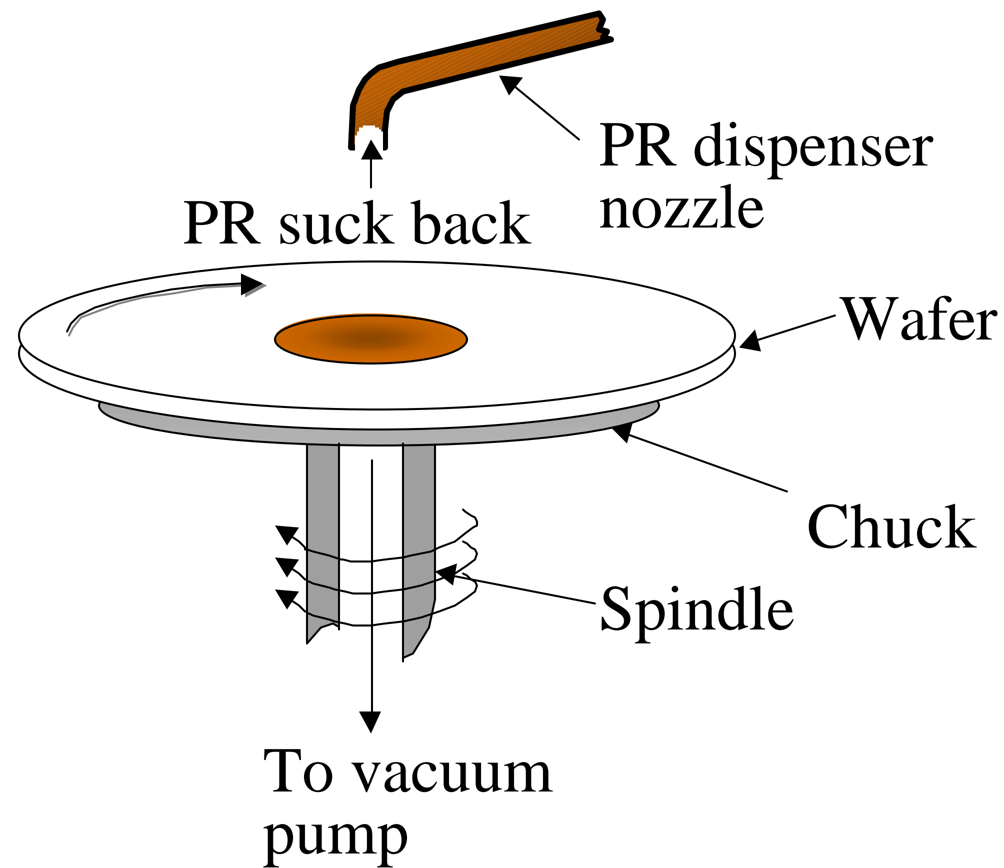
Photoresist Spin Coater



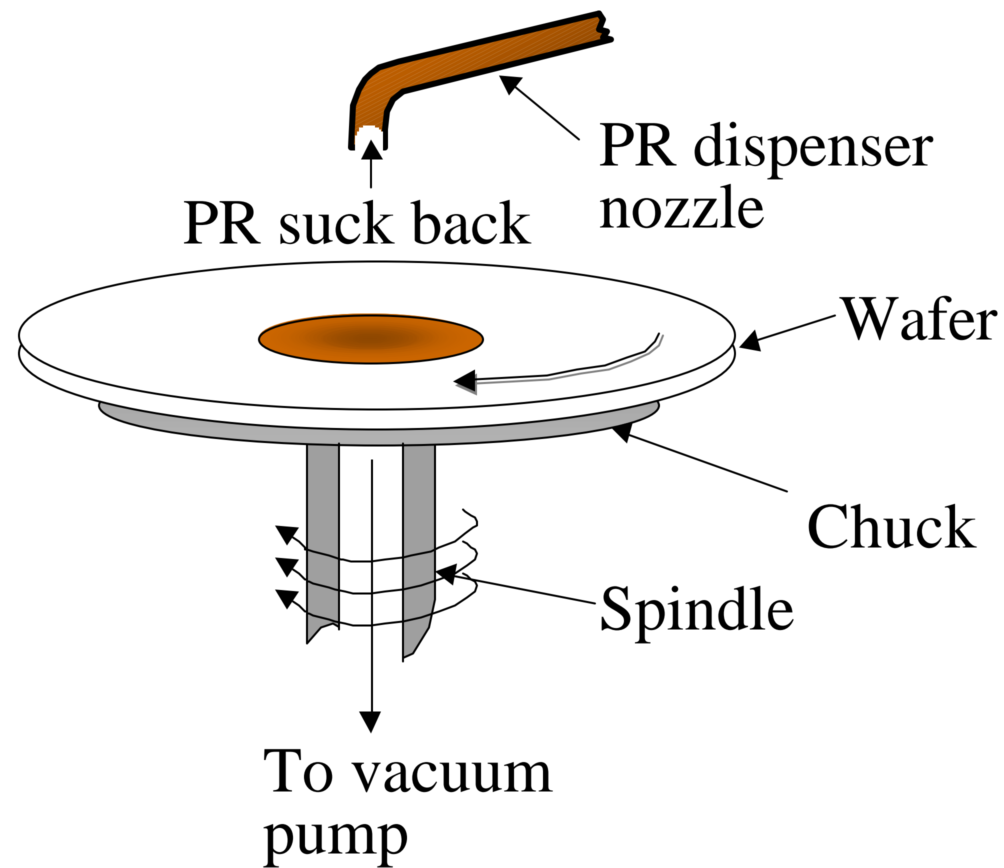
Photoresist Applying



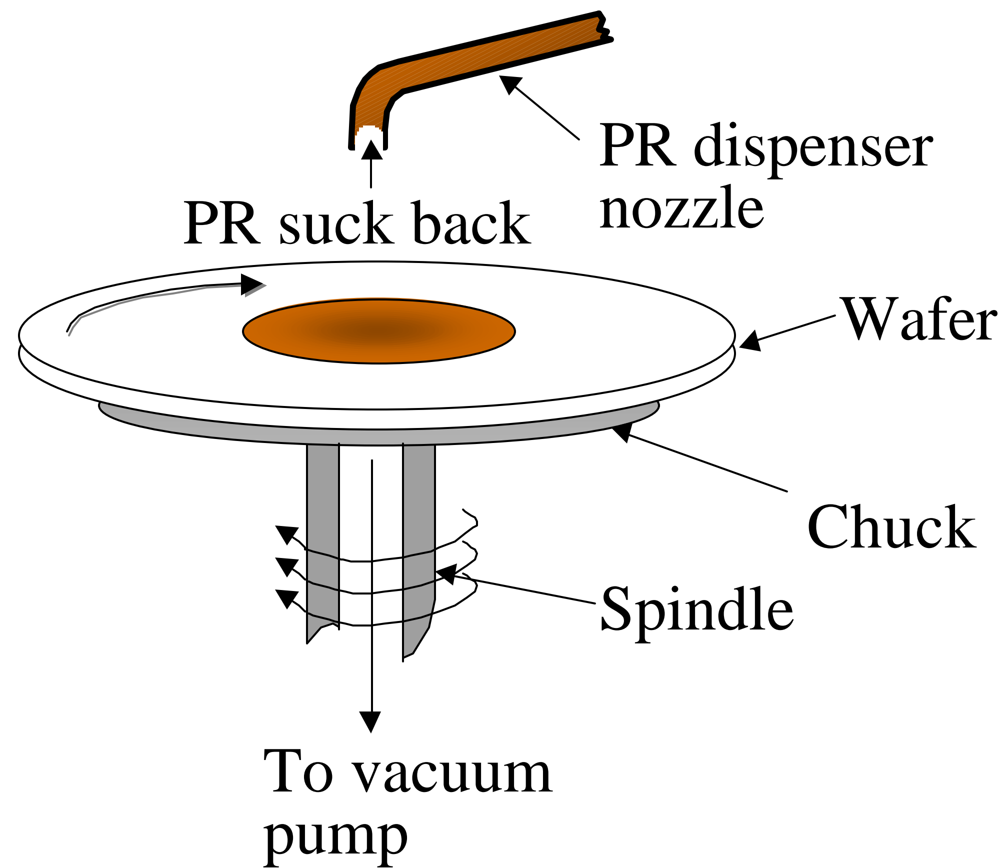
Photoresist Suck Back



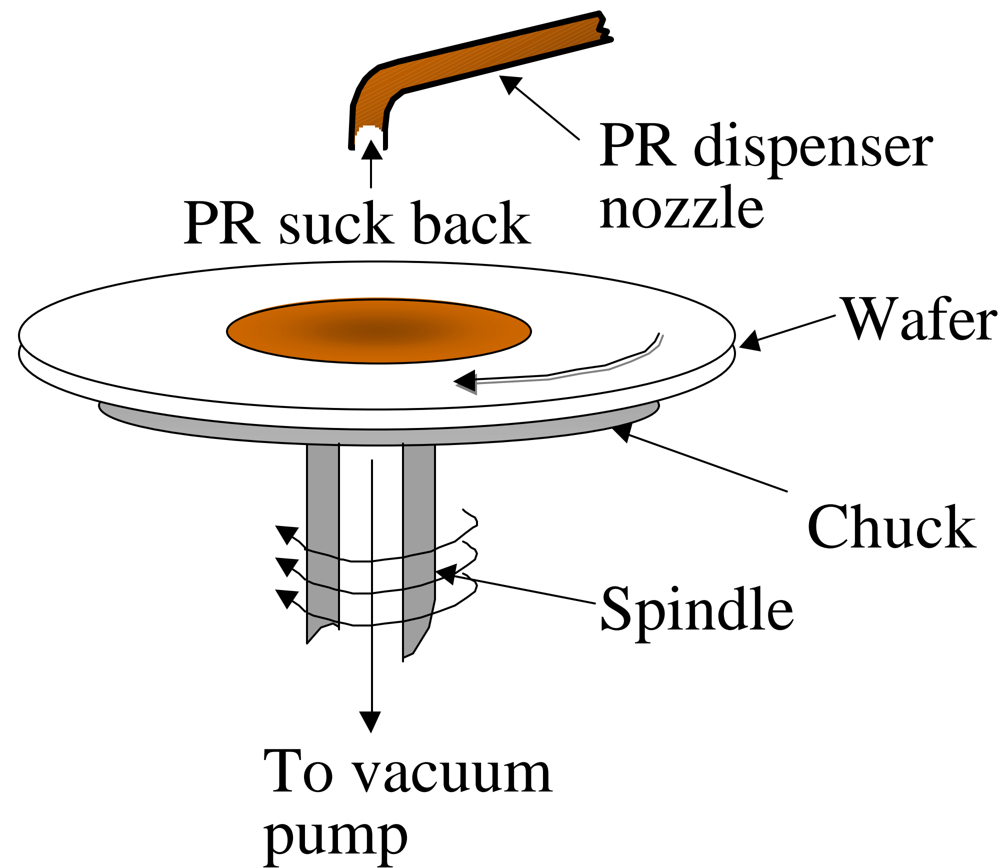
Photoresist Spin Coating



Photoresist Spin Coating

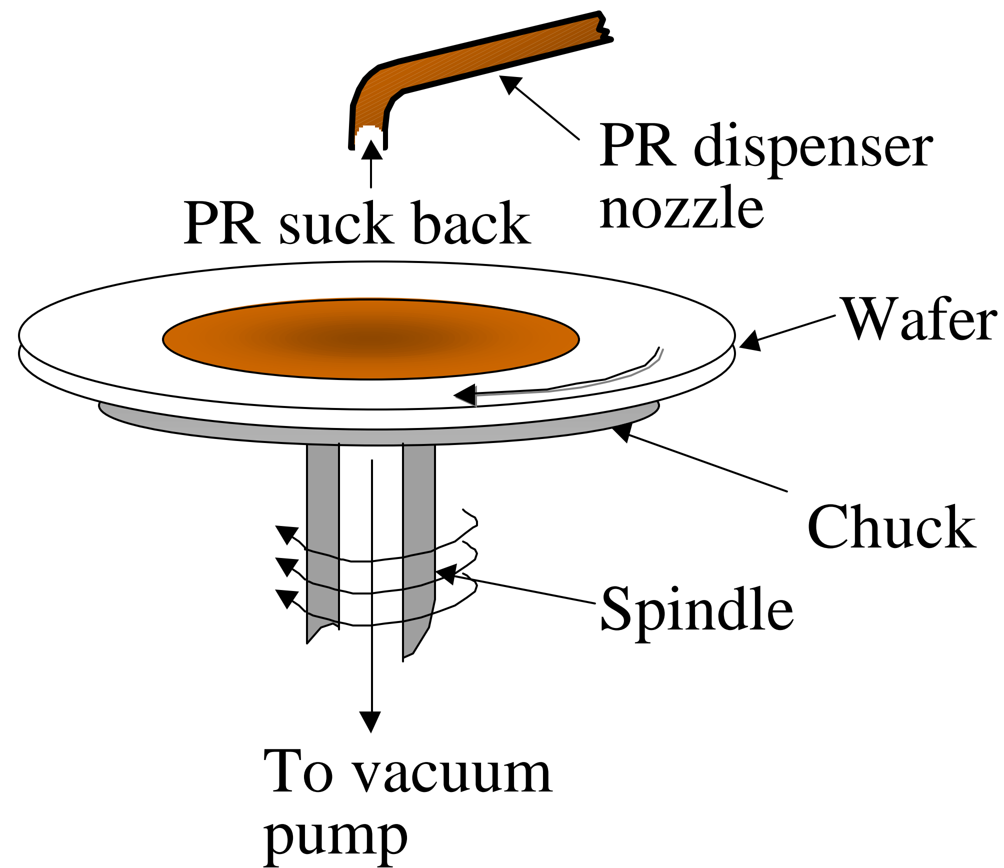


Photoresist Spin Coating

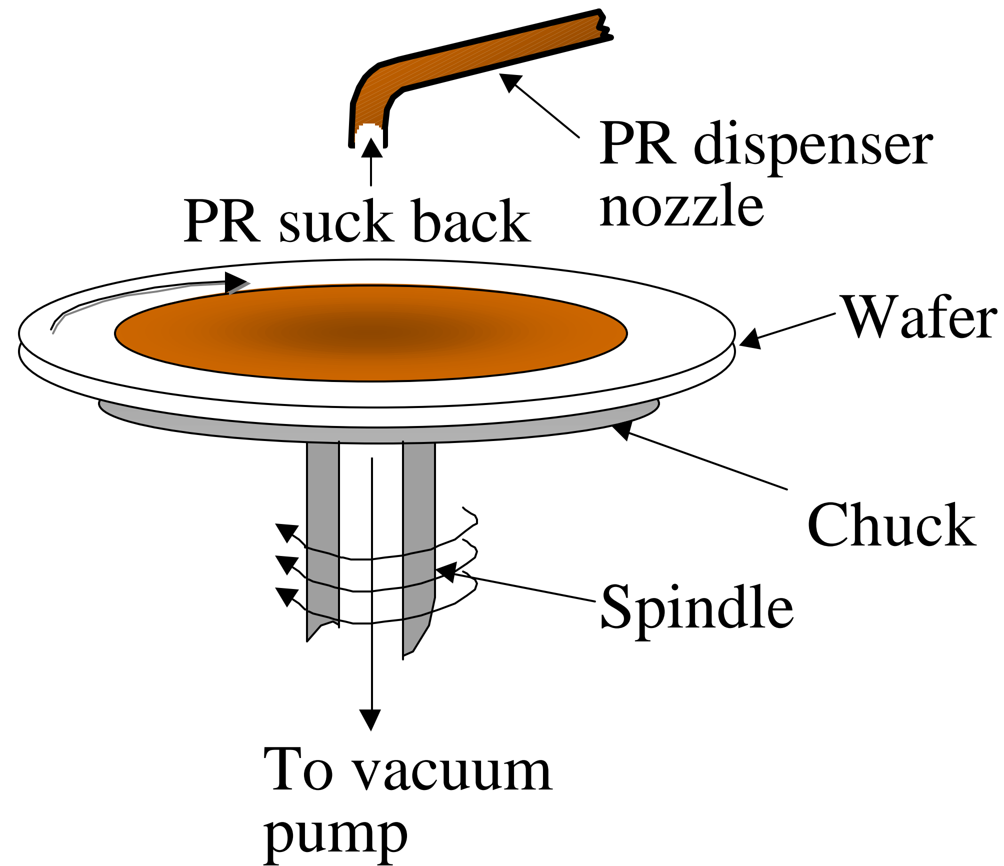


Photoresist Spin Coating

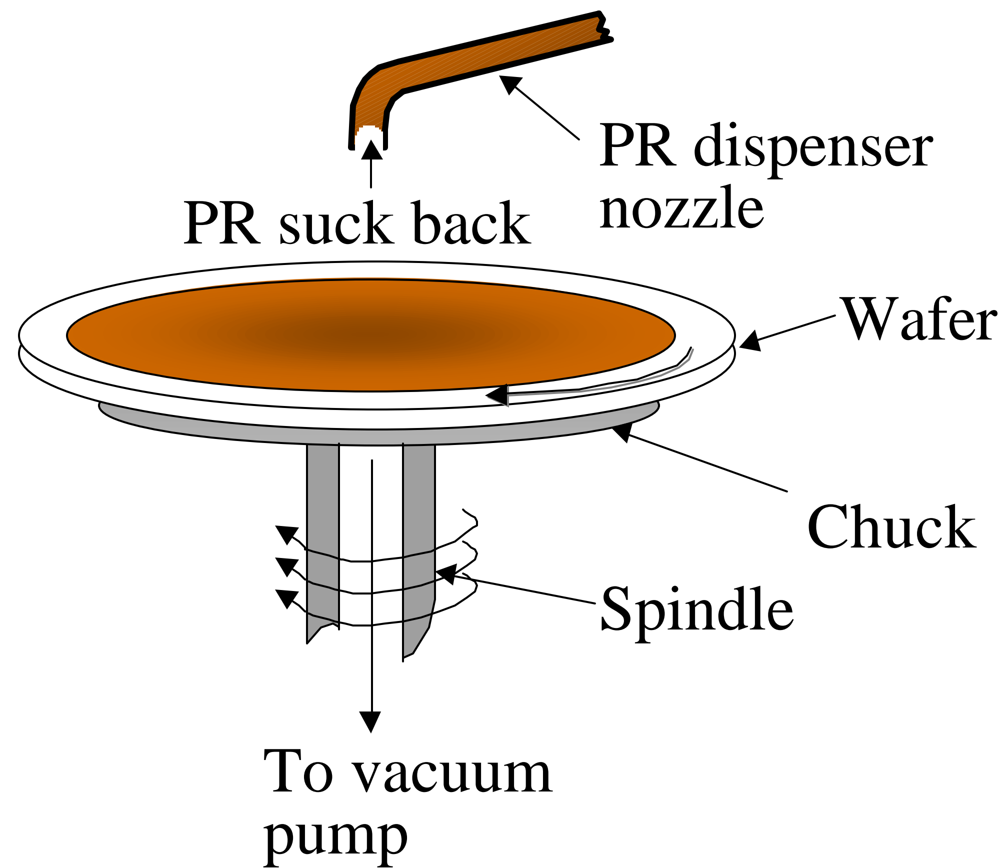
Photoresist Spin Coating



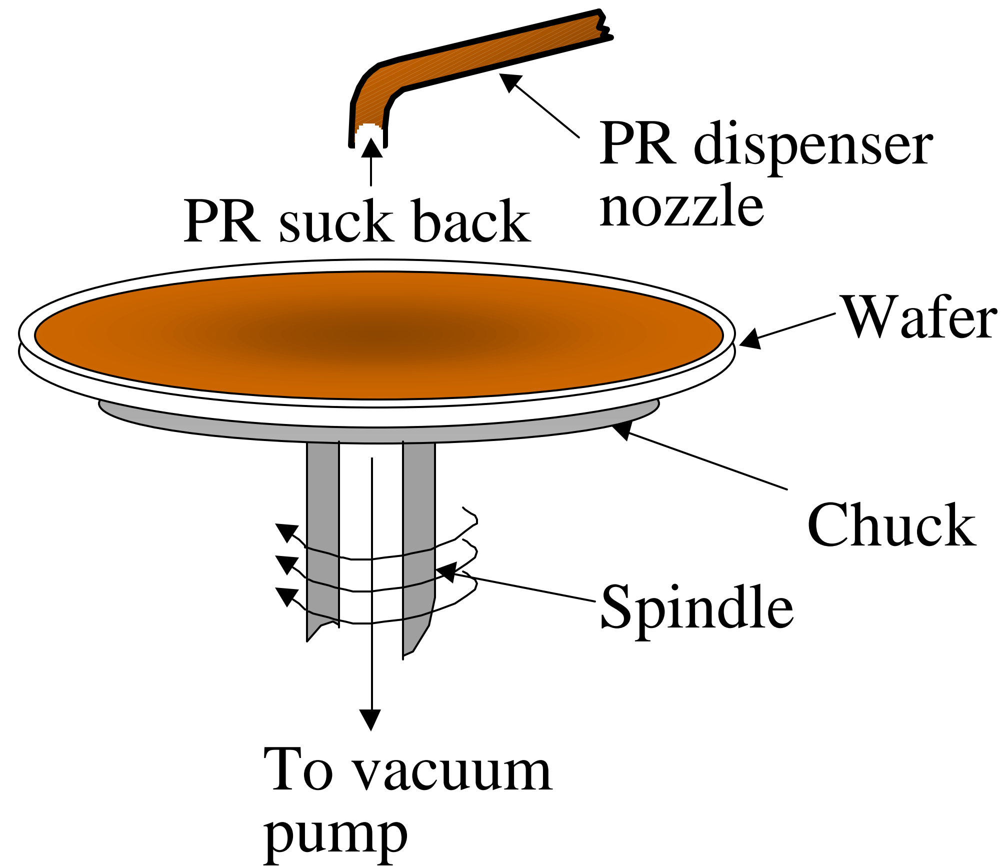
Photoresist Spin Coating



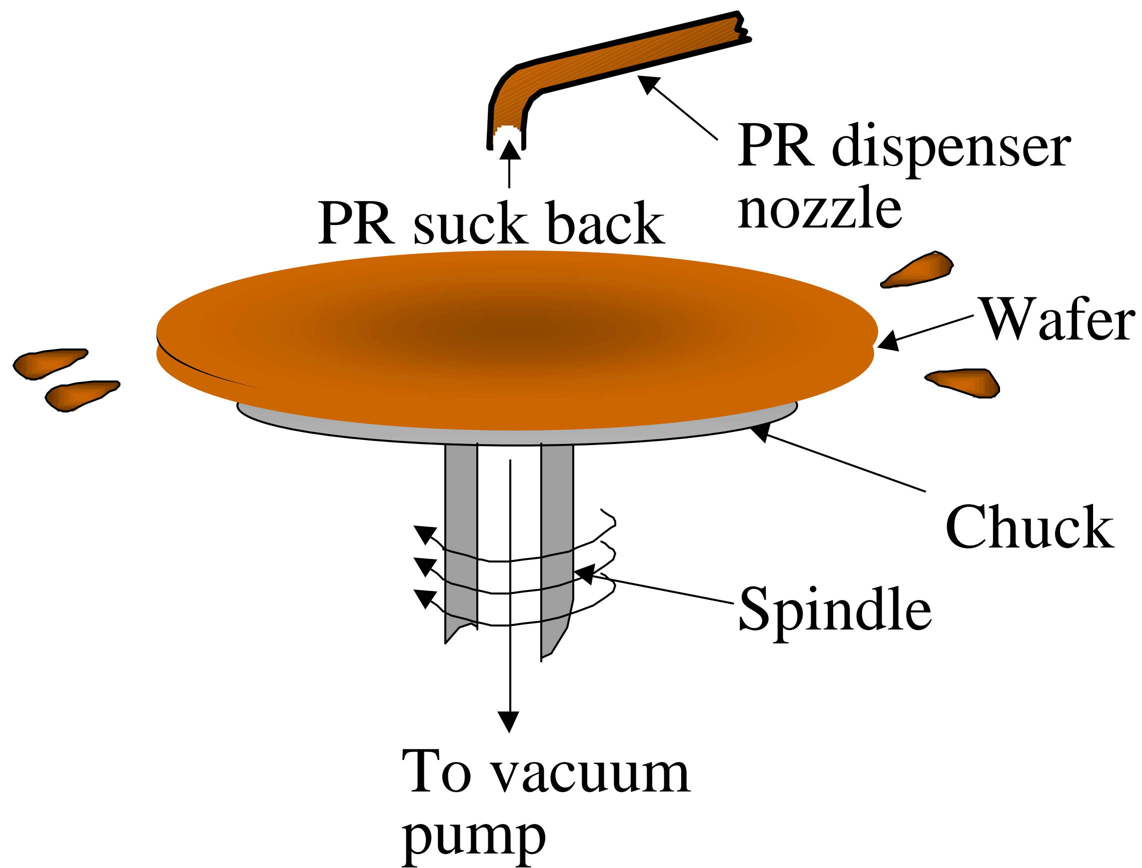
Photoresist Spin Coating



Photoresist Spin Coating



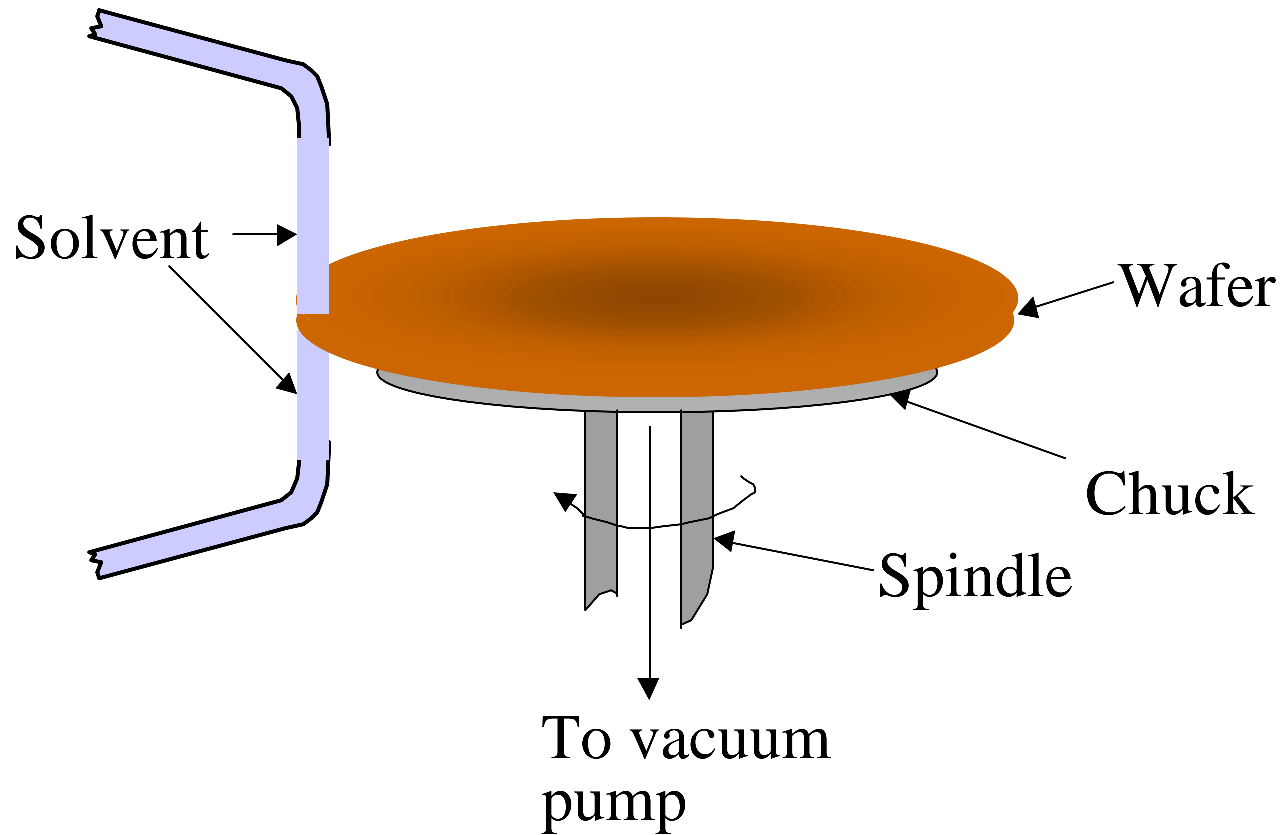
Photoresist Spin Coating



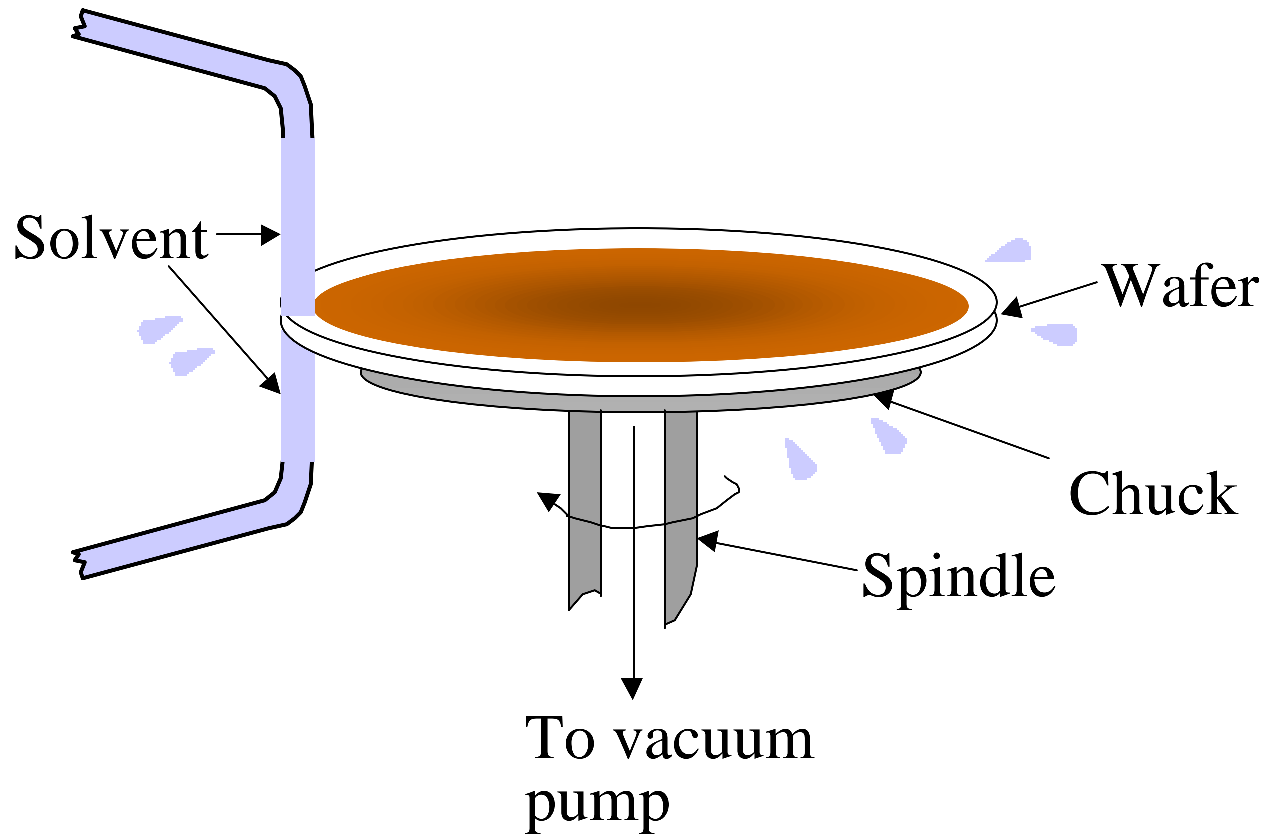
Edge Bead Removal (EBR)

- PR spread to the edges and backside
- PR could flakes off during mechanical handling and causes particles
- Front and back chemical EBR
- Front optical EBR

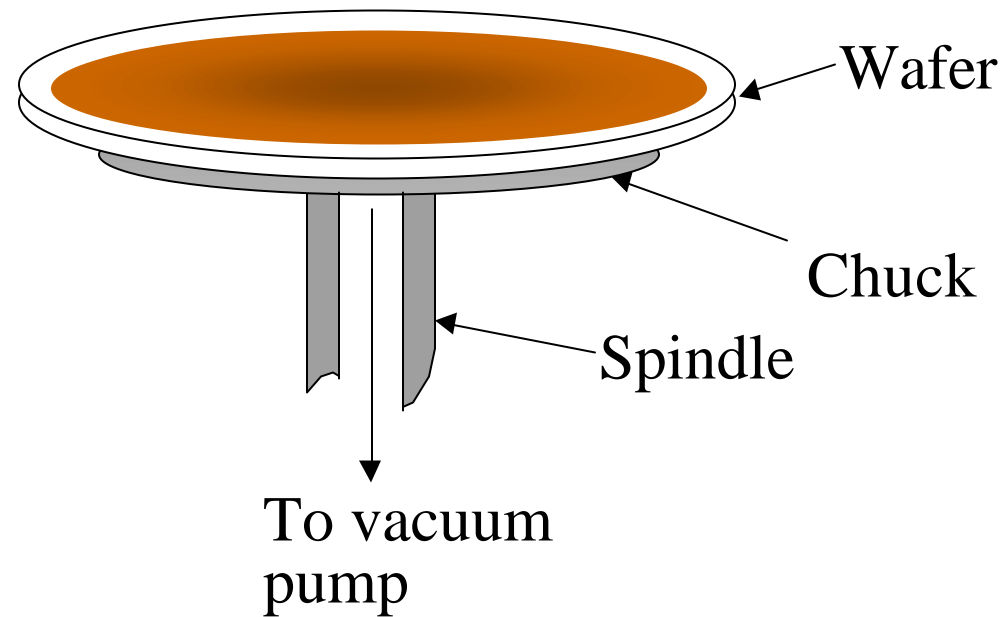
Edge Bead Removal



Edge Bead Removal



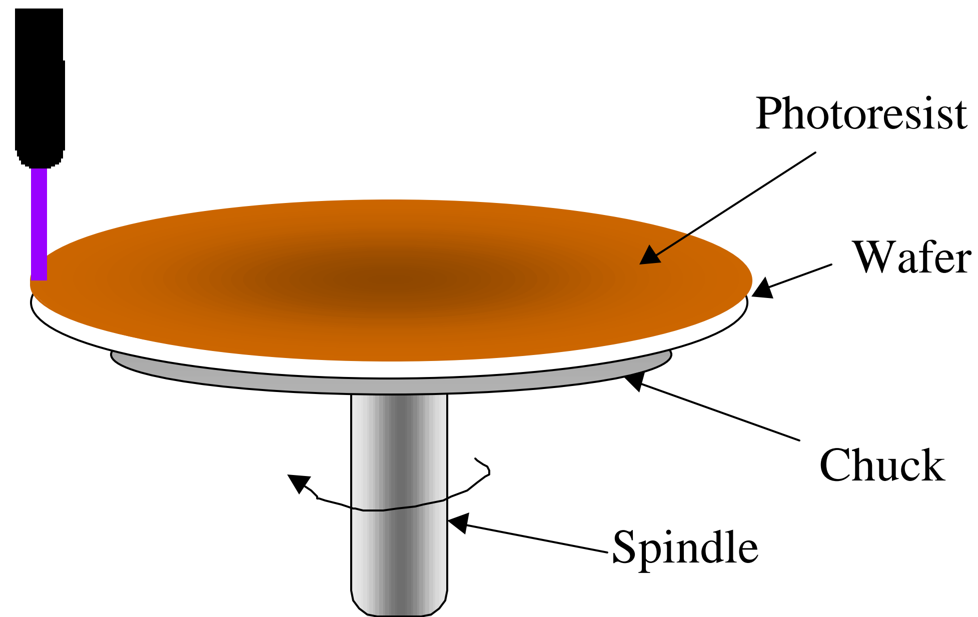
Ready For Soft Bake



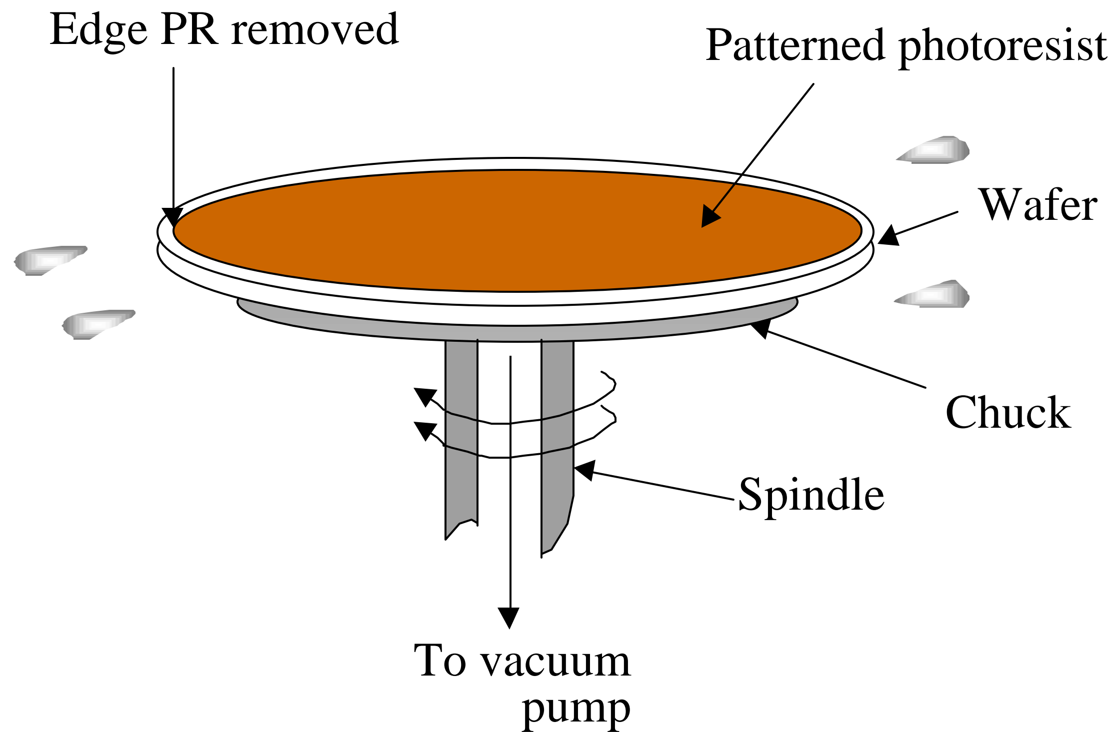
Optical Edge Bead Removal

- After alignment and exposure
- Wafer edge expose (WEE)
- Exposed photoresist at edge dissolves during development

Optical Edge Bead Removal



Developer Spin Off



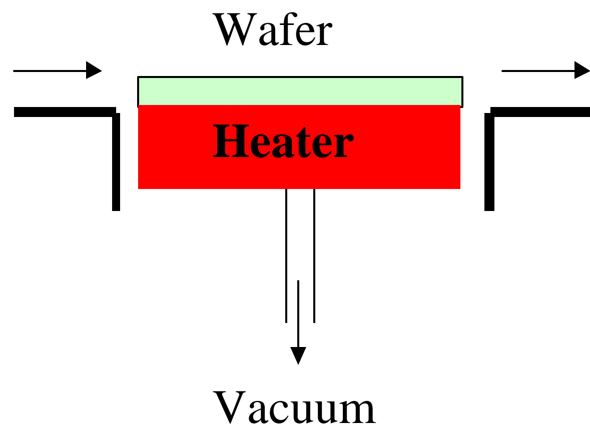
Soft Bake

- Evaporating most of solvents in PR
- Solvents help to make a thin PR but absorb radiation and affect adhesion
- Soft baking time and temperature are determined by the matrix evaluations
- Over bake: polymerized, less photo-sensitivity
- Under bake: affect adhesion and exposure

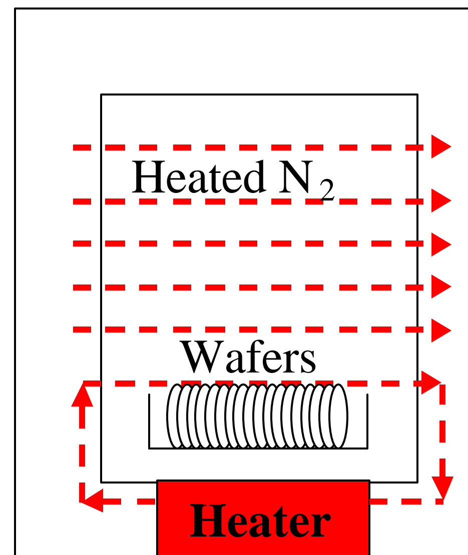
Soft Bake

- **Hot plates**
- Convection oven
- Infrared oven
- Microwave oven

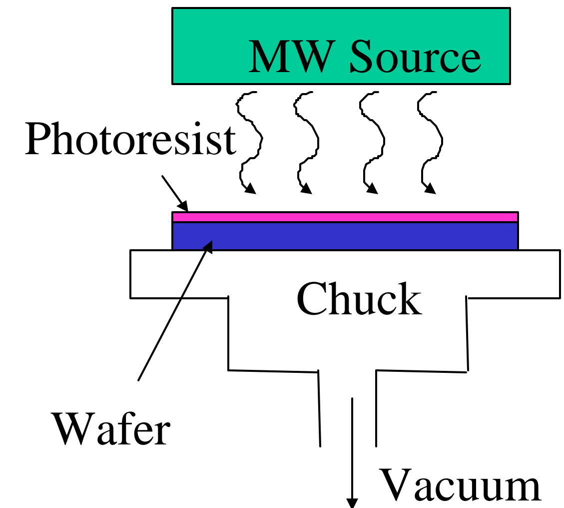
Baking Systems



Hot plate



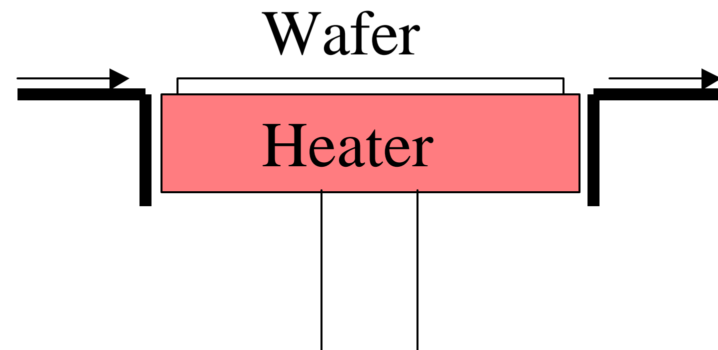
Convection oven



Microwave oven

Hot Plates

- Widely used in the industry
- Back side heating, no surface "crust"
- In-line track system



Wafer Cooling

- Need to cool down to ambient temperature
- Water-cooled chill plate
- Silicon thermal expansion rate: 2.5×10^{-6}/°C
- For 8 inch (200 mm) wafer, 1 °C change causes 0.5 μm difference in diameter

Alignment and Exposure

- Most critical process for IC fabrication
- Most expensive tool (stepper) in an IC fab.
- Most challenging technology
- Determines the minimum feature size
- Currently 0.18 μm and pushing to 0.13 μm

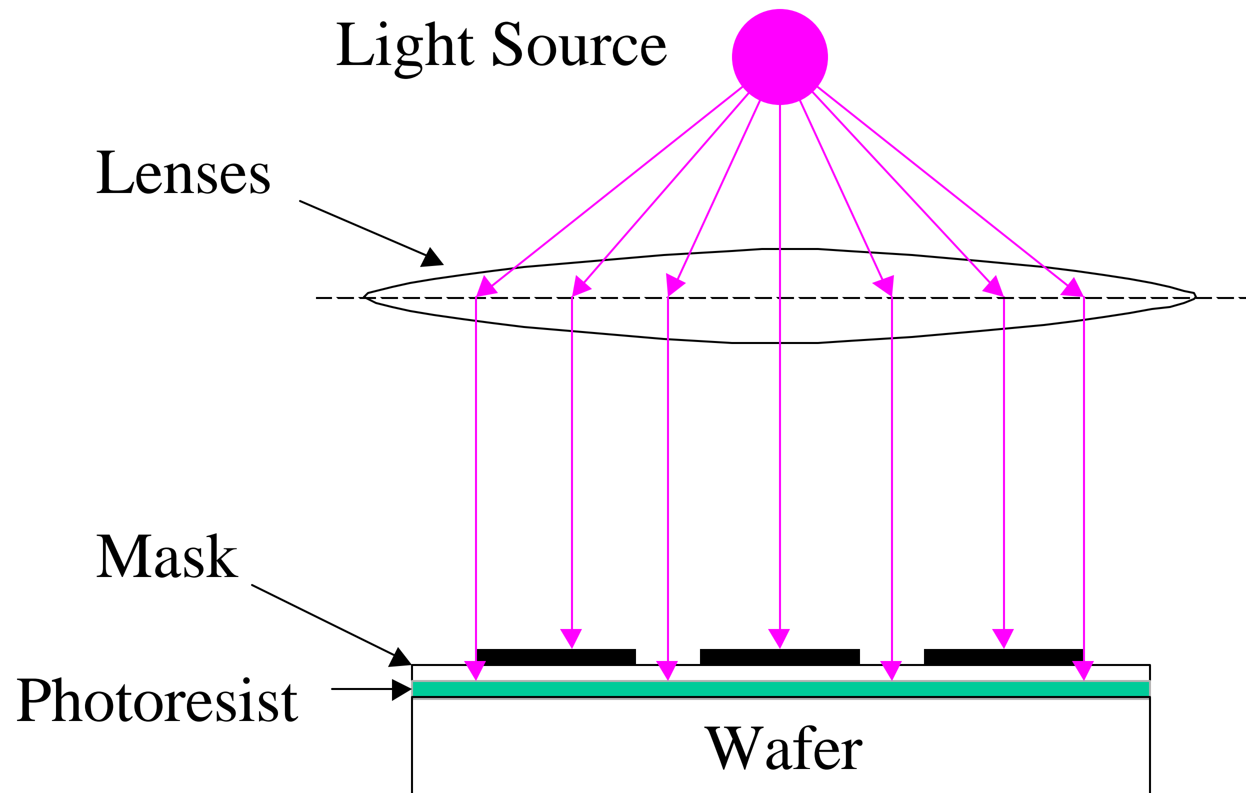
Alignment and Exposure Tools

- Contact printer
- Proximity printer
- Projection printer
- Stepper

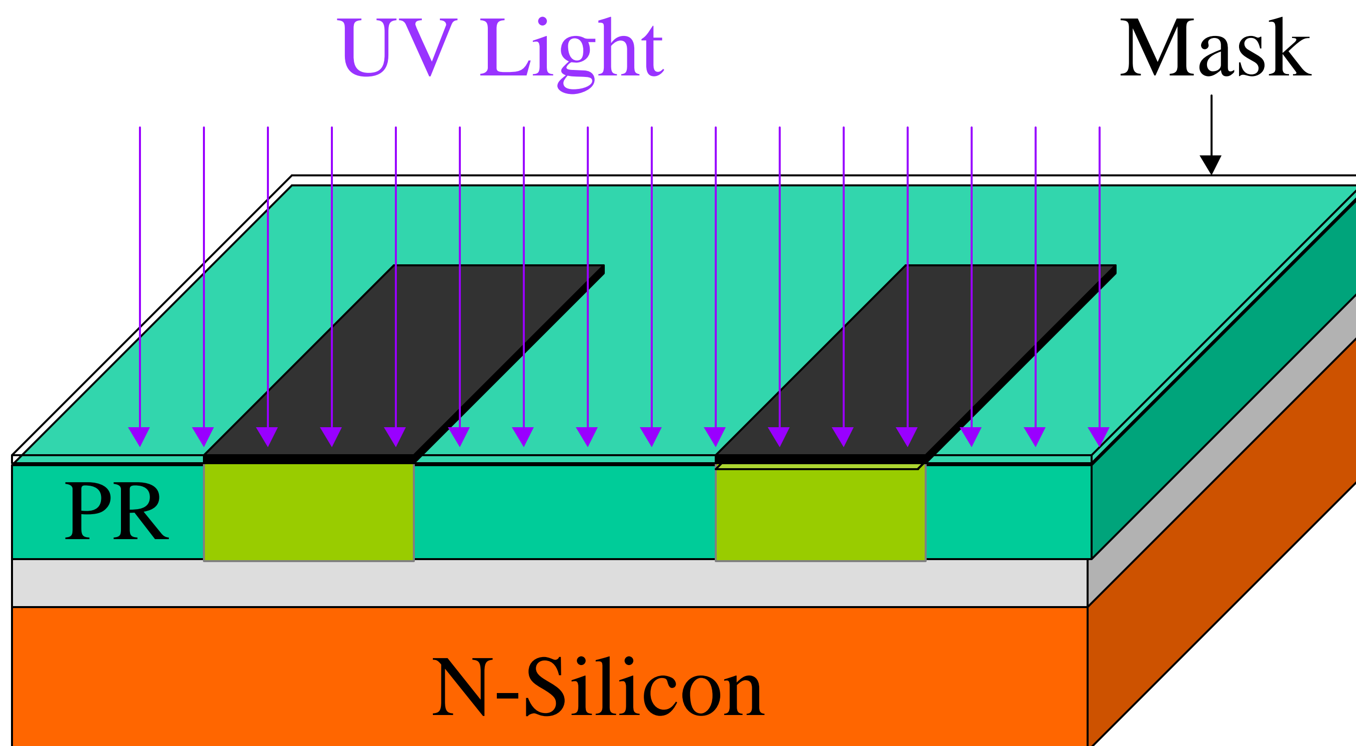
Contact Printer

- Simple equipment
- Use before mid-70s
- Resolution: capable for sub-micron
- Direct mask-wafer contact, limited mask lifetime
- Particles

Contact Printer



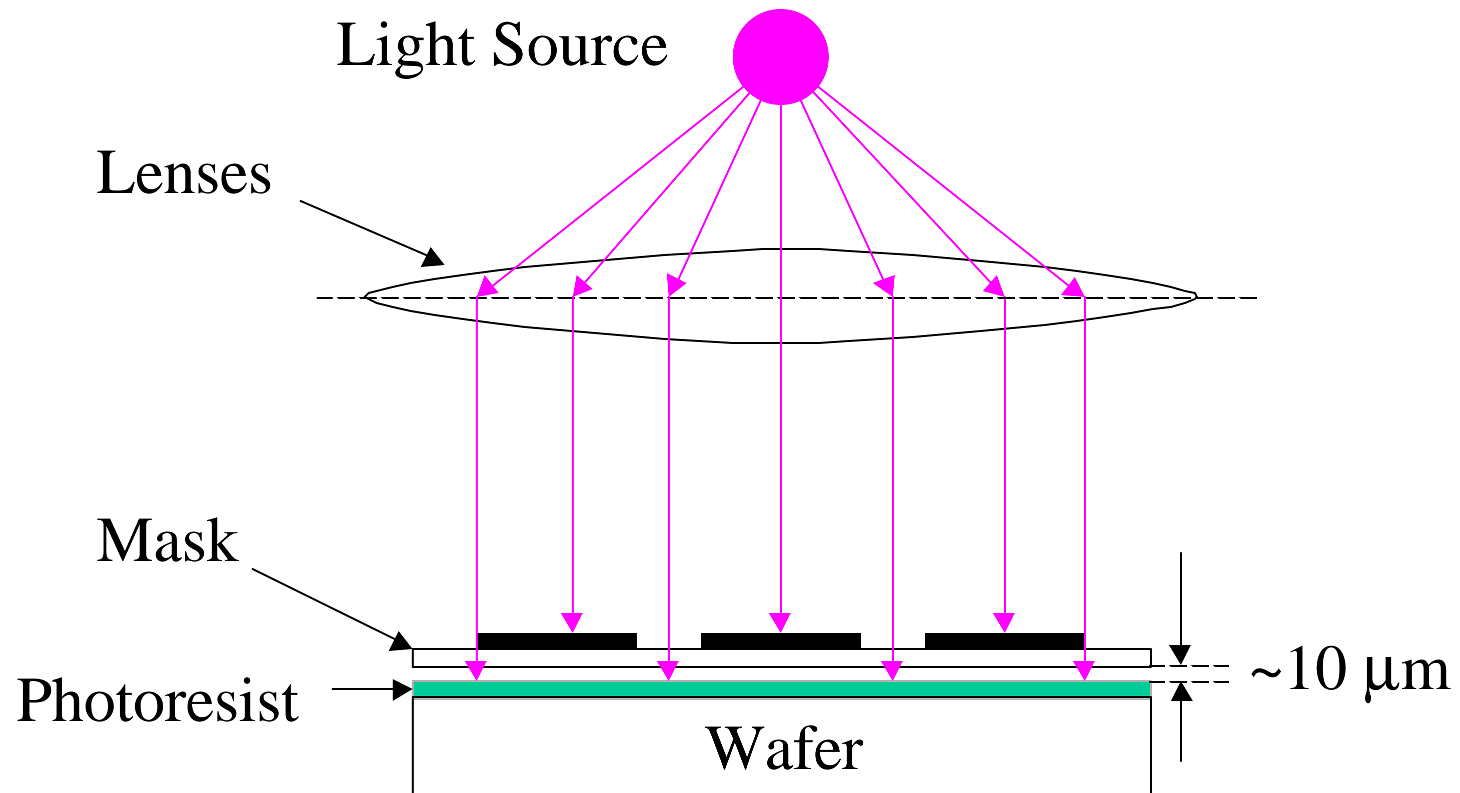
Contact Printing



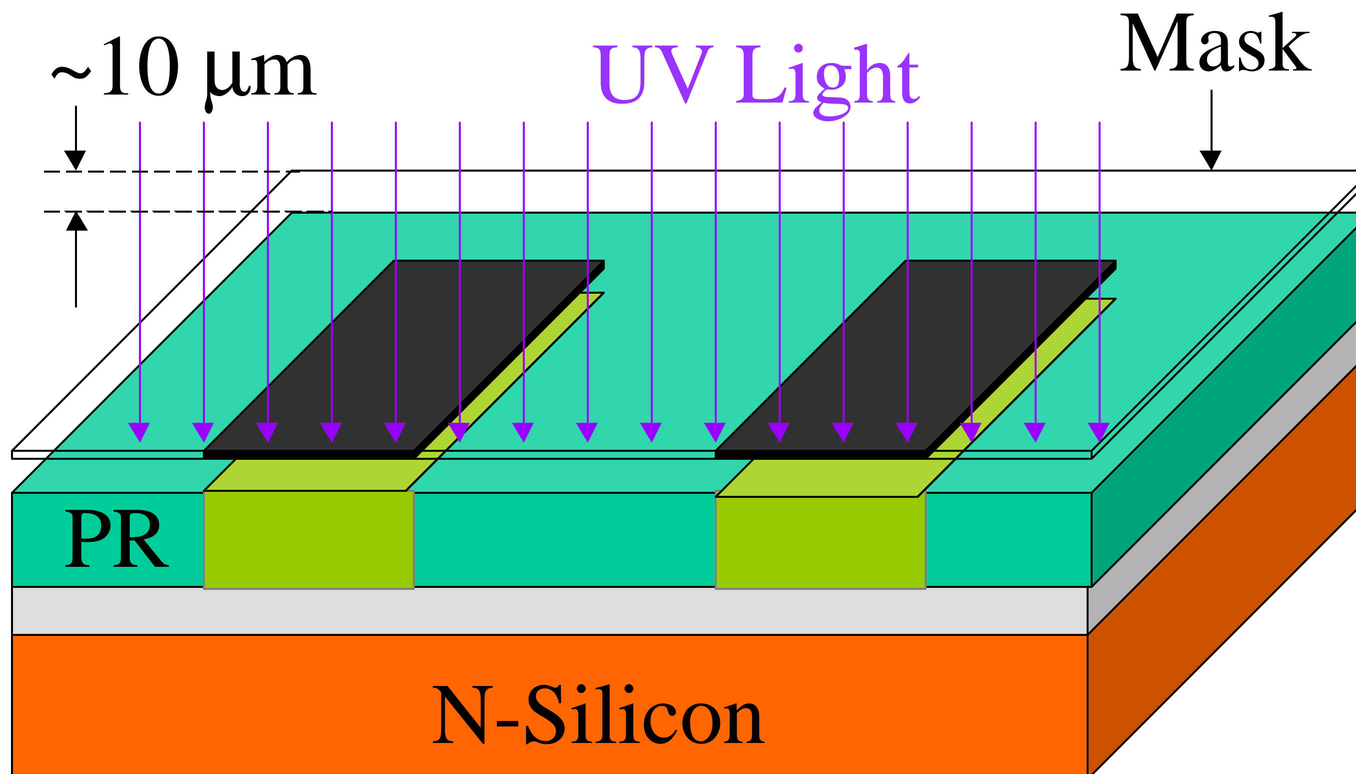
Proximity Printer

- ~ 10 μm from wafer surface
- No direct contact
- Longer mask lifetime
- Resolution: > 3 μm

Proximity Printer



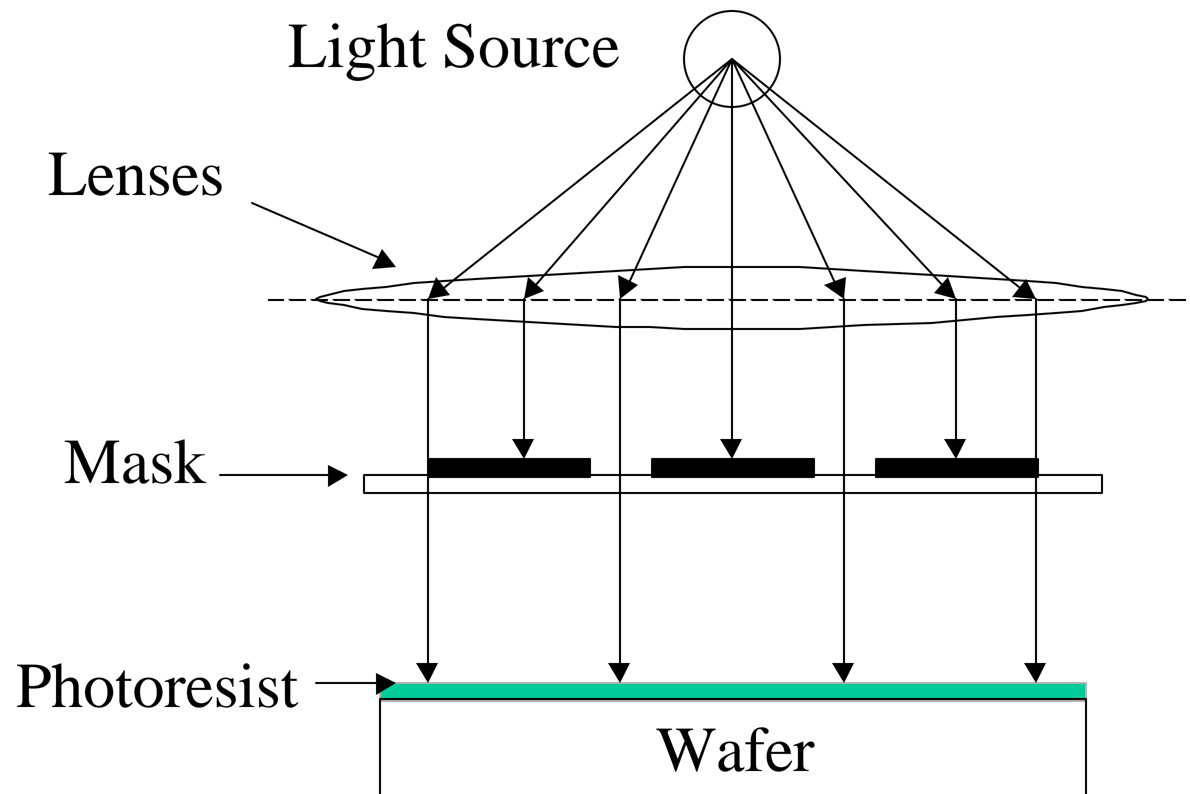
Proximity Printing



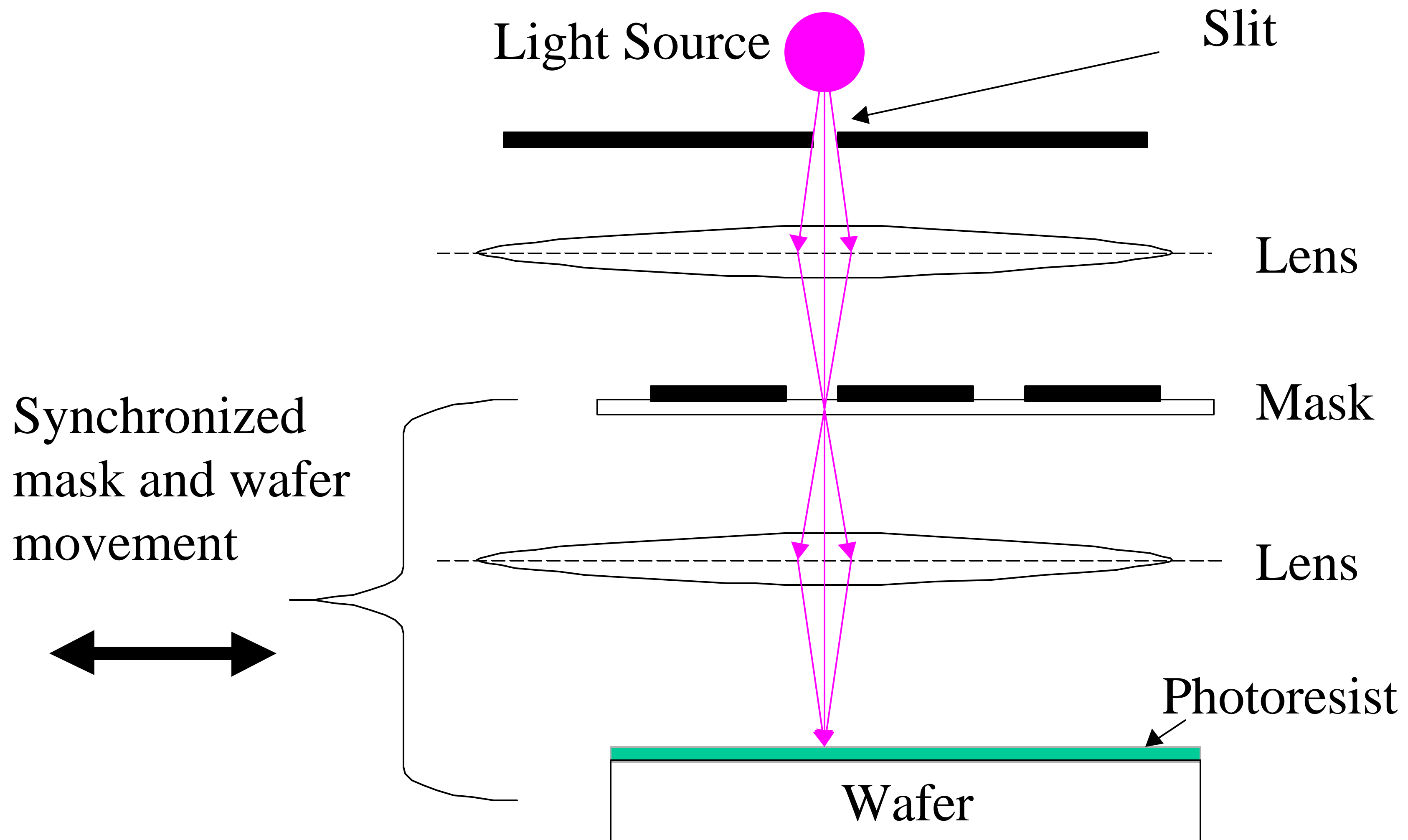
Projection Printer

- Works like an overhead projector
- Mask to wafer, 1:1
- Resolution to about 1 μm

Projection System



Scanning Projection System



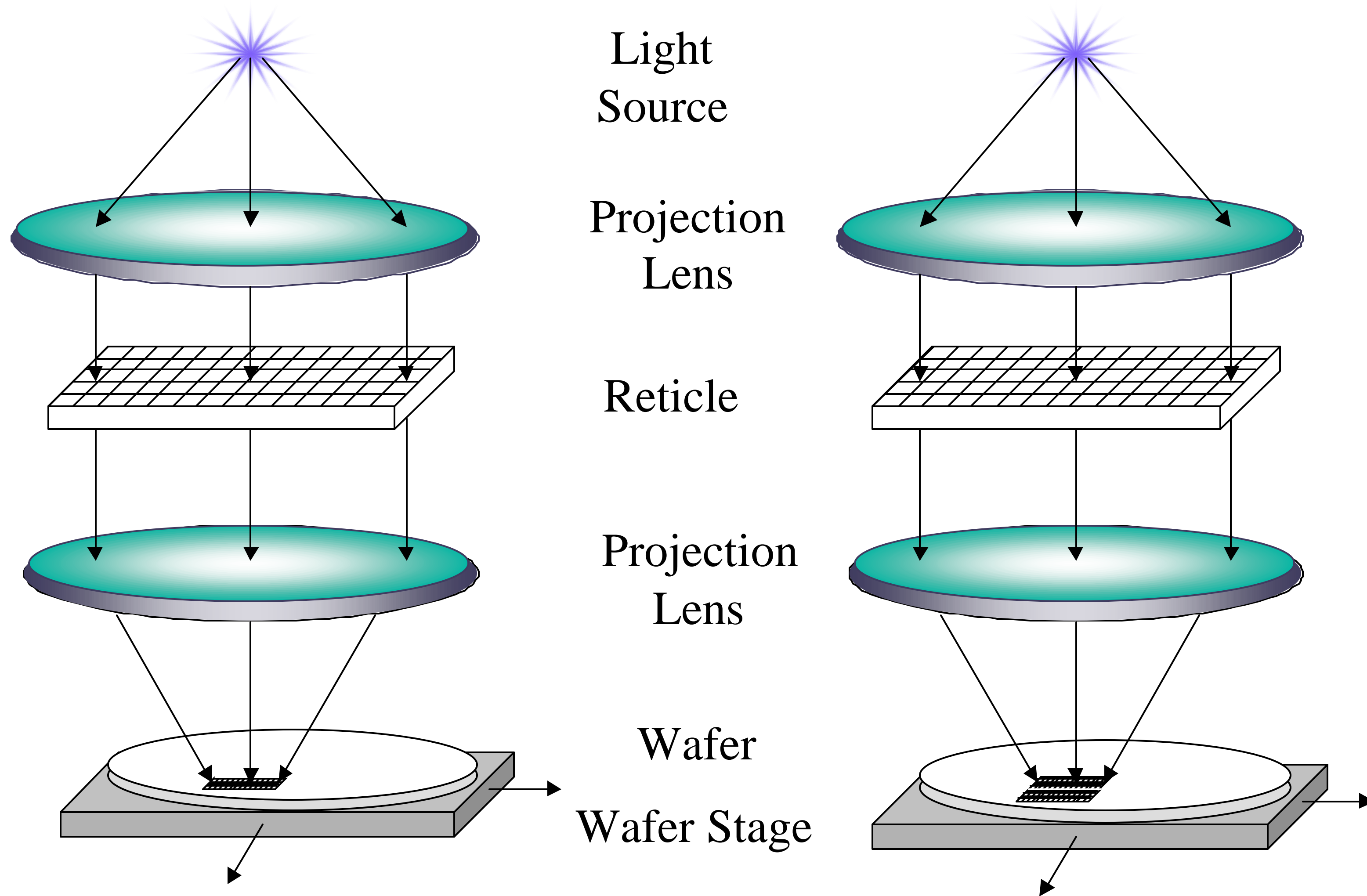
Stepper

- Most popular used photolithography tool in the advanced IC fabs
- Reduction of image gives high resolution
- 0.25 μm and beyond
- Very expensive

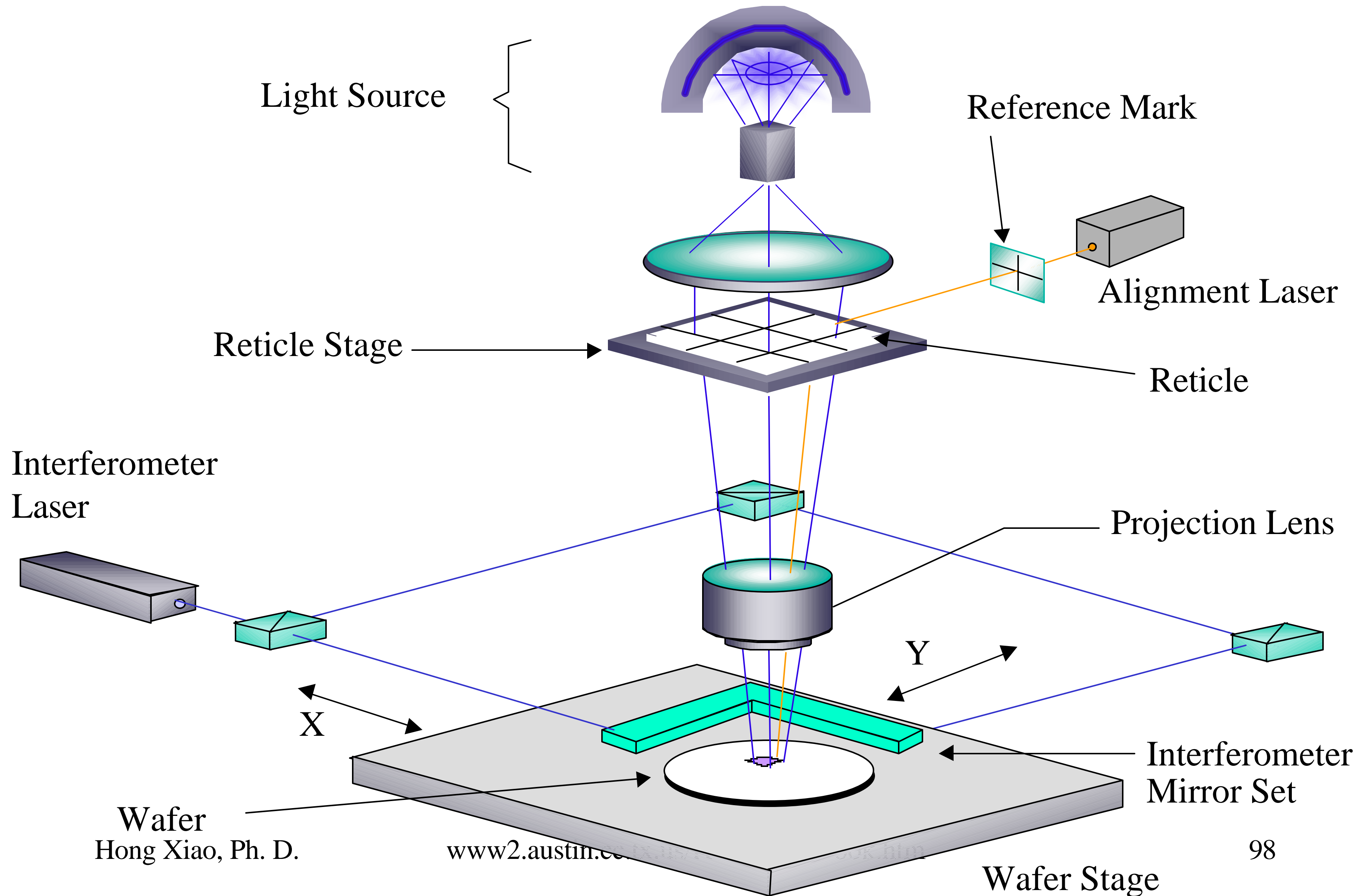
Q & A

- Why does the 5:1 shrink ratio is more popular than the 10:1 shrink ratio?
- 10:1 image shrink has better resolution than 5:1 image shrink. However, it only exposes a quarter of the area, which means total exposure time will be quadrupled.

Step-&-Repeat Alignment/Exposure



Step&Repeat Alignment System

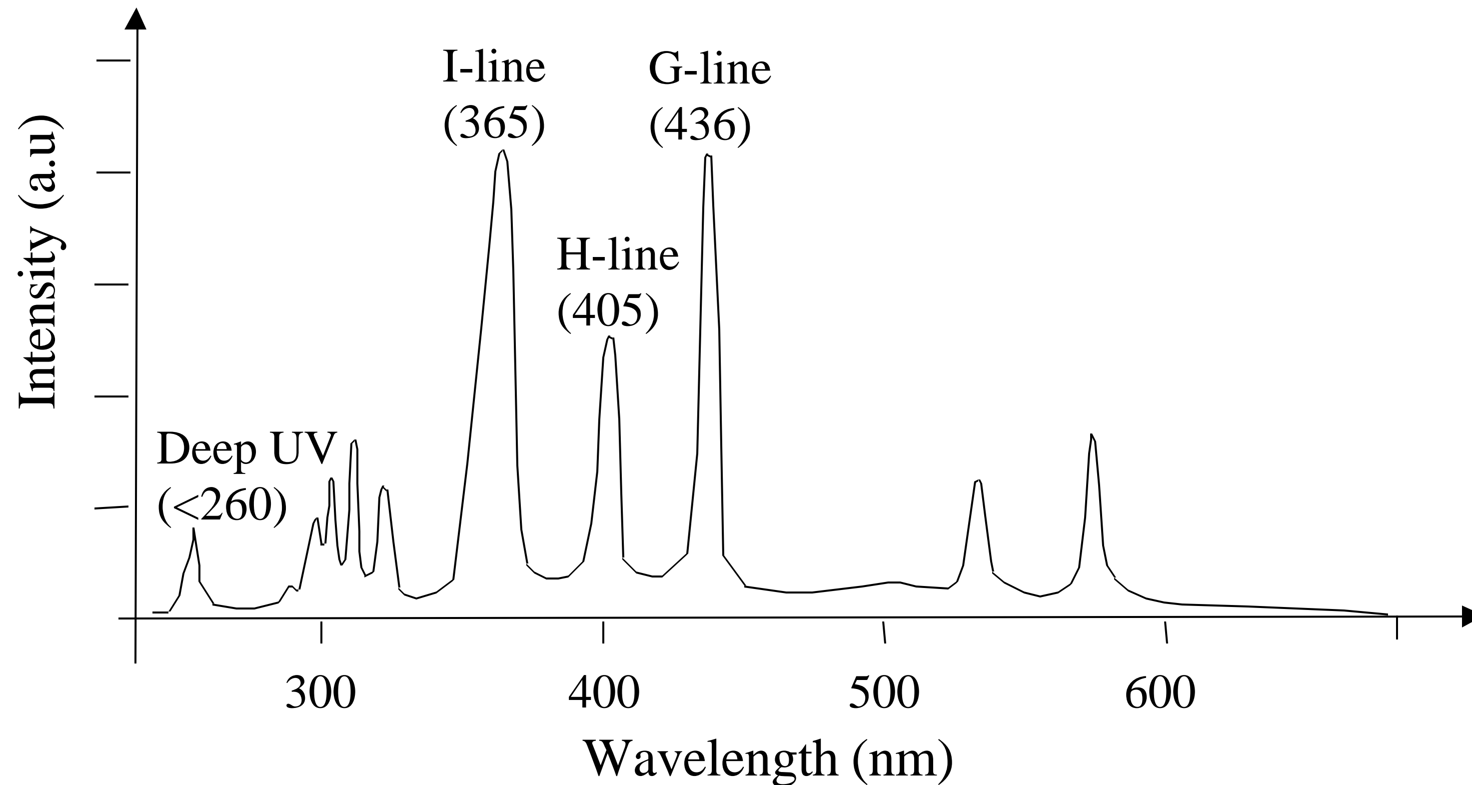


Exposure Light Source

- Short wavelength
- High intensity
- Stable

- High-pressure mercury lamp
- Excimer laser

Spectrum of the Mercury Lamp



Photolithography Light Sources

	Name	Wavelength (nm)	Application feature size (μm)
Mercury Lamp	G-line	436	0.50
	H-line	405	
	I-line	365	0.35 to 0.25
Excimer Laser	XeF	351	
	XeCl	308	
	KrF (DUV)	248	0.25 to 0.15
	ArF	193	0.18 to 0.13
Fluorine Laser	F_2	157	0.13 to 0.1

Exposure Control

- Exposure controlled by production of light intensity and exposure time
- Very similar to the exposure of a camera
- Intensity controlled by electrical power
- Adjustable light intensity
- Routine light intensity calibration

Question

- Someone did a routine illuminator intensity calibration with a reticle still on the stage. What kind of problem will it induce?

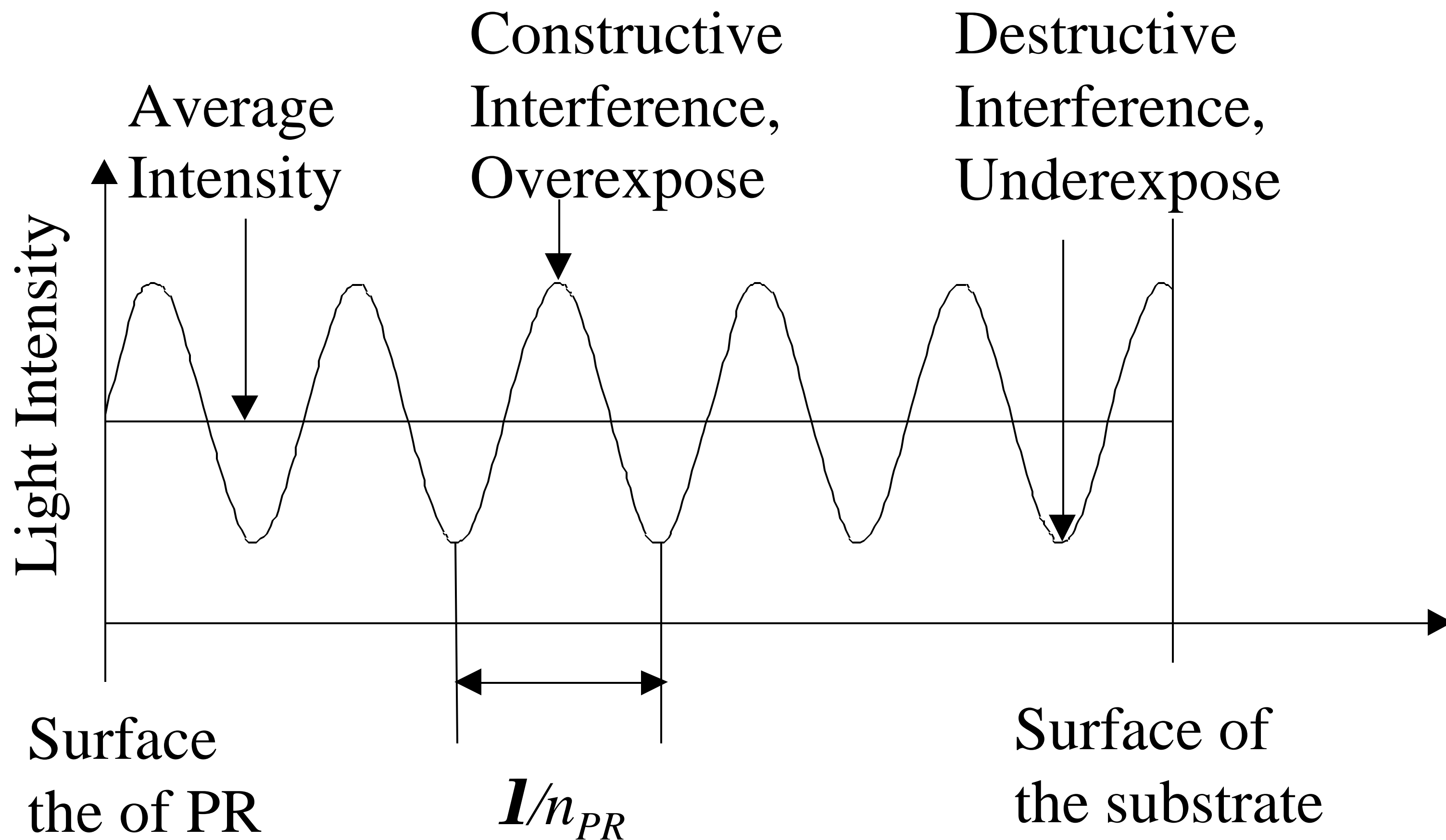
Answer

- Since the reticle can block some light, photodetector on wafer stage will receive less photons than it should receive. Therefore, it will give a lower reading. To calibrate, the applied power will be increased and the light intensity will be higher than it should be. It could cause overexposure and CD loss.

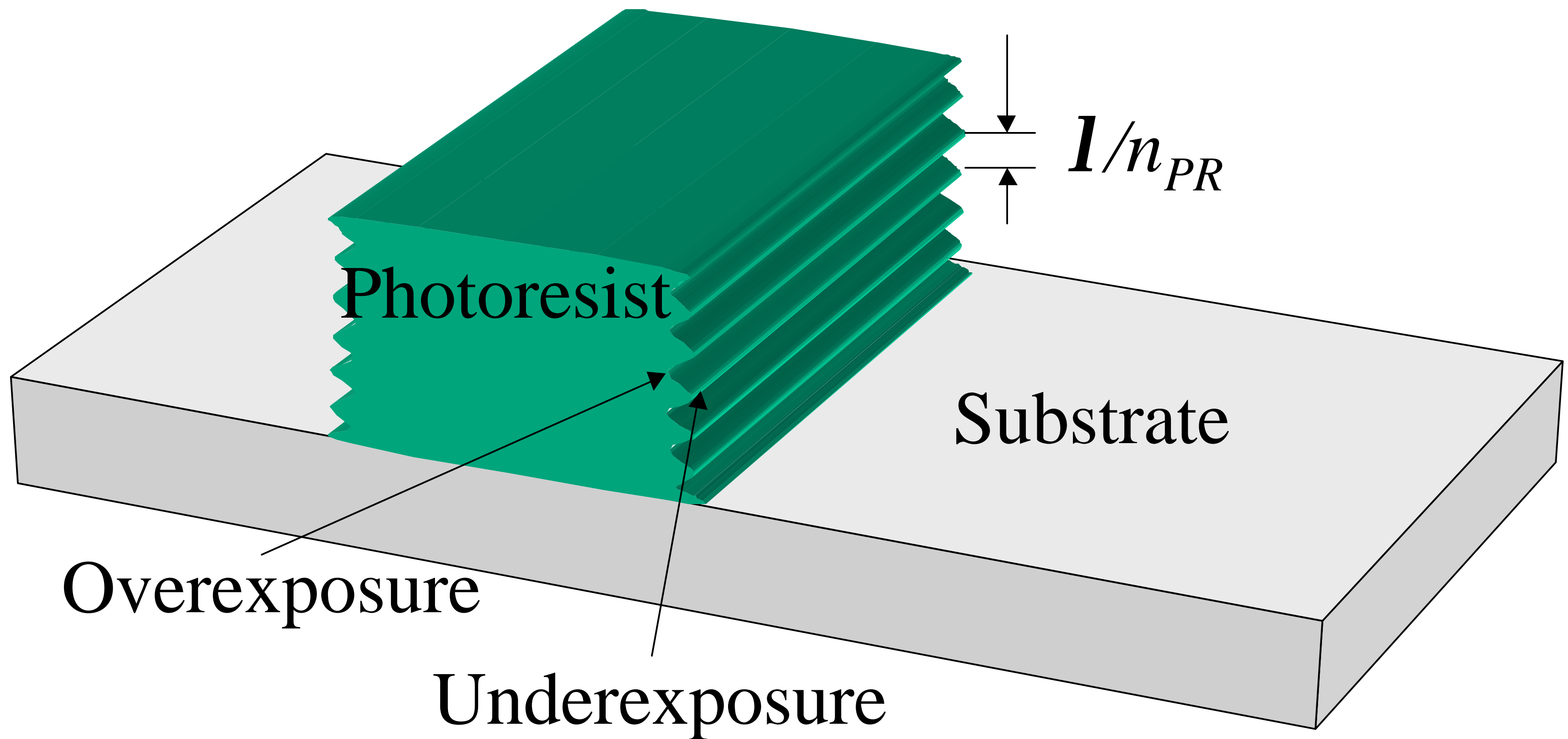
Standing Wave Effect

- Interference of the incident and reflection lights
- Periodically overexposure and underexposure
- Affects photolithography resolution.

Standing Wave Intensity



Standing Wave Effect on Photoresist



Post Exposure Bake

- Photoresist glass transition temperature T_g
- Baking temperature higher than T_g
- Thermal movement of photoresist molecules
- Rearrangement of the overexposed and underexposed PR molecules
- Average out standing wave effect,
- Smooth PR sidewall and improve resolution

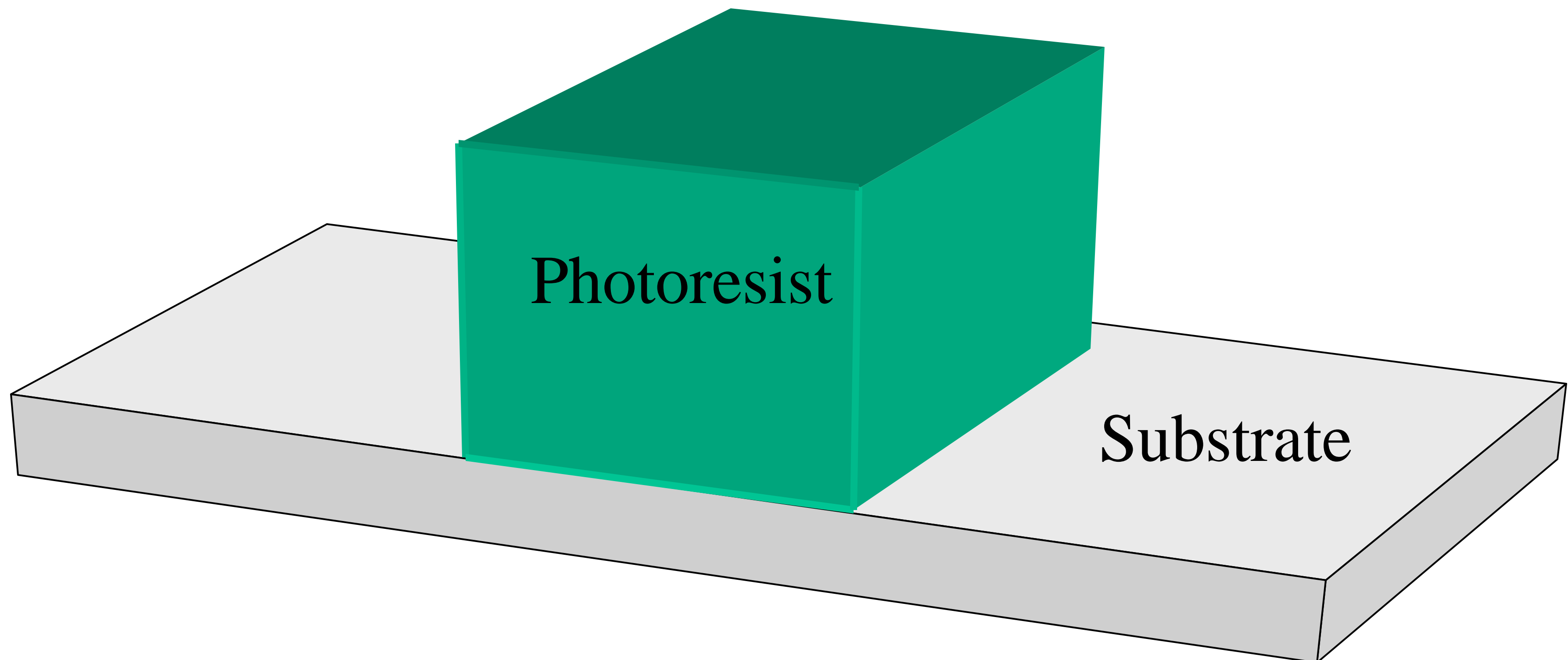
Post Exposure Bake

- For DUV chemical amplified photoresist, PEB provides the heat needed for acid diffusion and amplification.
- After the PEB process, the images of the exposed areas appear on the photoresist, due to the significant chemical change after the acid amplification

Post Exposure Bake

- PEB normally uses hot plate at 110 to 130 °C for about 1 minute.
- For the same kind of PR, PEB usually requires a higher temperature than soft bake.
- Insufficient PEB will not completely eliminate the standing wave pattern,
- Over-baking will cause polymerization and affects photoresist development

PEB Minimizes Standing Wave Effect



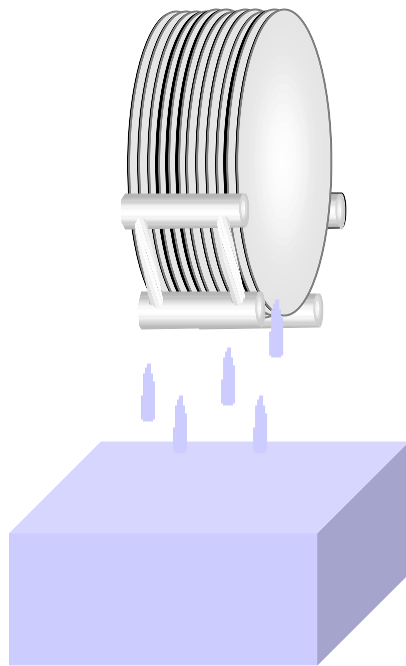
Wafer Cooling

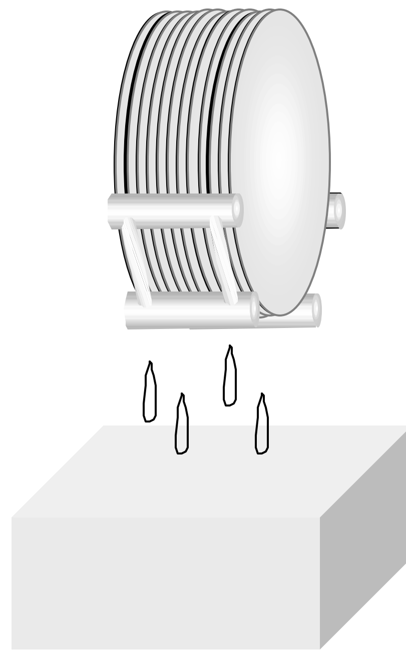
- After PEB the wafer is put on a chill plate to cool down to the ambient temperature before sent to the development process
- High temperature can accelerate chemical reaction and cause over-development,
- PR CD loss

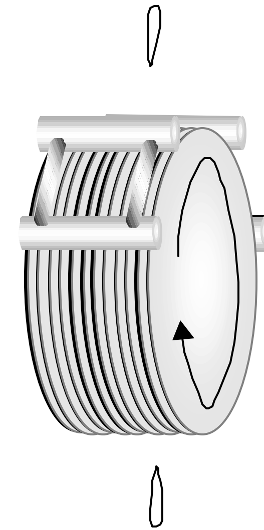
Development

- Developer solvent dissolves the softened part of photoresist
- Transfer the pattern from mask or reticle to photoresist
- Three basic steps:
  - Development
  - Rinse
  - Dry

Development: Immersion







Develop

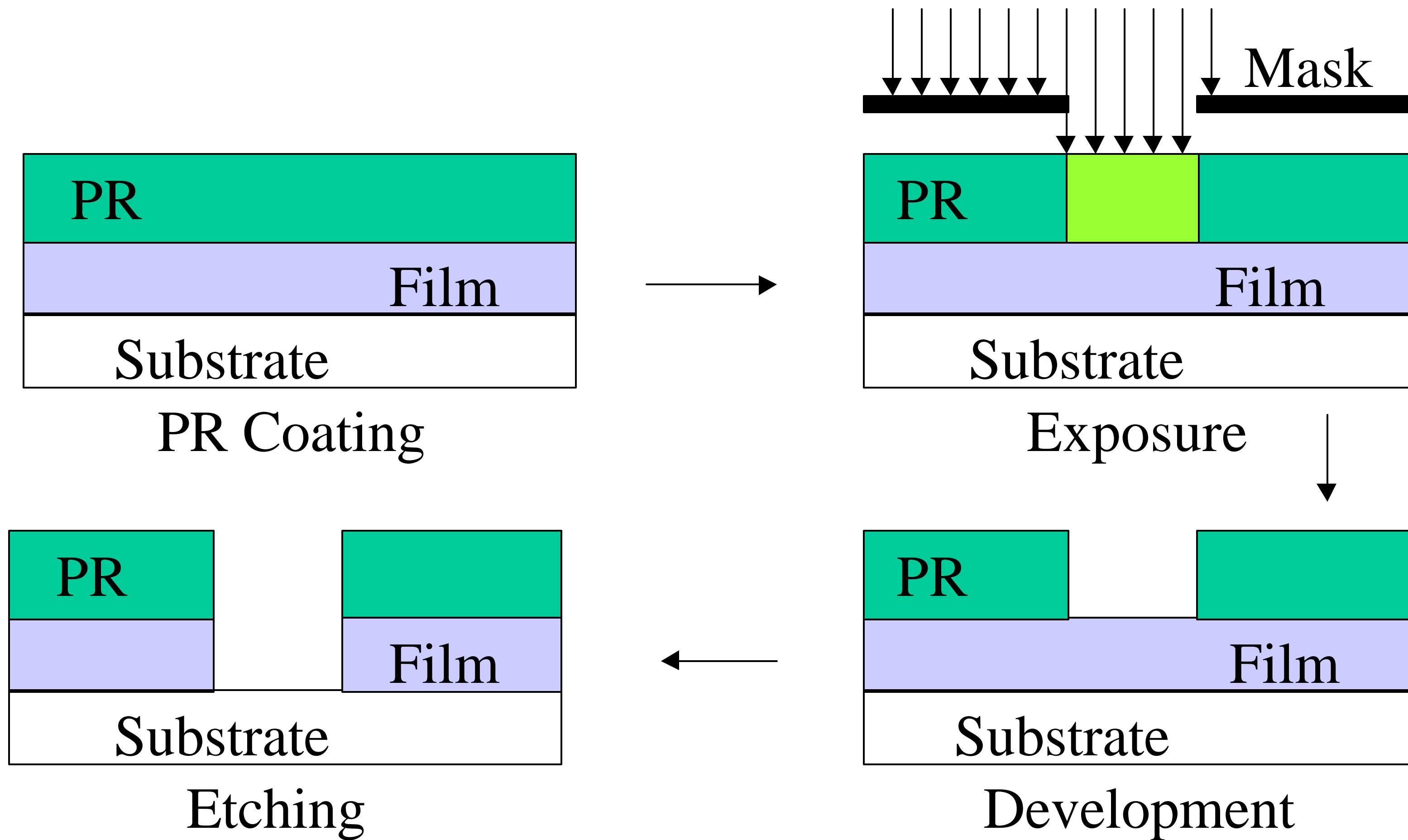
Rinse

Spin Dry

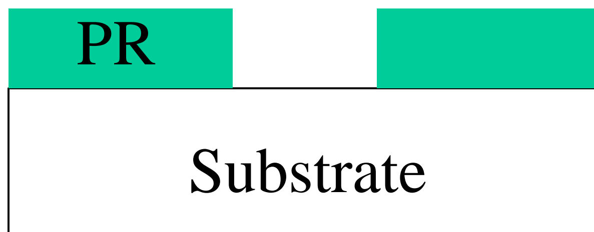
Developer Solution

- +PR normally uses weak base solution
- The most commonly used one is the tetramethyl ammonium hydride, or TMAH ($(CH_3)_4NOH$).

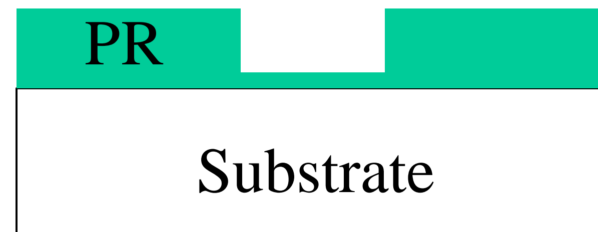
Development



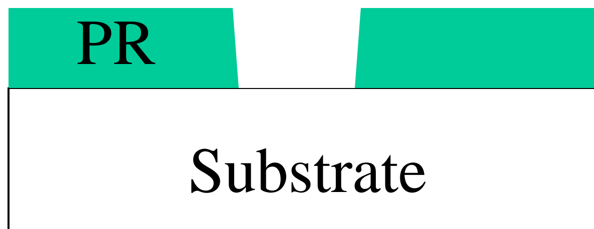
Development Profiles



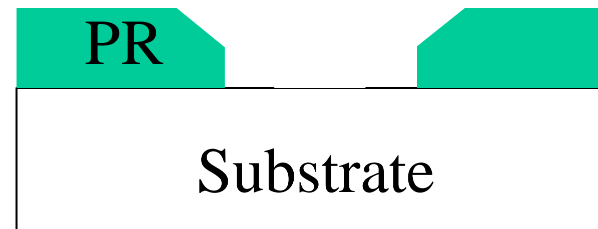
Normal Development



Incomplete Development



Under Development

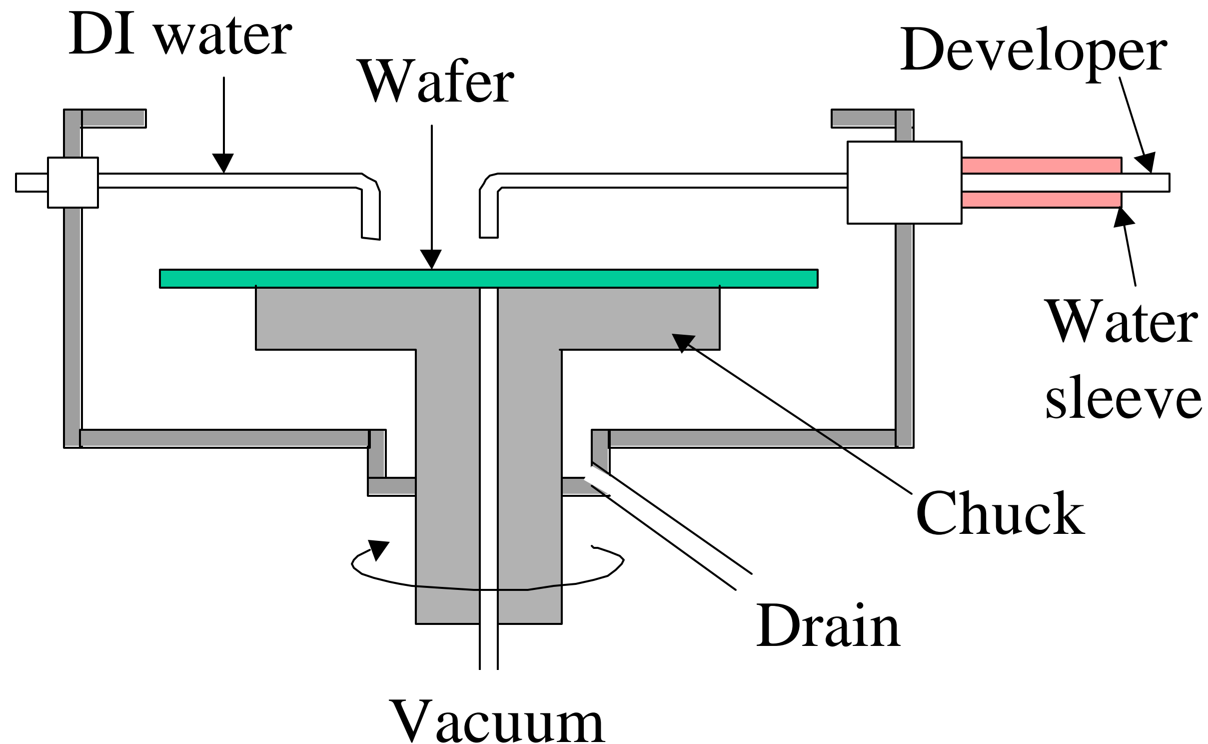


Over Development

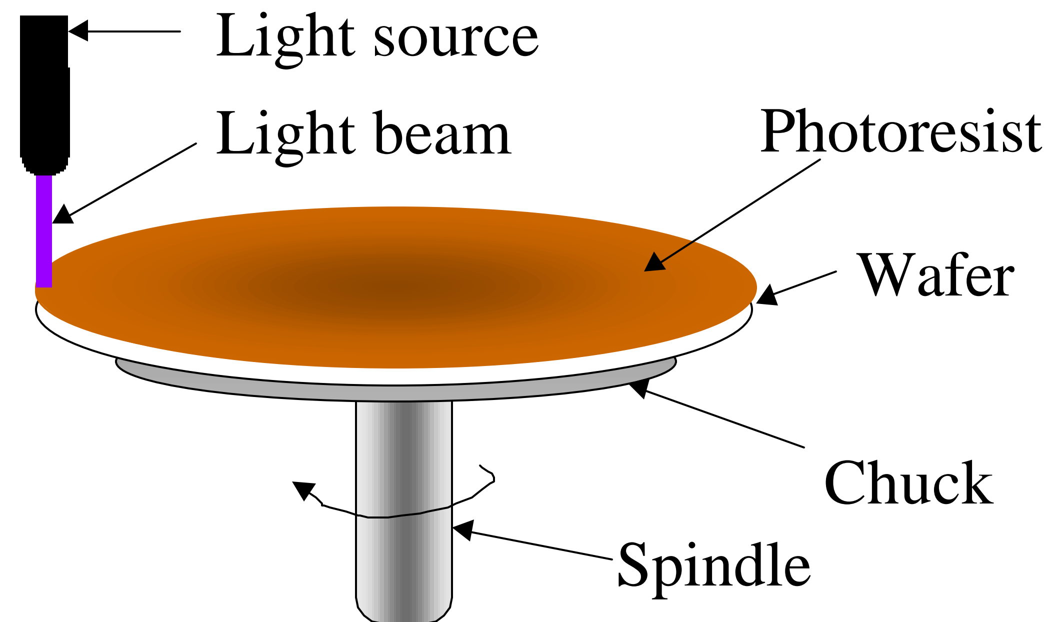
Developer Solutions

	Positive PR	Negative PR
Developer	TMAH	Xylene
Rinse	DI Water	n-Butylacetate

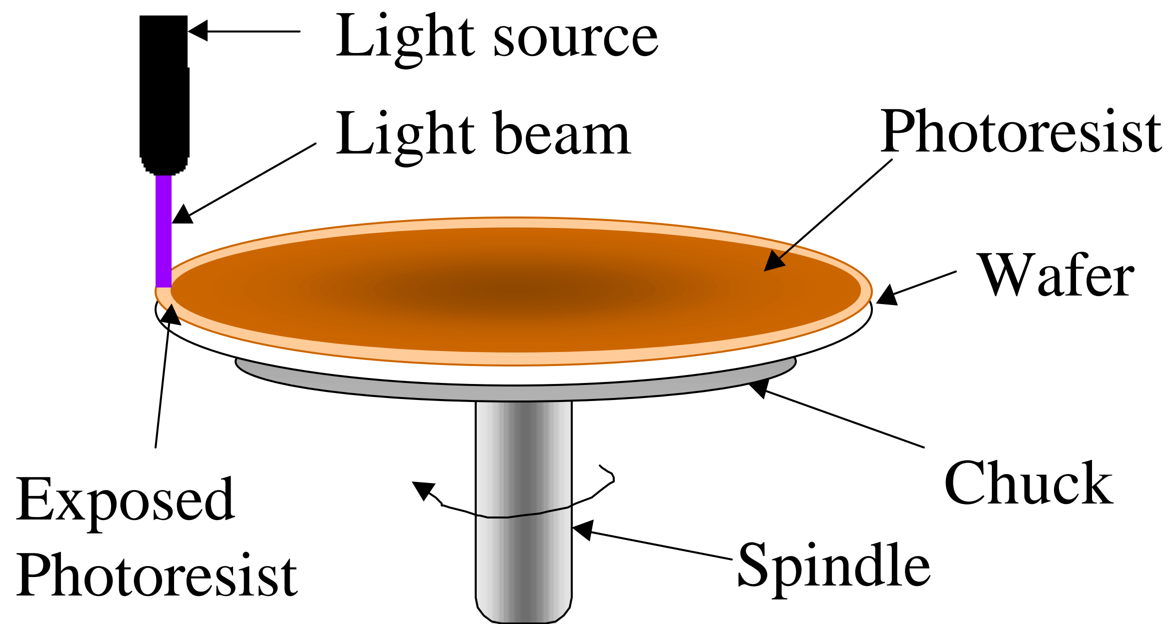
Schematic of a Spin Developer



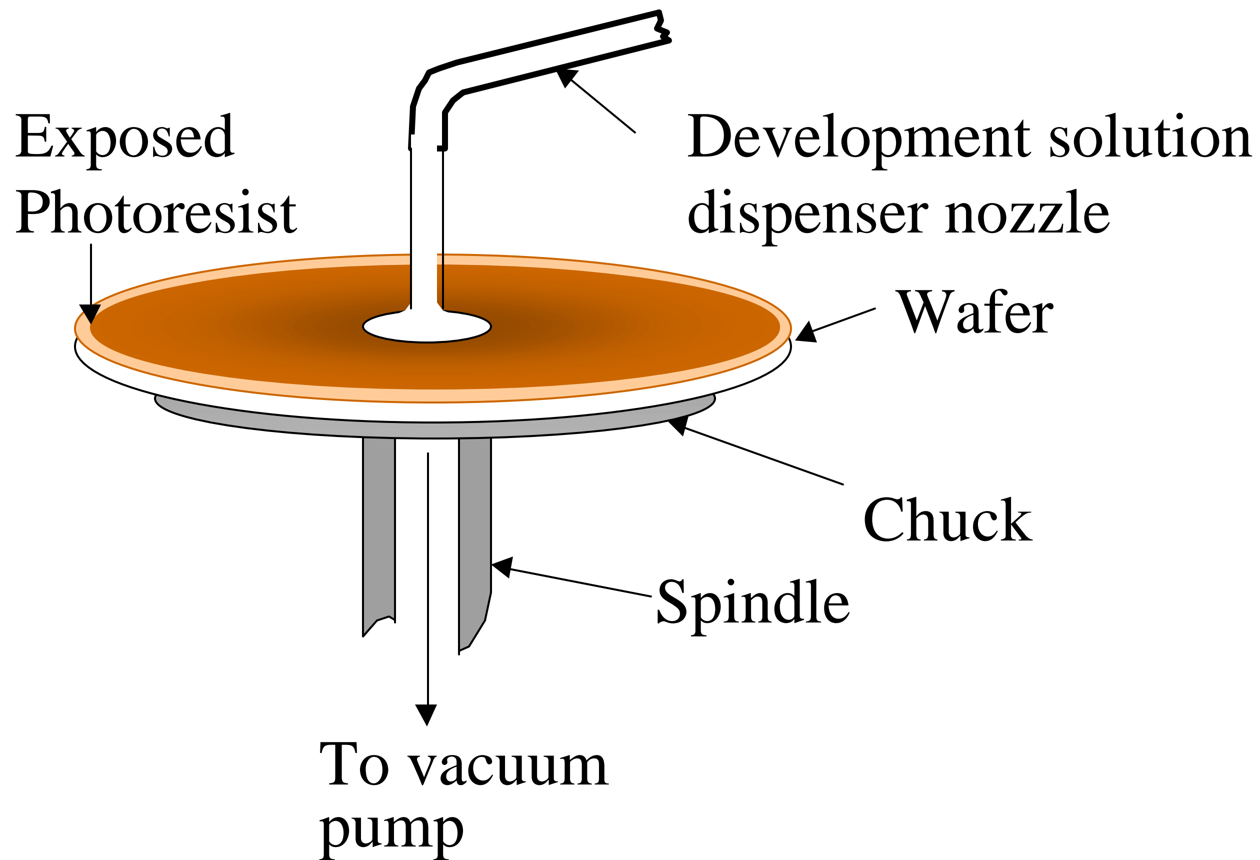
Optical Edge Bead Removal Exposure



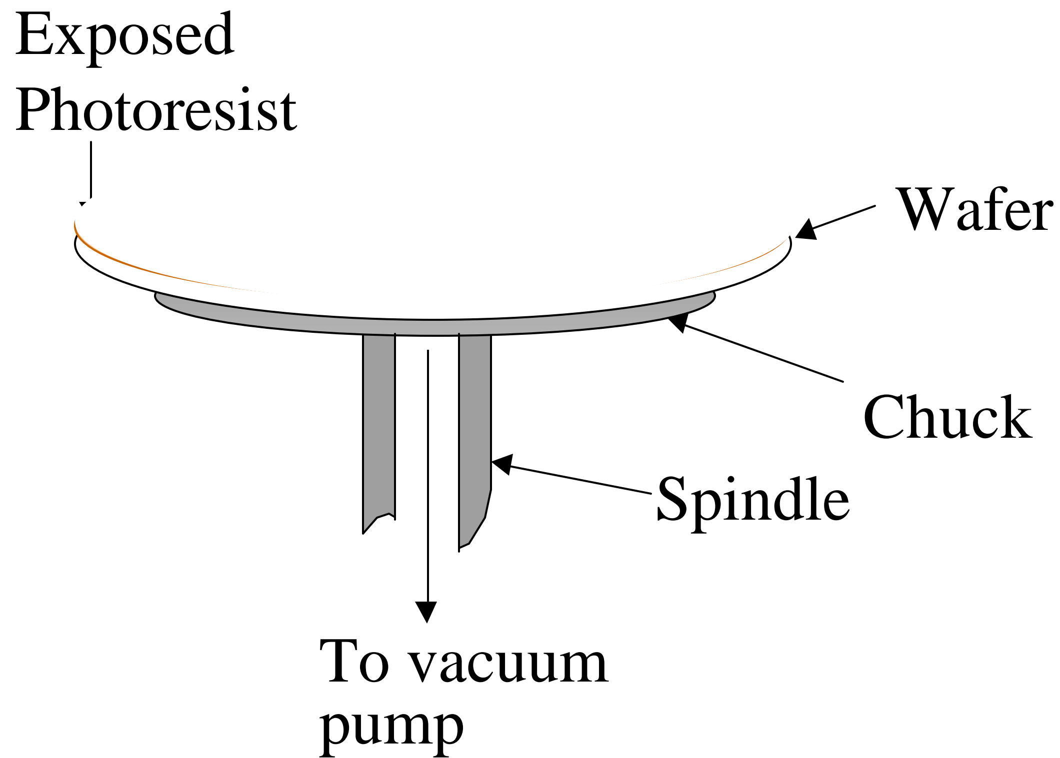
Optical Edge Bead Removal Exposure



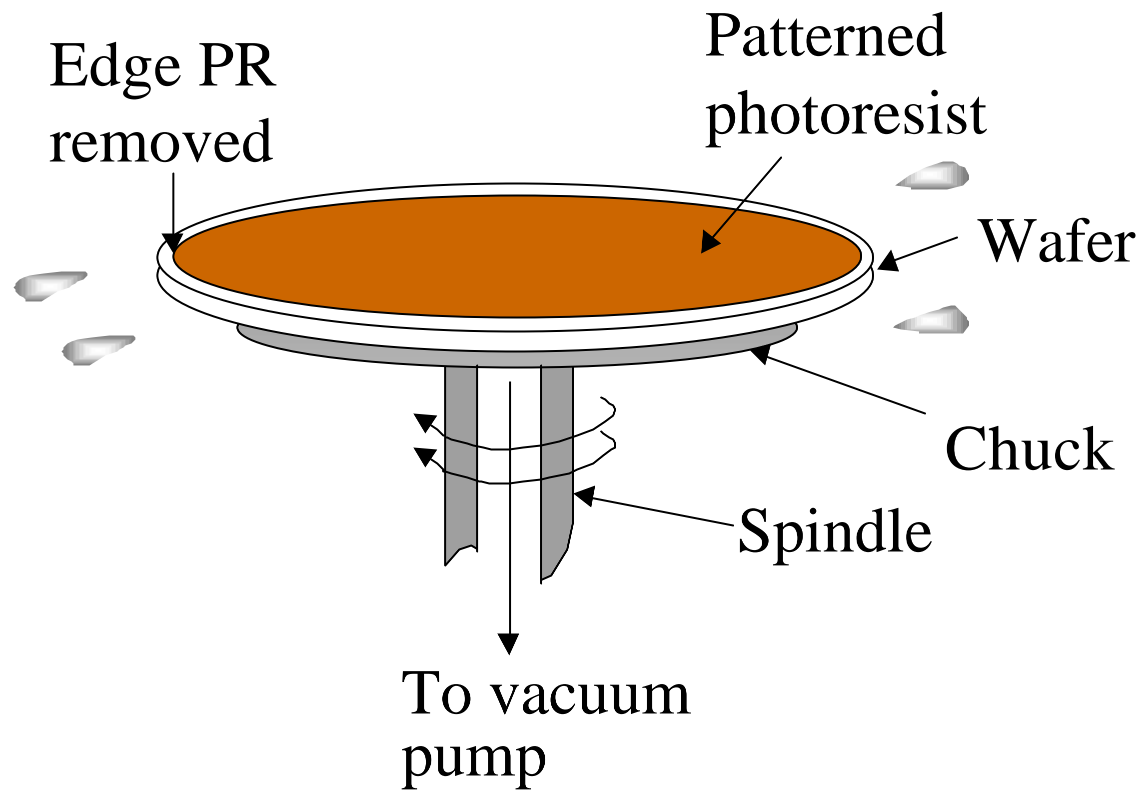
Applying Development Solution



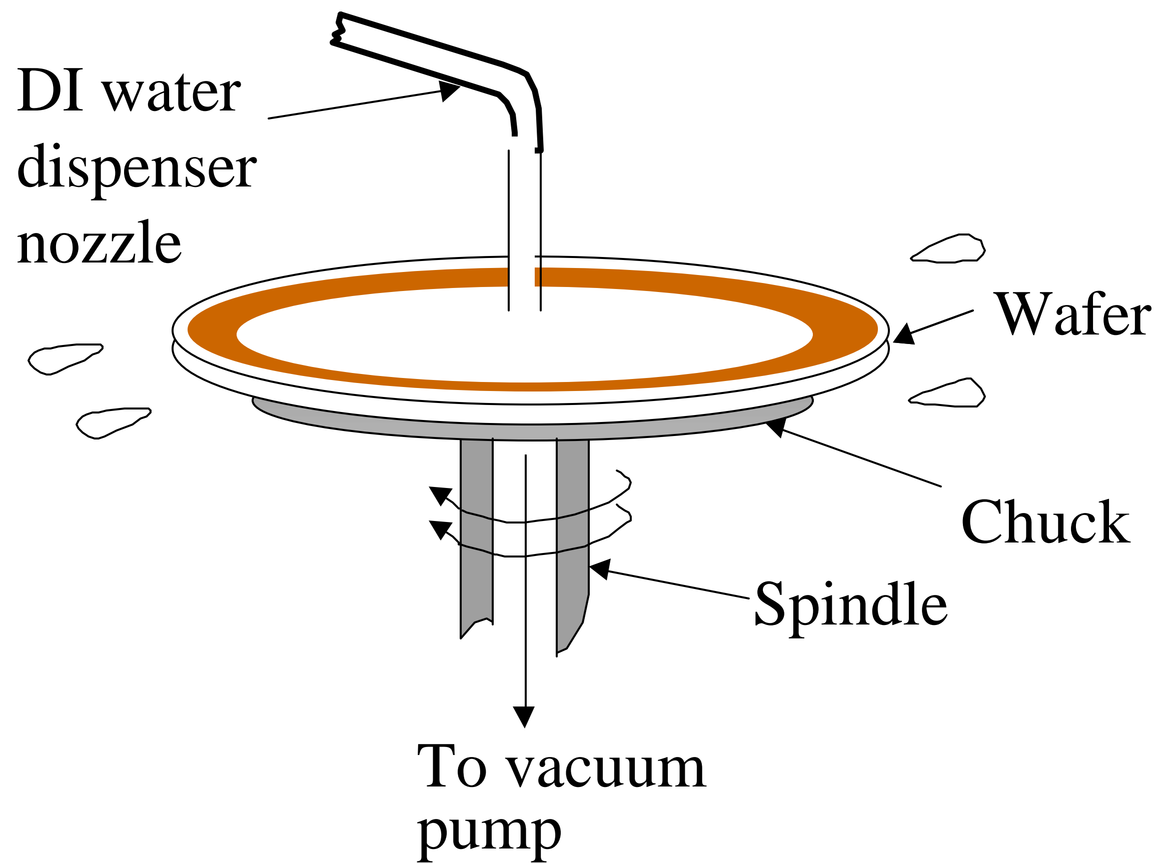
Applying Development Solution



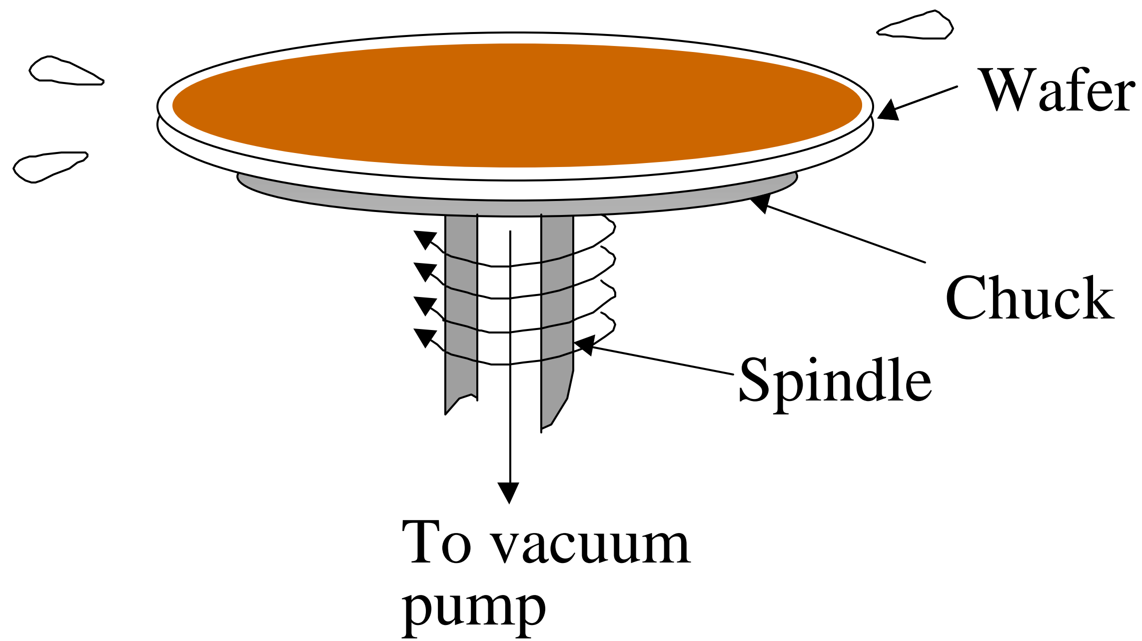
Development Solution Spin Off



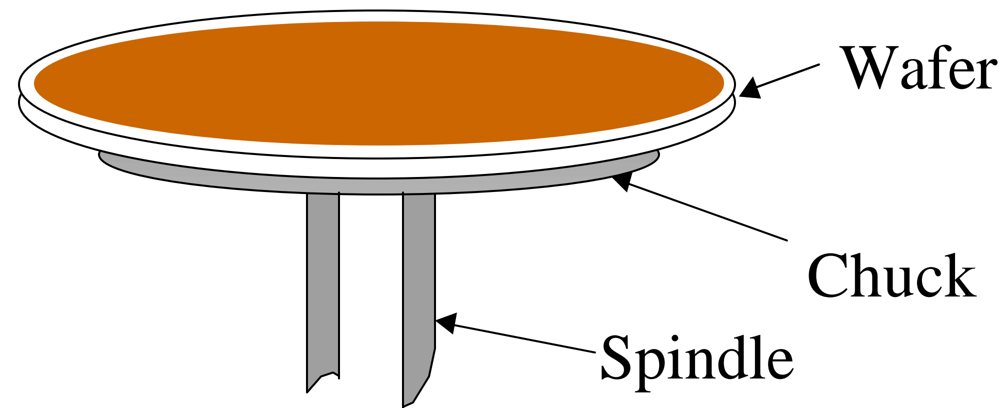
DI Water Rinse



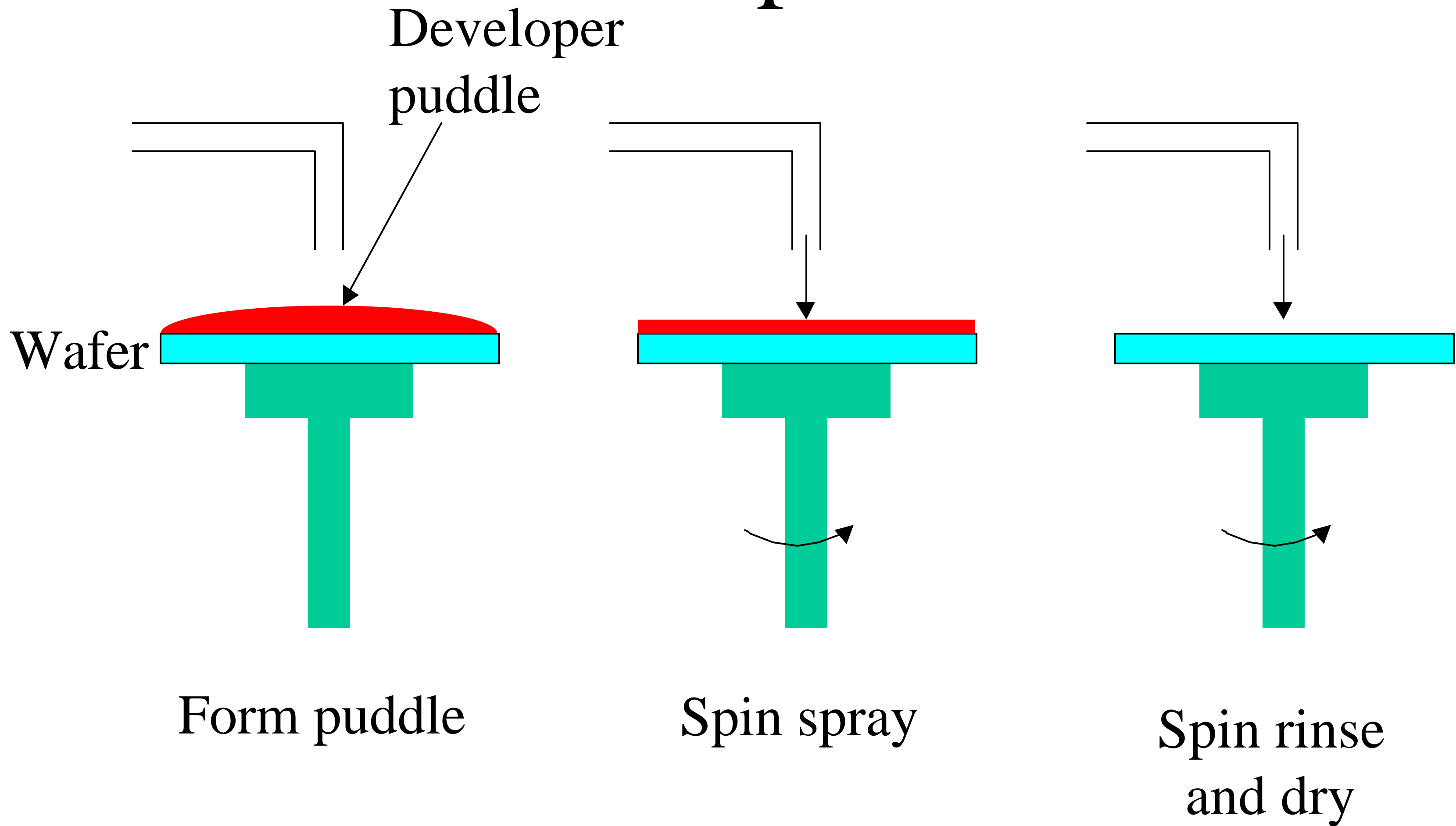
Spin Dry



Ready For Next Step



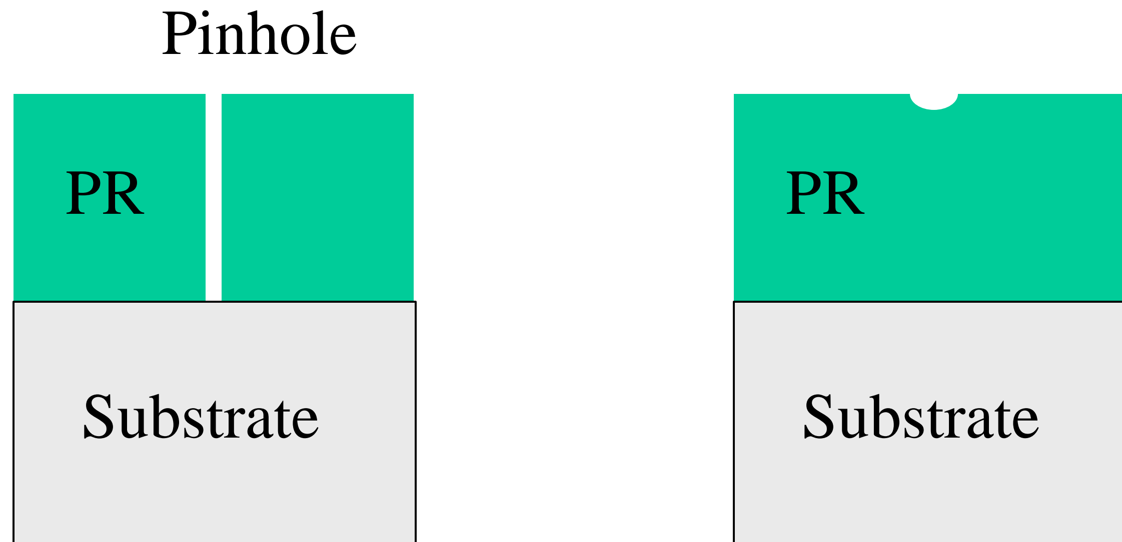
Development



Hard Bake

- Evaporating all solvents in PR
- Improving etch and implantation resistance
- Improve PR adhesion with surface
- Polymerize and stabilize photoresist
- PR flow to fill pinhole

PR Pinhole Fill by Thermal Flow



Hard Bake

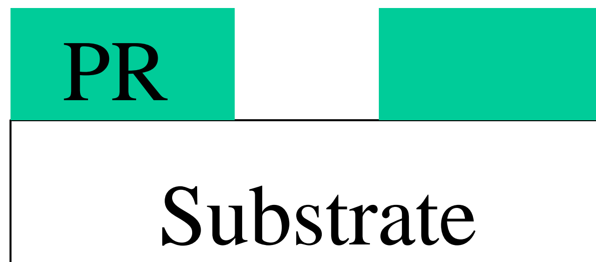
- Hot plate is commonly used
- Can be performed in a oven after inspection
- Hard bake temperature: 100 to 130 °C
- Baking time is about 1 to 2 minutes
- Hard bake temperature normally is higher than the soft bake temperature for the same kind of photoresist

Hard Bake

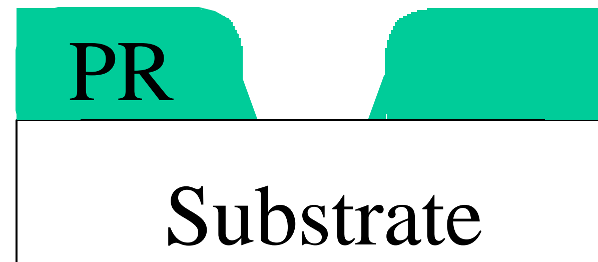
- Under-bake
  - Photoresist is not filly polymerized
  - High photoresist etch rate
  - Poor adhesion
- Over-baking
  - PR flow and bad resolution

Photoresist Flow

- Over baking can causes too much PR flow, which affects photolithography resolution.



Normal Baking



Over Baking

Q & A

- If wrong PR is refilled in the spinner, what could be the consequence?
- Each PR has its own sensitivity & viscosity, require its own spin rates, ramp rates, and time, baking times and temperature, exposure intensities and times, developer solutions and development conditions.
- Pattern transfer will fail.

Pattern Inspection

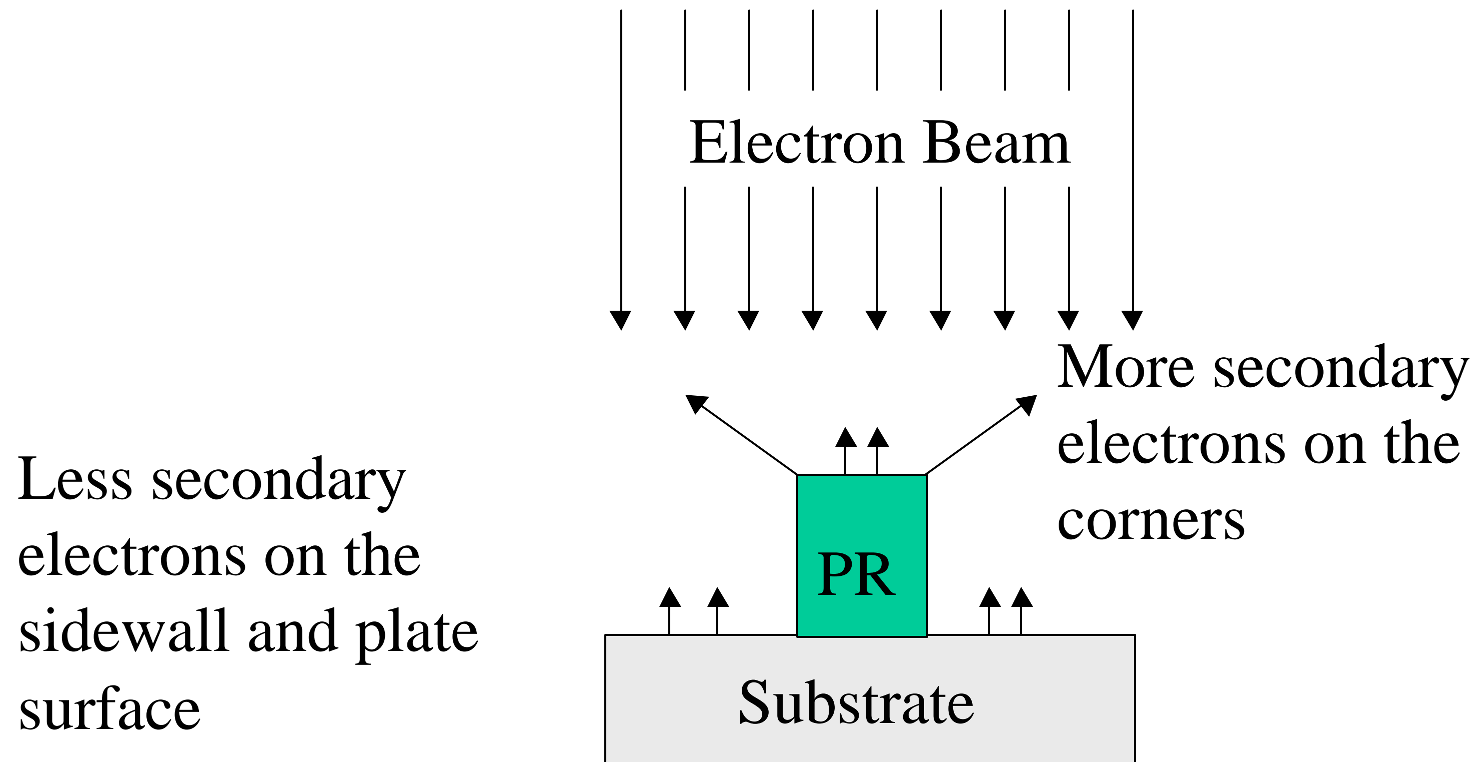
- Fail inspection, stripped PR and rework
  - Photoresist pattern is temporary
  - Etch or ion implantation pattern is permanent.
- Photolithography process can rework
- Can't rework after etch or implantation.
- Scanning electron microscope (SEM)
- Optical microscope

Q & A

- Why can’t optical microscope be used for the 0.25 μm feature inspection?

- Because the feature size (0.25 μm = 2500 Å) is smaller than the wavelength of the visible light, which is from 3900 Å (violet) to 7500 Å (red)..

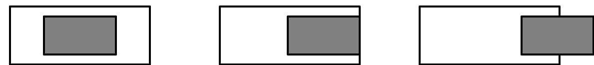
Electron Microscope



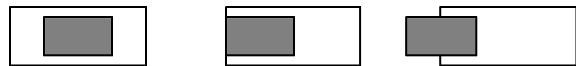
Pattern Inspection

- Overlay or alignment
  - run-out, run-in, reticle rotation, wafer rotation, misplacement in X-direction, and misplacement in Y-direction
- Critical dimension (CD)
- Surface irregularities such as scratches, pin holes, stains, contamination, etc.

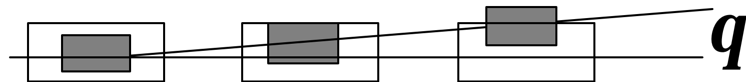
Misalignment Cases



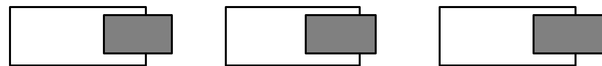
Run-out



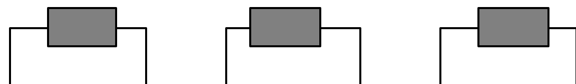
Run-in



Reticle rotation
Wafer rotation

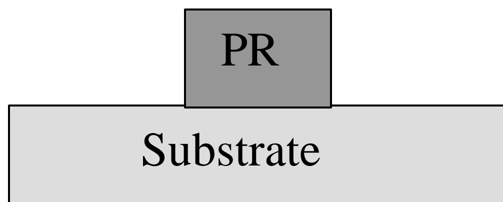


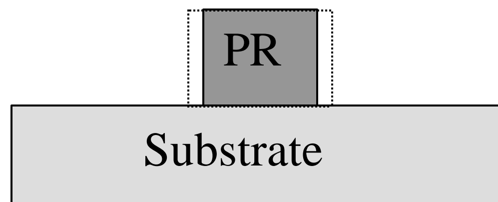
Misplacement in x-direction

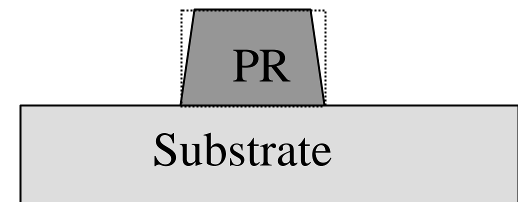


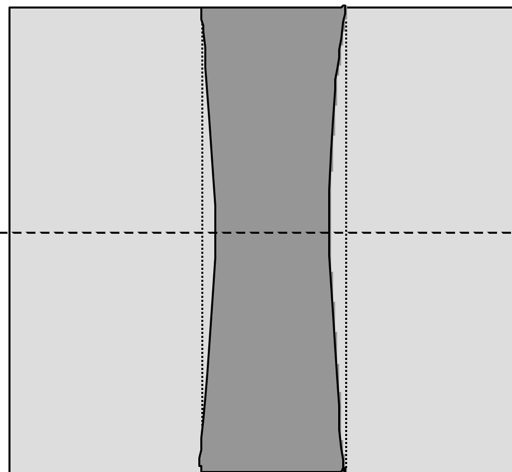
Misplacement in y-direction

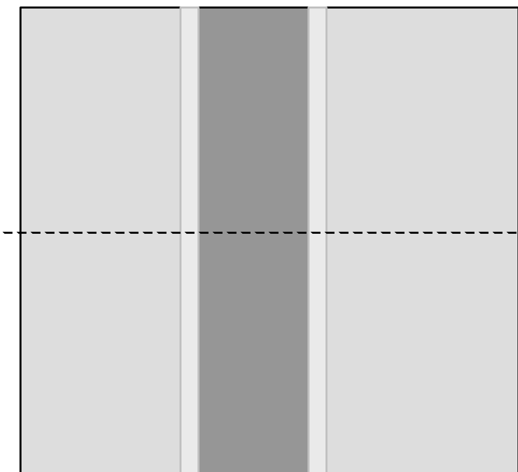
Critical Dimension











Good CD CD Loss Sloped Edge

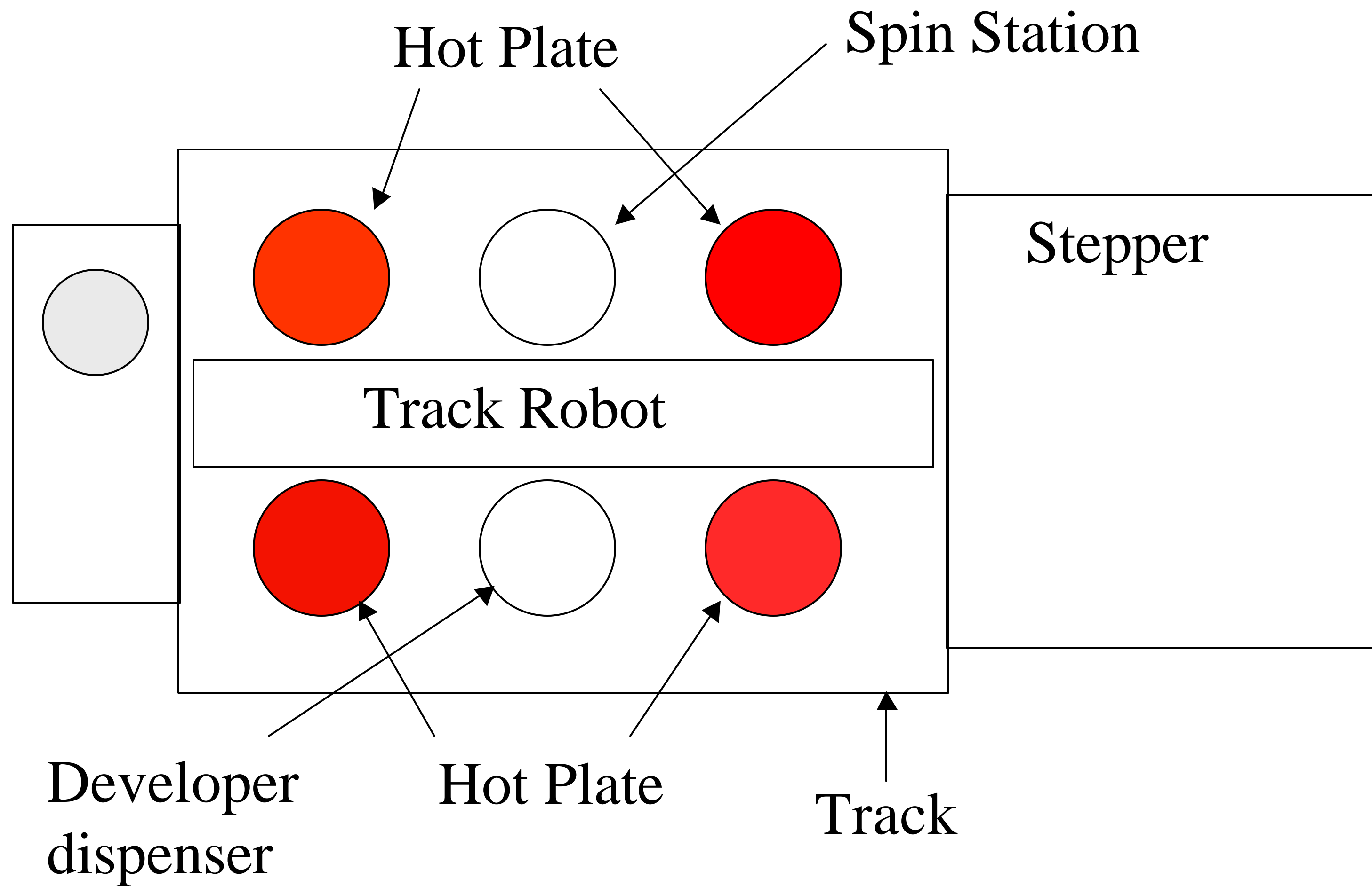
Pattern Inspection

- If the wafers pass the inspection, they will move out of photo bay and go to the next process step
- Either etch or ion implantation

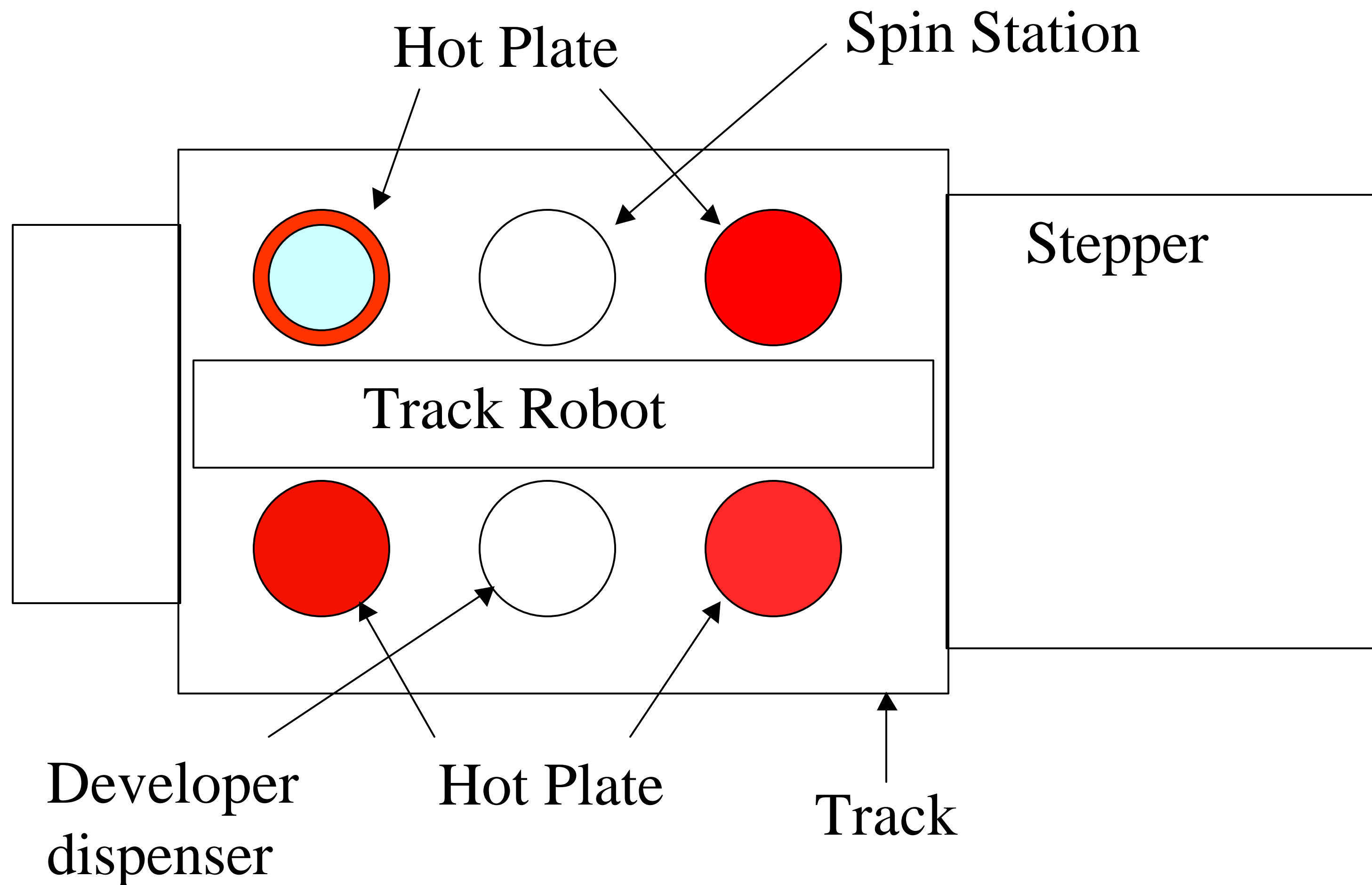
Track-Stepper System or Photo Cell

- Integrated process system of photoresist coating, exposure and development
- Center track robot
- Higher throughput
- Improves process yield

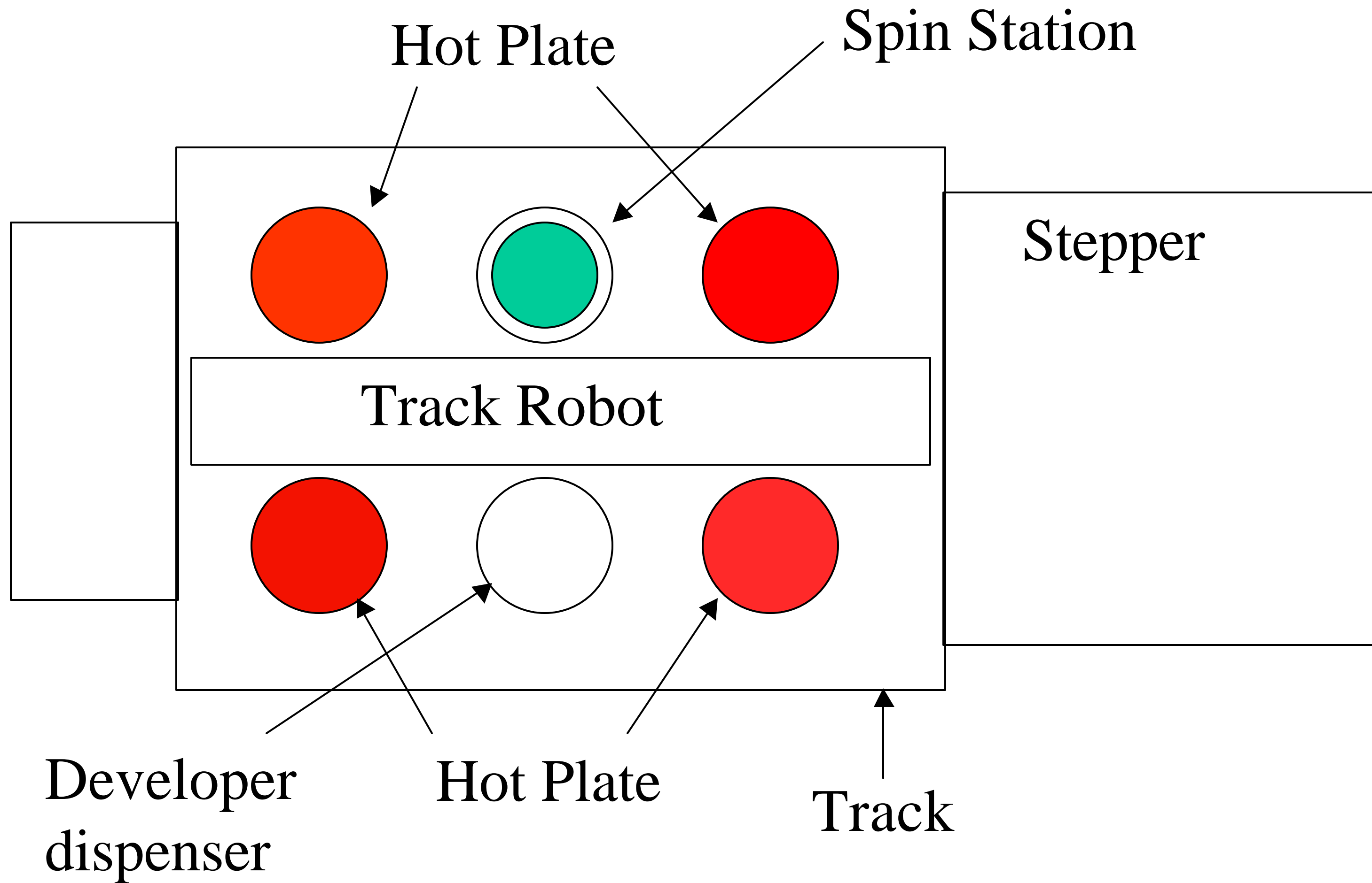
Wafer In



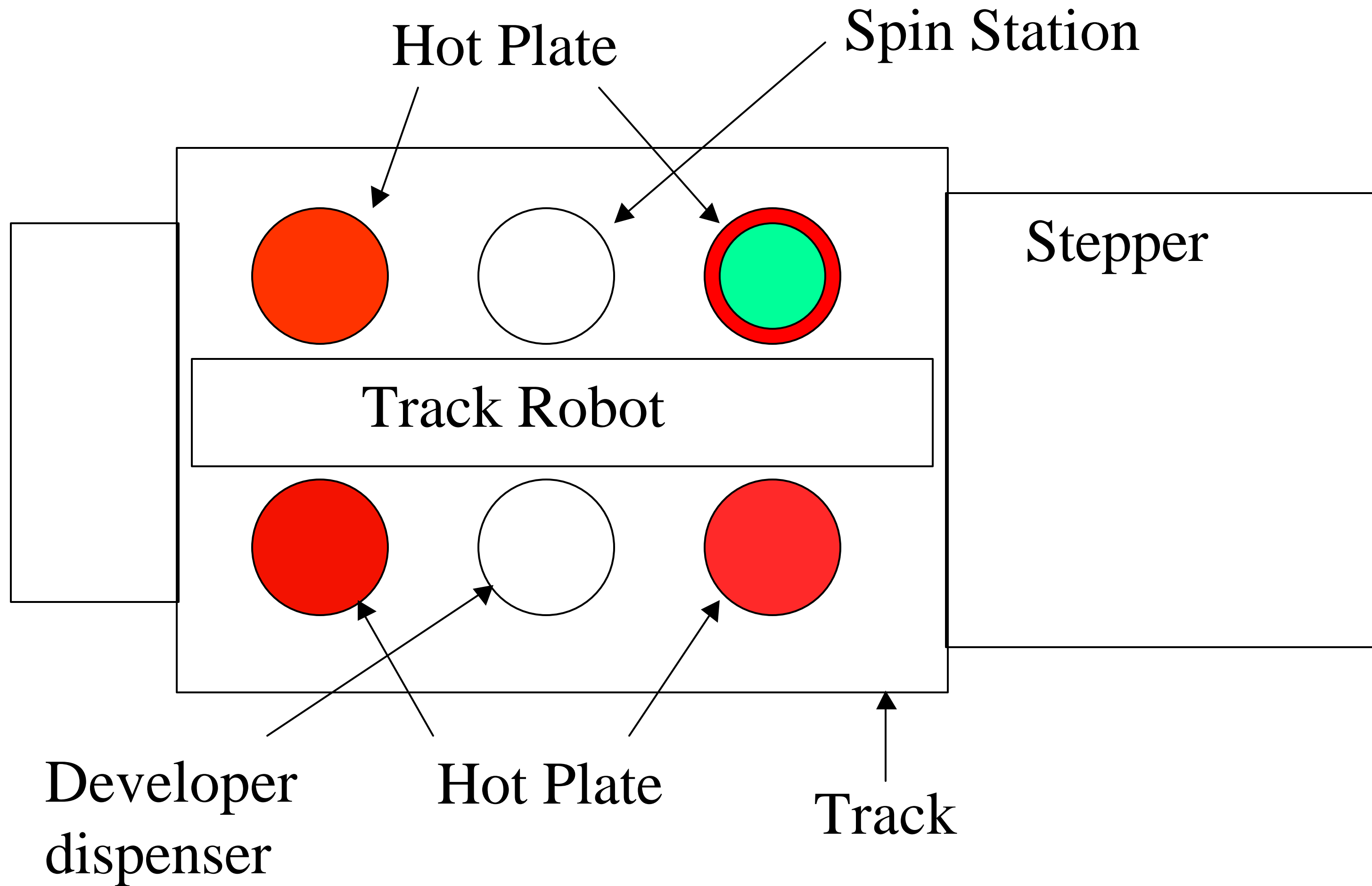
Pre-bake and Primer Vapor Coating



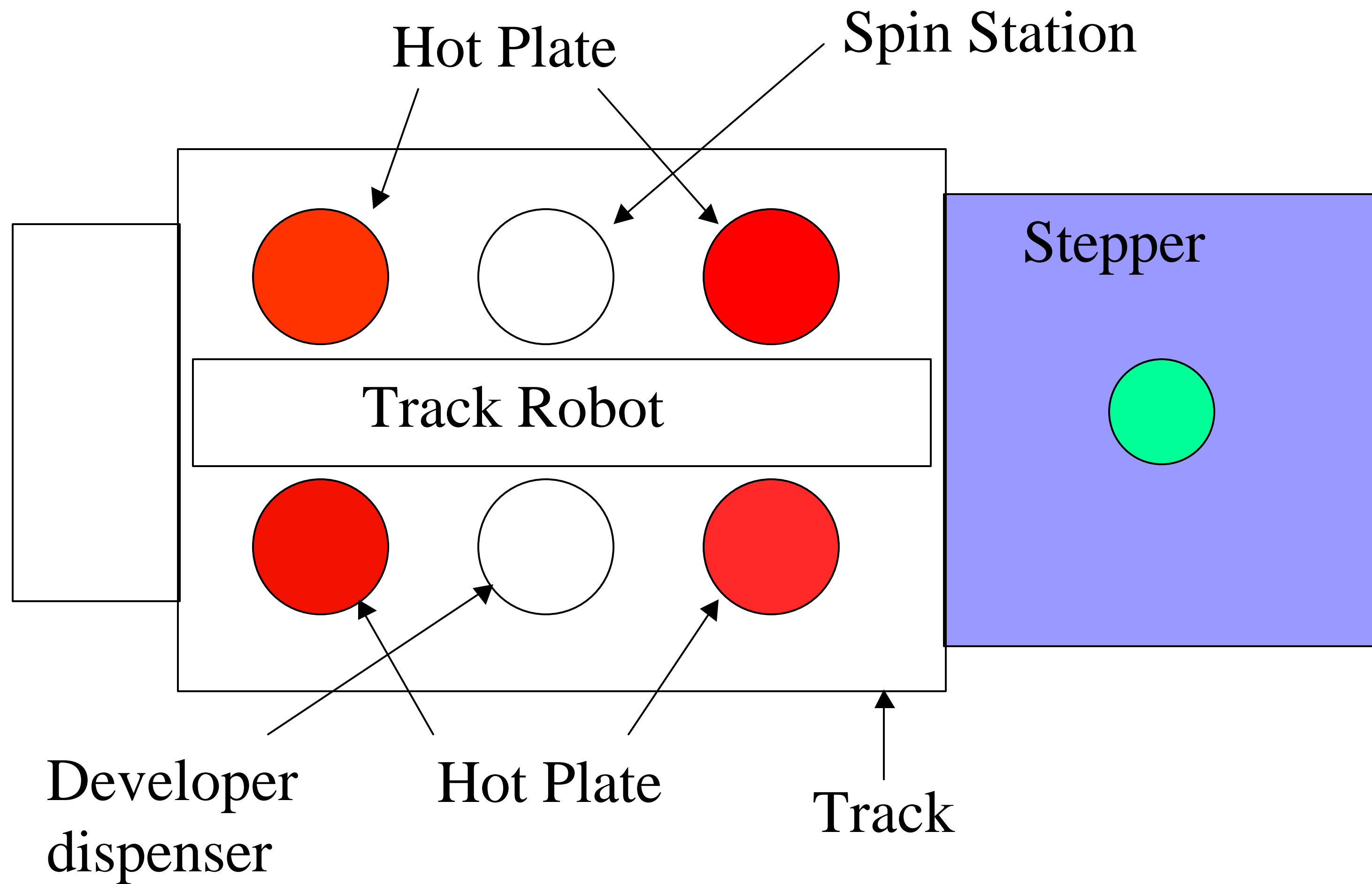
Photoresist Spin Coating



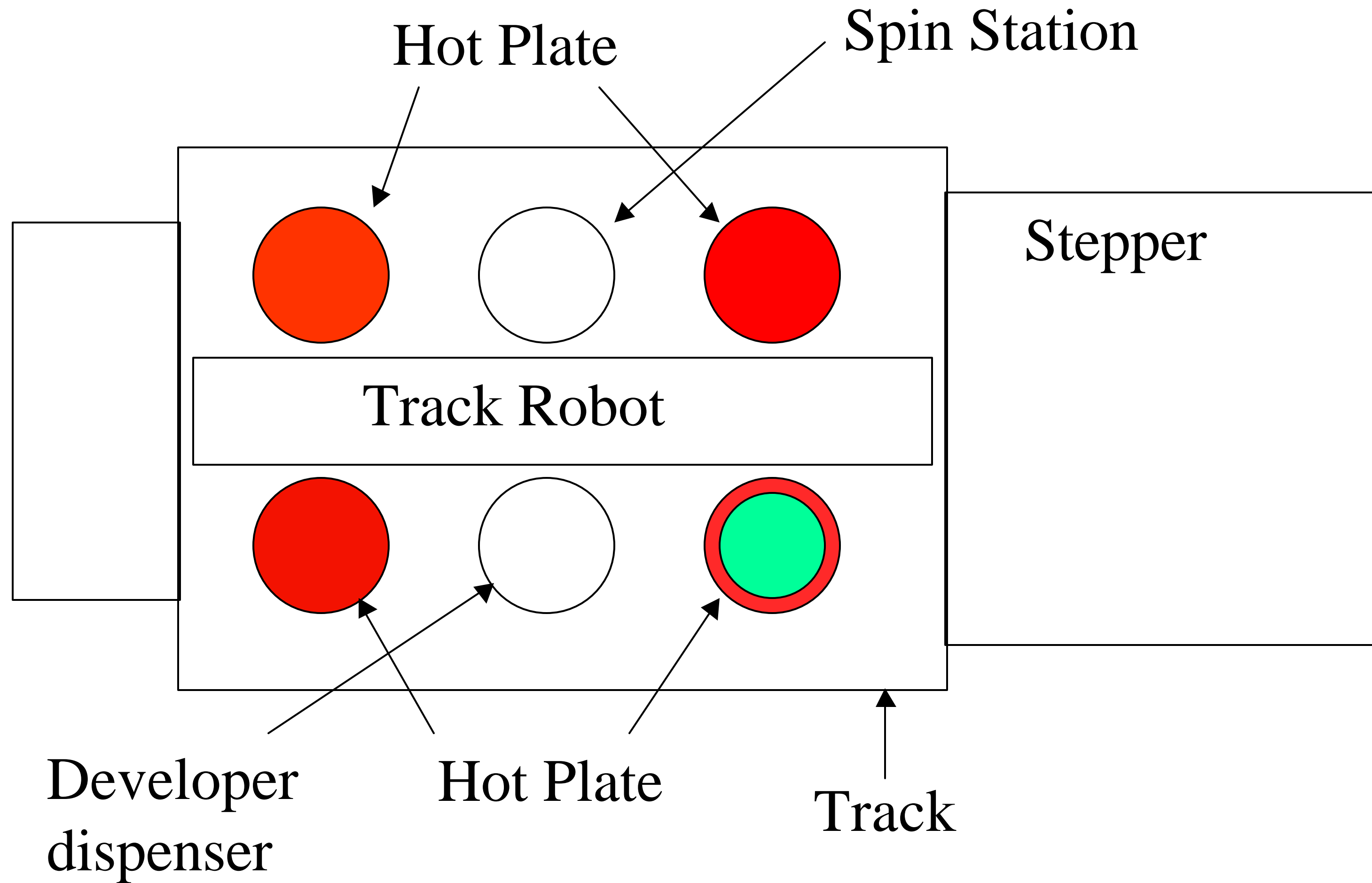
Soft Bake



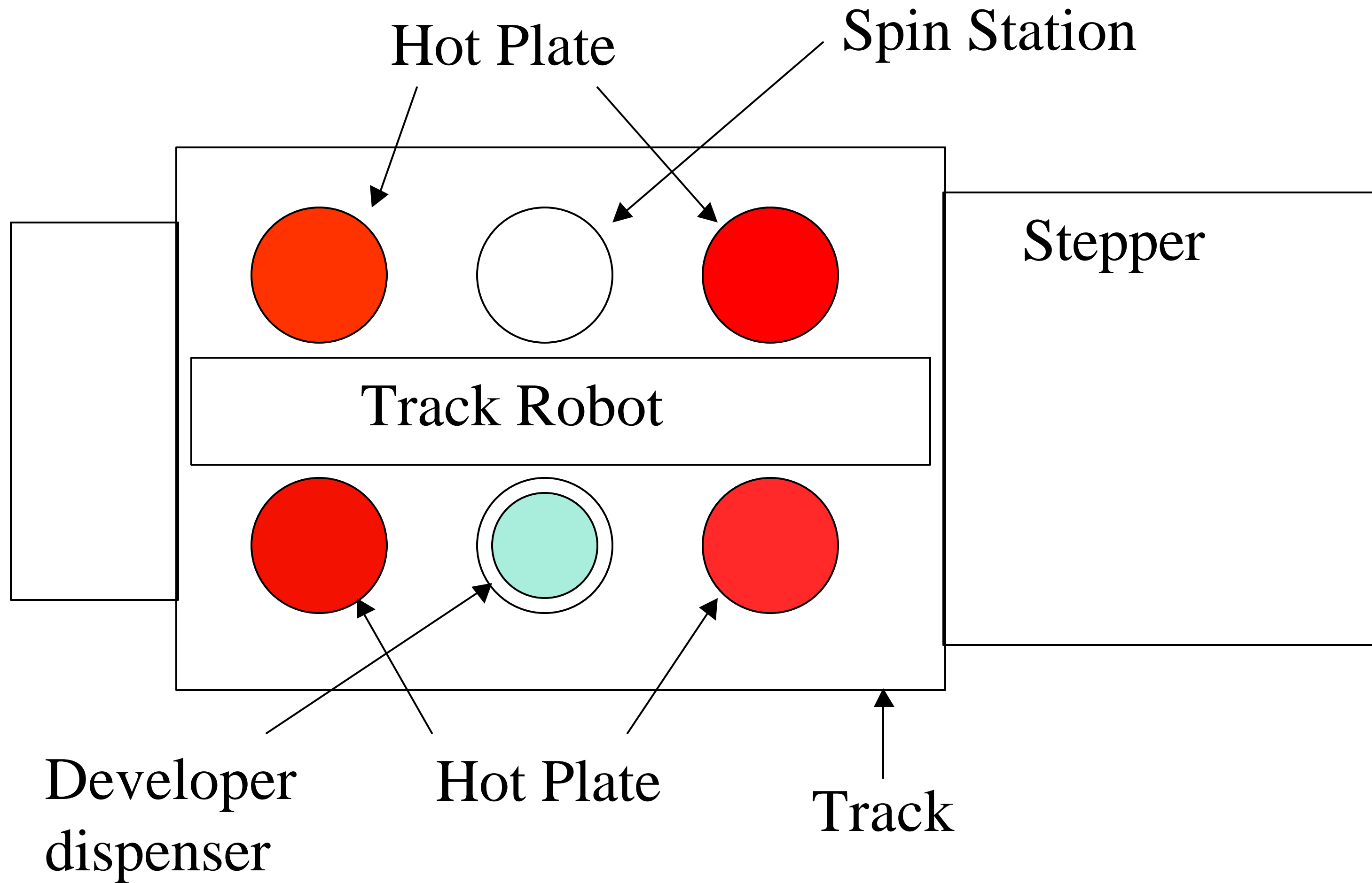
Alignment and Exposure



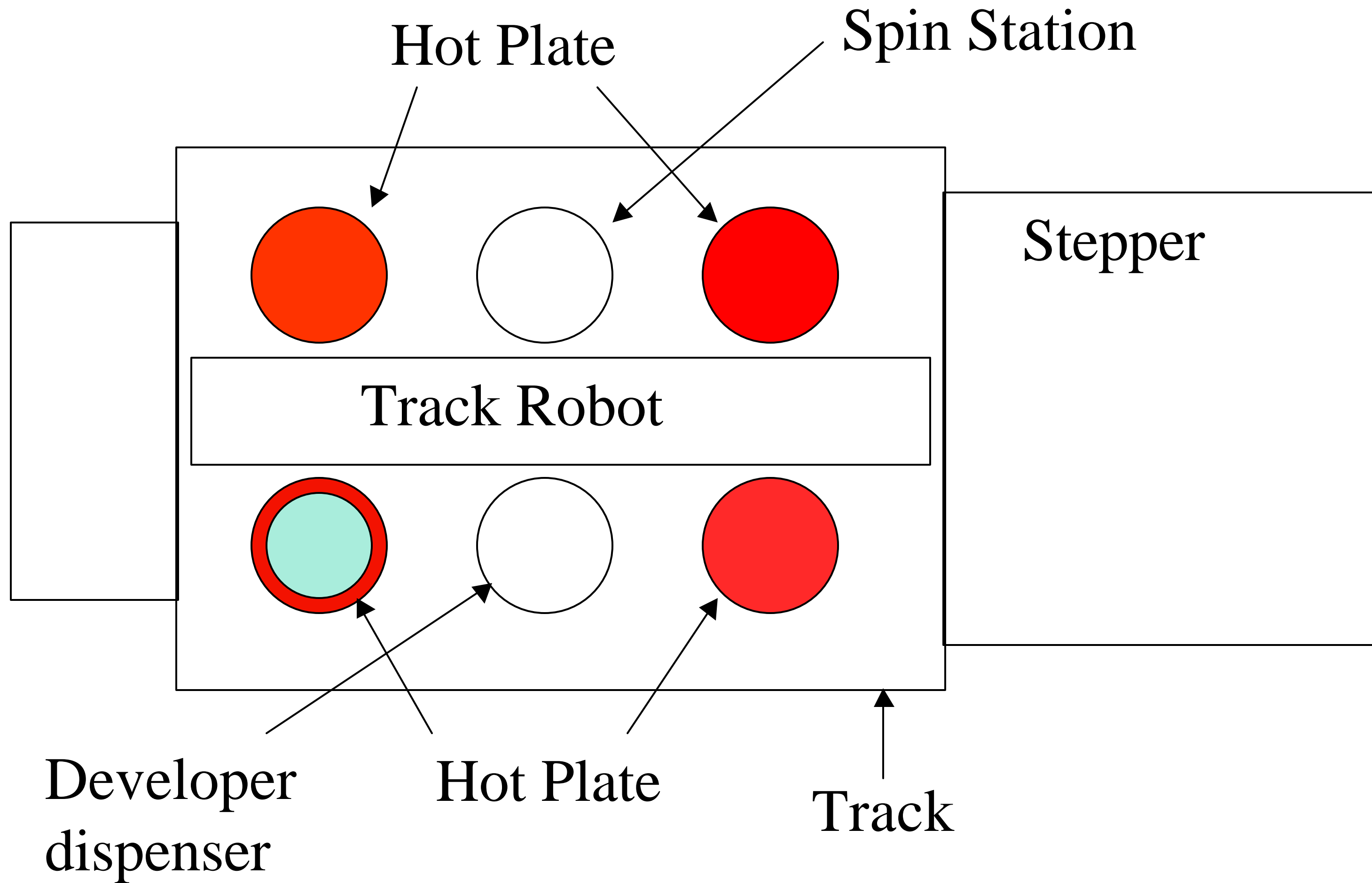
Post Exposure Bake (PEB)



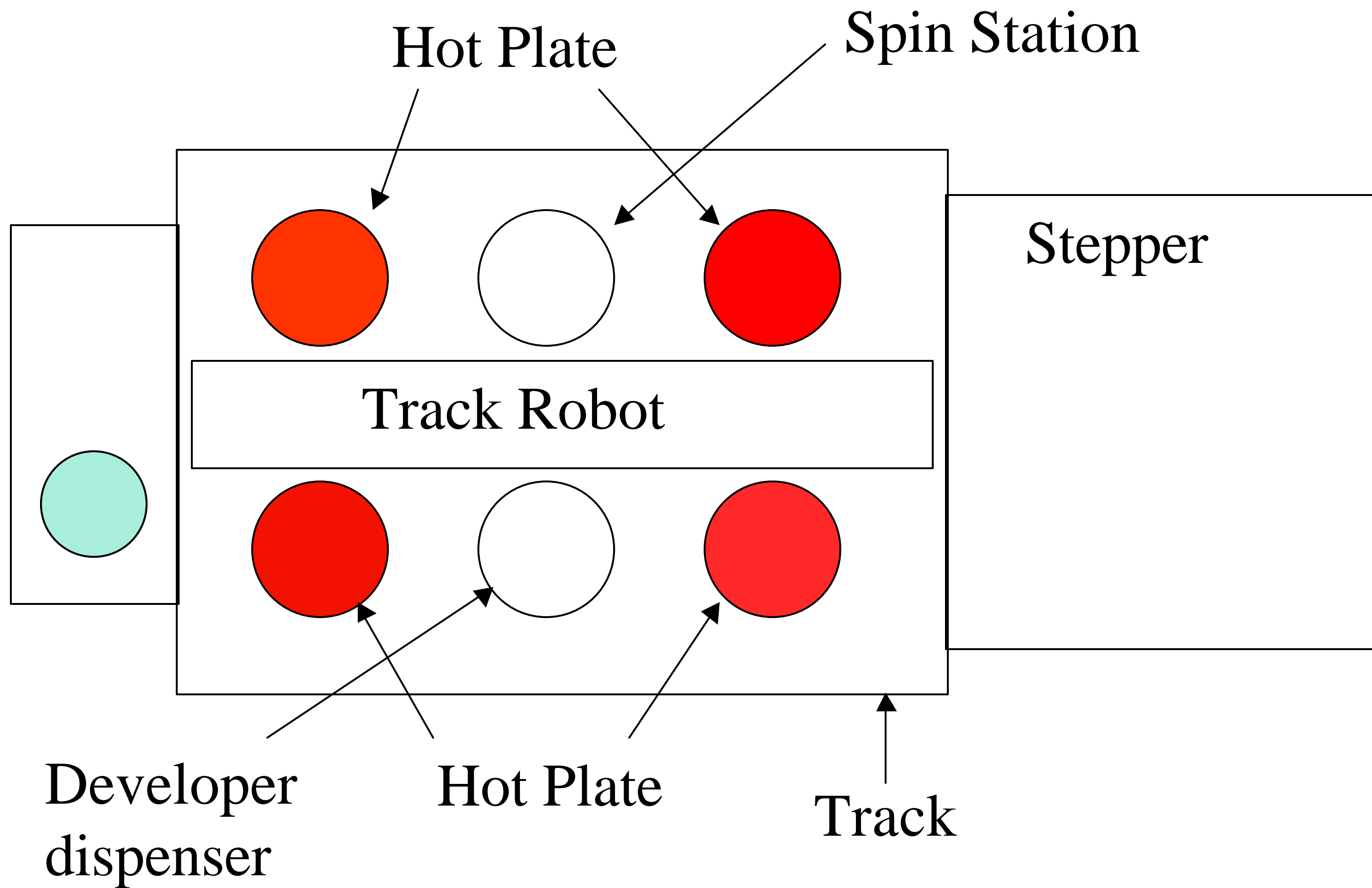
Development



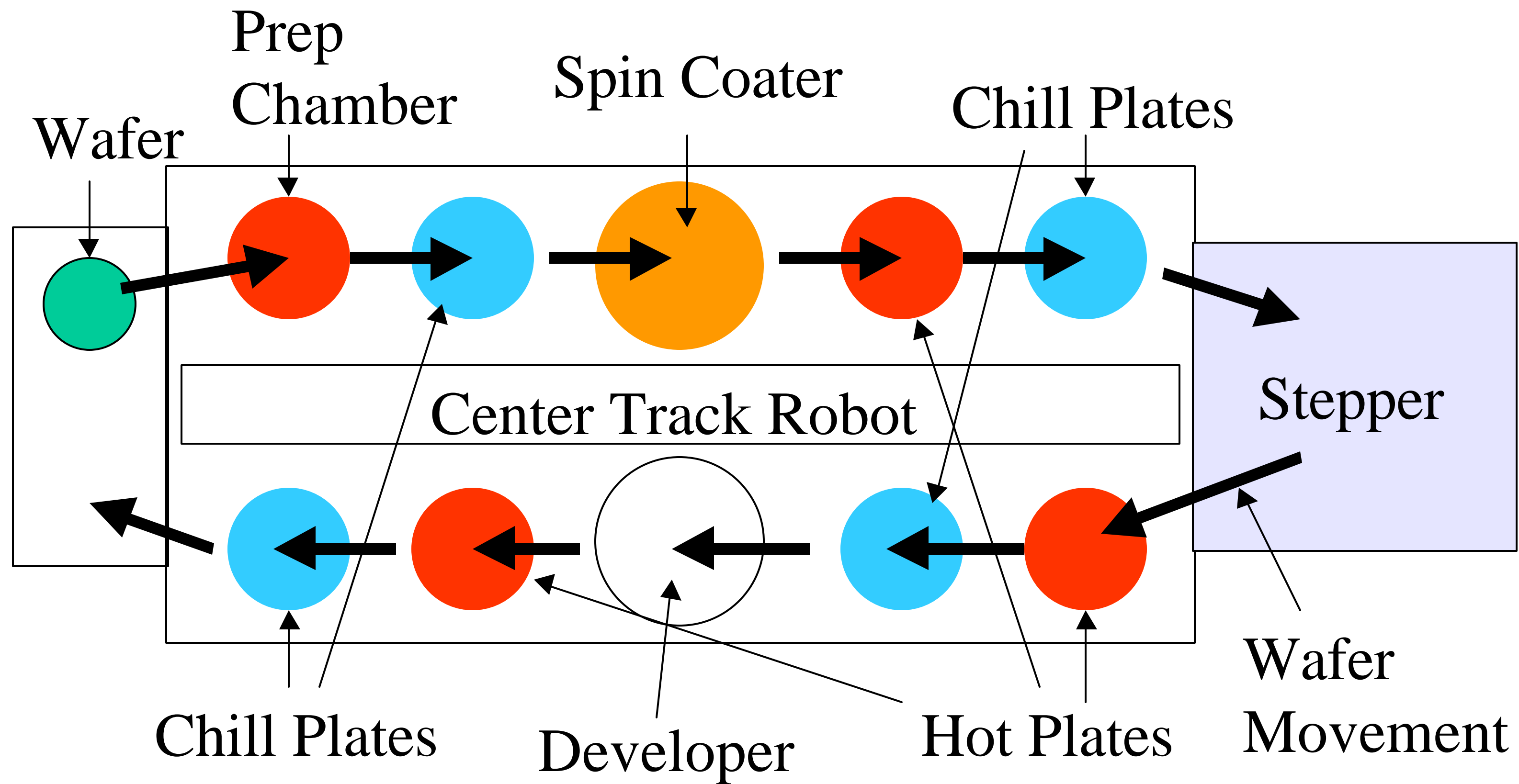
Hard Bake



Wafer out



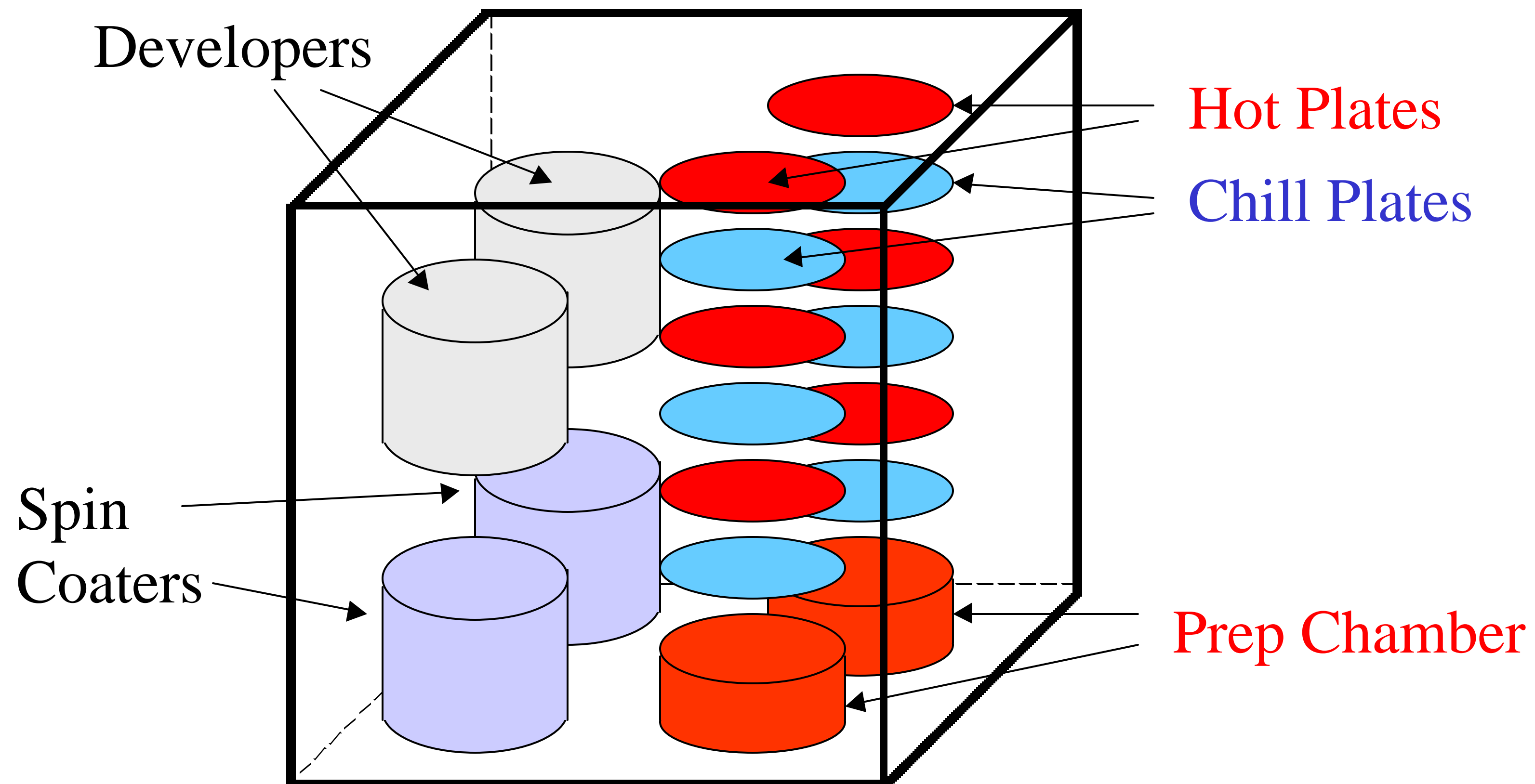
Schematic of a Photo Cell



Stacked Track System

- Smaller footprint
- Lower cost of ownership (COO)

Stacked Track System



Future Trends

- Smaller feature size
- Higher resolution
- Reducing wavelength
- Phase-shift mask

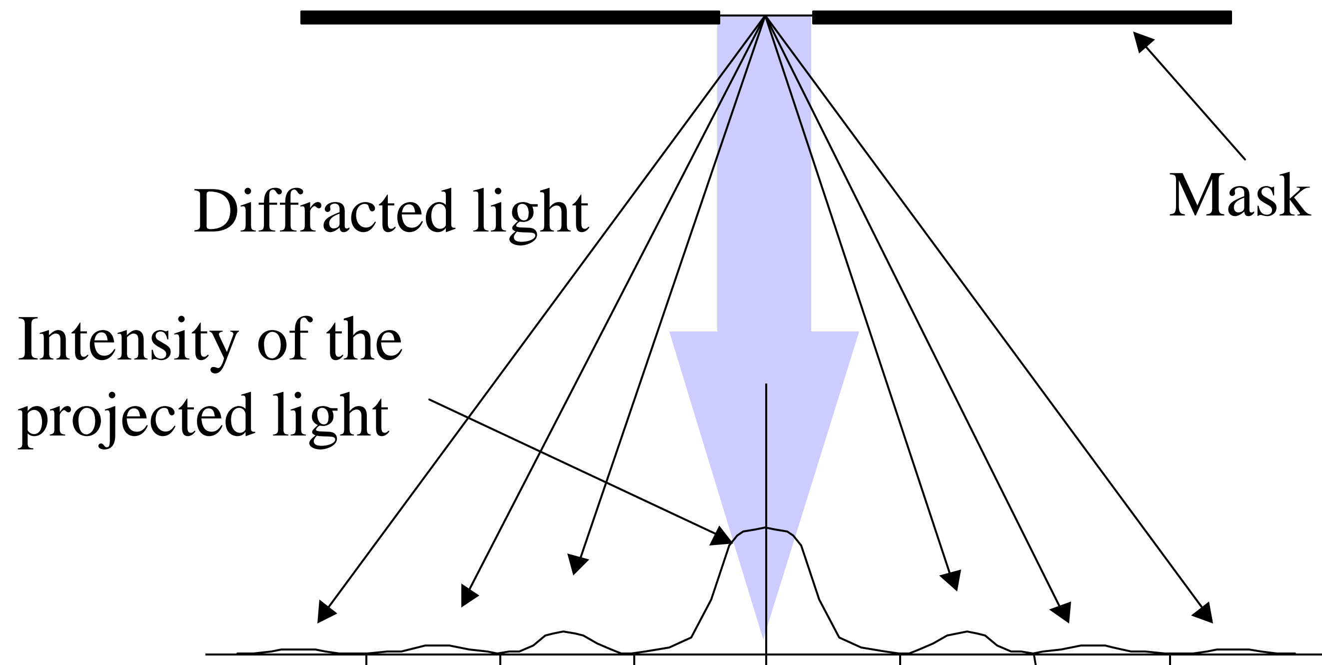
Optical Lithography

- Optics
- Light diffraction
- Resolution
- Depth of focus (DOF)

Diffraction

- Basic property of optics
- Light is a wave
- Wave diffracts
- Diffraction affects resolution

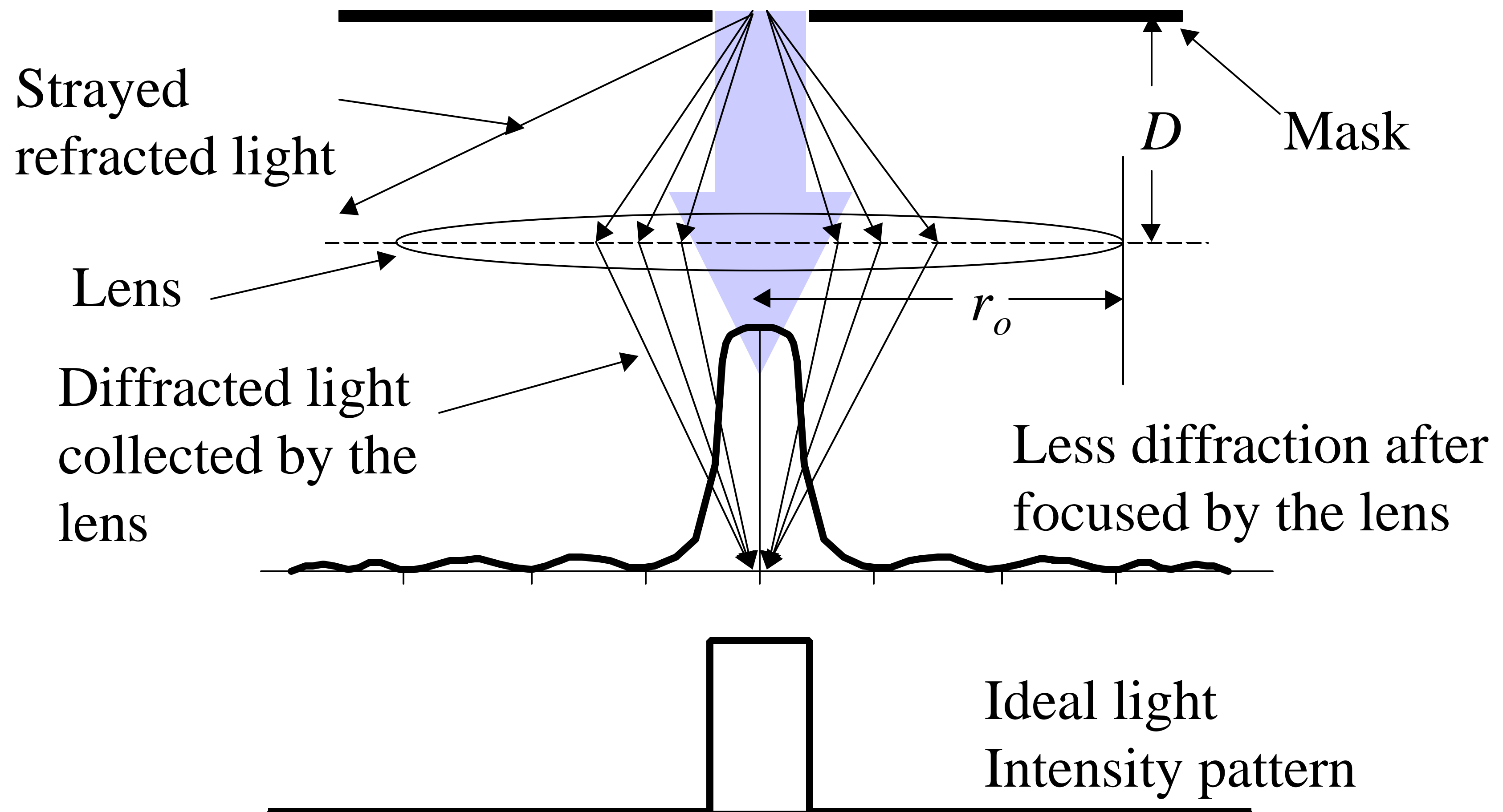
Light Diffraction Without Lens



Diffraction Reduction

- Short wavelength waves have less diffraction
- Optical lens can collect diffracted light and enhance the image

Light Diffraction With Lens



Numerical Aperture

- *NA* is the ability of a lens to collect diffracted light
- $NA = 2\, r_0 / D$
  - r_0 : radius of the lens
  - D = the distance of the object from the lens
- Lens with larger *NA* can capture higher order of diffracted light and generate sharper image.

Resolution

- The achievable, repeatable minimum feature size
- Determined by the wavelength of the light and the numerical aperture of the system. The resolution can be expressed as

Resolution

$$R = \frac{K_1 \lambda}{NA}$$

- K_1 is the system constant, λ is the wavelength of the light, $NA = 2\ r_o/D$, is the numerical aperture
- *NA*: capability of lens to collect diffraction light

Exercise 1, $K_1 = 0.6$

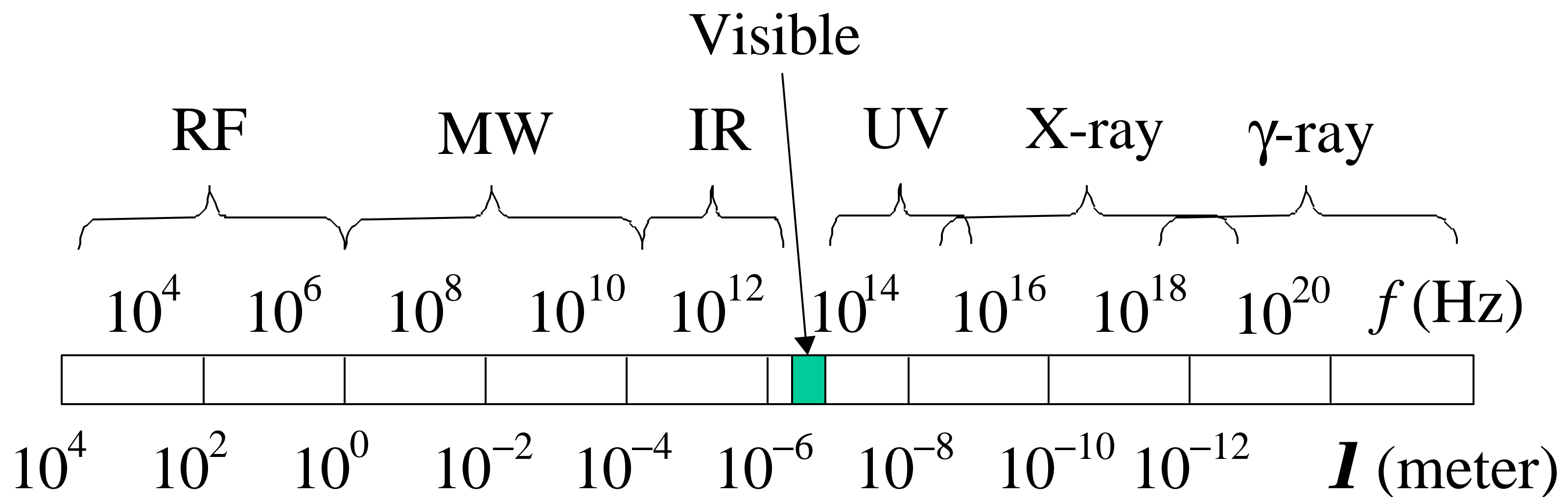
$$R = \frac{K_1 \mathbf{l}}{NA}$$

	l	***NA***	*R*
G-line	**436 nm**	**0.60**	**___ nm**
I-line	**365 nm**	**0.60**	**___ nm**
DUV	**248 nm**	**0.60**	**___ nm**
	193 nm	**0.60**	**___ nm**

To Improve Resolution

- Increase NA
  - Larger lens, could be too expensive and unpractical
  - Reduce DOF and cause fabrication difficulties
- Reduce wavelength
  - Need develop light source, PR and equipment
  - Limitation for reducing wavelength
  - UV to DUV, to EUV, and to X-Ray
- Reduce K_1
  - Phase shift mask

Wavelength and Frequency of Electromagnetic Wave



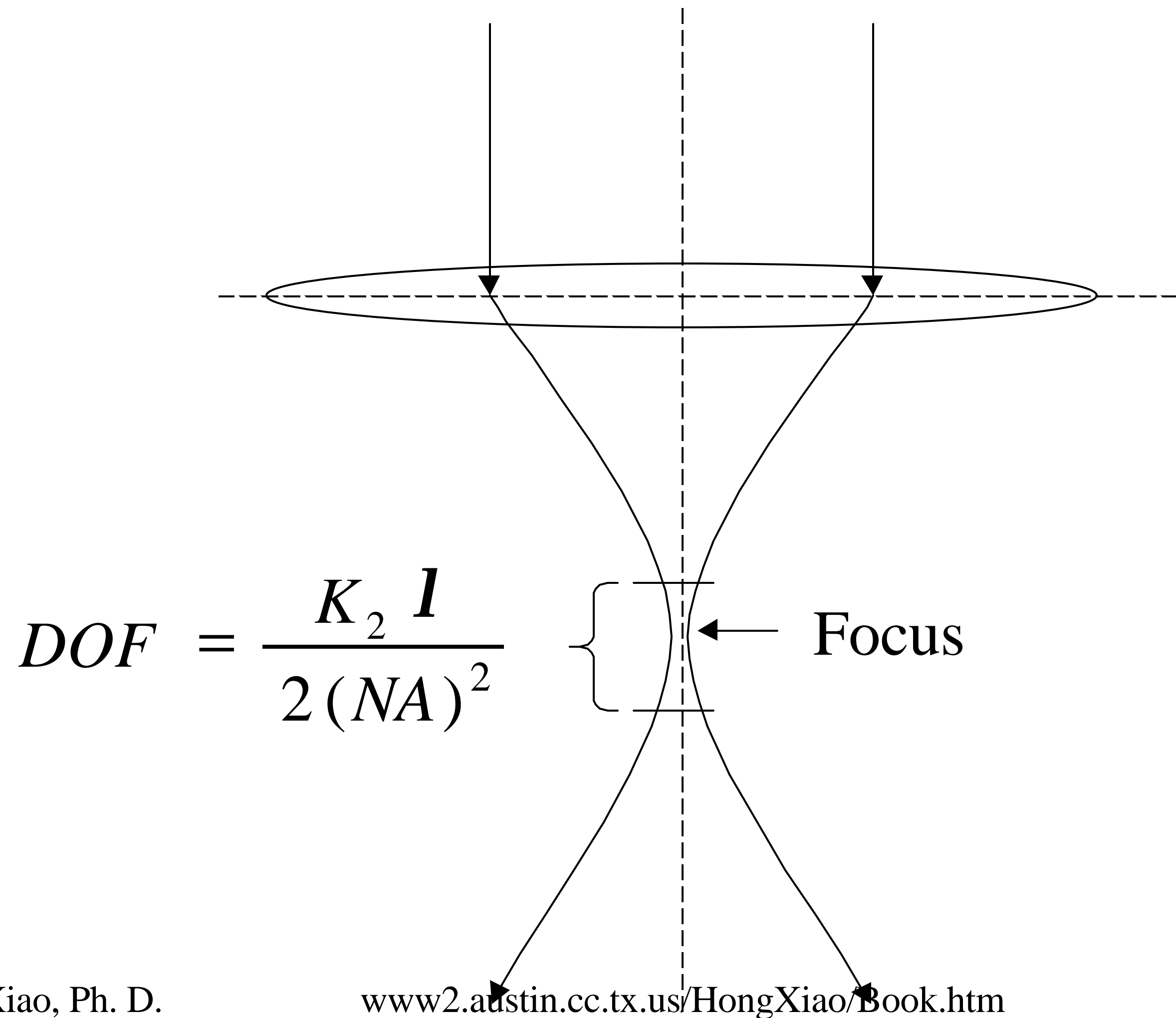
RF: Radio frequency; MW: Microwave; IR: infrared; and UV: ultraviolet

Depth of focus

- The range that light is in focus and can achieve good resolution of projected image
- Depth of focus can be expressed as:

$$DOF = \frac{K_2 \lambda}{2(NA)^2}$$

Depth of Focus



Exercise 2, $K_2 = 0.6$

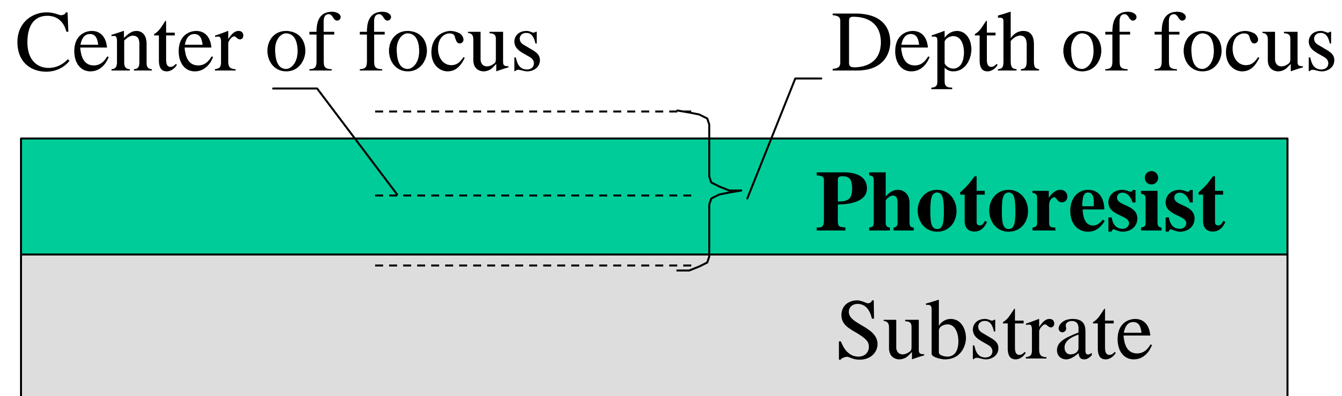
$$DOF = \frac{K_2 \mathbf{l}}{2(NA)^2}$$

	l	***NA***	*DOF*
G-line	**436 nm**	**0.60**	**____ mm**
I-line	**365 nm**	**0.60**	**____ mm**
DUV	**248 nm**	**0.60**	**____ mm**
	193 nm	**0.60**	**____ mm**

Depth of Focus

- Smaller numerical aperture, larger DOF
  - Disposable cameras with very small lenses
  - Almost everything is in focus
  - Bad resolution
- Prefer reduce wavelength than increase *NA* to improve resolution
- High resolution, small DOF
- Focus at the middle of PR layer

Focus on the Mid-Plain to Optimize the Resolution



Surface Planarization Requirement

- Higher resolution requires
  - Shorter ***l***
  - Larger *NA*.
- Both reduces *DOF*
- Wafer surface must be highly planarized.
- CMP is required for 0.25 μm feature patterning.

I-line and DUV

- Mercury i-line, 365 nm
  - Commonly used in 0.35 μm lithography
- DUV KrF excimer laser, 248 nm
  - 0.25 μm, 0.18 μm and 0.13 μm lithography
- ArF excimer laser,193 nm
  - Application: < 0.13 μm
- F_2 excimer laser 157 nm
  - Still in R&D, < 0.10 μm application

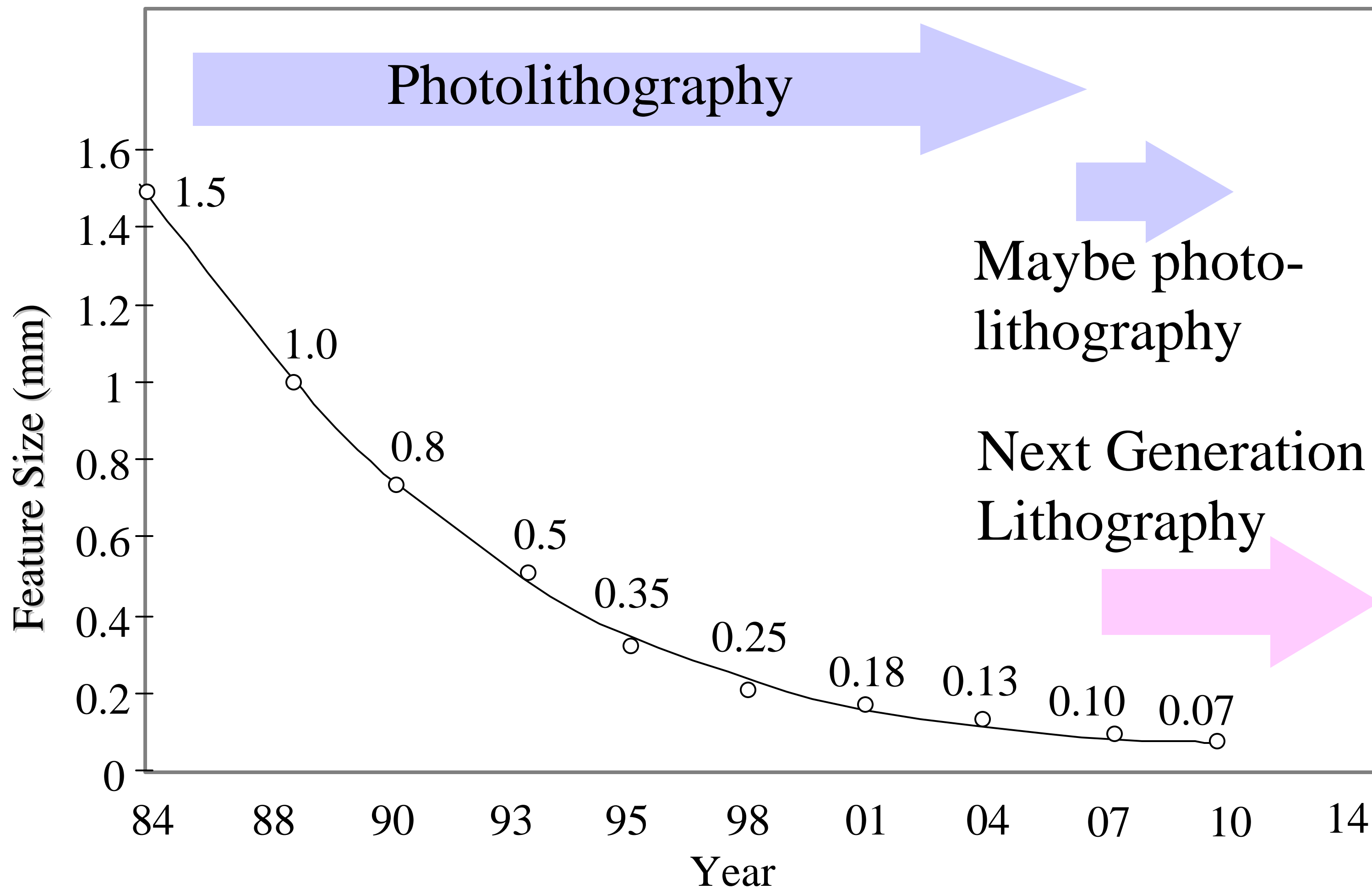
I-line and DUV

- SiO_2 strongly absorbs UV when $\lambda < 180$ nm
- Silica lenses and masks can't be used
- 157 nm F_2 laser photolithography
  - Fused silica with low OH concentration, fluorine doped silica, and calcium fluoride (CaF_2),
  - With phase-shift mask, even 0.035 μm is possible
- Further delay next generation lithography

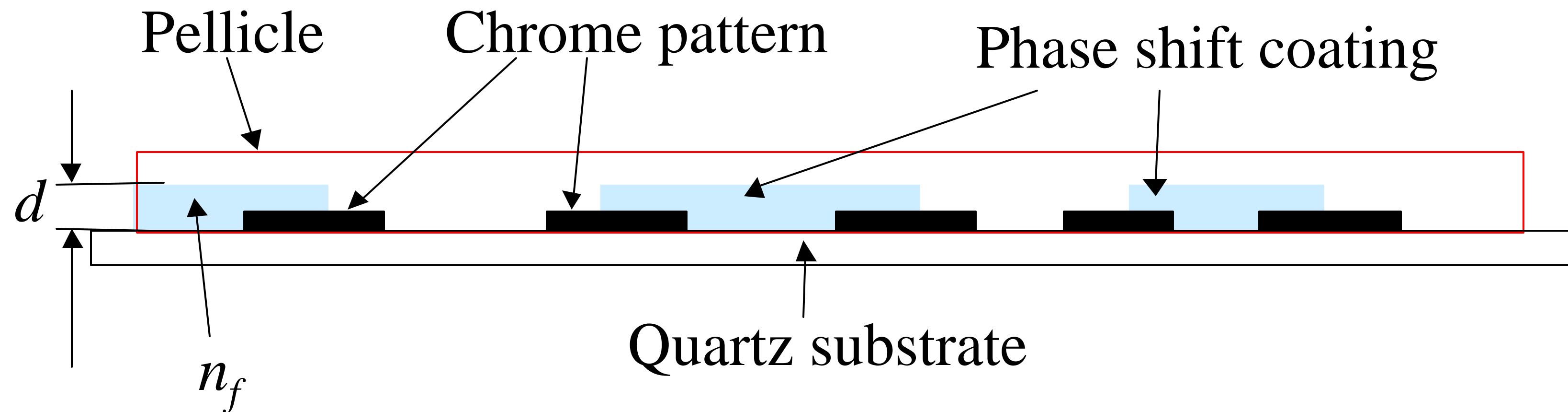
Next Generation Lithography (NGL)

- Extreme UV (EUV) lithography
- X-Ray lithography
- Electron beam (E-beam) lithography

Future Trends



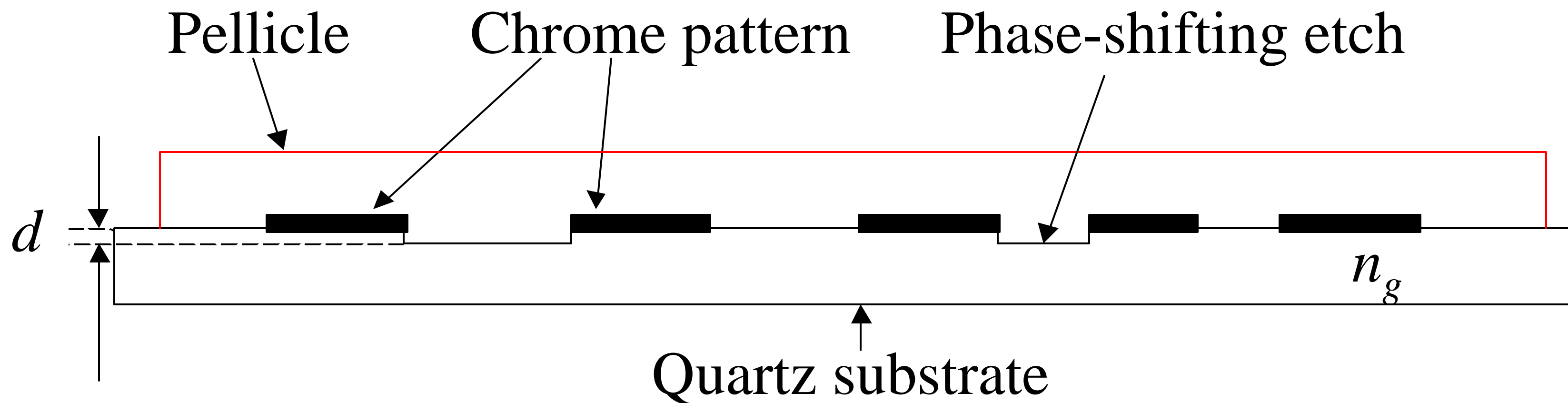
Phase Shift Mask



$$d(n_f - 1) = \lambda/2$$

n_f : Refractive index of phase shift coating

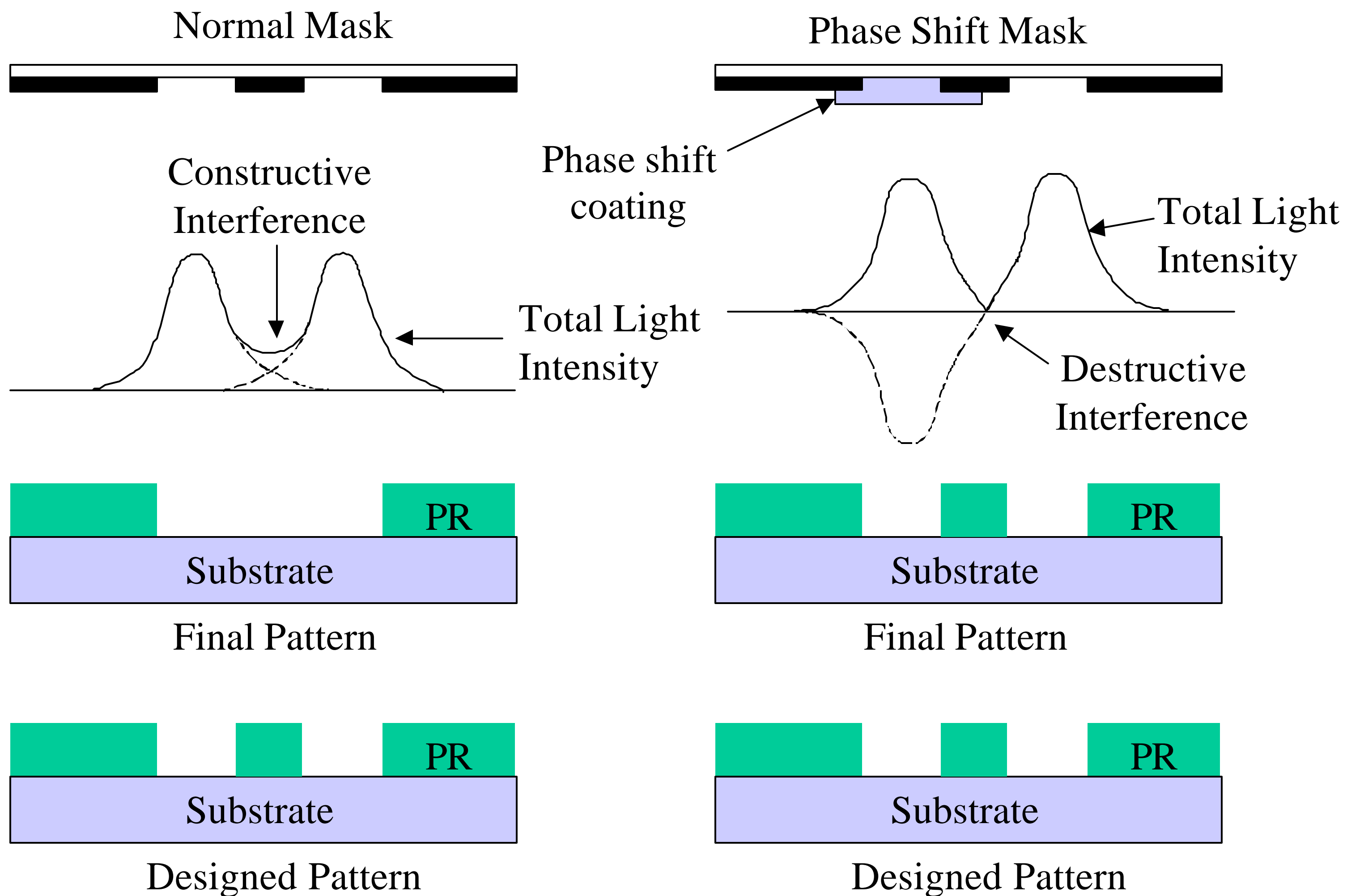
Phase Shift Mask



$$d(n_g - 1) = \lambda/2$$

n_g: refractive index of the quartz substrate

Phase Shift Mask Patterning



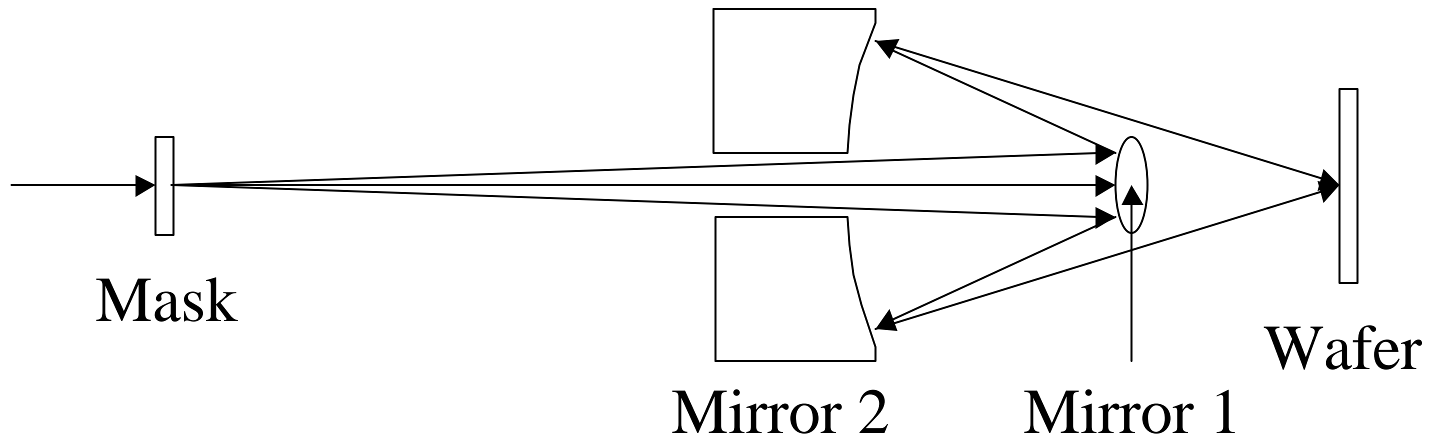
Future Trends

- Even shorter wavelength
  - 193 nm
  - 157 nm
    - Silicate glass absorbs UV light when $\lambda < 180$ nm
    - CaF_2 optical system
- Next generation lithography (NGL)
  - Extreme UV (EVU)
  - Electron Beam
  - X-ray (?)

EUV

- λ = 10 to 14 nm
- Higher resolution
- Mirror based
- Projected application ~ 2010
- 0.1 μm and beyond

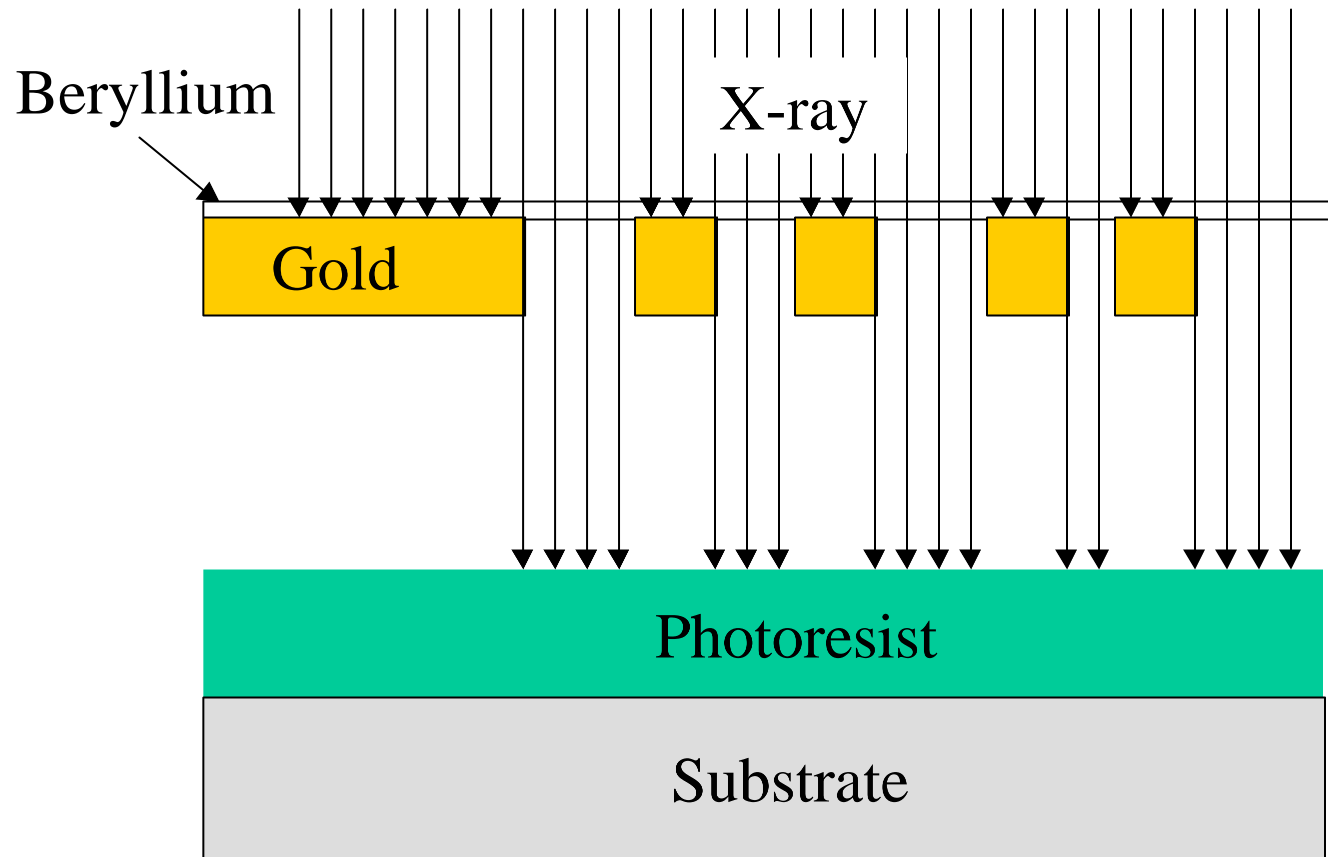
EUV Lithography



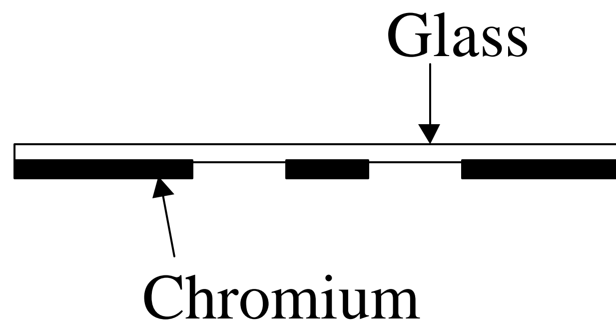
X-ray lithography

- Similar to proximity printer
- Difficult to find pure X-ray source
- Challenge on mask making
- Unlikely will be used in production

X-ray Printing



Optical Mask and X-ray Mask



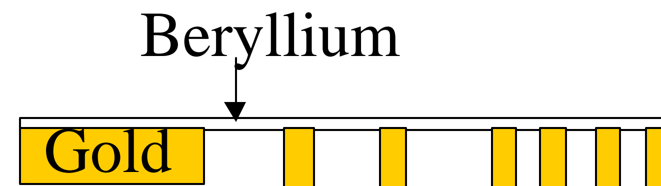


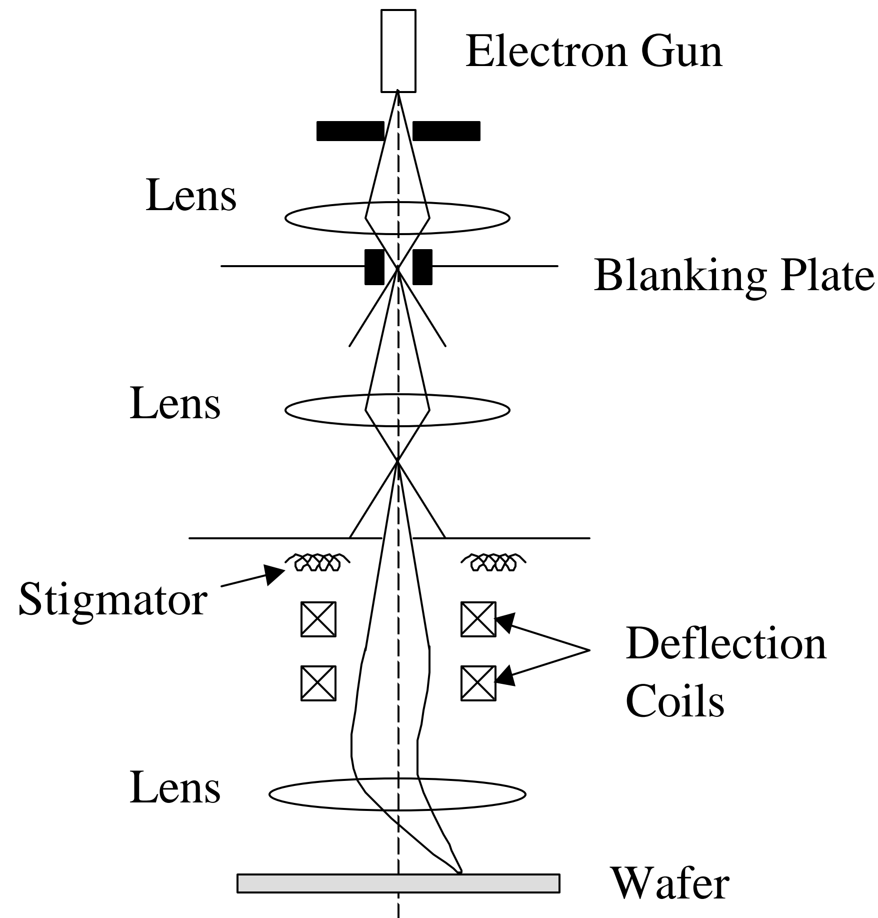
Photo Mask

X-ray Mask

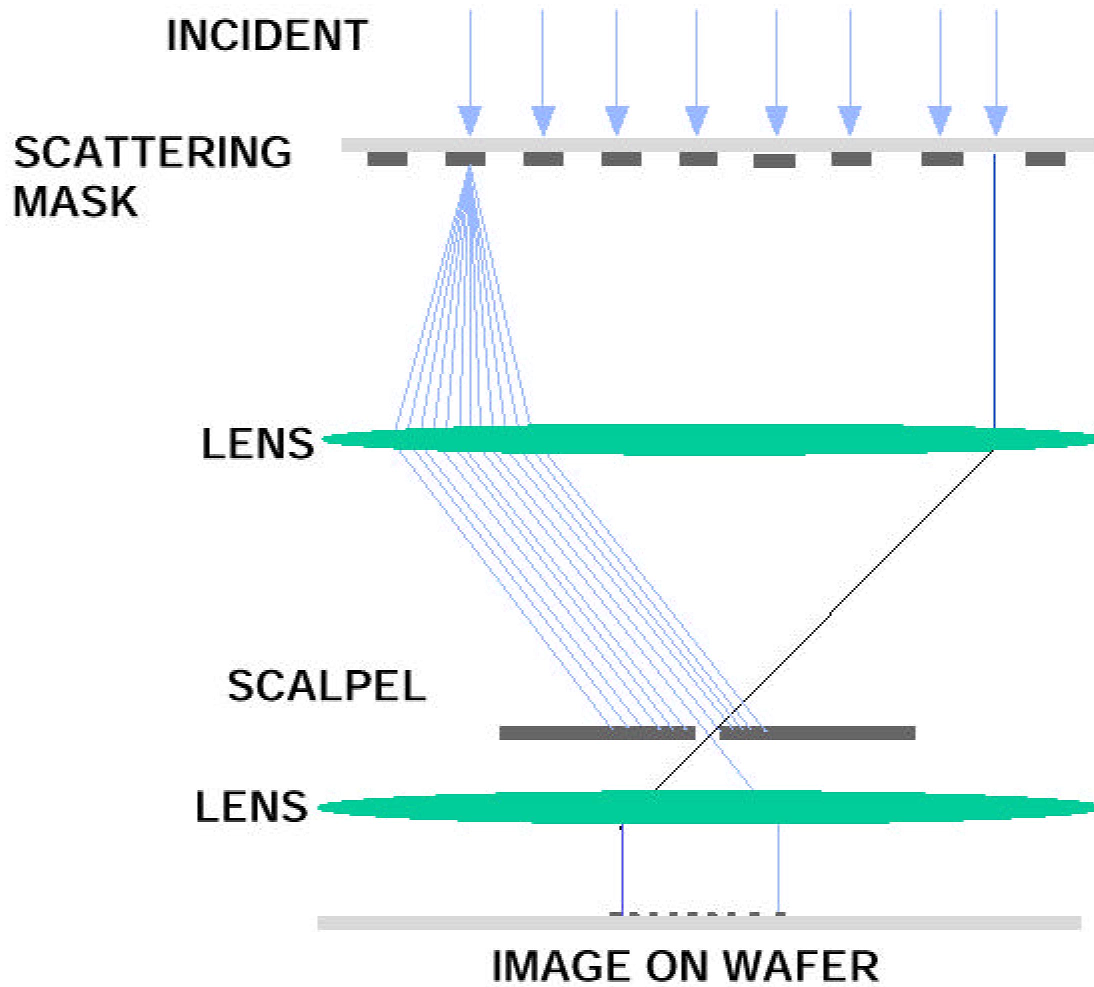
E-Beam

- Used for making mask and reticles
- Smallest geometry achieved: 0.014 μm
- Direct print possible, no mask is required
  - Low throughput
- Scattering exposure system (SCALPEL) looks promising
  - Tool development
  - Reticle making
  - Resist development

Electron Beam Lithography System



SCALPEL



Ion Beam Lithography

- Can achieve higher resolution
  - Direct writing and projection resist exposing
  - Direct ion implantation and ion beam sputtering patterned etch, save some process steps
- Serial writing, low throughput
- Unlikely will be used in the mass production
- Mask and reticle repairing
- IC device defect detection and repairing

Safety

- Chemical
- Mechanical
- Electrical
- Radiation

Chemical Safety

- Wet clean
  - Sulfuric acid (H_2SO_4): corrosive
  - Hydrogen peroxide (H_2O_2): strong oxidizer
- Xylene (solvent and developer of –PR): flammable and explosive
- HMDS (primer): flammable and explosive
- TMAH (+PR development solution): poisonous and corrosive

Chemical Safety

- Mercury (Hg, UV lamp) vapor
  - highly toxic;
- Chlorine (Cl_2, excimer laser)
  - toxic and corrosive
- Fluorine (F_2, excimer laser)
  - toxic and corrosive

Mechanical Safety

- Moving Parts
- Hot surface
- High pressure lump

Electrical Safety

- High voltage electric power supply
- Power off
- Ground static charges
- Tag-out and lock-out

Radiation Safety

- UV light can break chemical bonds
- Organic molecules have long-chain structure
- More vulnerable to the UV damage
- UV light can be used to kill bacteria for sterilization
- Can cause eye injury if direct look at UV source
- UV protection goggle sometimes is required.

Summary

- Photolithography: temporary patterning process
- Most critical process steps in IC processing
- Requirement: high resolution, low defect density
- Photoresist, positive and negative
- Process steps: Pre-bake and Primer coating, PR spin coating, soft bake, exposure, PEB, development, hard bake, and inspection
- NGL: EUV and e-beam lithography

Chapter 7
Plasma Basic

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Objectives

- List at least three IC processes using plasma
- Name three important collisions in plasma
- Describe mean free path
- Explain how plasma enhance etch and CVD processes
- Name two high density plasma sources

Topics of Discussion

- What is plasma?
- Why use plasma?
- Ion bombardment
- Application of plasma process

Applications of Plasma

- CVD
- Etch
- PVD
- Ion Implantation
- Photoresist strip
- Process chamber dry clean

What Is Plasma

- A plasma is a ionized gas with equal numbers of positive and negative charges.
- A more precise definition: *a plasma is a quasi-neutral gas of charged and neutral particles which exhibits collective behavior*.
- Examples: Sun, flame, neon light, etc.

Components of Plasma

- A plasma consists of neutral atoms or molecules, negative charges (electrons) and positive charges (ions)

- Quasi-neutral: n_i » n_e

- Ionization rate: $\boldsymbol{h}$ » $n_e/(n_e + n_n)$

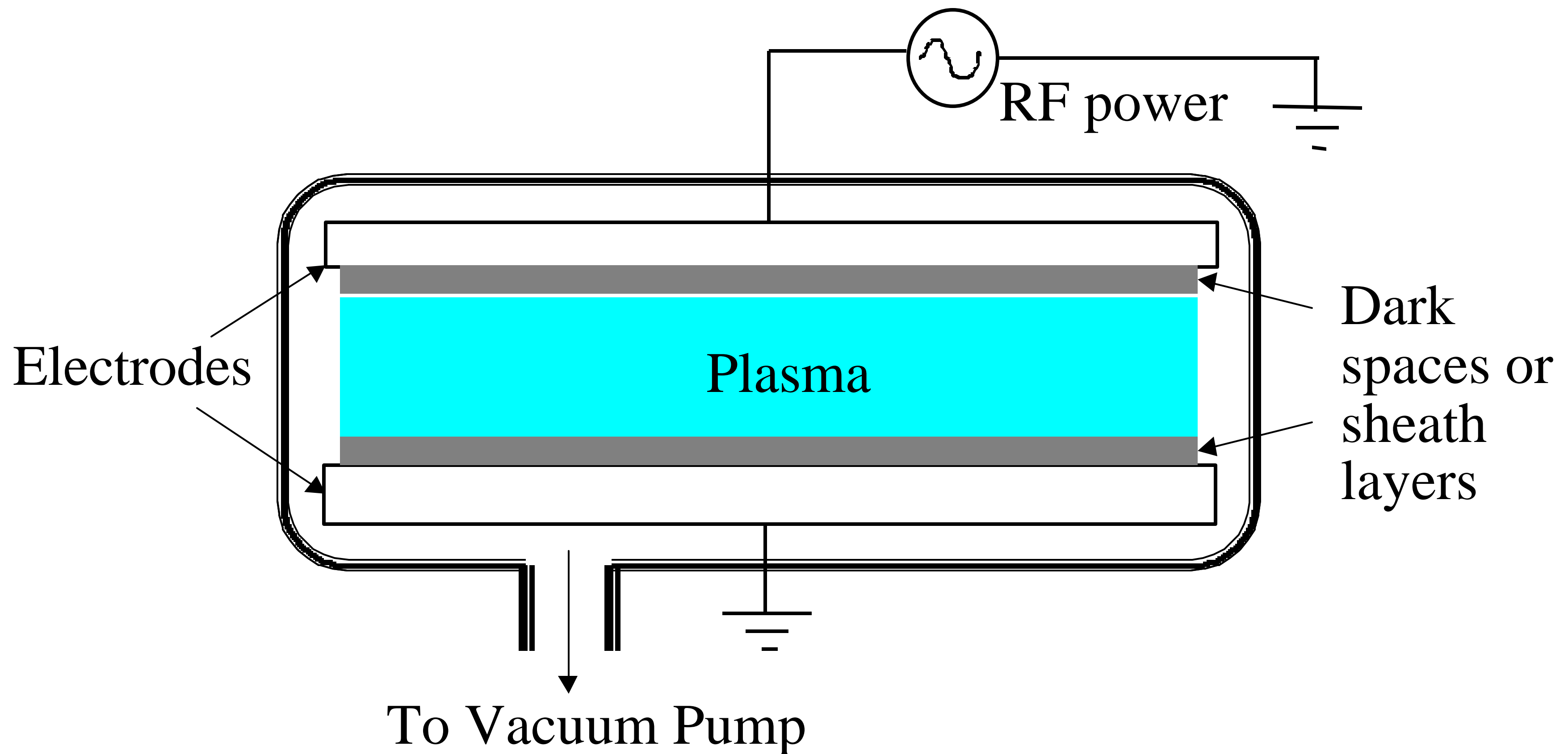
Ionization Rate

- Ionization rate is mainly determined by electron energy in plasma
- In most plasma processing chambers, the ionization rate is less than 0.001%.
- The ionization rate of high density plasma (HDP) source is much higher, about 1%.
- Ionization rate in the core of sun is ~100%.

Neutral Gas Density

- Idea gas
  - 1 mole = 22.4 Litter = 2.24×10^4 cm^3
  - 1 mole = 6.62×10^{23} molecules
- At 1 atm, gas density is 2.96×10^{19} cm^{-3}
- At 1 Torr, gas density is 3.89×10^{16} cm^{-3}
- At 1 mTorr, gas density is 3.89×10^{13} cm^{-3}
- RF plasma has very low ionization rate

Parallel Plate Plasma System

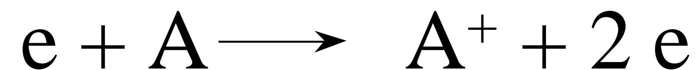


Generation of a Plasma

- External power is needed
- Radio frequency (RF) power is the most commonly used power source
- Vacuum system is required to generate a stable RF plasma

Ionization

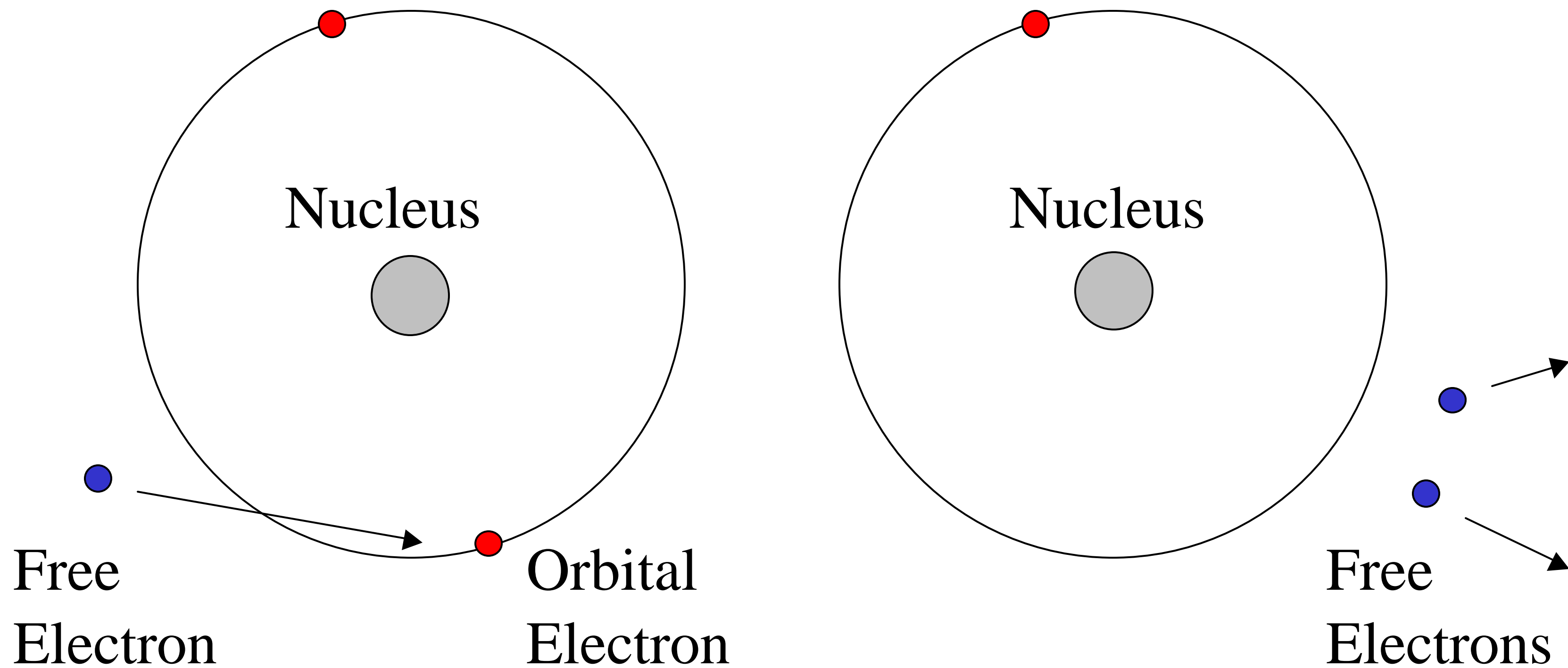
- Electron collides with neutral atom or molecule
- Knock out one of orbital electron



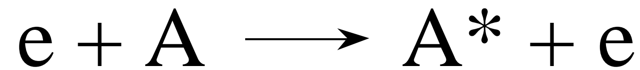
$$e + A \longrightarrow A^{+} + 2\,e$$

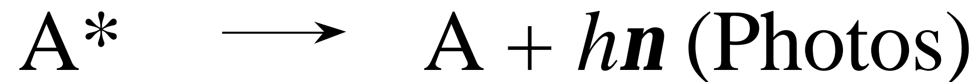
- Ionization collisions generate electrons and ions
- It sustains the stable plasma

Illustration of Ionization



Excitation-Relaxation

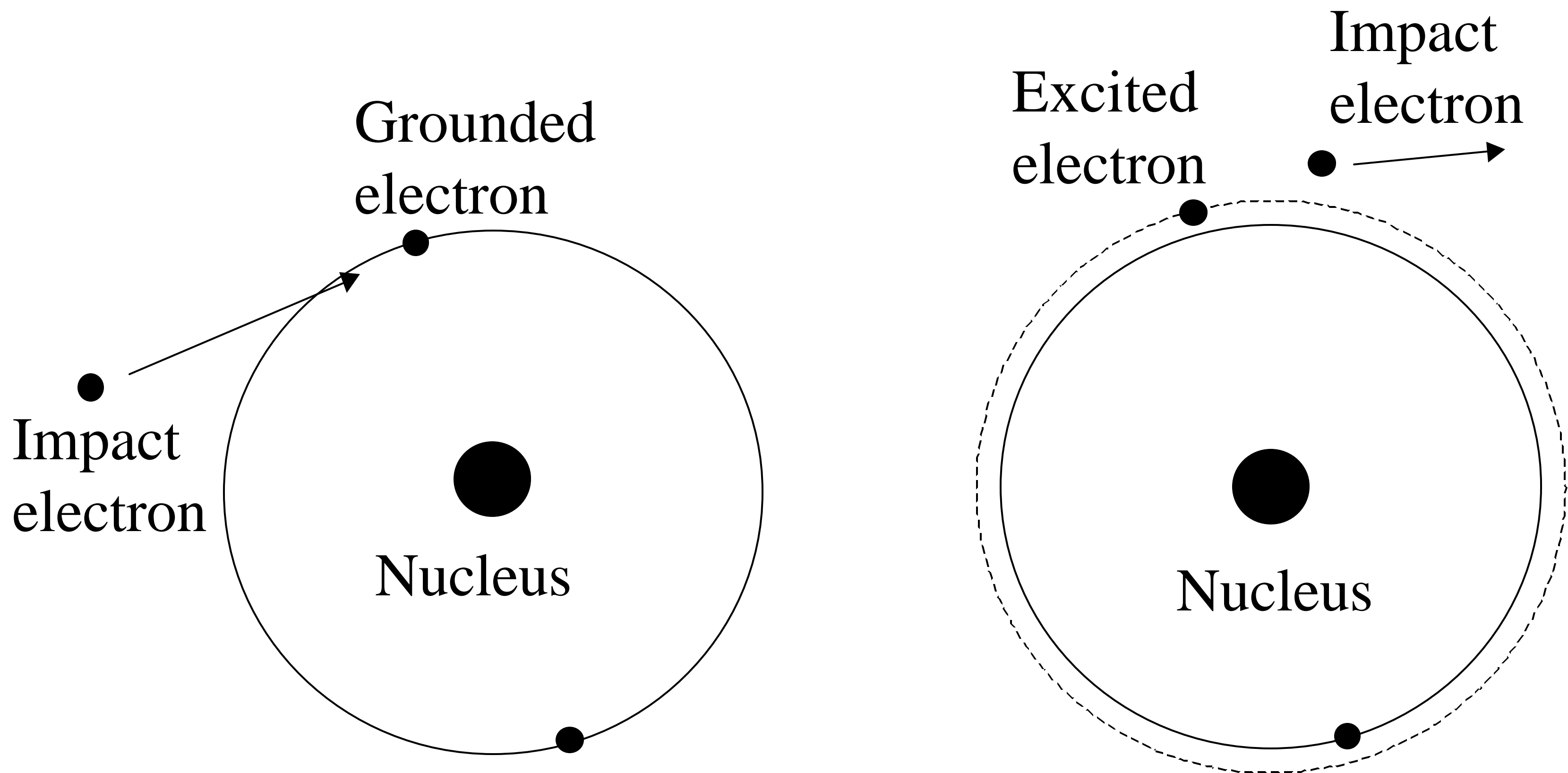




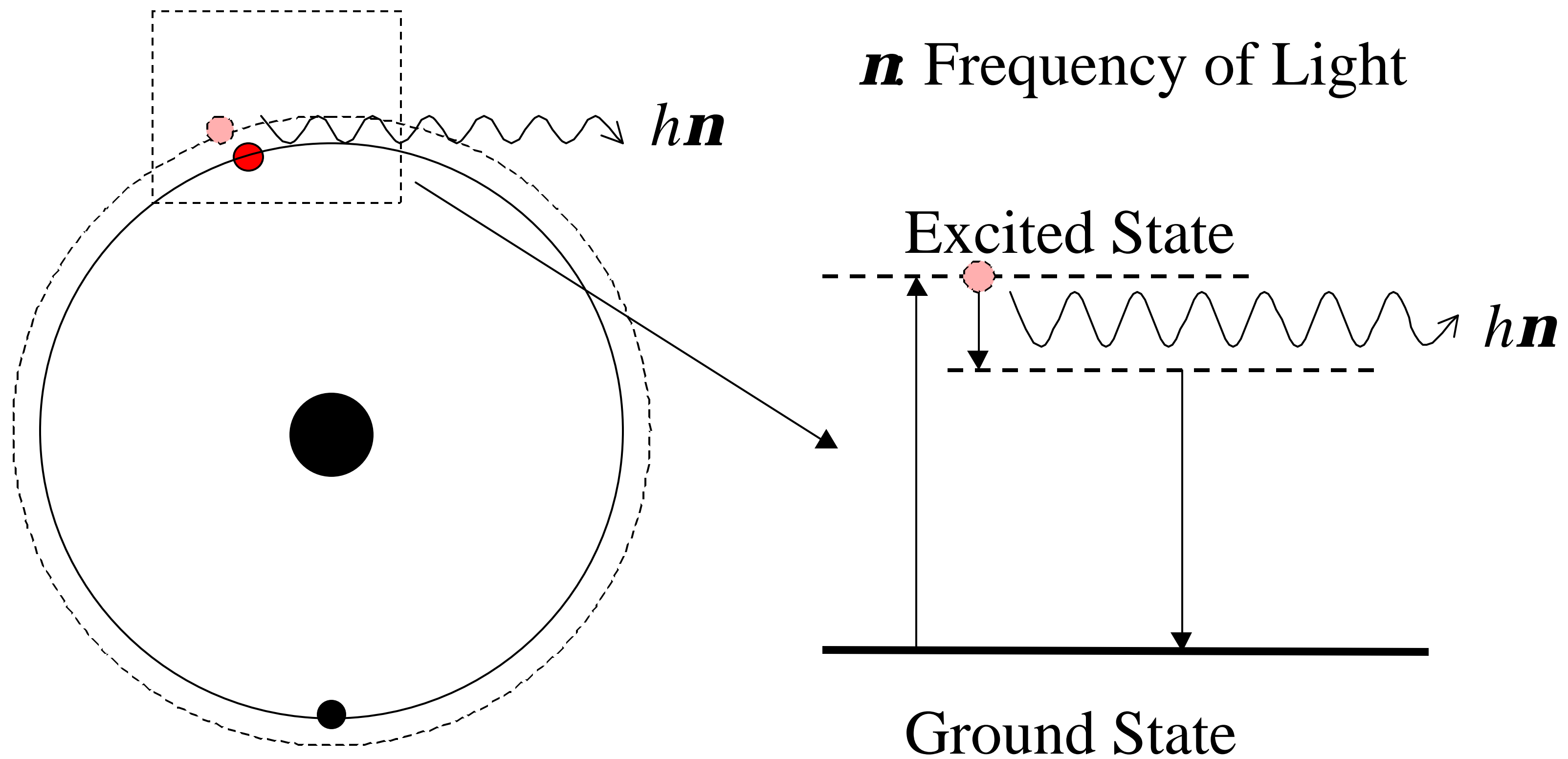
- Different atoms or molecules have difference frequencies, that is why different gases have different glow colors.

- The change of the glow colors is used for etch and chamber clean process **endpoint**.

Excitation Collision

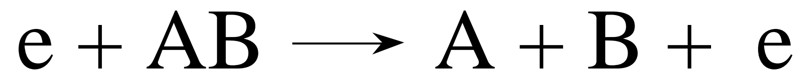


Relaxation



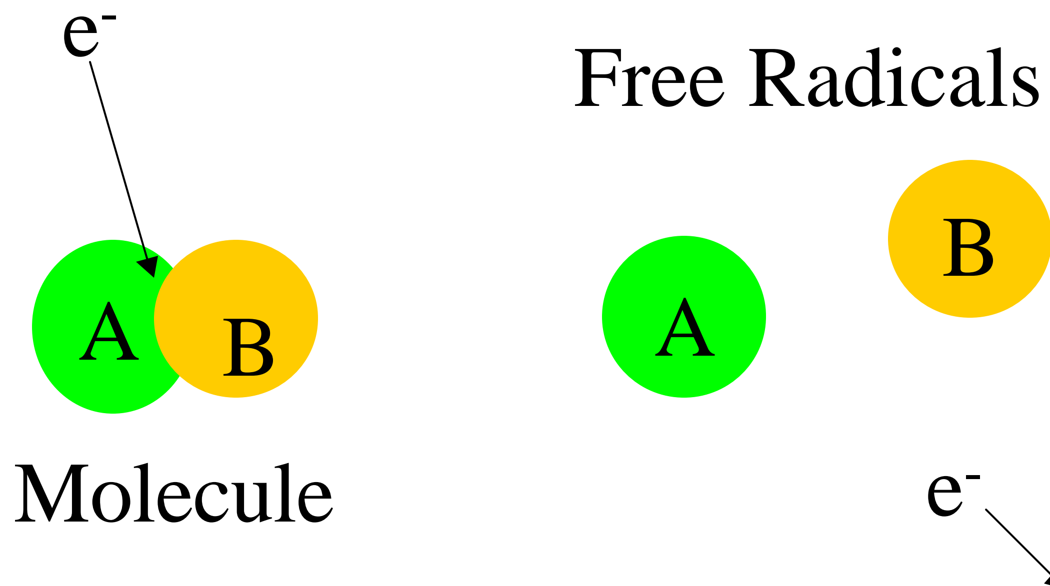
Dissociation

- Electron collides with a molecule, it can break the chemical bond and generate free radicals:



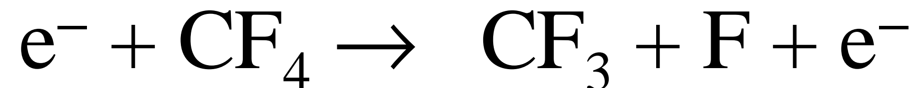
- Free radicals have at least one unpaired electron and are chemically very reactive.
- Increasing chemical reaction rate
- Very important for both etch and CVD.

Dissociation

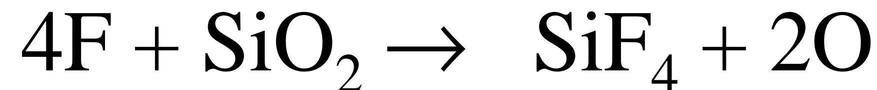


Plasma Etch

- CF_4 is used in plasma to generate fluorine free radical (F) for oxide etch



$$e^- + CF_4 \rightarrow CF_3 + F + e^-$$

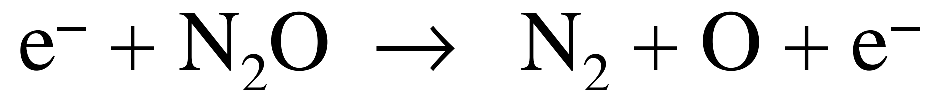


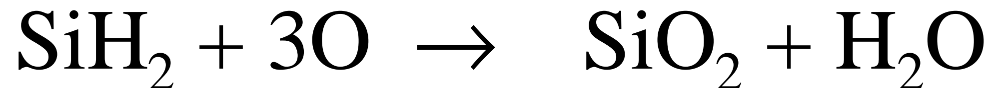
$$4F + SiO_2 \rightarrow SiF_4 + 2O$$

- Enhanced etch chemistry

Plasma **Enhanced** CVD

- PECVD with SiH_4 and NO_2 (laughing gas)





- Plasma enhanced chemical reaction
- PECVD can achieve high deposition rate at relatively lower temperature

Q & A

- Why are dissociation not important in the aluminum and copper PVD processes?

- Aluminum and copper sputtering processes only use argon. Argon is a noble gas, which exist in the form of atoms instead of molecules. Thus there is no dissociation process in argon plasma

Q & A

- Is there any dissociation collision in PVD processes?

- Yes. In TiN deposition process, both Ar and N_2 are used. In plasma, N_2 is dissociated to generate free radical N, which reacts with Ti target to from TiN on the surface. Ar^+ ions sputter TiN molecules from the surface and deposit them on wafer surface.

Table 7.1 Silane Dissociation

Collisions	Byproducts	Energy of Formation
$e^- + SiH_4$	$SiH_2 + H_2 + e^-$	2.2 eV
	$SiH_3 + H + e^-$	4.0 eV
	$Si + 2\ H_2 + e^-$	4.2 eV
	$SiH + H_2 + H + e^-$	5.7 eV
	$SiH_2^* + 2H + e^-$	8.9 eV
	$Si^* + 2H_2 + e^-$	9.5 eV
	$SiH_2^+ + H_2 + 2\ e^-$	11.9 eV
	$SiH_3^+ + H + 2\ e^-$	12.32 eV
	$Si^+ + 2H_2 + 2\ e^-$	13.6 eV
	$SiH^+ + H_2 + H + 2\ e^-$	15.3 eV

Q & A

- Which one of collisions in Table 7.1 is most likely to happen? Why?

- The one that requires the least energy is the one most likely to happen.

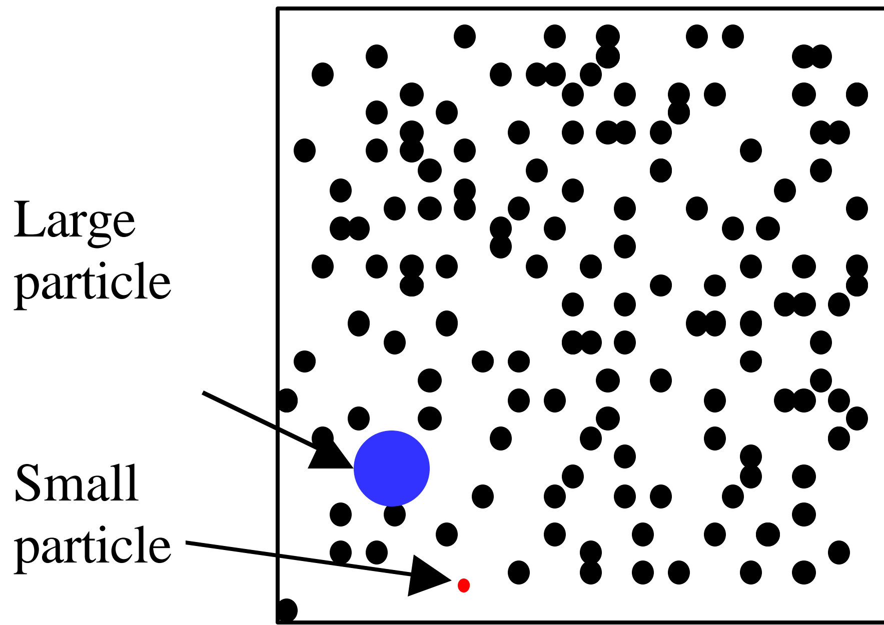
Mean Free Path (MFP)

- The average distance a particle can travel before colliding with another particle.

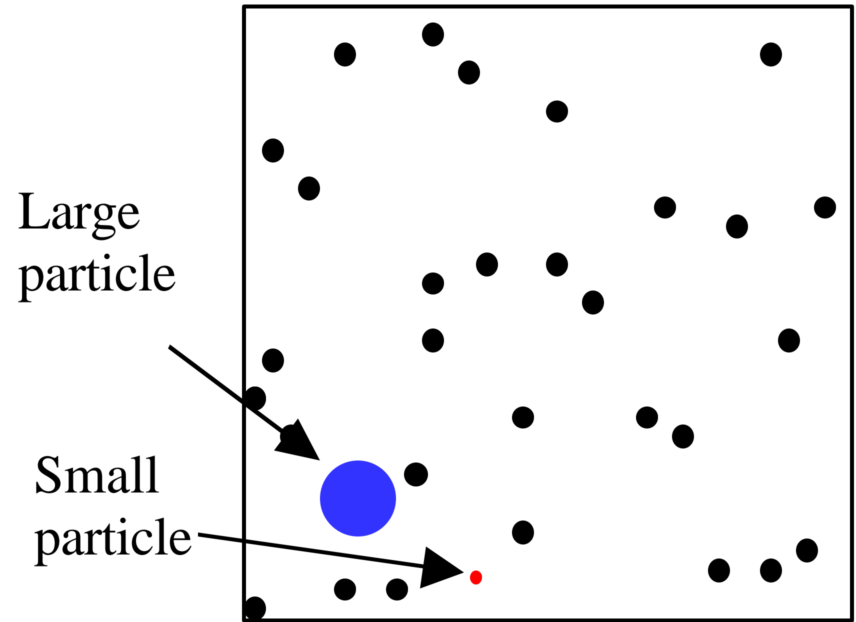
$$\boldsymbol{l} = \frac{1}{n\boldsymbol{s}}$$

- n is the density of the particle
- $\boldsymbol{s}$ is the collision cross-section of the particle

MFP Illustration



(a)



(b)

Mean Free Path (MFP)

- Effect of pressure:

$$\boldsymbol{l} \propto \frac{1}{p}$$

- Higher pressure, shorter MFP

- Lower pressure, longer MFP

Q & A

- Why does one need a vacuum chamber to generate a stable plasma?
- At atmospheric pressure (760 Torr), MFP of an electron is very short. Electrons are hard to get enough energy to ionize gases molecules.
- Extremely strong electric field can create plasma in the form of arcing (lightening) instead of steady state glow discharge.

Movement of Charged Particle

- Electron is much lighter than ion

$$m_e << m_i$$

$$m_e : m_{Hydrogen} = 1:1836$$

- Electric forces on electrons and ions are the same

$$F = qE$$

- Electron has much higher acceleration

$$a = F/m$$

Movement of Charged Particle

- RF electric field varies quickly, electrons are accelerated very quickly while ions react slowly
- Ions have more collisions due to their larger cross-section that further slowing them down
- Electrons move much faster than ions in plasma

Thermal Velocity

- Electron thermal velocity

$$v = (kT_e/m_e)^{1/2}$$

- RF plasma, T_e is about 2 eV

$$v_e \approx 5.93\times10^7 \text{ cm/sec} = 1.33\times10^7 \text{ mph}$$

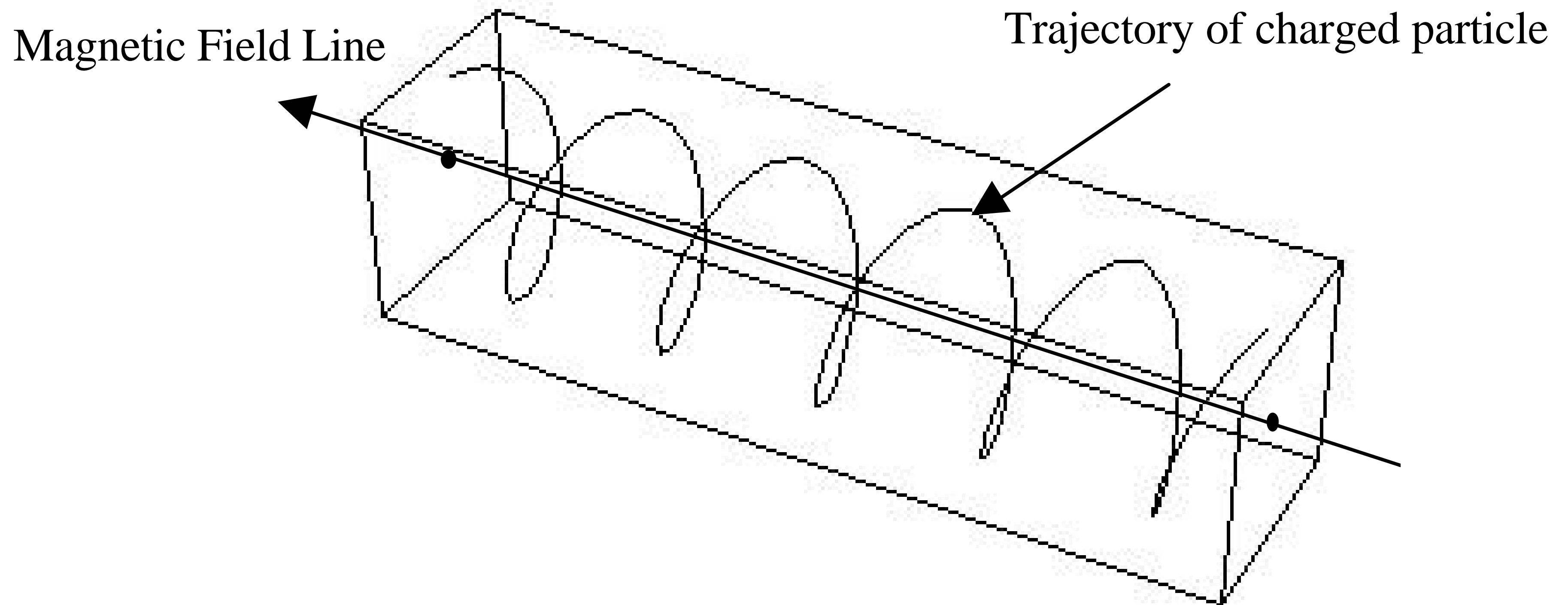
Magnetic Force and Gyro-motion

- Magnetic force on a charged particle:

$$\mathbf{F} = q\mathbf{v}\times\mathbf{B}$$

- Magnetic force is always perpendicular to the particle velocity
- Charged particle will spiral around the magnetic field line.
- Gyro-motion.

Gyro-motion



Gyrofrequency

- Charged particle in gyro motion in magnetic field

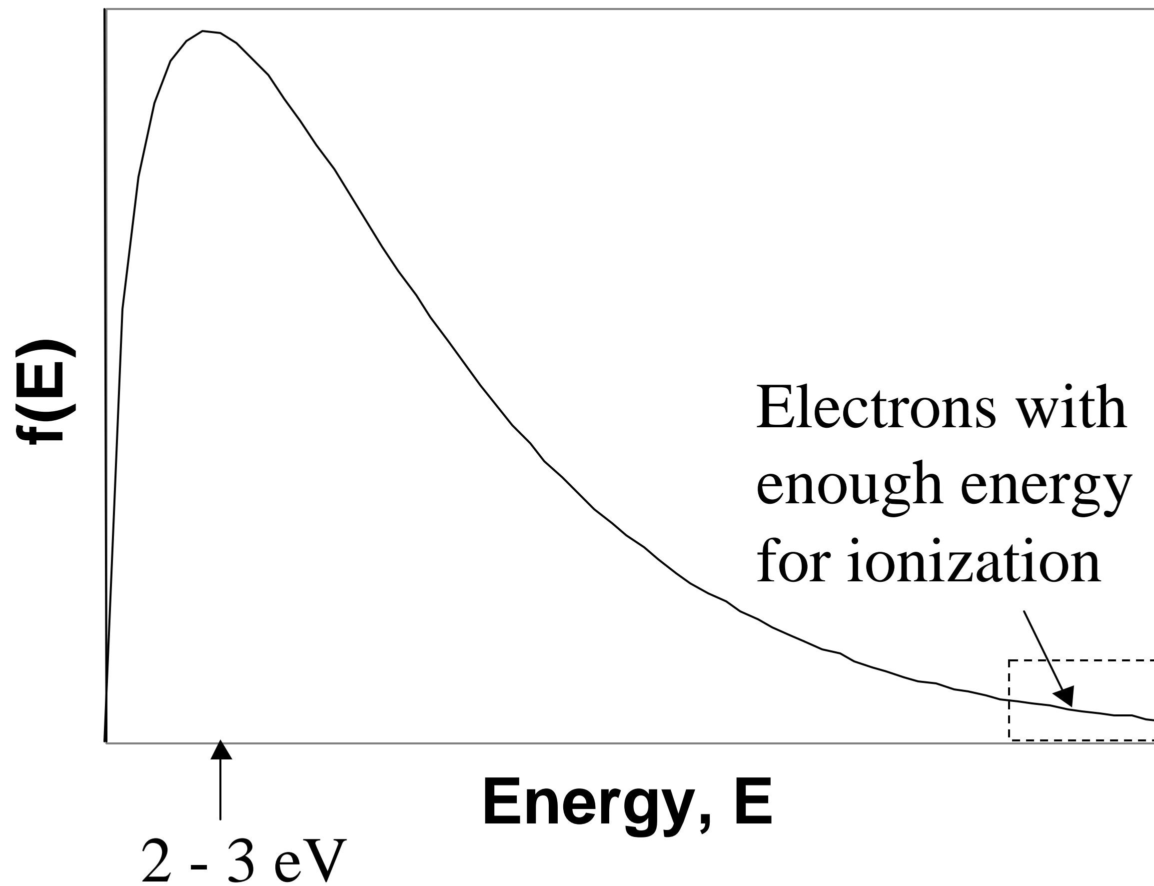
$$\Omega = \frac{qB}{m}$$

Gyro radius

- Gyroradius of charged particle in a magnetic field, $\boldsymbol{r}$, can be expressed as:

$$\boldsymbol{r} = v_{\perp}/\Omega$$

Boltzmann Distribution



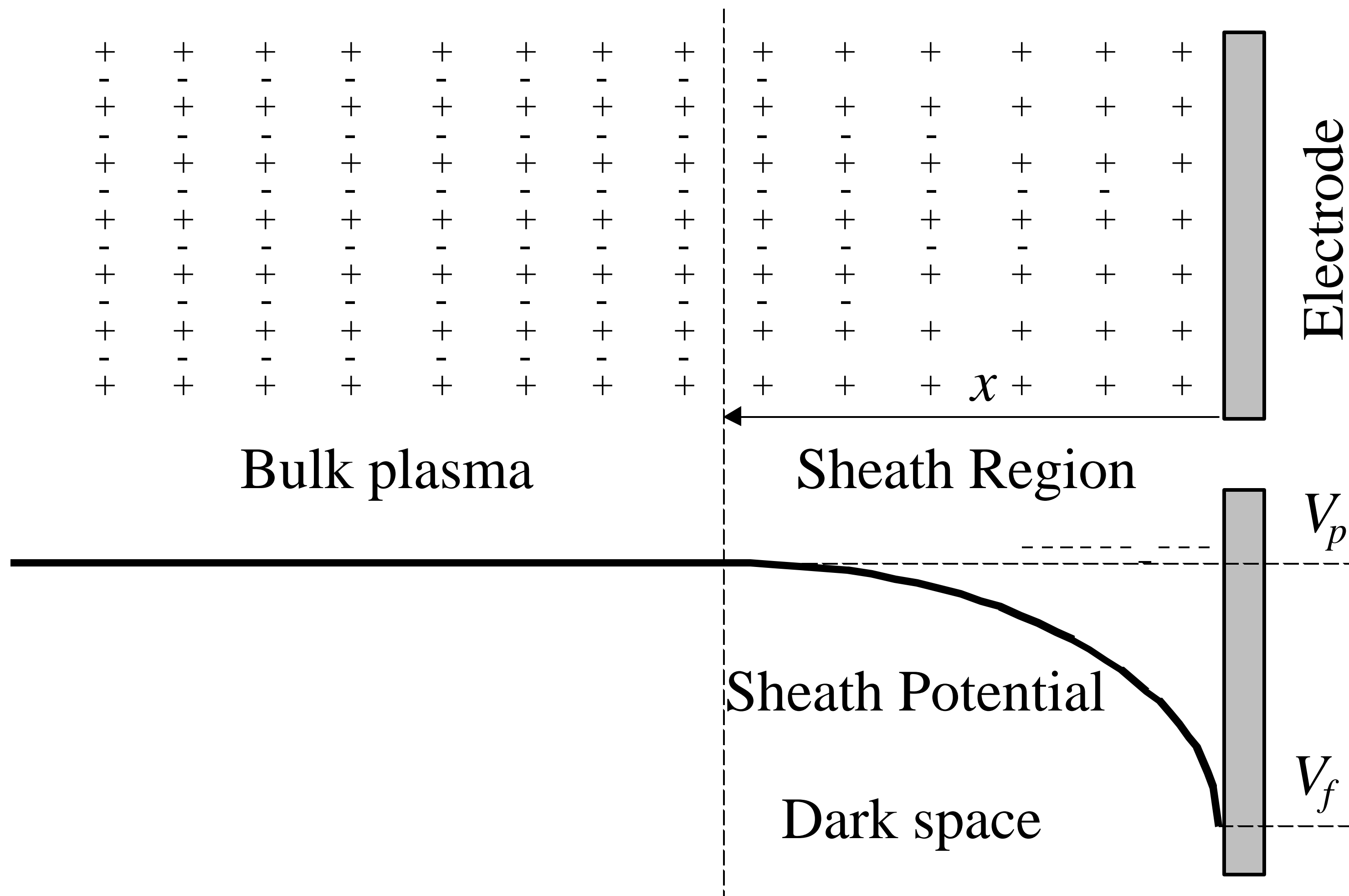
Ion Bombardment

- Anything close to plasma gets ion bombardment
- Very important for sputtering, etch and PECVD
- Mainly determined by RF power
- Pressure also can affect bombardment

Ion Bombardment

- Electrons reach electrodes and chamber wall first
- Electrodes charged negatively, repel electrons and attract ions.
- The sheath potential accelerates ions towards the electrode and causes ion bombardment.
- Ion bombardment is very important for etch, sputtering and PECVD processes.

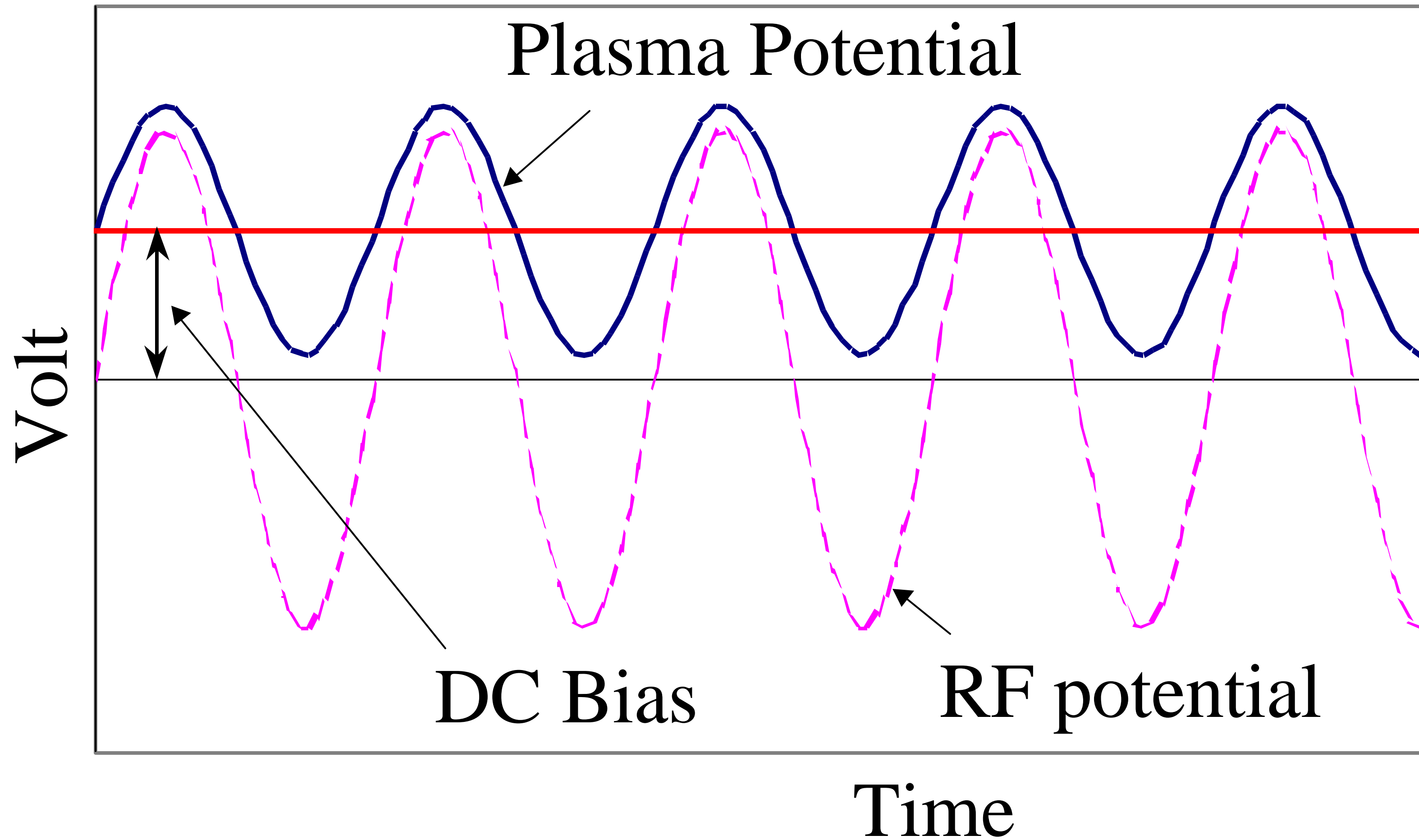
Sheath Potential



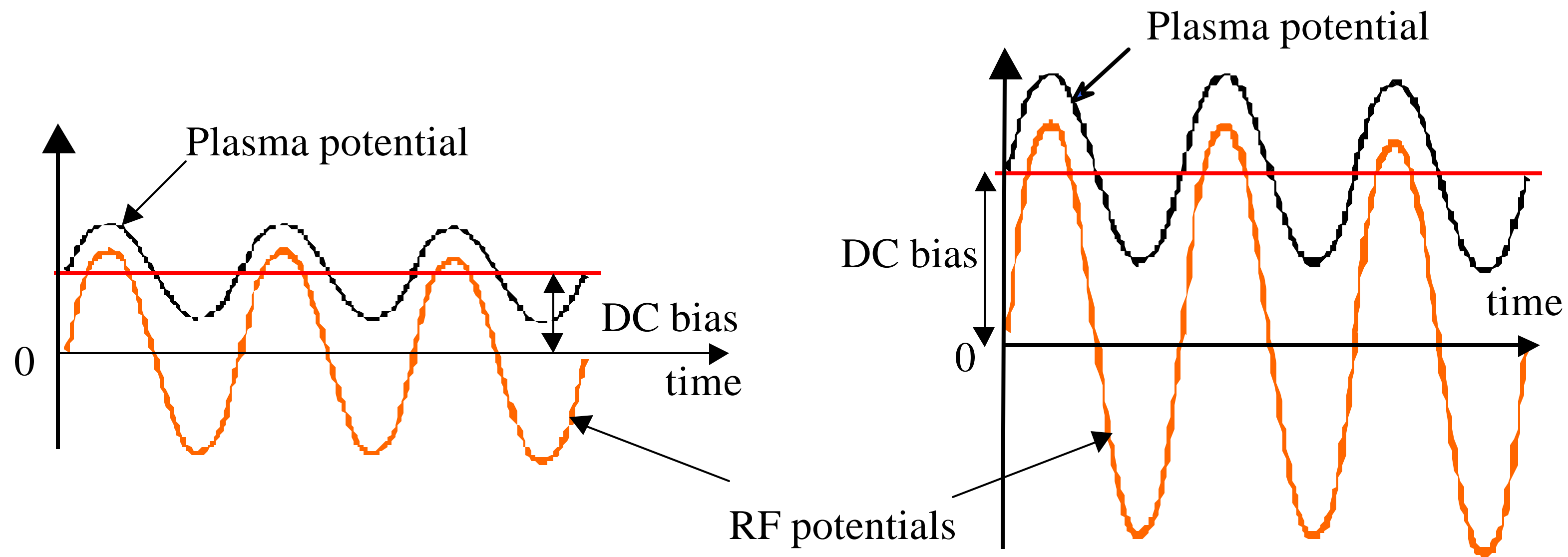
Applications of Ion bombardment

- Help to achieve anisotropic etch profile
  - Damaging mechanism
  - Blocking mechanism
- Argon sputtering
  - Dielectric etch for gap fill
  - Metal deposition
- Help control film stress in PECVD processes
  - Heavier bombardment, more compressive film

Plasma Potential & DC Bias



DC biases and RF powers



- Lower RF power
- Smaller DC bias

- Higher RF power
- Larger DC bias

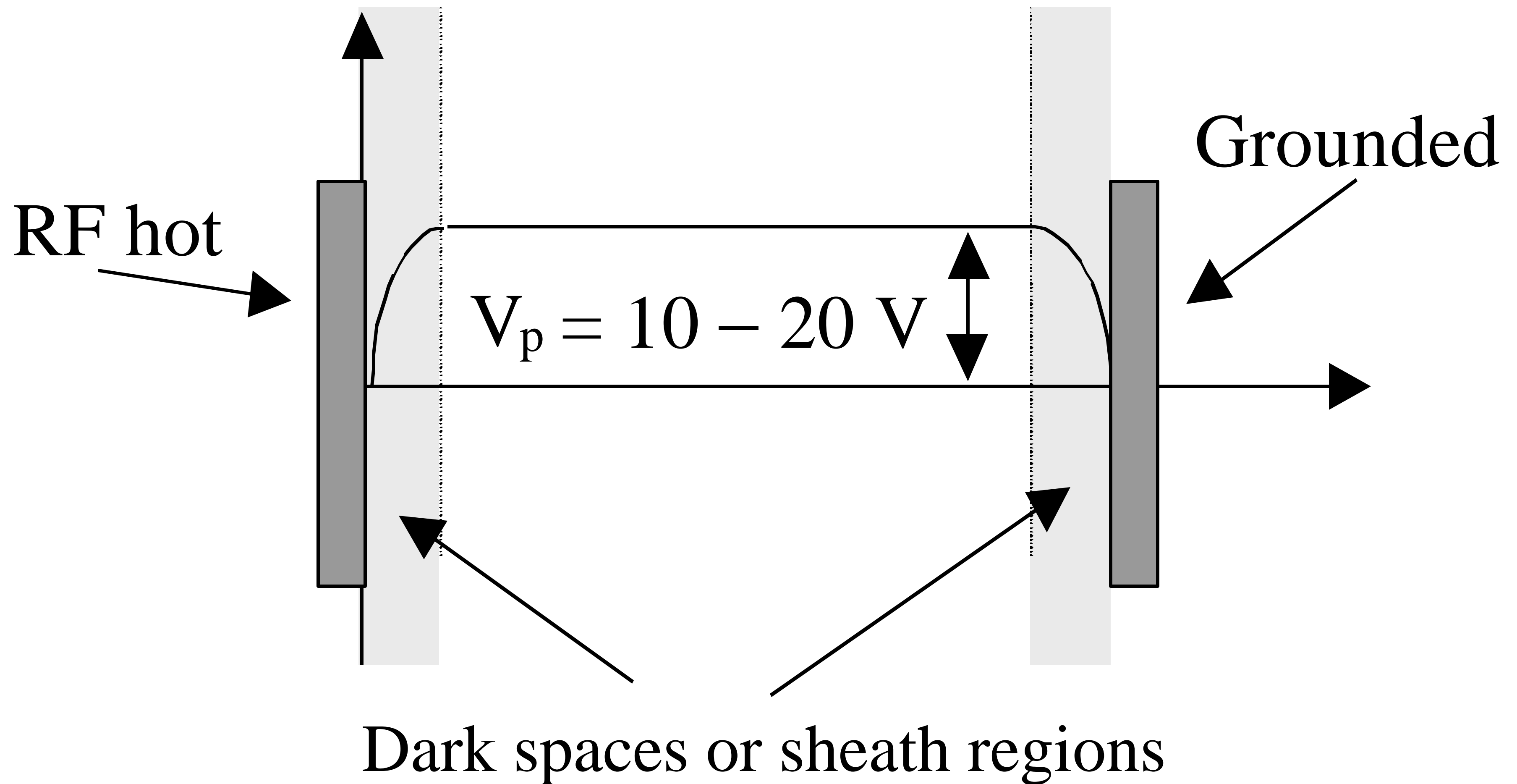
Ion Bombardment

- Ion energy
- Ion density
- Both controlled by RF power

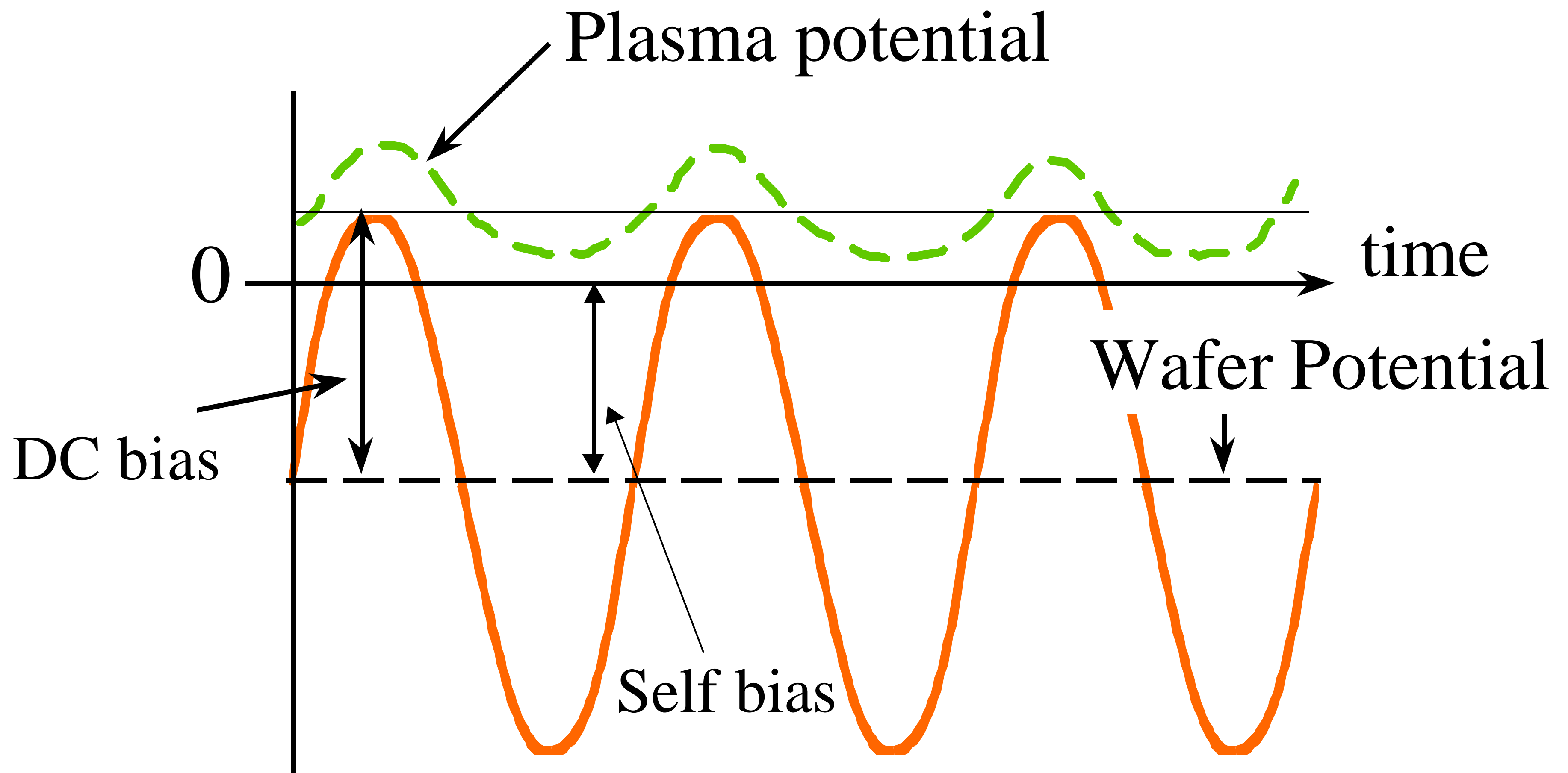
Ion Bombardment Control

- Increasing RF power, DC bias increases, ion density also increases.
- Both ion density and ion bombardment energy are controlled by RF power.
- RF power is the most important knob controlling ion bombardment
- RF power also used to control film stress for PECVD processes

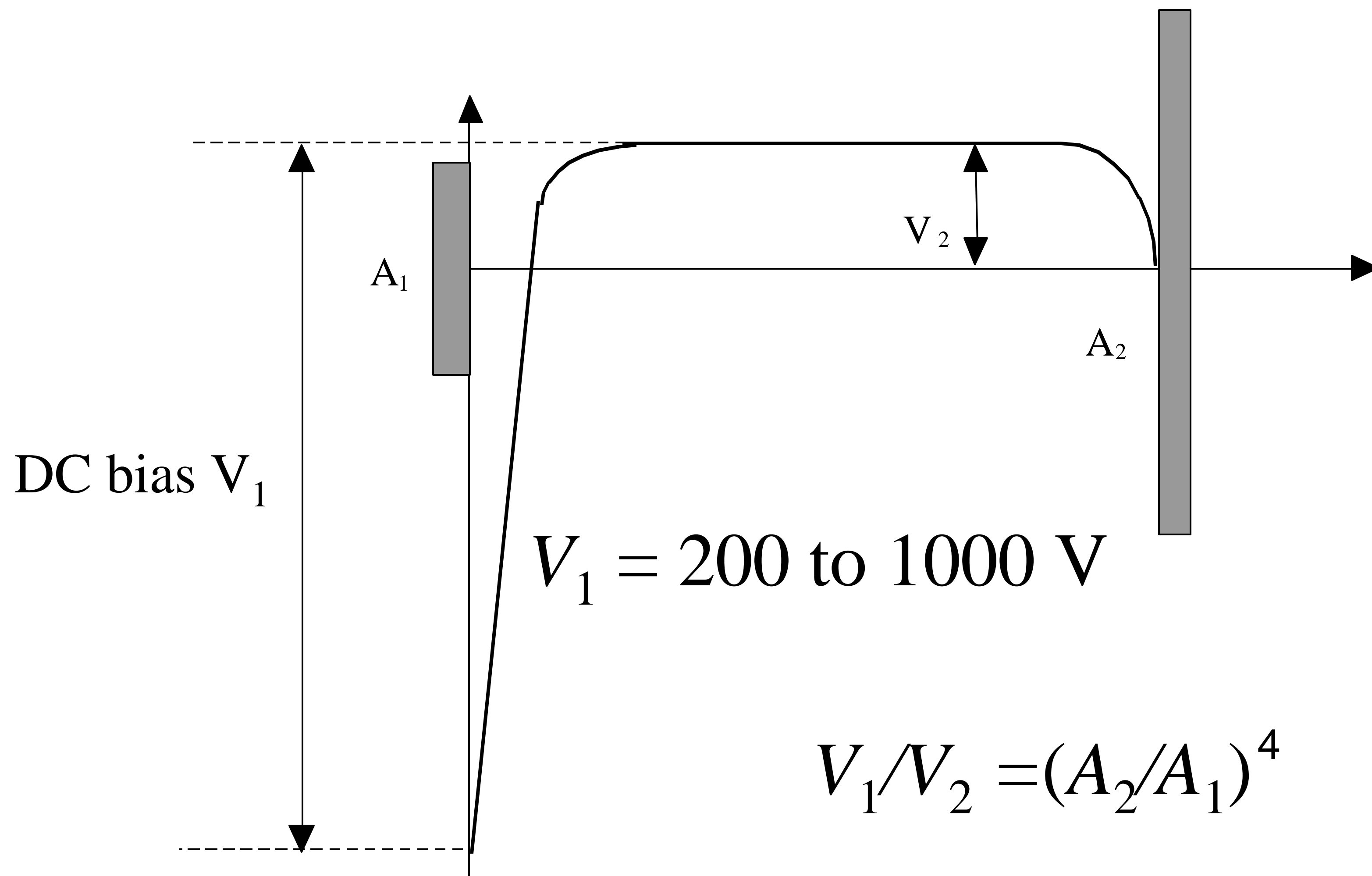
DC Bias of CVD Chamber Plasma



DC Bias of Etch Chamber Plasma



DC Bias of Etch Chamber Plasma



Question and Answer

- If the electrode area ratio is 1:3, what is the difference between the DC bias and the self-bias compare with the DC bias?

- The DC bias is V_1, the self-bias is $V_1 - V_2$, therefore, the difference is

$$[V_1 - (V_1 - V_2)]/V_1 = V_2/V_1 = (A_1/A_2)^4 = (1/3)^4 = 1/81 = 1.23\%$$

Question and Answer

- Can we insert a fine metal probe into the plasma to measure the plasma potential V_2?
- Yes, we can. However, it is not very accurate because of sheath potential near probe surface
- Measurement results are determined by the theoretical models of the sheath potential, which have not been fully developed, yet.

Ion Bombardment and Electrode Size

- Smaller electrode has more energetic ion bombardment due to self-bias
- Etch chambers usually place wafer on smaller electrode

Advantages of Using Plasma

- Plasma processes in IC fabrication:
  - PECVD
    - CVD chamber dry clean
  - Plasma Etch
  - PVD
  - Ion implantation

Benefits of Using Plasma For CVD Process

- High deposition rate at relatively lower temperature.
- Independent film stress control
- Chamber dry clean

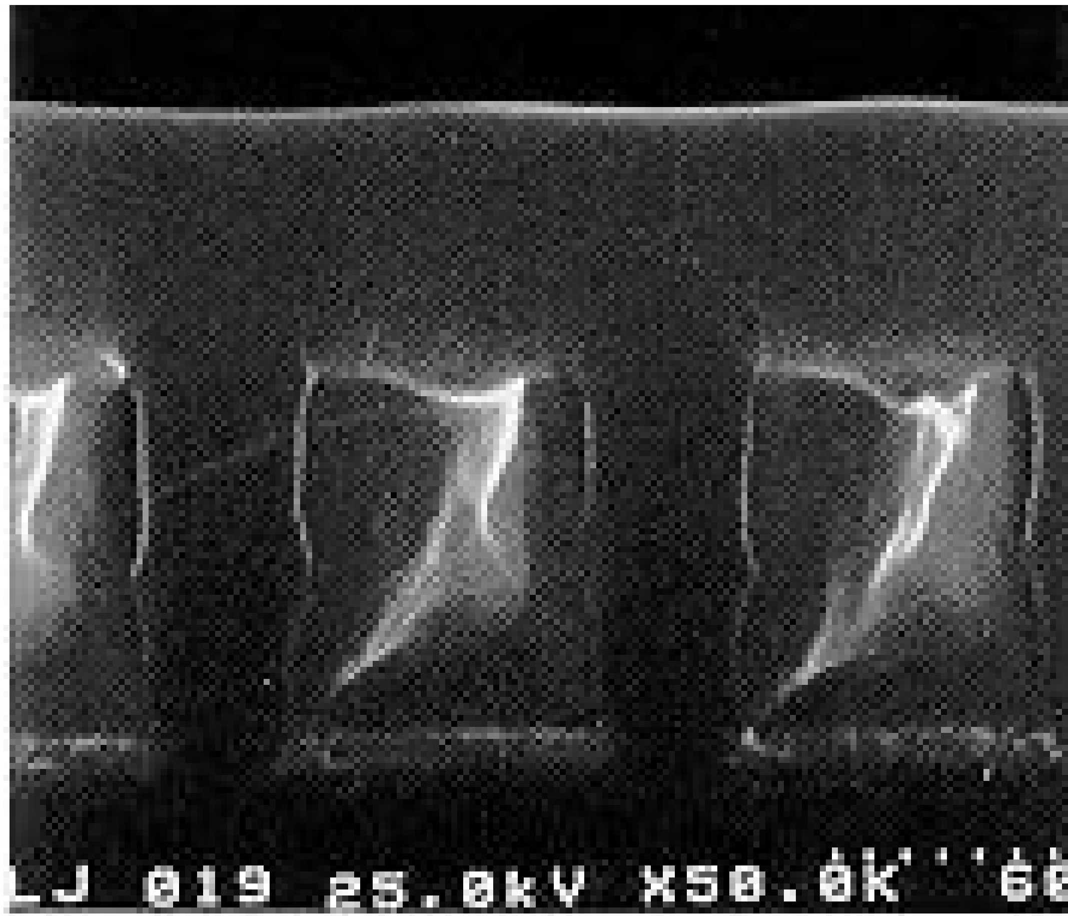
Comparison of PECVD and LPCVD

Processes	**LPCVD (150 mm)**	**PECVD (150 mm)**
Chemical reaction	$SiH_4 + O_2 \rightarrow SiO_2 + \ldots$	$SiH_4 + N_2O \rightarrow SiO_2 + \ldots$
Process parameters	p =3 Torr, T=400 °C	p=3 Torr, T=400 °C and **RF=180 W**
Deposition rate	**100 to 200 Å/min**	**≥ 8000 Å/min**
Process systems	Batch system	Single-wafer system
Wafer to wafer uniformity	Difficult to control	Easier to control

Gap Fill by HDP-CVD

- Simultaneously deposition and sputtering
- Tapering the gap opening
- Fill gap between metal lines bottom up

HDP CVD Void-free Gap Fill



0.25 μm, A/R 4:1

Benefits of Using Plasma For Etch Process

- High etch rate
- Anisotropic etch profile
- Optical endpoint
- Less chemical usage and disposal

Benefits of Using Plasma For PVD Process

- Argon sputtering
- Higher film quality
  - Less impurity and higher conductivity
- Better uniformity
- Better process control
- Higher process integration capability.
- Easier to deposit metal alloy films

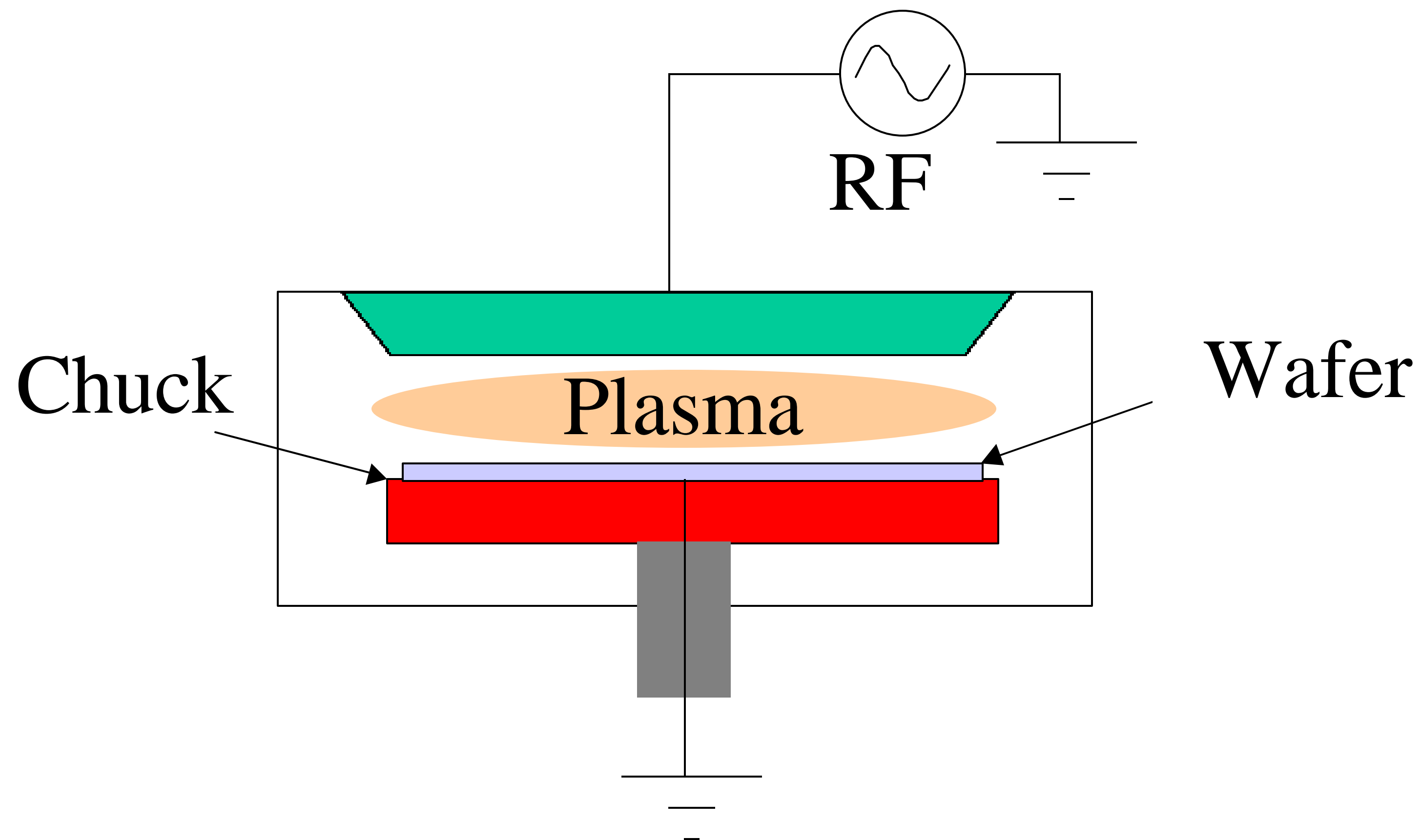
PECVD and Plasma Etch Chambers

- CVD: Adding materials on wafer surface
  - Free radicals
  - Some bombardment for stress control
- Etch: Removing materials from wafer surface
  - Free radicals
  - Heavy bombardment
  - Prefer low pressure, better directionality of ions

PECVD Chambers

- Ion bombardment control film stress
- Wafer is placed grounded electrode
- Both RF hot and grounded electrodes have about the same area
- It has very little self-bias
- The ion bombardment energy is about 10 to 20 eV, mainly determined by the RF power

Schematic of a PECVD Chamber



Plasma Etch Chambers

- Ion bombardment
  - Physically dislodge
  - break chemical bonds
- Wafer on smaller electrode
- Self-bias
- Ion bombardment energy
  - on wafer (RF hot electrode): 200 to 1000 eV
  - on lid (ground electrode): 10 to 20 eV.

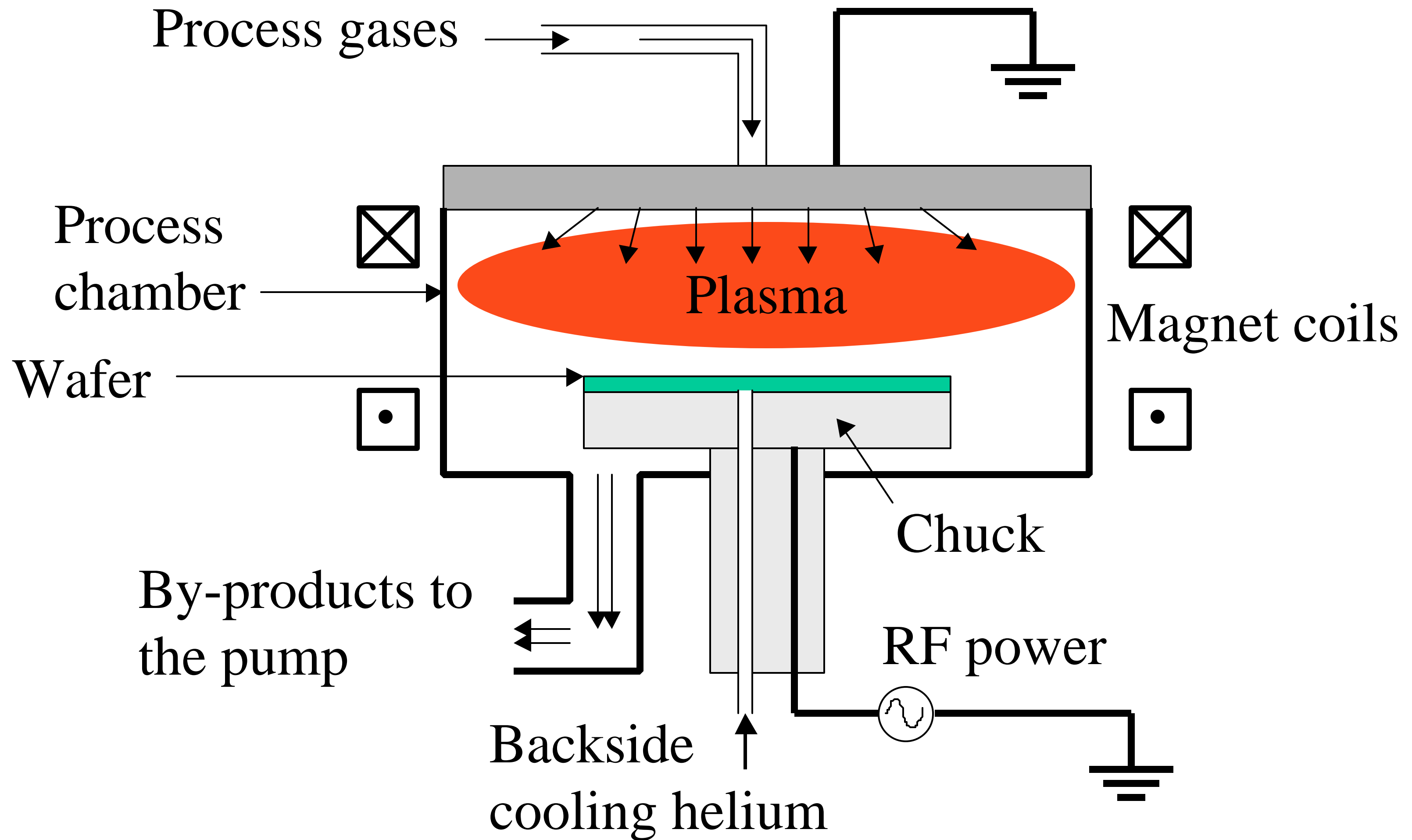
Plasma Etch Chambers

- Heat generation by heavy ion bombardment
- Need control temperature to protect masking PR
- Water-cool wafer chuck (pedestal, cathode)
- Lower pressure not good to transfer heat from wafer to chuck
- Helium backside cooling required
- Clamp ring or electrostatic chuck (E-chuck) to hold wafer

Plasma Etch Chambers

- Etch prefer lower pressure
  - longer MFP, more ion energy and less scattering
- Low pressure, long MFP, less ionization collision
  - hard to generate and sustain plasma
- Magnets are used to force electron spin and travel longer distance to increase collisions

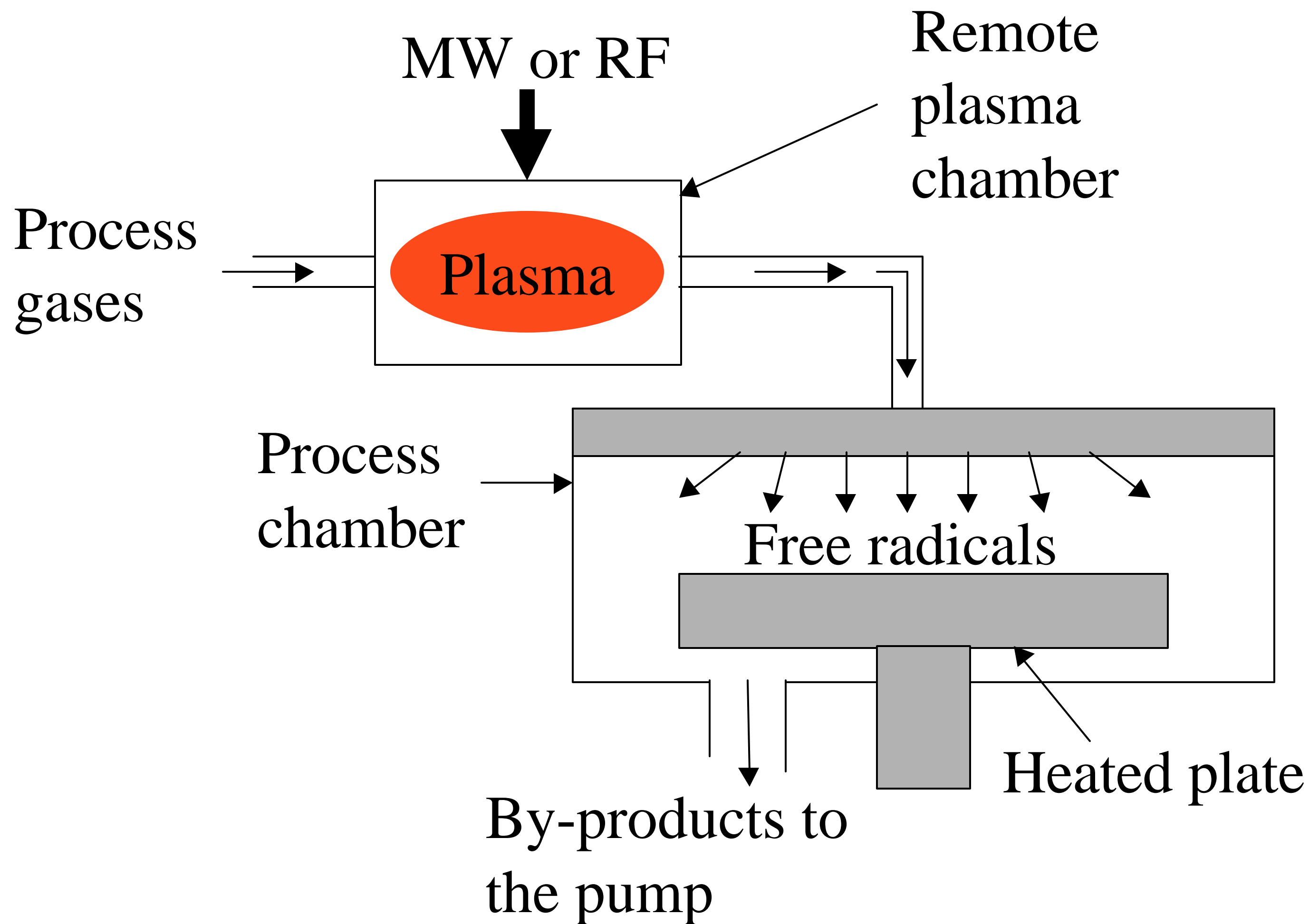
Schematic of an Etch Chamber



Remote Plasma Processes

- Need free radicals
  - Enhance chemical reactions
- Don’t want ion bombardment
  - Avoid plasma-induced damage
- Remote plasma systems

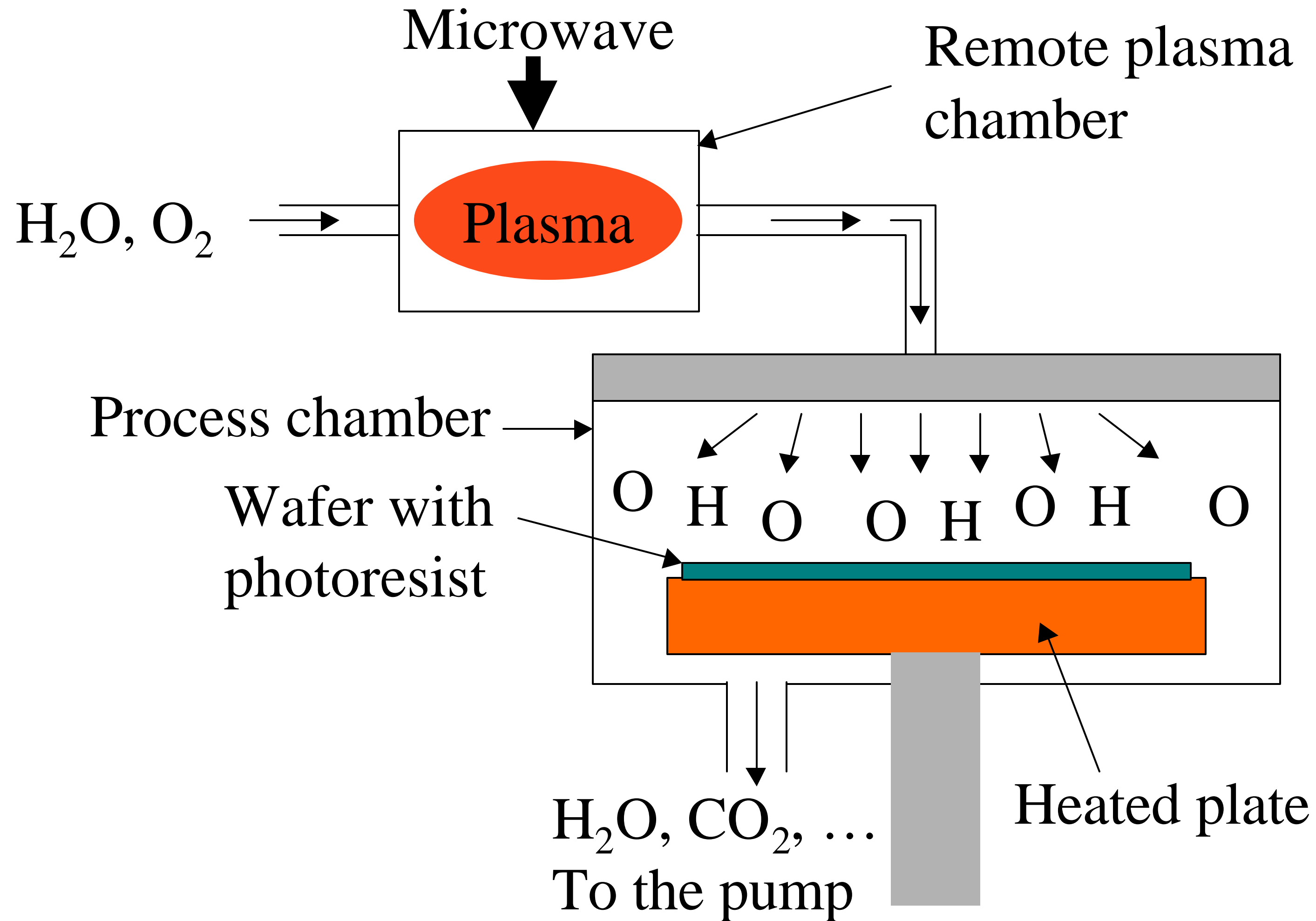
Remote Plasma System



Photoresist Strip

- Remove photoresist right after etch
- O_2 and H_2O chemistry
- Can be integrated with etch system
- In-situ etch and PR strip
- Improve both throughput and yield

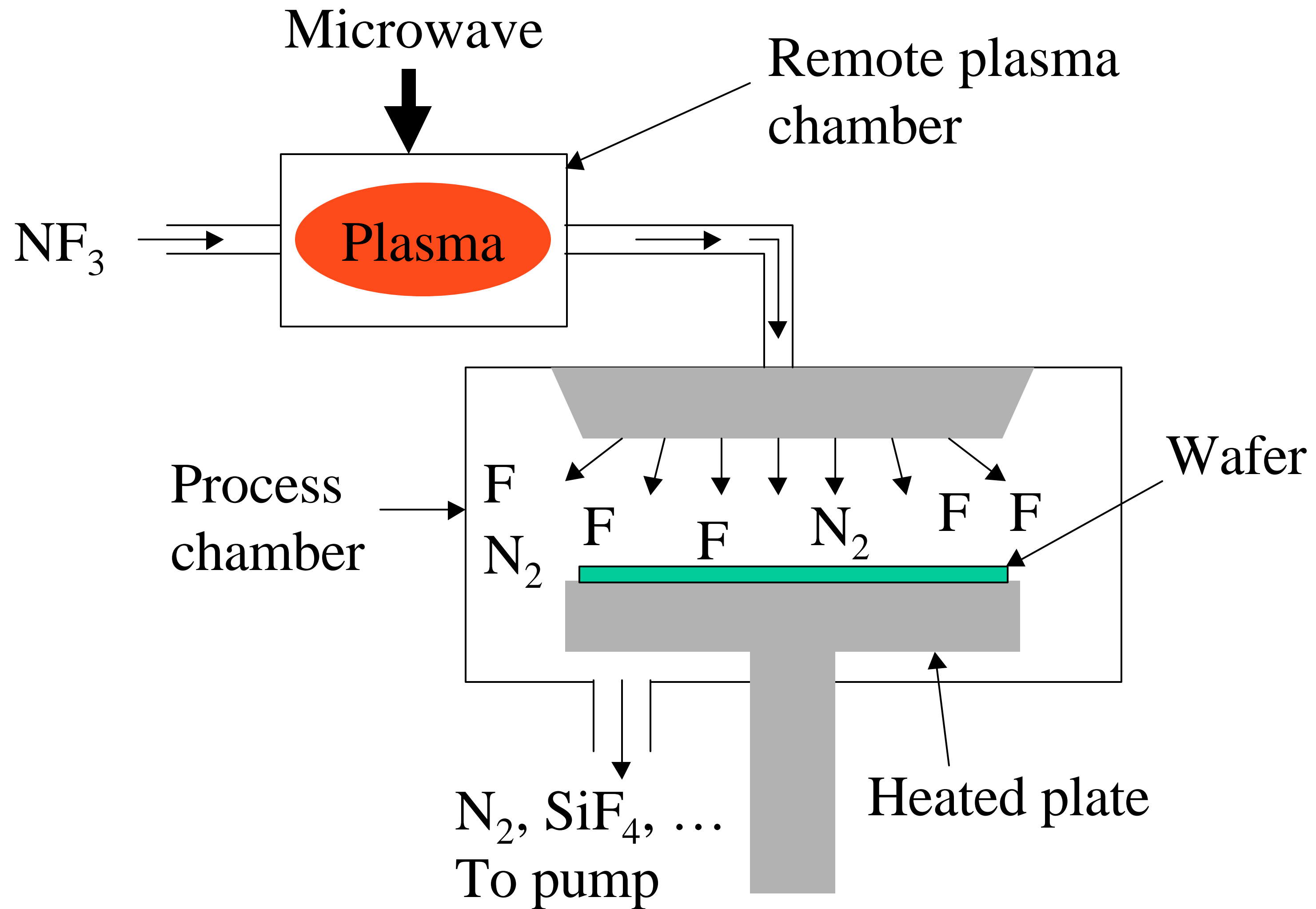
Photoresist Strip Process



Remote Plasma Etch

- Applications: isotropic etch processes:
  - LOCOS or STI nitride strip
  - wineglass contact hole etch
- Can be integrated with plasma etch system
  - improve throughput
- Part of efforts to replace wet process

Remote Plasma Etch System



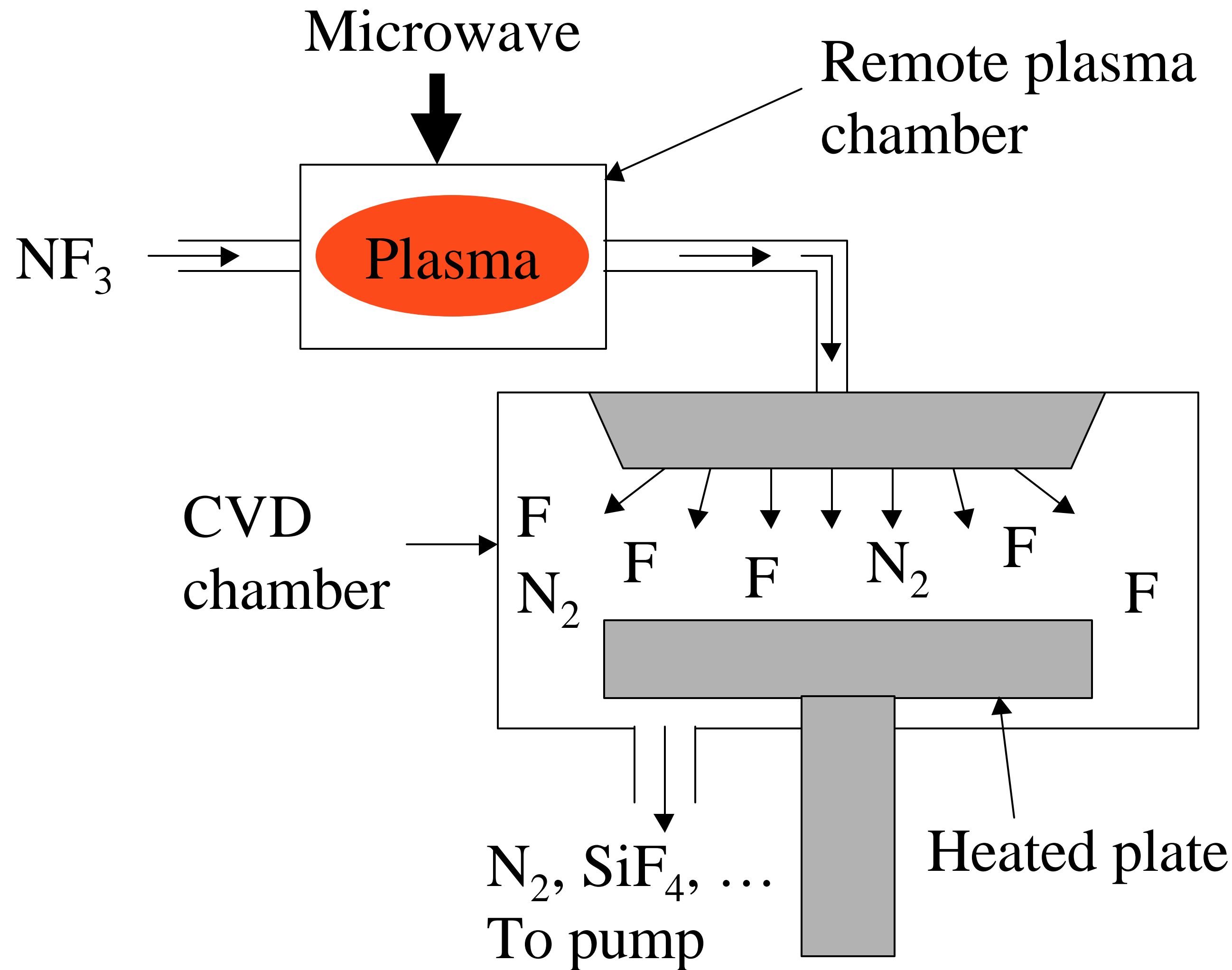
Remote Plasma Clean

- Deposition not only on wafer surface
- CVD chamber need clean routinely
  - Prevent particle contamination due to film crack
- Plasma clean with fluorocarbon gases is commonly used
  - Ion bombardment affects parts lifetime
  - Low dissociation rate of fluorocarbon
  - Environmental concern of fluorocarbon releases

Remote Plasma Clean

- Microwave high-density plasma
- The free radicals flow into CVD chamber
- React and remove deposited film
- Clean the chamber while
  - gentle process, prolonged part lifetime
  - high dissociation, little fluorocarbon releases

Remote Plasma Clean System



Remote Plasma CVD (RPCVD)

- Epitaxial Si-Ge for high-speed BiCMOS
- Still in R&D
- Gate dielectric: SiO_2, SiON, and Si_3N_4
- High-κ dielectrics: HfO_2, TiO_2, and Ta_2O_5
- PMD barrier nitride
  - LPCVD: budget limitations
  - PECVD: plasma induced damage

High-density Plasma

- High-density at low pressure are desired
- Lower pressure longer MFP, less ion scattering, enhances etch profile control.
- Higher density, more ions and free radicals
  - Enhance chemical reaction
  - Increase ion bombardment
- For CVD processes, HDP in-situ, simultaneous dep/etch/dep enhance gap fill

Limitation of Parallel Plate Plasma Source

- Capacitively coupled plasma source
- Can not generate high-density plasma
- Hard to generate plasma even with magnets at low pressure, about a few mTorr.
  - electron MFP too long, no enough ionization collisions.

Limitation of Parallel Plate Plasma Source

- Cannot independently control ion flux and ion energy
- Both are directly related to RF power
- Better process control requires a plasma source that capable to independently control both of them

ICP and ECR

- Most commonly used in IC industry
- Inductively coupled plasma, ICP
  - also called transformer coupled plasma, or TCP
- Electron cyclotron resonance, ECR,
- Low press at few mTorr
- Independently control ion flux and ion energy

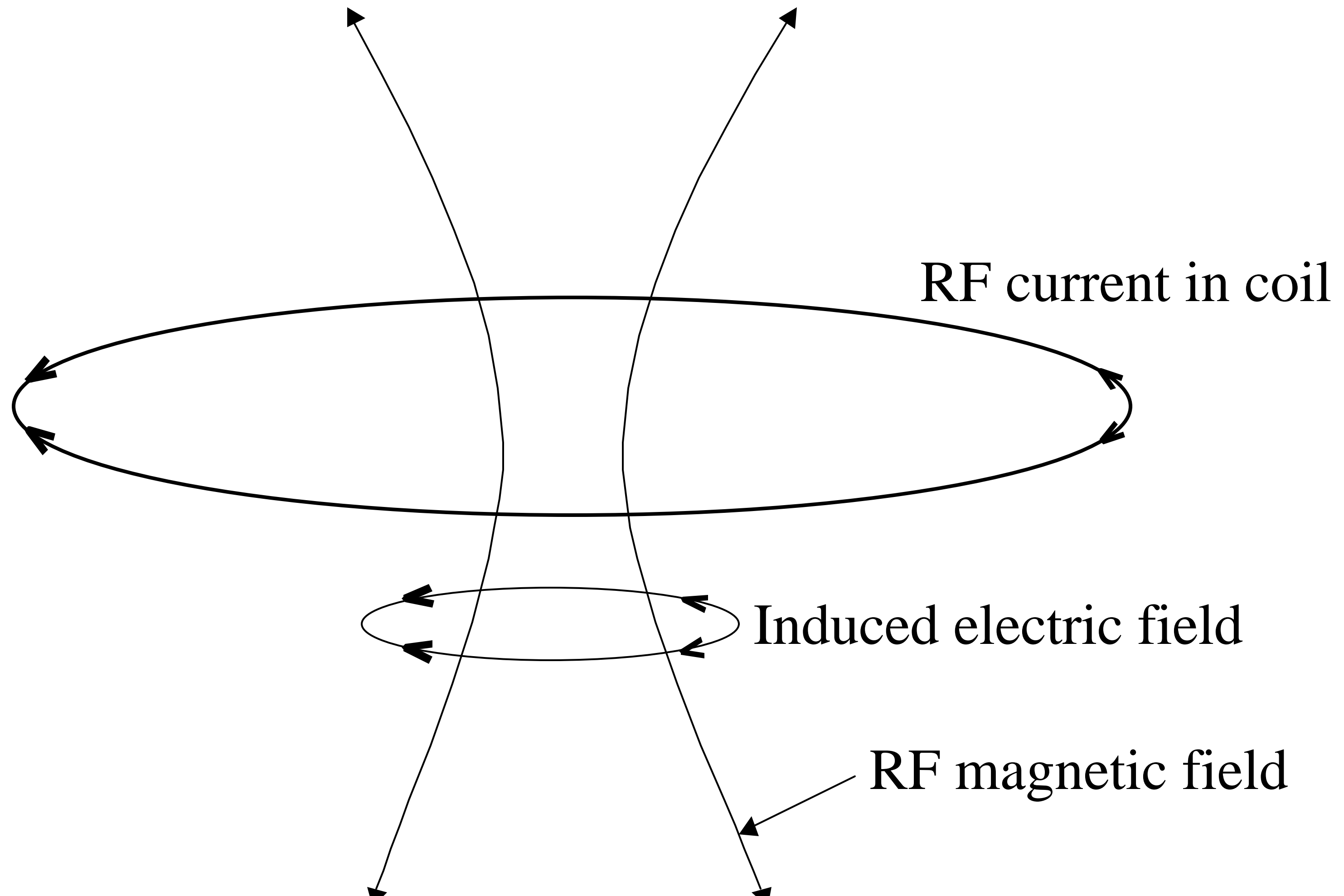
Inductively Coupled Plasma (ICP)

- RF current flows in the coils generates a changing electric field via inductive coupling
- The angular electric field accelerates electrons in angular direction.
- Electrons to travel a long distance without collision with the chamber wall or electrode.
- Ionization collisions generate high-density plasma at low pressure

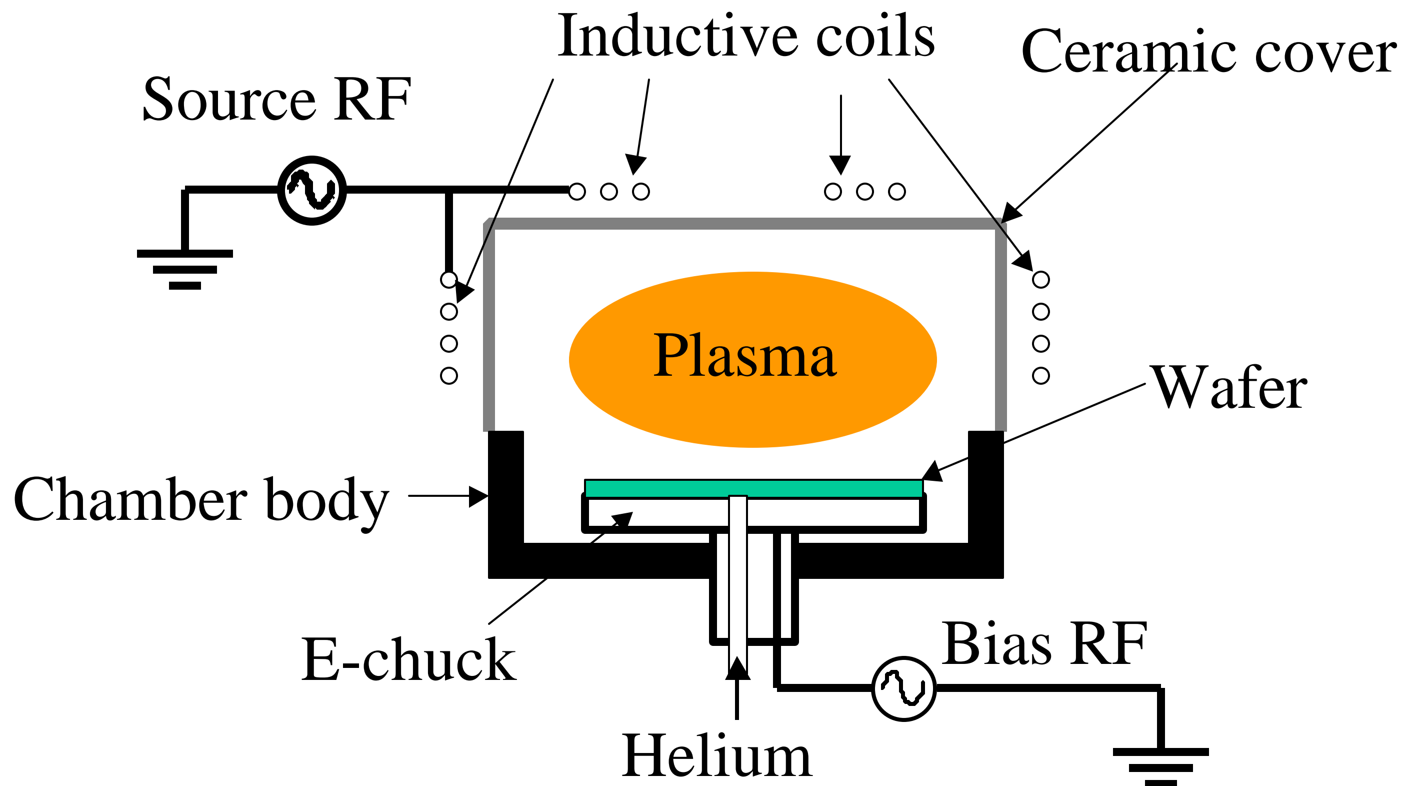
Inductively Coupled Plasma (ICP)

- Bias RF power controls the ion energy
- Source RF power controls the ion flux
- Helium backside cooling system with E-chuck controls wafer temperature

Illustration of Inductive Coupling



Schematic of ICP Chamber



Application of ICP

- Dielectric CVD
- All patterned etch processes
- Sputtering clean prior to metal deposition
- Metal plasma PVD
- Plasma immersion ion implantation

ECR

- Gyro-frequency or cyclotron frequency:

$$\Omega = \frac{qB}{m}$$

- Determined by magnetic field

ECR

- Electron cyclotron resonance when $\omega_{MW} = \Omega_e$
- Electrons get energy from MW
- Energetic electrons collide with other atoms or molecules
- Ionization collisions generate more electrons
- Electrons are spiraling around the field line
- Many collisions even at very low pressure

Illustration of ECR

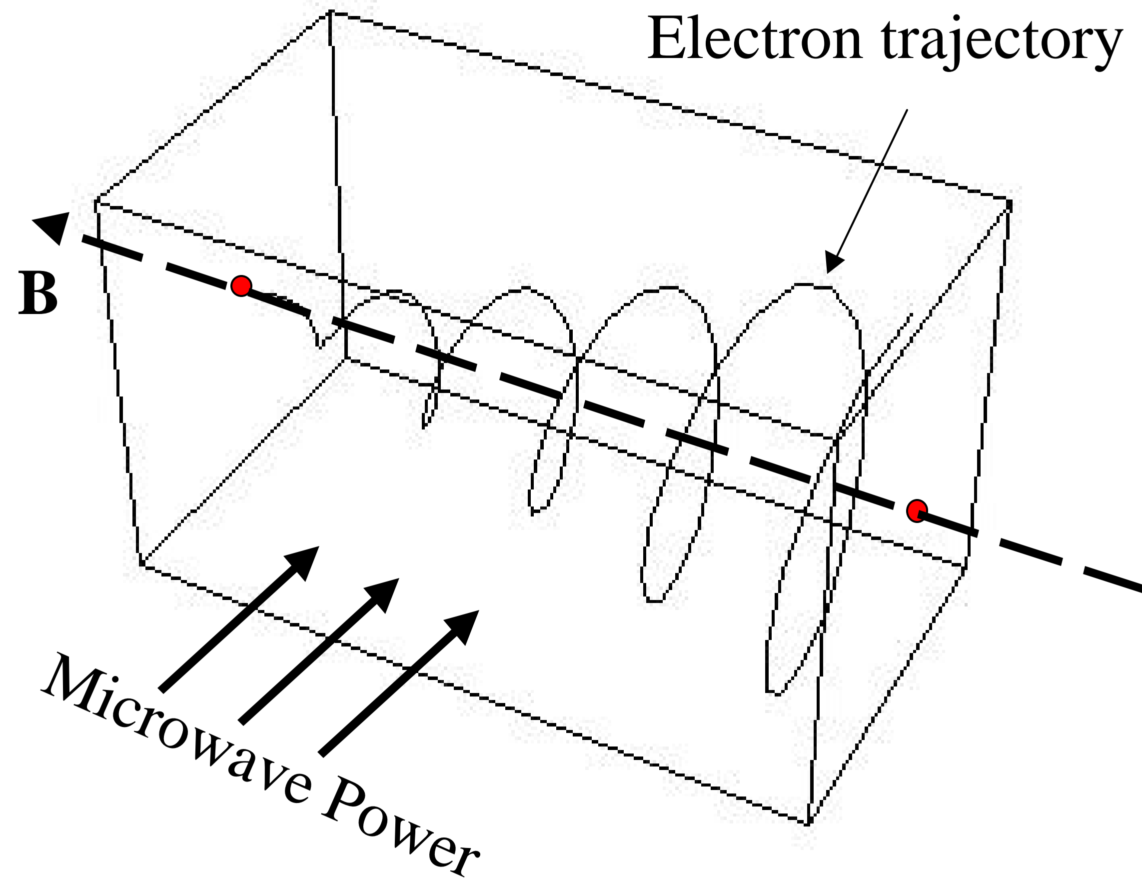
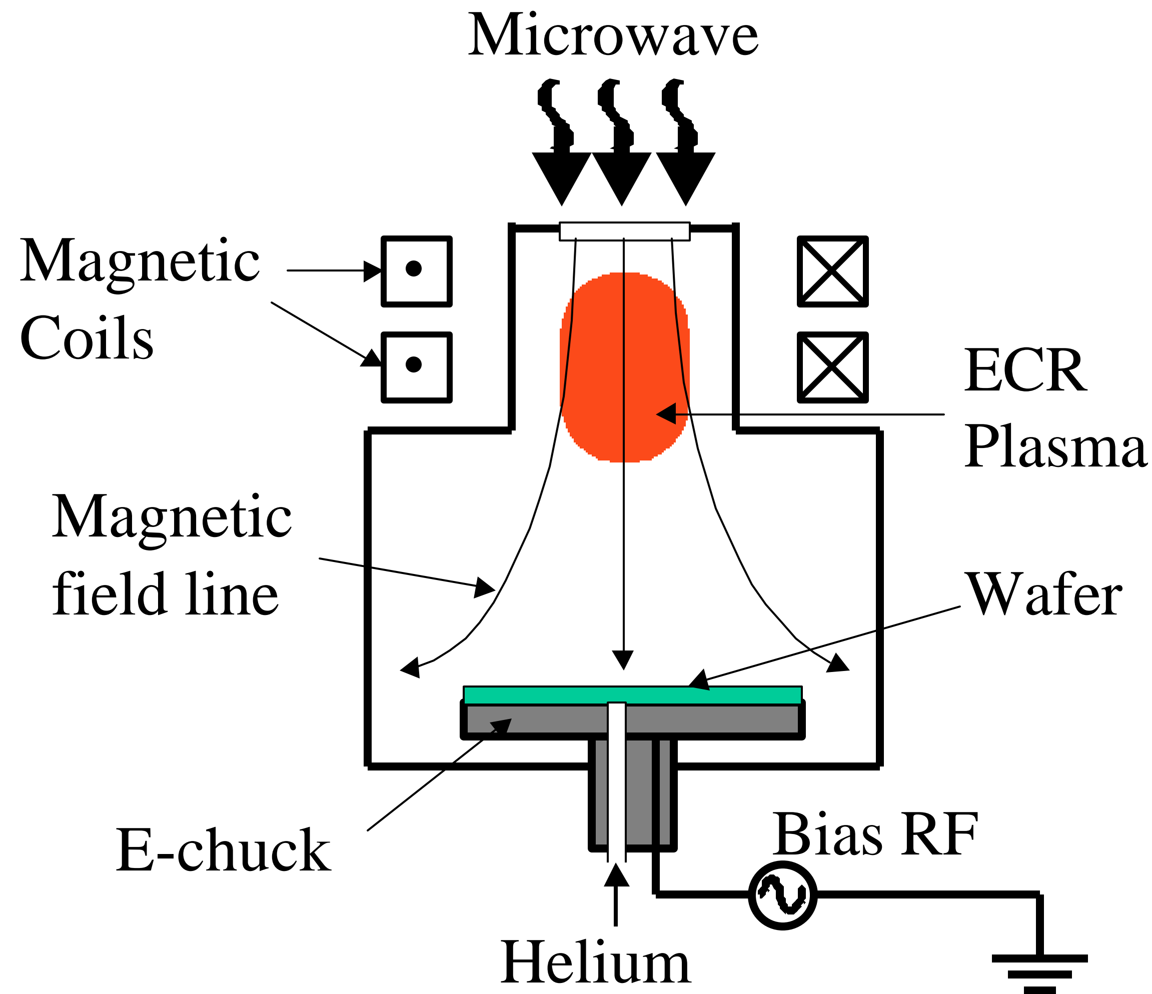


Illustration of ECR



ECR

- Bias RF power controls the ion energy
- Microwave power controls the ion flux
- Magnet coil current controls plasma position and process uniformity
- Helium backside cooling system with E-chuck controls wafer temperature

Application of ECR

- Dielectric CVD
- All patterned etch processes
- Plasma immersion ion implantation

Summary

- Plasma is ionized gas with $n_- = n_+$
- Plasma consist of *n*, *e*, and *i*
- Ionization, excitation-relaxation, dissociation
- Ion bombardment help increase etch rate and achieve anisotropic etch
- Light emission can be used for etch end point
- MFP and its relationship with pressure
- Ions from plasma always bombard electrodes

Summary

- Increasing RF power increases both ion flux and ion energy in capacitive coupled plasmas
- Low frequency RF power gives ions more energy, causes heavier ion bombardment
- The etch processes need much more ion bombardment than the PECVD
- Low pressure, high density plasma are desired
- ICP and ECR are two HDP systems used in IC fabrication

Chapter 8
Ion Implantation

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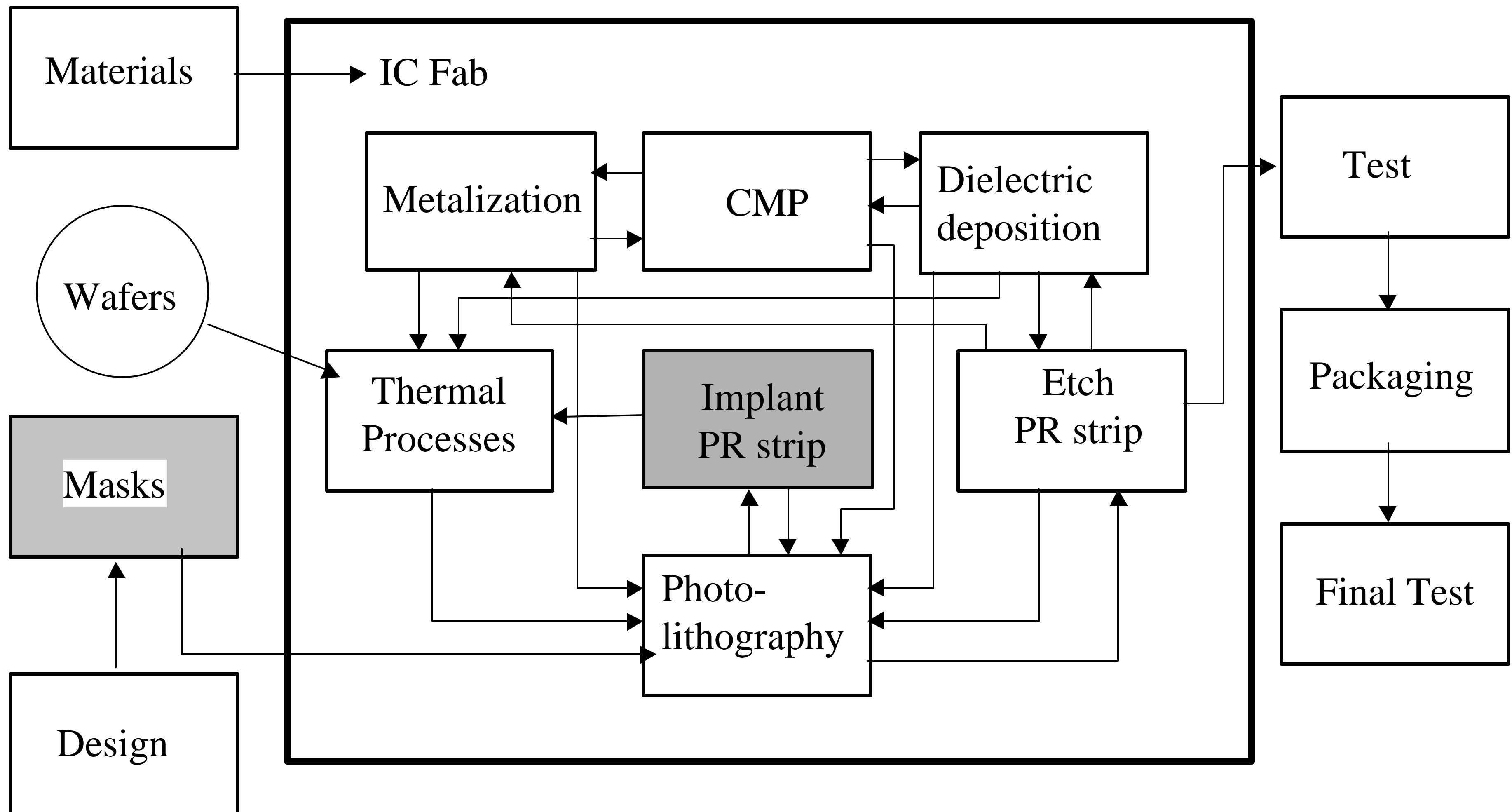
Objectives

- List at least three commonly used dopants
- Identify three doped areas
- Describe the advantages of ion implantation
- Describe major components of an implanter
- Explain the channeling effect
- Relationship of ion range and ion energy
- Explain the post-implantation annealing
- Identify safety hazards

Ion Implantation

- Introduction
- Safety
- Hardware
- Processes
- Summary

Wafer Process Flow



Introduction: Dope Semiconductor

- What is Semiconductor?
- Why semiconductor need to be doped?
- What is n-type dopant?
- What is p-type dopant?

Introduction

- Dope semiconductor
- Two way to dope
  - Diffusion
  - Ion implantation
- Other application of ion implantation

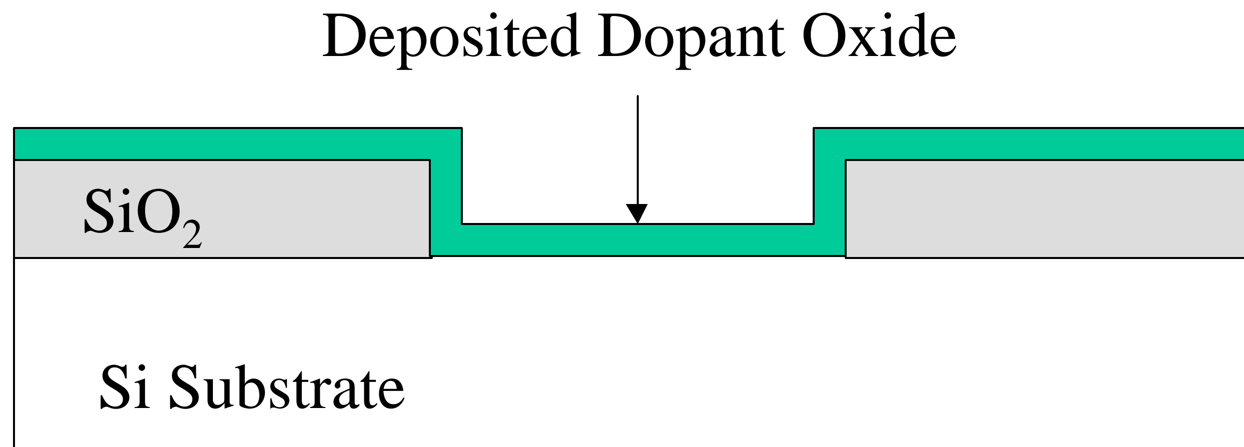
Dope Semiconductor: Diffusion

- Isotropic process
- Can’t independently control dopant profile and dopant concentration
- Replaced by ion implantation after its introduction in mid-1970s.

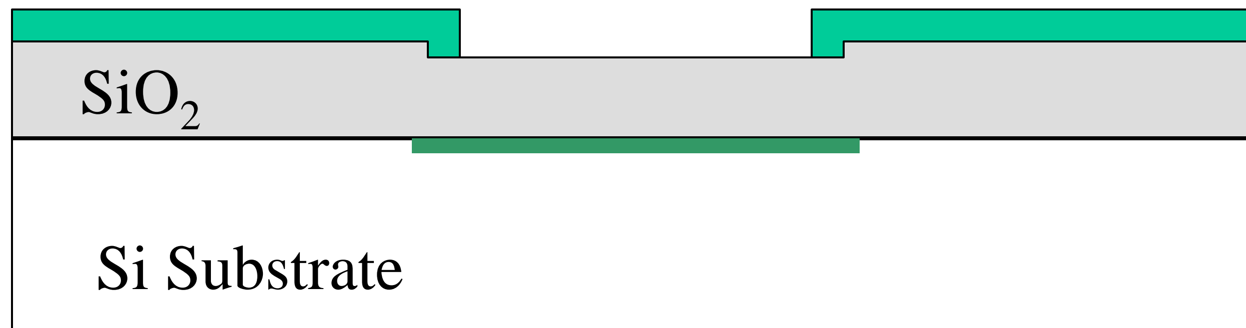
Dope Semiconductor: Diffusion

- First used to dope semiconductor
- Performed in high temperature furnace
- Using silicon dioxide mask
- Still used for dopant drive-in
- R&D on ultra shallow junction formation.

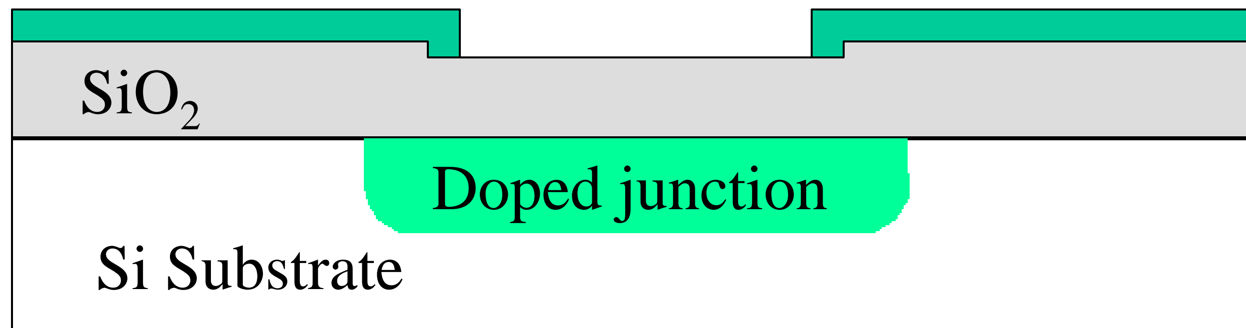
Dopant Oxide Deposition



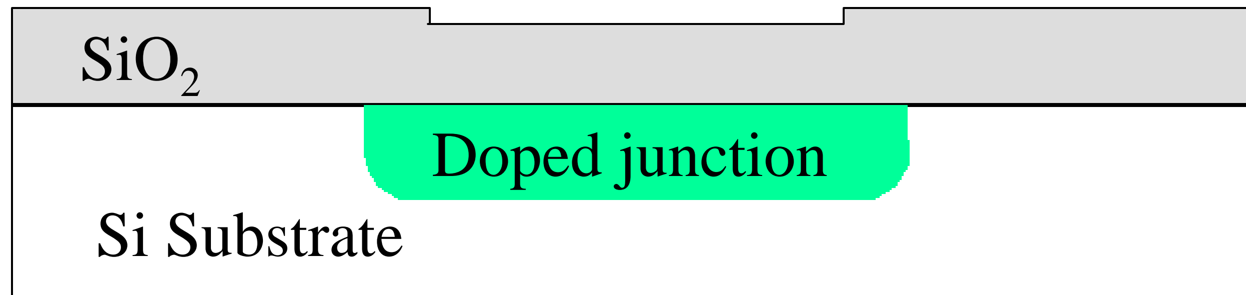
Oxidation



Drive-in



Strip and Clean



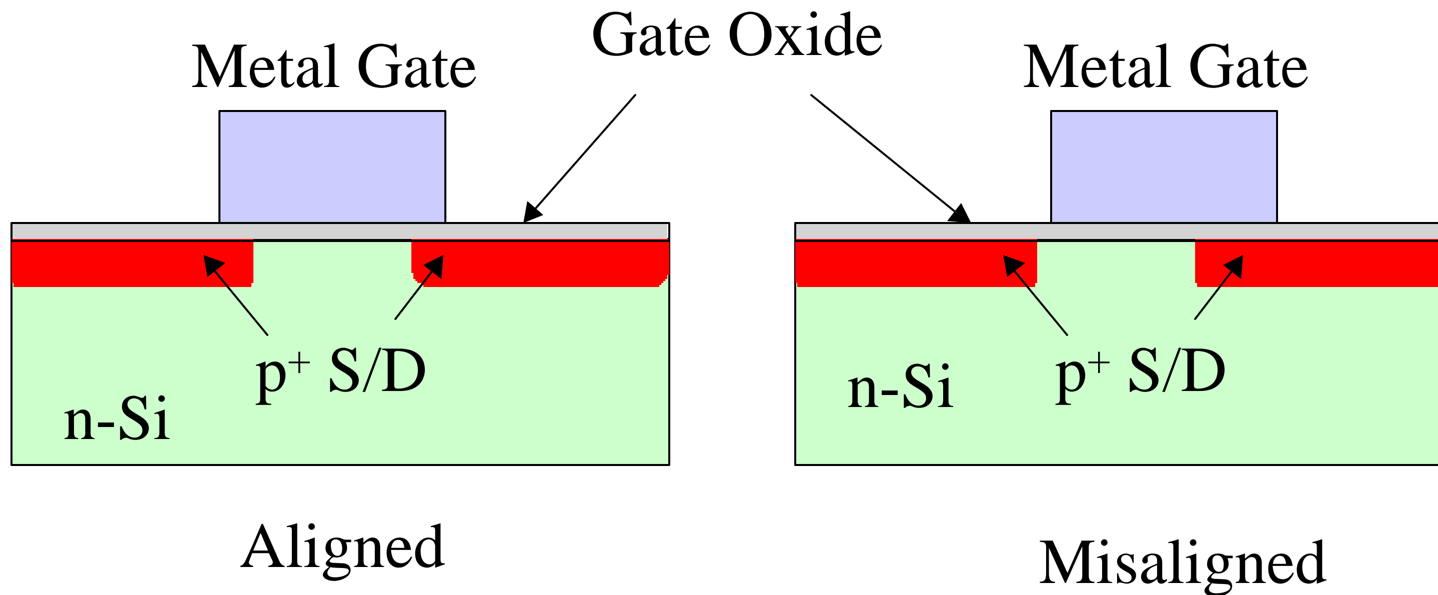
Dope Semiconductor: Ion Implantation

- Used for atomic and nuclear research
- Early idea introduced in 1950's
- Introduced to semiconductor manufacturing in mid-1970s.

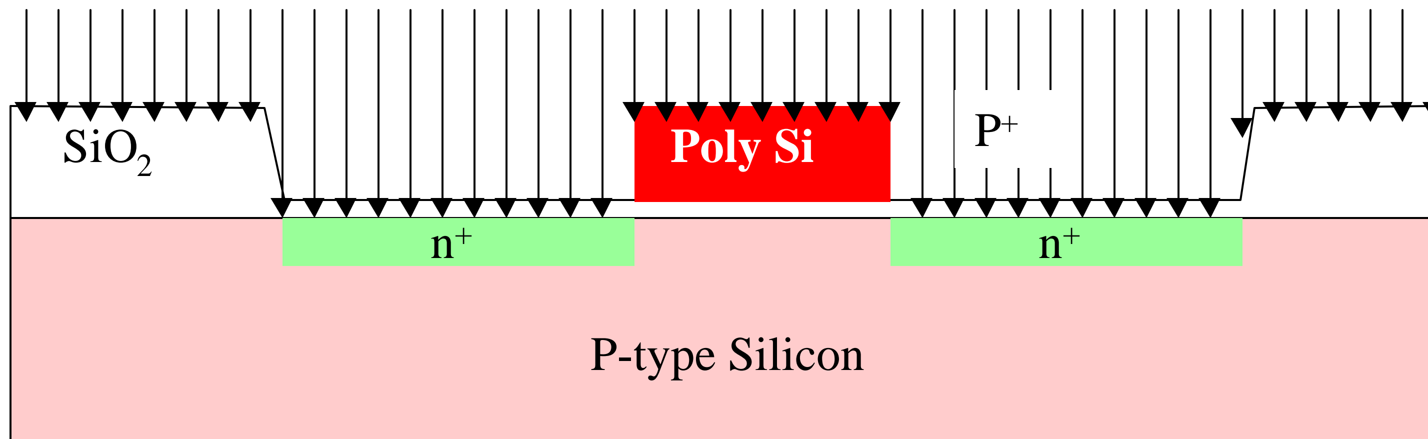
Dope Semiconductor: Ion Implantation

- Independently control dopant profile (ion energy) and dopant concentration (ion current times implantation time)
- Anisotropic dopant profile
- Easy to achieve high concentration dope of heavy dopant atom such as phosphorus and arsenic.

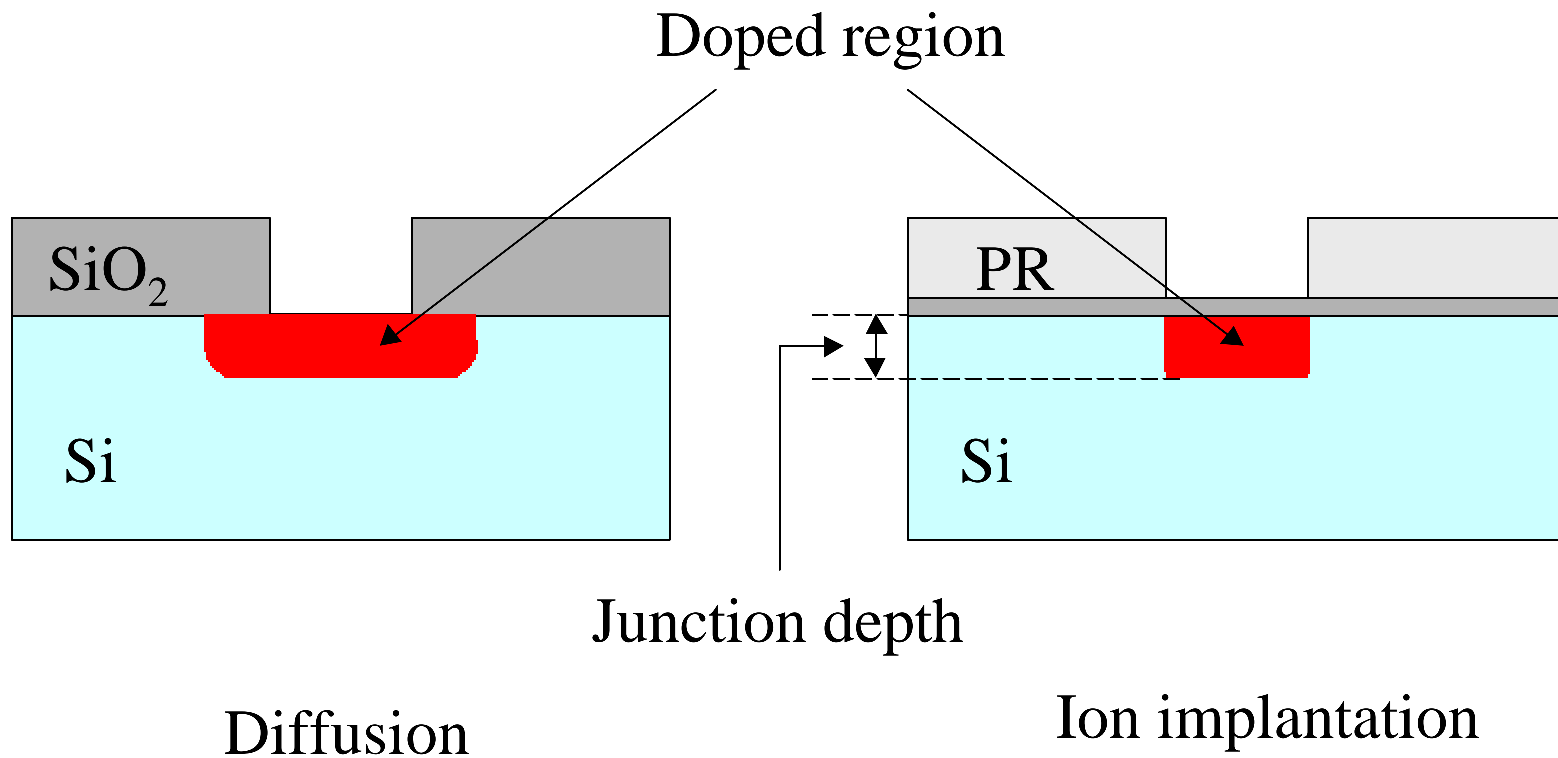
Misalignment of the Gate



Ion Implantation, Phosphorus



Comparison of Implantation and Diffusion



Comparison of Implantation and Diffusion

Diffusion	Ion Implantation
High temperature, hard mask	Low temperature, photoresist mask
Isotropic dopant profile	Anisotropic dopant profile
Cannot independently control of the dopant concentration and junction depth	Can independently control of the dopant concentration and junction depth
Batch process	Both Batch and single wafer process

Ion Implantation Control

- Beam current and implantation time control dopant concentration
- Ion energy controls junction depth
- Dopant profile is anisotropic

Applications of Ion Implantation

Applications	Doping	Pre-amorphous	Buried oxide	Poly barrier
Ions	n-type: P, As, Sb p-type: B	Si or Ge	O	N

Other Applications

- Oxygen implantation for silicon-on-insulator (SOI) device
- Pre-amorphous silicon implantation on titanium film for better annealing
- Pre-amorphous germanium implantation on silicon substrate for profile control
- ……..

Some Fact about Phosphorus

Name	Phosphorus
Symbol	P
Atomic number	15
Atomic weight	30.973762
Discoverer	Hennig Brand
Discovered at	Germany
Discovery date	1669
Origin of name	From the Greek word "phosphoros" meaning "bringer of light" (an ancient name for the planet Venus)
Density of solid	1.823 g/cm^3
Molar volume	17.02 cm^3
Velocity of sound	N/A
Electrical resistivity Refractivity	10 $\mu\Omega$ cm 1.001212
Reflectivity	N/A
Melting point	44.3 C
Boiling point	277 C
Thermal conductivity	0.236 W m^{-1} K^{-1}
Coefficient of linear thermal expansion	N/A
Applications	N-type dopant in diffusion, ion implantation, epitaxial grow and polysilicon deposition. Dopant of CVD silicate glass (PSG and BPSG).
Main sources	P (red), PH_3, $POCl_3$

Some Fact about Arsenic

Name	Arsenic
Symbol	As
Atomic number	33
Atomic weight	74.9216
Discoverer	Known since ancient times
Discovered at	not known
Discovery date	not known
Origin of name	From the Greek word "arsenikon" meaning "yellow orpiment"
Density of solid Molar volume	5.727 g/cm^3 12.95 cm^3
Velocity of sound	N/A
Electrical resistivity	30.03 $\mu\Omega$ cm
Refractivity	1.001552
Reflectivity	N/A
Melting point	614 C
Boiling point	817 C
Thermal conductivity	50.2 W m^{-1} K^{-1}
Coefficient of linear thermal expansion	N/A
Applications	N-type dopant in diffusion, ion implantation, epitaxial grow and polysilicon deposition.
Main sources	As, AsH_3

Some Fact about Boron

Name	Boron
Symbol	B
Atomic number	5
Atomic weight	10.811
Discoverer	Sir Humphrey Davy, Joseph-Louis Gay-Lussac,
Discovered at	England, France
Discovery date	1808
Origin of name	From the Arabic word "buraq" and the Persian word "burah"
Density of solid	2.460 g/cm^3
Molar volume	4.39 cm^3
Velocity of sound	16200 m/sec
Electrical resistivity	$> 10^{12}$ μΩ cm
Refractivity	N/A
Reflectivity	N/A
Melting point	2076 C
Boiling point	3927 C
Thermal conductivity	27 W m^{-1} K^{-1}
Coefficient of linear thermal expansion	6 10^{-6} K^{-1}
Applications	P-type dopant in diffusion, ion implantation, epitaxial grow and polysilicon deposition. Dopant of CVD silicate glass (BPSG)
Main sources	B, B_2H_6, BF_3

Stopping Mechanism

- Ions penetrate into substrate
- Collide with lattice atoms
- Gradually lose their energy and stop
- Two stop mechanisms

Two Stopping Mechanism

- Nuclear stopping
  - Collision with nuclei of the lattice atoms
  - Scattered significantly
  - Causes crystal structure damage.
- electronic stopping
  - Collision with electrons of the lattice atoms
  - Incident ion path is almost unchanged
  - Energy transfer is very small
  - Crystal structure damage is negligible

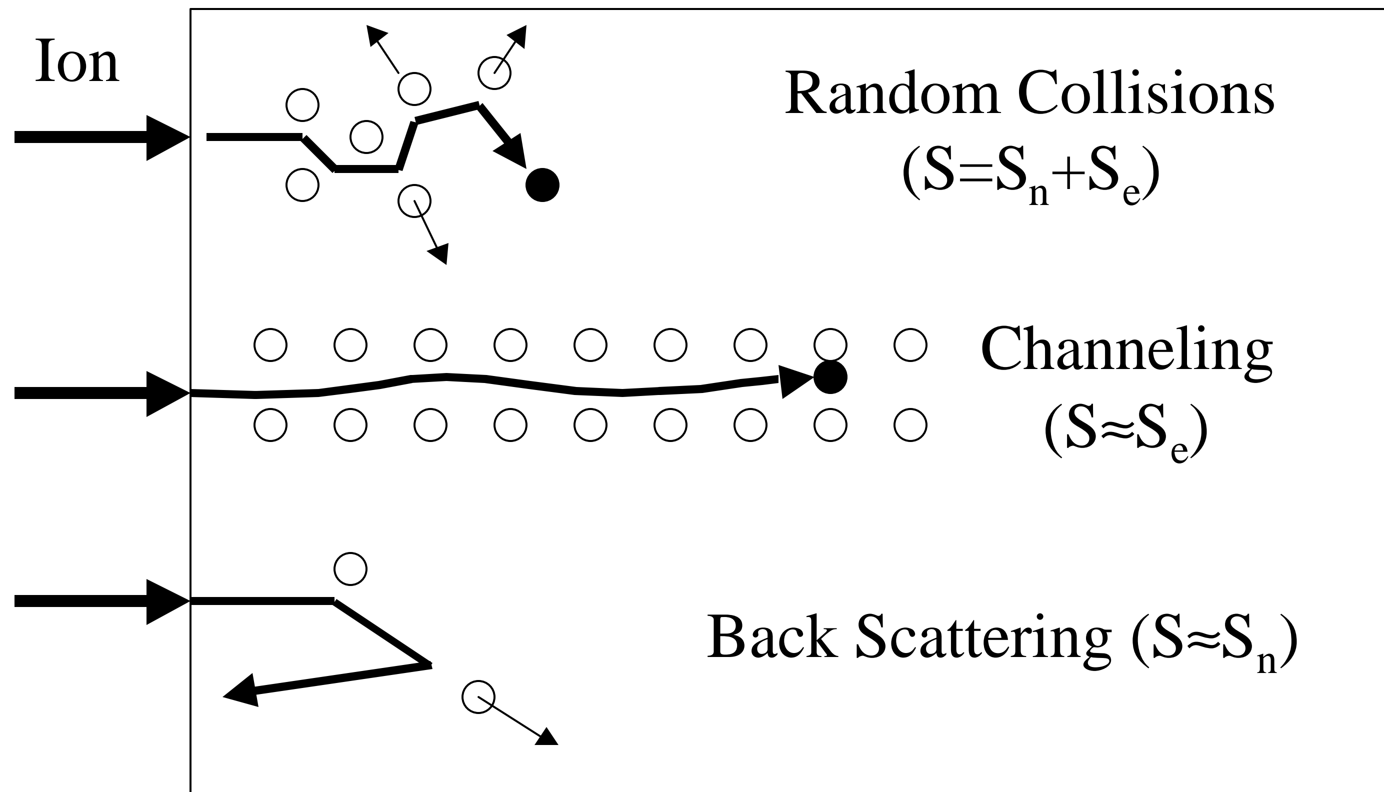
Stopping Mechanism

- The total stopping power

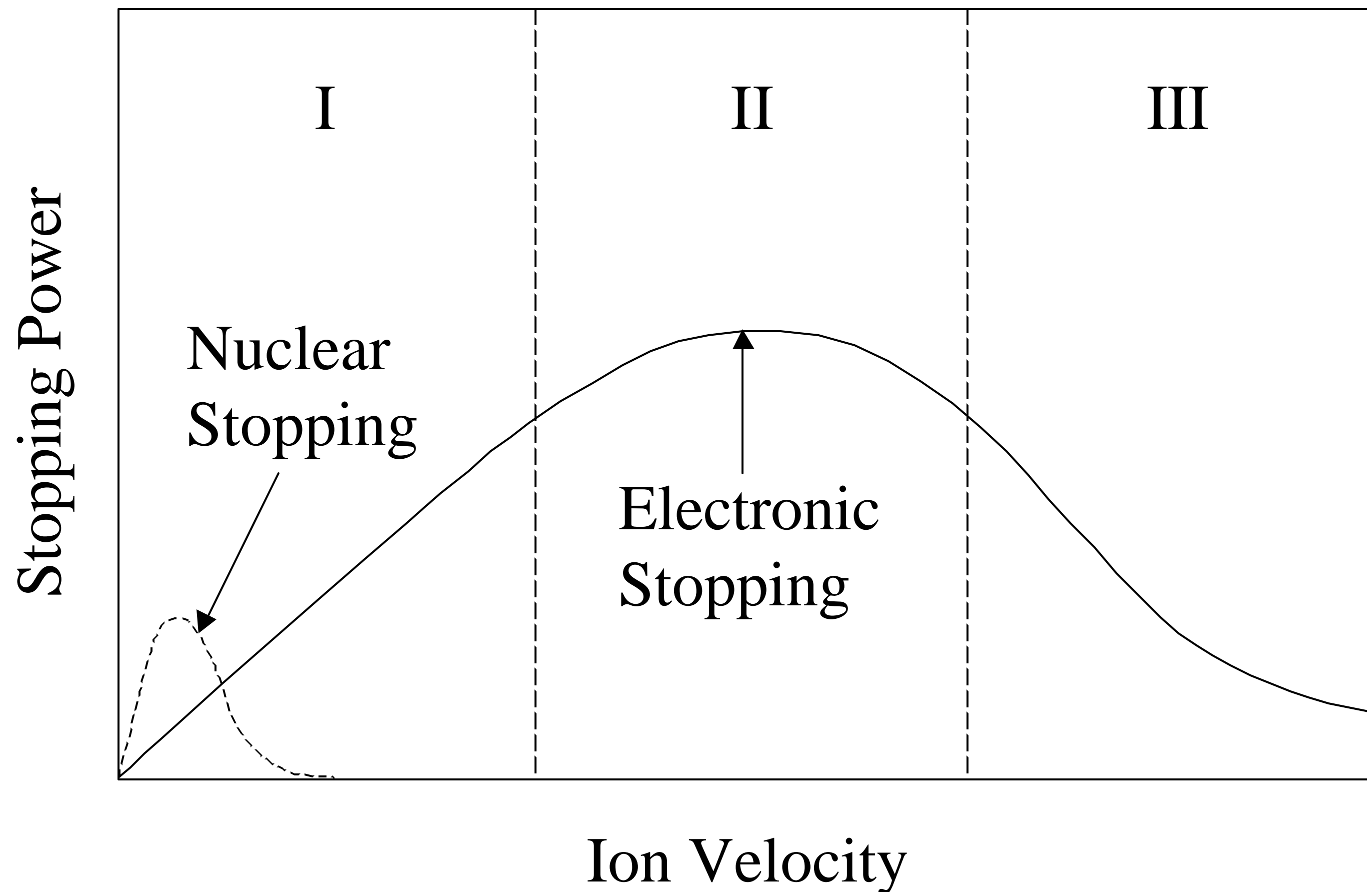
$$S_{total} = S_n + S_e$$

- S_n: nuclear stopping, S_e: electronic stopping
- Low E, high A ion implantation: mainly nuclear stopping
- High E, low A ion implantation, electronic stopping mechanism is more important

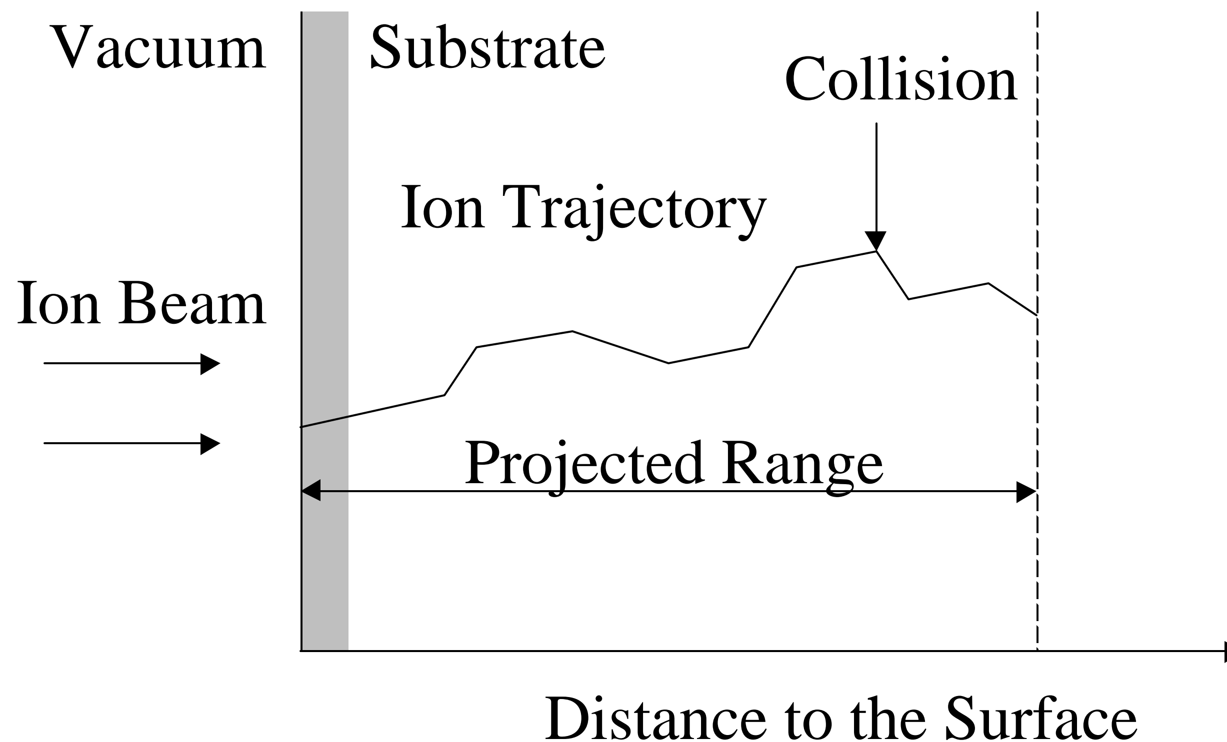
Stopping Mechanisms



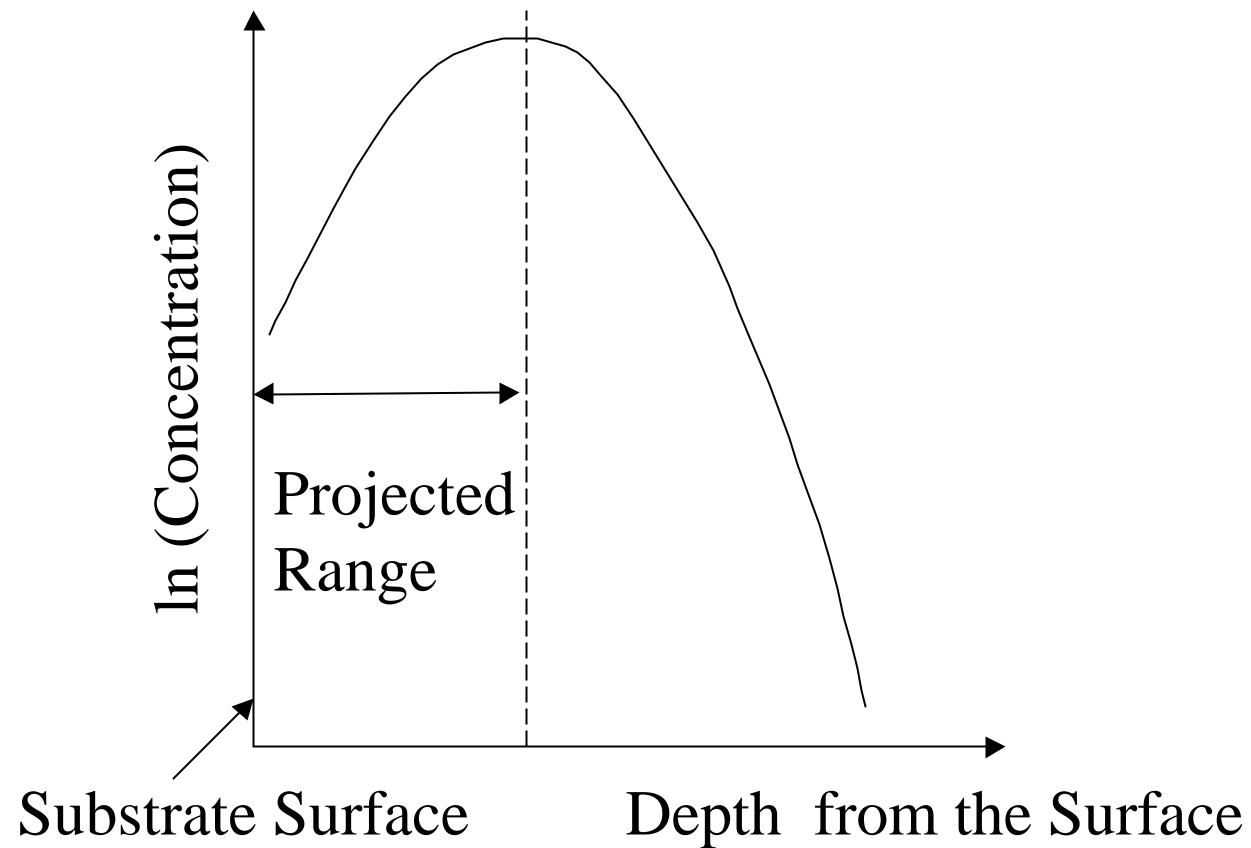
Stopping Power and Ion Velocity



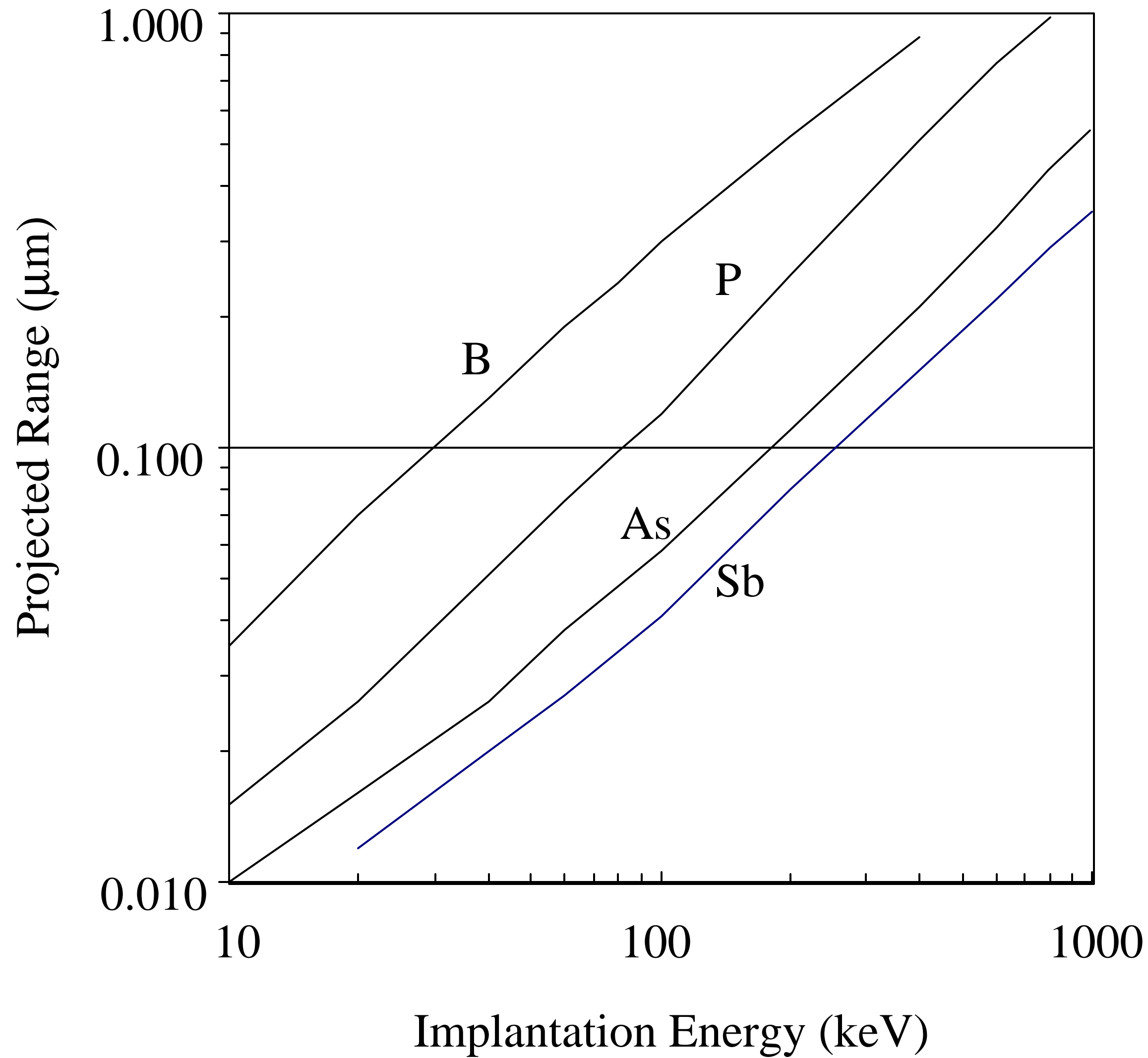
Ion Trajectory and Projected Range



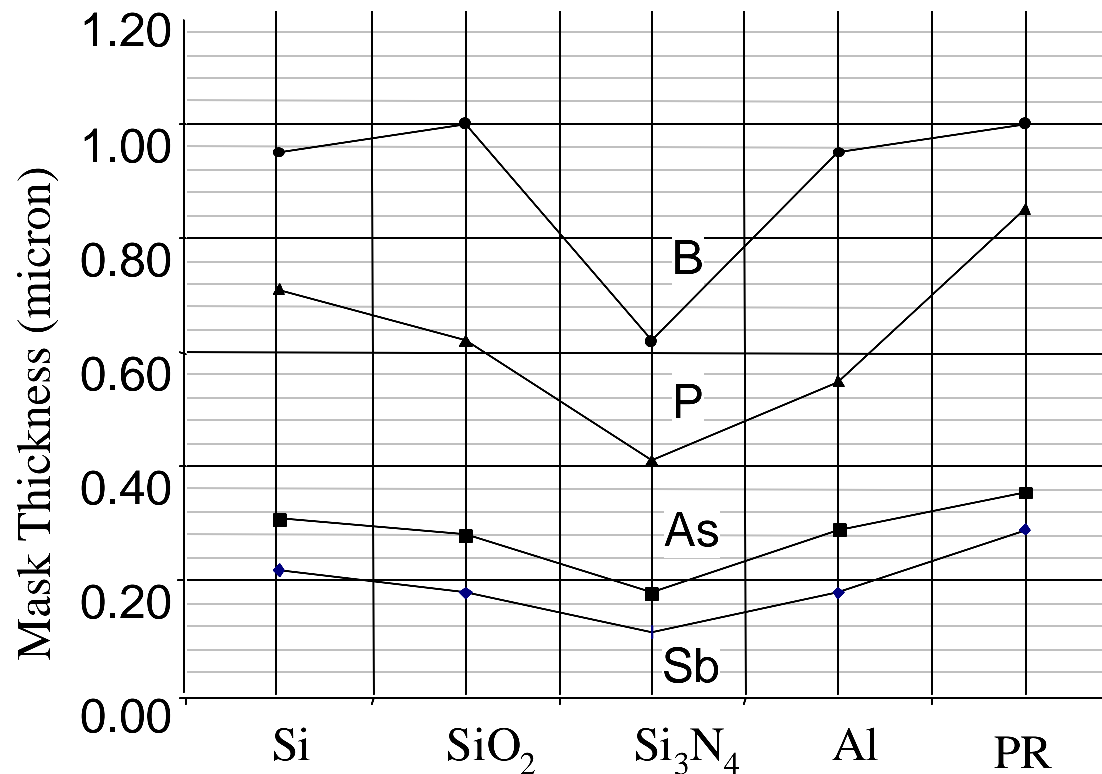
Ion Projection Range



Projected Range in Silicon

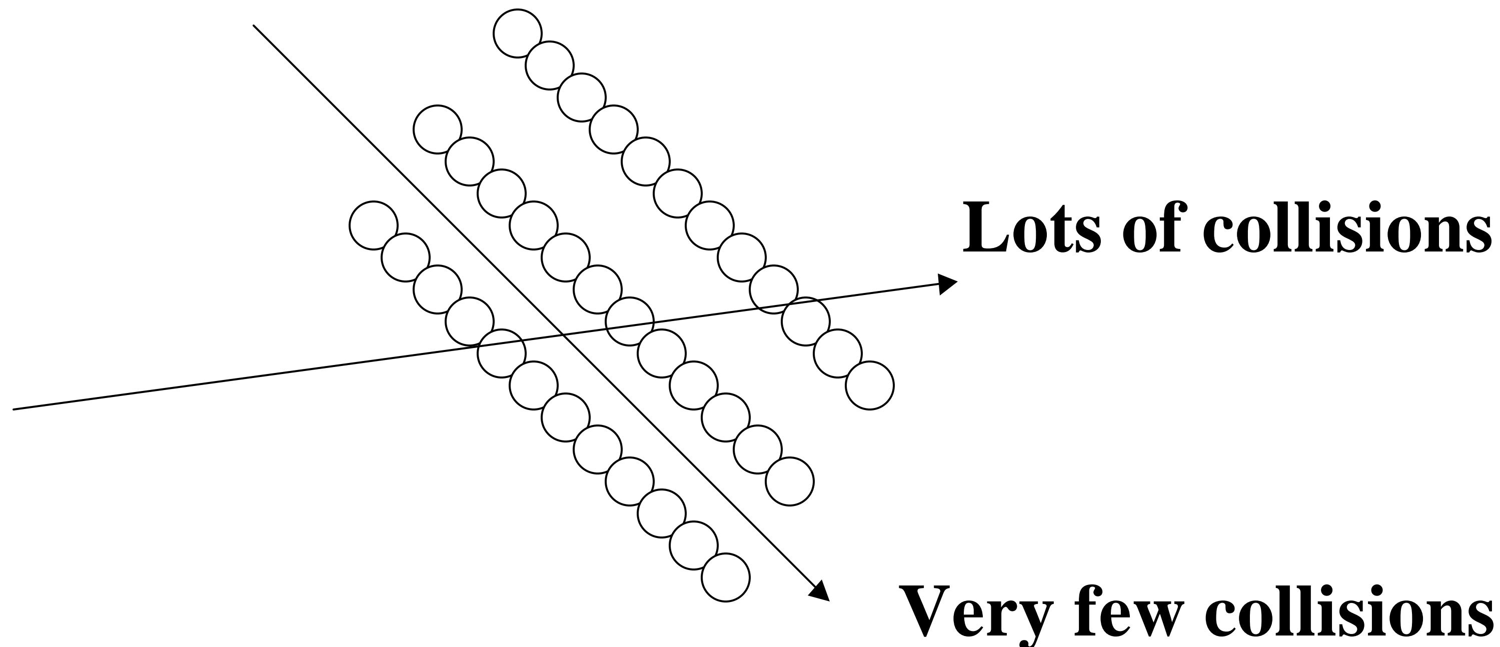


Barrier Thickness to Block 200 keV Ion Beam

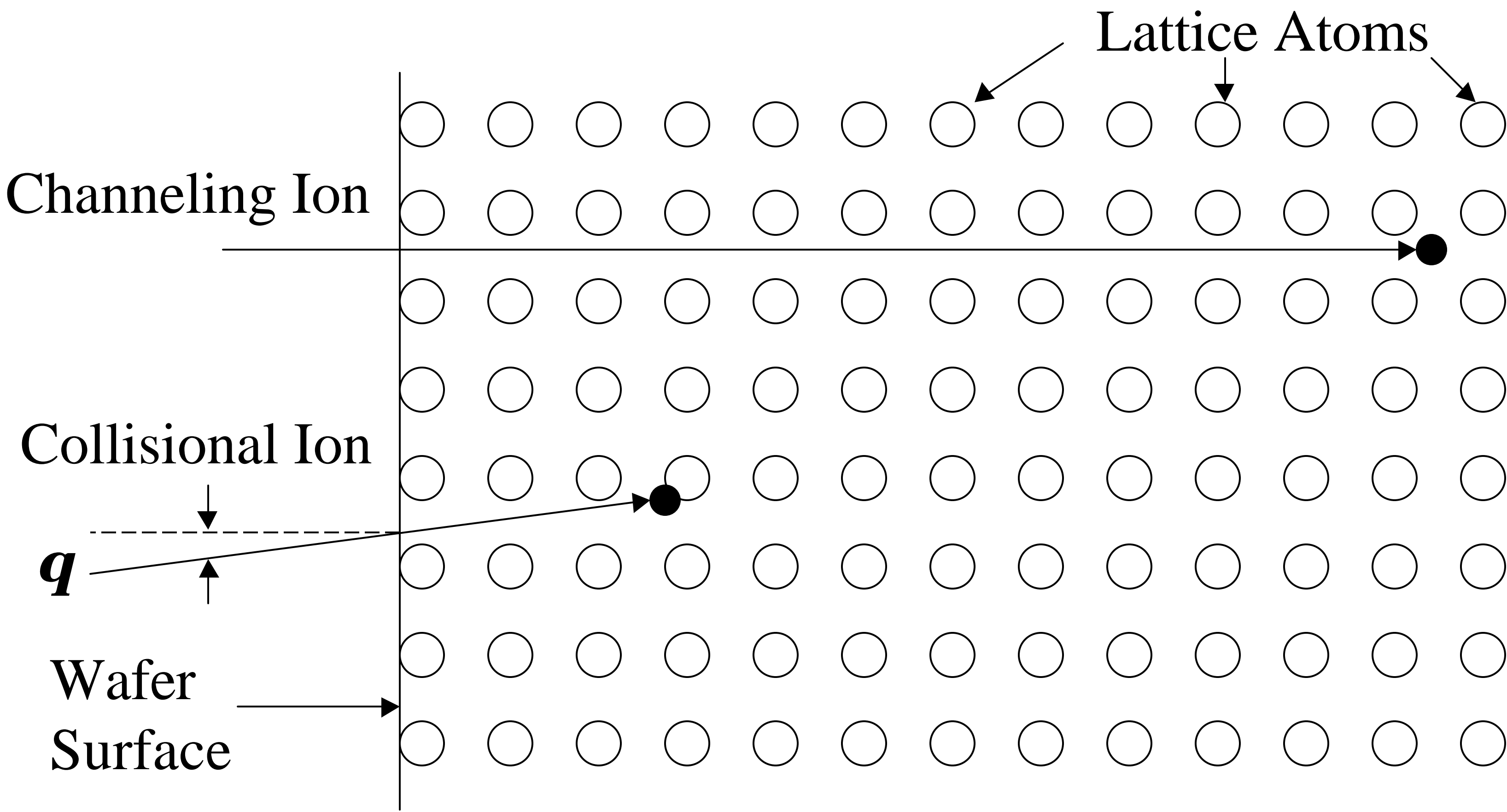


Implantation Processes: Channeling

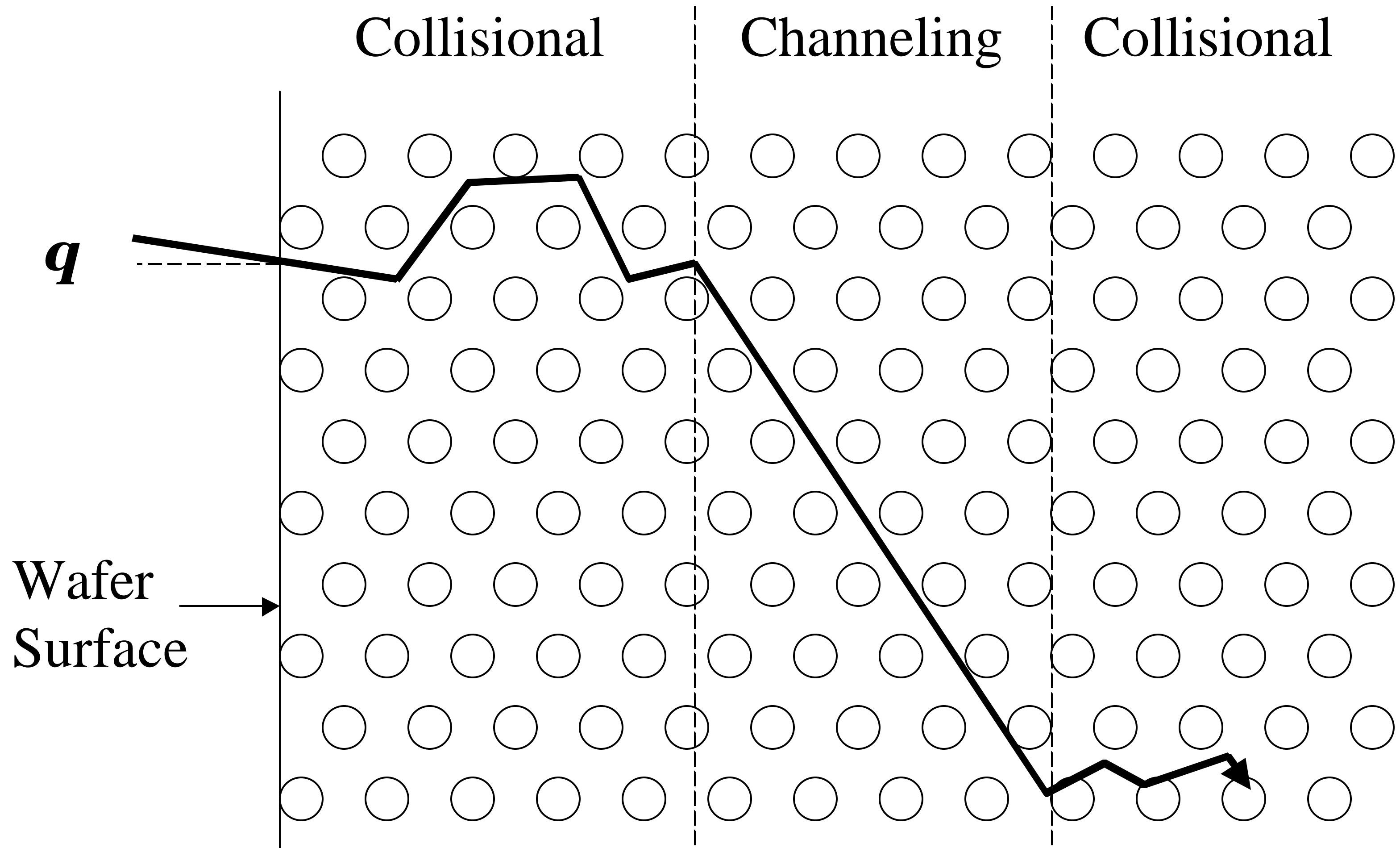
- If the incident angle is right, ion can travel long distance without collision with lattice atoms
- It causes uncontrollable dopant profile



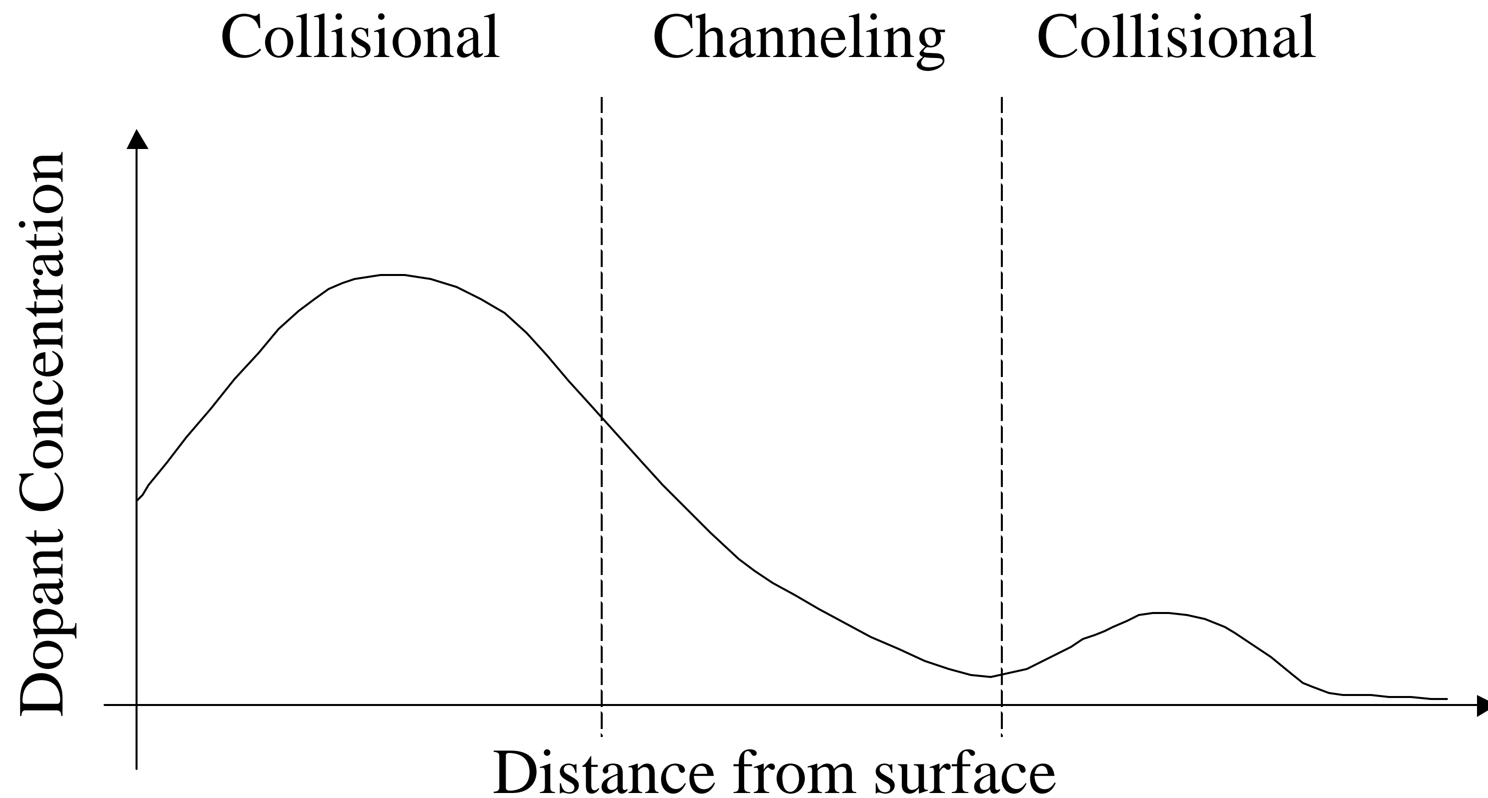
Channeling Effect



Post-collision Channeling



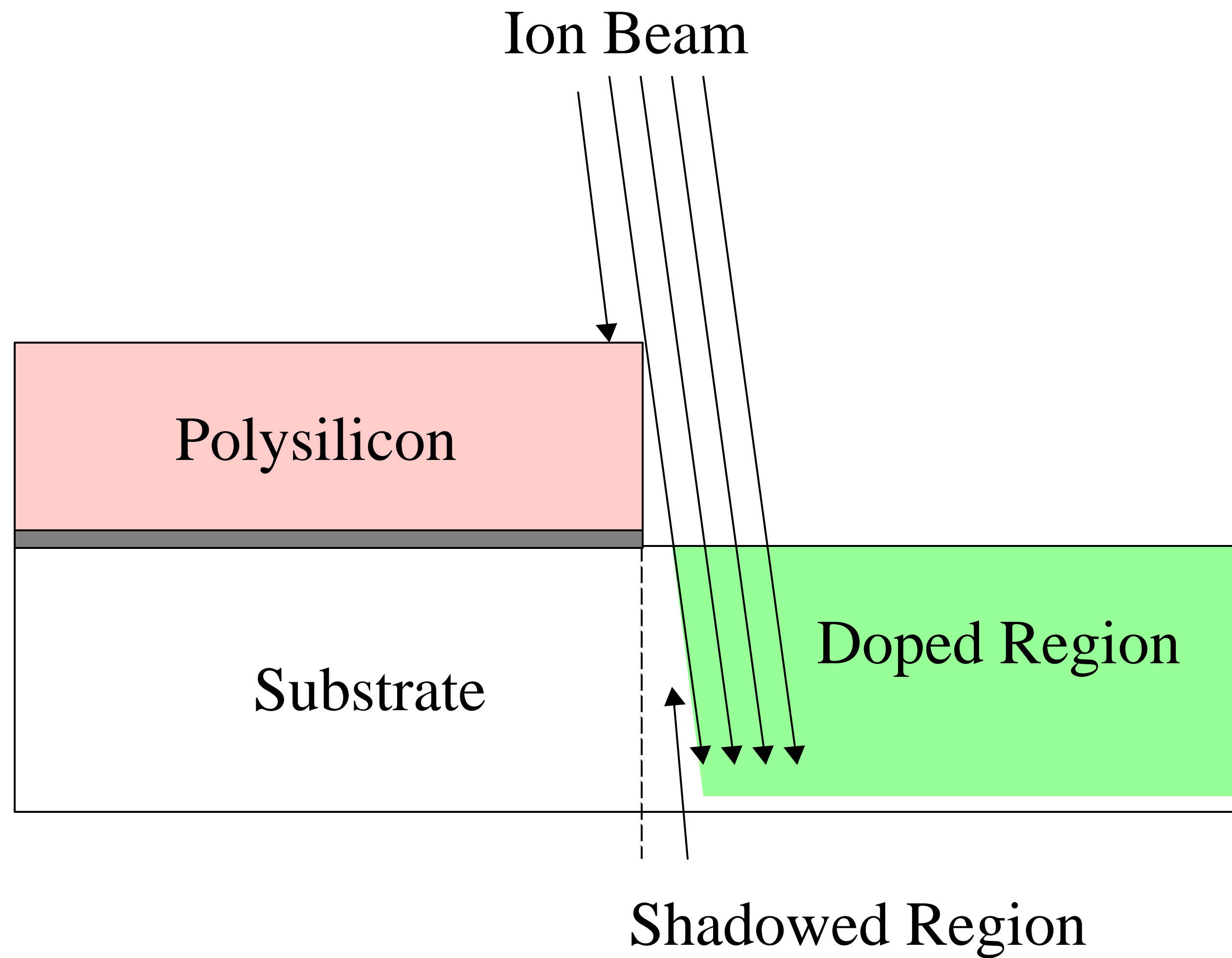
Post-collision Channeling



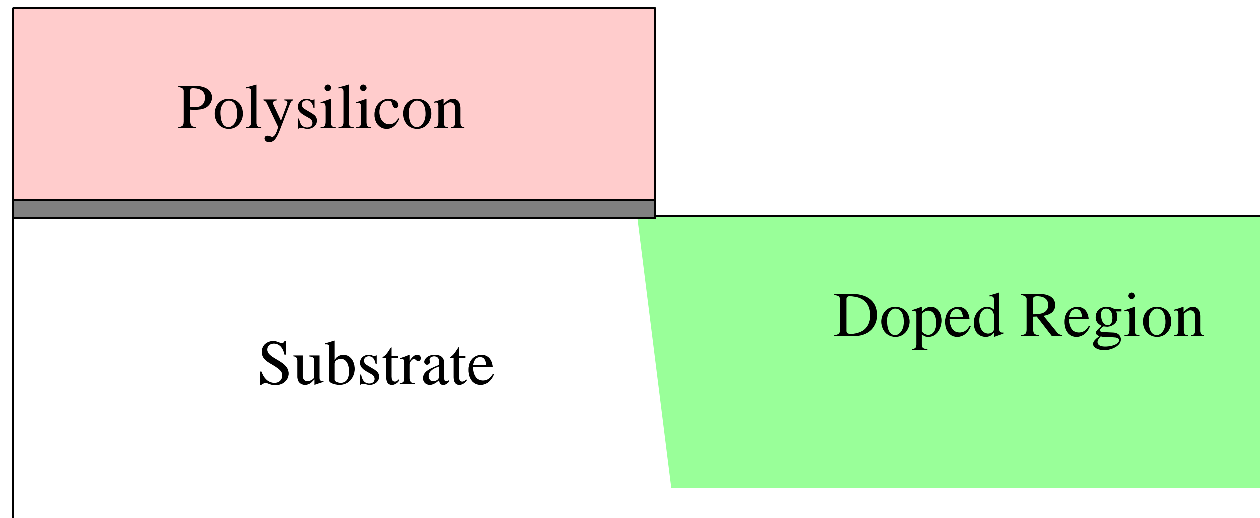
Implantation Processes: Channeling

- Ways to avoid channeling effect
  - Tilt wafer, 7° is most commonly used
  - Screen oxide
  - Pre-amorphous implantation, Germanium
- Shadowing effect
  - Ion blocked by structures
- Rotate wafer and post-implantation diffusion

Shadowing Effect



Shadowing Effect



Q & A

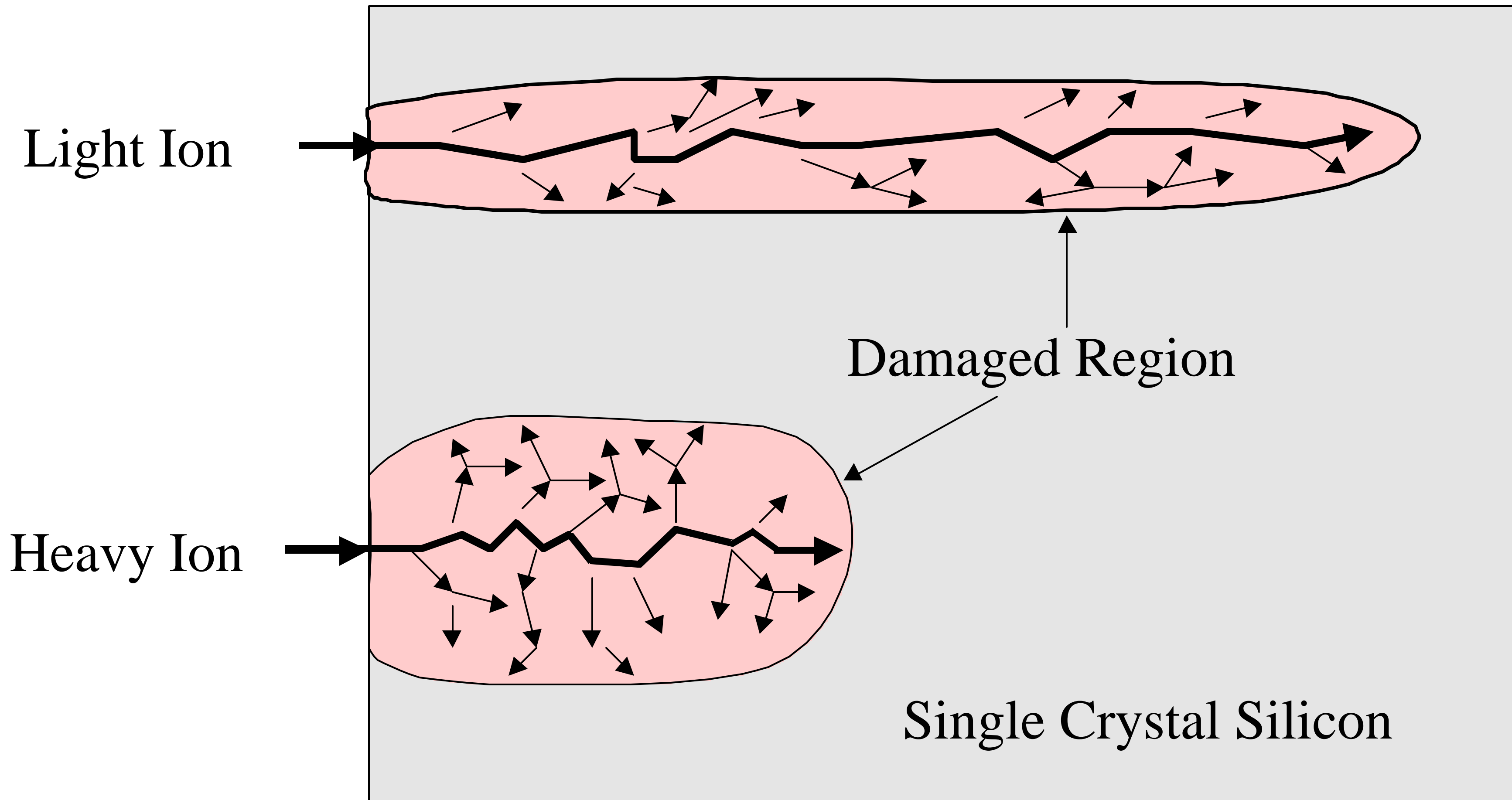
- Why don't people use channeling effect to create deep junction without high ion energy?

- Ion beam is not perfectly parallel. Many ions will start to have a lot of nuclear collisions with lattice atoms after they penetrating into the substrate. Some ions can channel deep into the substrate, while many others are stopped as the normal Gaussian distribution.

Damage Process

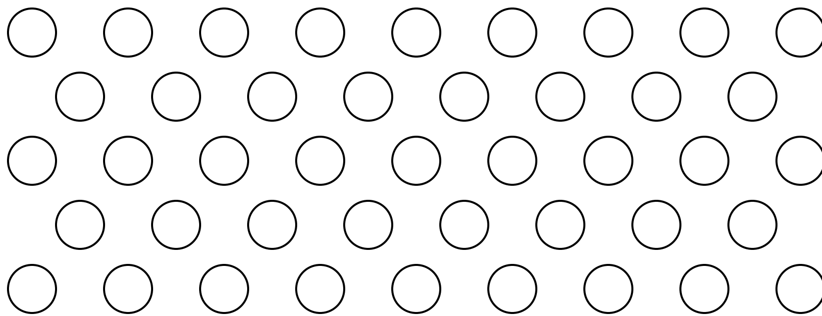
- Implanted ions transfer energy to lattice atoms
  - Atoms to break free
- Freed atoms collide with other lattice atoms
  - Free more lattice atoms
  - Damage continues until all freed atoms stop
- One energetic ion can cause thousands of displacements of lattice atoms

Lattice Damage With One Ion

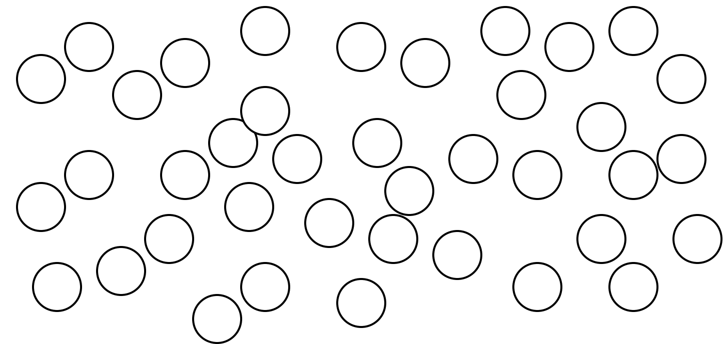


Implantation Processes: Damage

- Ion collides with lattice atoms and knock them out of lattice grid
- Implant area on substrate becomes amorphous structure



Before Implantation

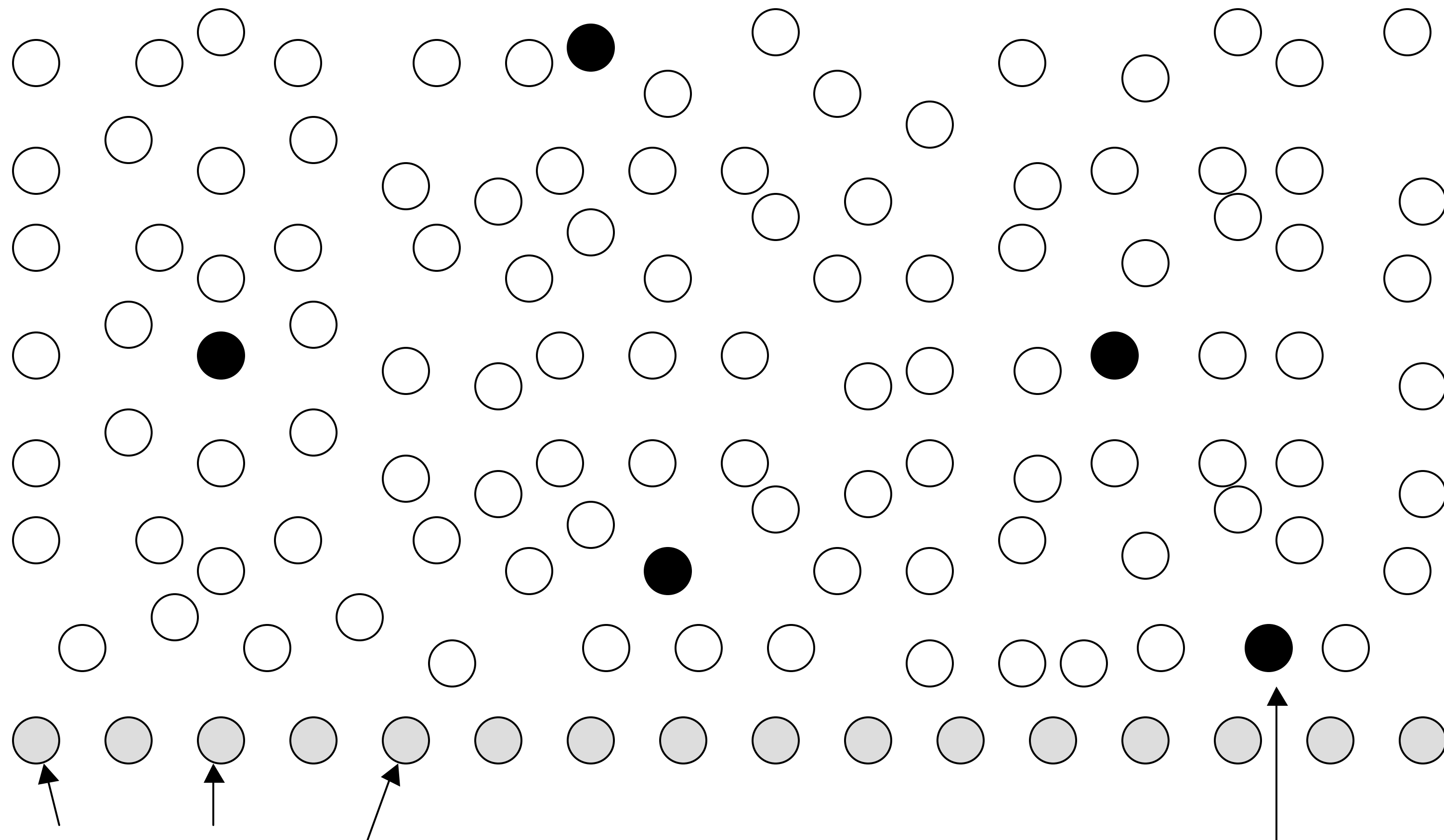


After Implantation

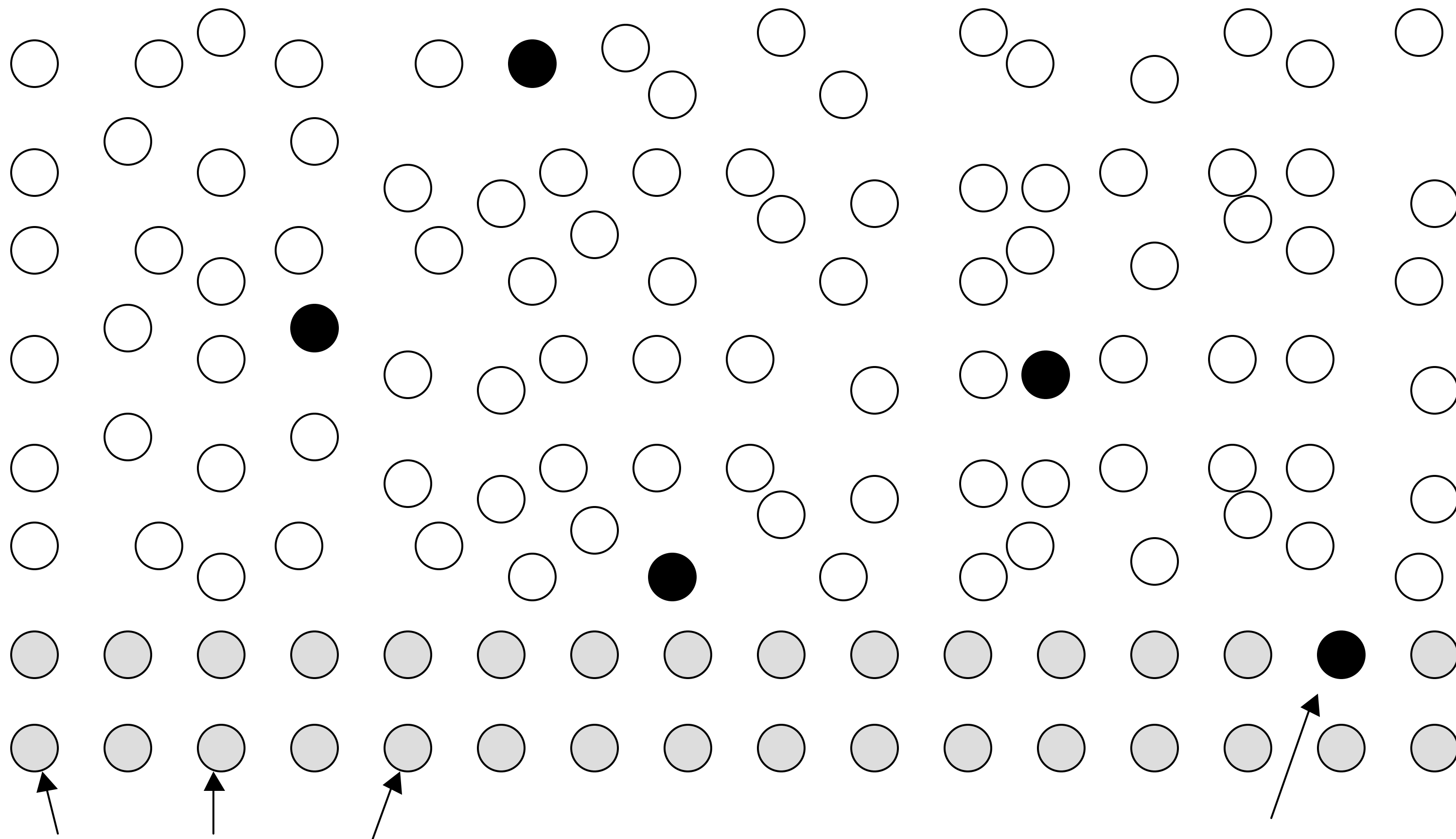
Implantation Processes: Anneal

- Dopant atom must in single crystal structure and bond with four silicon atoms to be activated as donor (N-type) or acceptor (P-type)
- Thermal energy from high temperature helps amorphous atoms to recover single crystal structure.

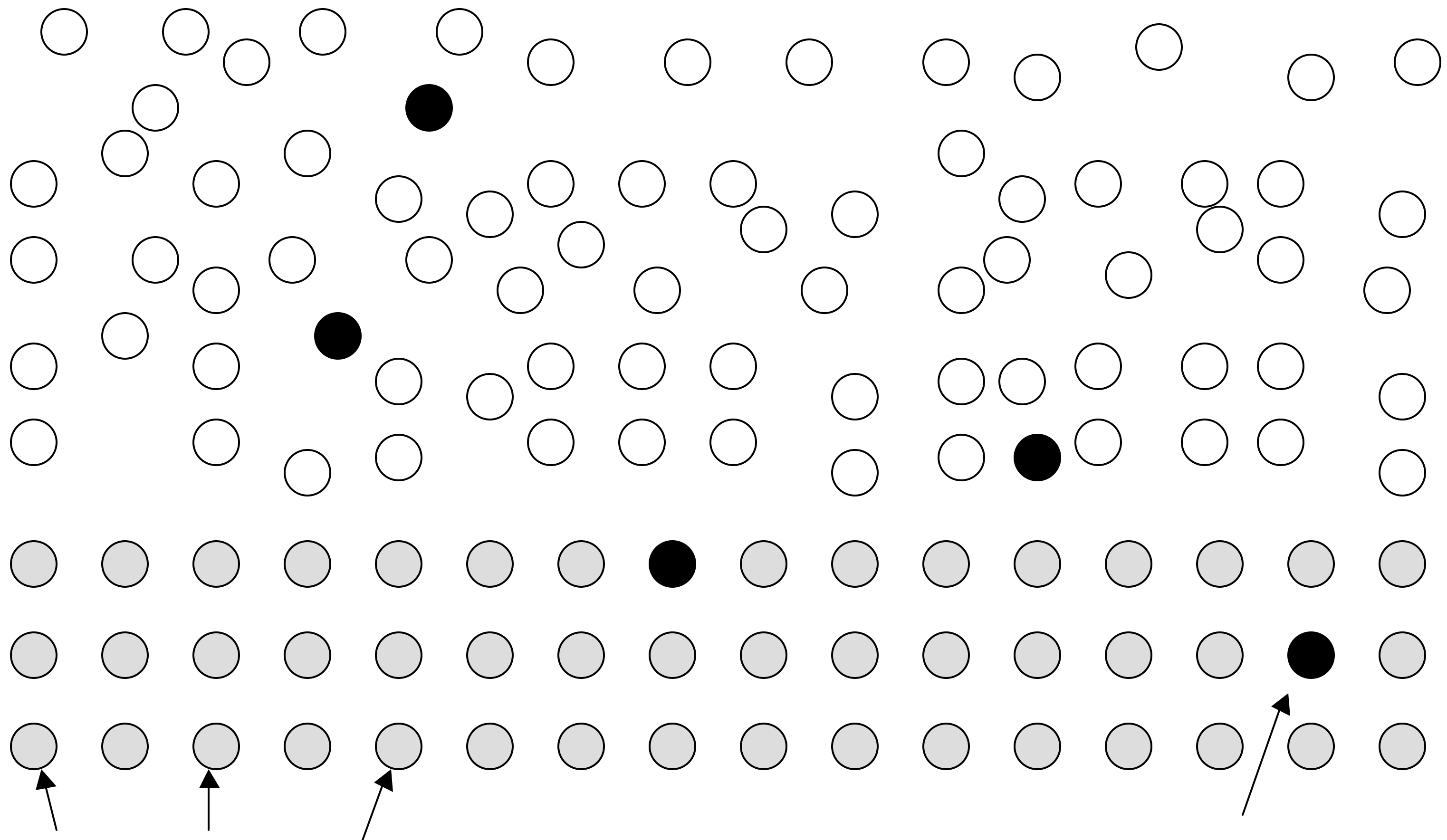
Thermal Annealing



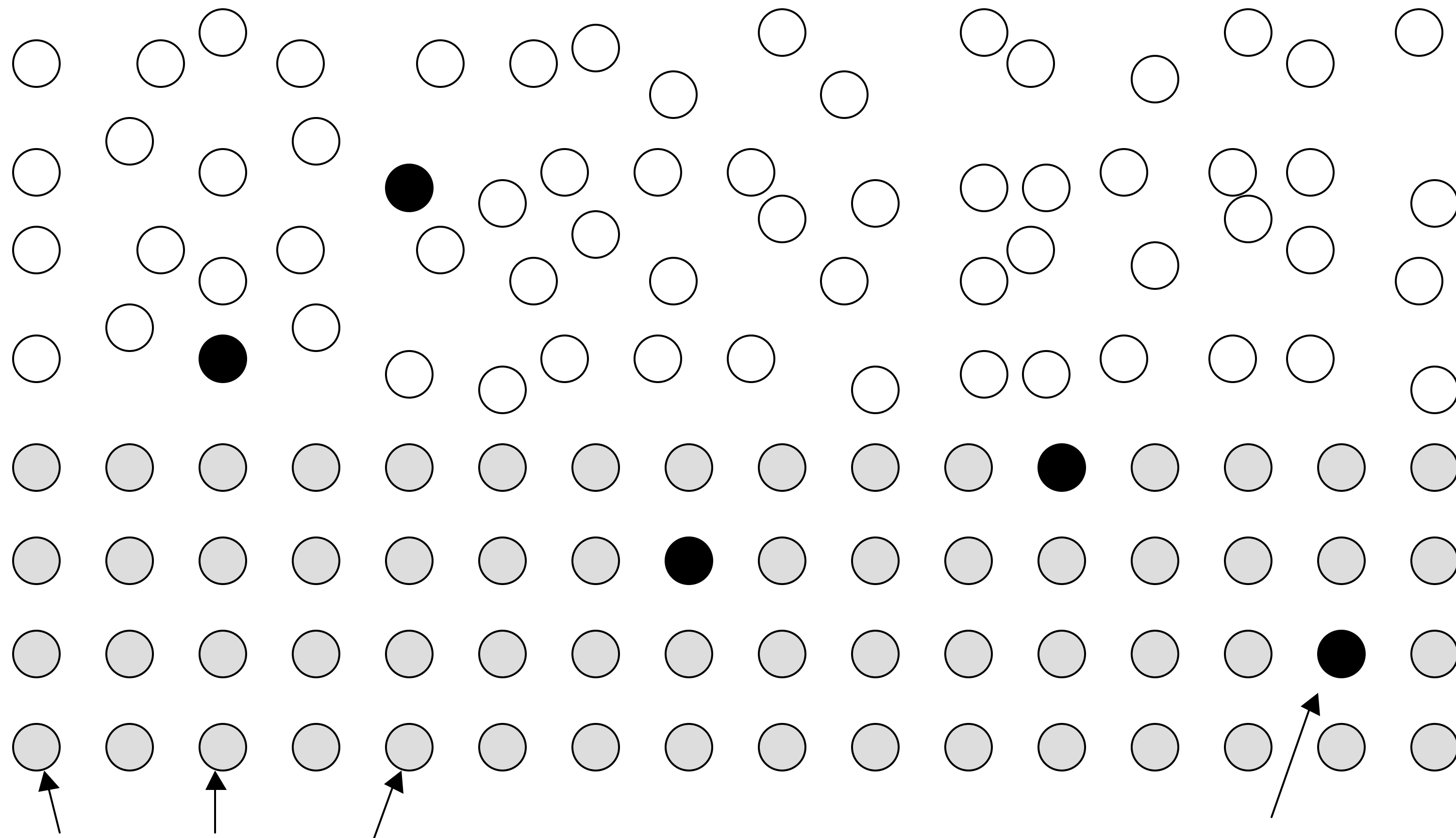
Thermal Annealing



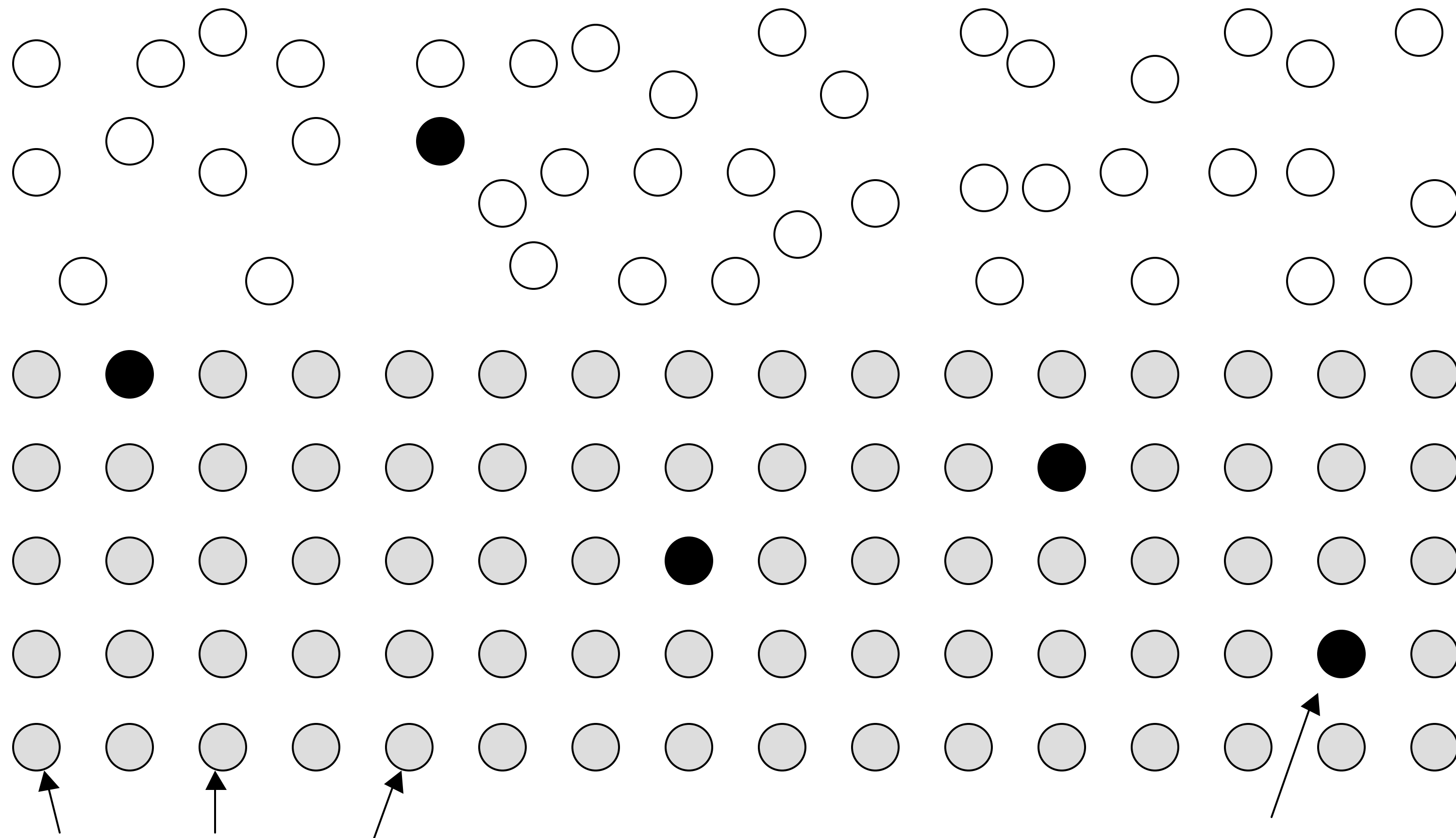
Thermal Annealing



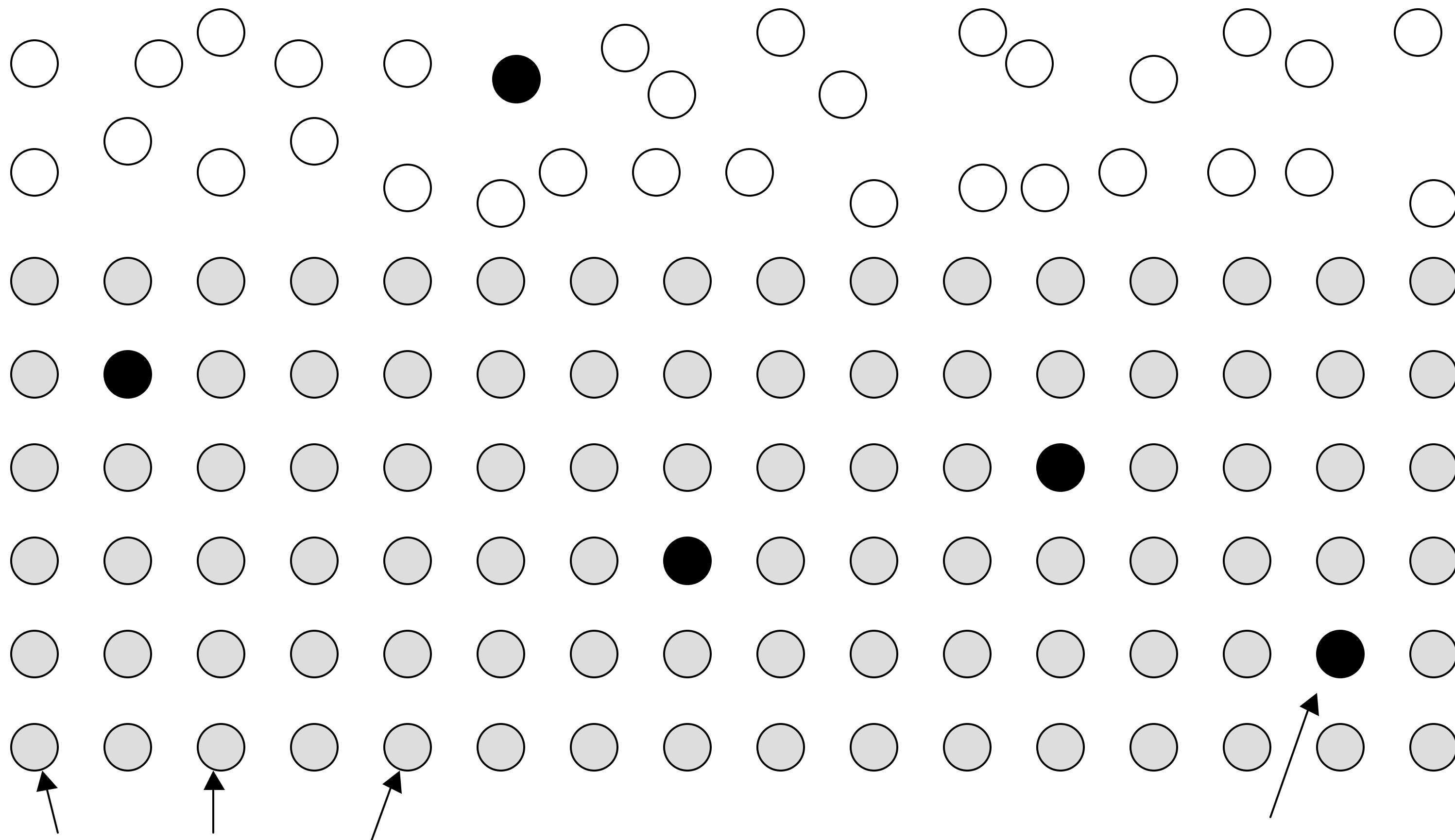
Thermal Annealing



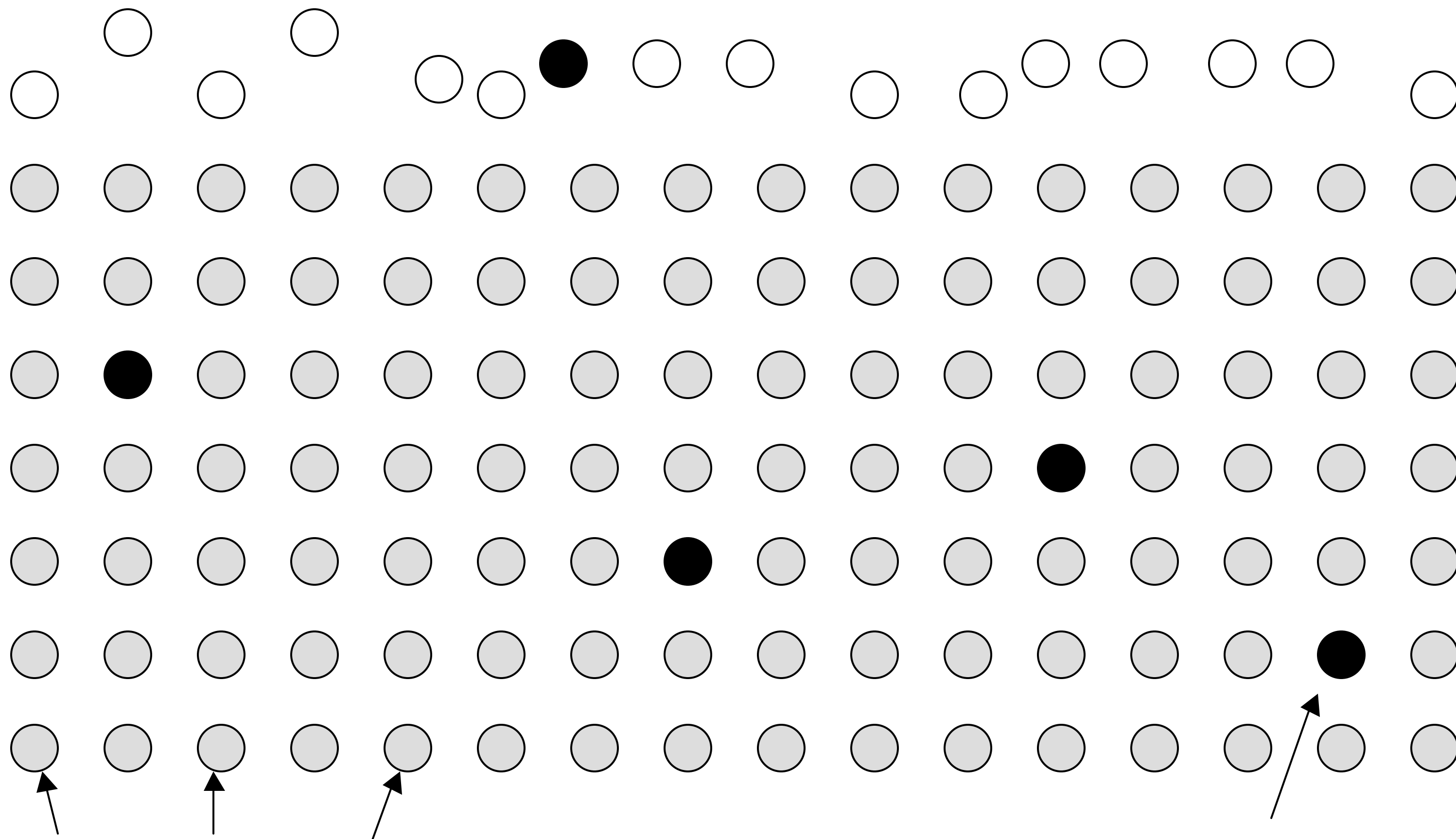
Thermal Annealing



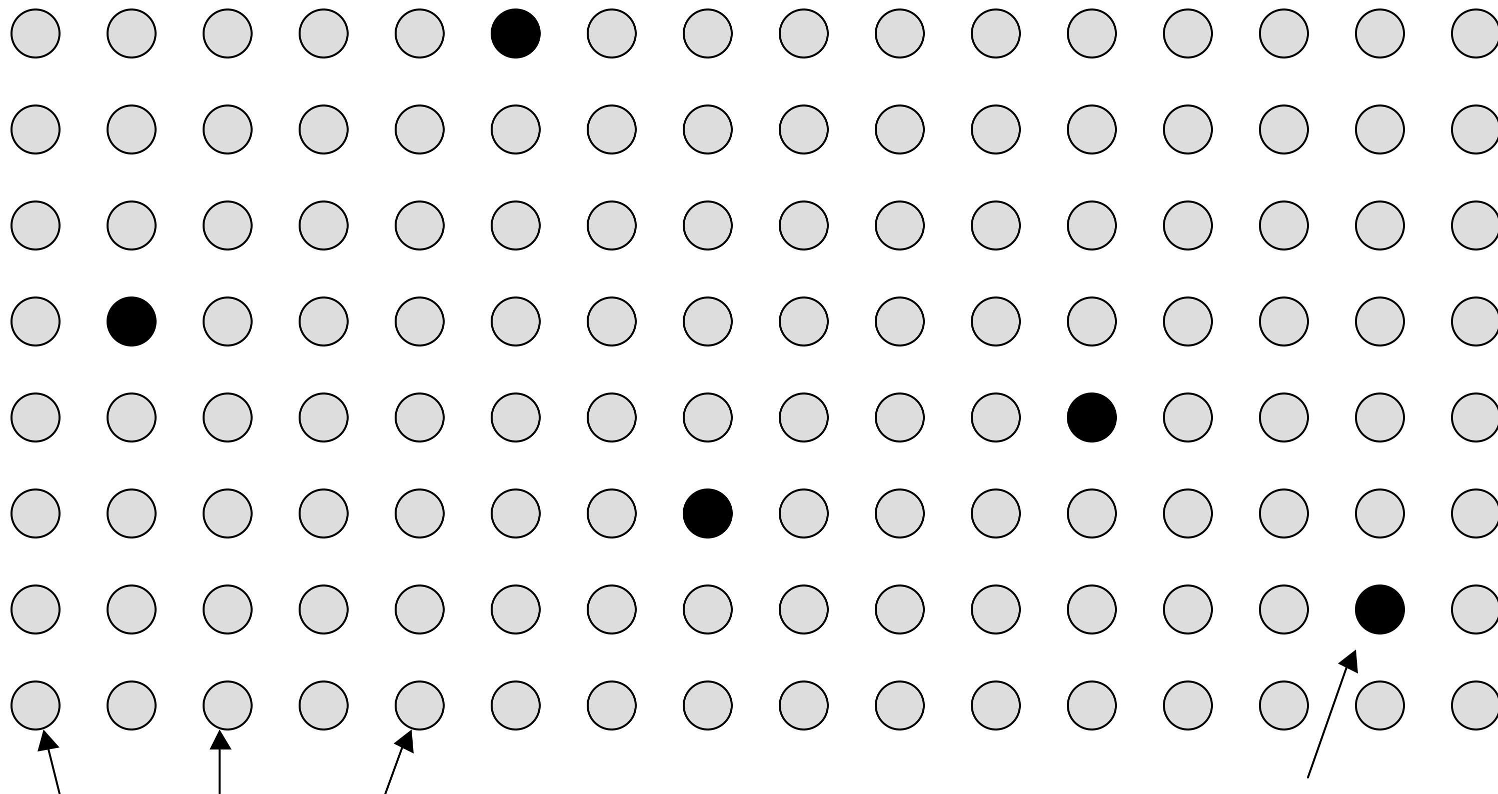
Thermal Annealing



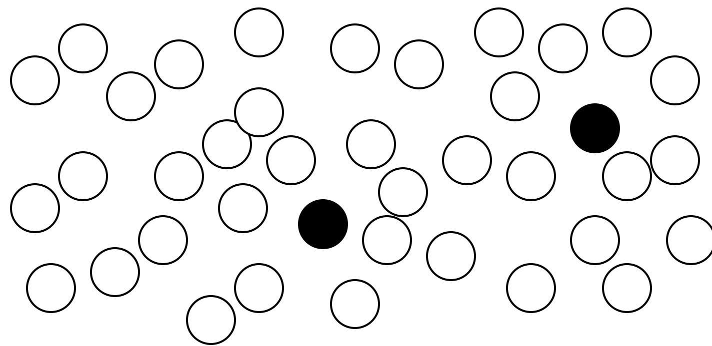
Thermal Annealing



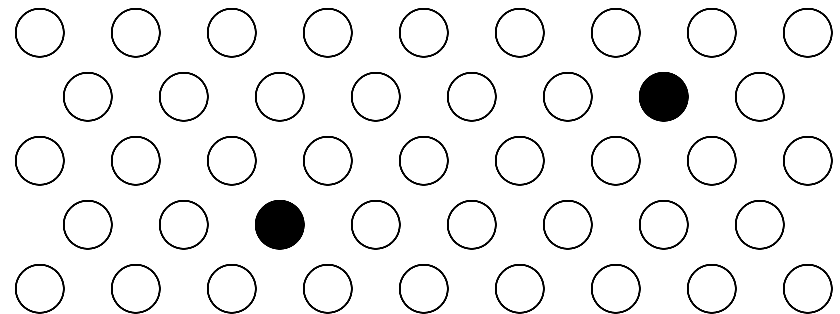
Thermal Annealing



Implantation Processes: Annealing



Before Annealing

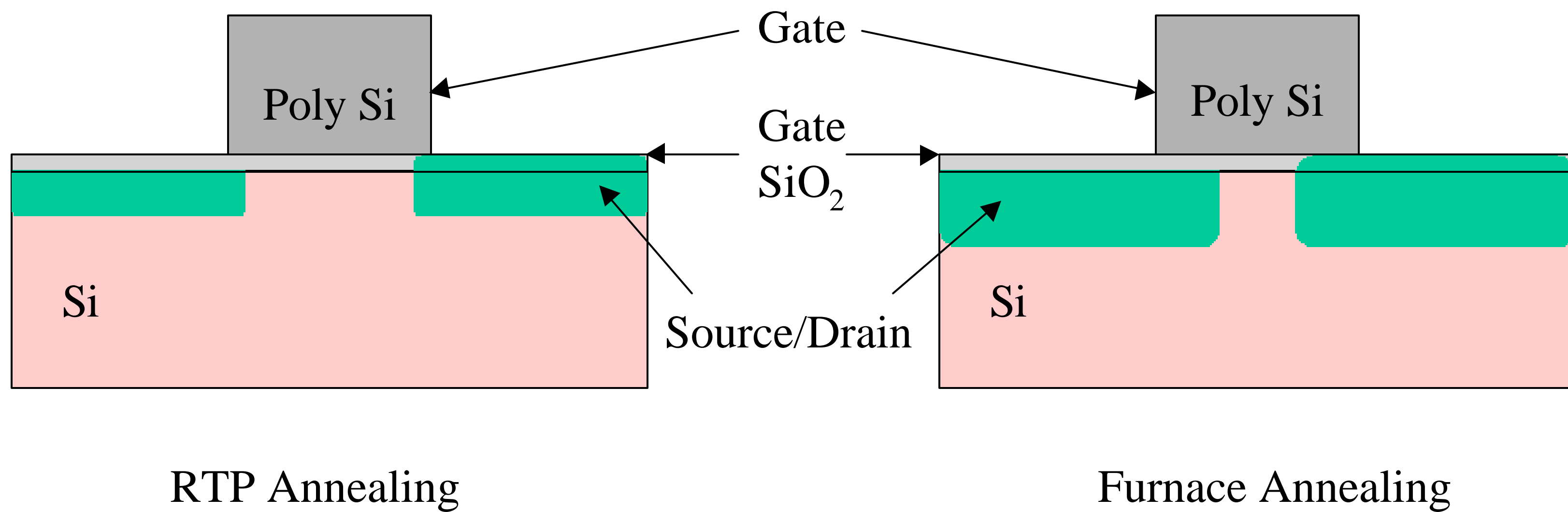


After Annealing

Rapid Thermal Annealing (RTA)

- At high temperature, annealing out pace diffusion
- Rapid thermal process (RTP) is widely used for post-implantation anneal
- RTA is fast (less than a minute), better WTW uniformity, better thermal budget control, and minimized the dopant diffusion

RTP and Furnace Annealing



Question and Answer

- Why can't the furnace temperature be ramped-up and cooled-down as quickly as RTP system ?

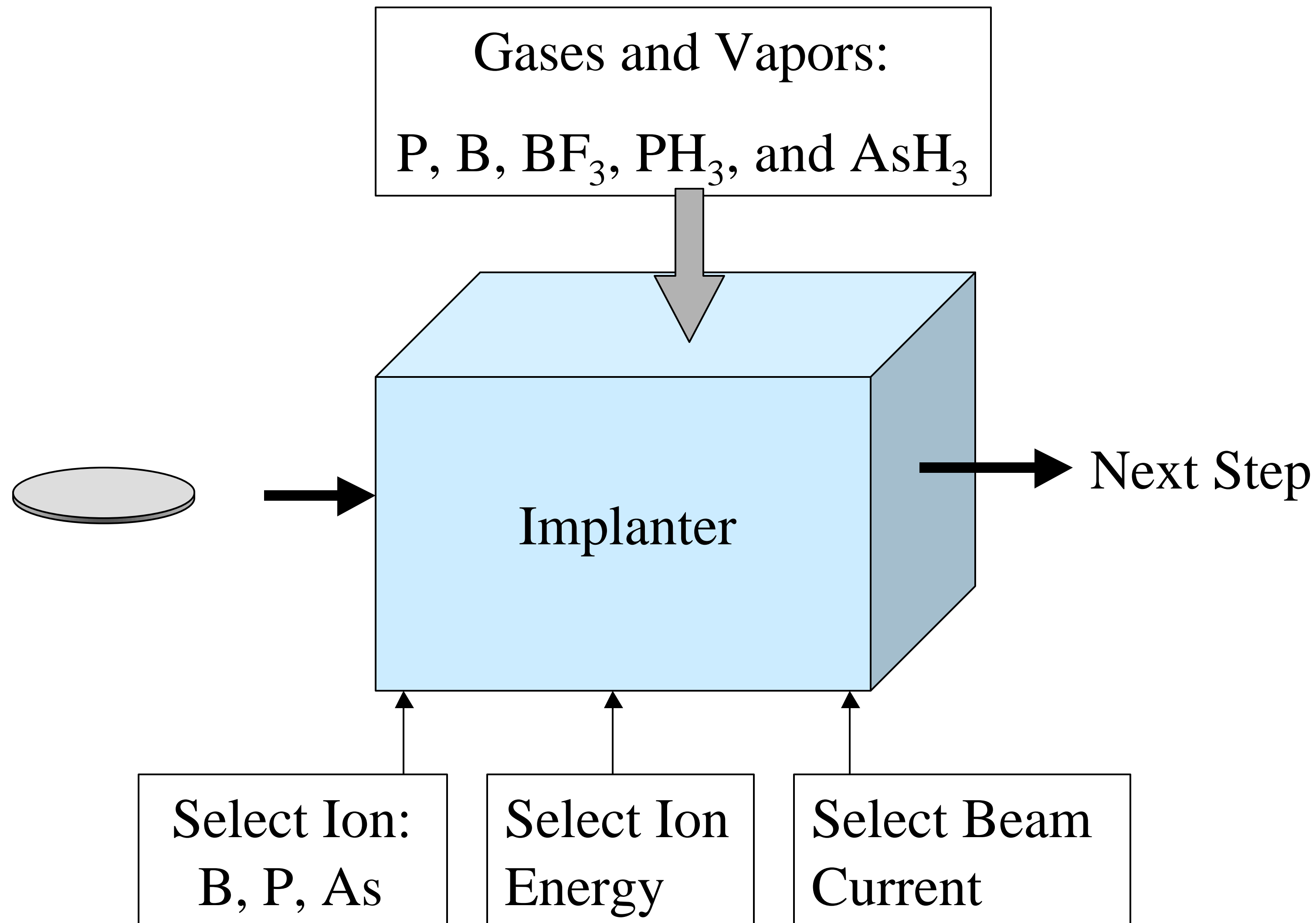
- A furnace has very large thermal capacity, it needs very high heating power to ramp-up temperature rapidly. It is very difficult to ramp up temperature very fast without large temperature oscillation due to the temperature overshoot and undershoot .

Ion Implantation: Hardware

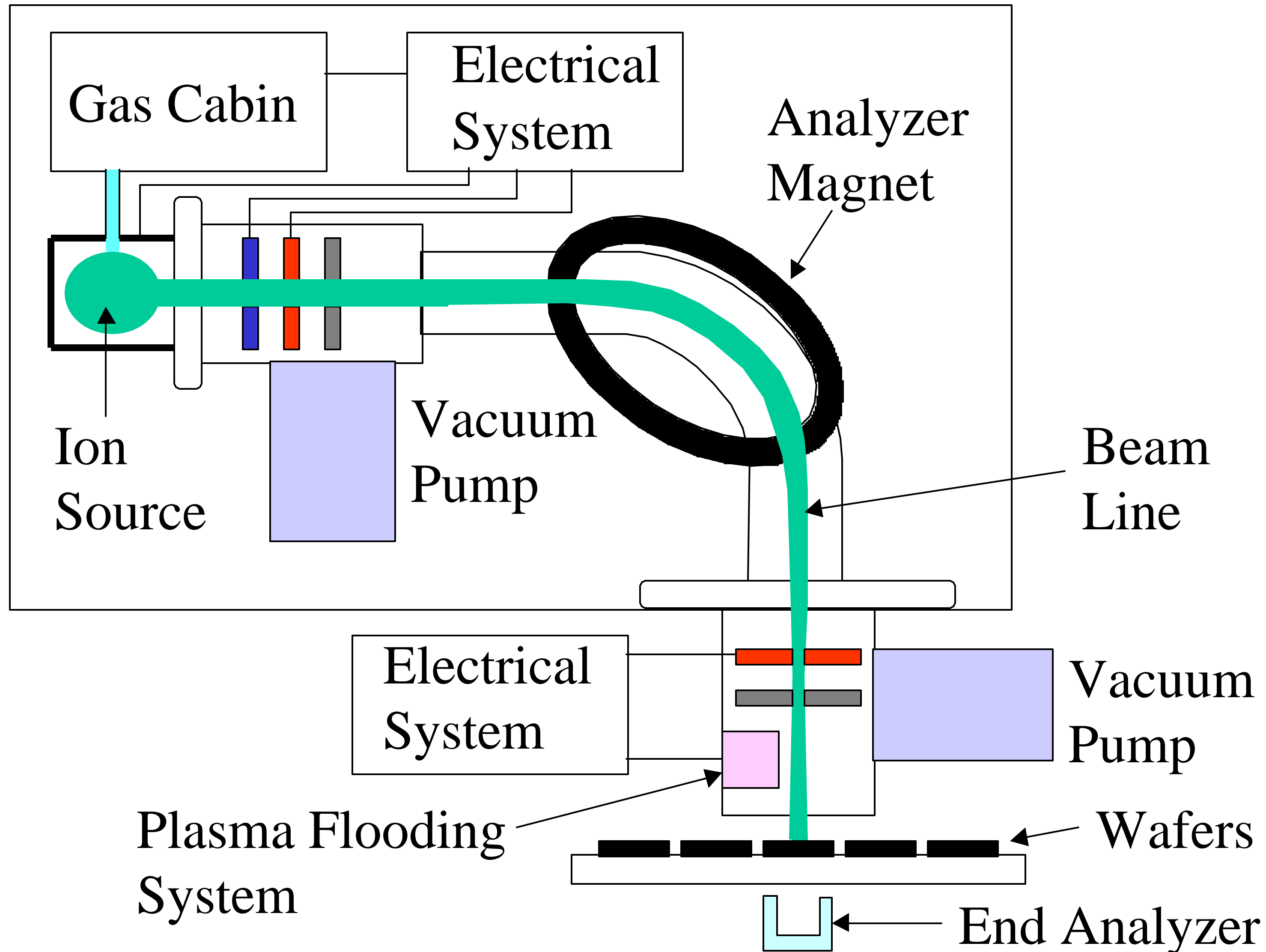
- Gas system
- Electrical system
- Vacuum system
- Ion beamline

Ion Implanter

Implantation Process



Ion Implanter



Ion Implantation: Gas System

- Special gas deliver system to handle hazardous gases
- Special training needed to change gases bottles
- Argon is used for purge and beam calibration

Ion Implantation: Electrical System

- High voltage system
  - Determine ion energy that controls junction depth
- High voltage system
  - Determine ion energy that controls junction depth
- RF system
  - Some ion sources use RF to generate ions

Ion Implantation: Vacuum System

- Need high vacuum to accelerate ions and reduce collision
- MFP >> beamline length
- 10^{-5} to 10^{-7} Torr
- Turbo pump and Cryo pump
- Exhaust system

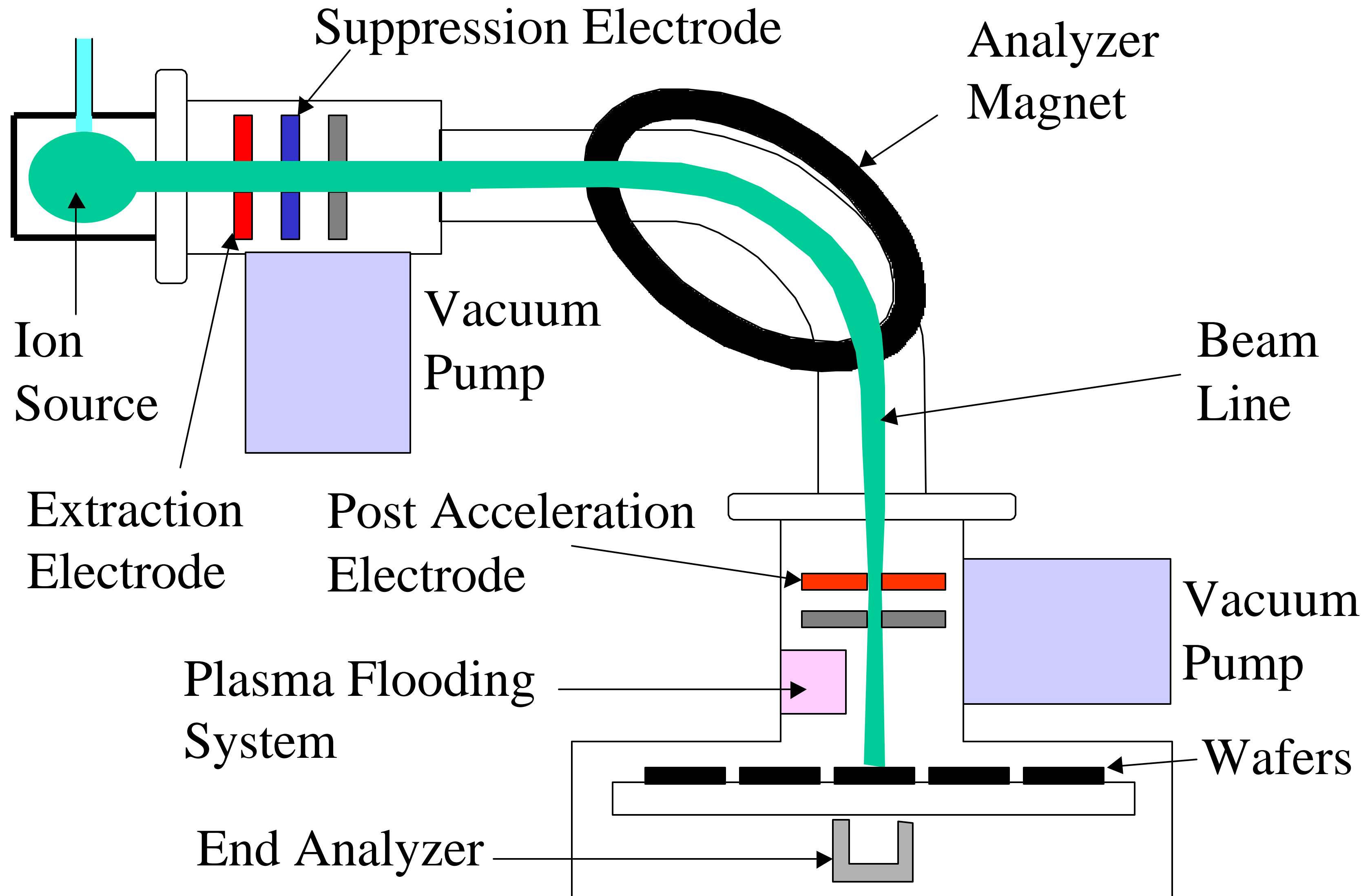
Ion Implantation: Control System

- Ion energy, beam current, and ion species.
- Mechanical parts for loading and unloading
- Wafer movement to get uniform beam scan
- CPU board control boards
  - Control boards collect data from the systems, send it to CPU board to process,
  - CPU sends instructions back to the systems through the control board.

Ion Implantation: Beamline

- Ion source
- Extraction electrode
- Analyzer magnet
- Post acceleration
- Plasma flooding system
- End analyzer

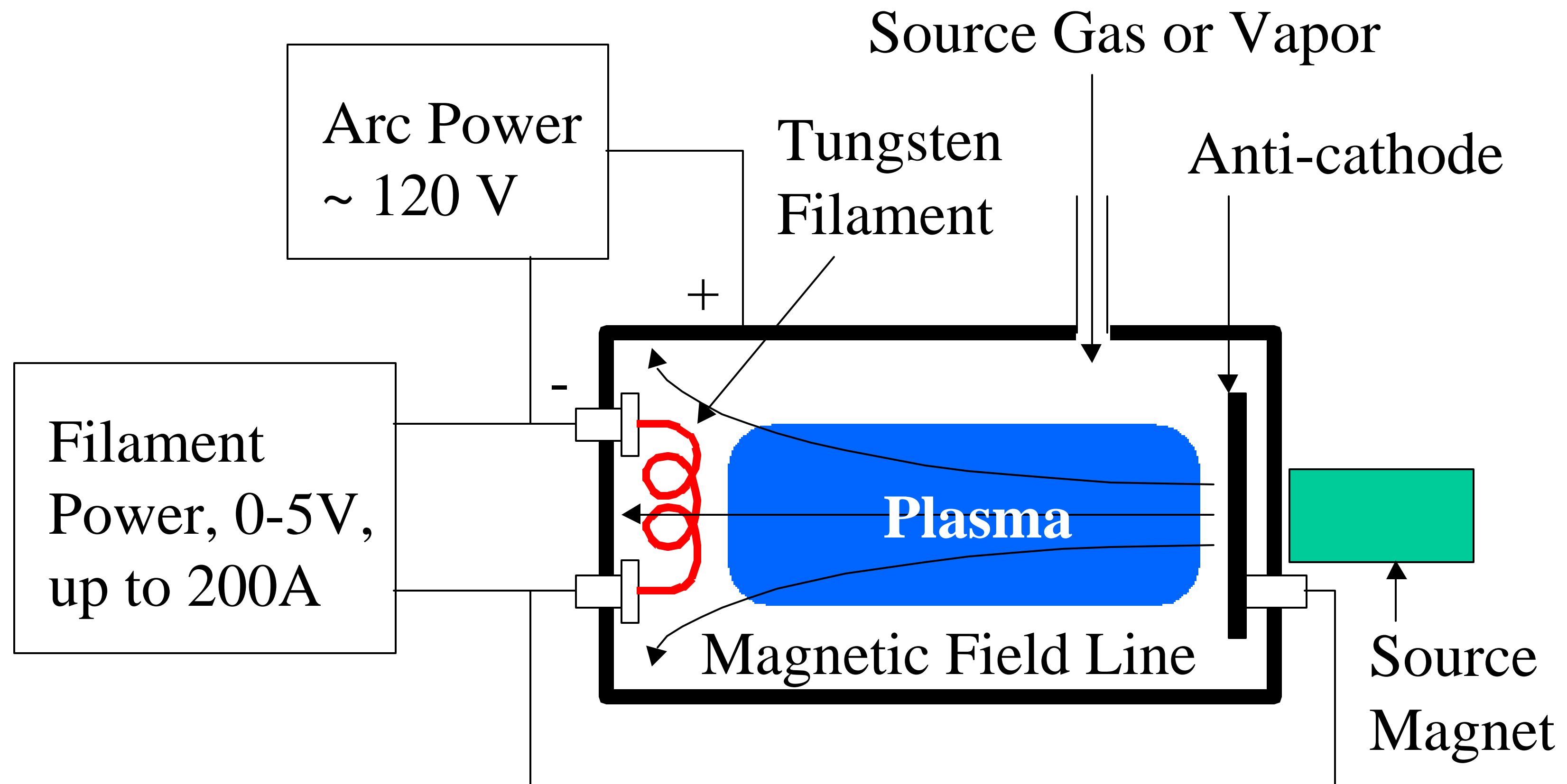
Ion Beam Line



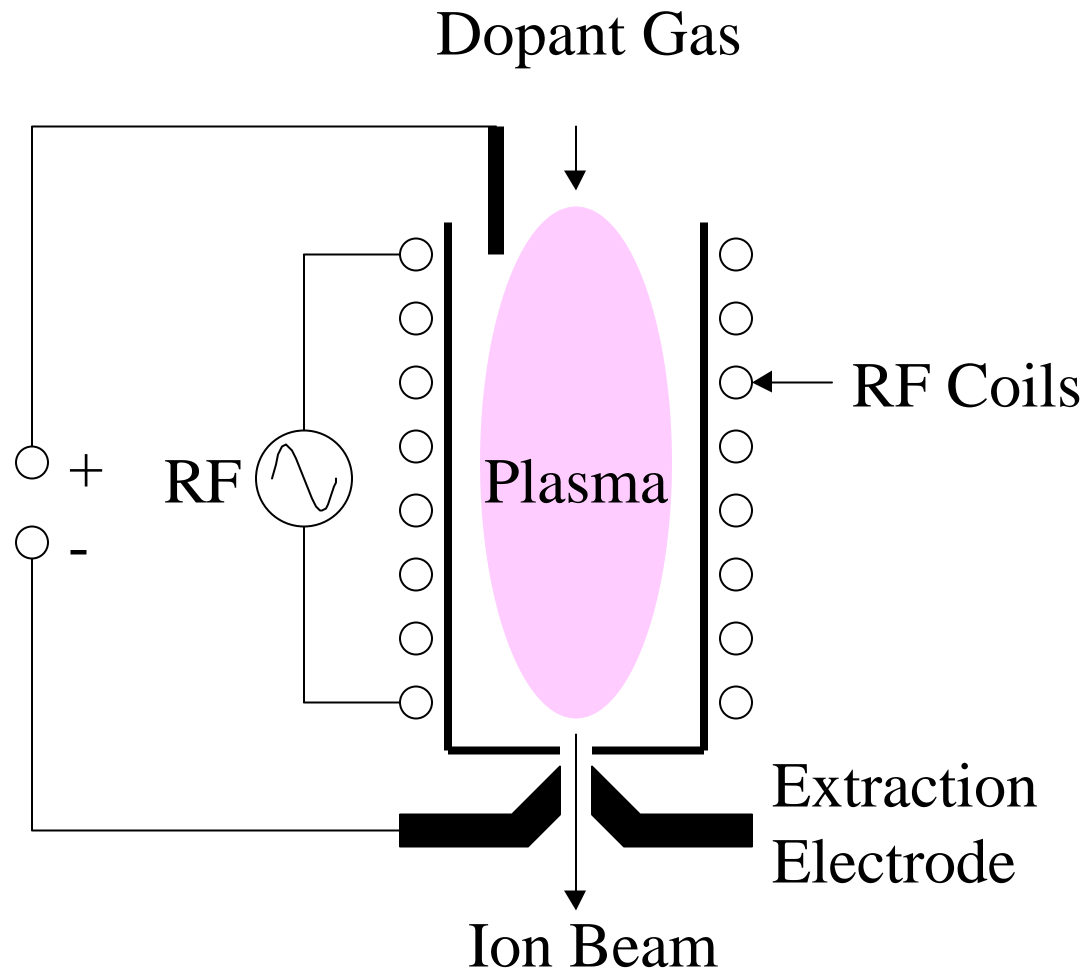
Ion implanter: Ion Source

- Hot tungsten filament emits thermal electron
- Electrons collide with source gas molecules to dissociate and ionize
- Ions are extracted out of source chamber and accelerated to the beamline
- RF and microwave power can also be used to ionize source gas

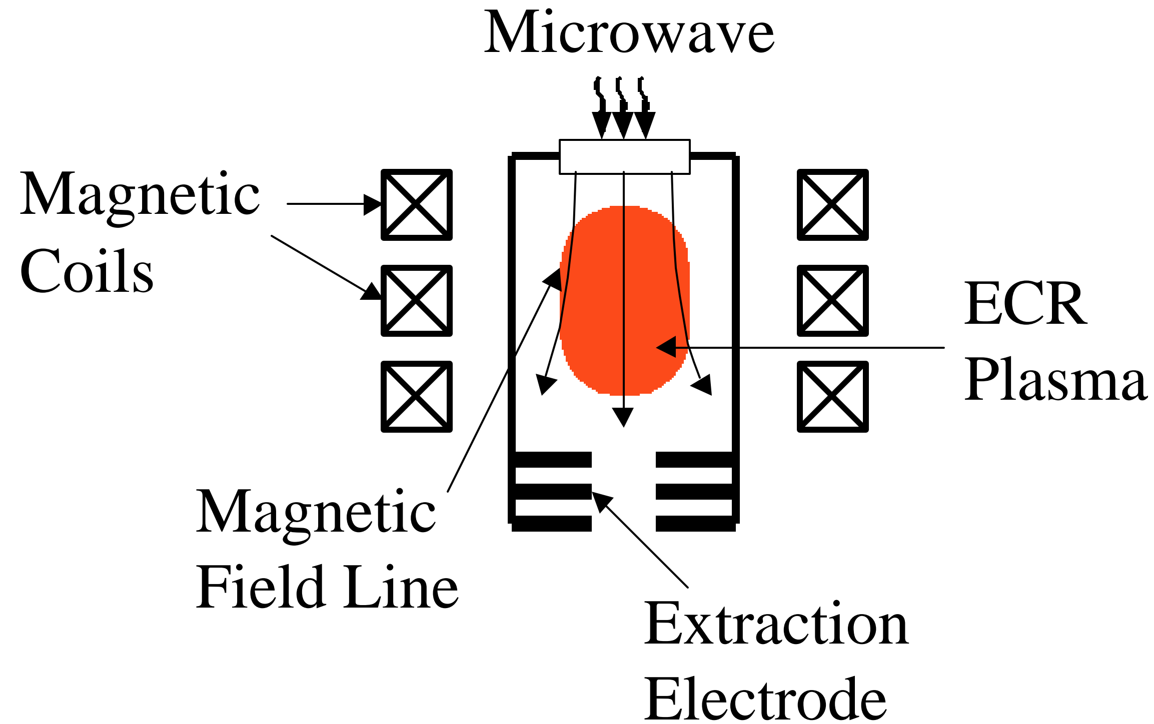
Ion Source



RF Ion Source



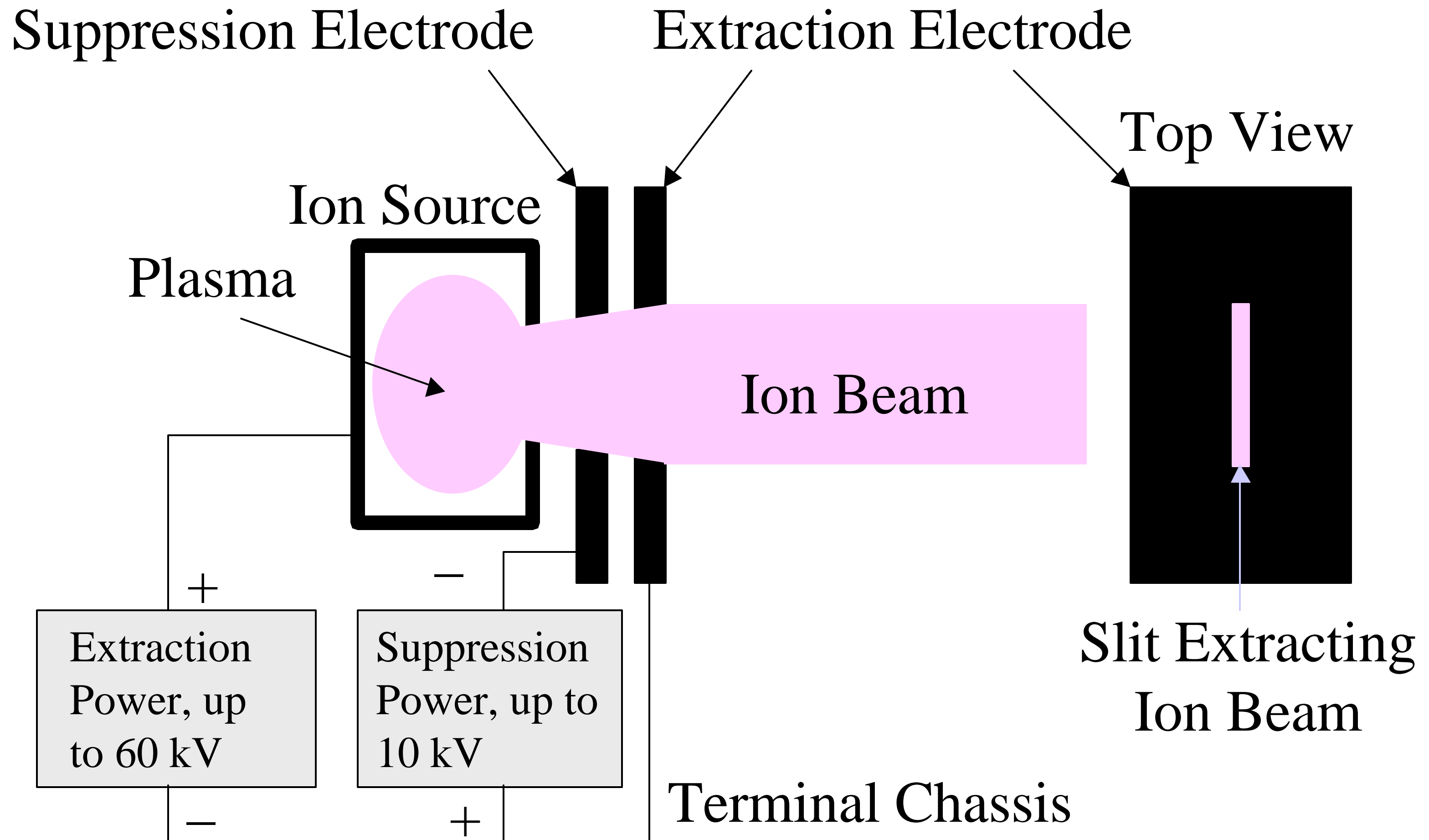
Microwave Ion Source



Ion Implantation: Extraction

- Extraction electrode accelerates ions up to 50 keV
- High energy is required for analyzer magnet to select right ion species.

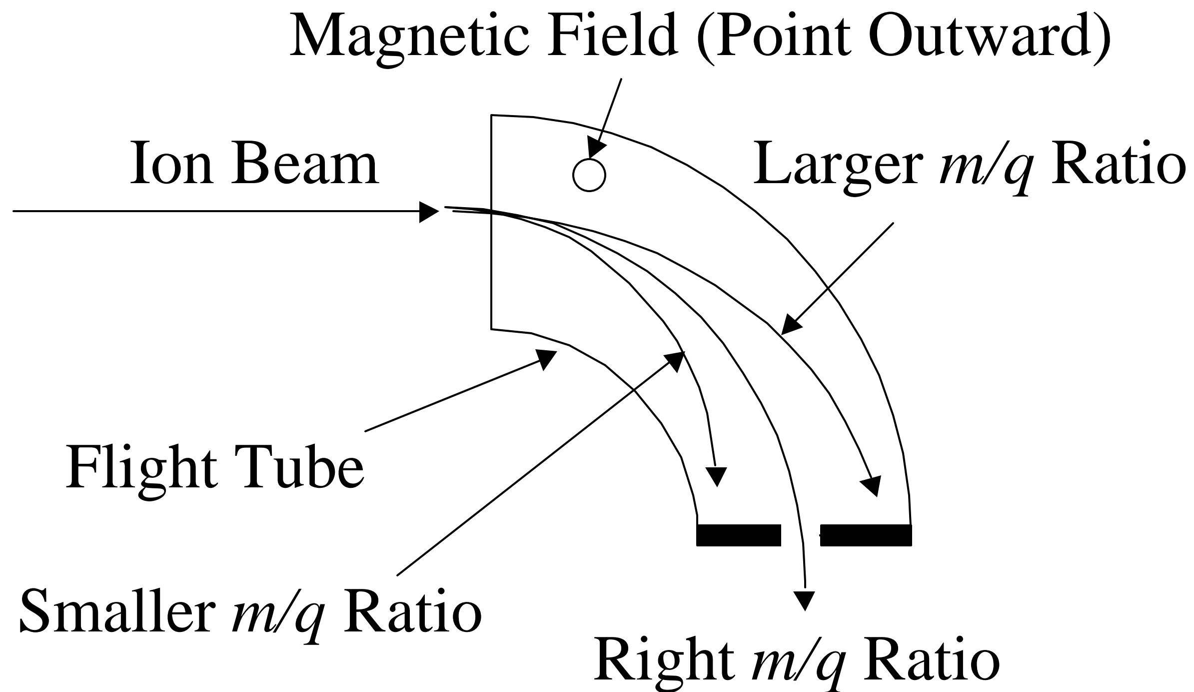
Extraction Assembly



Ion Implantation: Analyzer Magnet

- Gyro radius of charge particle in magnetic field relate with B-field and mass/charge ratio
- Used for isotope separation to get enriched U_{235}
- Only ions with right mass/charge ratio can go through the slit
- Purified the implanting ion beam

Analyzer



Ions in BF_3 Plasma

Ions	Atomic or molecule weight
^{10}B	10
^{11}B	11
^{10}BF	29
^{11}BF	30
F_2	38
$^{10}BF_2$	48
$^{11}BF_2$	49

Question and Answer

$^{10}B^+$ is lighter and can penetrate deeper than $^{11}B^+$, why don't use $^{10}B^+$ in deep junction implantation?

- Only 20% of boron atoms are ^{10}B
- $^{10}B^+$ ion concentration is only 1/4 of $^{11}B^+$
- $^{10}B^+$ beam current is 1/4 of $^{11}B^+$ beam current
- Quadruple implantation time, lower throughput

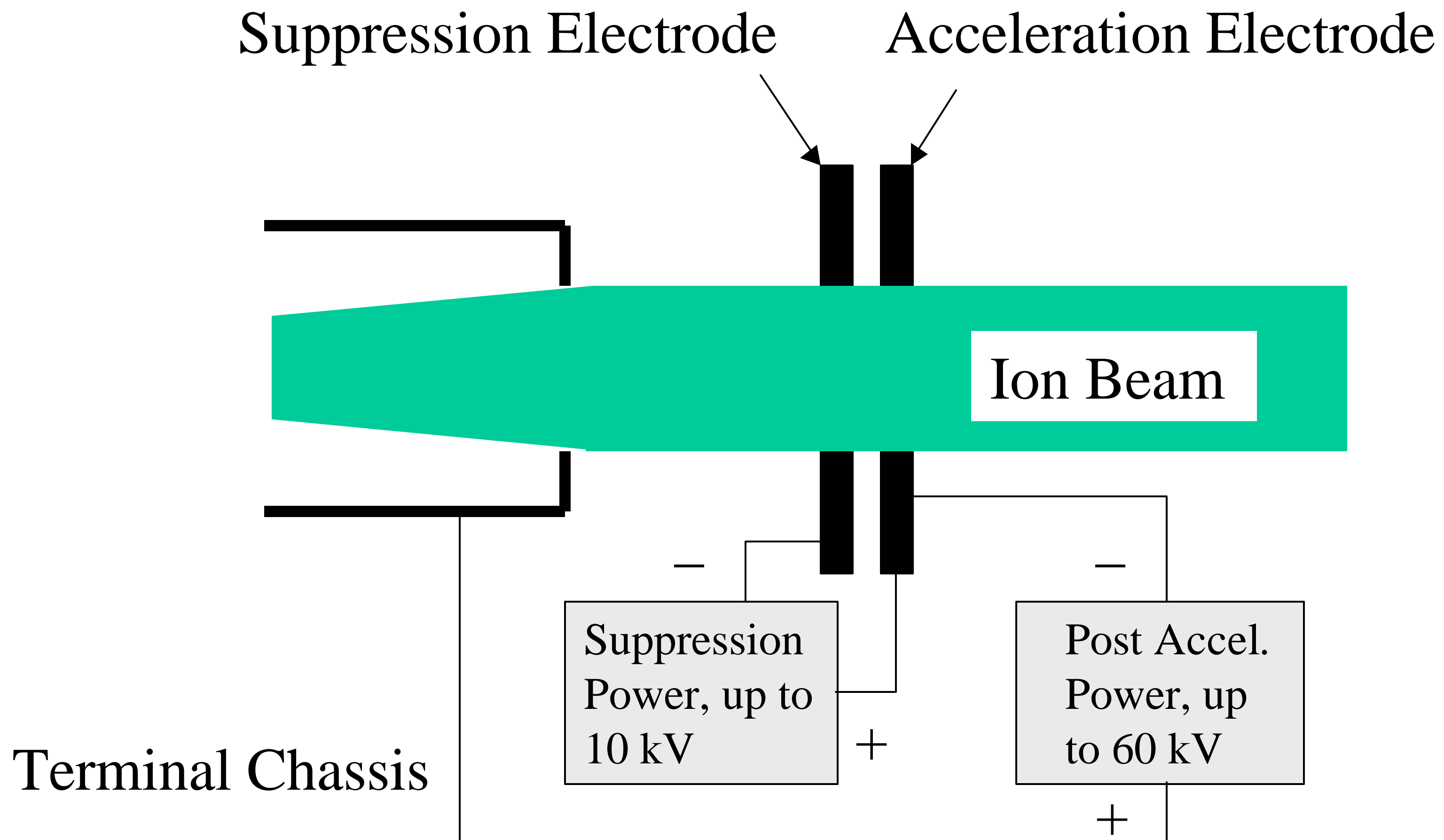
Ion Implantation: Post Acceleration

- Increasing (sometimes decreasing) ion energy for ion to reach the required junction depth determined by the device
- Electrodes with high DC voltage
- Adjustable vertical vanes control beam current

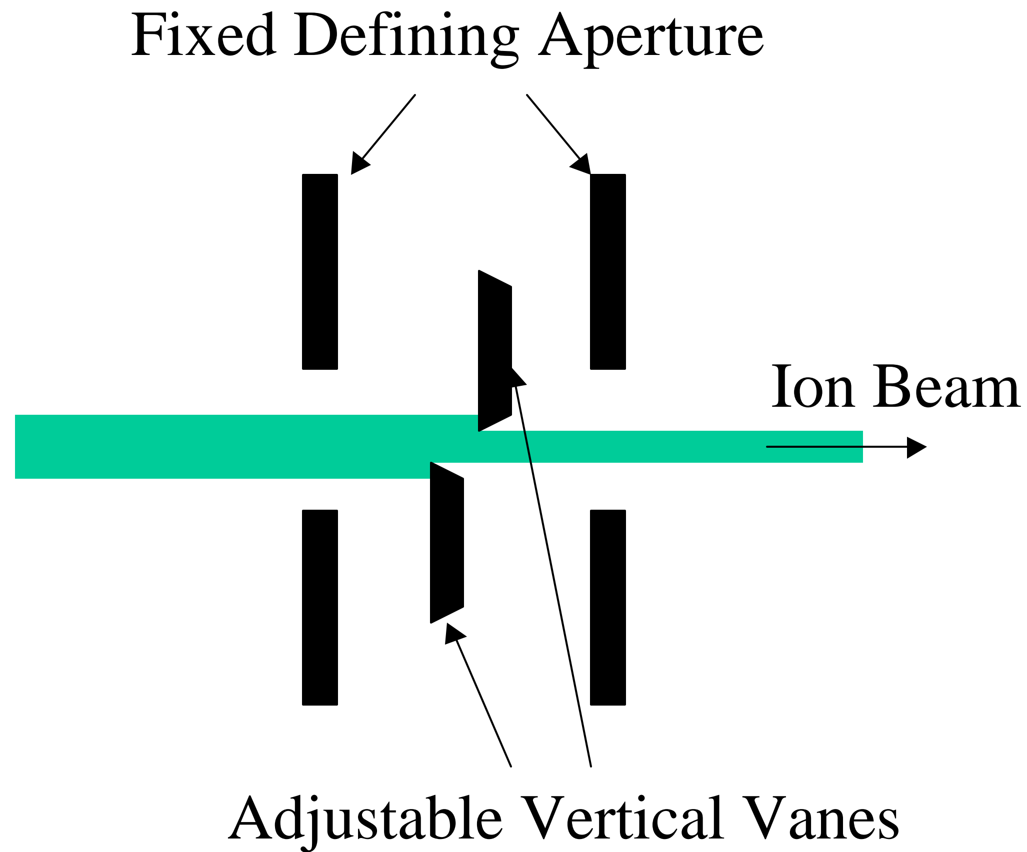
Ion Implantation: Plasma Flooding System

- Ions cause wafer charging
- Wafer charging can cause non-uniform doping and arcing defects
- Elections are “flooding” into ion beam and neutralized the charge on the wafer
- Argon plasma generated by thermal electrons emit from hot tungsten filament

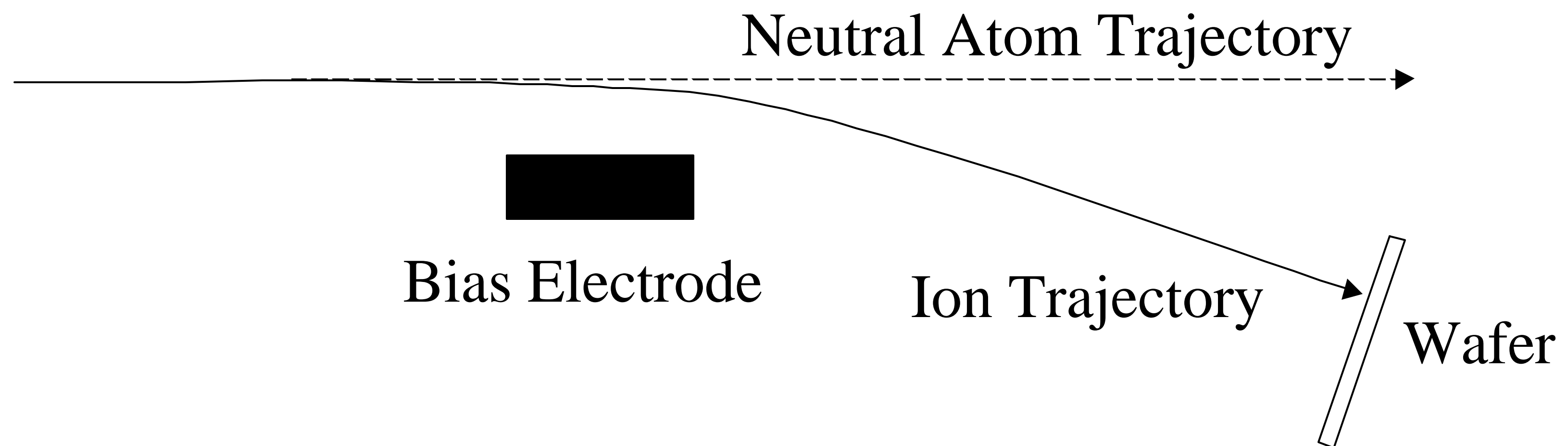
Post Acceleration



Ion Beam Current Control



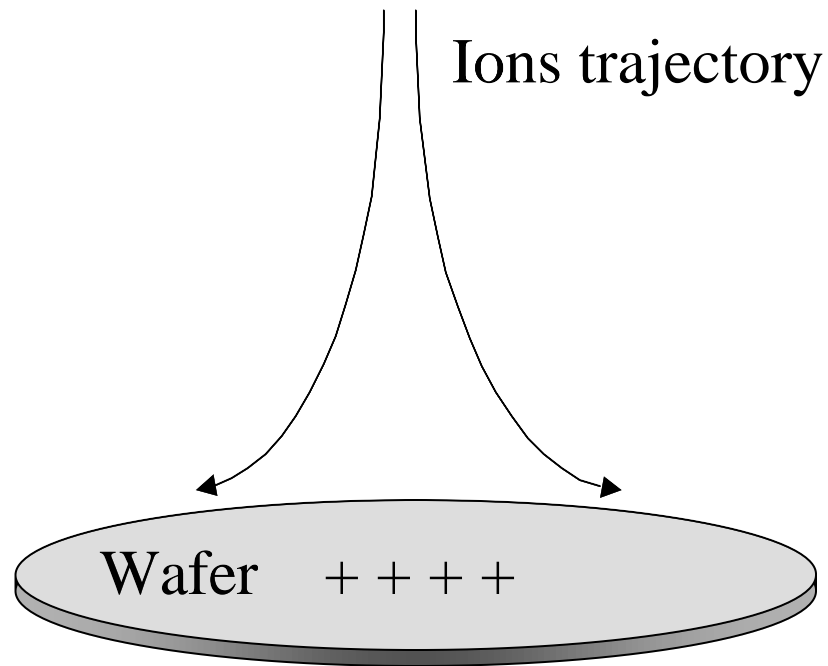
Bending Ion Trajectory



Charge Neutralization System

- Implanted ions charge wafer positively
- Cause wafer charging effect
- Expel positive ion, cause beam blowup and result non-uniform dopant distribution
- Discharge arcing create defects on wafer
- Breakdown gate oxide, low yield
- Need eliminate or minimize charging effect

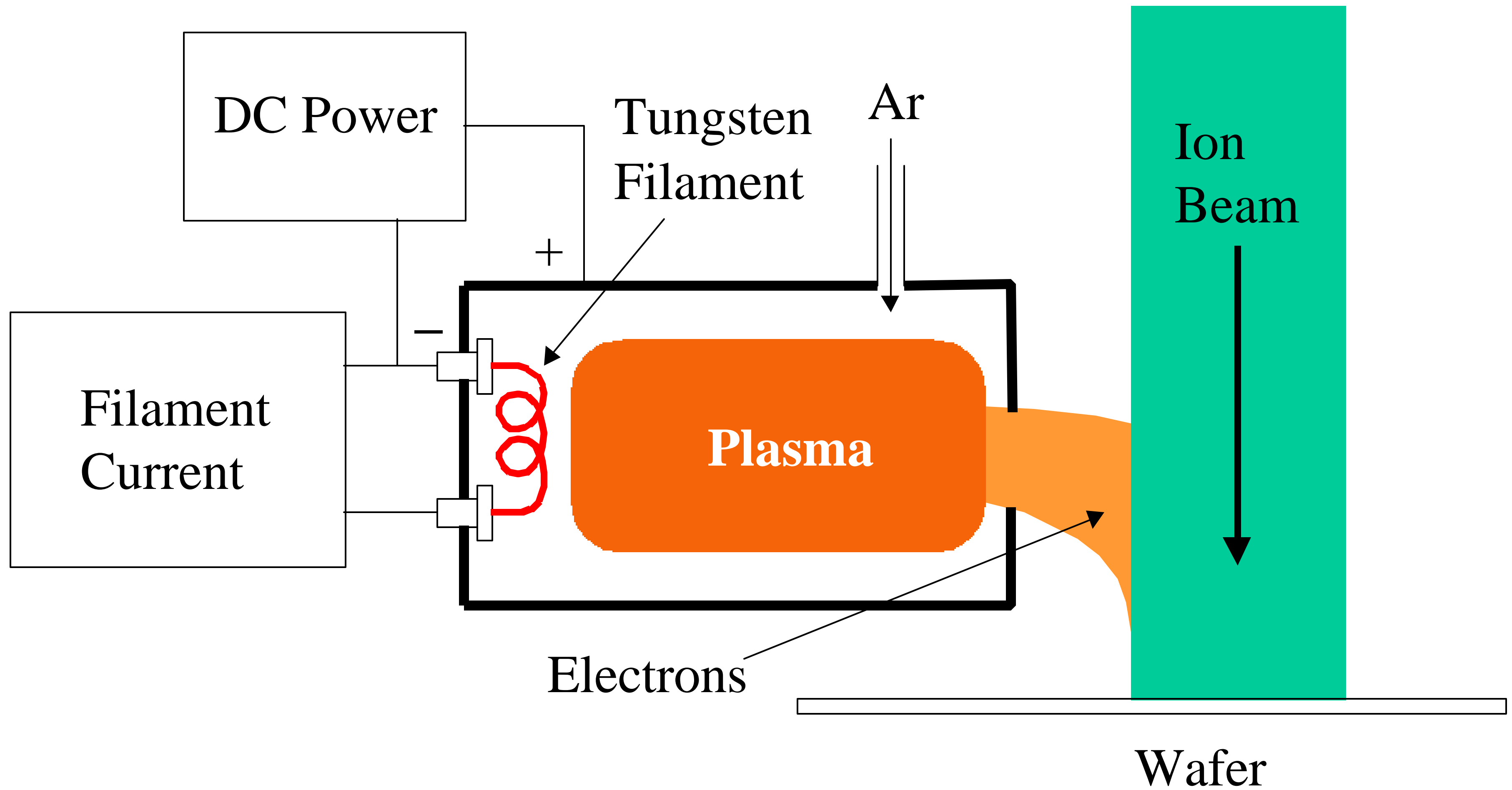
Charging Effect



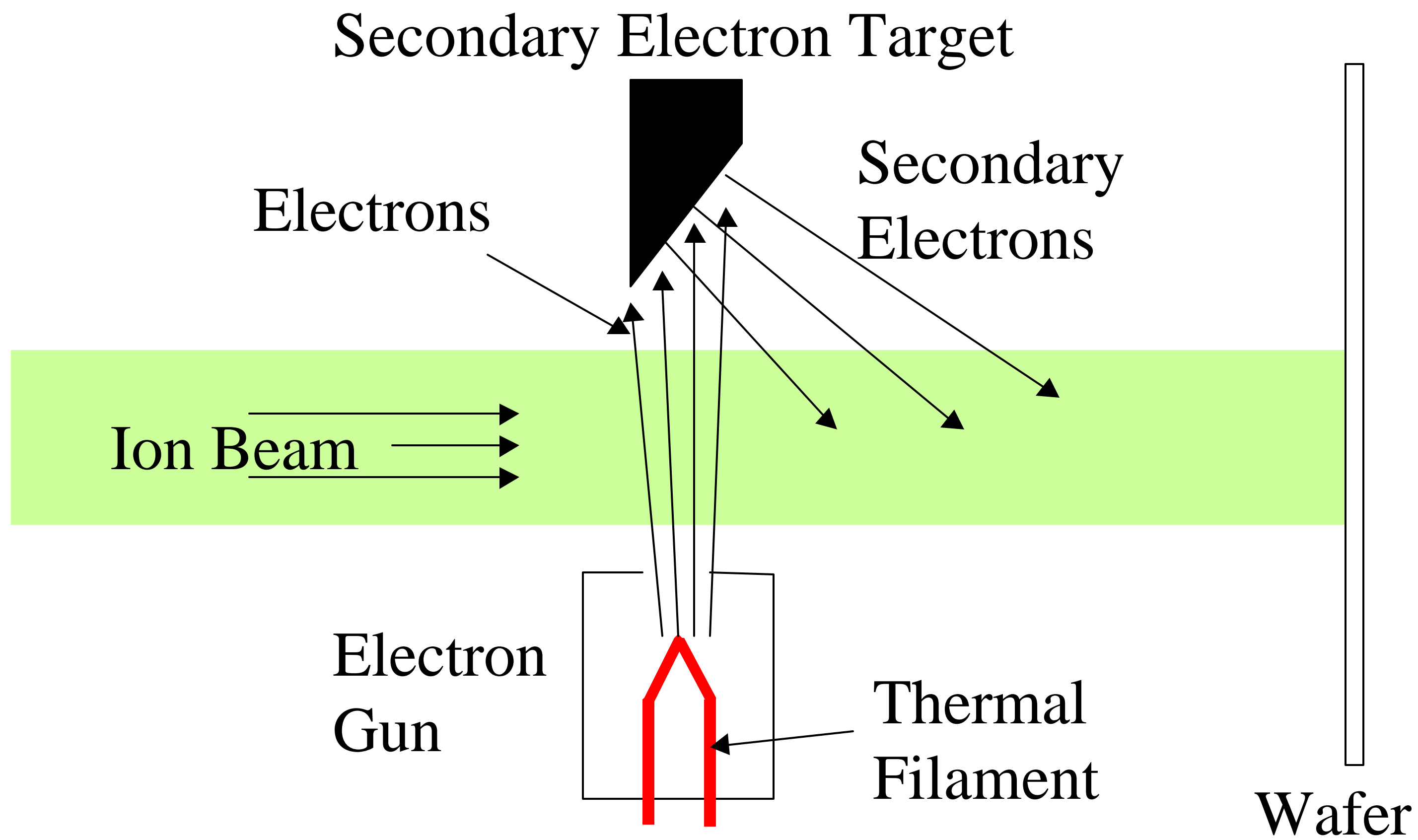
Charge Neutralization System

- Need to provide electrons to neutralize ions
- Plasma flooding system
- Electron gun
- Electron shower are used to

Plasma Flooding System



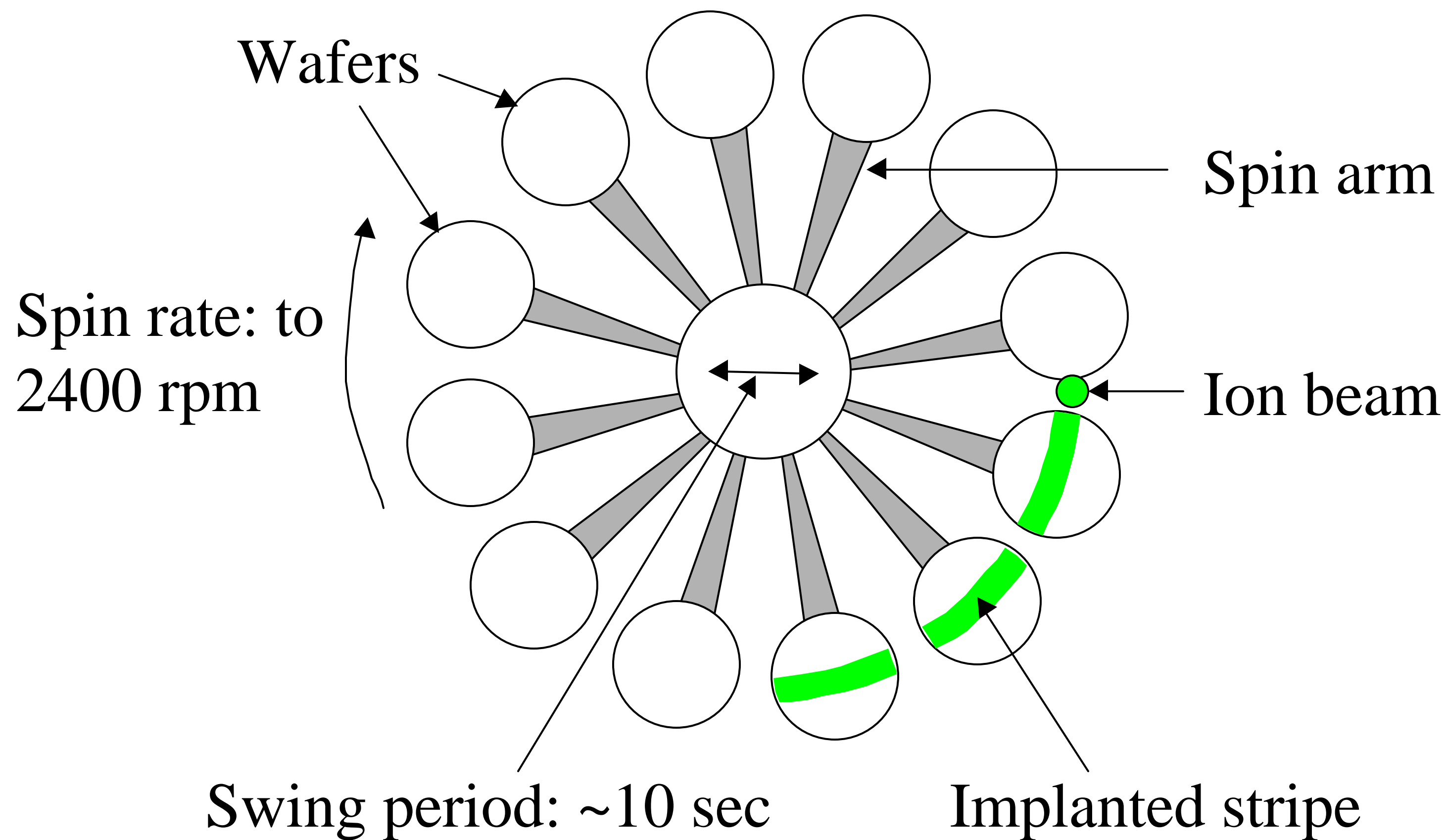
Electron Gun



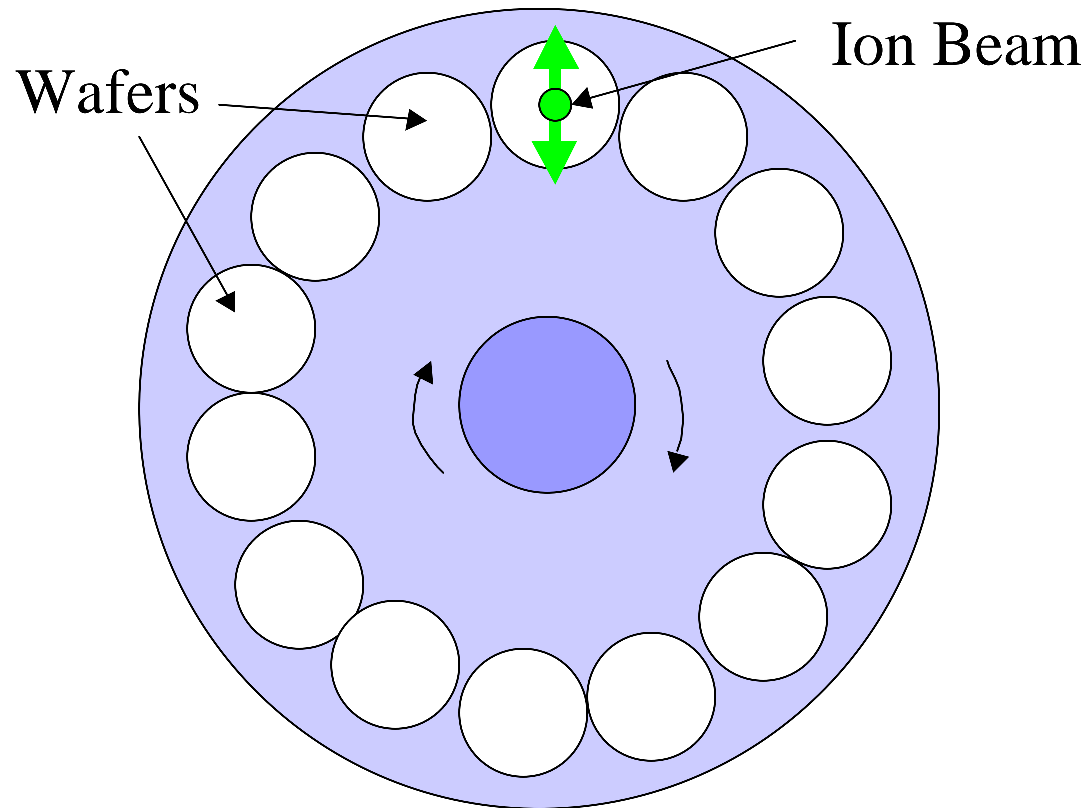
Wafer Handling

- Ion beam diameter: ~25 mm (~1”),
- Wafer diameter: 200 mm (8”) or larger
- Needs to move beam or wafer, or both, to scan ion beam across the whole wafer
  - Spin wheel
  - Spin disk
  - Single wafer scan

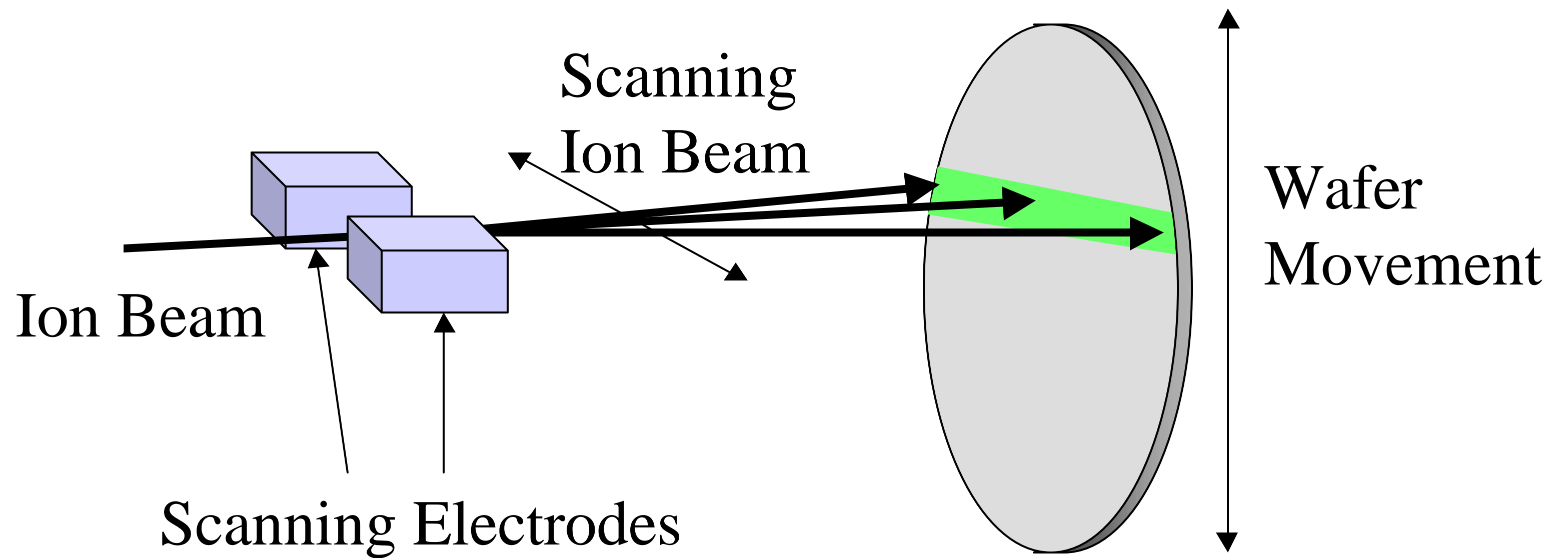
Spin Wheel



Spin Disk



Single Wafer Scanning System



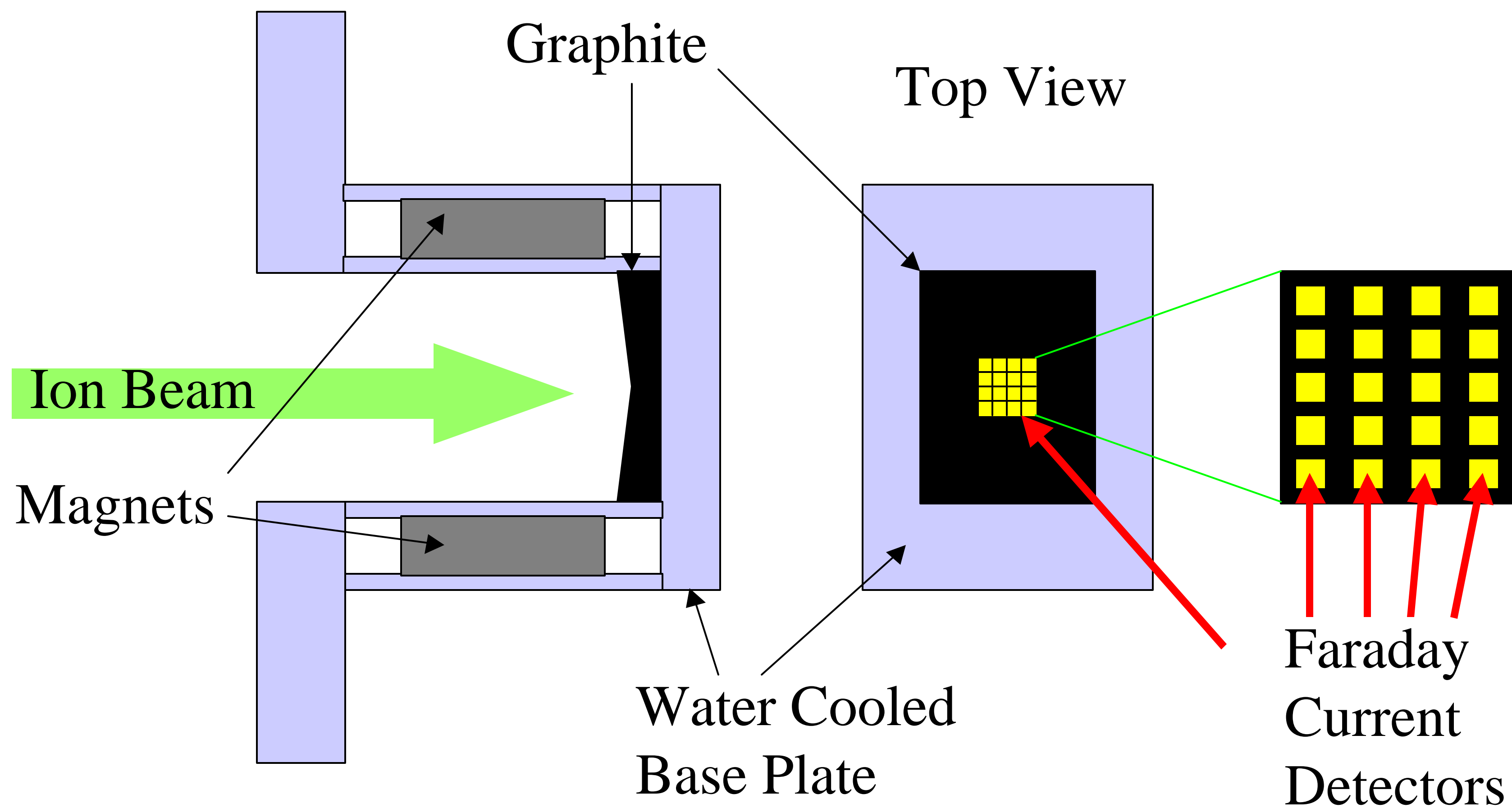
Ion Implantation: Beam Stop

- absorb the ion beam energy,
- ion beam detector
  - beam current, beam energy, and beam shape measurement
- Water cooled metal plate carries away the heat and blocks the X-ray radiation

Ion Implantation: End Analyzer

- Faraday charge detector
- Used to calibrate beam current, energy and profile

Beam Stop



Ion Implantation: The Process

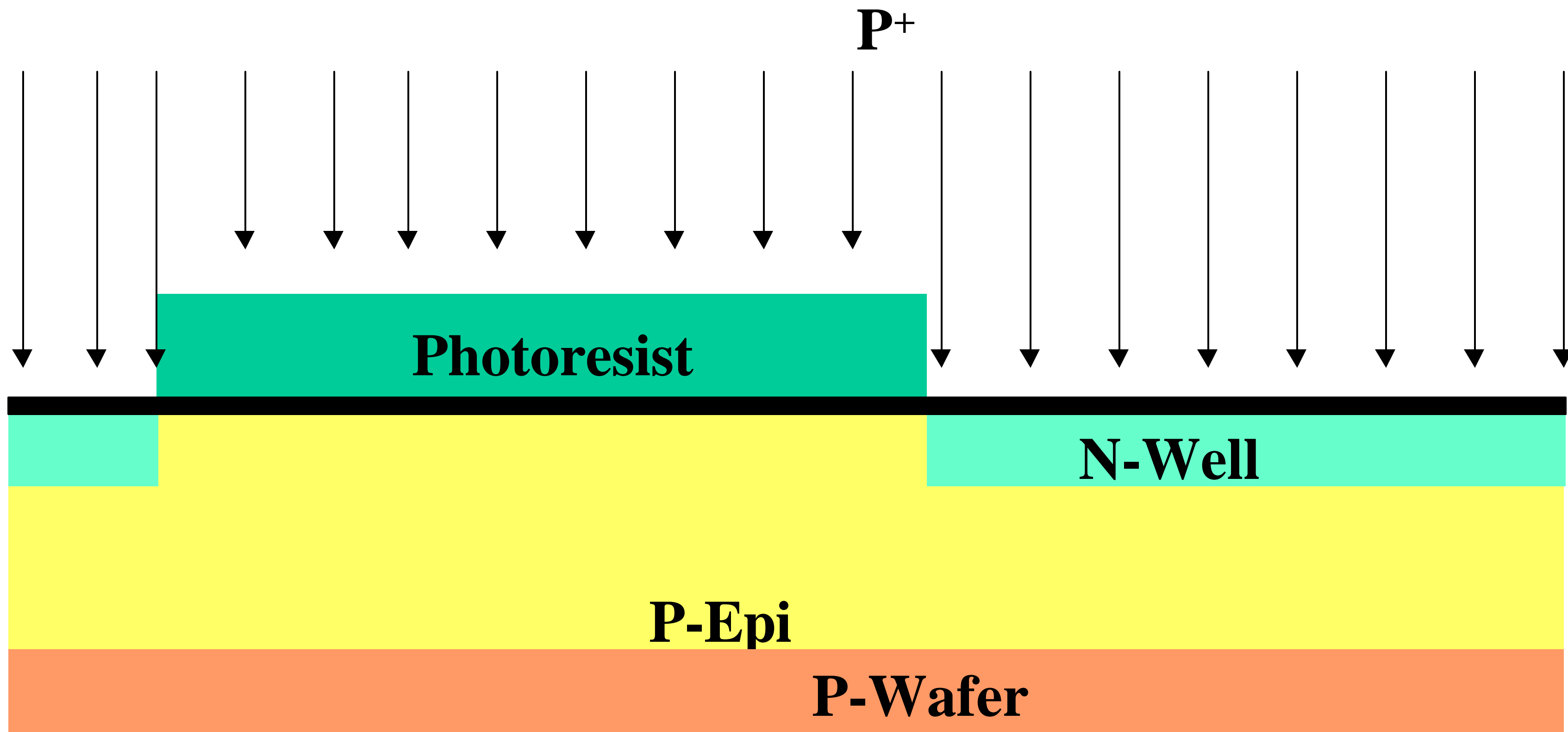
- CMOS applications
- CMOS ion implantation requirements
- Implantation process evaluations

CMOS Implantation Requirements

Implant Step	**0.35 μm, 64 Mb**	**0.25 μm, 256 Mb**	**0.18 μm, 1 Gb**
N-well			
Well	$P/600/2\times10^{13}$	$P/400/2\times10^{13}$	$P/300/1\times10^{13}$
Anti-punch through	$P/100/5\times10^{13}$	$As/100/5\times10^{12}$	$As/50/2\times10^{12}$
Threshold	$B/10/7\times10^{12}$	$B/5/3\times10^{12}$	$B/2/4\times10^{12}$
Poly dope	$P/30/2\times10^{15}$	$B/20/2\times10^{15}$	$B/20/3\times10^{15}$
Poly diffusion block	-	-	$N_2/20/3\times10^{15}$
Lightly doped drain (LDD)	$B/7/5\times10^{13}$	$B/5/1\times10^{14}$	$B/2/8\times10^{13}$
Halo (45° implant)	-	-	$As/30/5\times10^{13}$
Source/drain contact	$B/10/2\times10^{15}$	$B/7/2\times10^{15}$	$B/6/2\times10^{15}$
P-well			
Well	$B/225/3\times10^{13}$	$B/200/1\times10^{13}$	$B/175/1\times10^{13}$
Anti-punch through	$B/30/2\times10^{13}$	$B/50/5\times10^{12}$	$B/45/5\times10^{12}$
Threshold	$B/10/7\times10^{12}$	$B/5/3\times10^{12}$	$B/2/4\times10^{12}$
Poly dope	$P/30/5\times10^{15}$	$P/20/2\times10^{15}$	$As/40/3\times10^{15}$
Poly diffusion block	-	-	$N_2/20/3\times10^{15}$
Lightly doped drain (LDD)	$P/20/5\times10^{13}$	$P/12/5\times10^{13}$	$P/5/3\times10^{13}$
Halo (45° implant)	$B/30/3\times10^{12}$	$B/20/3\times10^{12}$	$B/7/2\times10^{13}$
Source/drain contact	$As/30/3\times10^{15}$	$As/20/3\times10^{15}$	$As/15/3\times10^{15}$

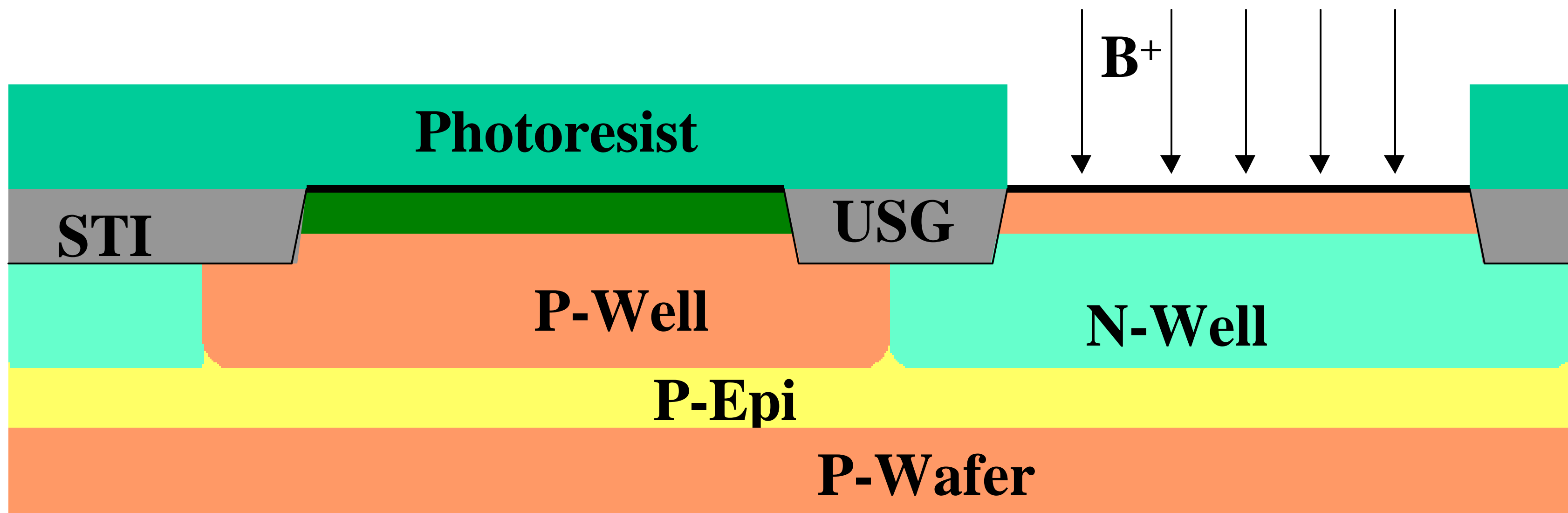
Implantation Process: Well Implantation

- High energy (to MeV), low current ($10^{13}/cm^2$)



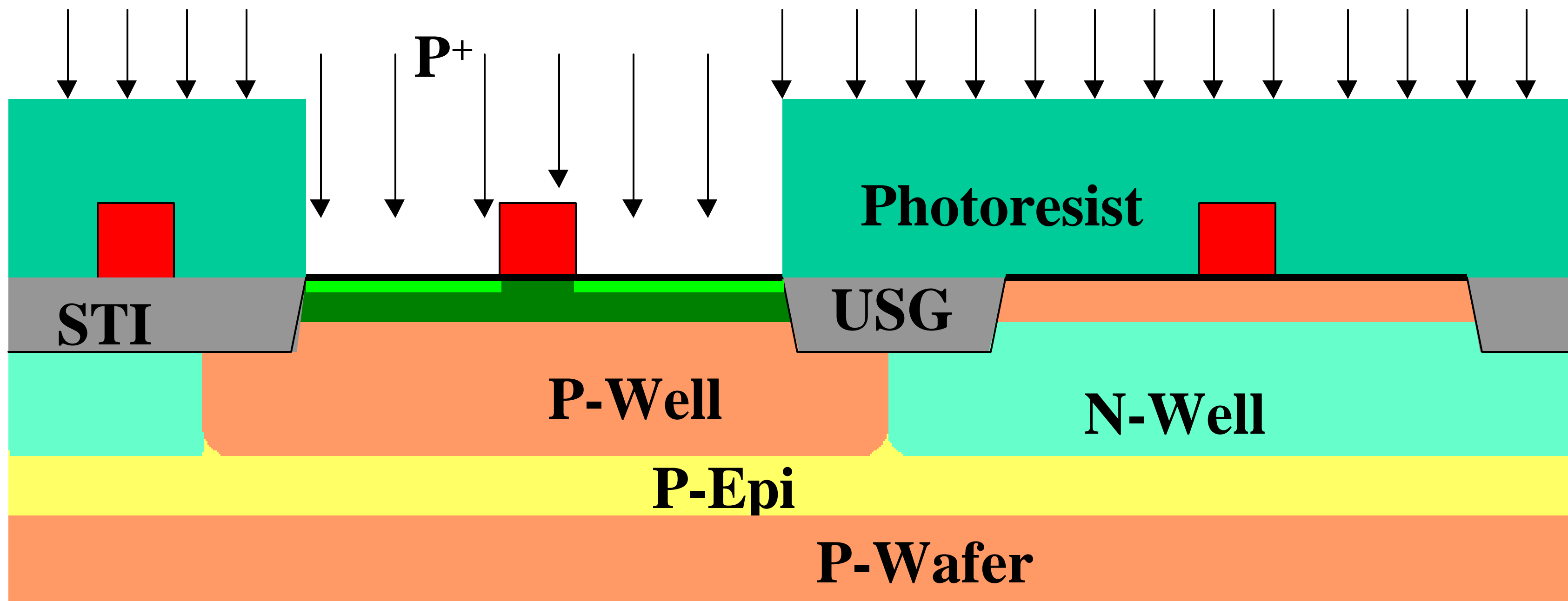
Implantation Process: V_T Adjust Implantation

Low Energy , Low Current



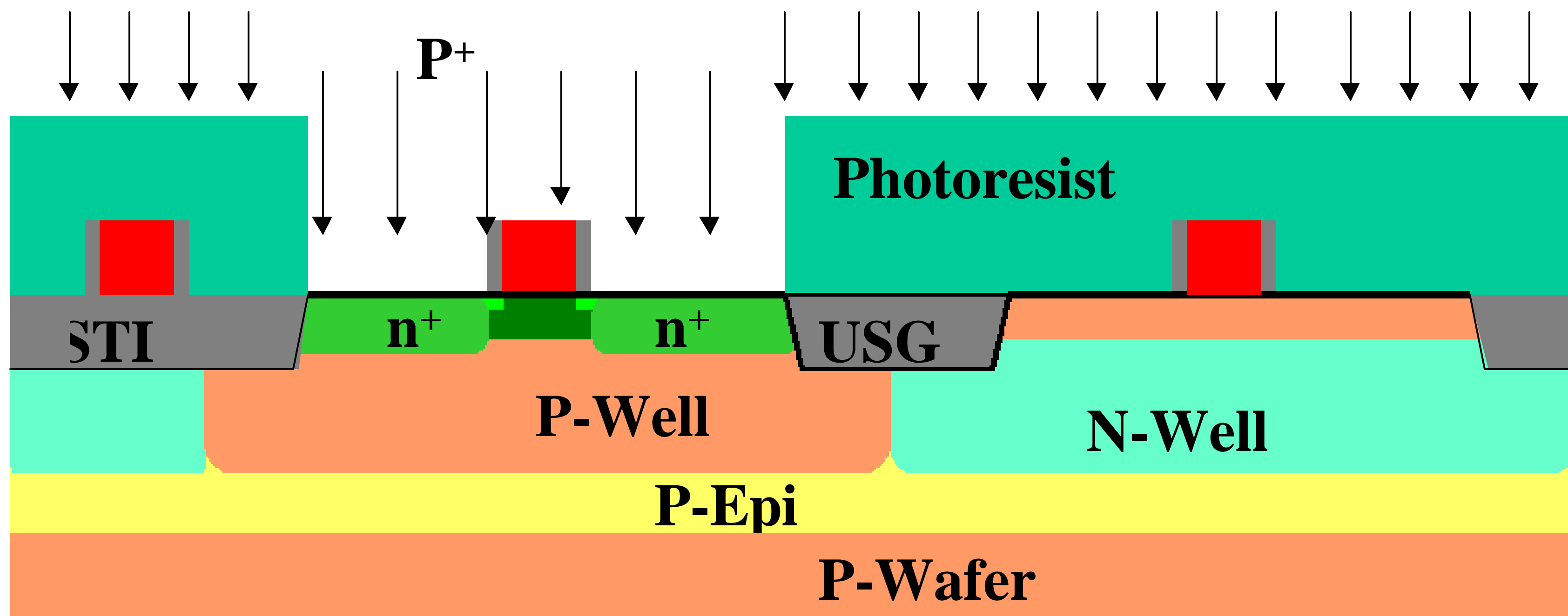
Lightly Doped Drain (LDD) Implantation

- Low energy (10 keV), low current ($10^{13}/cm^2$)



Implantation Process: S/D Implantation

- Low energy (20 keV), high current (>10^{15}/cm^2)



Ion Implantation Processes

Ion Implantation	Energy	Current
Well	High energy	low current
Source/Drain	Low energy	high current
V_T Adjust	Low energy	low current
LDD	Low energy	low current

Process Issues

- Wafer charging
- Particle contamination
- Elemental contamination
- Process evaluation

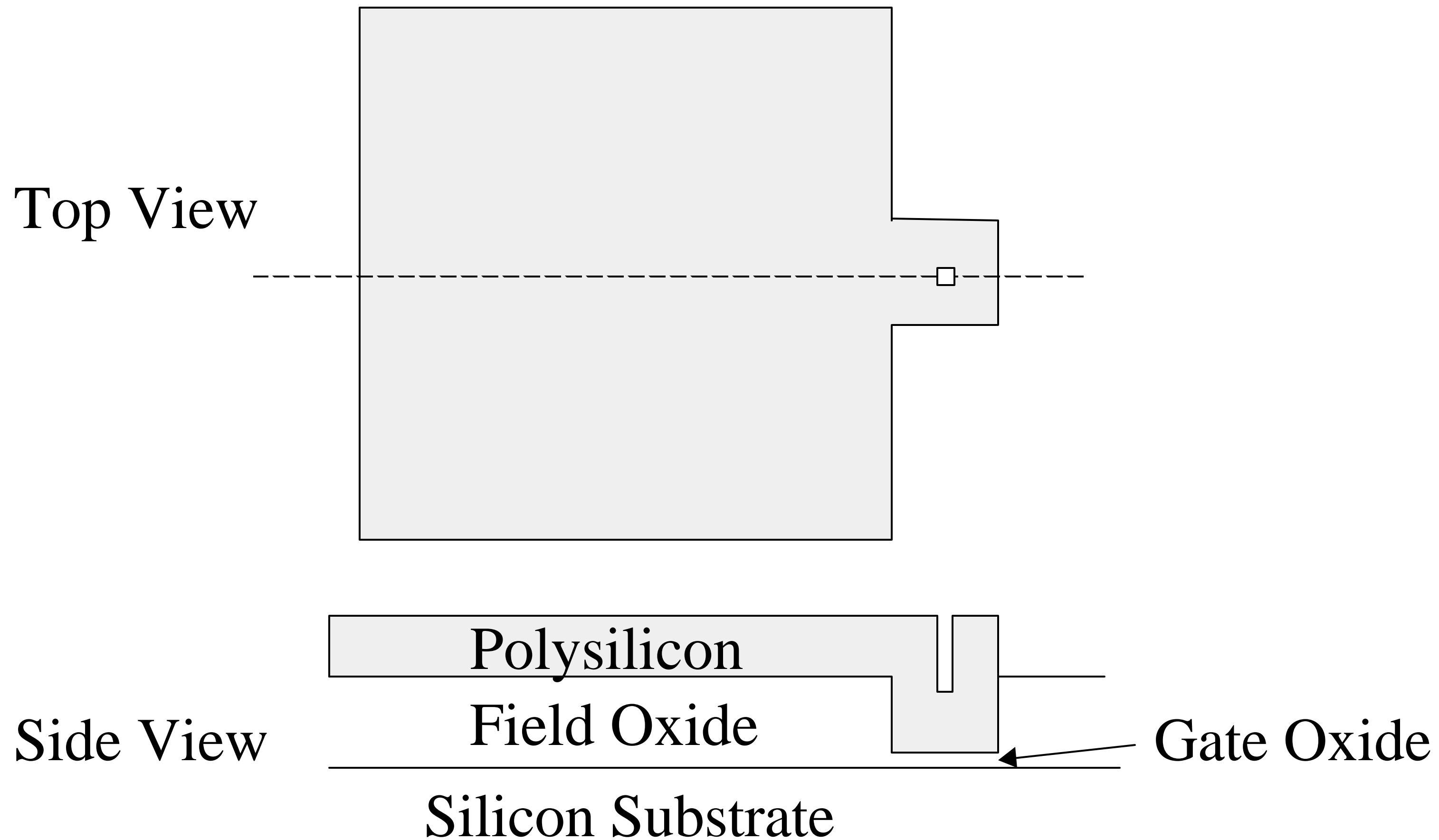
Wafer Charging

- Break down gate oxide
- Dielectric strength of SiO_2: ~10 MV/cm
- 100 Å oxide breakdown voltage is 10 V
- Gate oxide: 30 to 35 Å for 0.18 μm device
- Require better charge neutralization

Wafer Charging Monitoring

- Antenna capacitor changing test structure
- The ratio of polysilicon pad area and thin oxide area is called antenna ratio
- Can be as high as 100,000:1
- The larger antenna ratio, the easier to breakdown the thin gate oxide

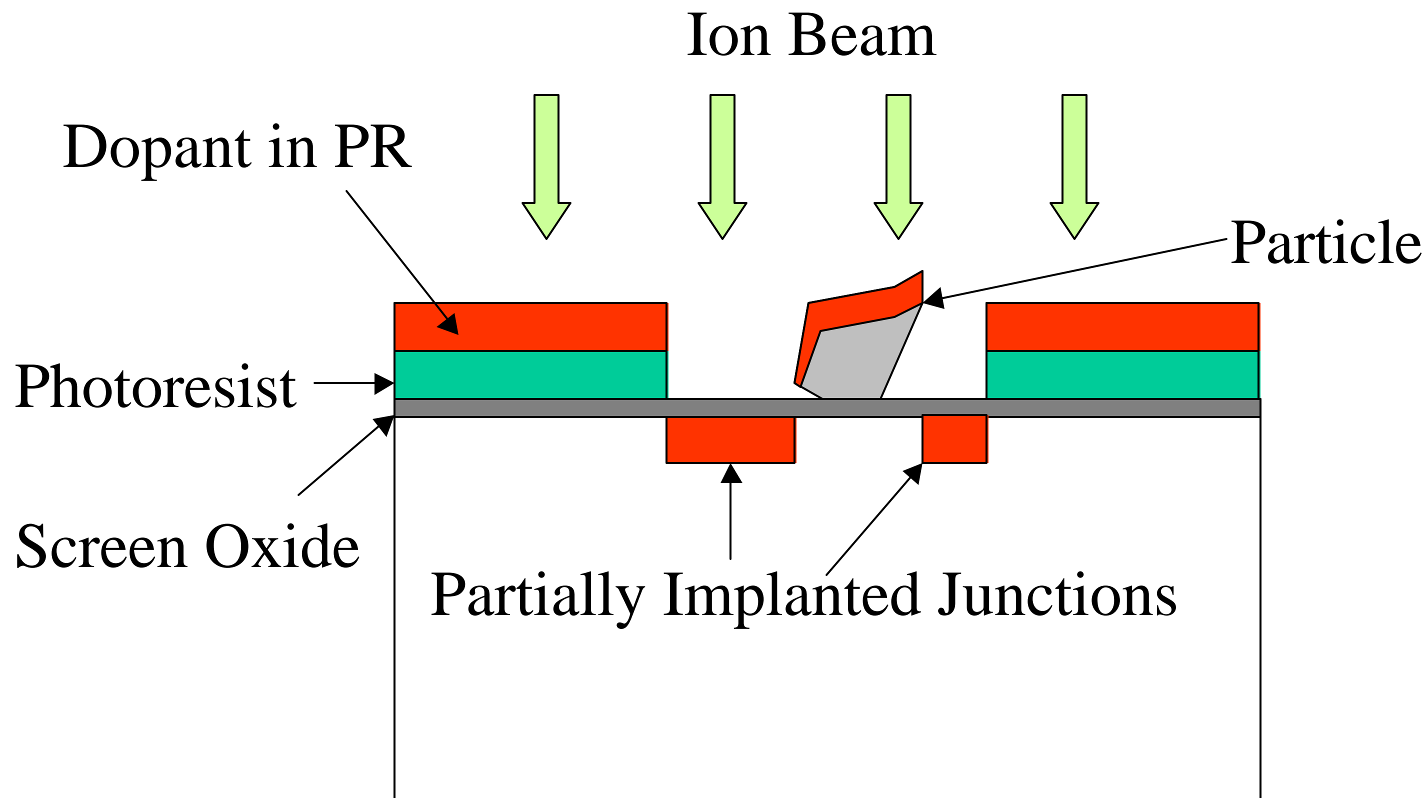
Antenna Ratio



Particle Contamination

- Large particles can block the ion beam especially for the low energy processes,
- V_T adjust, LDD and S/D implantations,
- Cause incomplete dopant junction.
- Harmful to yield

Effect of Particle Contamination



Elemental Contamination

- Co-implantation other elements with intended dopant
- $^{94}Mo^{++}$ and $^{11}BF_2^{+}$, same mass/charge ratio (A/e = 49)
- Mass analyzer can't separate these two
- $^{94}Mo^{++}$ causes heavy metal contamination
- Ion source can't use standard stainless steel
- Other materials such as graphite and tantalum are normally used

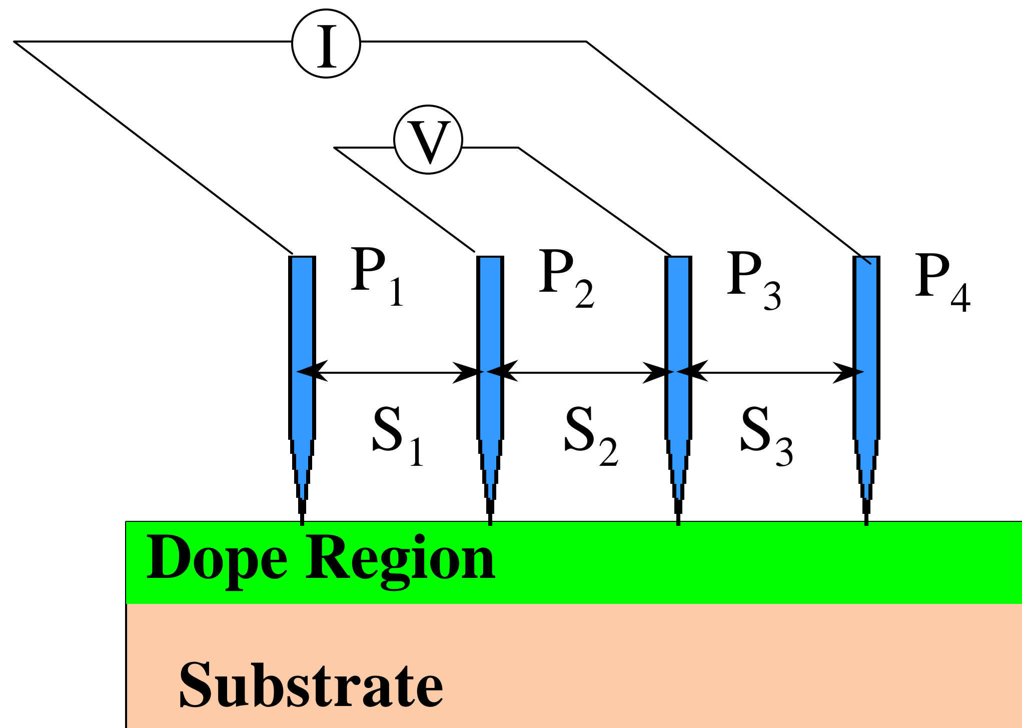
Process Evaluation

- Four-point probe
- Thermal wave
- Optical measurement system (OMS)

Four-Point Probe

- Perform after anneal
- Measure sheet resistance
- Sheet resistant is a function of dopant concentration and junction depth
- Commonly used to monitor doping process

Four-Point Probe Measurement

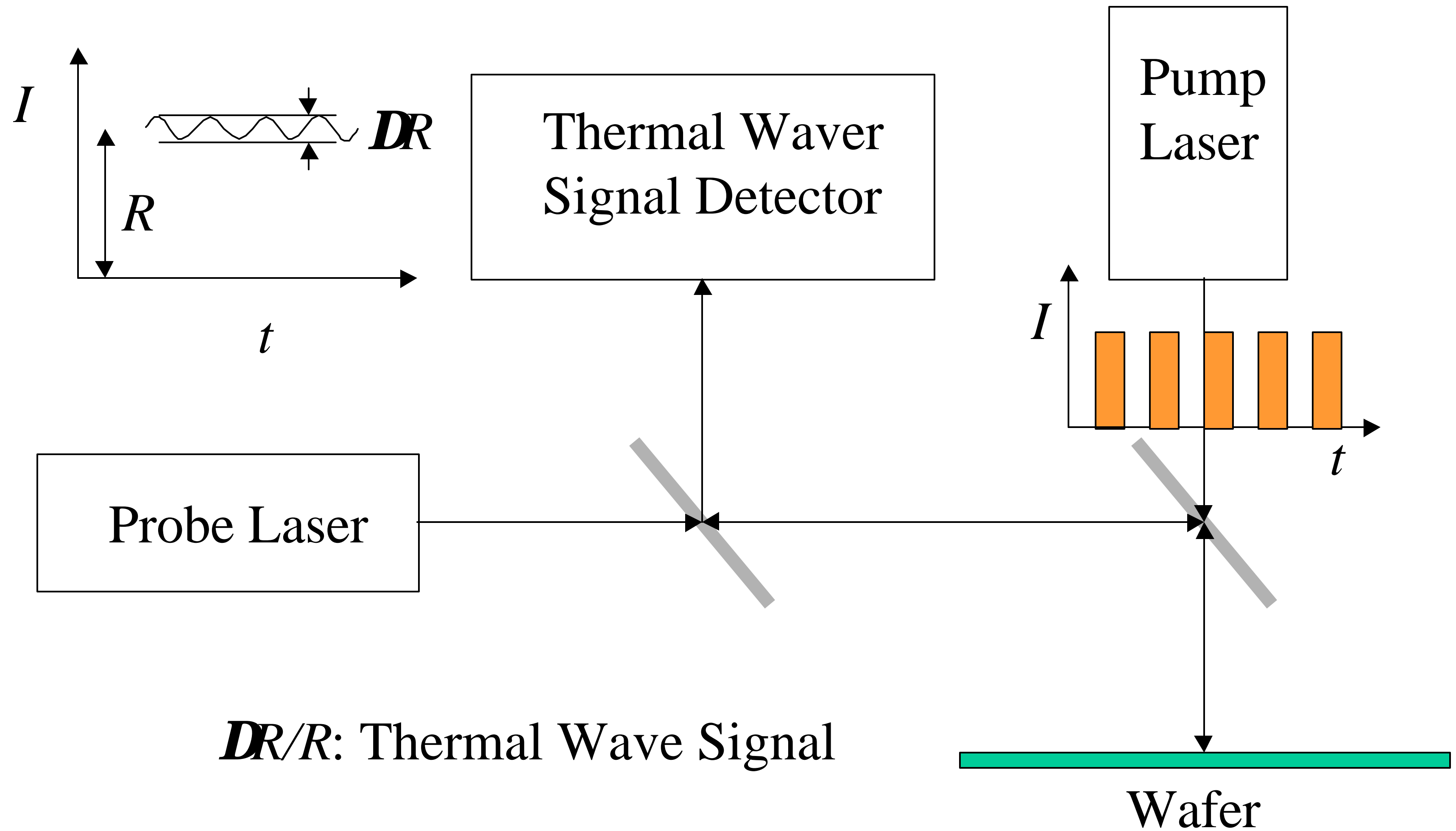


For a typical four-point probe, $S_1 = S_2 = S_3 = 1\text{mm}$,
If current is applied between P_1 and P_4, $R_s = 4.53$ V/I
If current is applied between P_1 and P_3, $R_s = 5.75$ V/I

Thermal Wave System

- Argon “pump” laser generates thermal pulses on wafer surface
- He-Ne probe laser measures DC reflectivity (*R*) and reflectivity modulation induced by the pump laser (***D****R*) at the same spot
- Ratio ***D****R*/*R* is called thermal wave (TW) signal,
  - TW signal ***D****R*/*R* related to the crystal damage
  - crystal damage is a function of the implant dose

Thermal Wave System



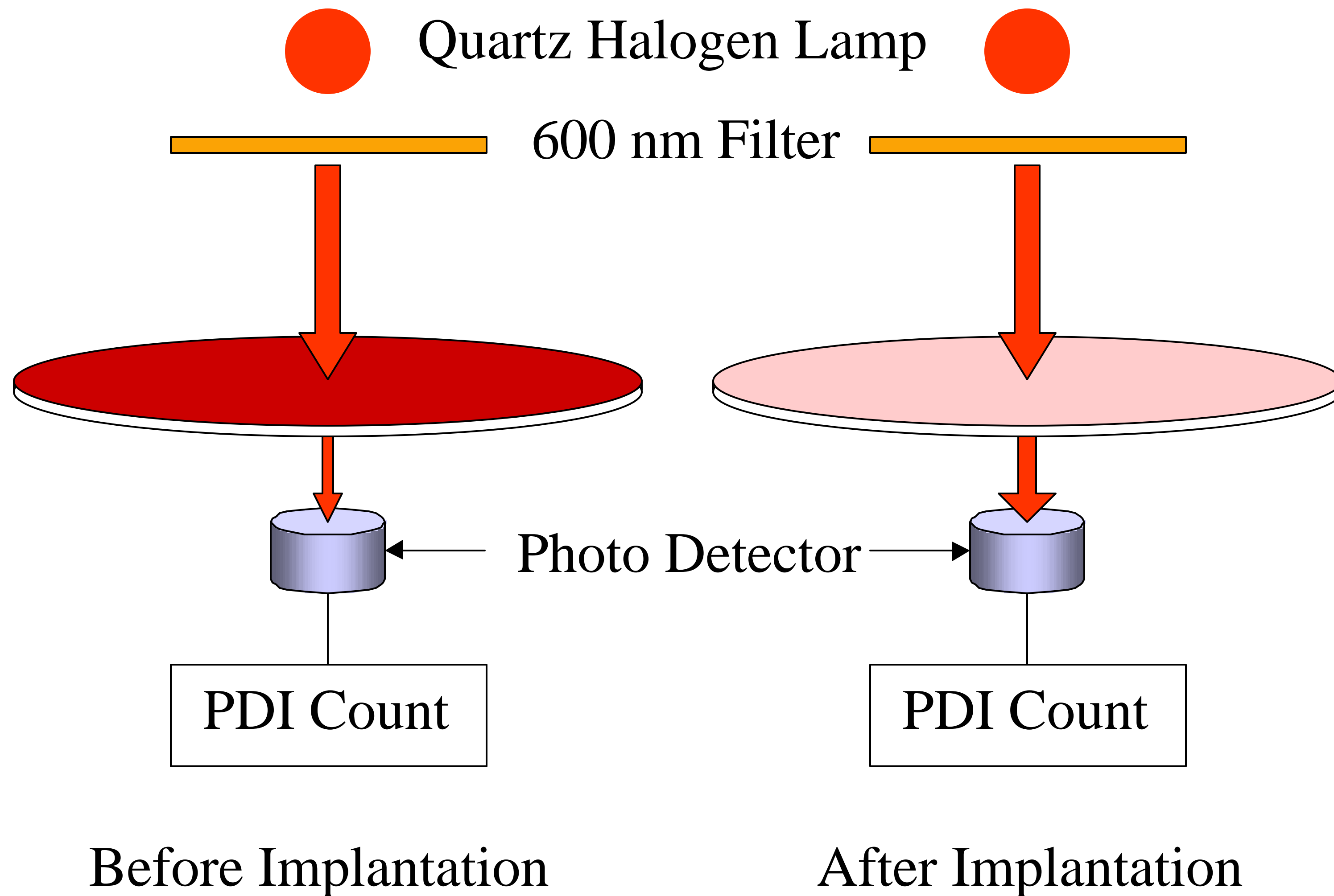
Thermal Wave System

- Performed immediately after the implant process
  - Four-point probe needs anneal first
- Non-destructive, can measure production wafers
  - Four-point probe is only good for test wafers
- Low sensitivity at low dosage
- Drift of the TW signal over time
  - needs to be taken as soon as the implantation finished
- Don't have very high measurement accuracy
  - Laser heating relax crystal damage

Optical Measurement System (OMS)

- transparent wafer coated a with a thin layer of copolymer, which contains energy sensitive dye
- During ion implantation, energetic ions collide with dye molecules and break them down
- Makes the copolymer becomes more transparent
- The higher the dosage, the higher the transparency
- Photon count change before and after implantation
- Determine dosage of certain ion at certain energy

Optical Measurement System (OME)



Ion Implantation: Safety

- One of most hazardous process tools in semiconductor industry
- Chemical
- Electro-magnetic
- Mechanical

Ion Implantation: Chemical Safety

- Most dopant materials are highly toxic, flammable and explosive.
- Poisonous and explosive: AsH_3, PH_3, B_2H_6
- Corrosive: BF_3
- Toxic: P, B, As, Sb
- Common sense: get out first, let the trained people to do the investigation.

Ion Implantation: Electro-magnetic Safety

- High voltage: from facility 208 V to acceleration electrode up to 50 kV.
- Ground strip, Work with buddy!
- Lock & tag
- Magnetic field: pacemaker, etc.

Ion Implantation: Radiation Safety

- High energy ions cause strong X-ray radiation
- Normally well shield

Ion Implantation: Corrosive by-products

- BF_3 as dopant gas
- Fluorine will react with hydrogen to from HF
- Anything in the beamline could have HF
- Double glove needed while wet clean those parts

Ion Implantation: Mechanical Safety

- Moving parts, doors, valves and robots
- Spin wheel
- Hot surface
- ……

Technology Trends

- Ultra shallow junction (USJ)
- Silicon on insulator (SOI)
- Plasma immersion ion implantation (PIII)

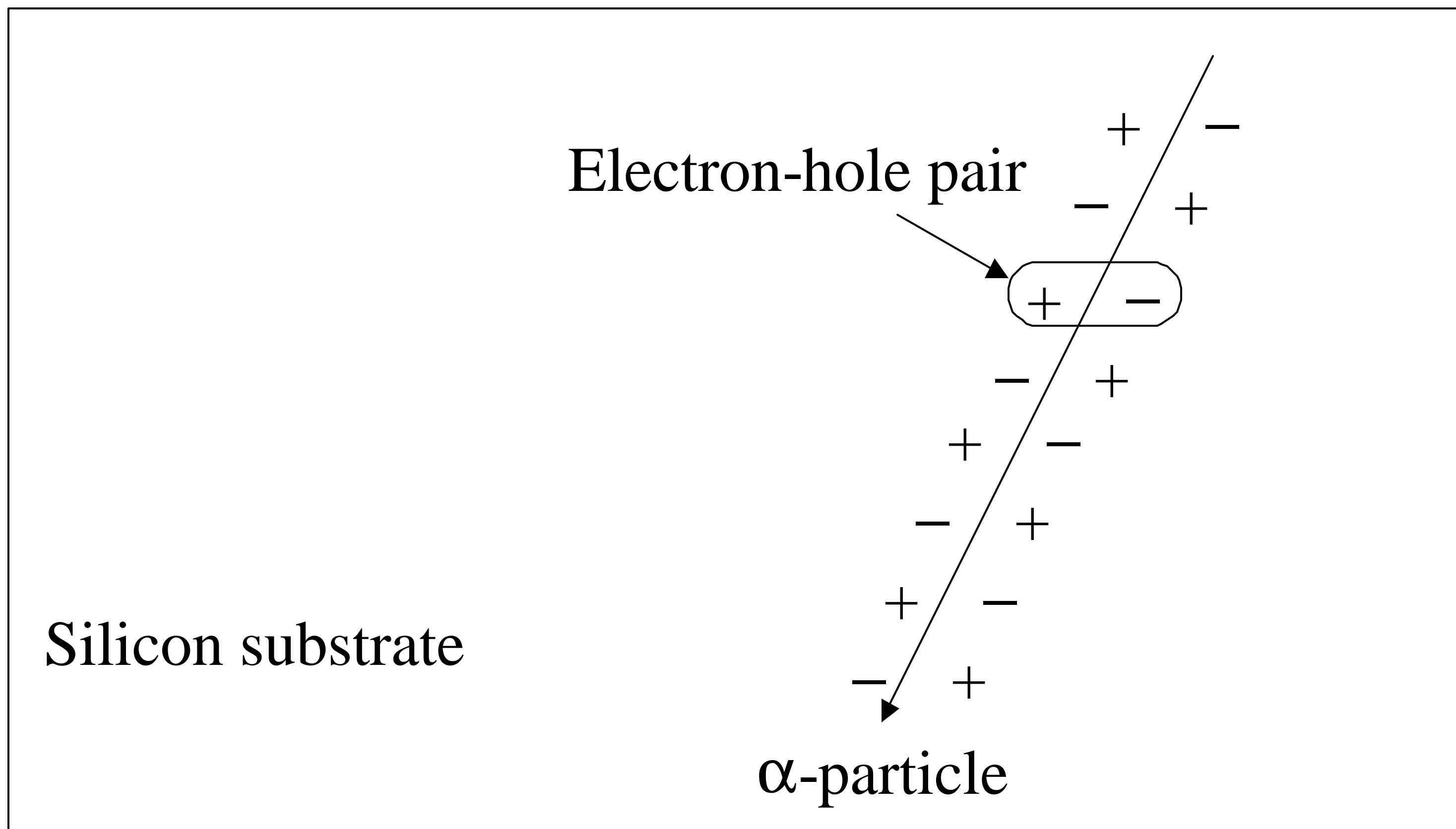
Ultra Shallow Junction (USJ)

- USJ ($x_j \leq 0.05$ μm) for sub-0.1 μm devices
  - p-type junction, boron ion beam at extremely low energy, as low as 0.2 keV
- The requirements for the USJ
  - Shallow
  - Low sheet resistance
  - Low contact resistance
  - Minimal impact on channel profile
  - Compatible with polysilicon gate

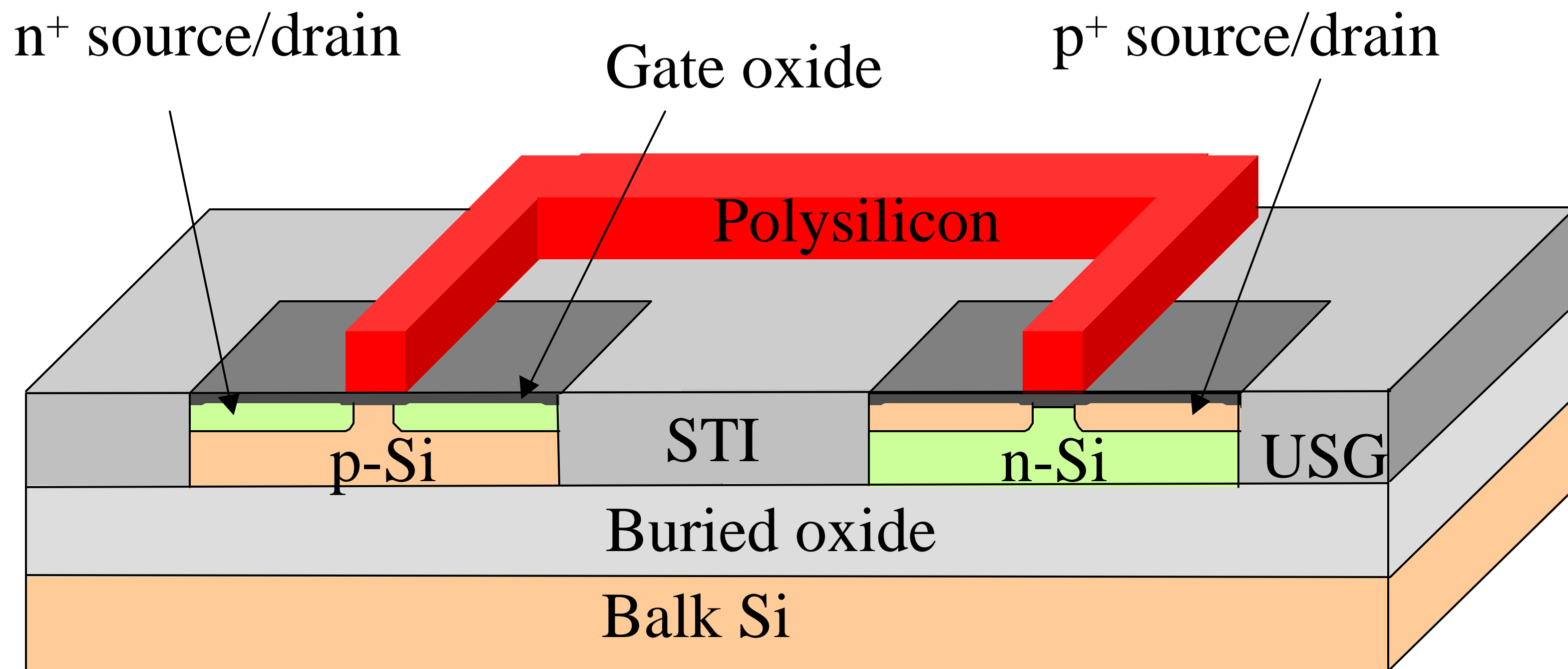
Soft Error

- Electron-hole pairs generated by α-decay
- Electrons from substrate overwrite the messages in memory capacitors
  - Storage capacitors need large capacitance
  - Limit further shrinking device feature size
- Silicon-on-insulator (SOI) complete isolate device from bulk substrate

α-particle Induced Electron-hole Pairs



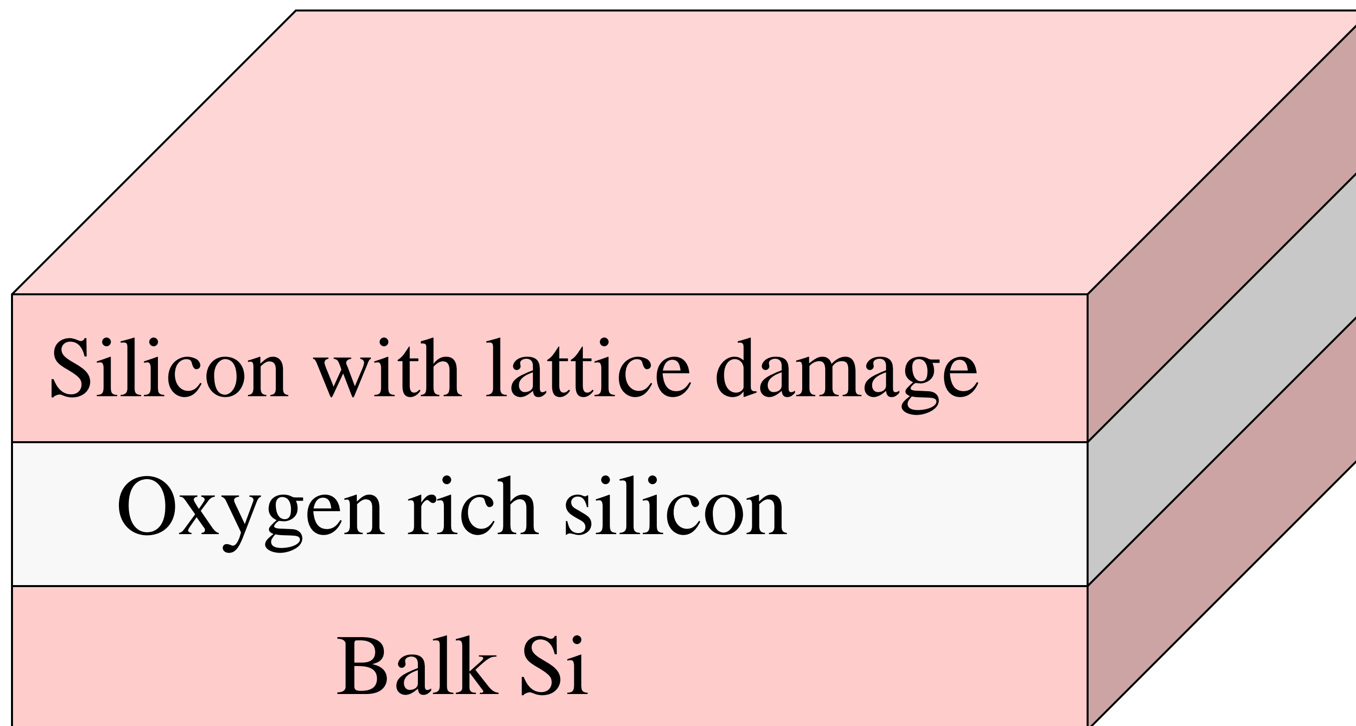
CMOS on SOI Substrate



SOI Formation

- Implanted wafers
  - Heavy oxygen ion implantation
  - High temperature annealing
- Bonded wafers
  - Two wafers
  - Grow oxide on one wafer
  - High temperature bond wafer bonding
  - Polish one wafer until thousand Å away from SiO_2

Oxygen Ion Implantation

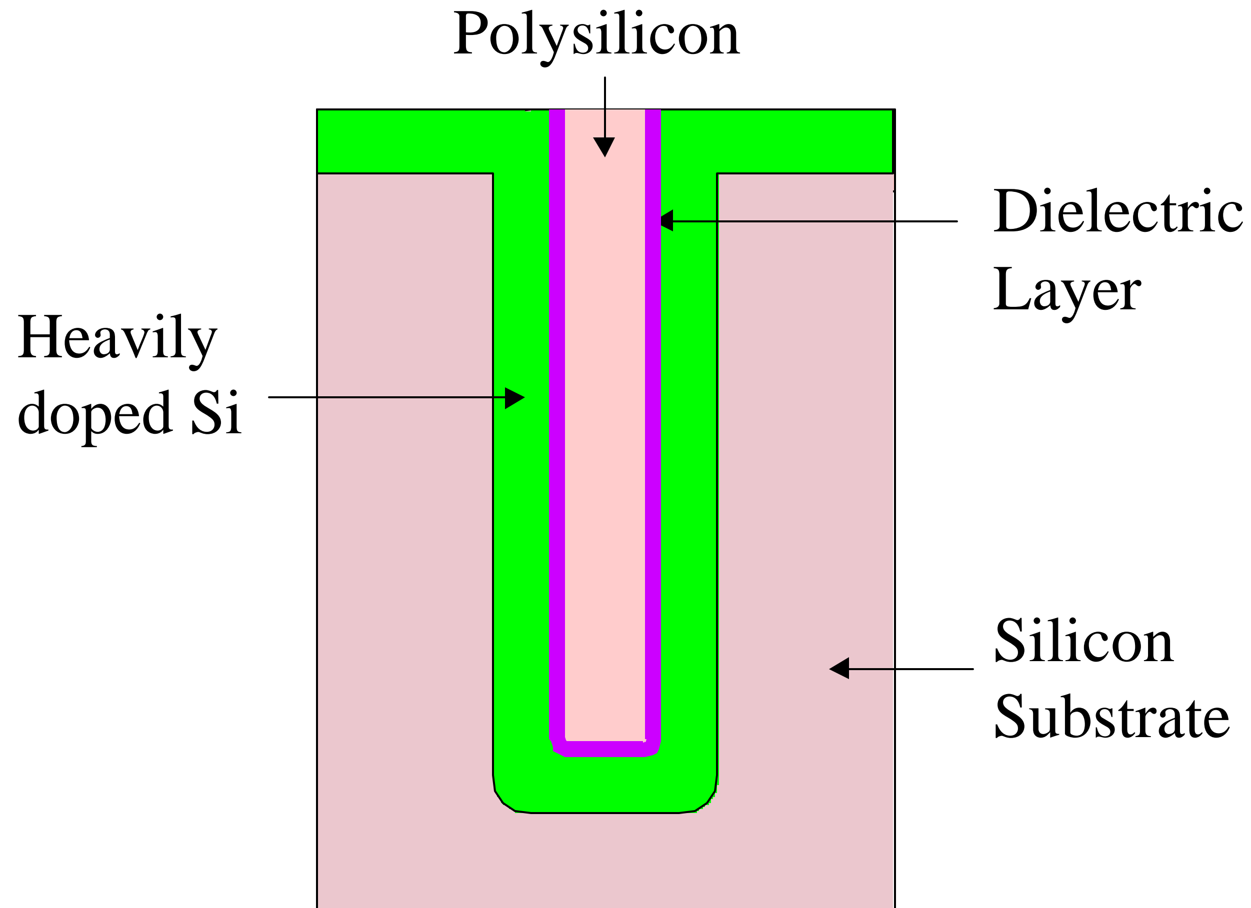


High Temperature Annealing

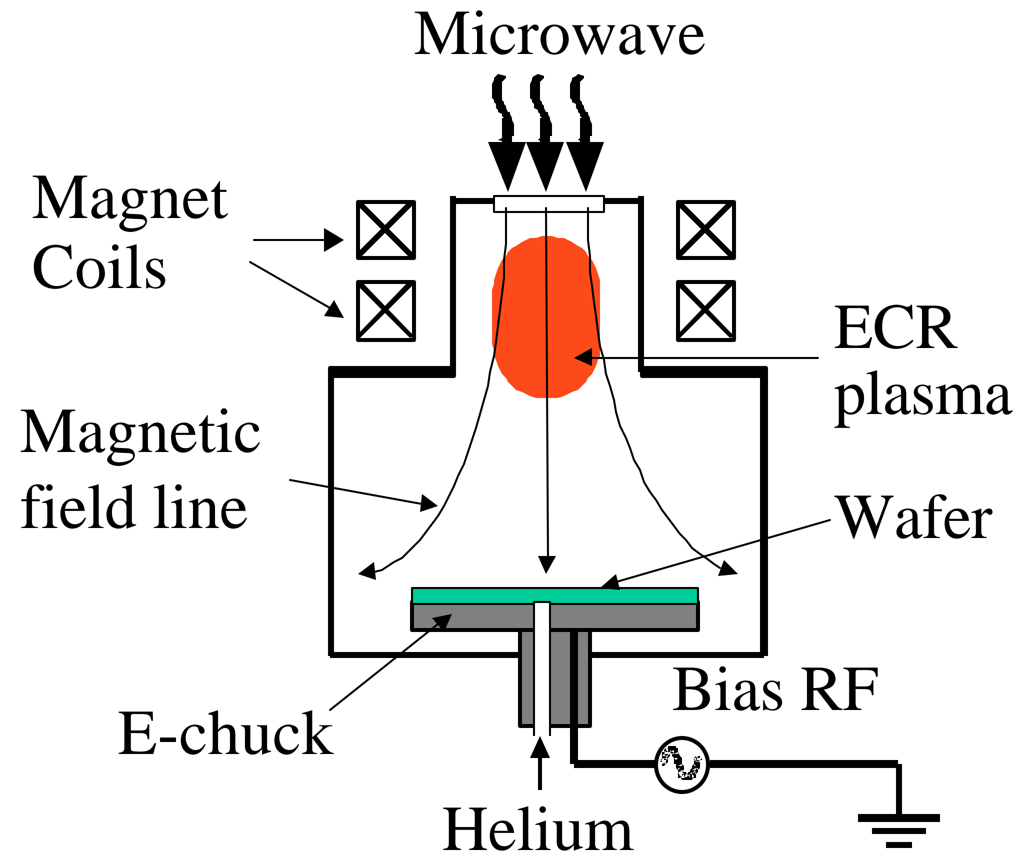
Plasma Immersion Ion Implantation

- Deep trench capacitor for DRAM
- Deeper and narrower
- Very difficult to heavily dope both sidewall and bottom by ion implantation
- Plasma immersion ion implantation (PIII)
- An ion implantation process without precise ion species and ion energy selection

Deep Trench Capacitor



ECR Plasma Immersion System



Summary of Ion Implantation

- Dope semiconductor
- Better doping method than diffusion
- Easy to control junction depth (by ion energy) and dopant concentration (by ion current and implantation time).
- Anisotropic dopant profile.

Summary of Ion Implantation

- Ion source
- Extraction
- Analyzer magnets
- Post acceleration
- Charge neutralization system
- Beam stop

Summary of Ion Implantation

• Well	High energy, low current
• Source/Drain	Low energy, high current
• Vt Adjust	Low energy, low current
• LDD	Low energy, low current

Chapter 9, Etch

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Objectives

Upon finishing this course, you should able to:

- Familiar with etch terminology
- Compare wet and dry etch processes
- List four materials need to be etched during IC processing and list the main dry etch etchants
- Describe etch process in IC fabrication
- Become aware of hazards in etch processes

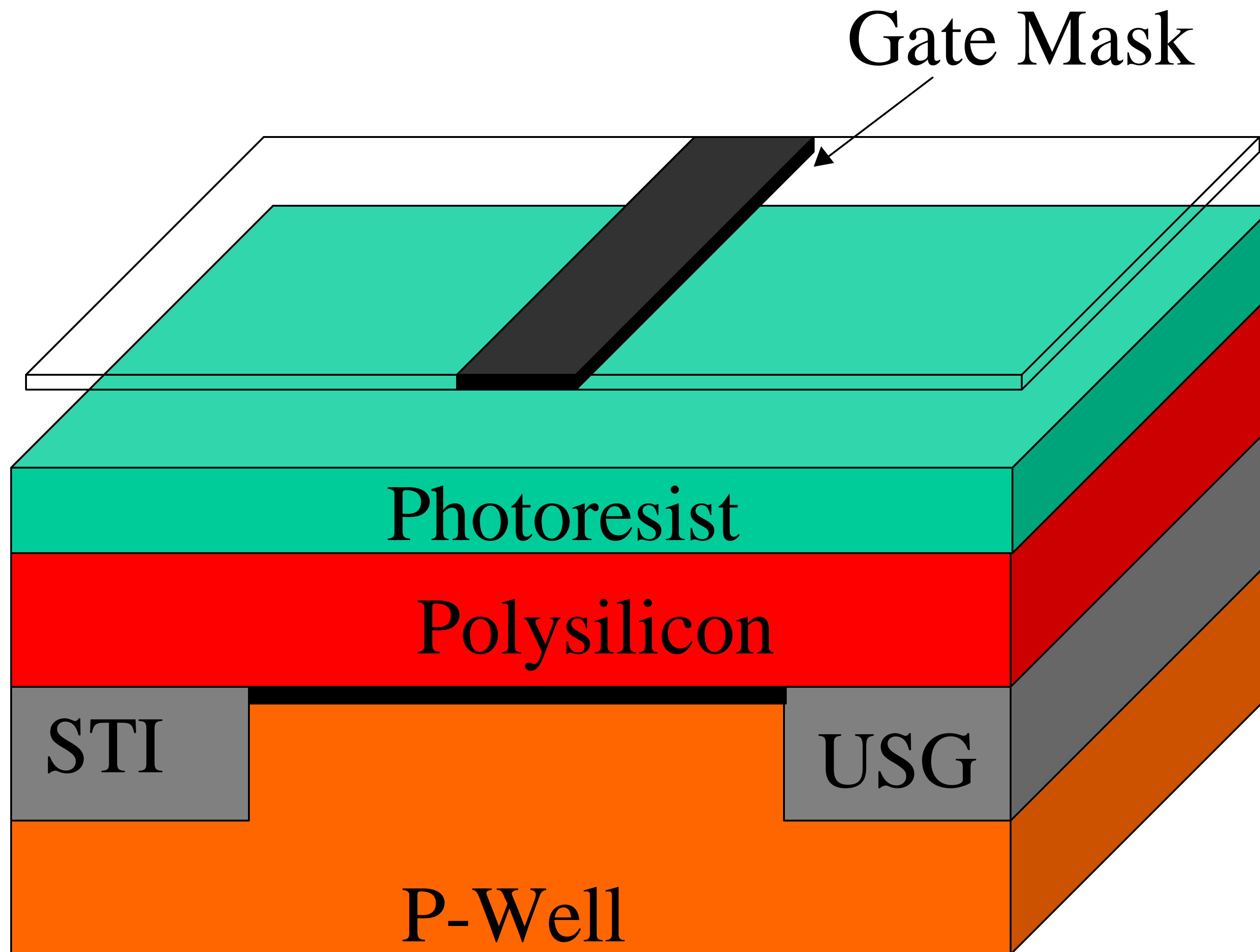
Outline

- Introduction
- Terminology
- Wet and dry etch
- Plasma basics
- Plasma etch processes

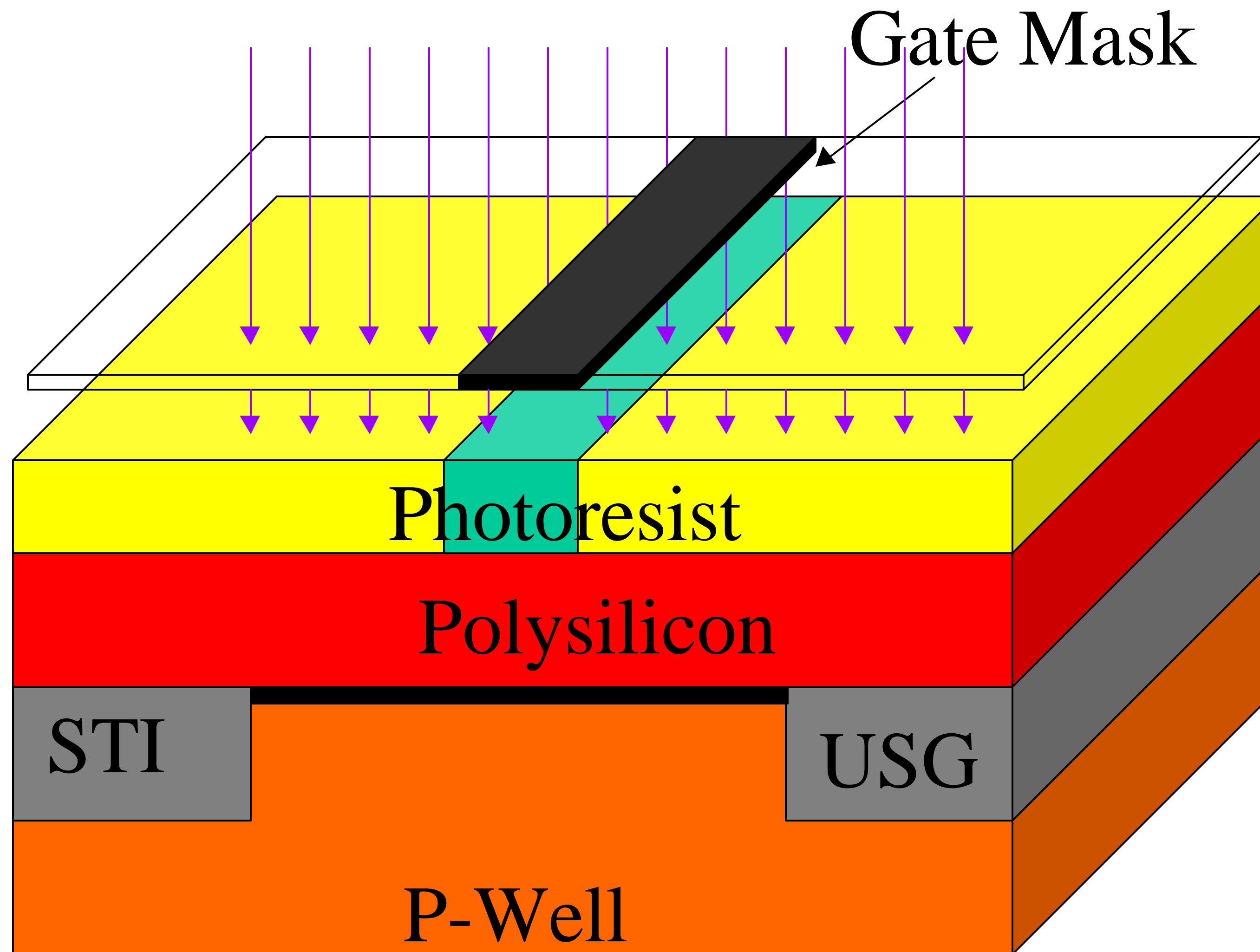
Definition of Etch

- Process that removes material from surface
- Chemical, physical or combination of the two
- Selective or blanket etch
- Selective etch transfers IC design image on the photoresist to the surface layer on wafer
- Other applications: Mask making, Printed electronic board, Artwork, etc.

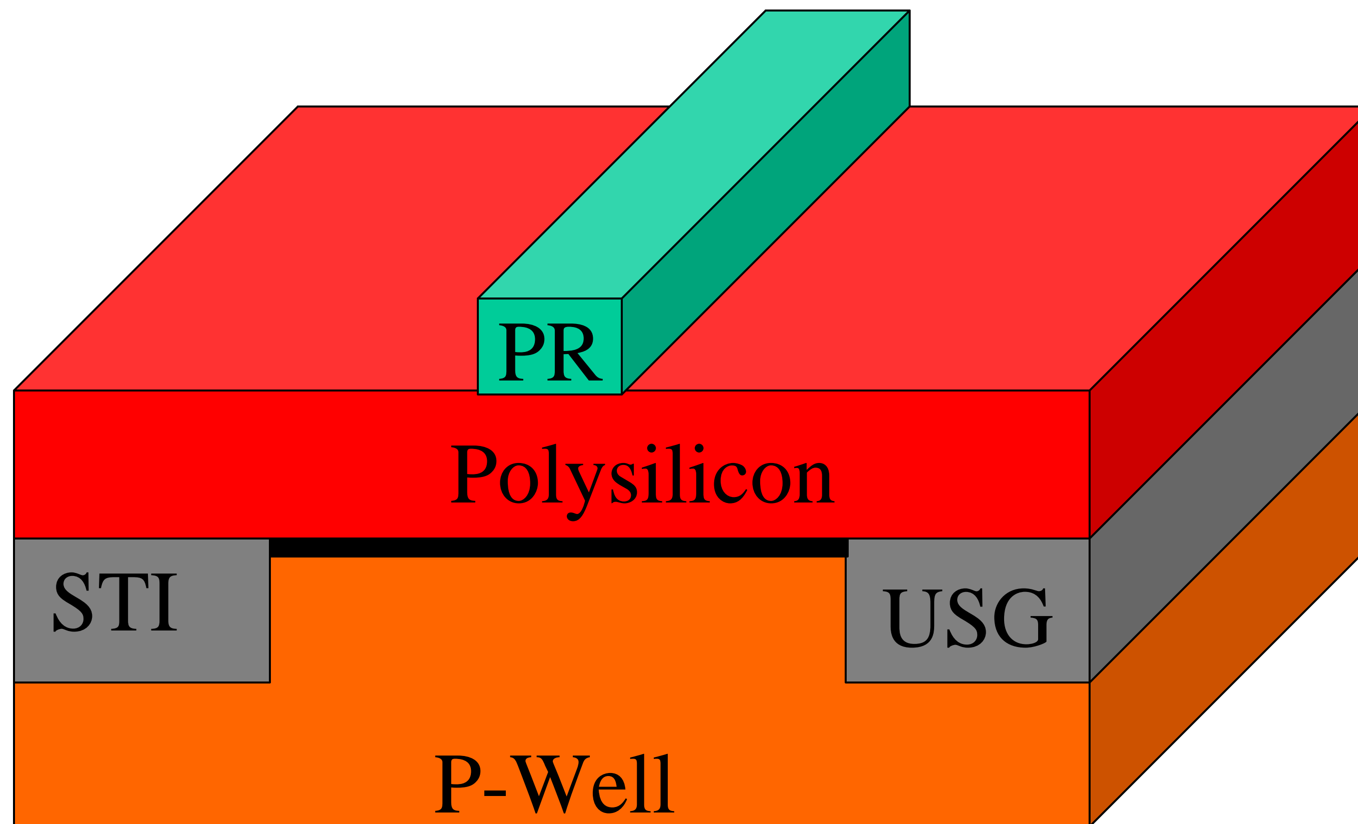
Gate Mask Alignment



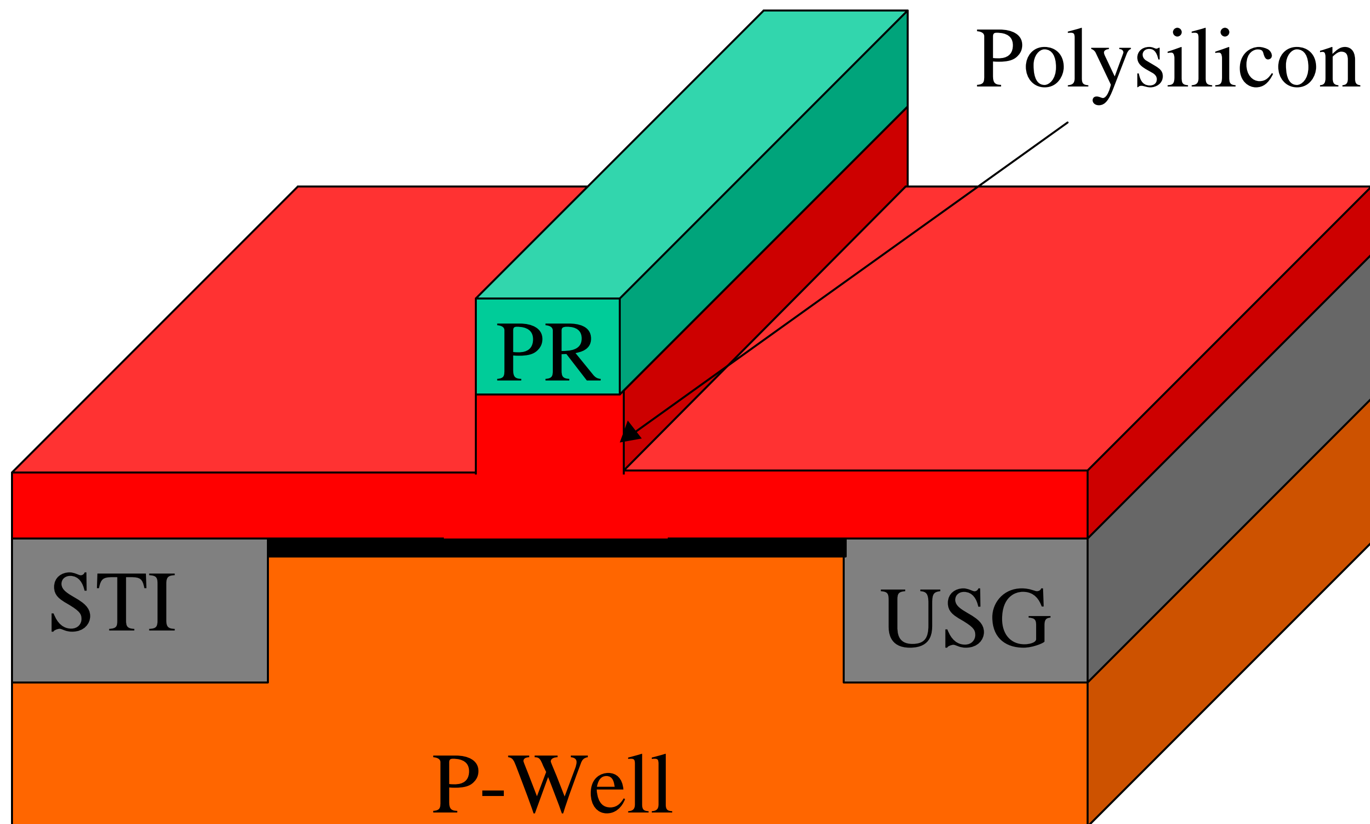
Gate Mask Exposure



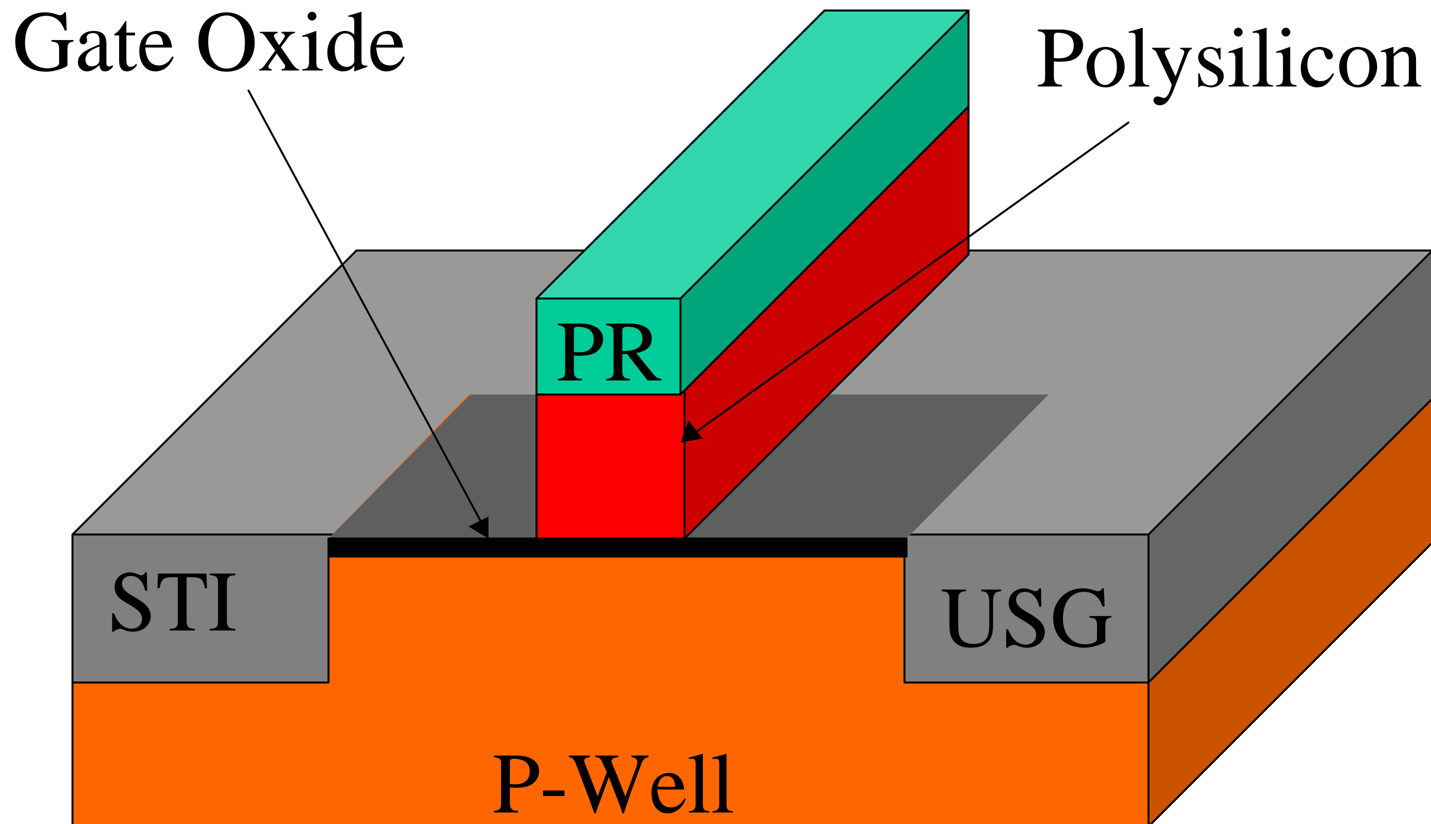
Development/Hard Bake/Inspection



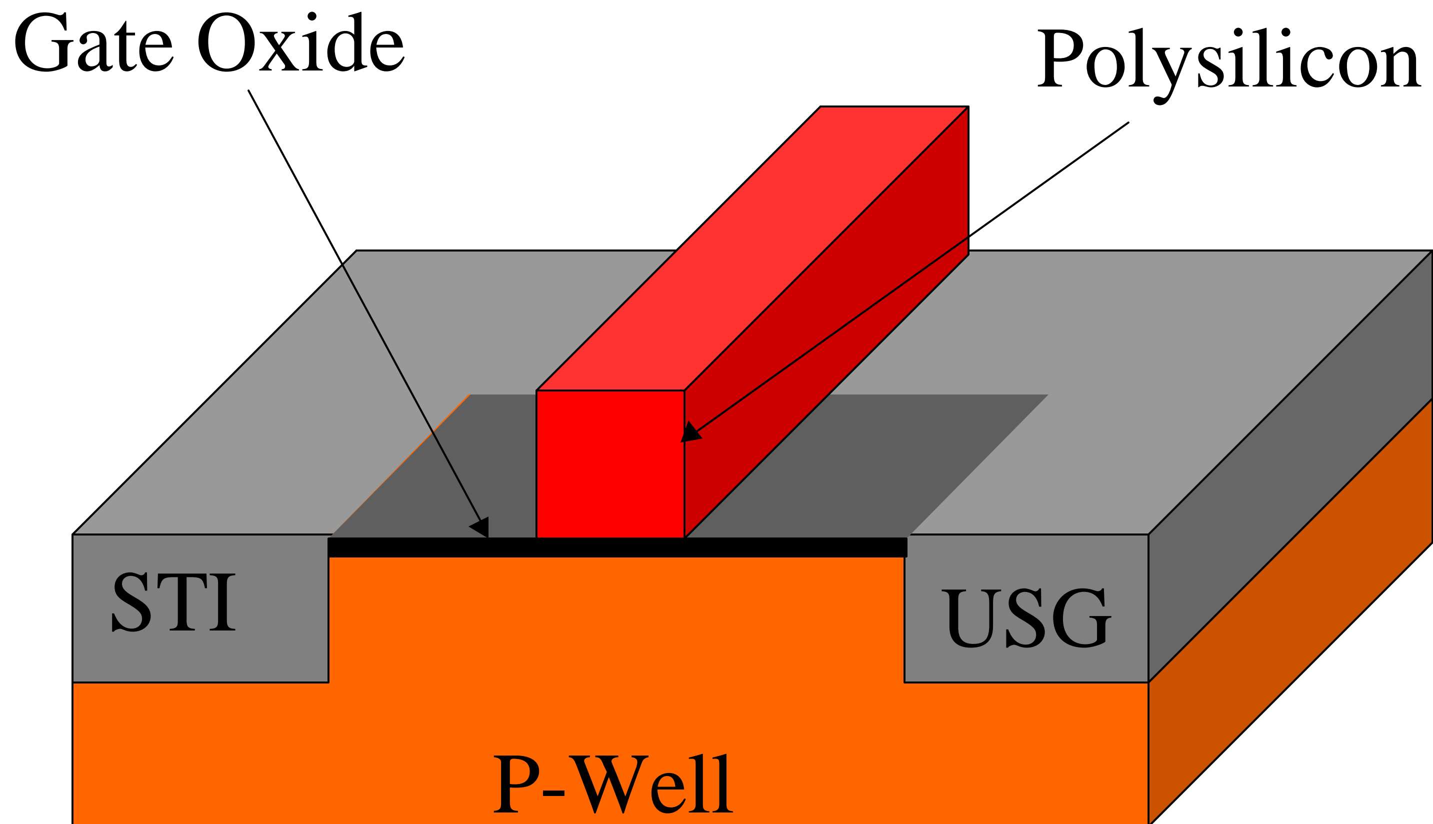
Etch Polysilicon



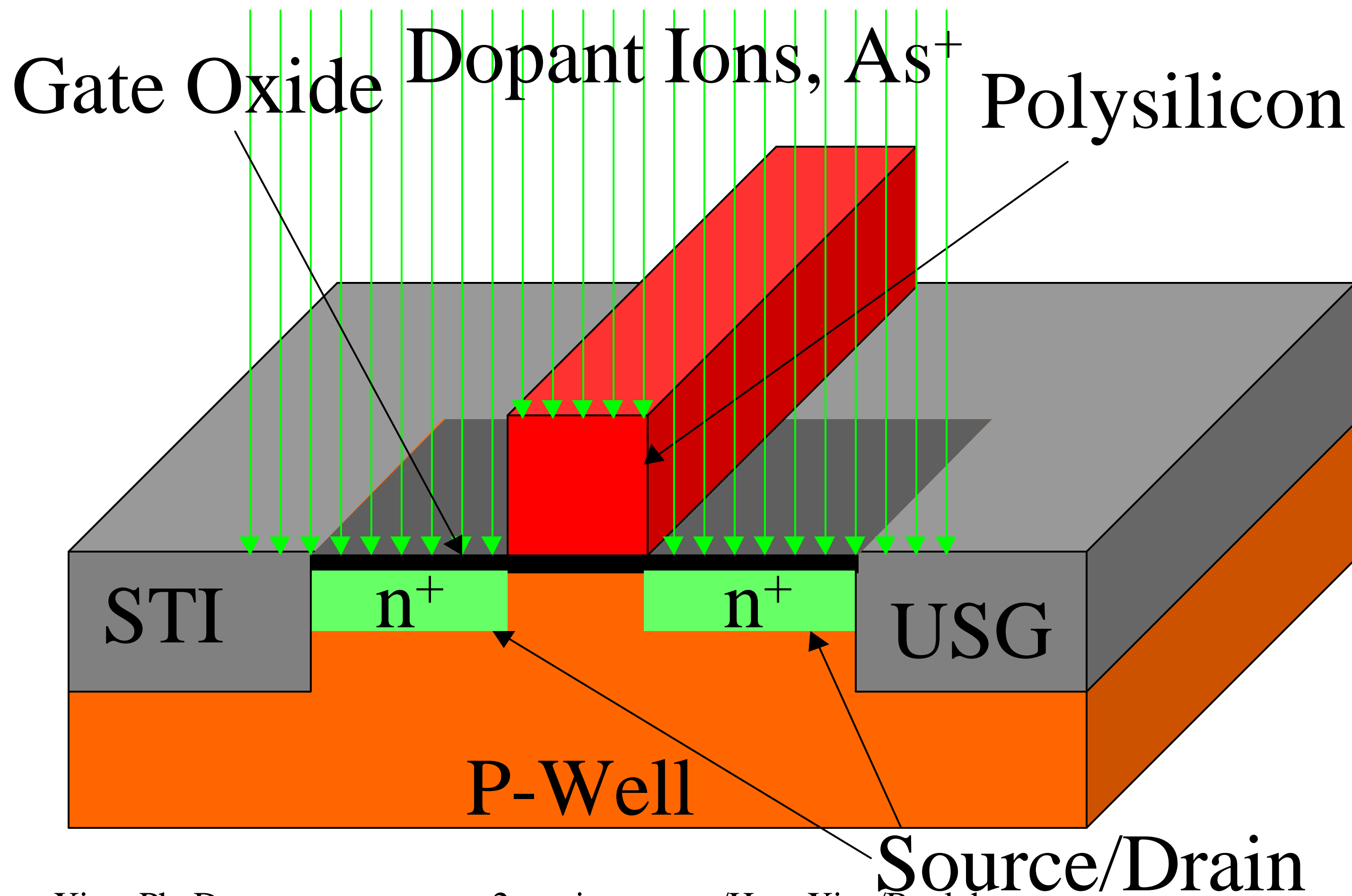
Etch Polysilicon, Continue



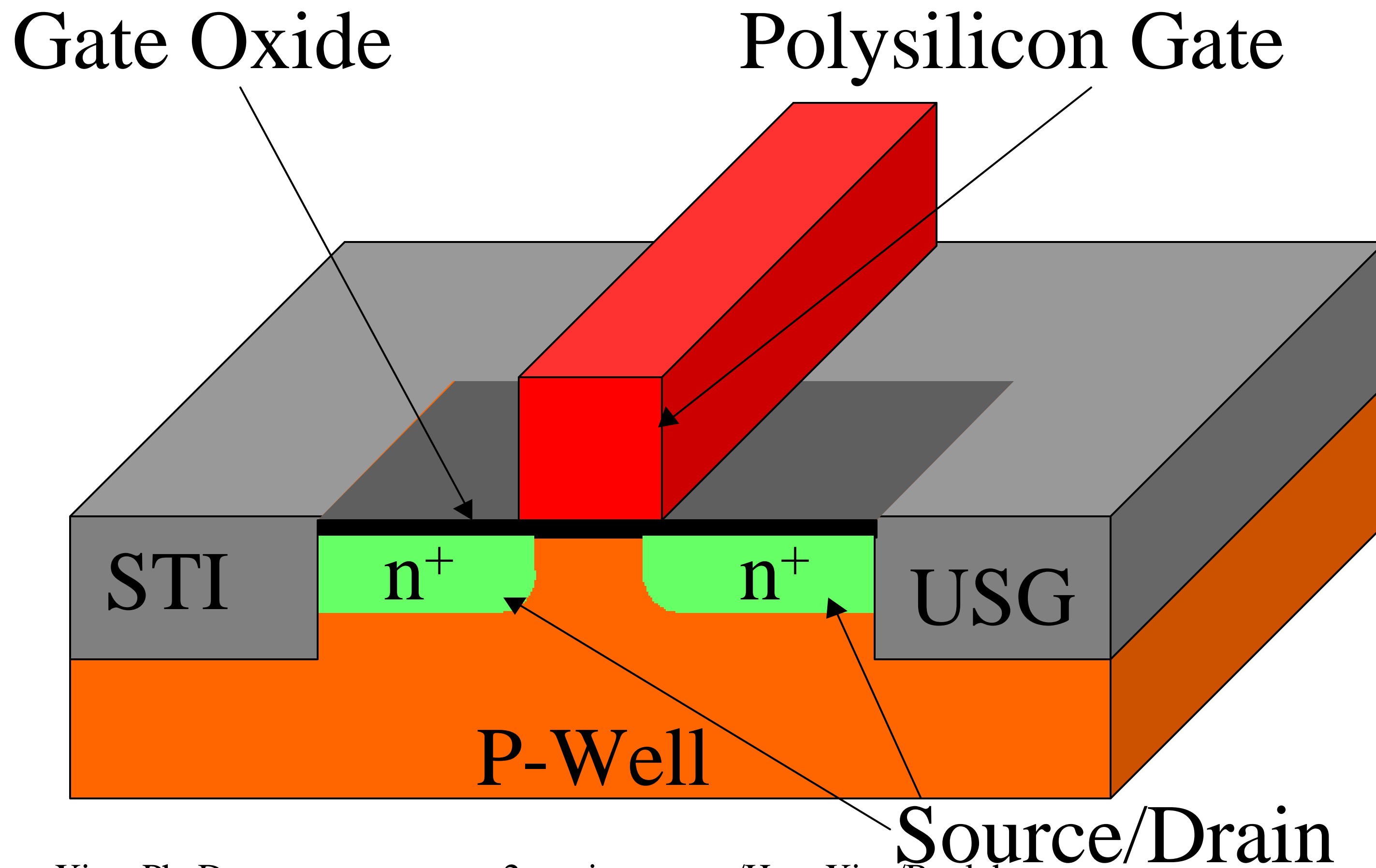
Strip Photoresist



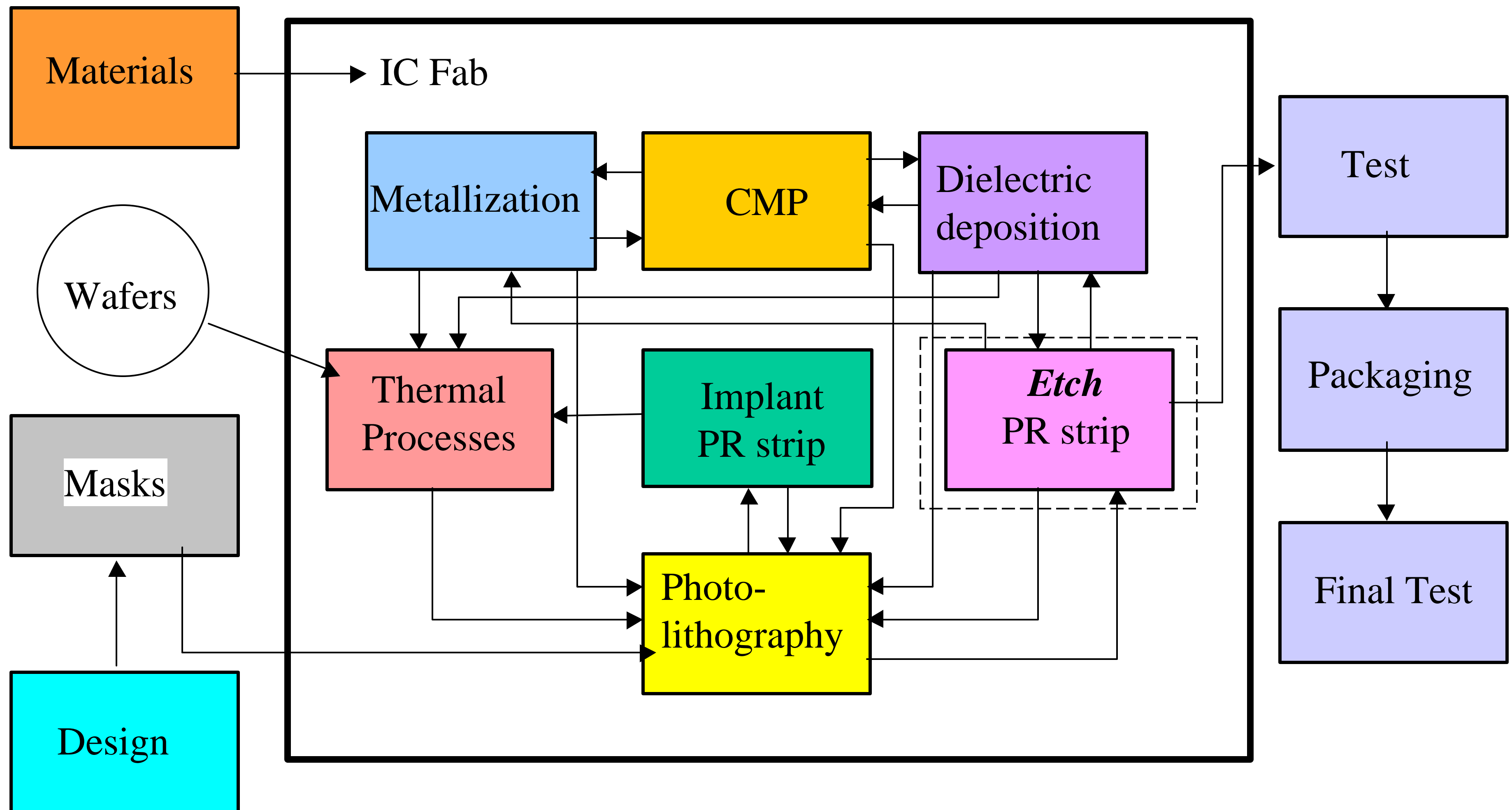
Ion Implantation



Rapid Thermal Annealing



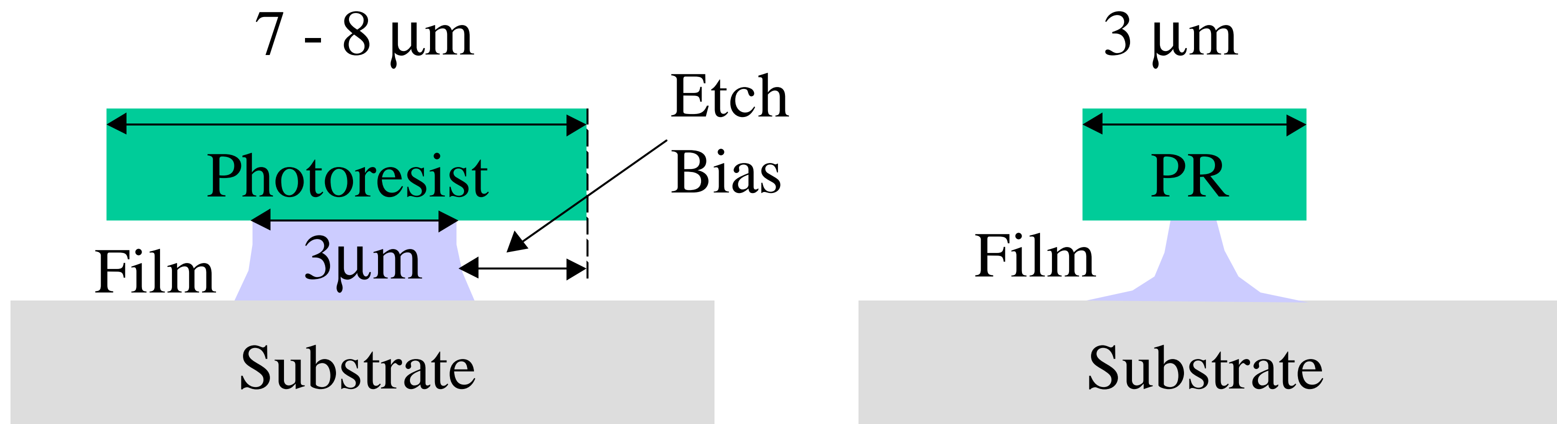
Wafer Process Flow



Applications of Etch

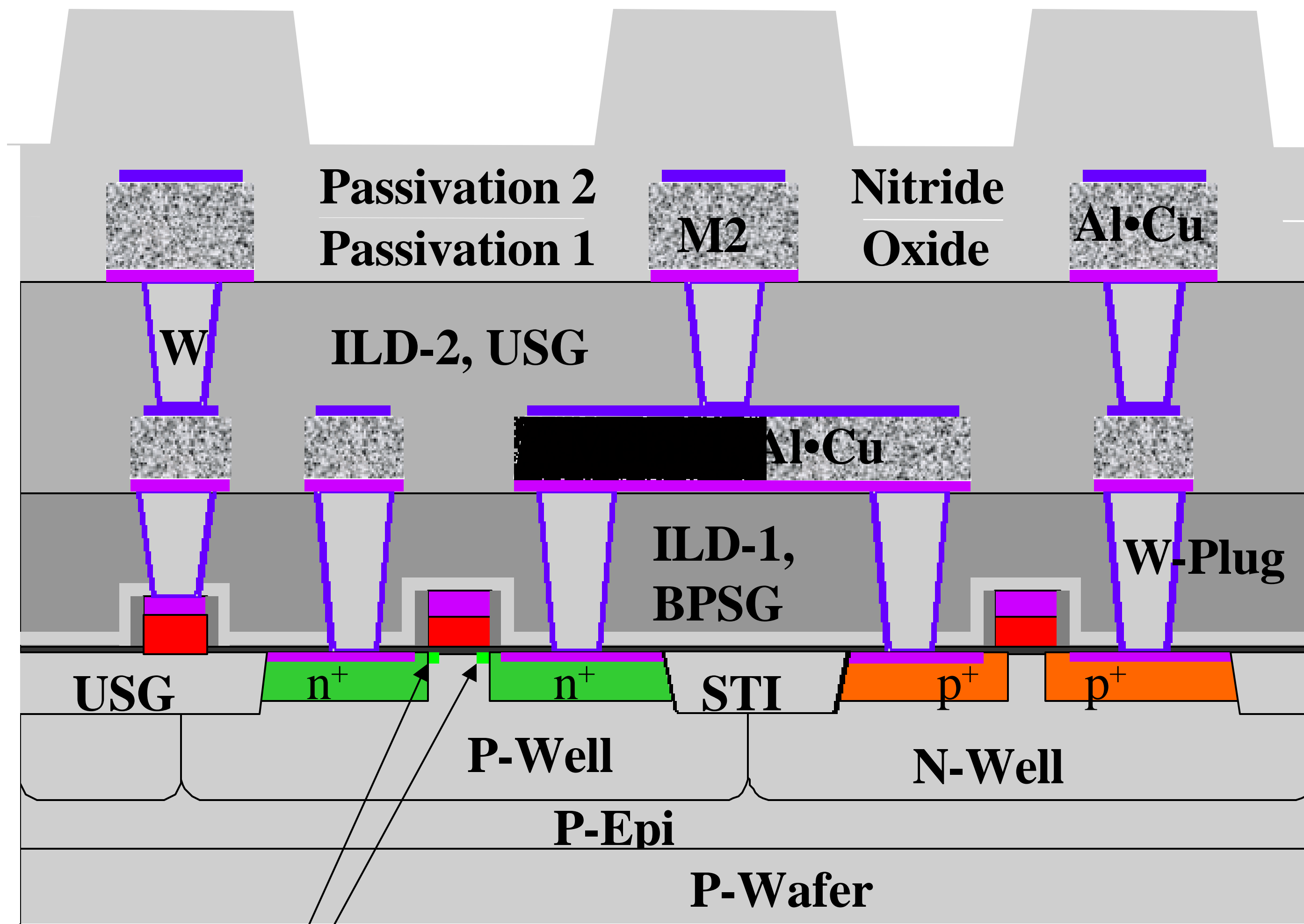
- IC Fabrication
- Mask making
- Printed electronic board
- Art work
- Nameplate
- Glassware

Wet Etch Profiles



- Can't be used for feature size is smaller than 3 μm
- Replaced by plasma etch for all patterned etch

CMOS Cross-Section

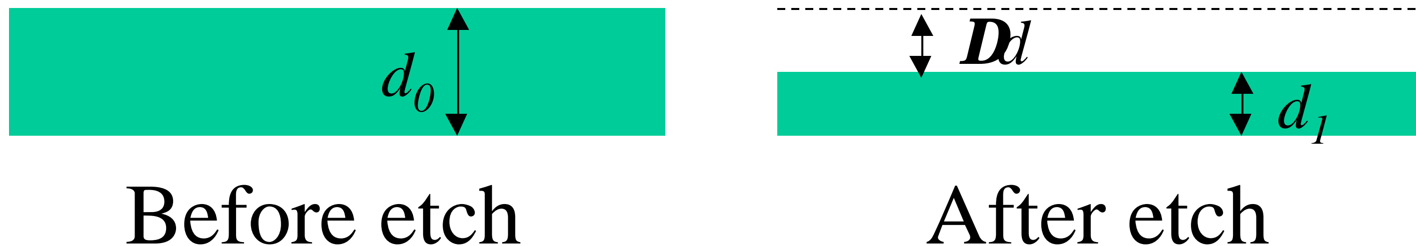


Etch Terminology

- Etch rate
- Selectivity
- Etch uniformity
- Etch profile
- Wet etch
- Dry etch
- RIE
- Endpoint

Etch Rate

Etch rate measures of the how fast the material is removed from wafer surface.



$$\text{Etch Rate} = \frac{\boldsymbol{D}d}{t} \quad (\text{Å/min})$$

$\boldsymbol{D}d = d_0 - d_1$ (Å) is thickness change and t is etch time (min)

Etch Rate

$$\text{Etch rate} = \frac{\text{thickness change after etch}}{\text{etch time}}$$

PE-TEOS PSG film, 1 minute in 6:1 BOE at 22 °C,

Before etch, t = 1.7 μm, After wet etch, t = 1.1 μm

$$ER = \frac{17000-11000}{1} = 6000 \text{ Å/min}$$

Etch Uniformity

- Etch uniformity is a measure of the process repeatability within the wafer (WIW) and wafer to wafer (WTW)
- Thickness measurements are made before and after etch at different points
- More measure points, higher the accuracy
- Standard deviation definition are normally used
- Different definitions give different results

Standard Deviation Non-uniformity

N points measurements

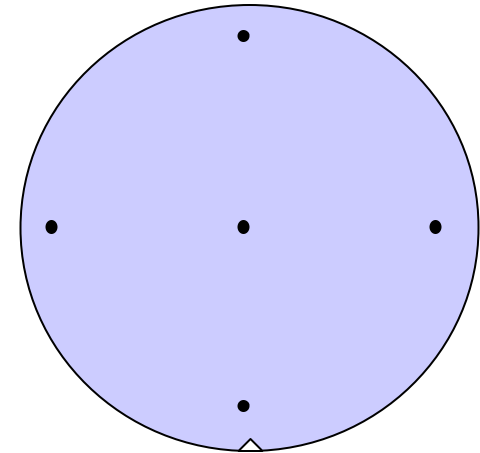
$$\sigma = \sqrt{\frac{(x_1 - \overline{x})^2 + (x_2 - \overline{x})^2 + (x_3 - \overline{x})^2 + \cdots + (x_N - \overline{x})^2}{N-1}}$$

$$\overline{x} = \frac{x_1 + x_2 + x_3 + \cdots + x_N}{N}$$

Max-Min Uniformity

Etch non-uniformity (NU) can be calculated by using following equation (called Max-Min uniformity, good for classroom exercise):

$$NU(\%) = (E_{max} - E_{min})/ 2E_{ave}$$



E_{max} = Maximum etch rate measured

E_{min} = Minimum etch rate measured

E_{ave} = Average etch rate

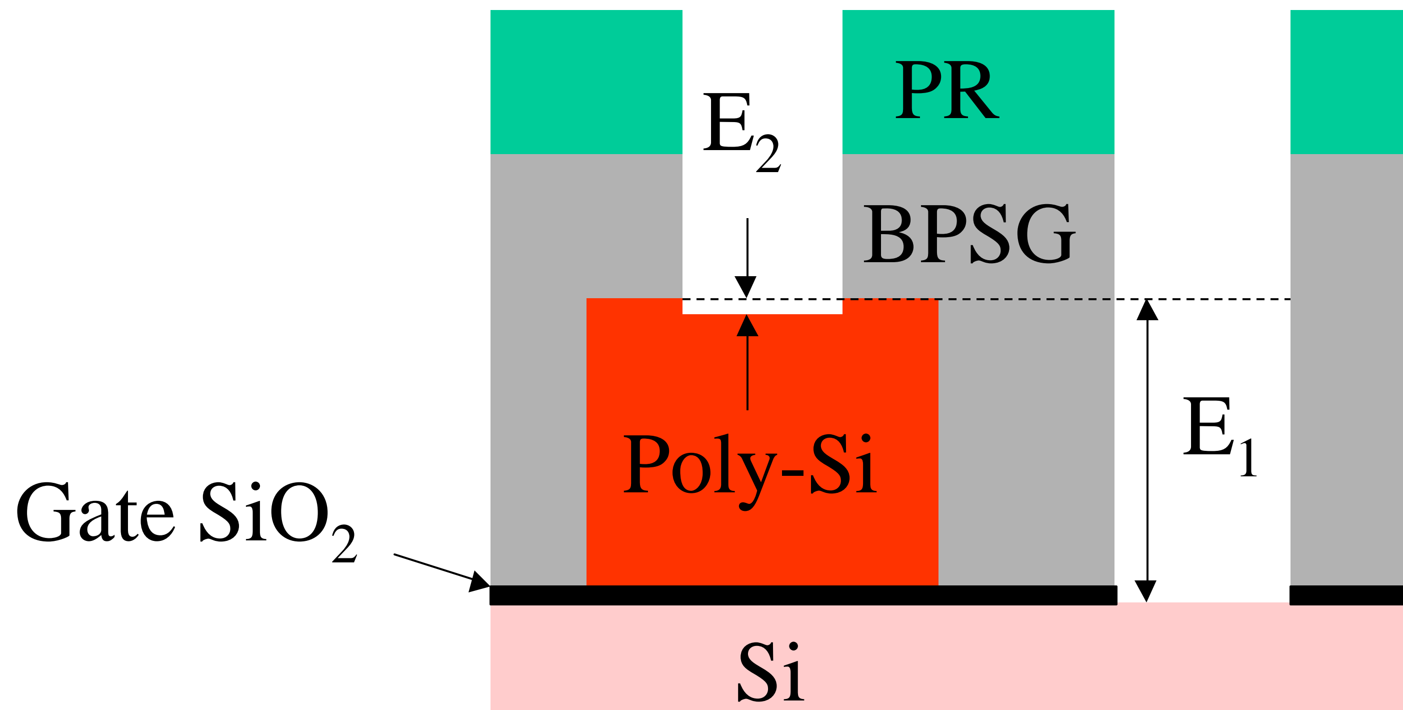
Selectivity

- Selectivity is the ratio of etch rates of different materials.
- Very important in patterned etch
- Selectivity to underneath layer and to photoresist

$$S = \frac{E_1}{E_2}$$

Selectivity

- Selectivity of BPSG to Poly-Si: $S = \dfrac{E_1}{E_2}$



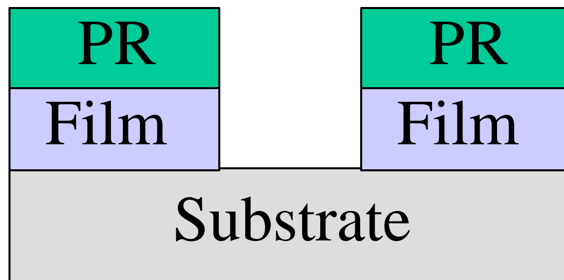
Selectivity

$$\text{Selectivity} = \frac{\text{Etch rate 1}}{\text{Etch rate 2}}$$

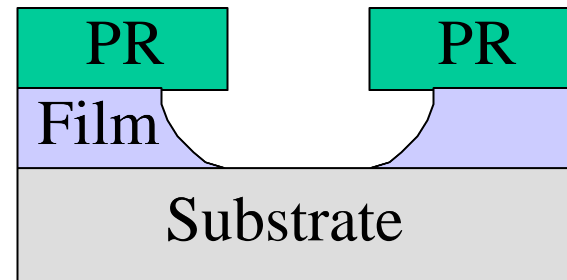
Etch rate for PE-TEOS PSG film is 6000 Å/min, etch rate for silicon is 30 Å/min, PSG to silicon

$$\text{Selectivity} = \frac{6000}{30} = 200:1$$

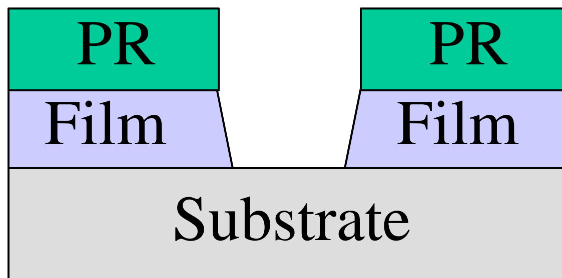
Etch Profiles



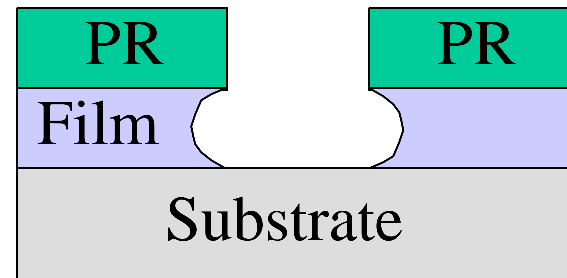
Anisotropic



Isotropic

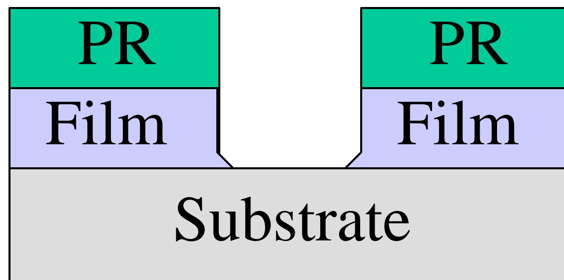


Anisotropic, tapered

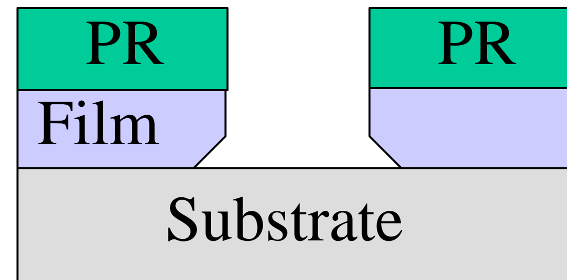


Anisotropic, Undercut

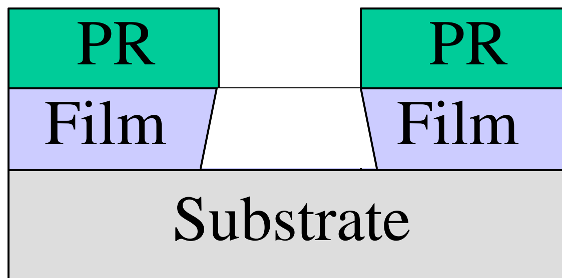
Etch Profiles



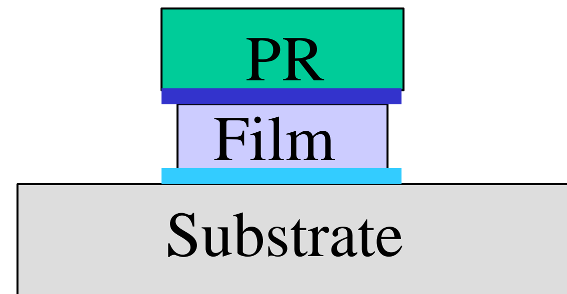
Anisotropic, Foot



Undercut, reversed foot



Undercut, reversed tapered



Undercut, I-beam

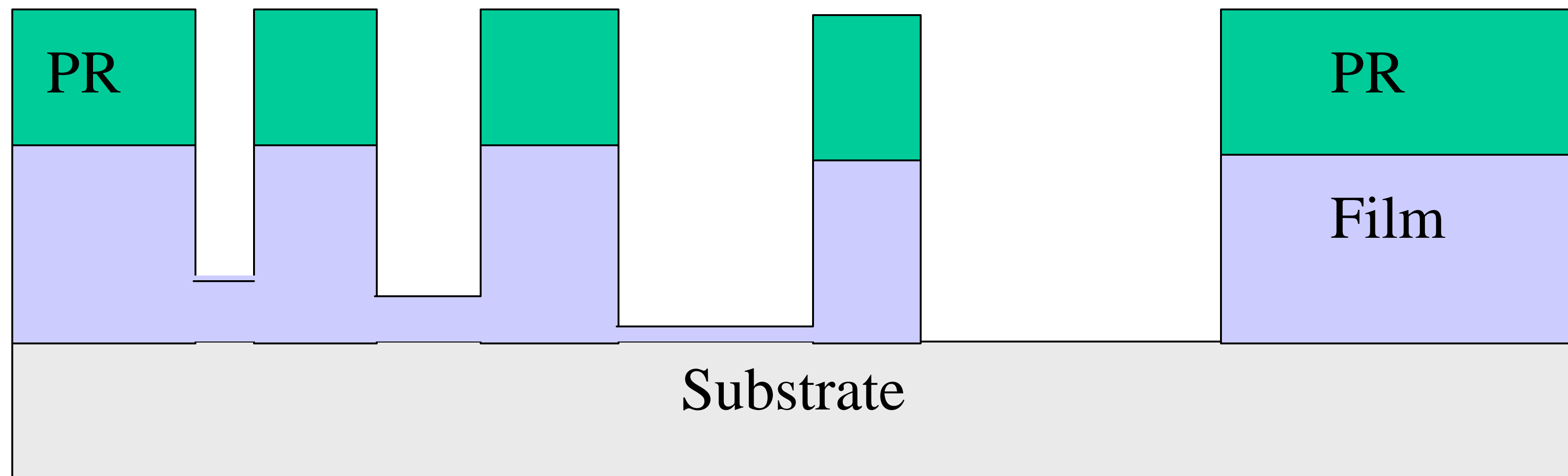
Loading Effects: Macro Loading

- ER of a wafer with a larger open area is different from the wafer with a smaller open area
- Mainly affects the batch etch process,
- Has a minimal effect on the single wafer process

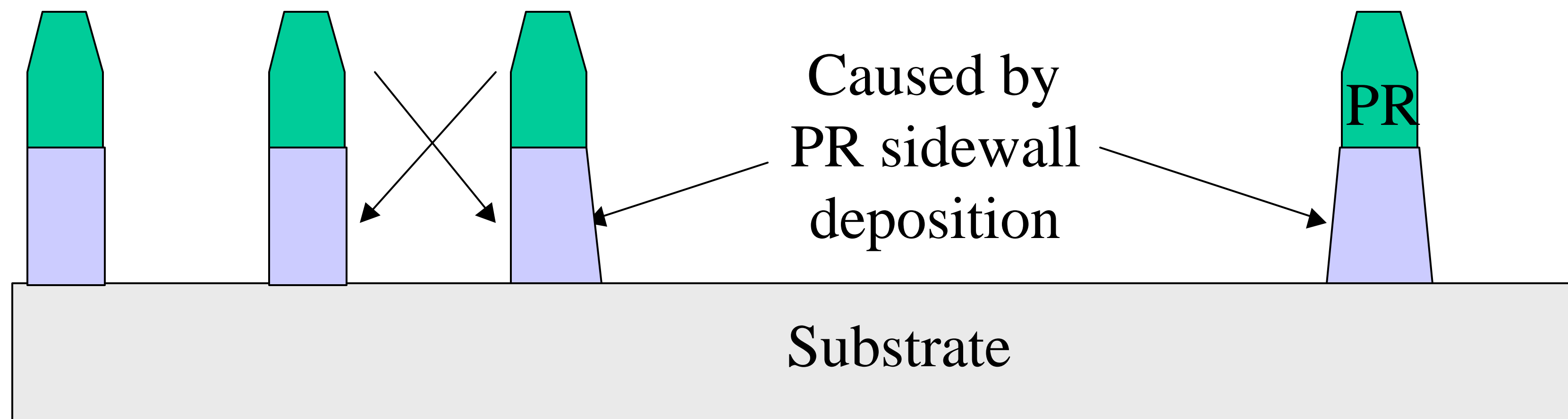
Loading Effects: Micro Loading

- Smaller hole has a lower etch rate than the larger holes
- Etchants are more difficult to pass through the smaller hole
- Etch byproducts are harder to diffuse out
- Lower pressure can minimize the effect.
- Longer MFP, easier for etchants reaching the film and for etch byproducts to get out

Micro Loading



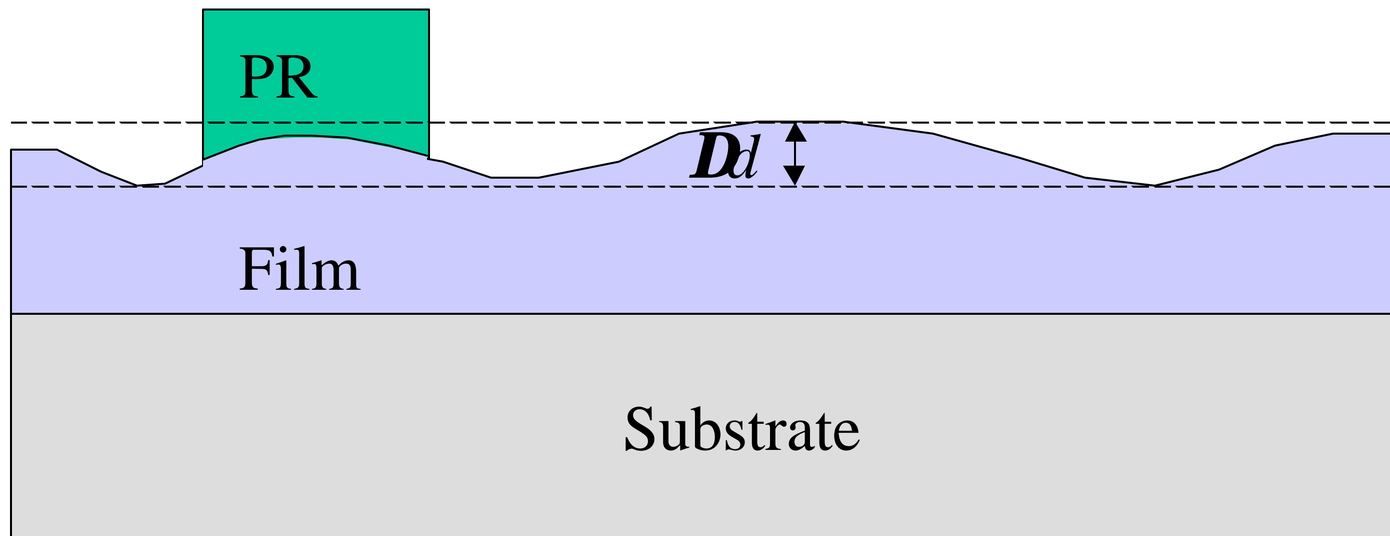
Profile Micro Loading



Over Etch

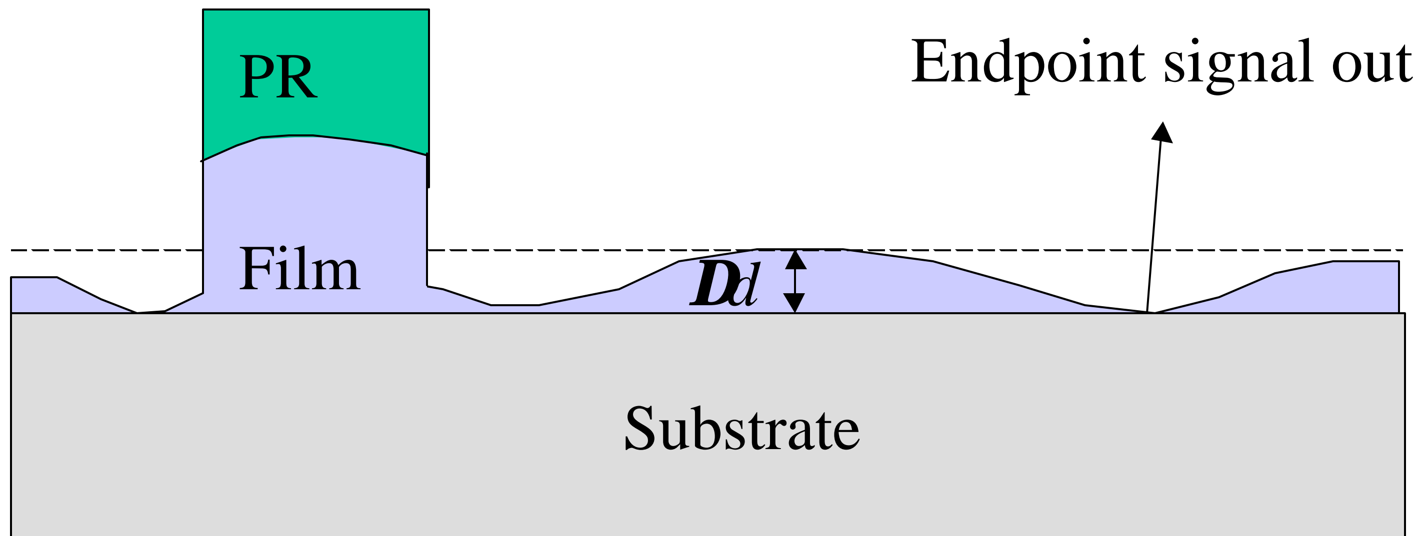
- Film thickness and etch rate is not uniform
- Over etch: removes the leftover film
- Selectivity of etched film and substrate
- RIE uses optical endpoint to switch from main etch to over etch

Start Etch Process



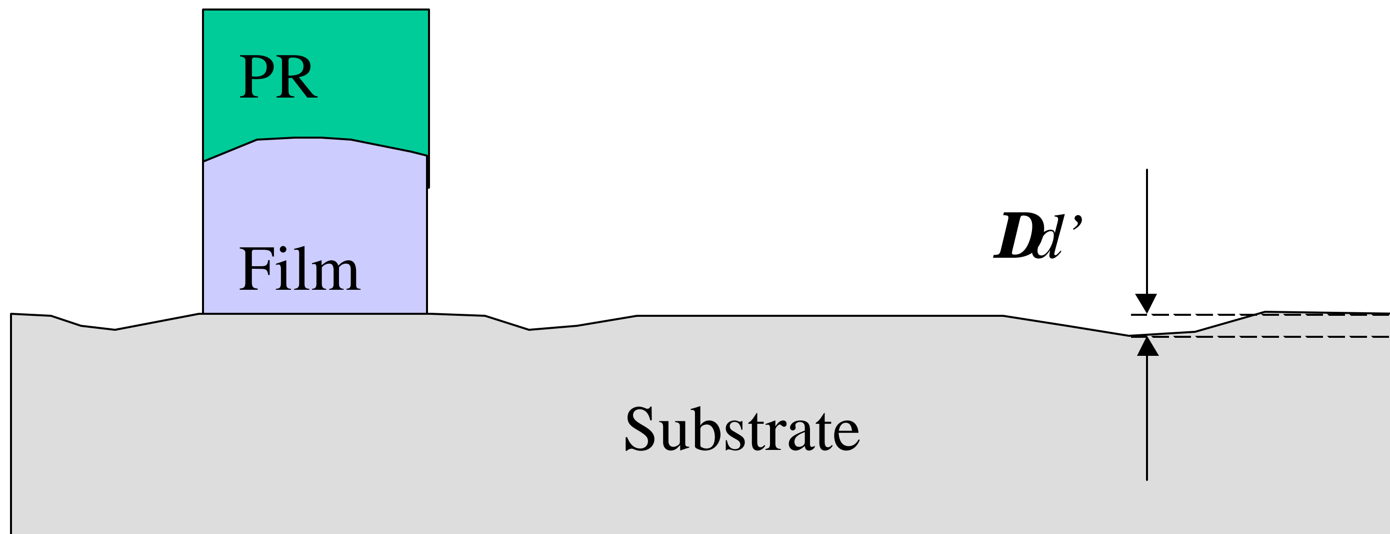
Start main etch

Main Etch Endpoint



Before over etch

After Overetch

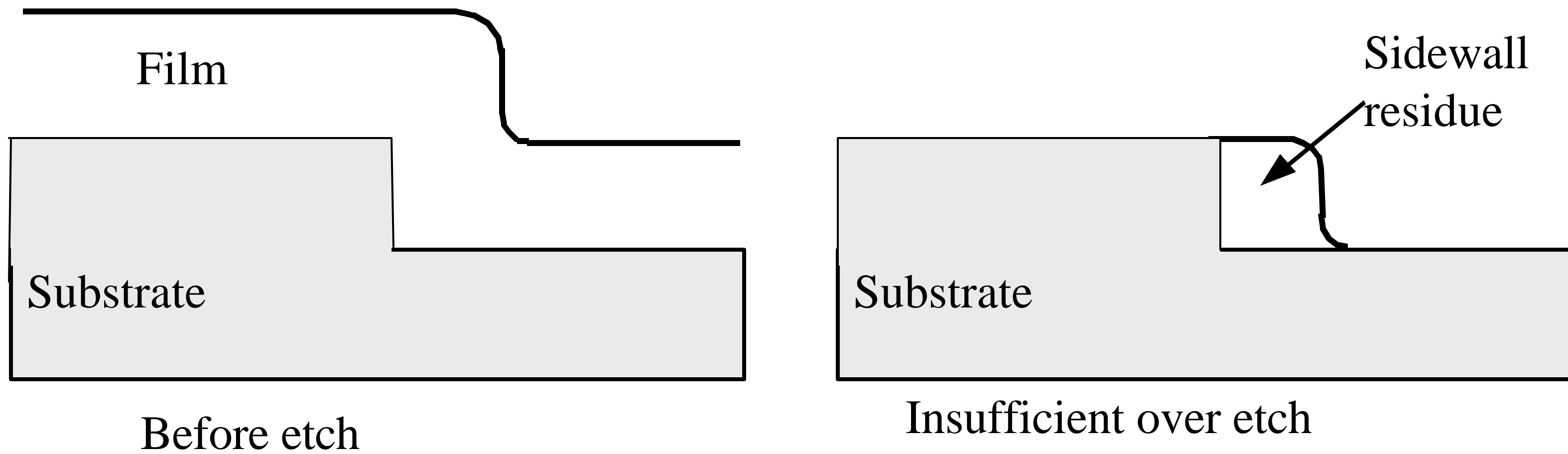


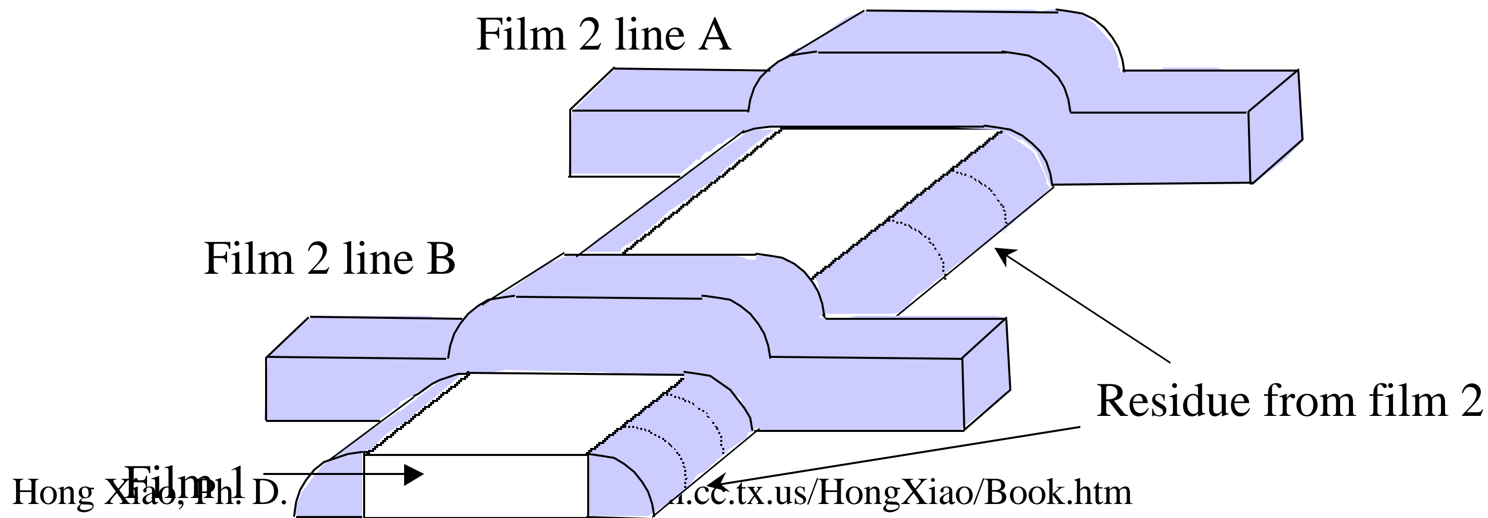
After over etch

Residues

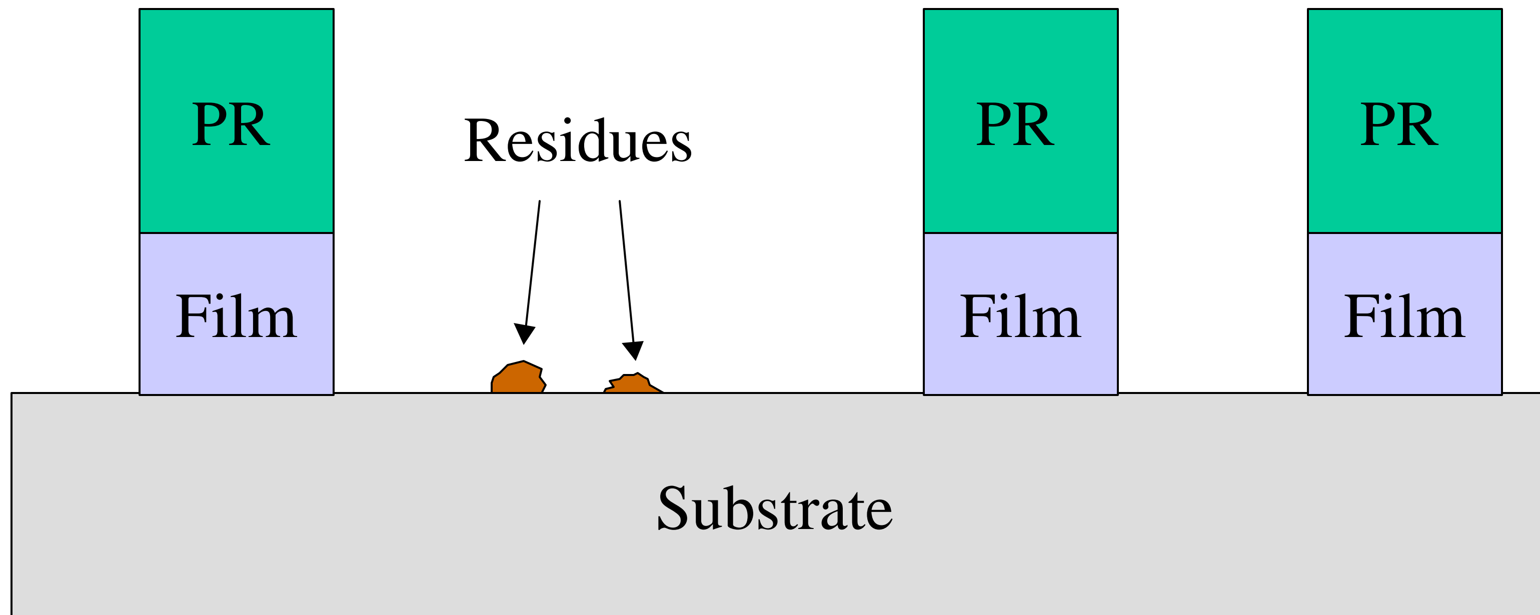
- Unwanted leftovers
- Causes
  - insufficient over etch
  - non-volatile etch byproducts

Insufficient Over Etch





Non-volatile Residue on Surface



Residues

- Adequate over etch
- Removal of non-volatile residues
  - Sufficient ion bombardment to dislodge
  - Right amount of chemical etch to scoop
- Oxygen plasma ashing: Organic residues
- Wet chemical clean: inorganic residues

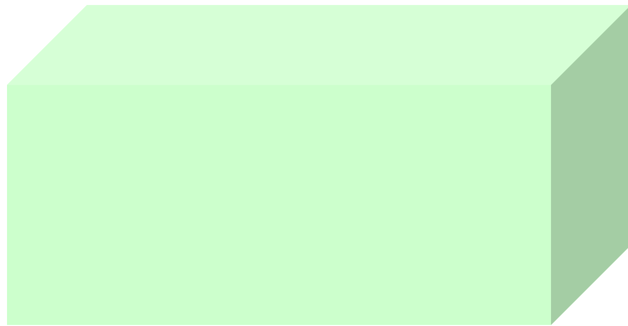
Wet Etch

Wet Etch

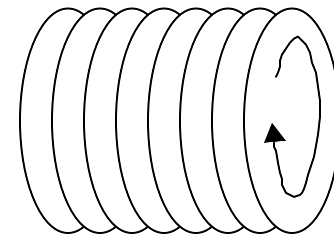
- Chemical solution to dissolve the materials on the wafer surface
- The byproducts are gases, liquids or materials that are soluble in the etchant solution.
- Three basic steps, etch, rinse and dry

Basic Wet Etch Process Steps

Etchant Sink



Spin Dryer

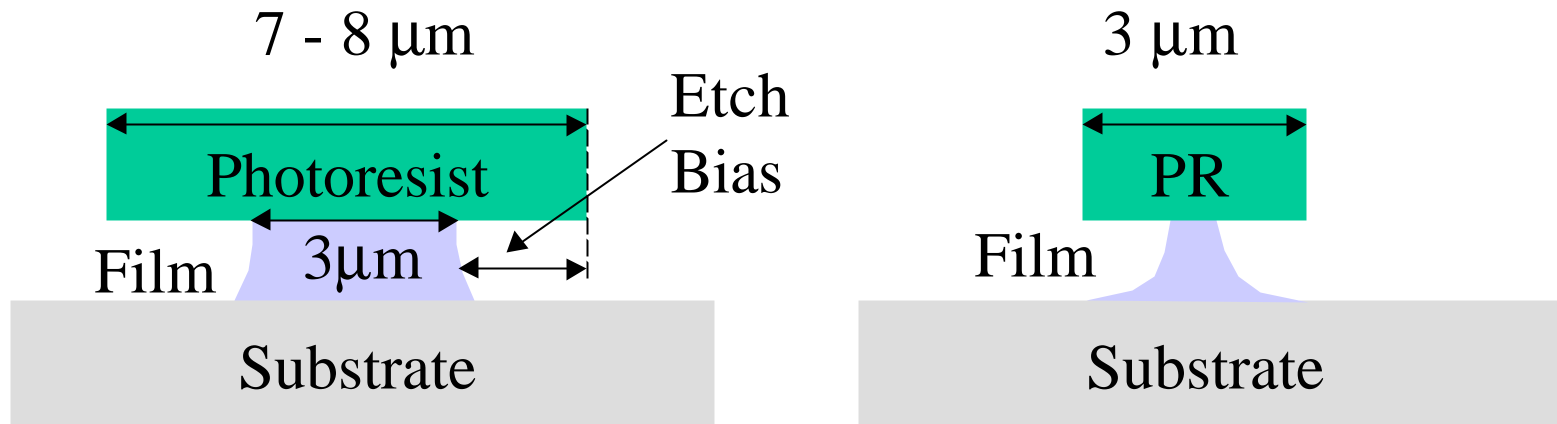


D.I. Wafer Rinse

Wet Etch

- Pure chemical process, isotropic profile
- Was widely used in IC industry when feature size was larger than 3 micron
- Still used in advanced IC fabs
  - Wafer clean
  - Blanket film strip
  - Test wafer film strip and clean

Wet Etch Profiles



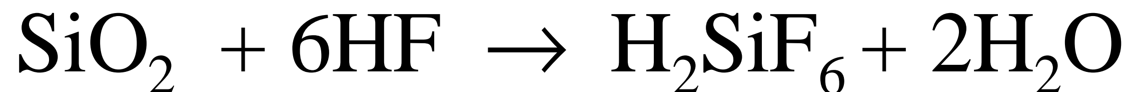
- Can't be used for feature size is smaller than 3 μm
- Replaced by plasma etch for all patterned etch

Applications of Wet Etch

- Wet etch can not be used for patterned etch when CD < 3 μm
- High selectivity
- It is widely used for strip etch process, such as nitride strip and titanium strip, etc.
- Also widely used for CVD film quality control (buffered oxide etch or BOE)
- Test wafers strip, clean, and reuse

Wet Etching Silicon Dioxide

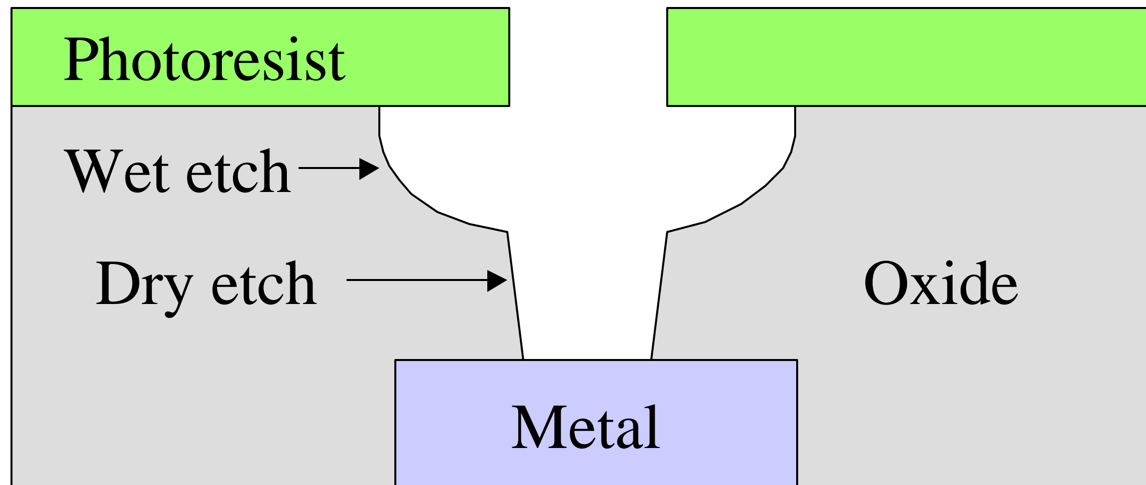
- Hydrofluoric Acid (HF) Solution
- Normally diluted in buffer solution or DI water to reduce etch rate.



$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$$

- Widely used for CVD film quality control
- BOE: Buffered oxide etch
- WERR: wet etch rate ratio

Wide Glass Contact

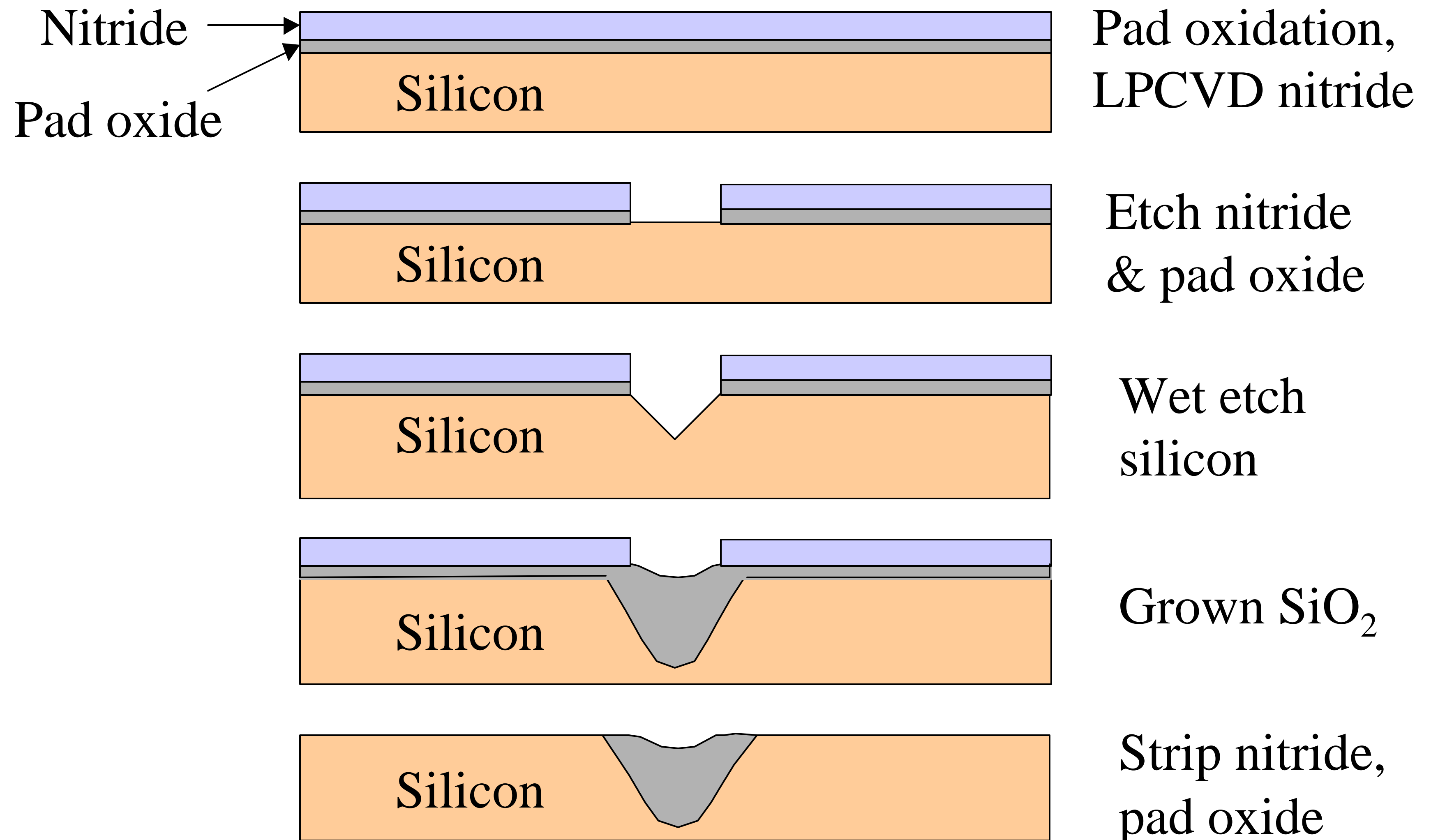


Wet Etching Silicon or Poly

- Silicon etch normally use mixture of nitric acid (HNO_3) and hydrofluoric acid (HF)
- HNO_3 oxidizes the silicon and HF removes the oxide at the same time.
- DI water or acetic acid can be used to dilute the etchant, and reduces the etch rate.

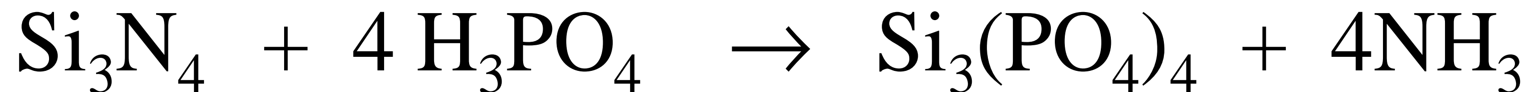
$$\mathbf{Si + 2HNO_3 + 6HF \rightarrow H_2SiF_6 + 2HNO_2 + 2H_2O}$$

Isolation Formation



Wet Etching Silicon Nitride

- Hot (150 to 200 °C) phosphoric acid H_3PO_4 Solution
- High selectivity to silicon oxide
- Used for LOCOS and STI nitride strip



$$Si_3N_4 + 4\,H_3PO_4 \rightarrow Si_3(PO_4)_4 + 4NH_3$$

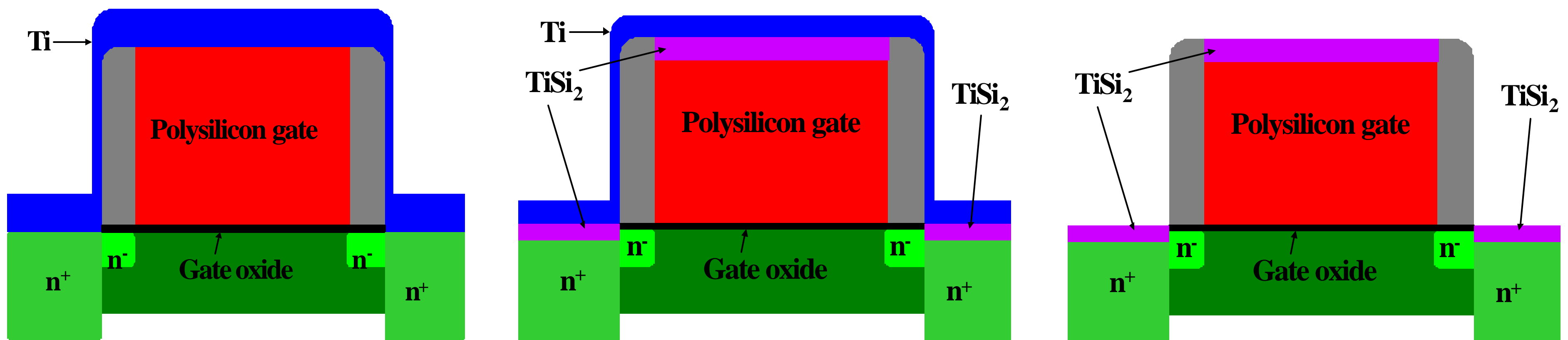
Wet Etching Aluminum

- Heated (42 to 45°C) solution
- One example: 80% phosphoric acid, 5% acetic acid, 5% nitric acid, and 10 % water
- Nitric acid oxidizes aluminum and phosphoric acid removes aluminum oxide at the same time.
- Acetic acid slows down the oxidation of the nitric acid.

Wet Etching Titanium

- 1:1 mixture of hydrogen peroxide (H_2O_2) and sulfuric acid (H_2SO_4)
- H_2O_2 oxidizes titanium to form TiO_2
- H_2SO_4 reacts with TiO_2 and removes it simultaneously
- H_2O_2 oxidizes silicon and silicide to form SiO_2
- H_2SO_4 doesn't react with SiO_2

Self-aligned Titanium Silicide Formation



Titanium deposition

Silicide annealing

Titanium wet striping

Factors that Affect Wet Etch Rate

- Temperature
- Chemical concentration
- Composition of film to be etched

Wet Chemical Hazards

- HF
- H_3PO_3
- HNO_4

- Corrosive
- Oxidizer
- Special hazard

Wet Chemical Hazards

- HF
- Don't feel when contact
- Attack bone and neutralize by calcium
- Acute pain

- Never assume. Treat all unknown clear liquid as HF in IC fab.

Advantages of Wet Etch

- High selectivity
- Relatively inexpensive equipment
- Batch system, high throughput

Disadvantages of Wet Etch

- Isotropic Profile
- Can't pattern sub-3μm feature

- High chemical usage
- Chemical hazards
  - Direct exposure to liquids
  - Direct and indirect exposure to fumes
  - Potential for explosion

Plasma Etch

Introduction

- Gas in, gas out
- Plasma generates free radicals and ion bombardment
- RIE (Reactive Ion Etch)
  - combined chemical and physical etch
- Most patterned etches are RIEs

Comparison of Wet and Dry Etch

	Wet Etch	**Dry Etch**
Etch Bias	Unacceptable for < 3μm	Minimum
Etch Profile	Isotropic	Anisotropic to isotropic, controllable
Etch rate Selectivity	High High	Acceptable, controllable Acceptable, controllable
Equipment cost	Low	High
Throughput	High (batch)	Acceptable, controllable
Chemical usage	High	Low

Plasma Basics

- A plasma is an ionized gas with equal numbers of positive and negative charges.
- Three important collisions:
  - *Ionization* generates and sustains the plasma
  - *Excitation-relaxation* causes plasma glow
  - *Disassociation* creates reactive free radicals

Components of Plasma

- A plasma consists of neutral atoms or molecules, negative charges (electrons) and positive charges (ions)
- Quasi-neutral: n_i » n_e
- Ionization rate: $\boldsymbol{h}$ » $n_e/(n_e + n_n)$

Ionization Rate

- Ionization rate is mainly determined by electron energy in plasma
- In most plasma processing chambers, the ionization rate is less than 0.001%.
- The ionization rate of high density plasma (HDP) source is much higher, about 1%.
- Ionization rate in the core of sun is ~100%.

Mean Free Path (MFP)

- The average distance a particle can travel before colliding with another particle.

$$\boldsymbol{l} = \frac{1}{n\boldsymbol{s}}$$

- n is the density of the particle
- $\boldsymbol{s}$ is the collision cross-section of the particle

Mean Free Path (MFP)

- Effect of pressure:

$$\boldsymbol{l} \propto \frac{1}{p}$$

- Higher pressure, shorter MFP
- Lower pressure, longer MFP

Vacuum and Plasma

- Pressure too high, MFP will be too short
- Ionization usually require at least 15 eV
- Electrons can't get enough energy to ionize if MFP is too short
- Need vacuum and RF to start and maintain stabilize plasma

Ion Bombardment

- Anything close to plasma gets ion bombardment
- Very important for sputtering, RIE and PECVD
- Mainly determined by RF power
- Pressure also affects ion bombardment

Ion Bombardment

- Electrons are moving much faster than ions
- Electrons reach electrodes and chamber wall first
- Electrodes are charged negatively, repel electrons and attract ions
- Charge difference near the surface forms sheath potential
- Sheath potential accelerates ions towards the electrode and causes ion bombardment

Ion Bombardment

- Ion energy
- Ion density
- Both controlled by RF power

Applications of Ion Bombardment

- Help to achieve anisotropic etch profile
  - Damaging mechanism
  - Blocking mechanism
- Argon sputtering
  - Dielectric etch for gap fill
  - Metal deposition
- Help control film stress in PECVD processes
  - Heavier bombardment, more compressive film

Ion Bombardment Control

- Increasing RF power, DC bias increases, ion density also increases.
- Both ion density and ion bombardment energy are controlled by RF power.
- RF power is the most important knob controlling ion bombardment

Ion Bombardment Control

- RF power is the main knob to control etch rate
  - Increasing RF power, increases etch rate
  - usually reduces selectivity
- RF power also used to control film stress for PECVD processes
  - Increasing RF power increase compressive stress

Self-Bias

- Different size electrodes
- No net charge build up in plasma
- Charge fluxes on both electrodes are the same
- Smaller electrode has higher charge density
- Larger DC bias between plasma and smaller electrode

Etch Processes

Chemical RIE Physical

Blocking Mechanism **Damaging Mechanism**

Blocking Mechanism	Damaging Mechanism
Silicon Etch	Oxide Etch
Poly Etch	Nitride Etch
Metal Etch	

Chemical Etch

- Purely chemical reaction
- By products are gases or soluble in etchants
- High selectivity
- Isotropic etch profile
- Examples:
  - Wet etch
  - Dry strip

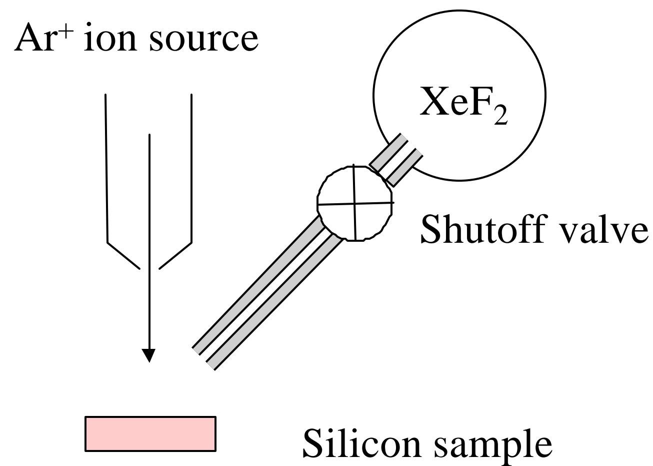
Physical Etch

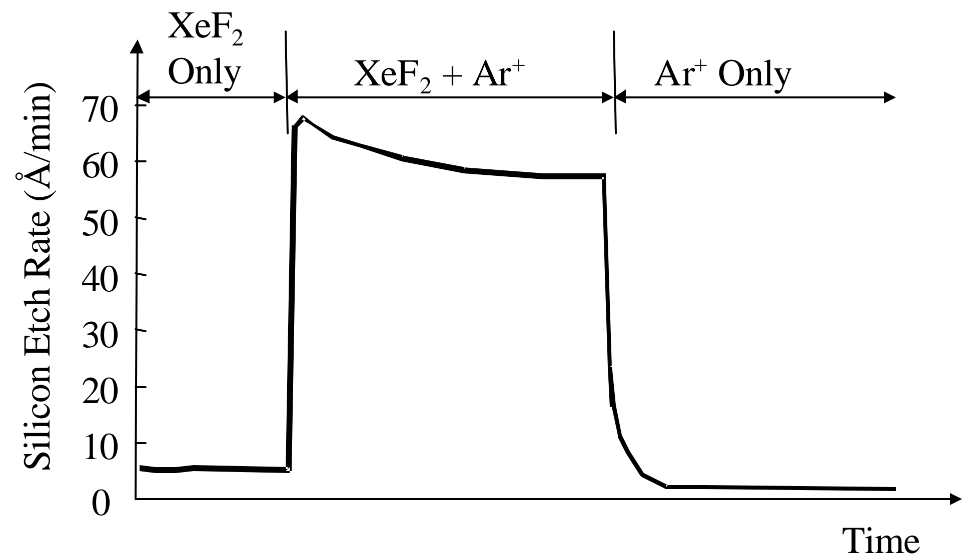
- Bombardment with inert ions such as Ar^+
- Physically dislodging material from surface
- Plasma process
- Anisotropic profile
- Low selectivity
- Example:
  - Argon sputtering etch

Reactive Ion Etch (RIE)

- Combination of chemical and physical etch
- Plasma process, ion bombardment plus free radicals
- Misleading name, should be called ion assistant etch (IAE)
- High and controllable etch rate
- Anisotropic and controllable etch profile
- Good and controllable selectivity
- All patterned etches are RIE processes in 8" fabs

RIE Experiment





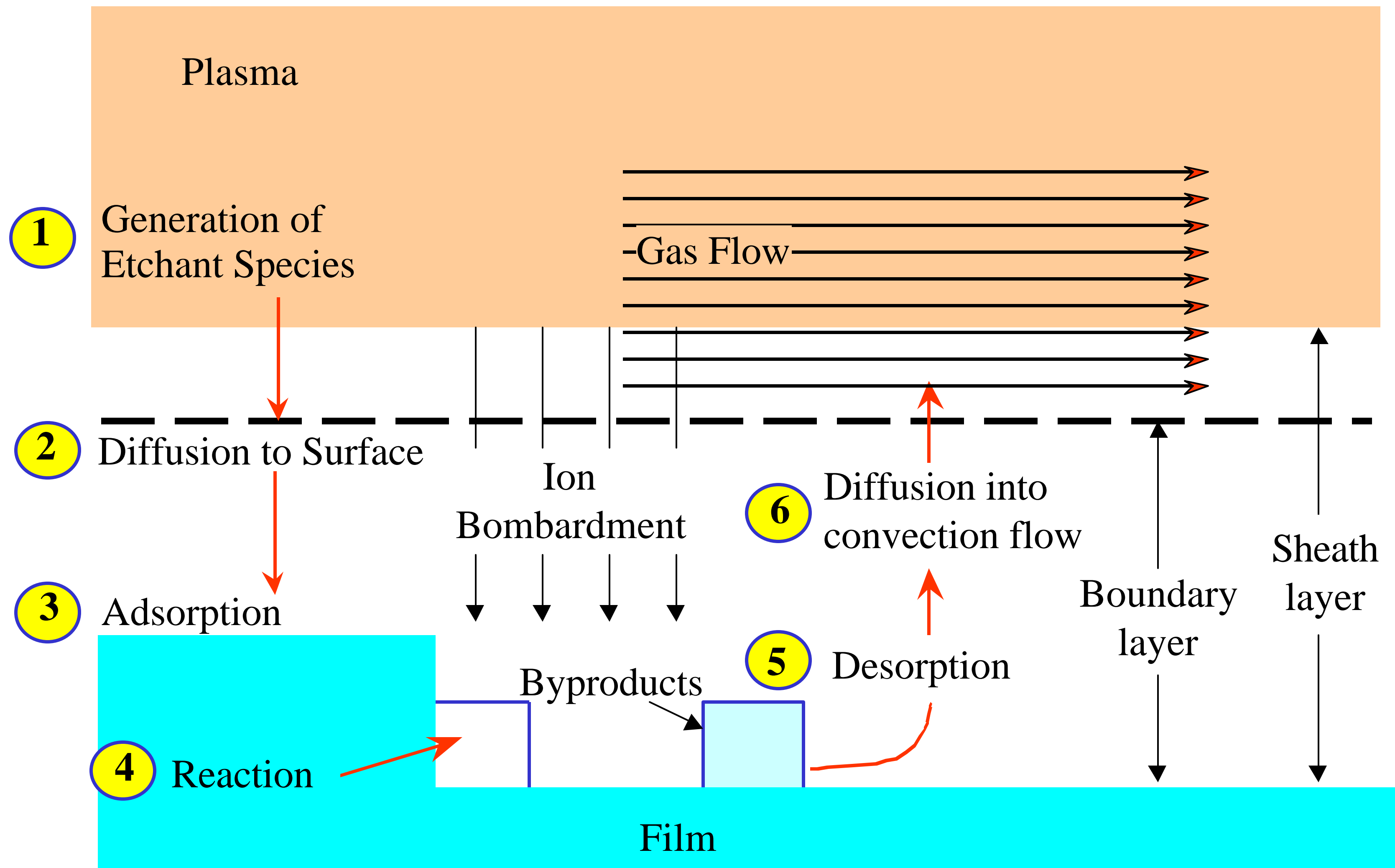
Experiment arrangement

Experiment results

Three Etch Processes

	Chemical Etch	RIE	Physical Etch
Examples	Wet etch, strip, RP etch	Plasma patterned etches	Argon sputtering
Etch rate	High to low	High, controllable	Low
Selectivity	Very good	Reasonable, controllable	Very poor
Etch profile	Isotropic	Anisotropic, controllable	Anisotropic
Endpoint	By time or visual	Optical	By time

Etch Process Sequence



Etch Profile Control

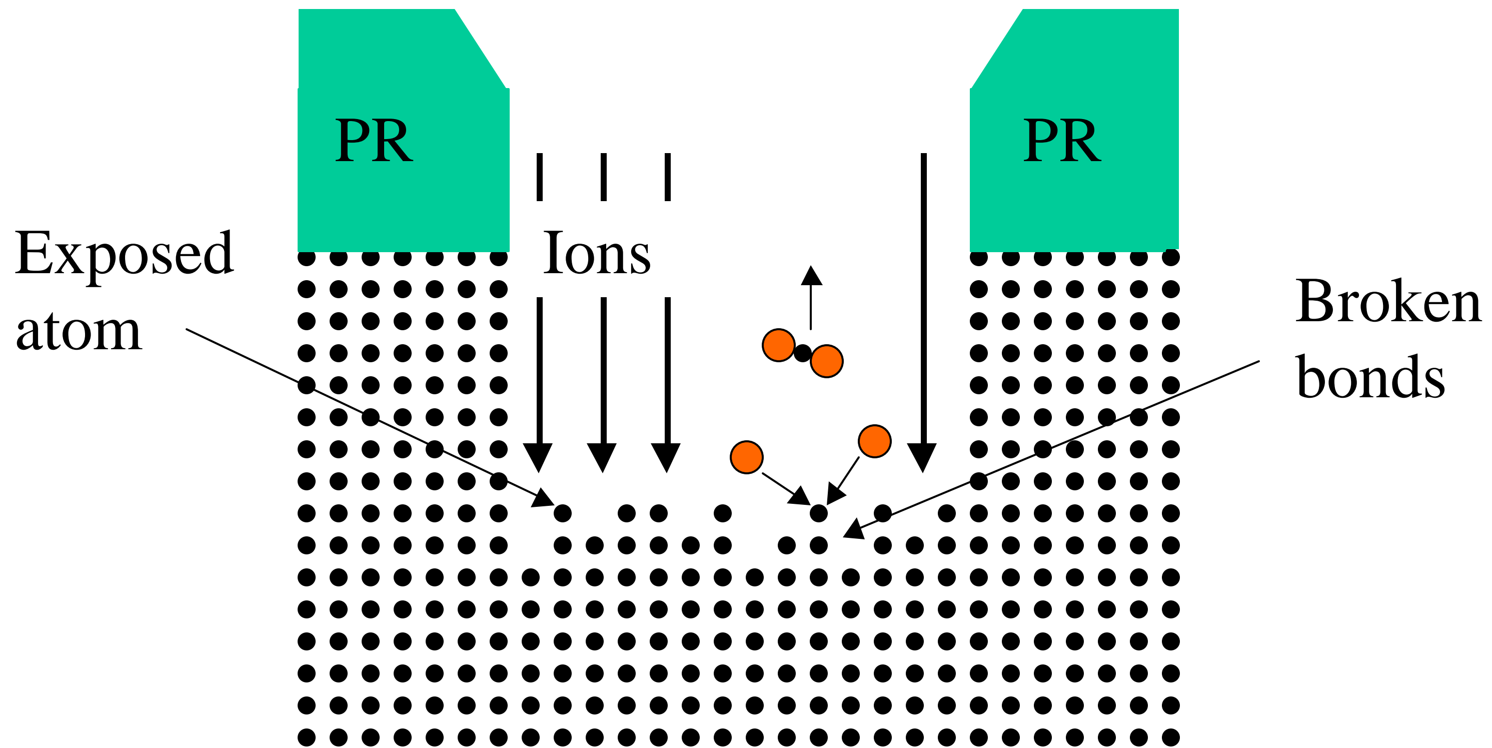
Damaging	**Blocking**
Oxide	Epi-silicon
Nitride	Polysilicon
	Metal

Anisotropic profile control can be achieved by using ion bombardment from plasma

Damaging Mechanism

- Heavy ion bombardment damages chemical bonds
- Exposed surface atoms are easier to react with etchant free radicals
- Ion bombardment is mainly in vertical direction
- Etch rate on vertical direction is much higher than on horizontal direction → anisotropic etch

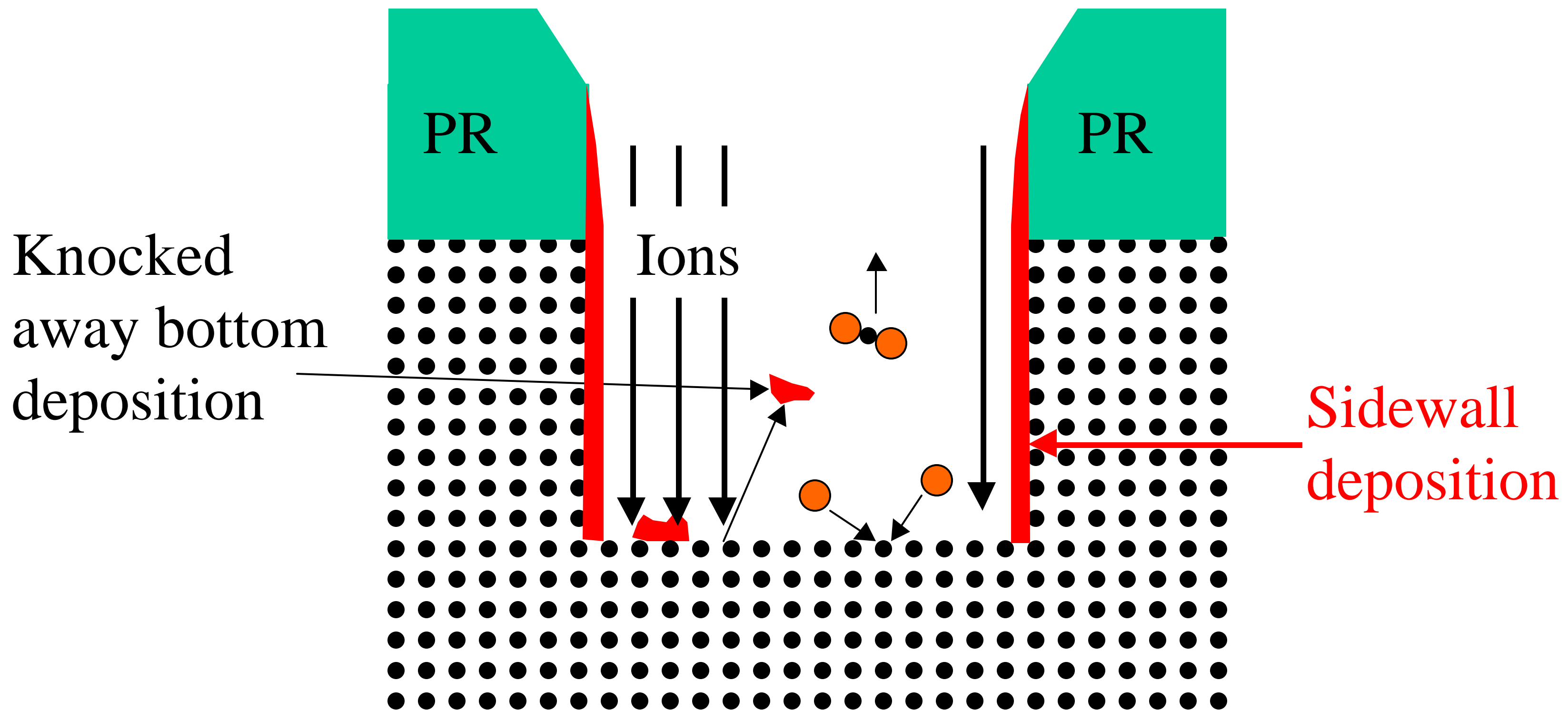
Damage Mechanism



Blocking Mechanism

- Chemicals deposit on the surface
- Sputtered photoresist and/or byproducts of etch chemical reaction
- Ion bombardment is mainly in vertical direction
- It prevents deposition to buildup on bottom
- Deposition on sidewall blocks etch process
- Etch process is mainly in vertical direction

Blocking Mechanism



Etched Atom or molecule

Etchant free radical

Etch Byproduct

Etch Mechanisms and Their Applications

Pure Chemical Etch	**Reactive Ion Etch (RIE)**		**Pure Physical Etch**
	Blocking mechanism	Damaging mechanism	
No ion bombardment	Light ion bombardment	Heavy ion bombardment	Only ion bombardment
PR strip	Single crystal silicon etch		
Ti strip	Polysilicon etch	Oxide etch	Sputtering etch
Nitride strip	Metal etch	Nitride etch	

Benefits of Using Plasma For Etch Process

- High etch rate
- Anisotropic etch profile
- Optical endpoint

Plasma Etch Chambers

- Batch system
- Single wafer system
- High density plasma system
  - IPC
  - ECR
  - Helicon

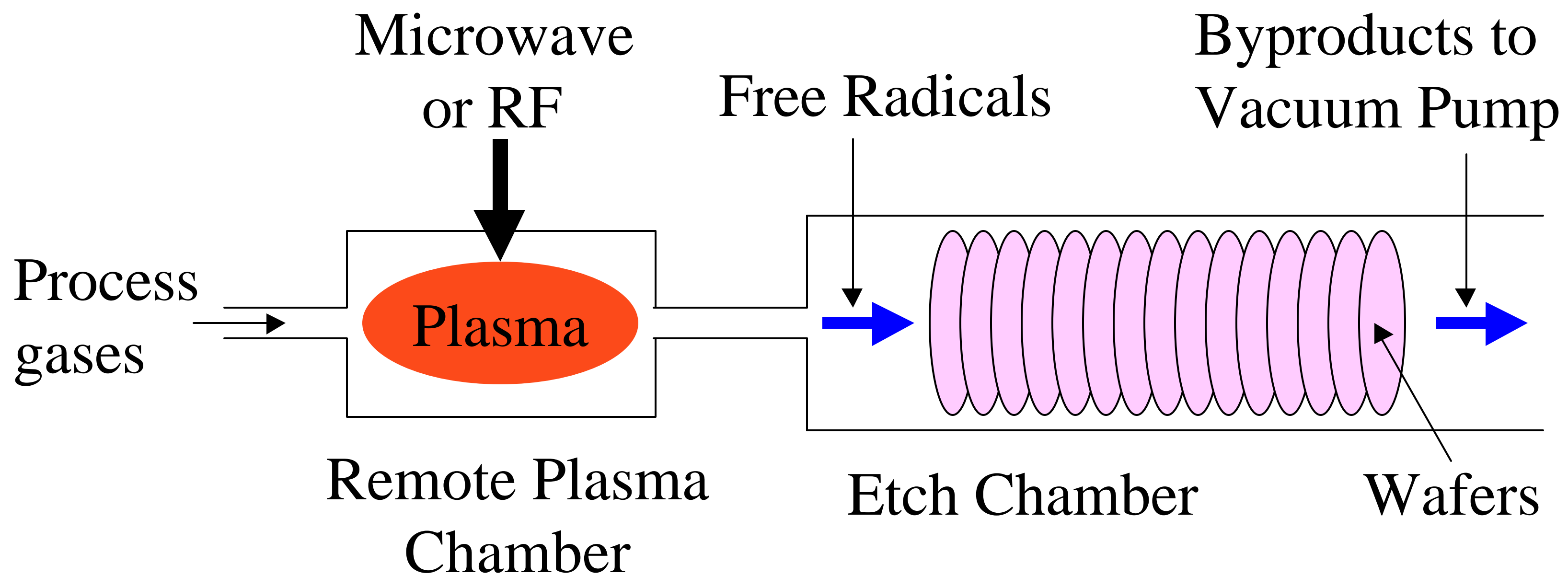
Batch Systems

- High throughput
- Older systems
- Smaller diameter, <150 mm or 6 inch
- Downstream etcher and barrel etch system
  - Both are pure chemical etch, no ion bombardment

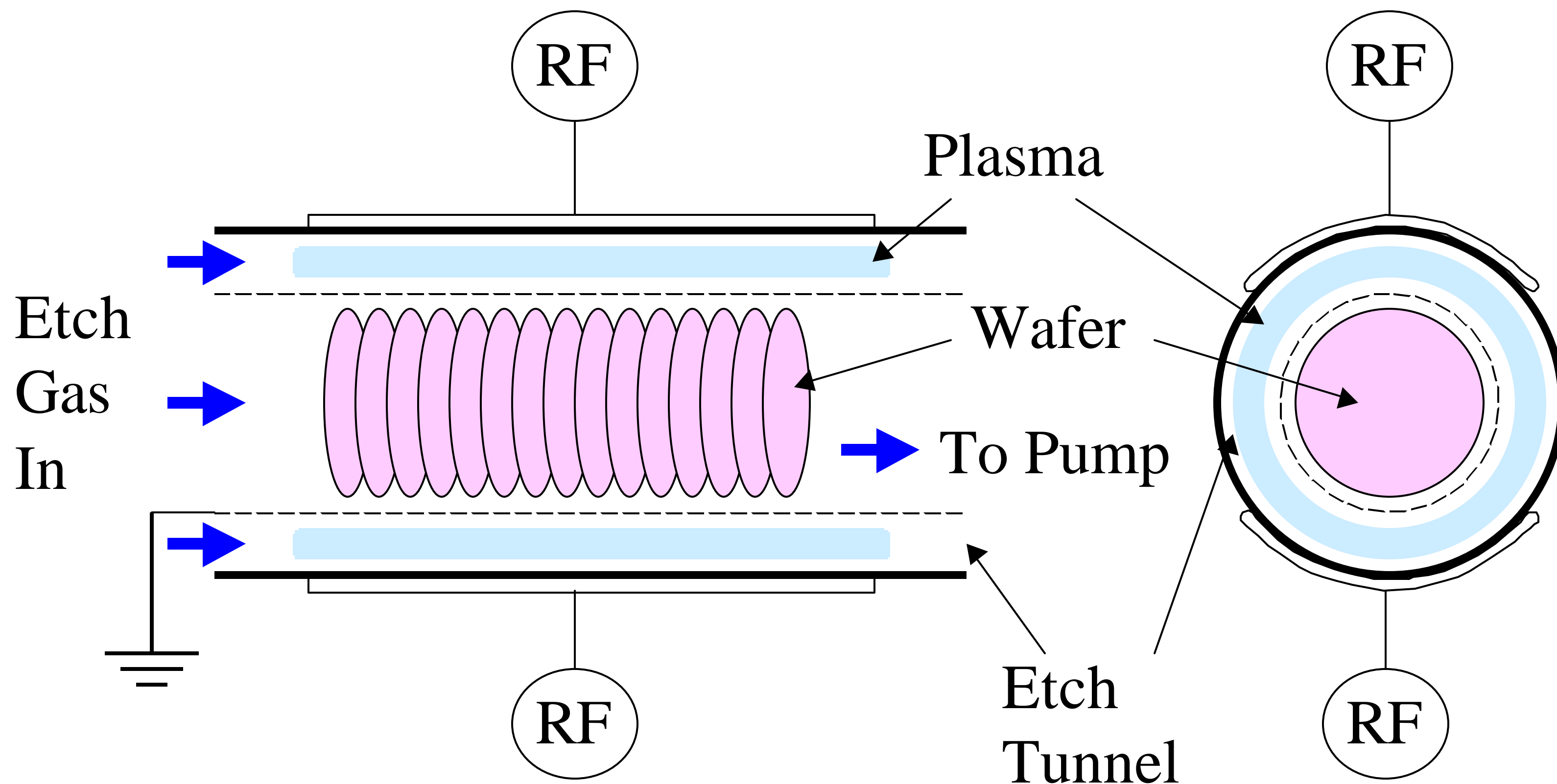
Etch Chamber

- Lower pressure, longer MFP, less collisions
- High ion energy, less ion scattering and better anisotropy etch profile
- Lower pressure also helps to remove the etch byproducts
- Etch chambers usually operate at lower pressure

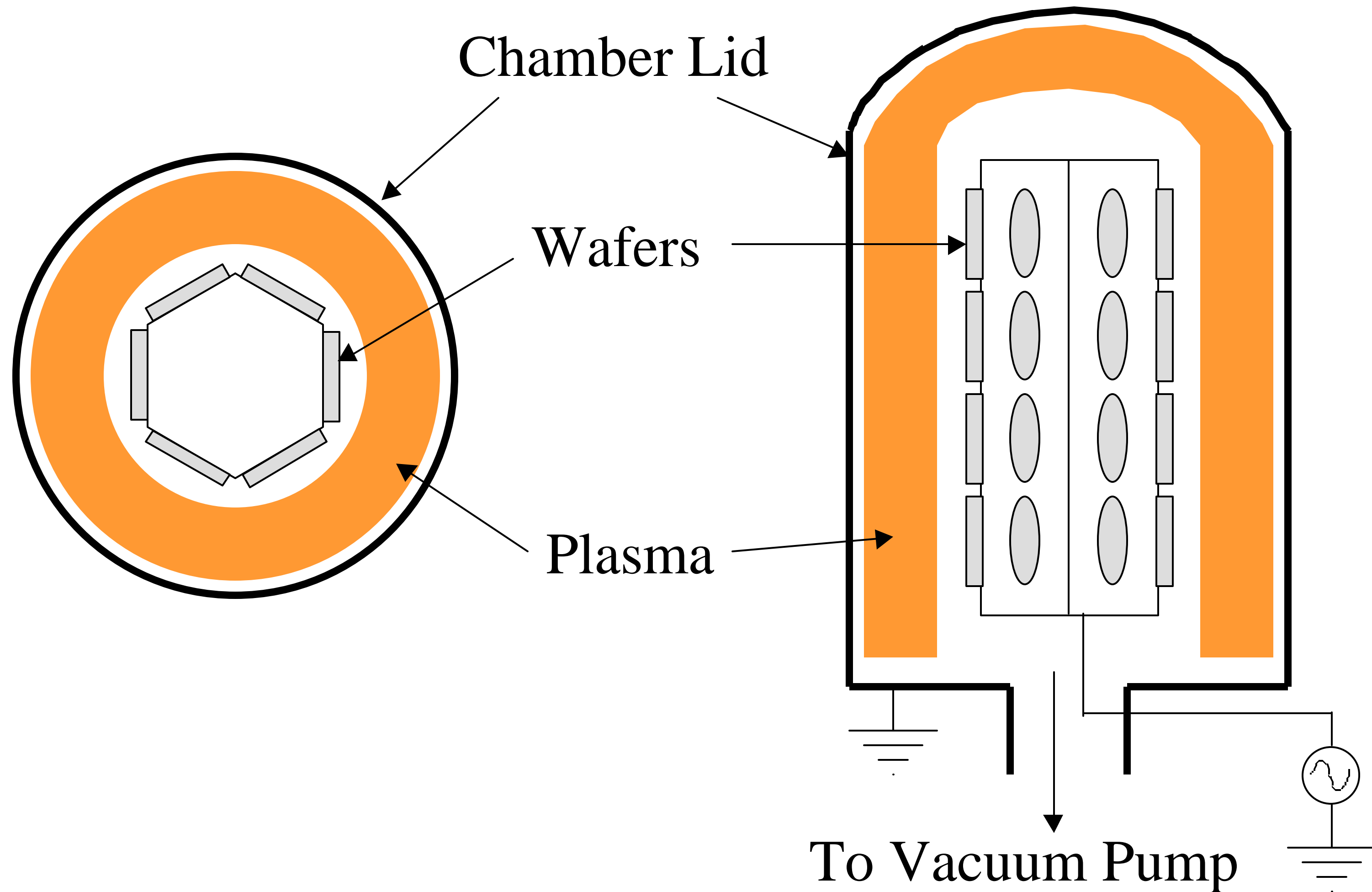
Down Stream Plasma Etcher



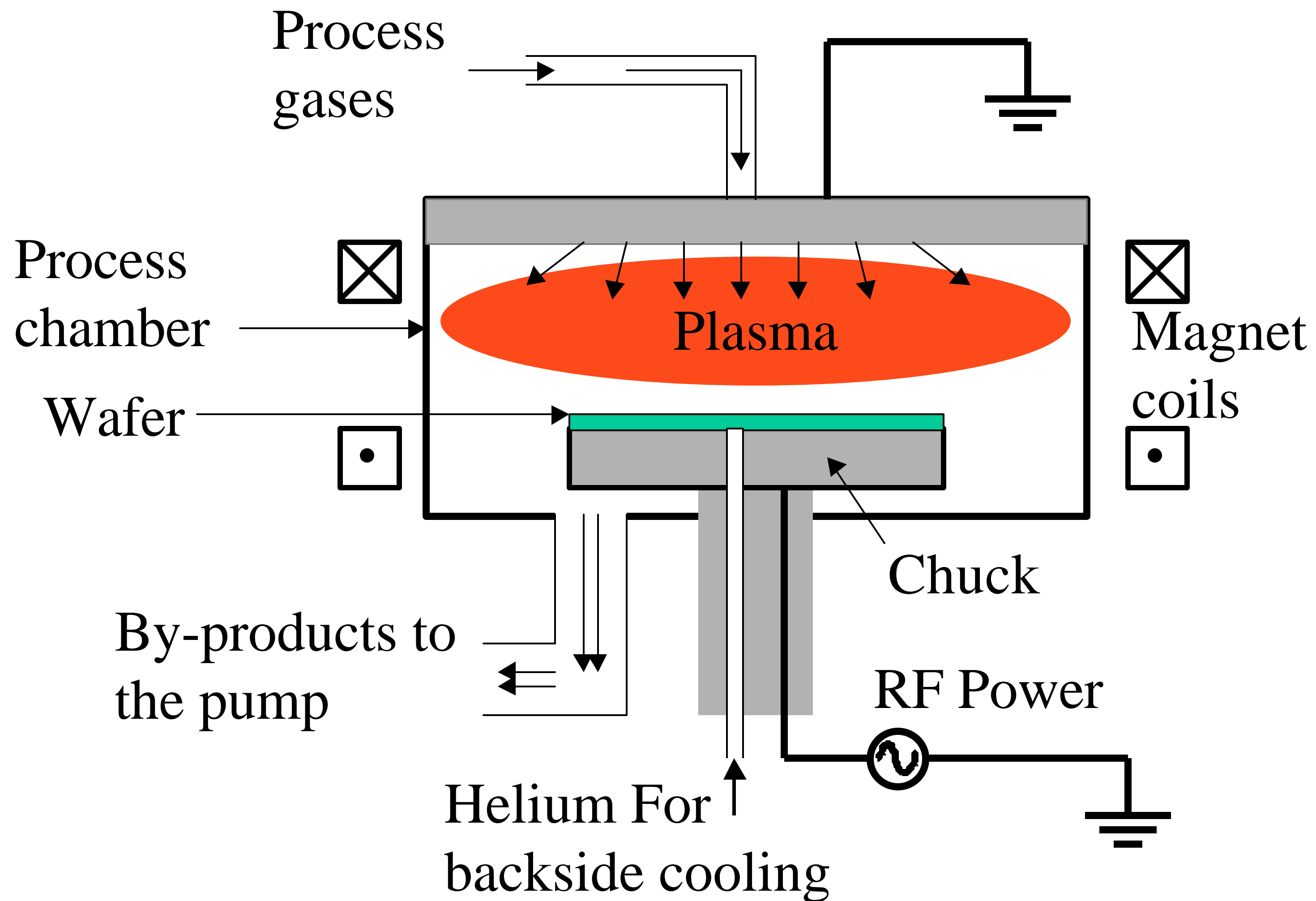
Barrel Etch System



Batch RIE System



Schematic of an RIE System



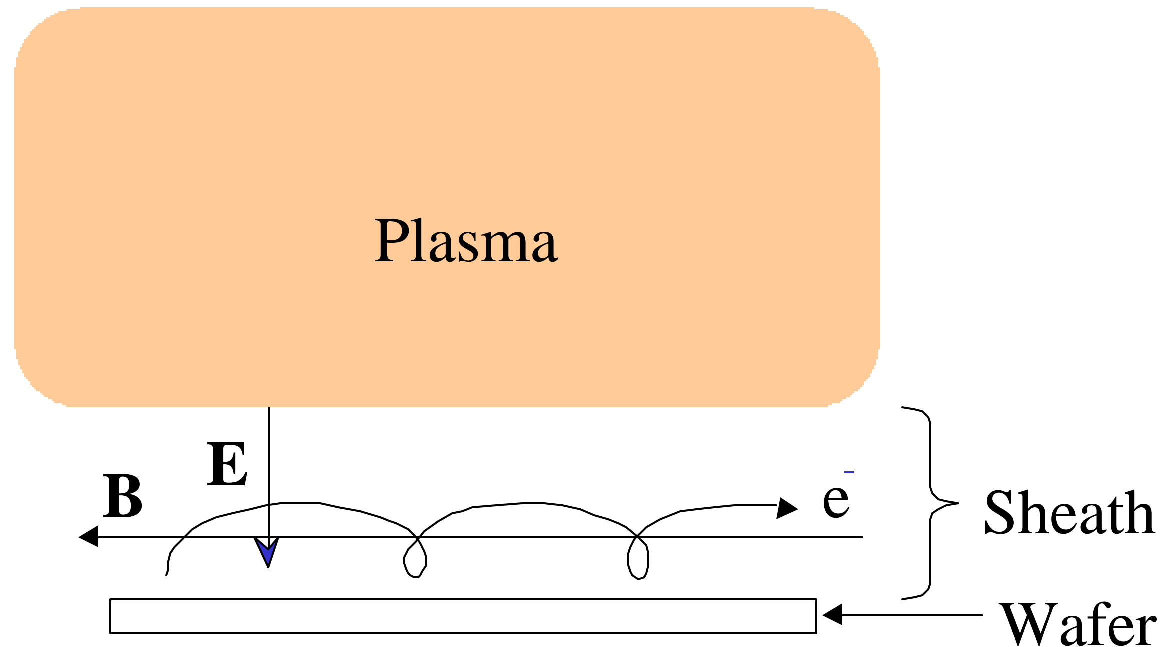
Purpose of Magnets

- Long MFP, insufficient ionization collisions
- In a magnetic field, electron is forced to spin with very small gyro-radius
- Electrons have to travel longer distance
- More chance to collide
- Increasing plasma density at low pressure

Effect of Magnetic Field on DC Bias

- Magnetic field increasing electron density in sheath layer
- Less charge difference in sheath region
- Lower DC Bias
- Effects on ion bombardment
  - increasing ion density
  - reducing ion energy

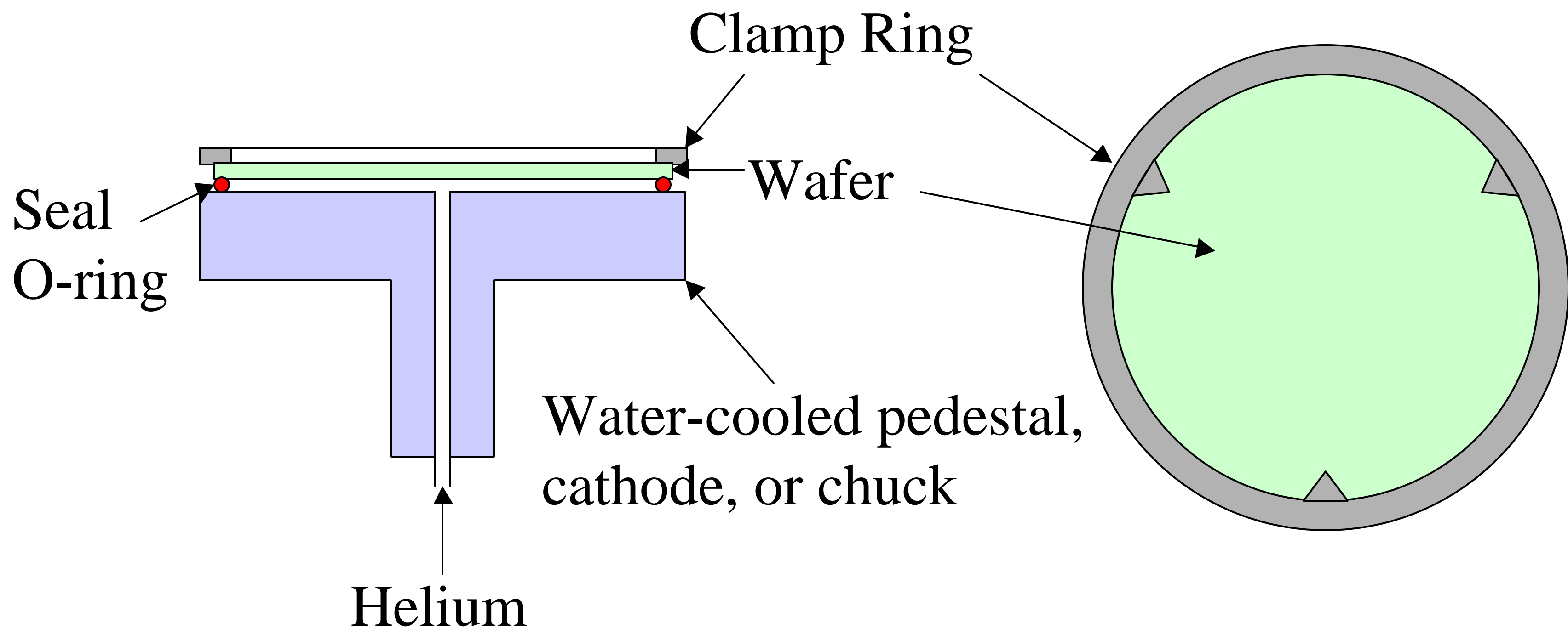
Effect of Magnetic Field on DC Bias



Wafer Cooling

- Ion bombardment generate large amount heat
- High temperature can cause PR reticulation
- Need cool wafer to control temperature
- Helium backside cooling is commonly used
- Helium transfer heat from wafer to water cooled chuck

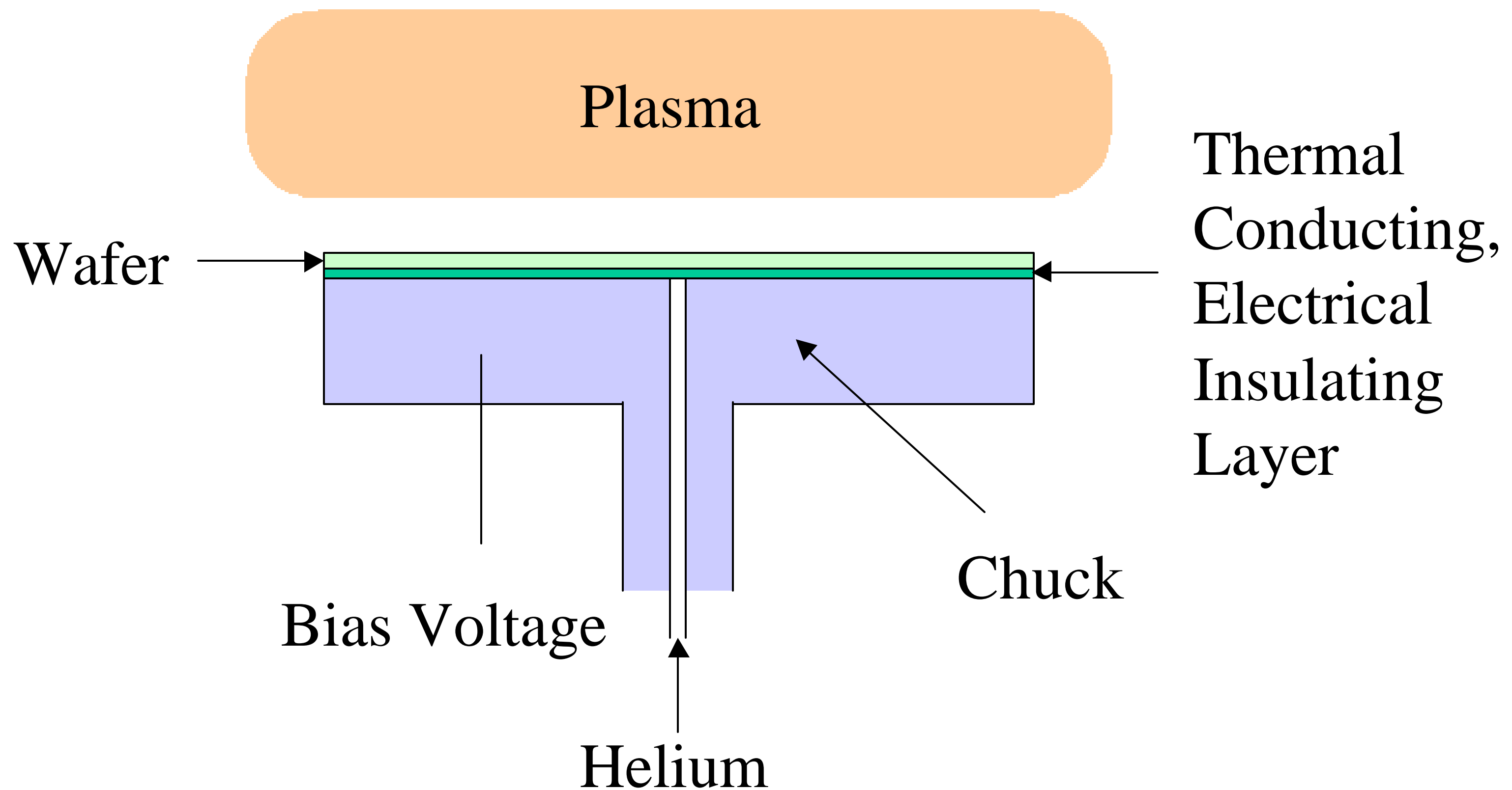
Clamp Ring



Electrostatic Chuck (E-chuck)

- Helium needs to be pressurized
- Wafer has high pressure at backside because low chamber pressure
- Need mechanisms to hold wafer
- Either mechanical clamp or E-chuck
- Clamp ring causes particles and shadowing effect
- E-chuck is rapidly replacing clamp ring

Electrostatic Chuck



Facts of Helium

Name	Helium
Symbol Atomic number	He 2
Atomic weight	4.002602
Discoverer	Sir William Ramsay and independently by N. A. Langley and P. T. Cleve
Discovered at	London, England and Uppsala, Sweden
Discovery date	1895
Origin of name	From the Greek word "helios" meaning "sun". Its line radiation (a yellow line at 587.49 nm) was first detected from the solar spectrum during in solar eclipse of 1868 in India by French astronomer,
Molar volume	21.0cm^3
Velocity of sound	970 m/sec
Refractive index	1.000035
Melting point	0.95 K or -272.05 C
Boiling point	4.22 K or -268.78 C
Thermal conductivity Applications	0.1513 W m^{-1} K^{-1} Cooling gas and carrier gas in CVD and etch processes

High Density Plasma (HDP) Sources

- Low pressure is desired for etch process
- Electrons are easily lost due to long MFP by collide with electrodes or chamber wall
- Hard to generate plasma
- Parallel plate system or capacitive coupled system can not generate high density plasma
- Different plasma systems are needed to generate HDP at low pressure

HDP Systems

- Inductively coupled plasma (ICP)
- Electron cyclotron resonance (ECR)
- Helicon

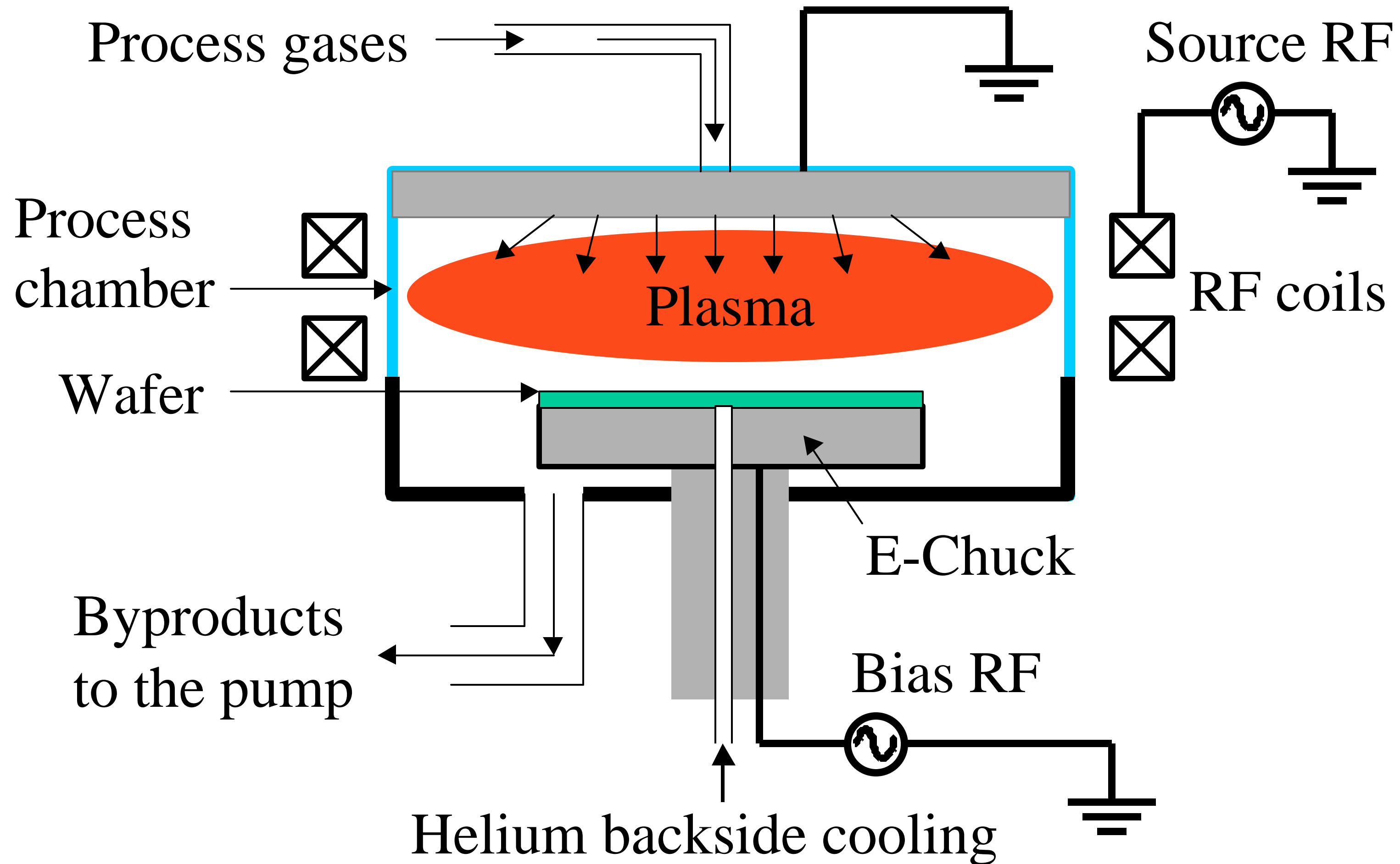
ICP

- Inductively couple RF power to plasma
- Like a transformer, also called TCP
- Changing magnetic field cause electric field
- Electrons are accelerated in angular direction
- Could achieve high plasma density at low pressure

ICP Chamber

- Upper part of chamber: ceramic or quartz
- Source RF inductively couple with plasma
- Source RF generates plasma and controls ion density
- Bias RF controls ion bombardment energy
- Ion energy and density independently controlled

Schematic of ICP Chamber



ECR

- In magnetic field, electron gyro-frequency

$$W_e \text{ (MHz)} = 2.80\ B \text{ (Gauss)}$$

- If incident microwave frequency equals to W_e

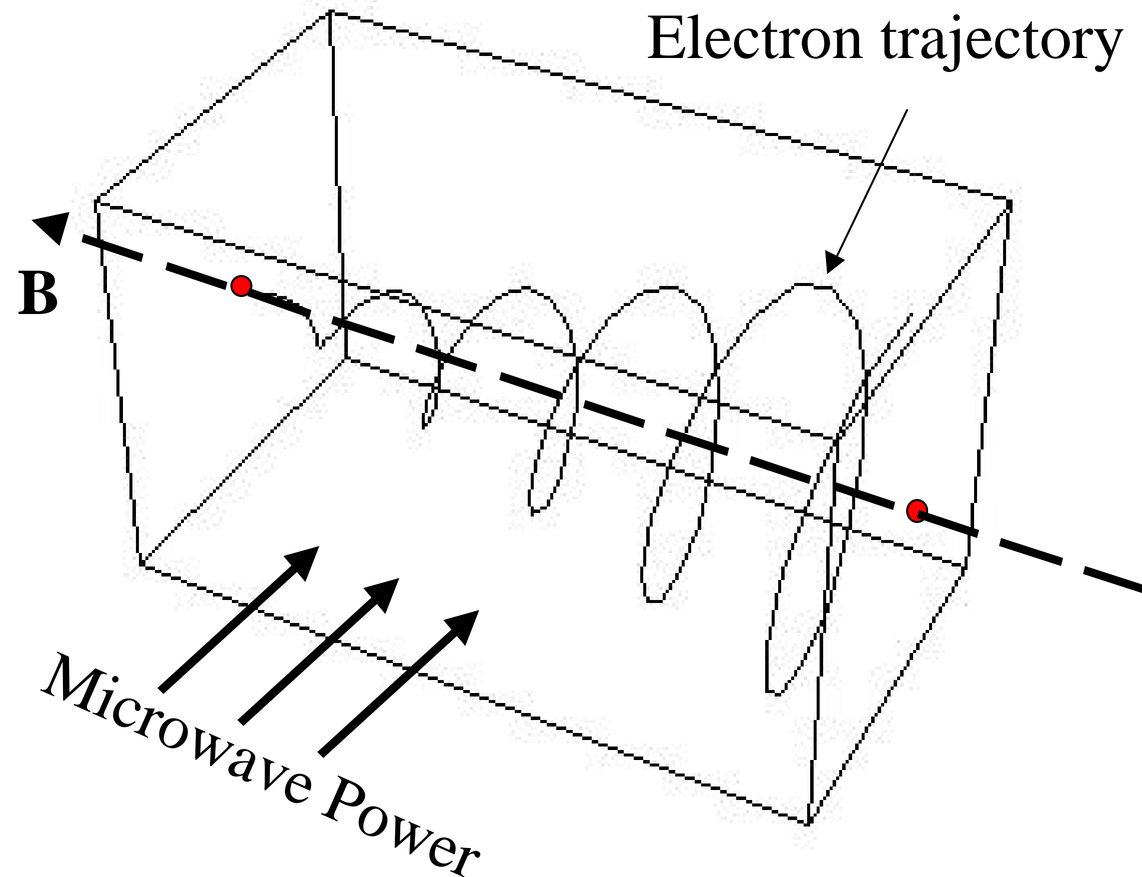
$$w_{MW} = W_e$$

- Resonance
- Electrons get energy from microwave

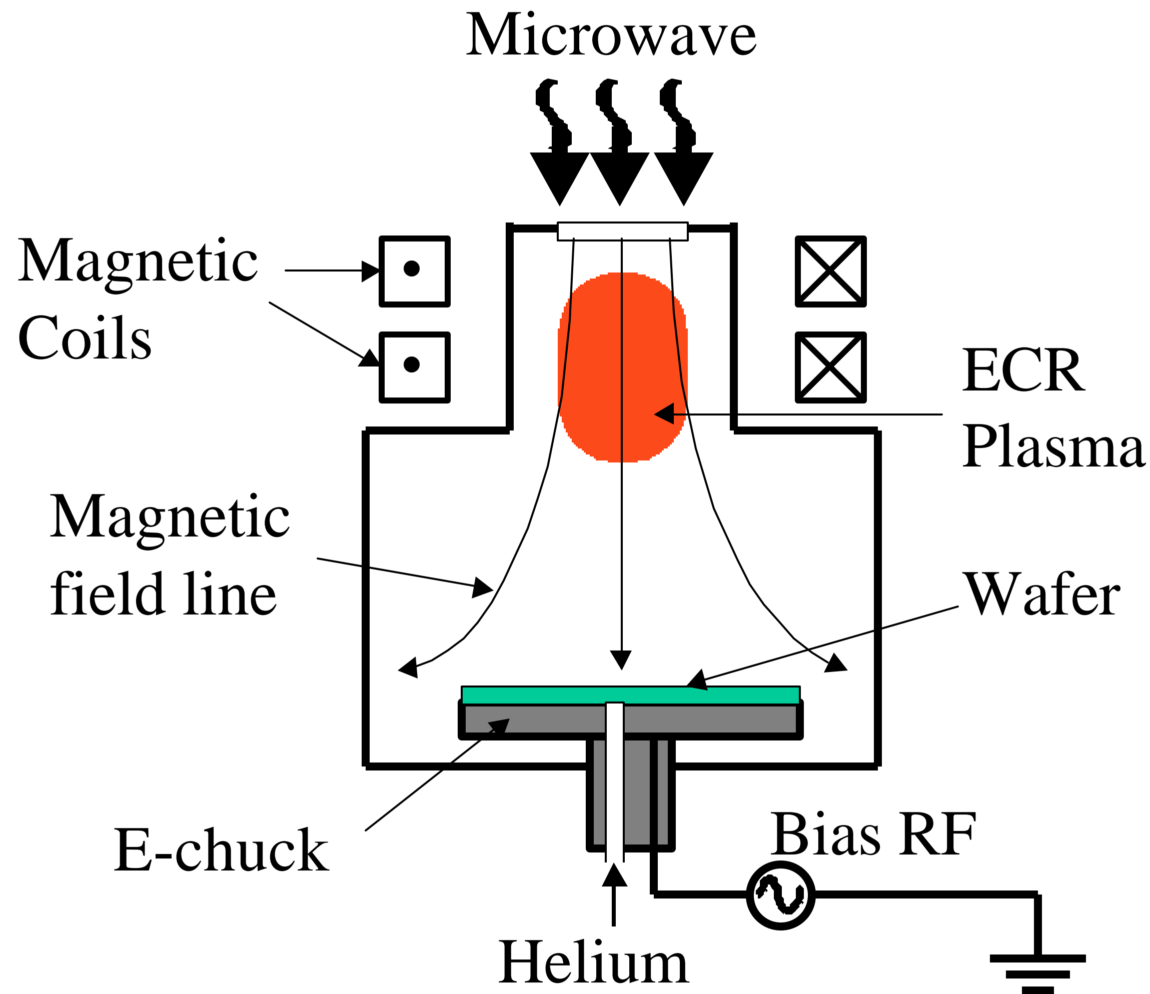
ECR

- Resonance condition won't change with fixed $\boldsymbol{w}_{MW}$ and B
- Electrons gyro-radius, $\boldsymbol{r} = v_t/\boldsymbol{W}_e$ is very small
- Electron can be accelerated to high energy for ionization collision
- Generate high density plasma at low pressure

Illustration of ECR



Schematic of ECR Chamber



Endpoint

- Each atom has its own emission wavelength
- Color of plasma changes when etch different materials
- Optical sensors can be used to detect the change and indicate the endpoint for plasma etch processes

Etch Endpoint Wavelengths

Film	Etchant	Wavelength (Å)	Emitter
Al	Cl_2, BCl_3	2614	AlCl
		3962	Al
Poly Si	Cl_2	2882	Si
		6156	O
Si_3N_4	CF_4/O_2	3370	N_2
		3862	CN
		7037	F
		6740	N
SiO_2	CF_4 and CHF_3	7037	F
		4835	CO
		6156	O
PSG, BPSG	CF_4 and CHF_3	2535	P
W	SF_6	7037	F

Plasma Etch Processes

Advantage of the Plasma Etch

- High, controllable etch rate
- Good selectivity
- Anisotropic etch profile

- Disadvantage: expensive, complicated system
  - Vacuum, RF, robot, E-chuck and etc.

Etch Mechanisms and Requirements

- Oxide etch using damaging mechanism
- More physical than chemical
- Higher RF power and lower pressure
- Silicon and metal etches using blocking mechanism
- Chemical than physical
- Usually require less RF power

PLASMA ETCH

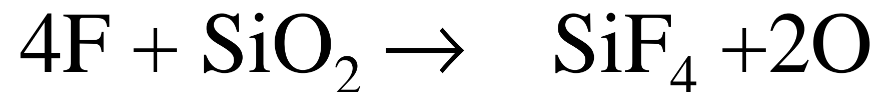
- Etch dielectric
- Etch single crystal silicon
- Etch polysilicon
- Etch metal
- Summary

Dielectric Etch

- Etch oxide
  - Doped and undoped silicate glass
  - Contact (PSG or BPSG)
  - Via (USG, FSG or low-κ dielectric)
- Etch nitride
  - STI
  - Bonding pad

Dielectric Etch

- Fluorine chemistry



$$4F + SiO_2 \rightarrow SiF_4 + 2O$$

- CF_4 is commonly used as fluorine source
- NF_3 and SF_6 have also been used

Some Facts About Fluorine

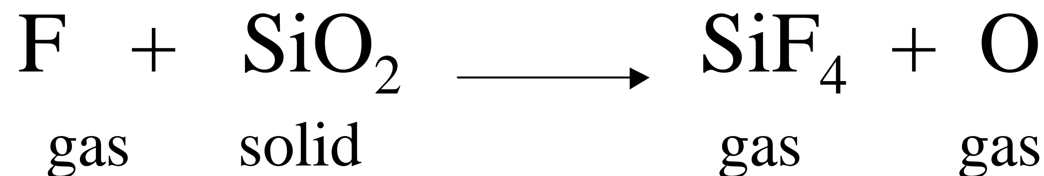
Name	Fluorine
Symbol	F
Atomic number	9
Atomic weight	18.9984032
Discoverer	Henri Moissan
Discovered at	France
Discovery date	1886
Origin of name	From the Latin word "fluere" meaning "to flow"
Molar volume	11.20 cm^3
Velocity of sound	No data
Refractive index	1.000195
Melting point	53.53 K or -219.47 C
Boiling point	85.03 K or -187.97 C
Thermal conductivity	0.0277 W m^{-1} K^{-1}
Applications	Free fluorine as the main etchant for silicon oxide and silicon nitride etching processes

Contact Etch

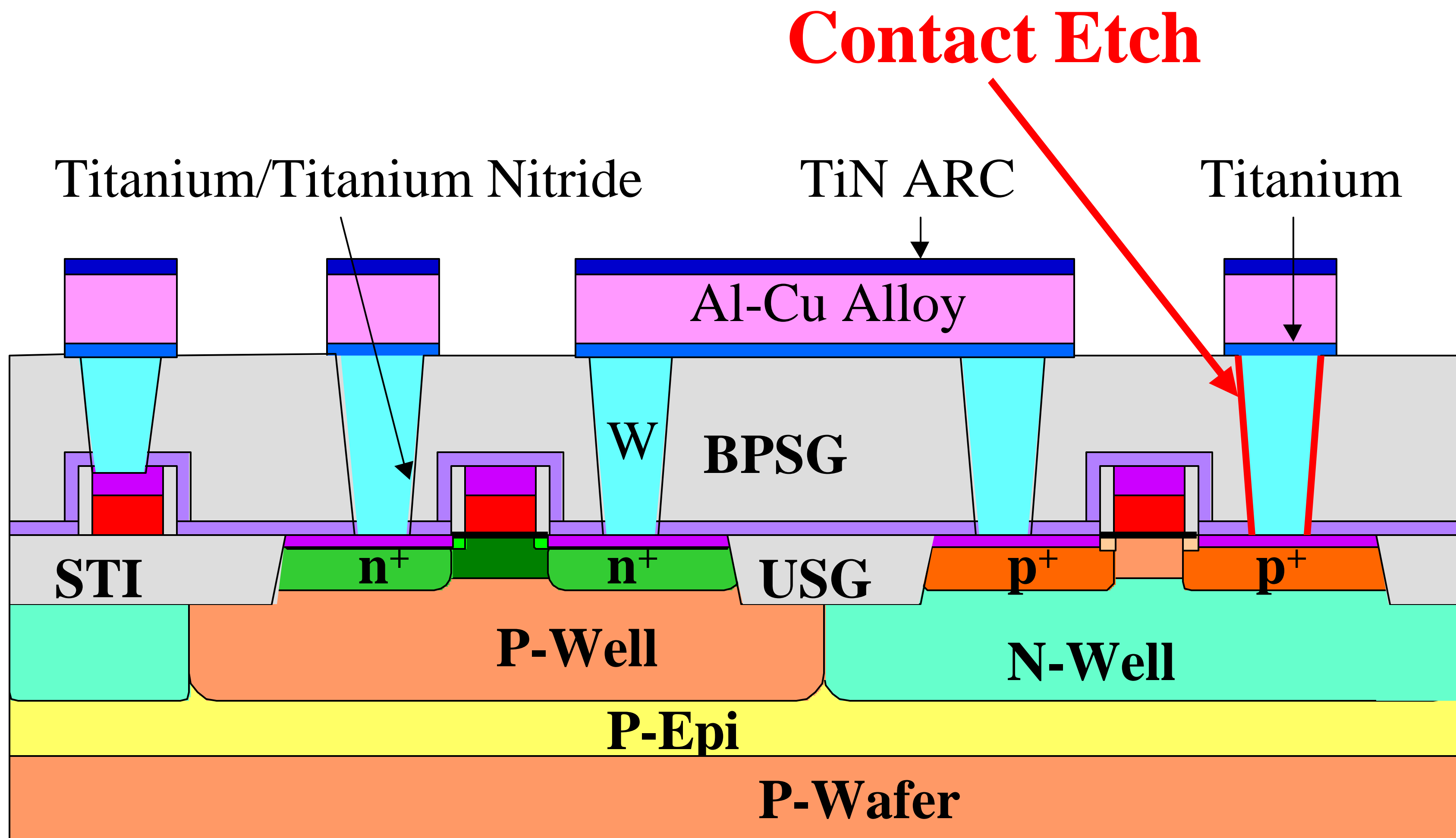
- Holes connect silicon to metal lines
- Doped silicate glass, PSG for BPSG
- Fluorine form CF_4 as the main etchant
- CHF_3 as polymer precursor to improve selectivity to silicon and silicide
- Ar to improve damaging effect
- Some people also use O_2 or H_2
- High selectivity to Si or silicide is required

Contact Etch

- Etch PSG or BPSG
- Open contact hole for silicon to metal interconnections
- Need high selectivity over silicide and photoresist
- Fluorine chemistry



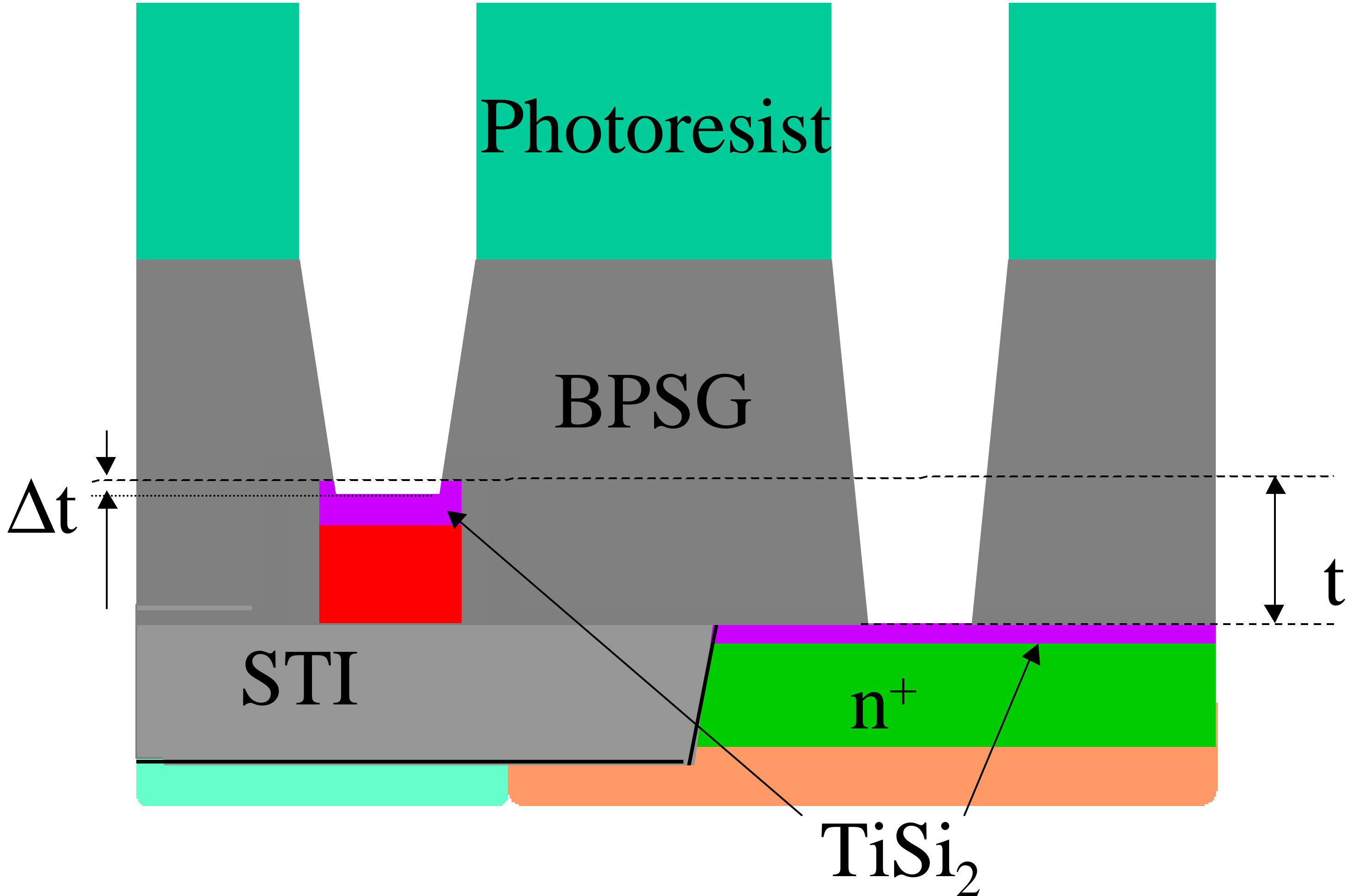
CMOS Cross-section



Challenge for Contact Etch

- Contact holes to polyside gate and local interconnection are about half of the depth of source/drain contact holes
- Require high (B)PSG to silicide selectivity

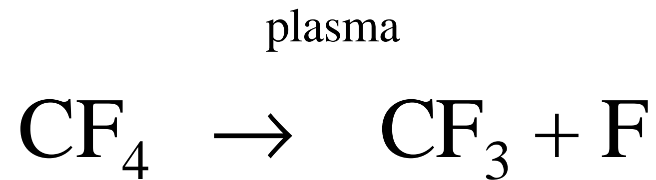
Contact Etch



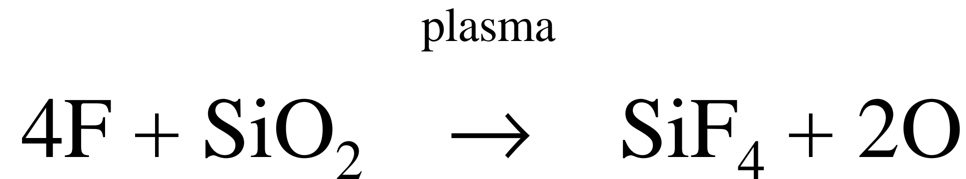
Contact Etch

- F/C ratio F/C > 3, etch dominant
  F/C < 2, polymerization
- When etching oxide, oxygen byproduct can react with C to free more fluorine
- When etching silicon or silicide, no oxygen releasing, fluorine is consumed, F/C ratio drop below 2 and start polymer deposition
- Polymer blocks further etch process
- High BPSG-to-$TiSi_2$ selectivity

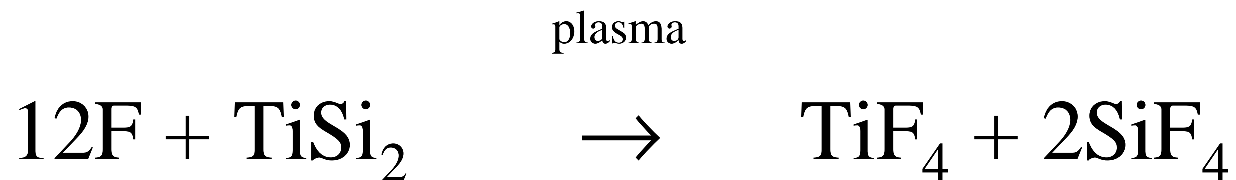
Dielectric Etch



$$CF_4 \xrightarrow{\text{plasma}} CF_3 + F$$

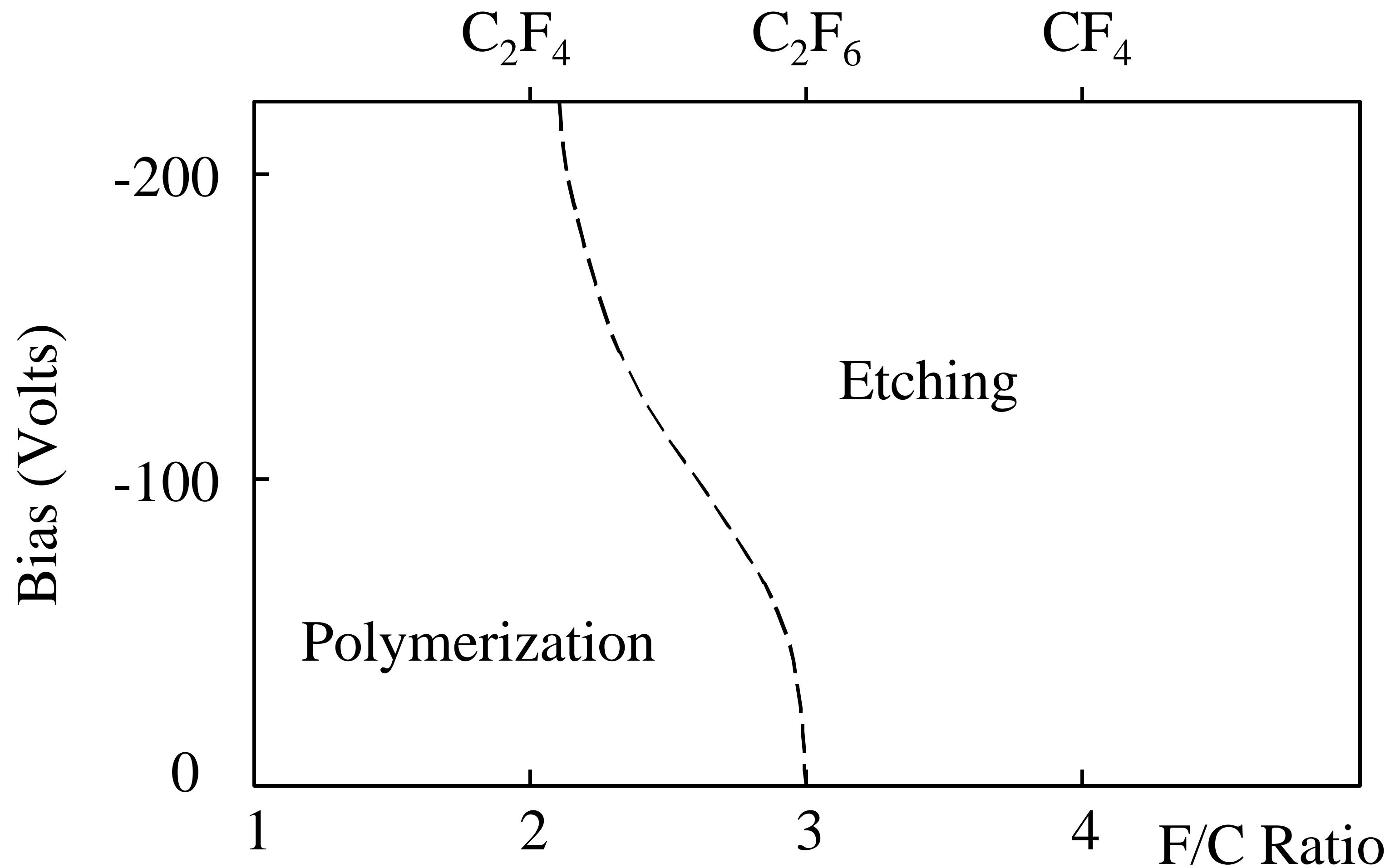


$$4F + SiO_2 \xrightarrow{\text{plasma}} SiF_4 + 2O$$



$$12F + TiSi_2 \xrightarrow{\text{plasma}} TiF_4 + 2SiF_4$$

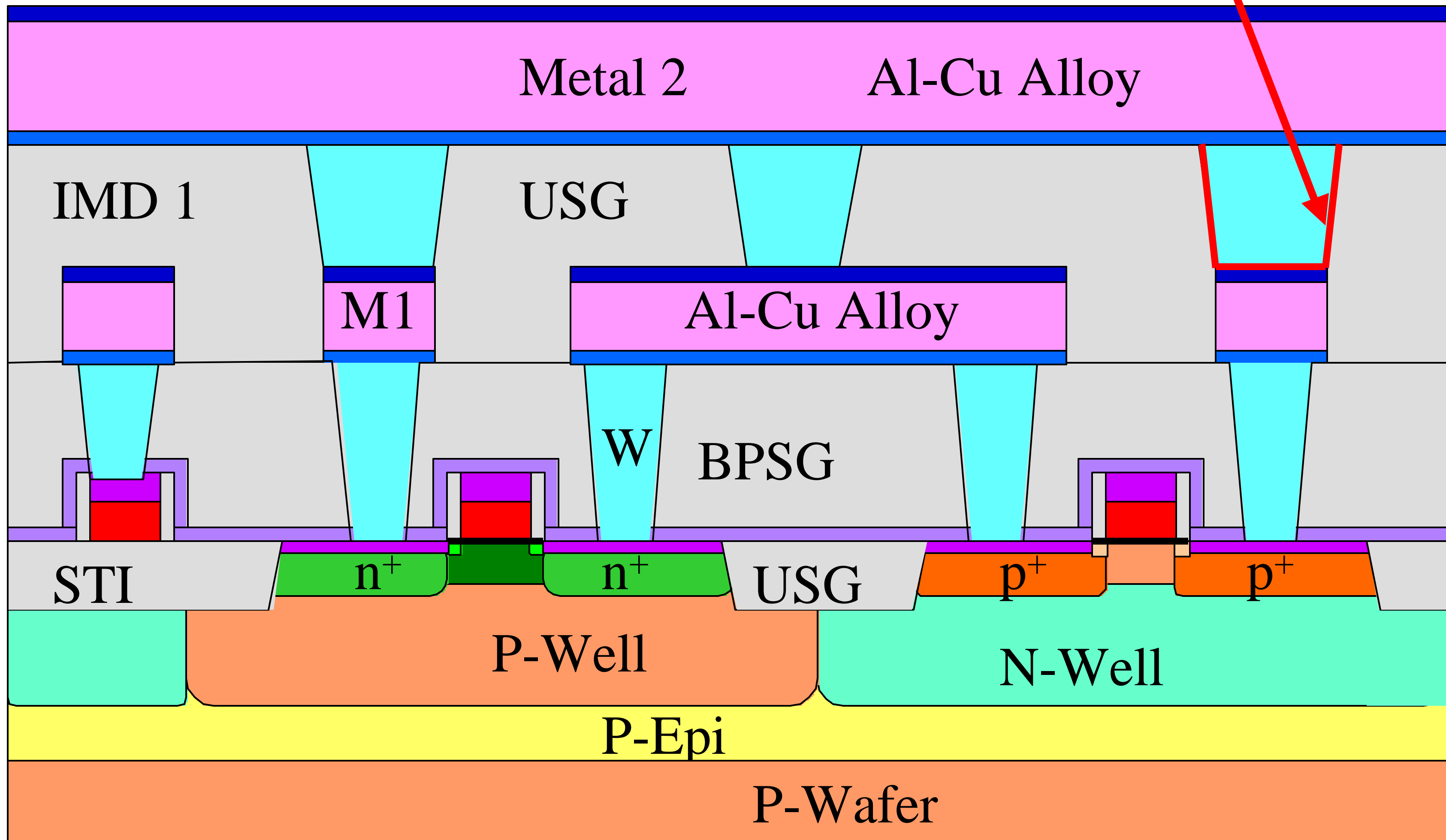
F/C Ratio, DC Bias and Polymerization



Via Etch

- Etch USG
- Open via hole for metal to metal interconnections
- Need high selectivity over metal and photoresist
- Fluorine chemistry

CMOS Cross-section



Etch Via

- PR mask
- Fluorine as the main etchant
- CF_4, CHF_3 and Ar are used for the etch process. O_2 or H_2 also can be used
- High selectivity over metal
- Avoiding metal sputtering
- Dual damascene etch

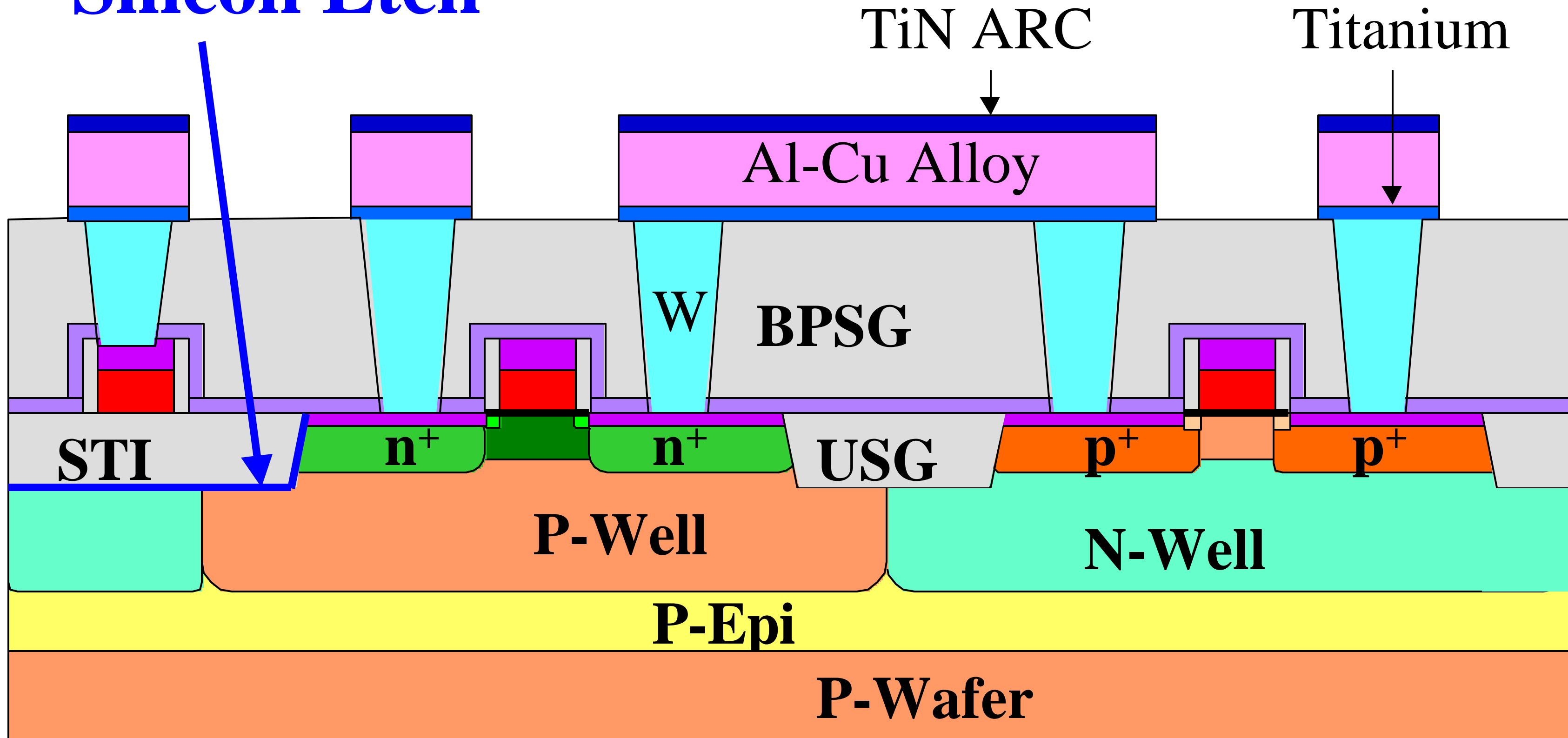
Summary of Dielectric Etch

Name of etch	Hard mask	Contact	Via	Bonding pad
Materials	Si_3N_4 or SiO_2	PSG or BPSG	USG or FSG	Nitride and oxide
Etchants	CF_4, CHF_3	CF_4, CHF_3, ...	CF_4, CHF_3, ...	CF_4, CHF_3, ...
Underneath layer	Si, Cu, Au,	Poly or silicide	Metal	Metal
Endpoints	CN, N or O	P, O, and F	O, Al and F	O, Al and F

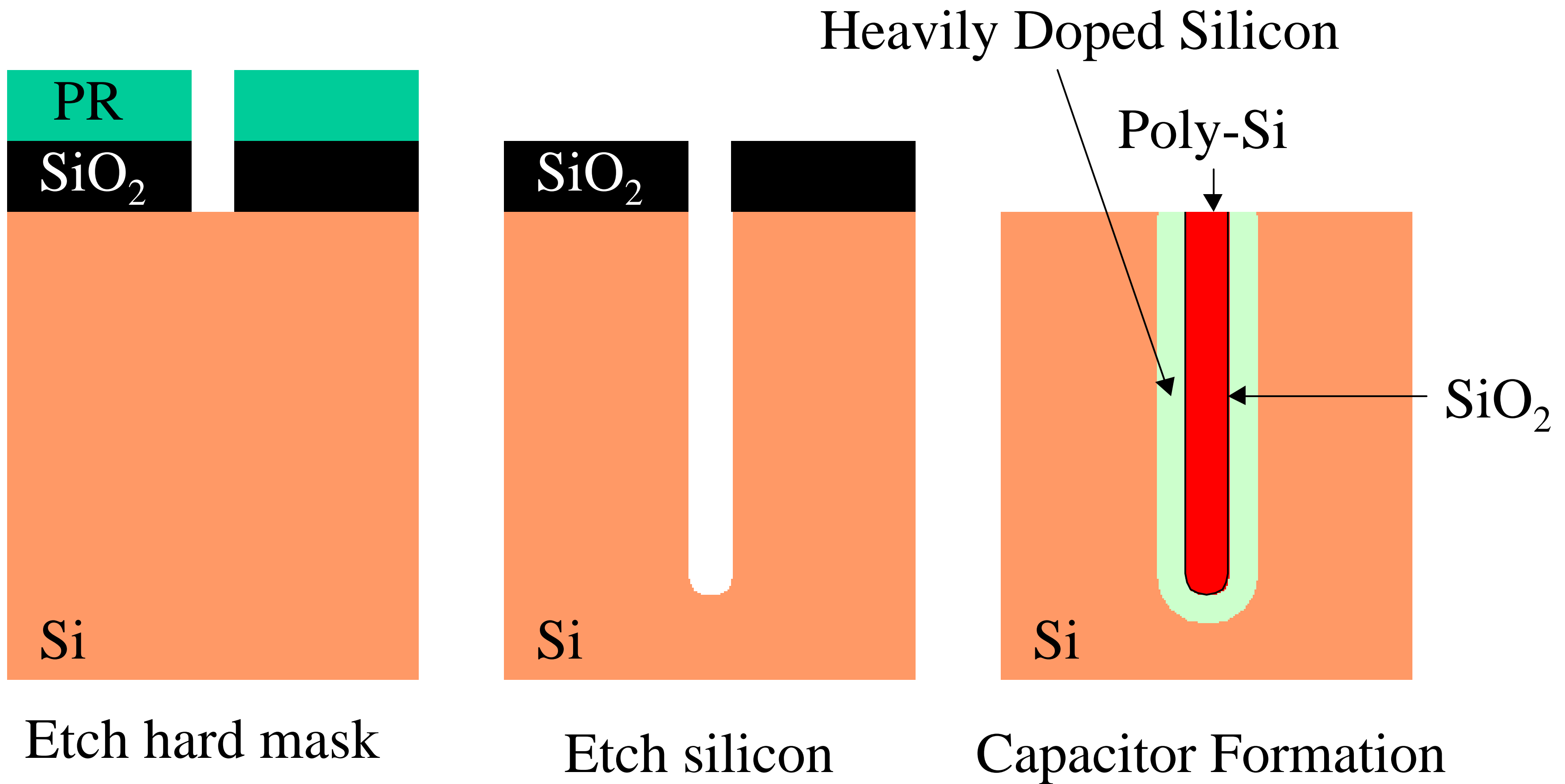
Single Crystal Silicon Etch

- Shallow trench isolation (STI)
- Deep trench for capacitor
- Hard mask, silicon nitride and oxide
- PR may cause substrate contamination
- Bromine chemistry
- HBr as the main etchant

CMOS Cross-Section



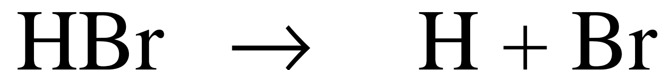
Deep Trench Capacitor

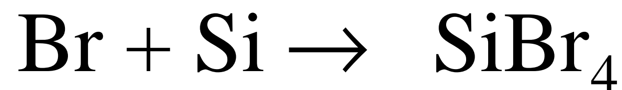


Some Facts About Bromine

Name	Bromine
Symbol	Br
Atomic number	35
Atomic weight	79.904
Discoverer	Antoine-J. Balard
Discovered at	France
Discovery date	1826
Origin of name	From the Greek word "bromos" meaning "stench"
Molar volume	19.78 cm^3
Velocity of sound	No data
Resistivity	$> 10^{18}$ μΩ cm
Refractive index	1.001132
Melting point	-7.2 C
Boiling point	59 C
Thermal conductivity	0.12 $W\ m^{-1}\ K^{-1}$
Applications	Free bromine as the main etchant for single crystal silicon etching processes
Source	HBr

Single Crystal Silicon Etch Chemistry





- Small amount O_2 for sidewall passivation
- A little NF_3 for preventing black silicon
- Endpoint by time

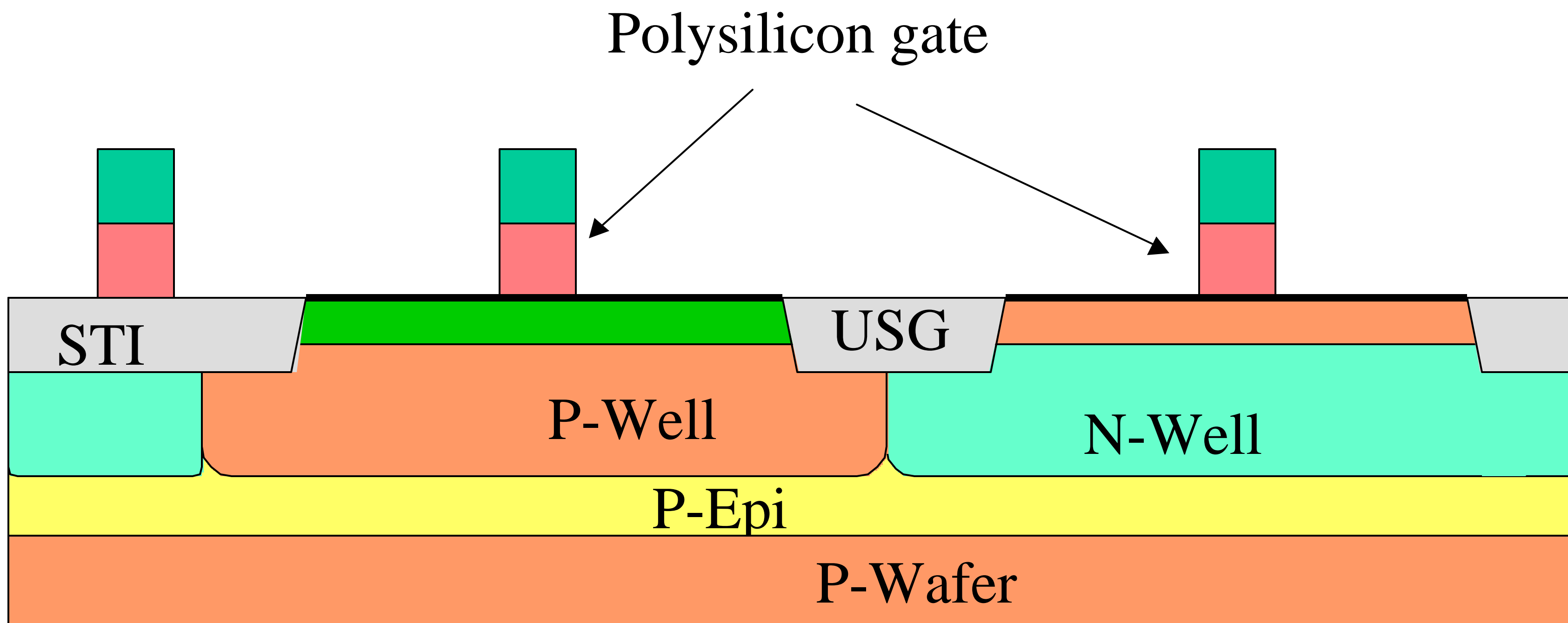
Polysilicon Etch

- Gates and local interconnections
  - Most critical etch process, smallest CD
- Capacitor electrodes for DRAM
- Require high selectivity over silicon dioxide
- Cl_2 chemistry

Some Facts About Chlorine

Name	Chlorine
Symbol	Cl
Atomic number	17
Atomic weight	35.4527
Discoverer	Carl William Scheele
Discovered at	Sweden
Discovery date	1774
Origin of name	From the Greek word "chloros" meaning "pale green"
Molar volume	17.39 cm^3
Velocity of sound	206 m/sec
Resistivity	$> 10^{10}$ μΩ cm
Refractive index	1.000773
Melting point	-101.4 C or 171.6 K
Boiling point	-33.89 C or 239.11 K
Thermal conductivity	0.0089 W m^{-1} K^{-1}
Applications	Used as the main etchant for poly silicon and metal etching processes. Polysilicon, epitaxy silicon deposition chamber clean.
Sources	Cl_2, HCl

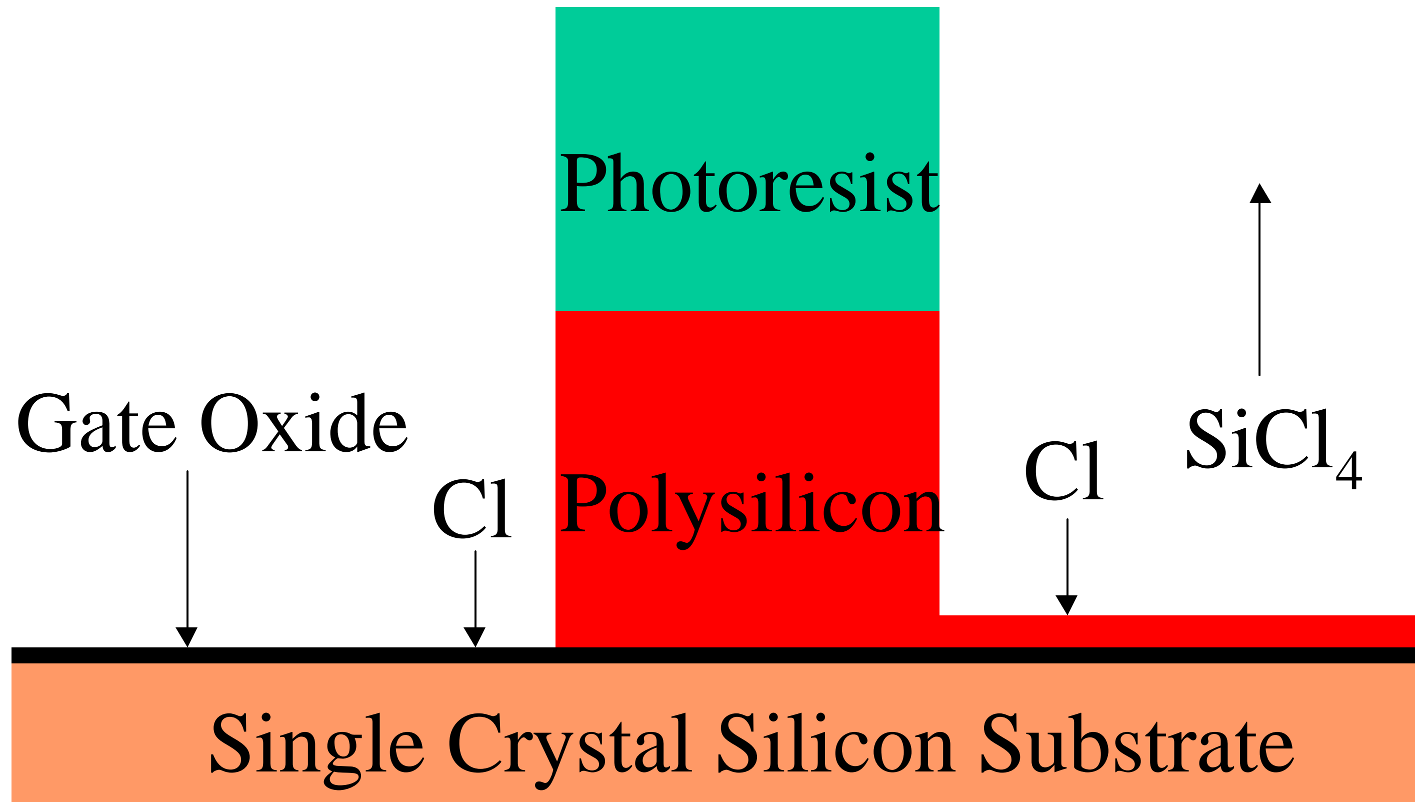
Gate etch



Polysilicon Etch

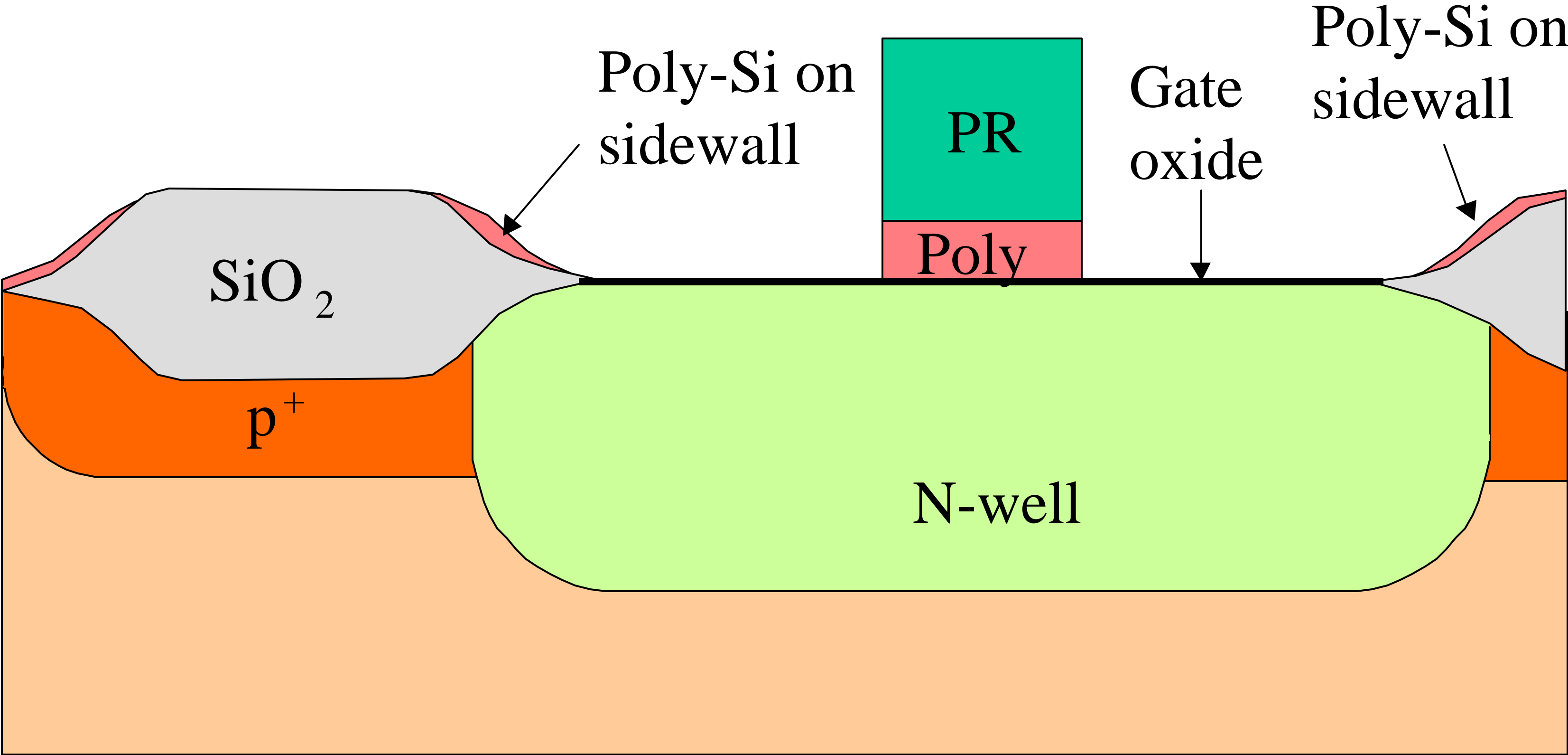
- Cl_2 as the main etchant
- HBr for sidewall passivation, blocking mechanism
- Add O_2 in over etch step to improve selectivity to SiO_2.
- High selectivity over SiO_2 is required

Polysilicon Etch



- High poly-to-oxide selectivity is required

Polysilicon Etch



Polysilicon Etch

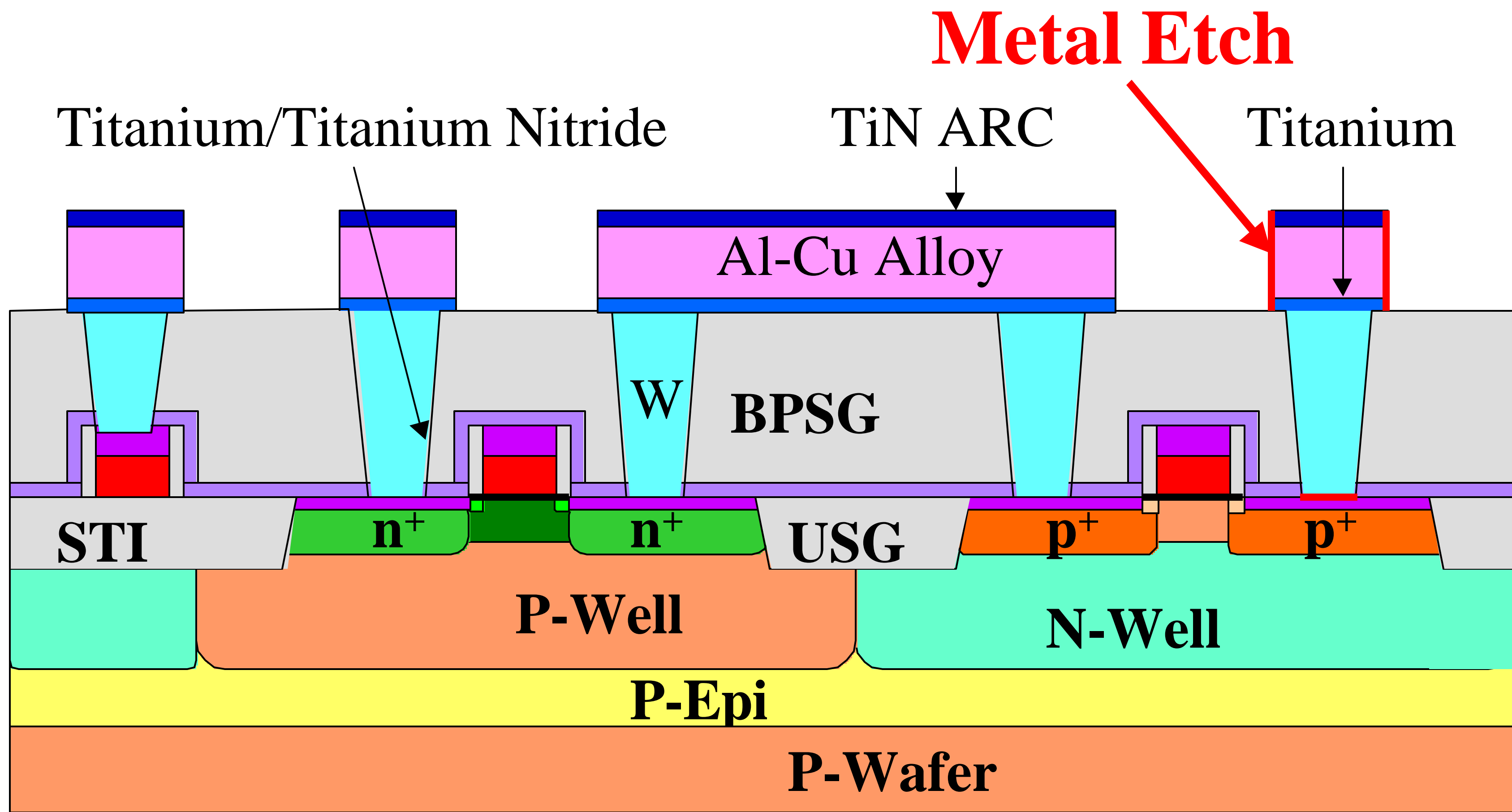
Process steps:

- Breakthrough
  - Removal of native oxide, energetic Ar^+ bombardment
- Main etch
  - High poly etch rate, Cl and HBr chemistry
  - Endpoint on O line
- Over etch
  - Reduce power, add O_2 for high selectivity over SiO_2

Metal Etch

- Etch TiN/Al·Cu/Ti metal stack to form metal interconnection
- Usually use $Cl_2 + BCl_3$ chemistry
- Need etch away Cu in Al either physically or chemically
- Need strip photoresist before wafer exposure to moisture in atmosphere

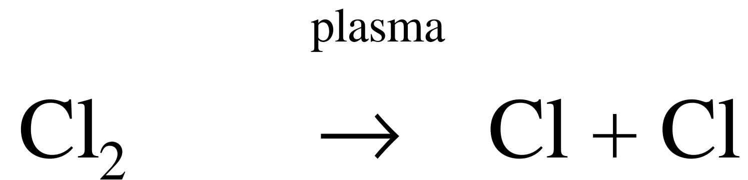
CMOS Cross-section

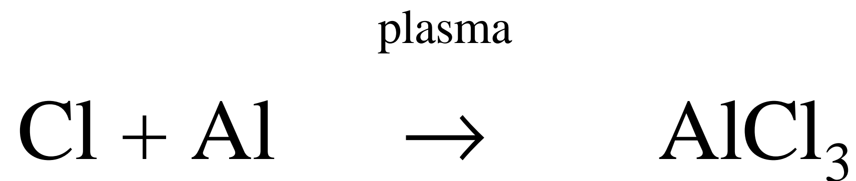


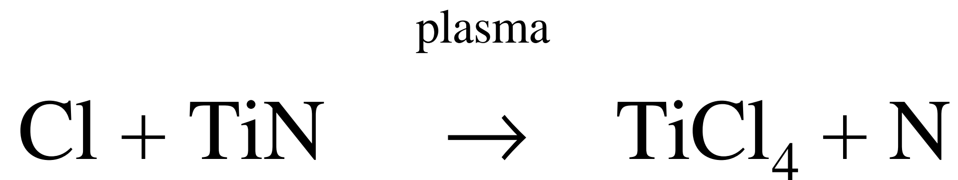
Etch Metal

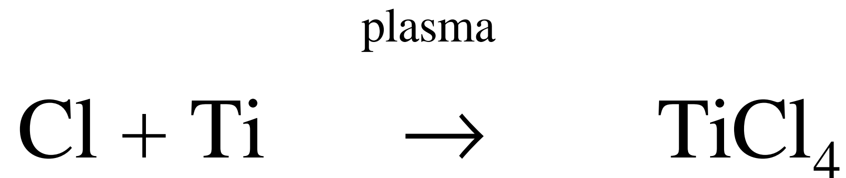
- For metal interconnection
- Metal stack: TiN/Al•Cu/Ti
- Cl_2 as the main etchant
- BCl_3, N_2 are used for sidewall passivation
- O_2 is used to improve selectivity to oxide
- Main challenges: etch profile and avoiding etch residue
- Metal grain size can affect etch process

Metal Etch Chemistries







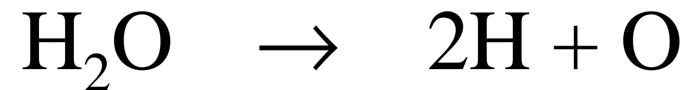


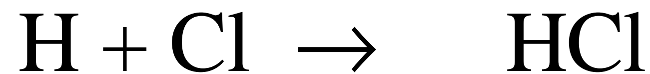
Photoresist Dry Strip

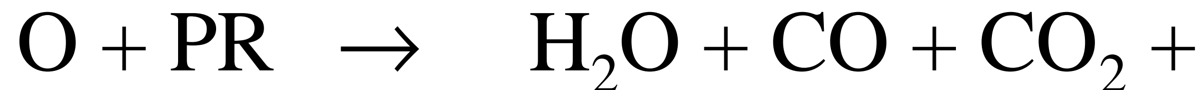
- Remote plasma source
  - Free radicals without ion bombardment
- High pressure, microwave plasma
- Very important to strip chlorine containing PR after metal etch to avoid metal corrosion
- In-situ with etch process in a cluster tool
- Improve throughput and yield

Photoresist Dry Strip

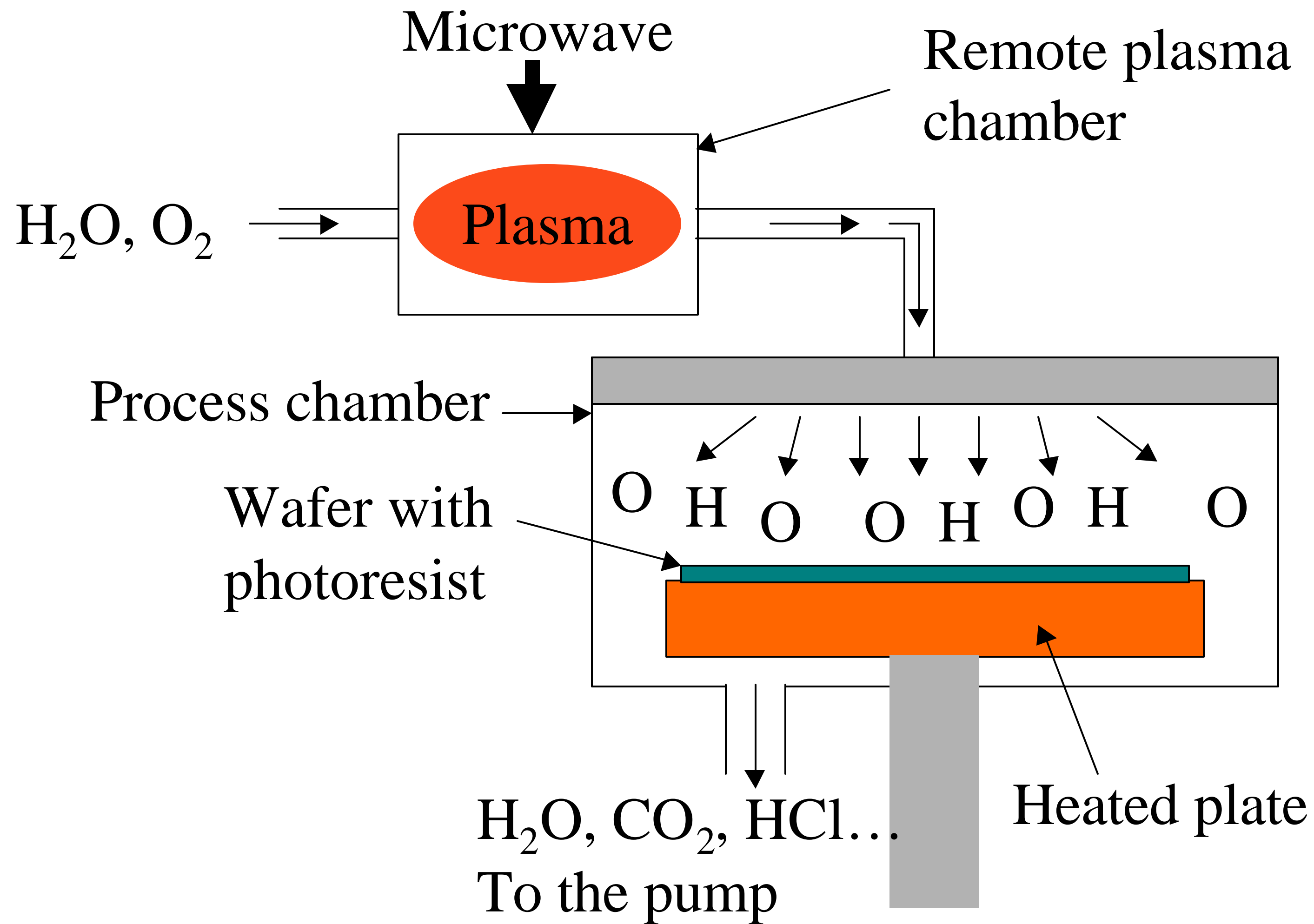
- O_2, H_2O chemistry







Photoresist Strip Process



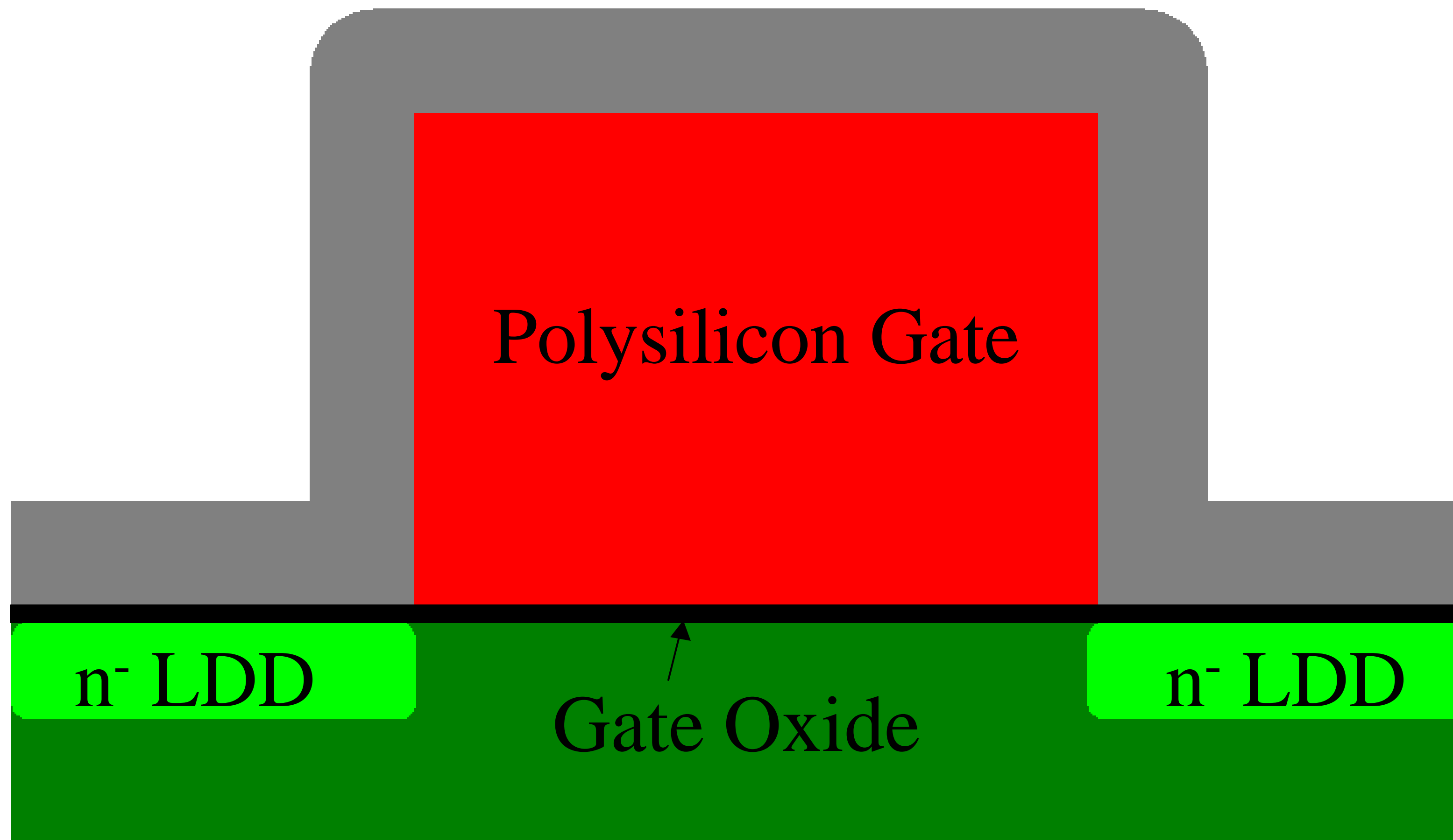
Dry Chemical Etch

- Unstable gases, such as XeF_2 and O_3
- Remote plasma source free radicals
- Free from ion bombardment
- Thin film strip and wineglass contact etch
- In-situ with RIE chambers on one frame
- Nitride strip in both LOCOS and STI
- Nitride and Poly-Si strip in PBL

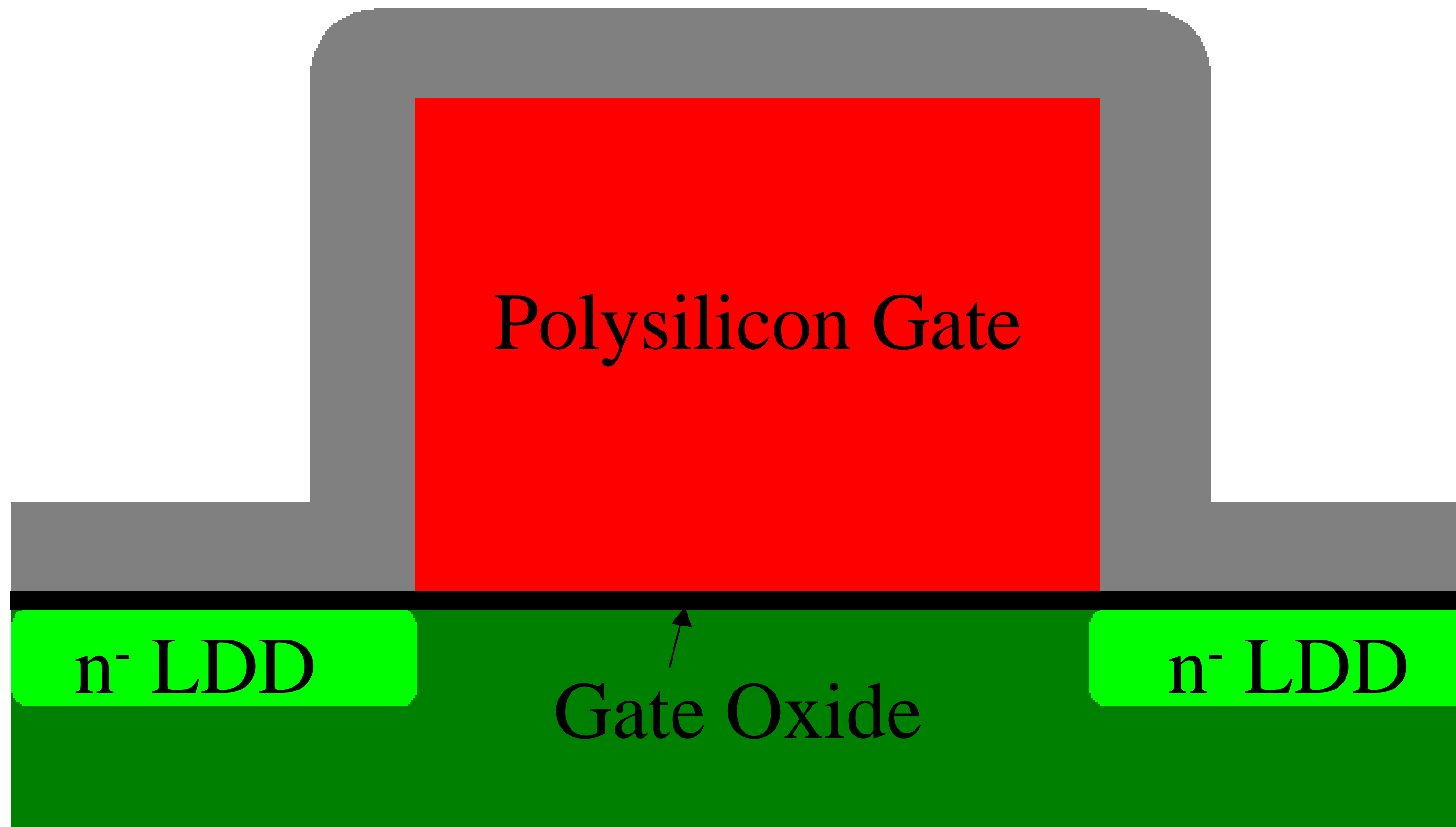
Blanket Dry Etch

- No photoresist. Etchback and film strip.
- Argon sputtering etch
  - Dielectric thin film applications
  - native oxide clean prior to metal deposition
- RIE etchback system
  - Can be used in-line with dielectric CVD tools
  - Sidewall spacer formation
  - PR or SOG planarization etchback

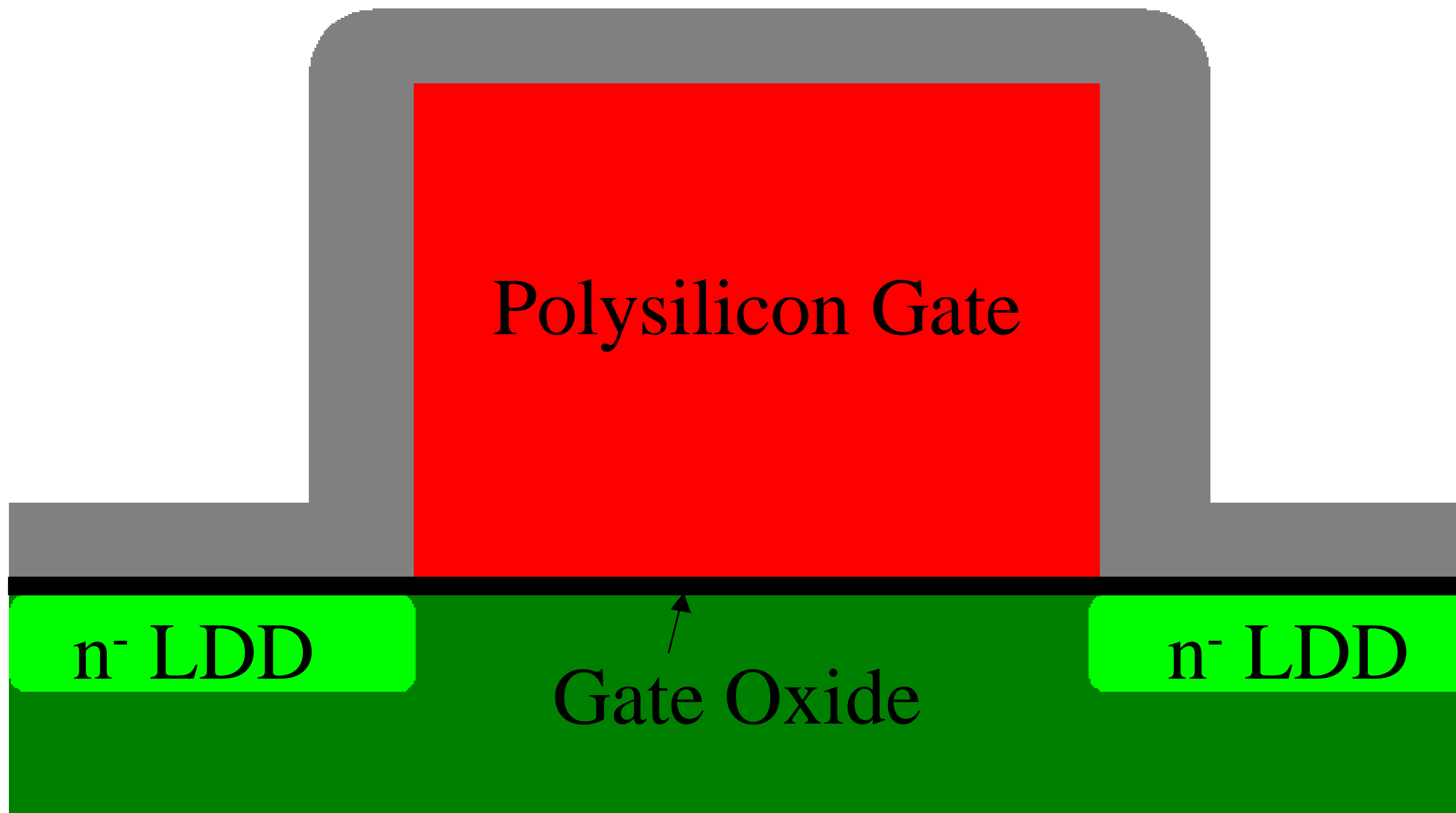
CVD O_3-TEOS USG



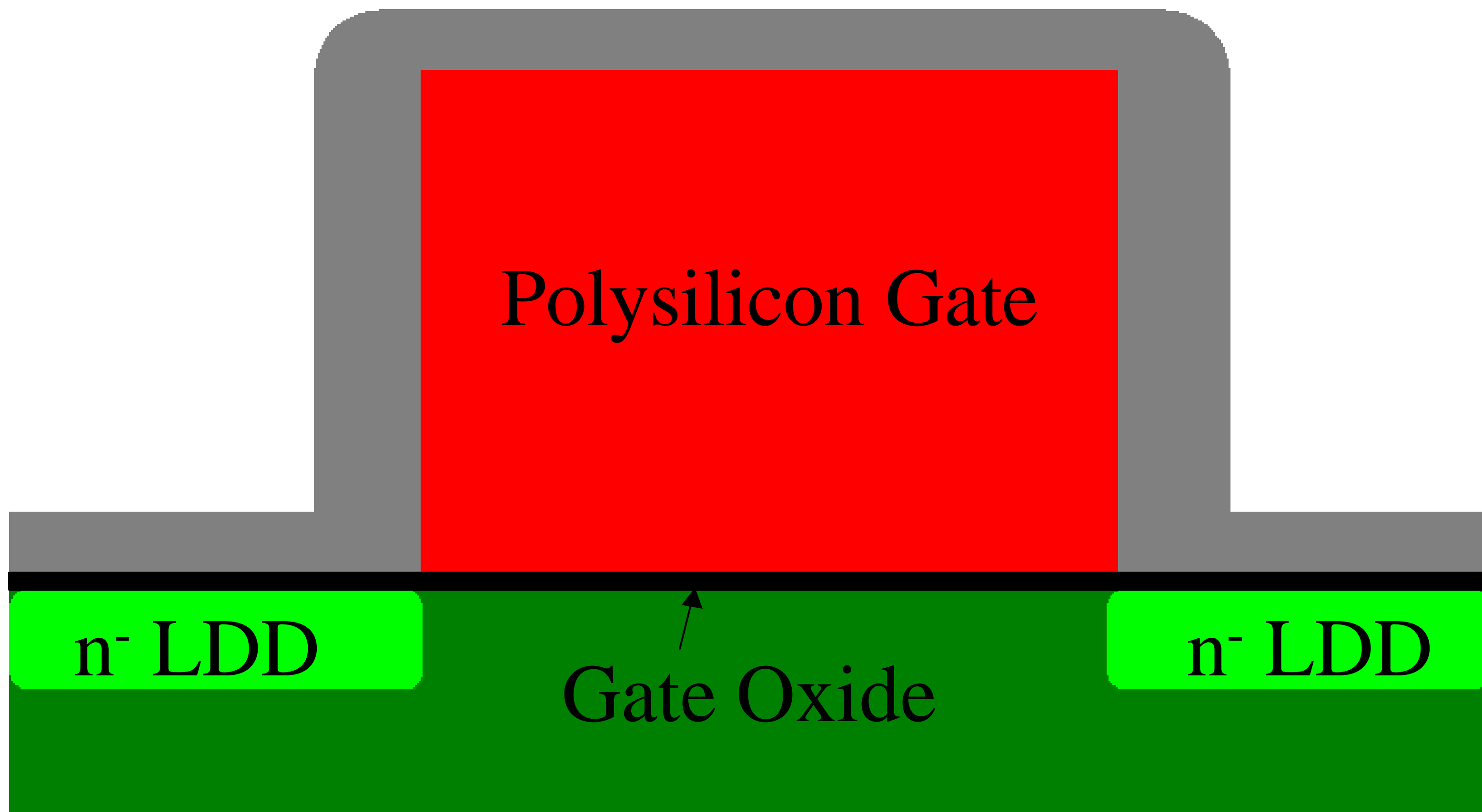
O_3-TEOS USG Etchback



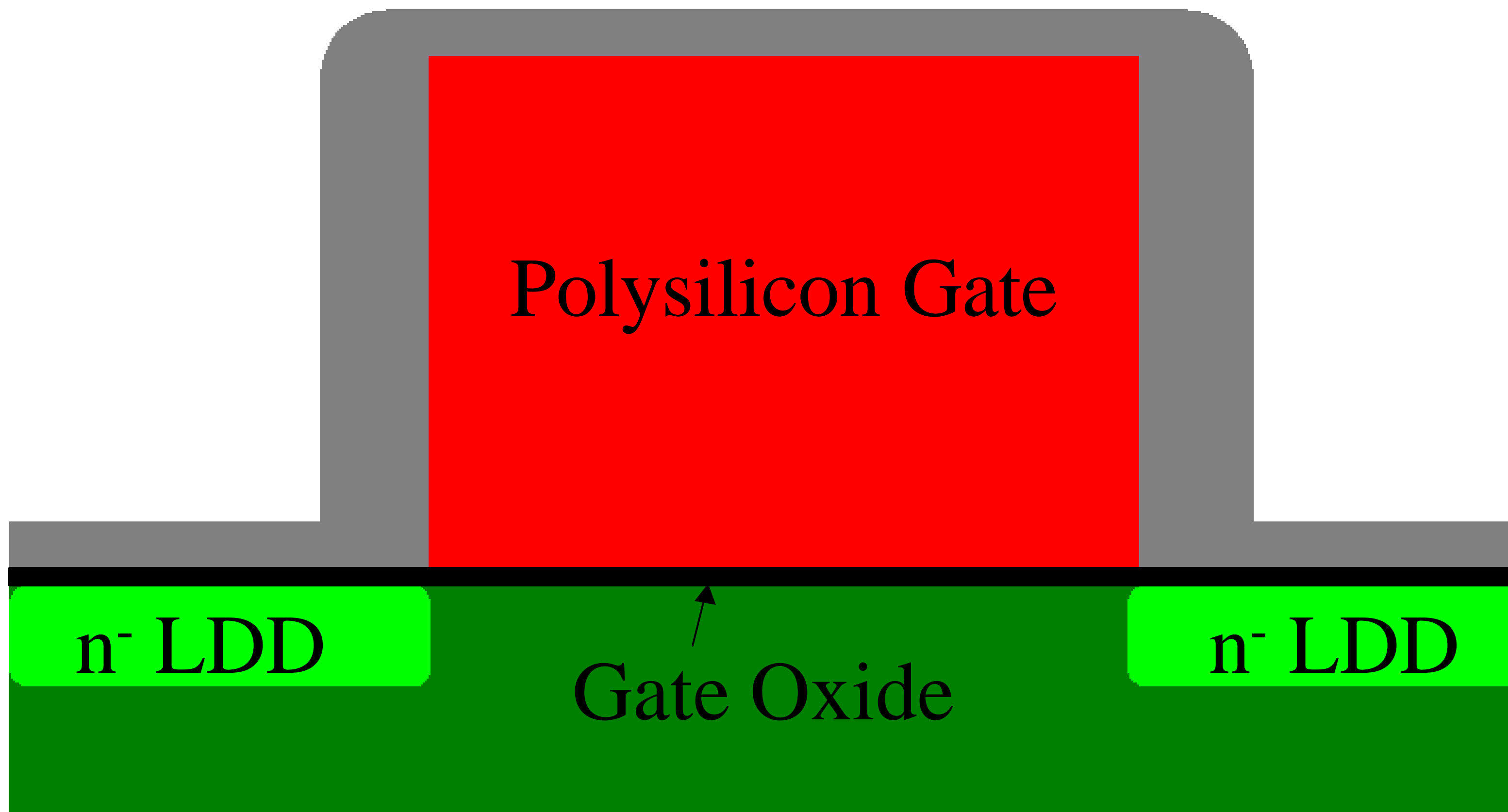
O_3-TEOS USG Etchback



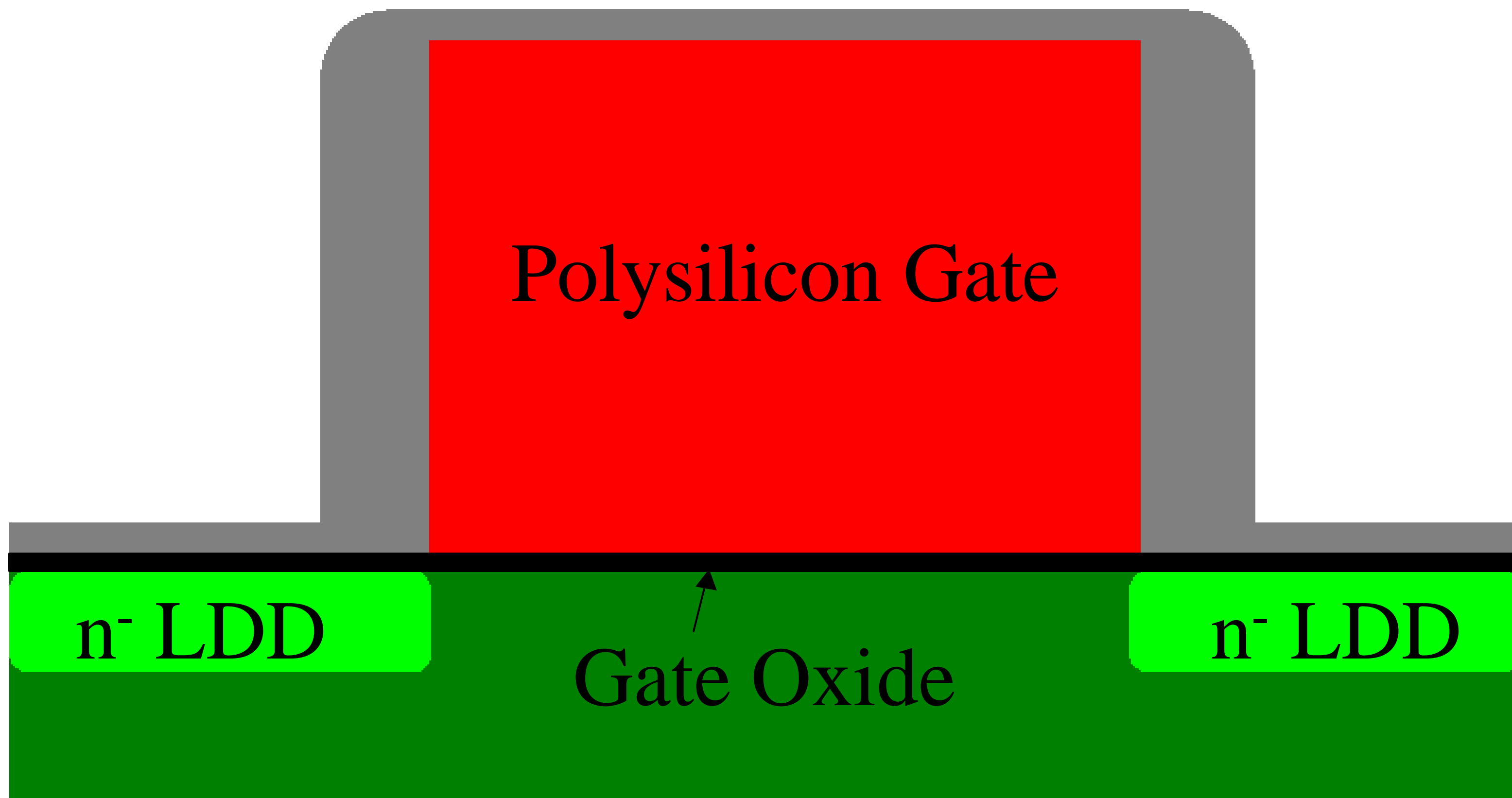
O_3-TEOS USG Etchback



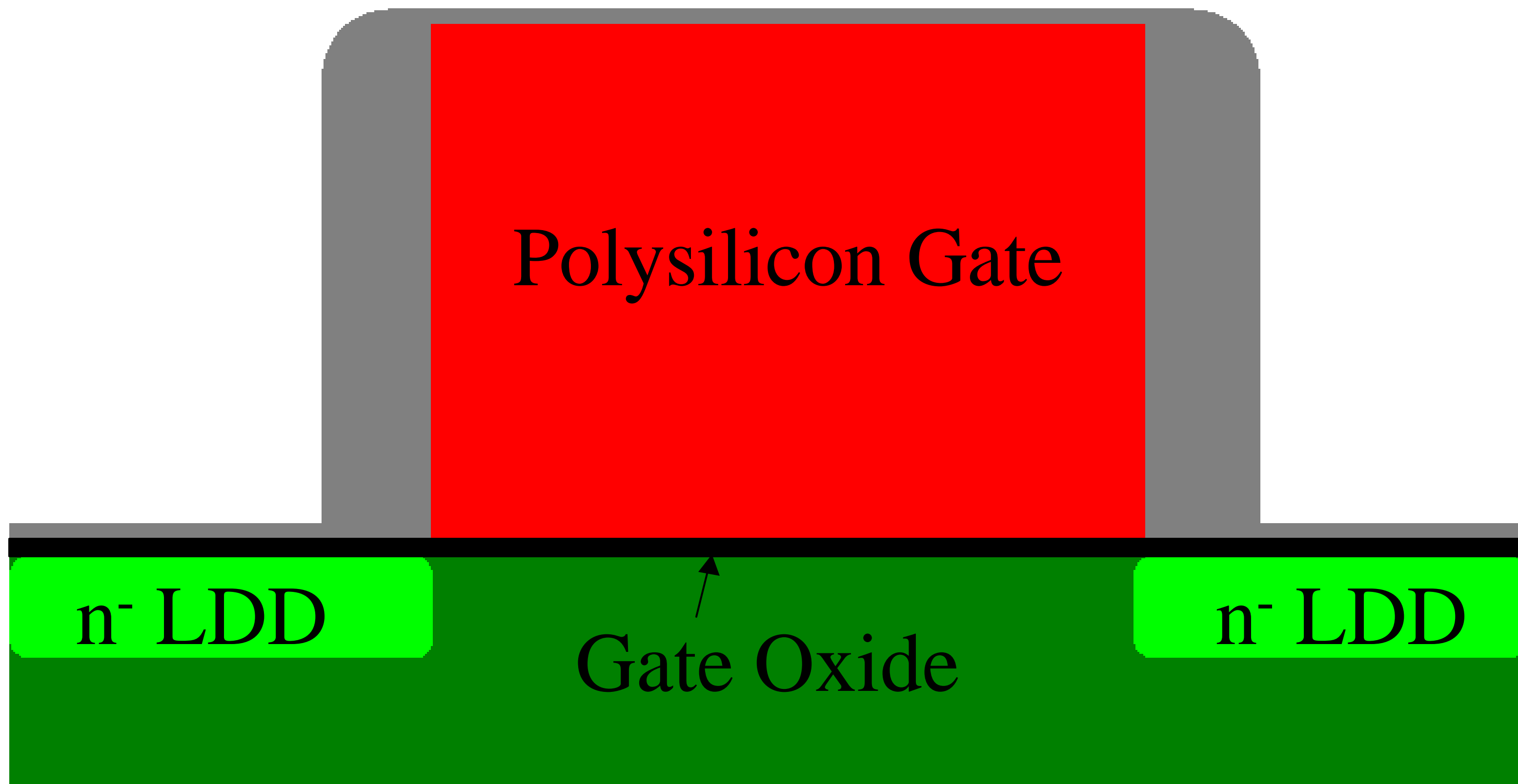
O_3-TEOS USG Etchback



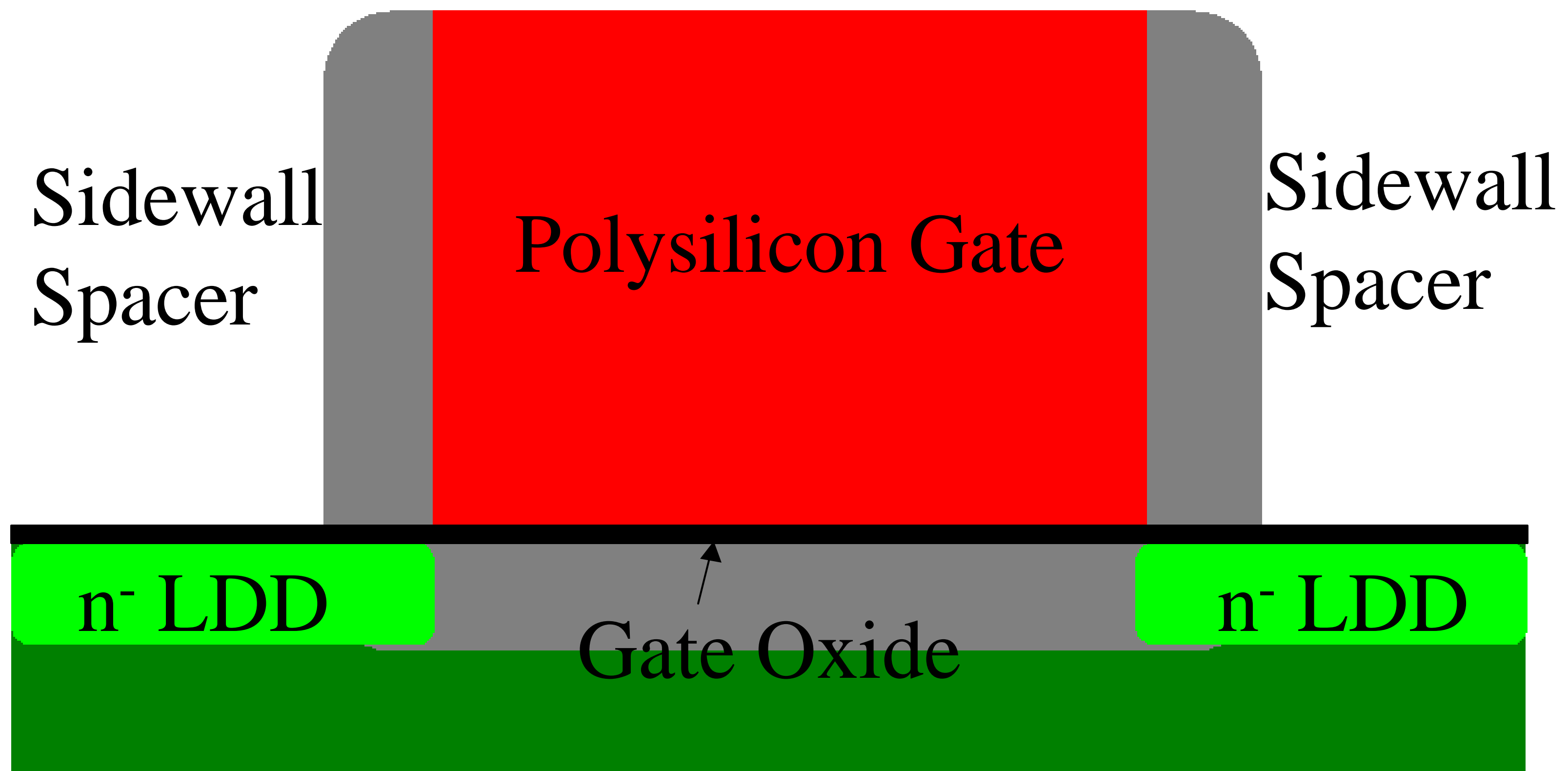
O_3-TEOS USG Etchback



O_3-TEOS USG Etchback



O_3-TEOS USG Etchback



Etch Safety

- Corrosive and toxic gases
  - Cl_2, BCl_3, SiF_4 and HBr
  - Could be fatal if inhalation at a high concentration (>1000 ppm)
- RF power can cause electric shock
- Can be lethal at high power

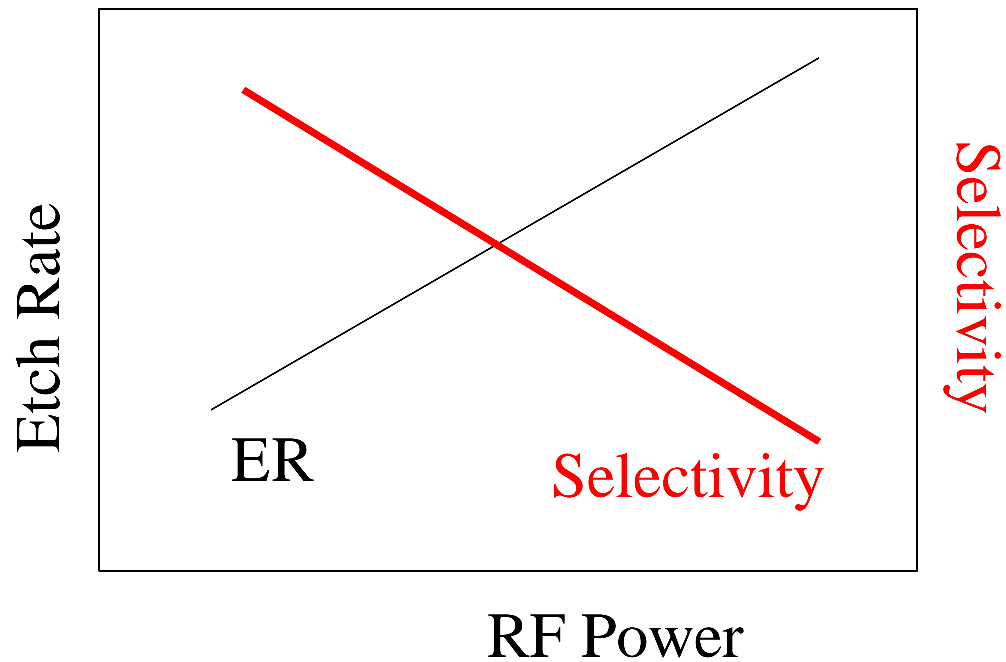
Etch Safety

- All moving parts, are mechanical hazards
- May cause injury if one does not stay clear
- Lock-out, tag-out

RF Power

- Increasing RF power increases ion density, ion bombardment energy, and number of free radicals
- Etch rate will increase significantly
- The most important “knob” that controls etch rate
- Check RF system first if etch rate is out of specifications

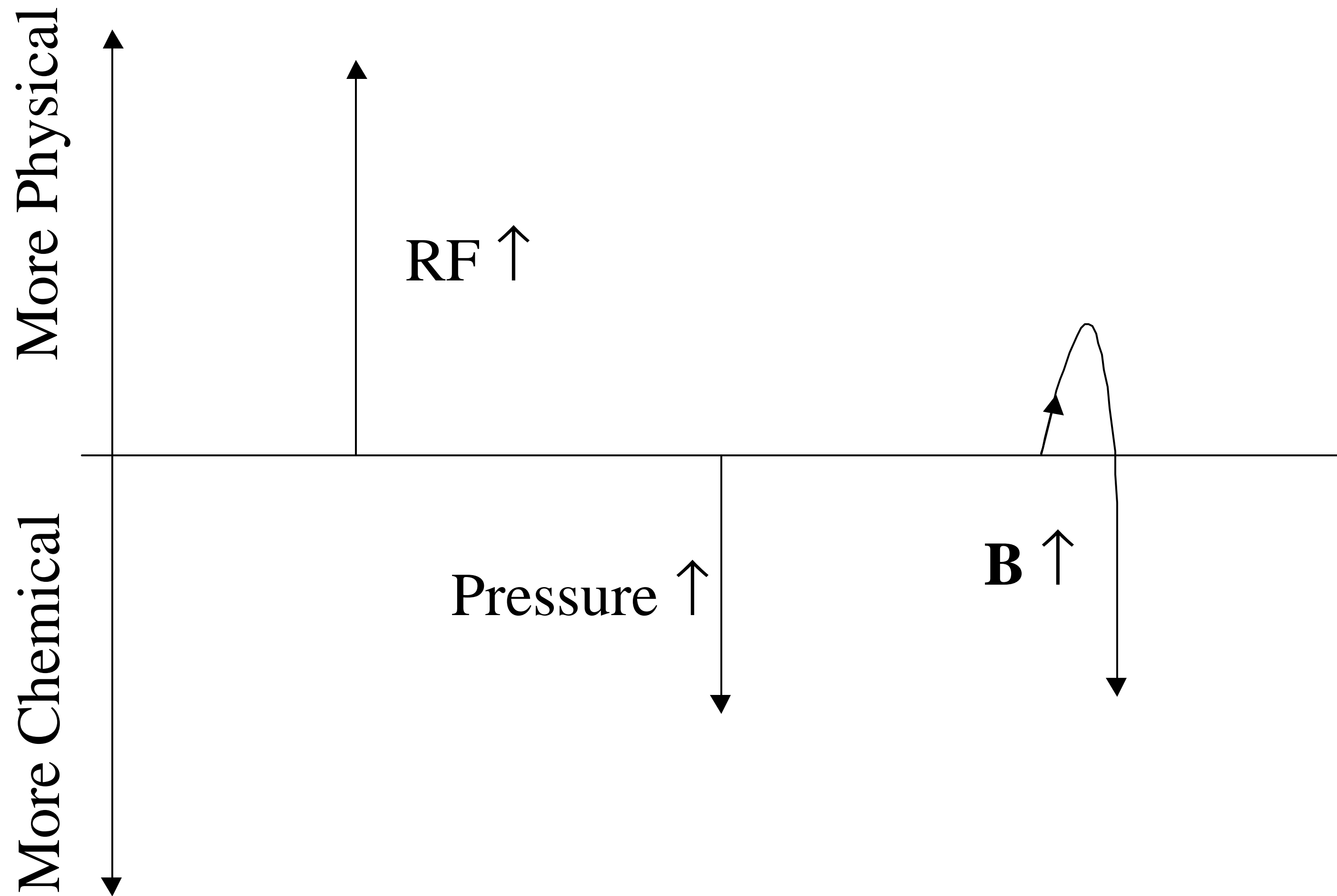
Plasma Etch Trends



Pressure

- Pressure affects plasma density and shape
- Has strong effects on etch uniformity

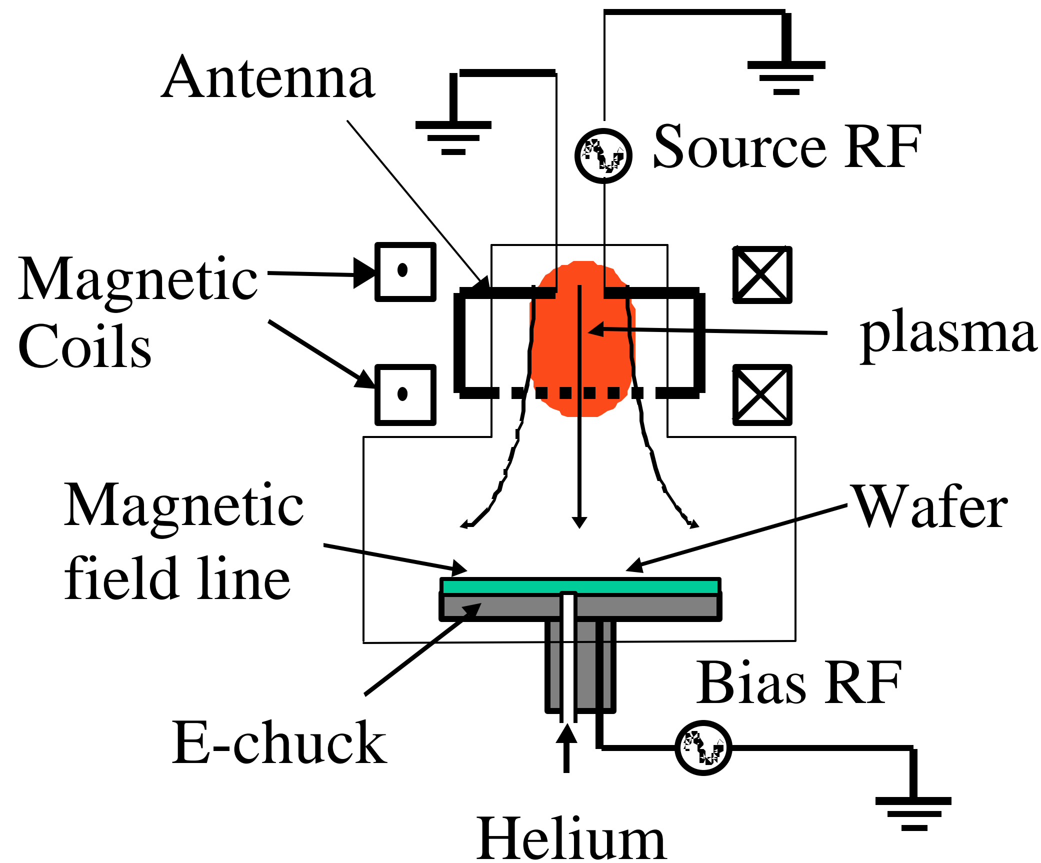
Etch Trends



Future Trends for Etch Processes

- High density plasma (HDP) at low pressure
  - Improve profile control
  - Increasing plasma density
  - Ion bombardment flux
- Independent ion flux and ion energy control
- HDP etchers in IC processing: ICP & ECR
- Helicon plasma source: ~100% ionization, candidate for future etch chamber design

Helicon Plasma Source



Future Trends for Etch Processes

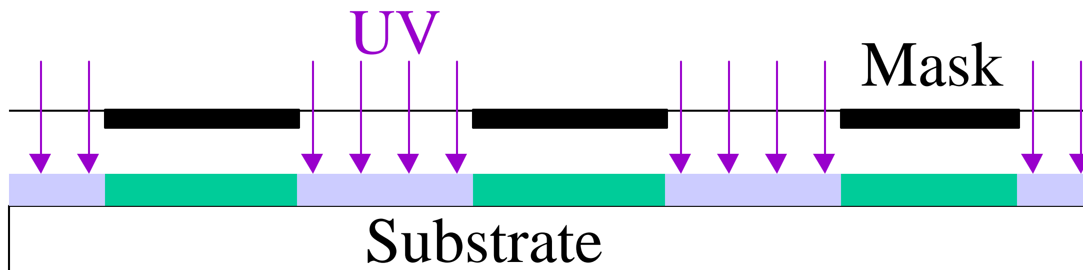
- 300 mm system
- Plasma uniformity control
- Plasma position control

Copper Etch?

- Cl_2 chemistry
- Low pressure (< 5 mTorr)
- High temperature (>250 °C)
  - Cannot use photoresist
  - Need CVD oxide hard mask
- Competition with dual damascene process
- Very unlike can be used in IC production

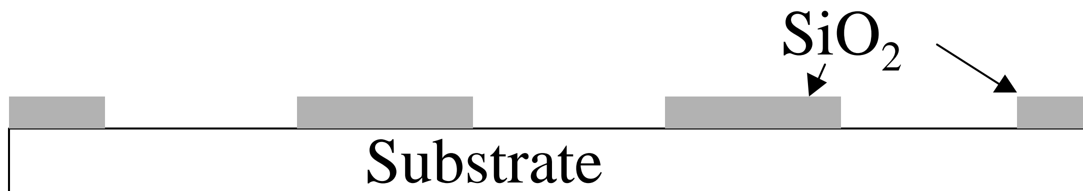
Direct Hard Masking Photolithography

PECVD Si-PR



Exposure, partially oxidation of Si-PR

Cl_2 plasma removes unexposed Si-PR



Down Stream O_2 fully oxidation of Si-PR

Future Trends

- Challenges ahead:
- Etch high-κ materials of gate dielectric and capacitor dielectric
- Etch low-κ materials of inter-metal dielectric

Summary

- Plasma etch is widely used for patterned etch process to transfer image on photoresist to surface materials.
- Epi, poly, oxide and metal
- Fluorine for oxide etch
- HBr for single crystal silicon etch
- Chlorine for polysilicon and metal etch

Summary

- Certain vacuum and constant RF power are need to strike and maintain a stable plasma
- RF power is main knob to control etch rate
- Pressure affects uniformity and etch profile
- High plasma density at low pressure are desired for etch deep sub-micron features.
- Dry chemical etch can be achieved with remote plasma source

Chapter 10
CVD and Dielectric Thin Film

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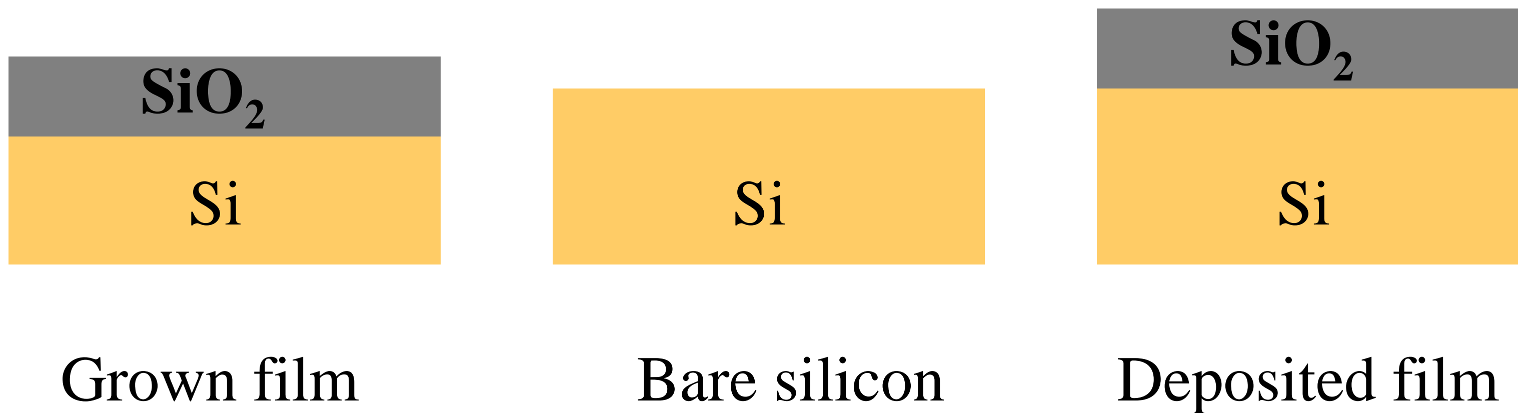
Objectives

- Identify at least four CVD applications
- Describe CVD process sequence
- List the two deposition regimes and describe their relation to temperature
- List two dielectric thin films
- Name the two most commonly used silicon precursors for dielectric CVD

CVD Oxide vs. Grown Oxide



CVD Oxide vs. Grown Oxide

Grow

- Oxygen is from gas phase
- Silicon from substrate
- Oxide grow into silicon
- Higher quality

CVD

- Both oxygen and silicon are from gas phase
- Deposit on substrate surface
- Lower temperature
- Higher growth rate

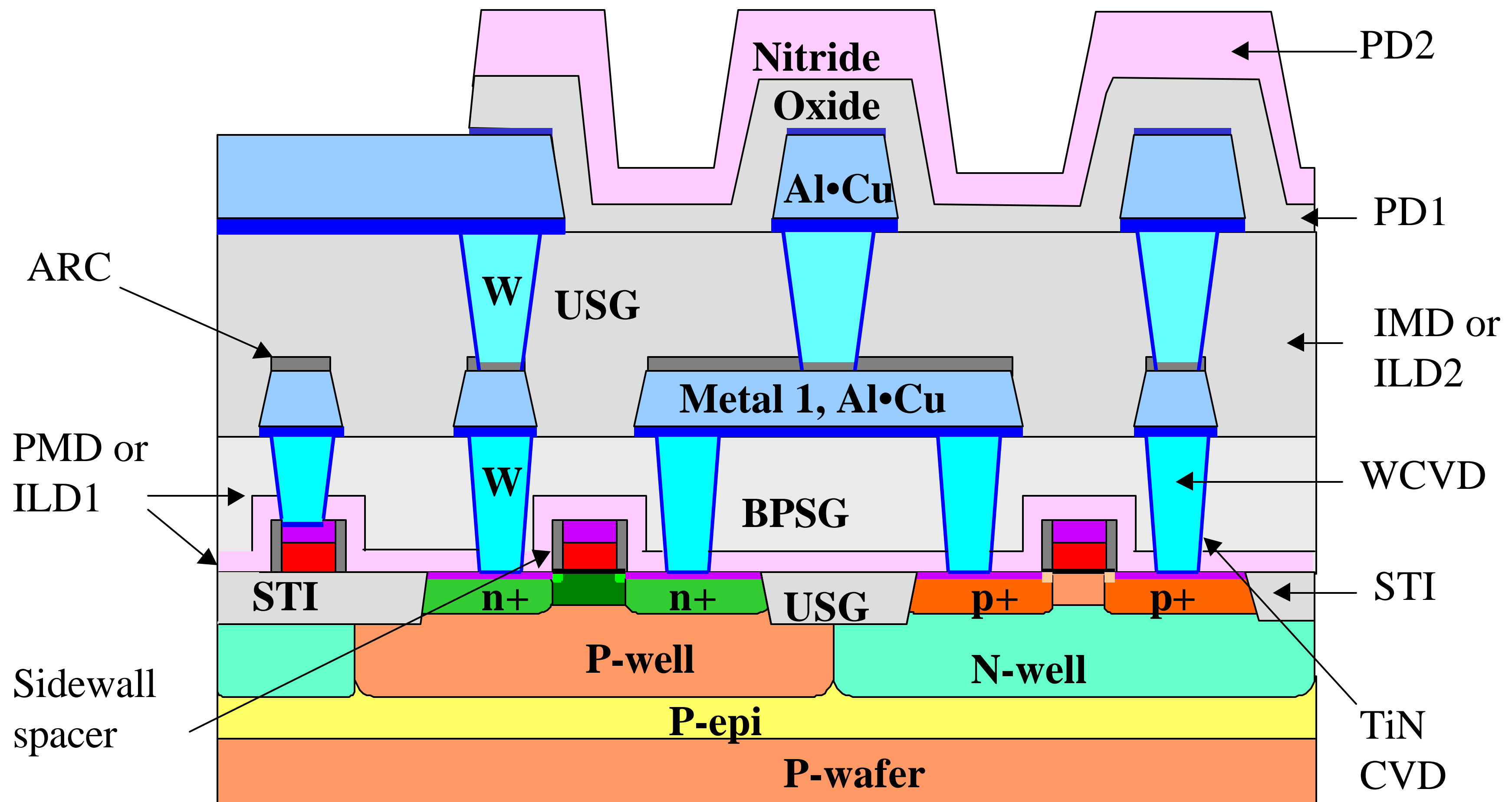
Dielectric Thin Film Applications

- Multi-level metal interconnection
- CVD and SOG plus CVD dielectrics
- Shallow trench isolation (STI)
- Sidewall spacer for salicide, LDD, and the source/drain diffusion buffer
- The passivation dielectric (PD)
- Dielectric ARC for feature size < 0.25 μm

Dielectric Thin Film Applications

- Inter layer dielectric, or ILD, include PMD and IMD
- Pre-metal dielectric: PMD
  - normally PSG or BPSG
  - Temperature limited by thermal budget
- Inter-metal dielectric: IMD
  - USG or FSG
  - Normally deposited around 400 °C

Figure 10.2



Dielectric Processes

An N-layer metal interconnection IC chip with STI, the minimum number of dielectric process is:

Dielectric layer	=	1	+ 1	+ 1	+ (N−1)	+ 1	=	N + 3
		STI	spacer	PMD	IMD	PD		

CVD

- Chemical Vapor Deposition
- Chemical gases or vapors react on the surface of solid, produce solid byproduct on the surface in the form of thin film. Other byproducts are volatile and leave the surface.

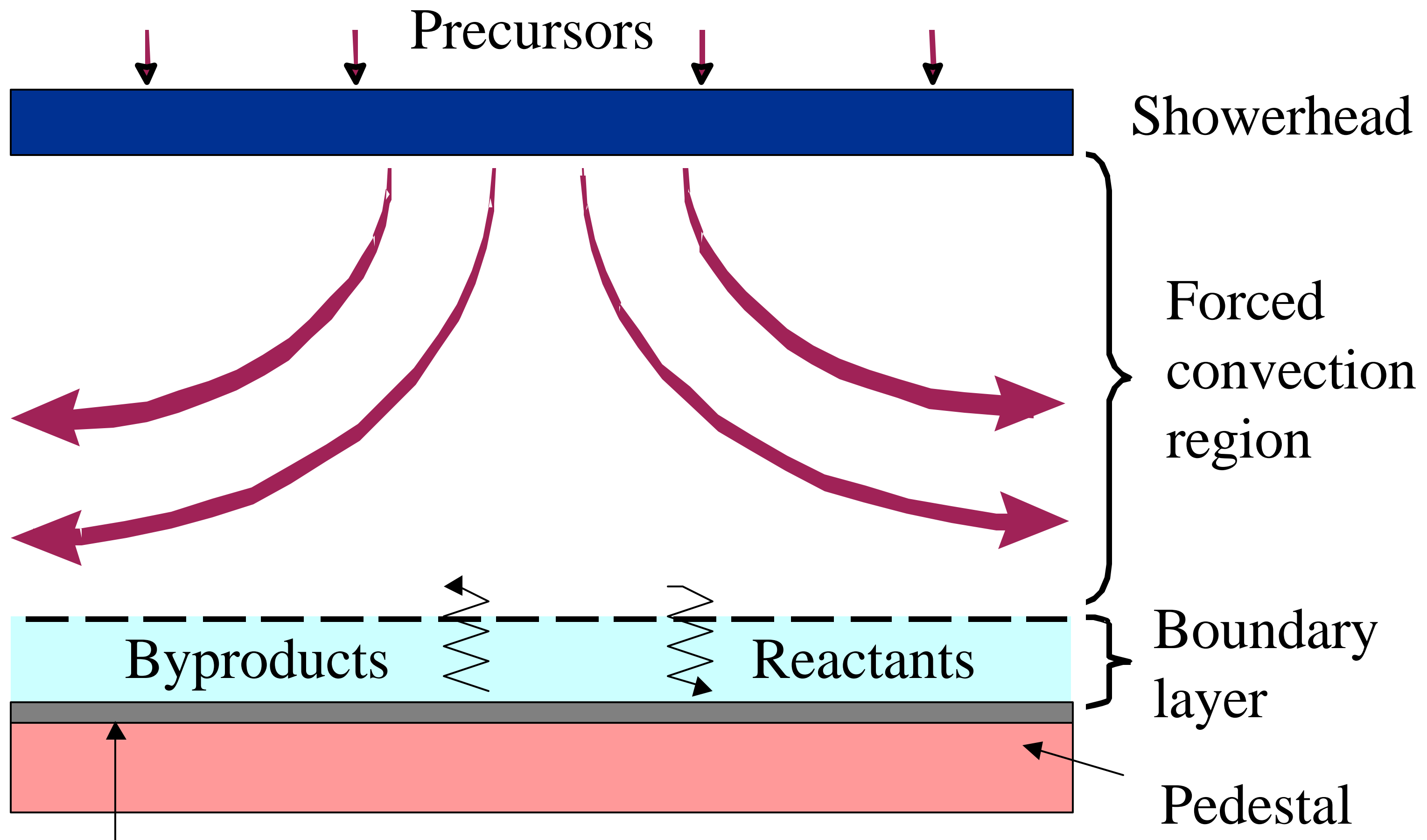
CVD Applications

	FILMS	*PRECURSORS*
Semiconductor	Si (poly) Si (epi)	SiH_4 (silane) $SiCl_2H_2$ (DCS) $SiCl_3H$ (TCS) $SiCl_4$ (Siltet)
Dielectrics	SiO_2 (glass)	LPCVD SiH_4, O_2 PECVD SiH_4, N_2O PECVD $Si(OC_2H_5)_4$ (TEOS), O_2
		LPCVD TEOS APCVD&SACVD™ TEOS, O_3 (ozone)
	Oxynitride	SiH_4, N_2O, N_2, NH_3
	Si_3N_4	PECVD SiH_4, N_2, NH_3 LPCVD SiH_4, N_2, NH_3 LPCVD $C_8H_{22}N_2Si$ (BTBAS)
Conductors	W (Tungsten) WSi_2 TiN Ti Cu	WF_6 (Tungsten hexafluoride), SiH_4, H_2 WF_6 (Tungsten hexafluoride), SiH_4, H_2 $Ti[N(CH_3)_2]_4$ (TDMAT) $TiCl_4$

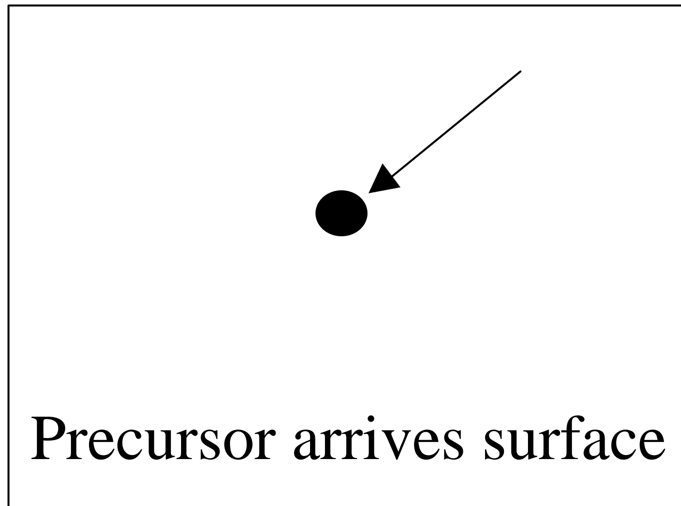
CVD

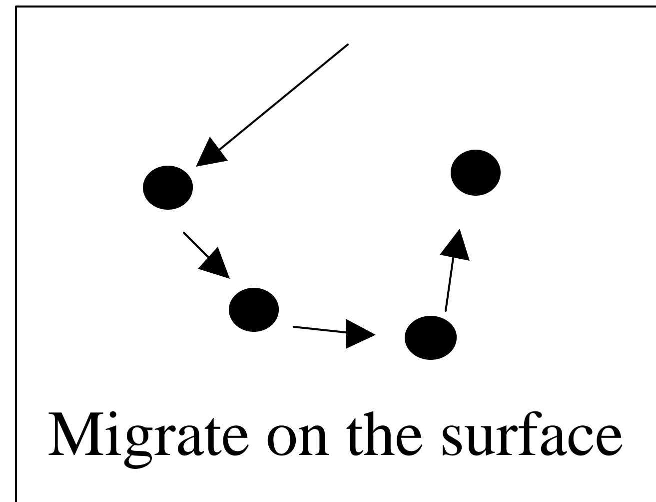
- Gas or vapor phase precursors are introduced into the reactor
- Precursors across the boundary layer and reach the surface
- Precursors adsorb on the substrate surface
- Adsorbed precursors migrate on the substrate surface
- Chemical reaction on the substrate surface
- Solid byproducts form nuclei on the substrate surface
- Nuclei grow into islands
- Islands merge into the continuous thin film
- Other gaseous byproducts desorb from the substrate surface
- Gaseous byproducts diffuse across the boundary layer
- Gaseous byproducts flow out of the reactor.

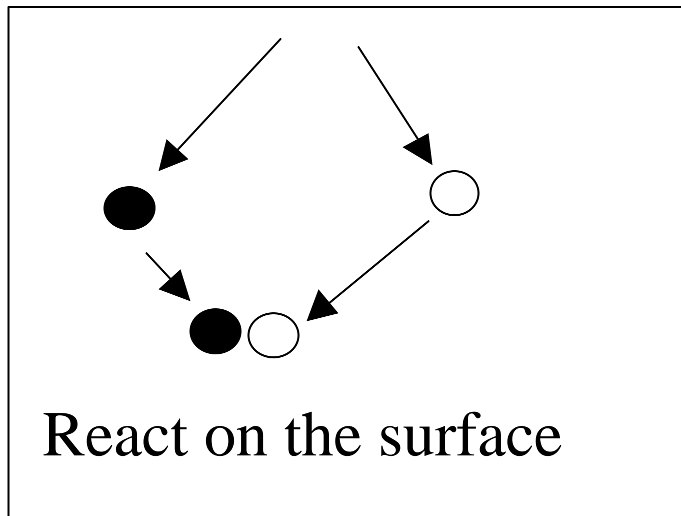
Figure 10.3

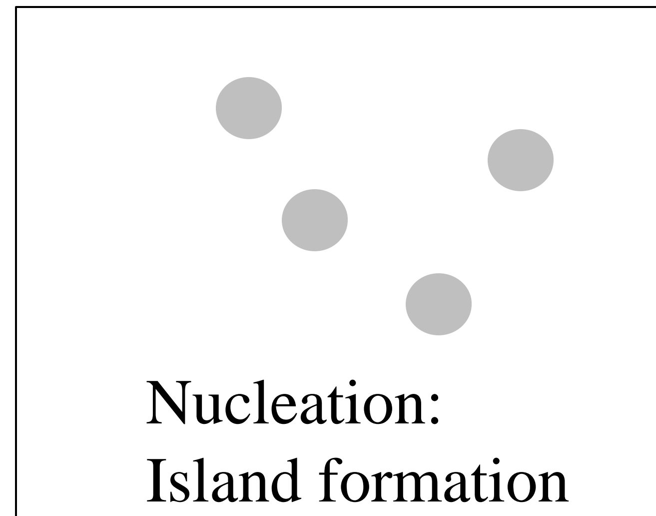


Deposition Process

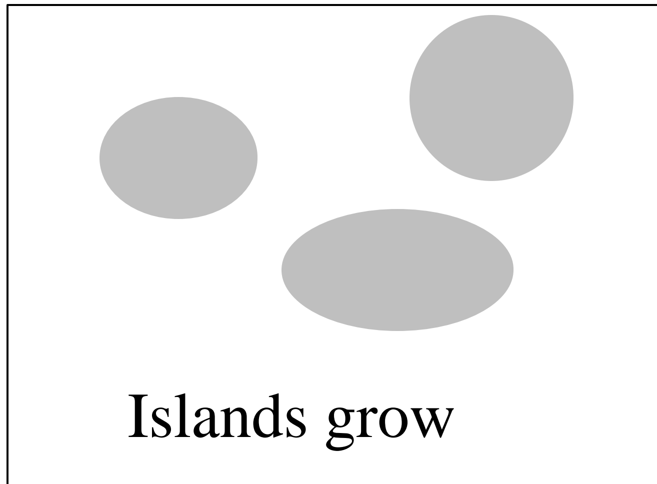


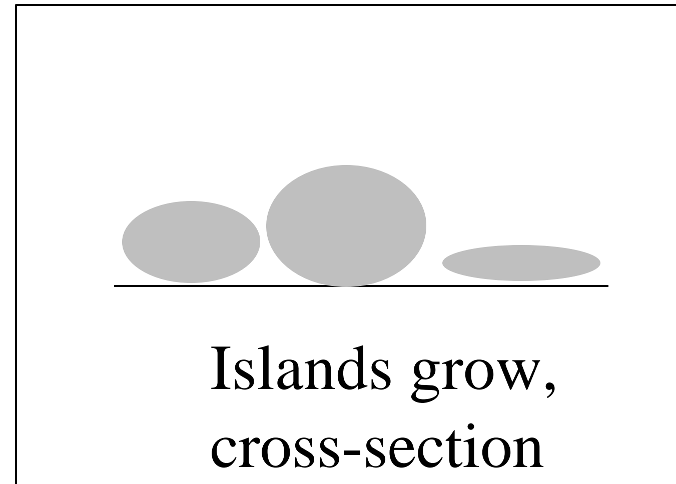


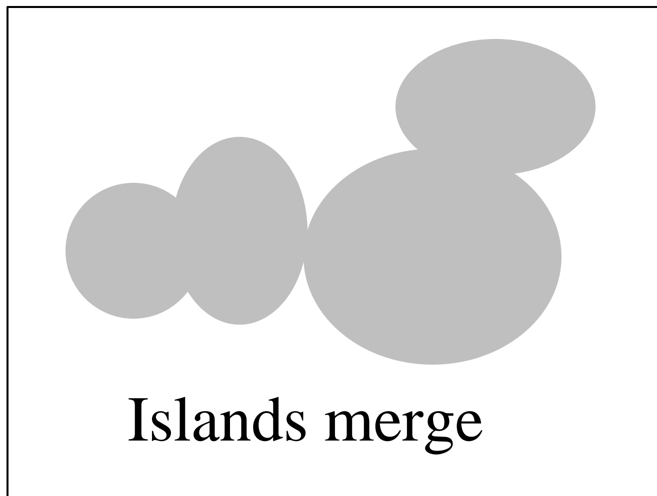


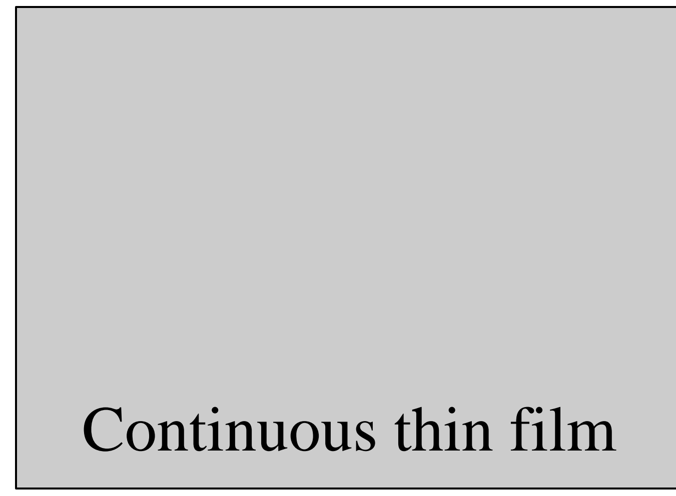


Deposition Process









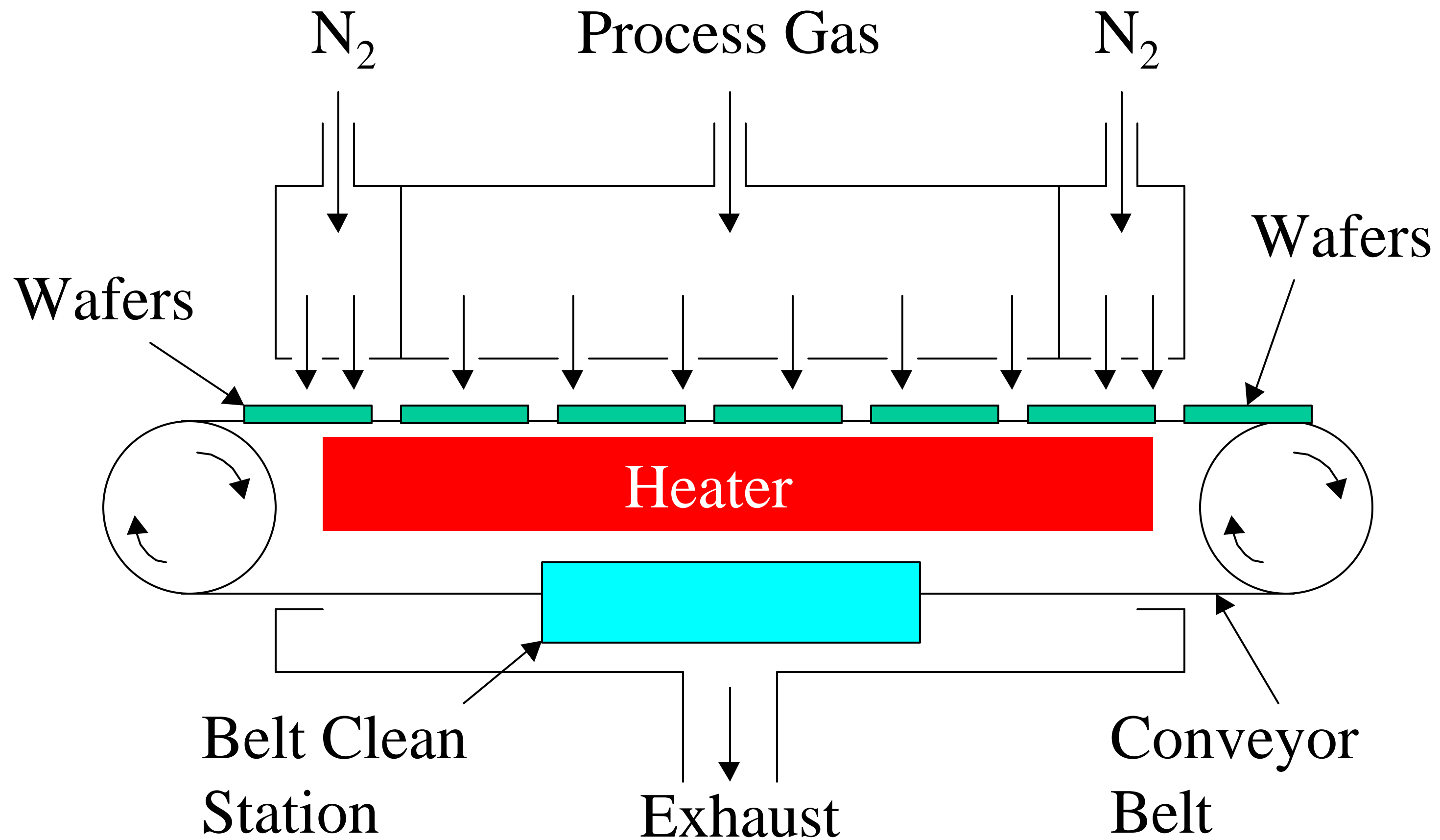
CVD Processes

- APCVD
- LPCVD
- PECVD

Atmospheric Pressure CVD

- CVD process taking place at atmospheric pressure
- APCVD process has been used to deposit silicon oxide and silicon nitride
- APCVD O_3-TEOS oxide process is widely used in the semiconductor industry, especially in STI and PMD applications
- Conveyor belt system with in-situ belt clean

APCVD Reactor



Question

- A semiconductor manufacturer has its R&D lab on the coast near sea level and one of its manufacturing fabs on a high altitude plateau. It was found that the APCVD processes developed in the R&D lab couldn’t directly apply in that particular fab. Why?

Answer

- On a high-altitude plateau, the atmospheric pressure is significantly lower than at sea level. Because earlier APCVD reactor didn’t have a pressure-control system, a process that worked fine in the R&D lab at sea level might not work well in the high altitude fab because of pressure difference

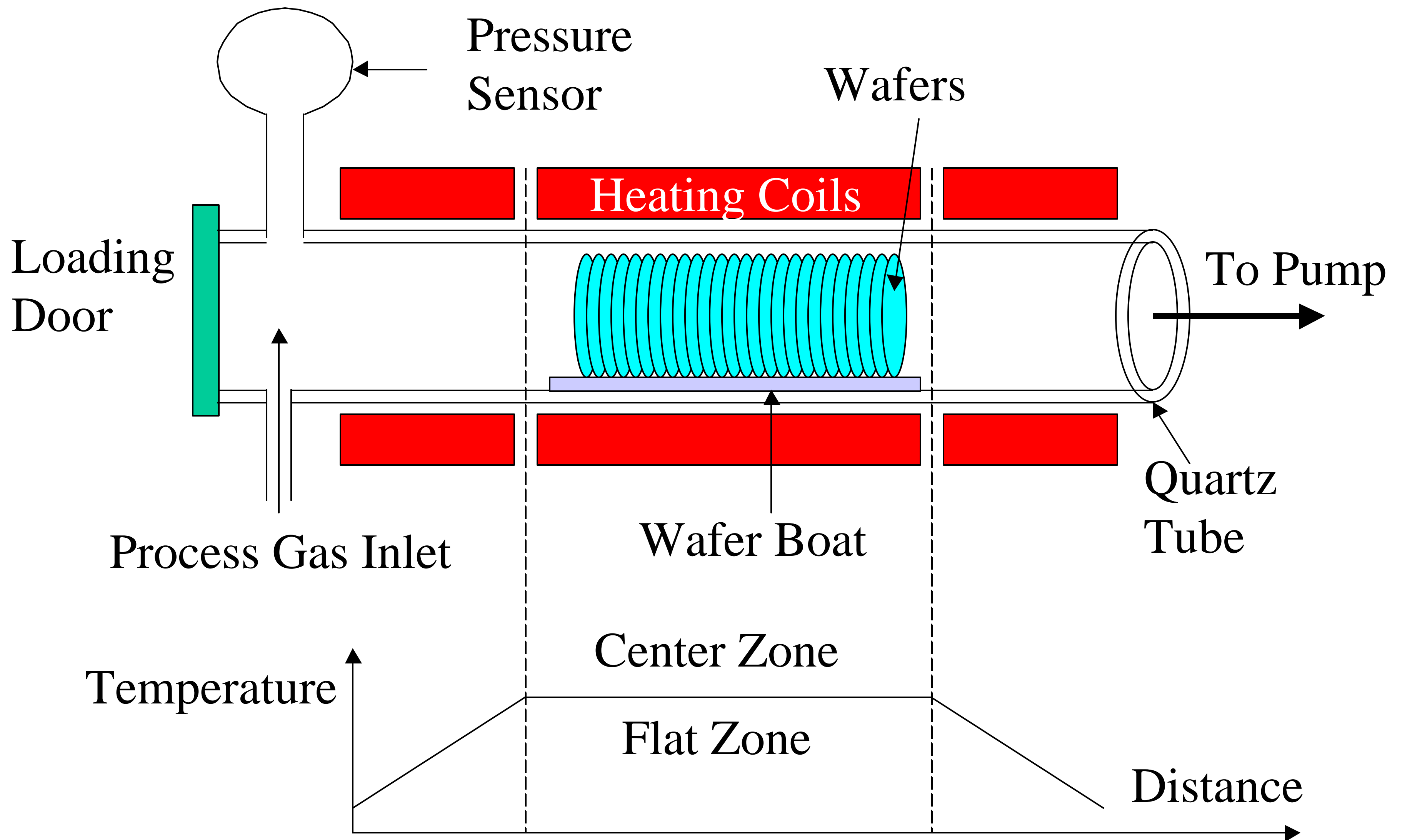
LPCVD

- Longer MFP
- Good step coverage & uniformity
- Vertical loading of wafer
- Fewer particles and increased productivity
- Less dependence on gas flow
- Vertical and horizontal furnace

Horizontal Conduction-Convection-heated LPCVD

- Adaptation of horizontal tube furnace
  - Low pressure: from 0.25 to 2 Torr
  - Used mainly for polysilicon, silicon dioxide and silicon nitride films
  - Can process 200 wafers per batch

LPCVD System

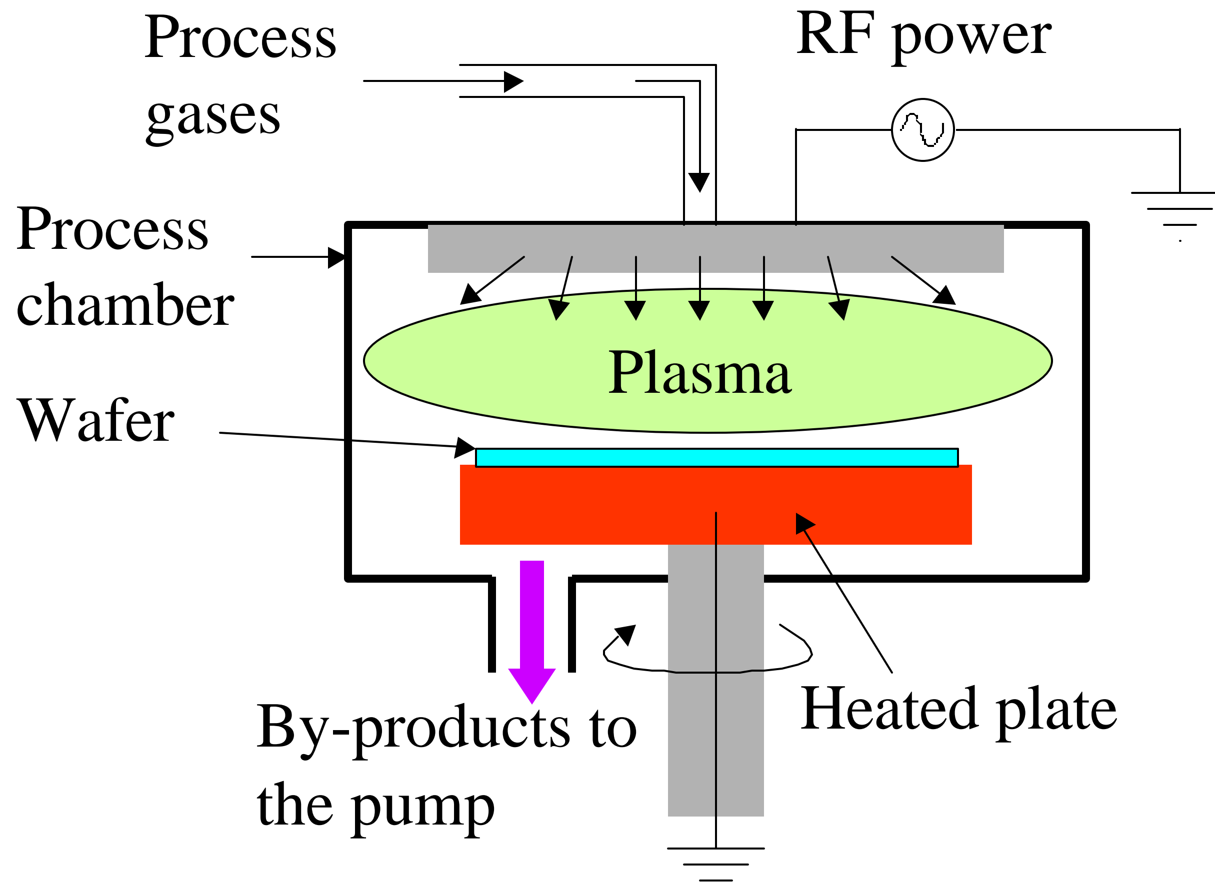


PECVD

- Developed when silicon nitride replaced silicon dioxide for passivation layer.

- High deposition rate at relatively low temp.
- RF induces plasma field in deposition gas
- Stress control by RF
- Chamber plasma clean.

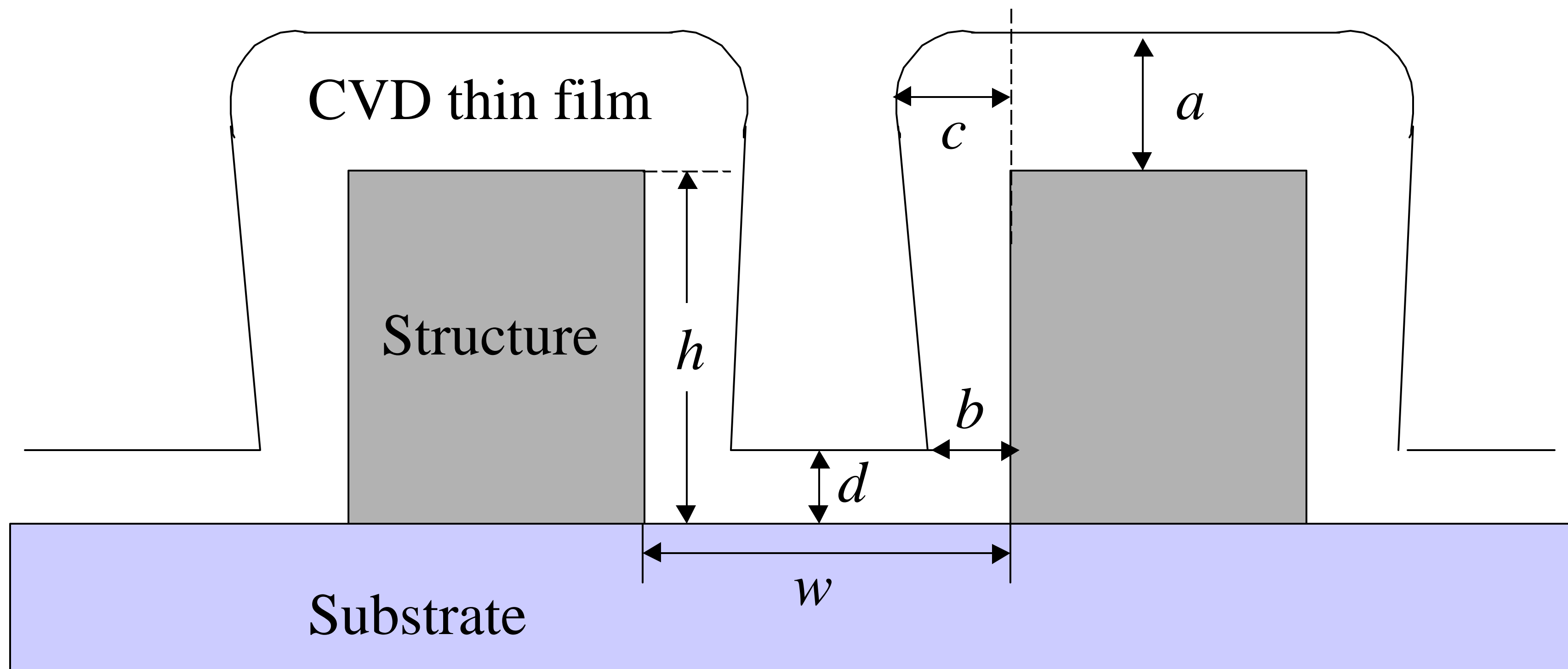
Plasma Enhanced CVD System



Step Coverage

- A measurement of the deposited film reproducing the slope of a step on the substrate surface
- One of the most important specifications
  - Sidewall step coverage
  - Bottom step coverage
  - Conformality
  - Overhang

Step Coverage and Conformity



Sidewall step coverage = b/a

Bottom step coverage = d/a

Conformity = b/c

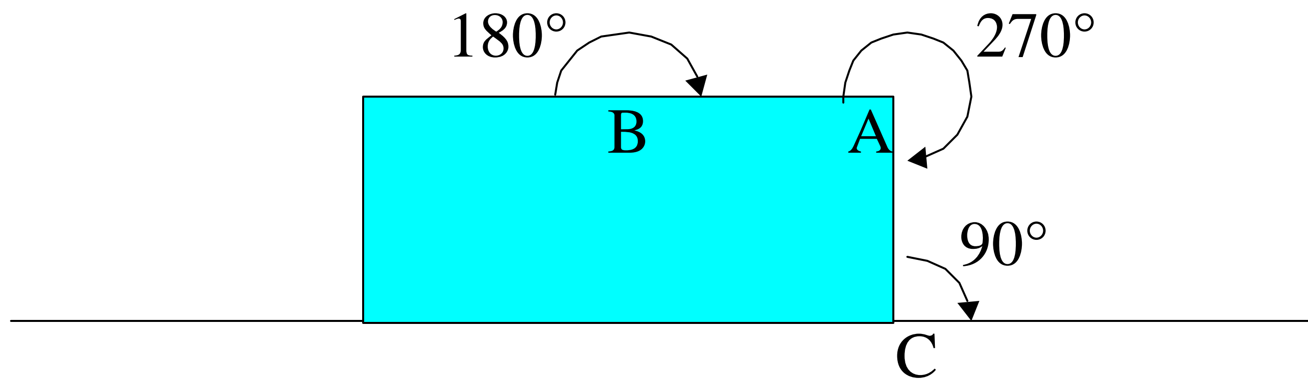
Overhang = $(c - b)/b$

Aspect ratio = h/w

Factors Affect Step Coverage

- Arriving angle of precursor
- Surface mobility of adsorbed precursor

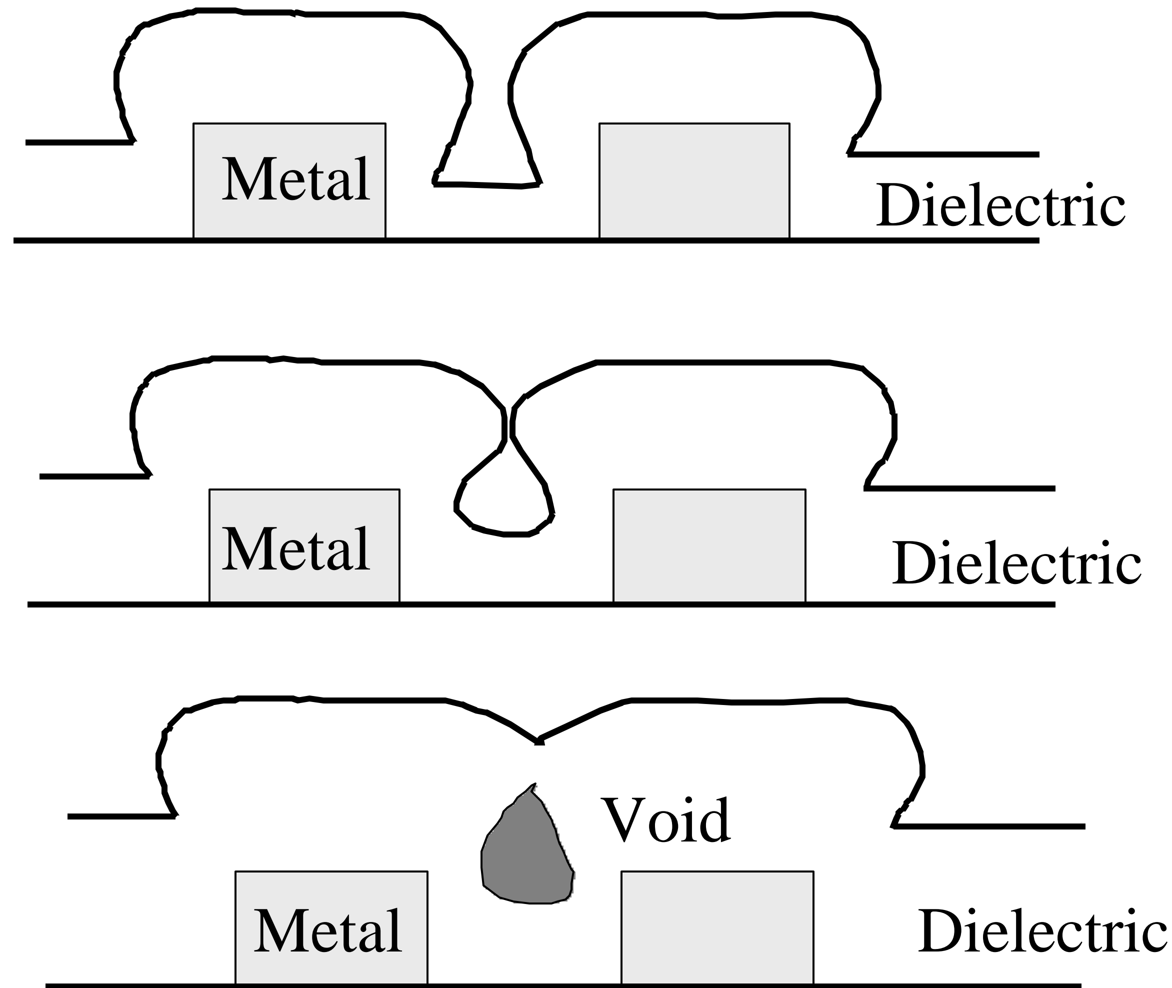
Arriving Angles



Arriving Angle

- Corner A: 270°, corner C: 90°
- More precursors at corner A
- More deposition
- Form the overhang
- Overhang can cause voids or keyholes

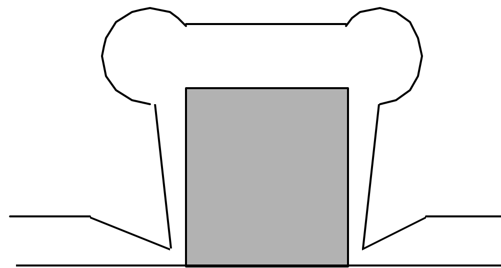
Void Formation Process



Control of Arriving Angle

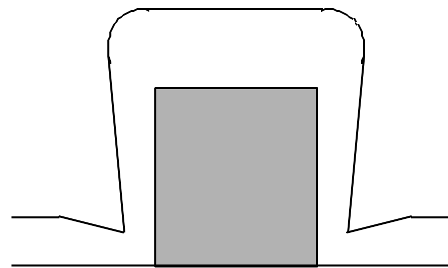
- |Changing pressure
- Tapering opening

Step Coverage, Pressure and Surface Mobility



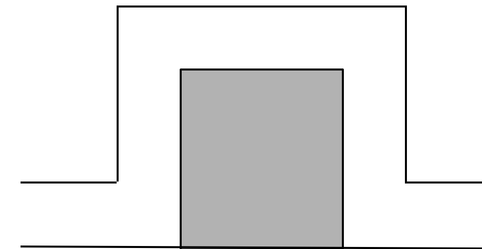
APCVD

No mobility



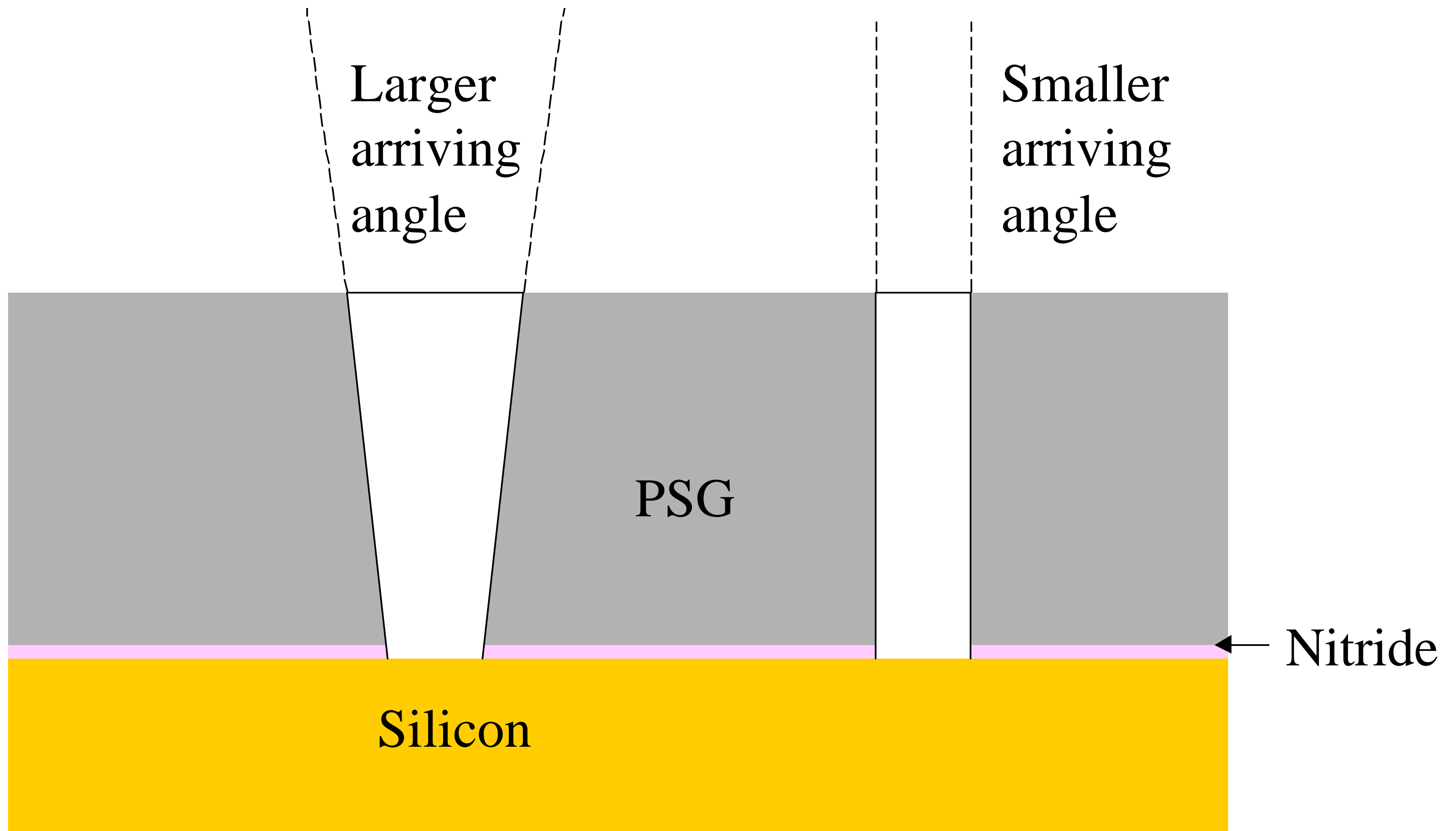
LPCVD

No mobility



High mobility

Arriving Angles, Contact Holes



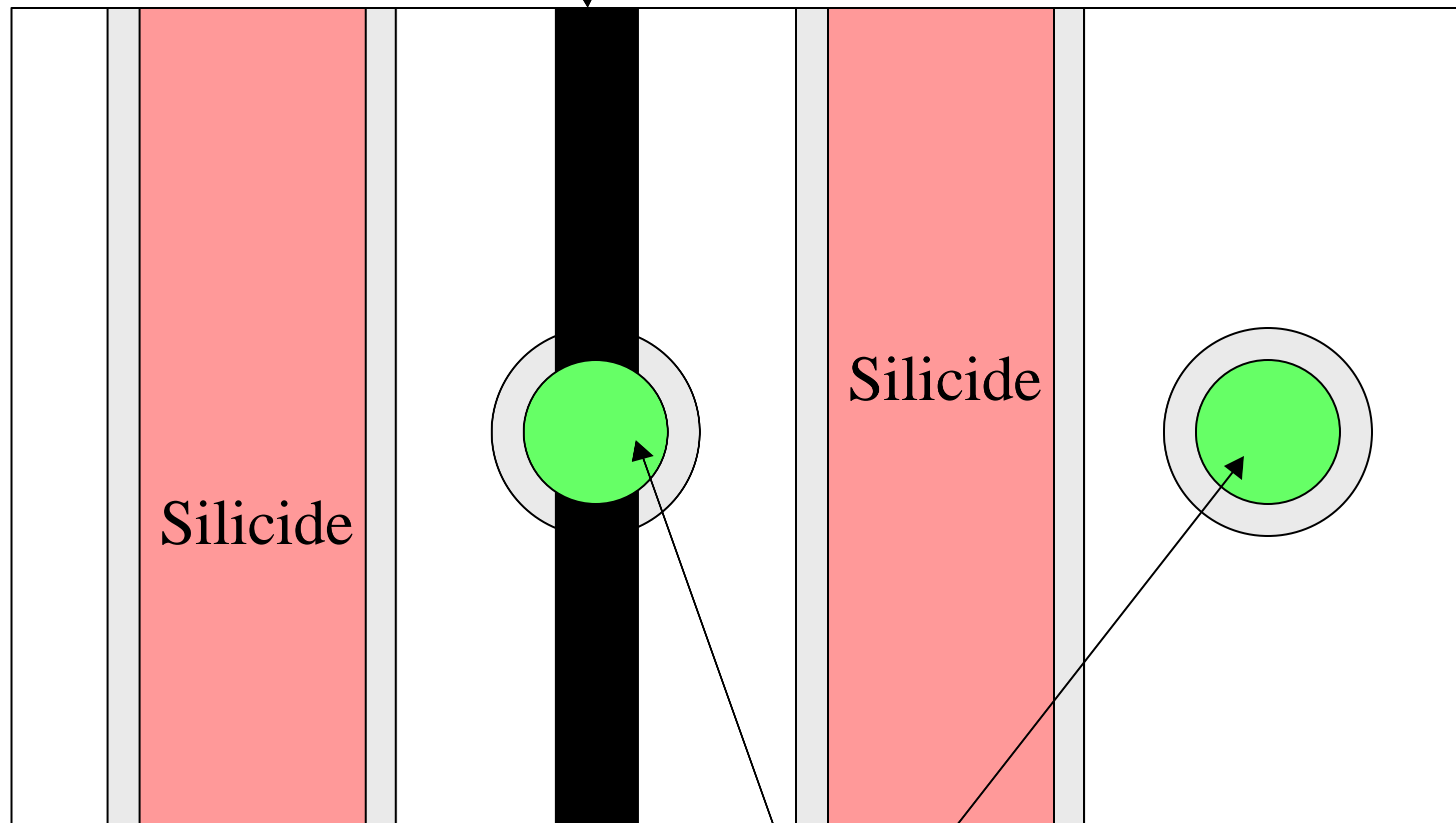
Gap Fill

- Fill a gap without voids
- Voids: cause defect and reliability problems
- Deposition/Etchback/Deposition
  - Silane and PE-TEOS film
- Conformal deposition
  - O_3-TEOS and tungsten CVD
- High density plasma CVD

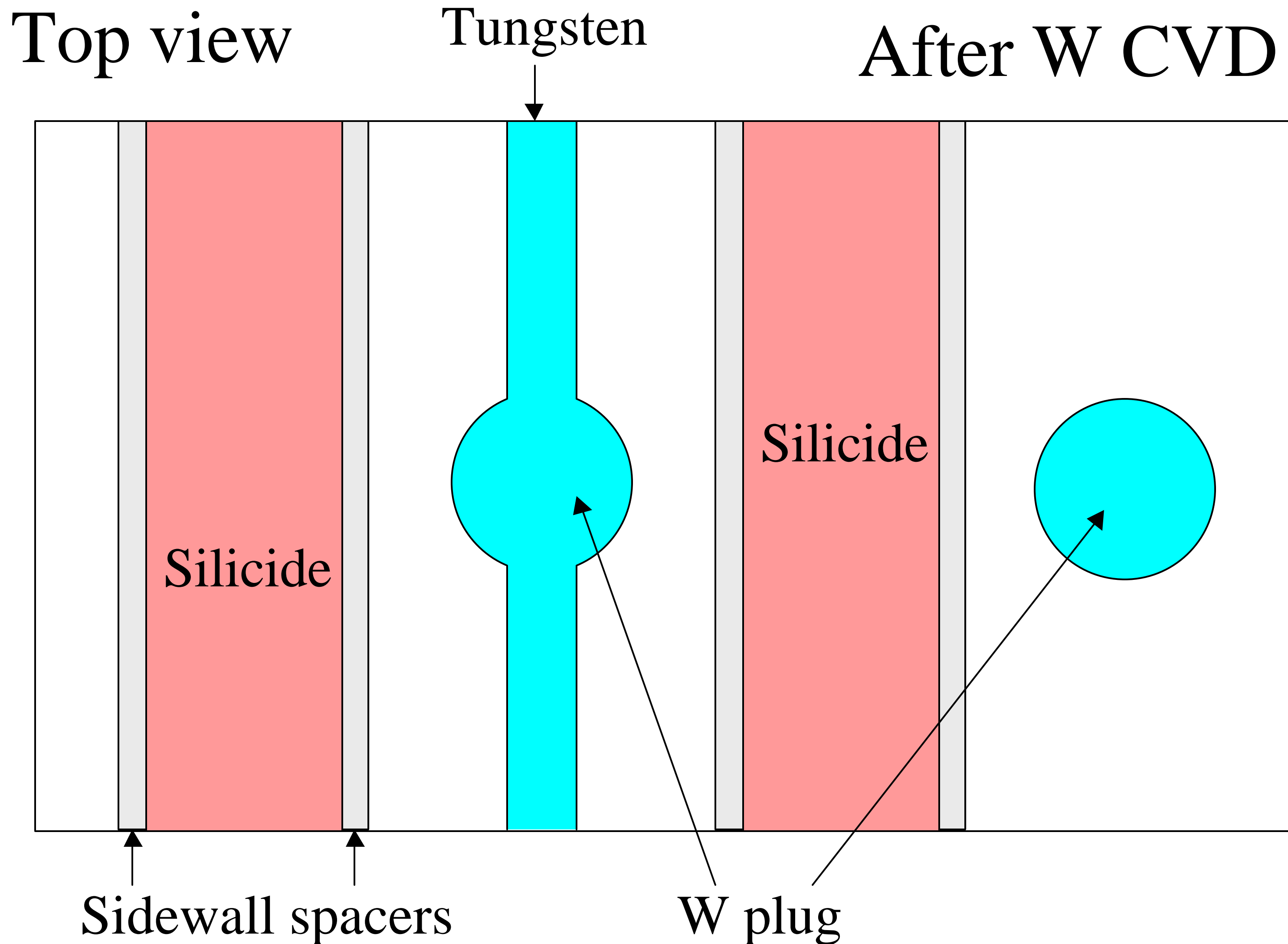
Gap Fill

- PMD: zero tolerance voids
  - Tungsten can be deposited into these voids
  - Causing shorts
- IMD: voids below metal may tolerable
  - reducing κ
  - process gas could come out later and cause reliability problem

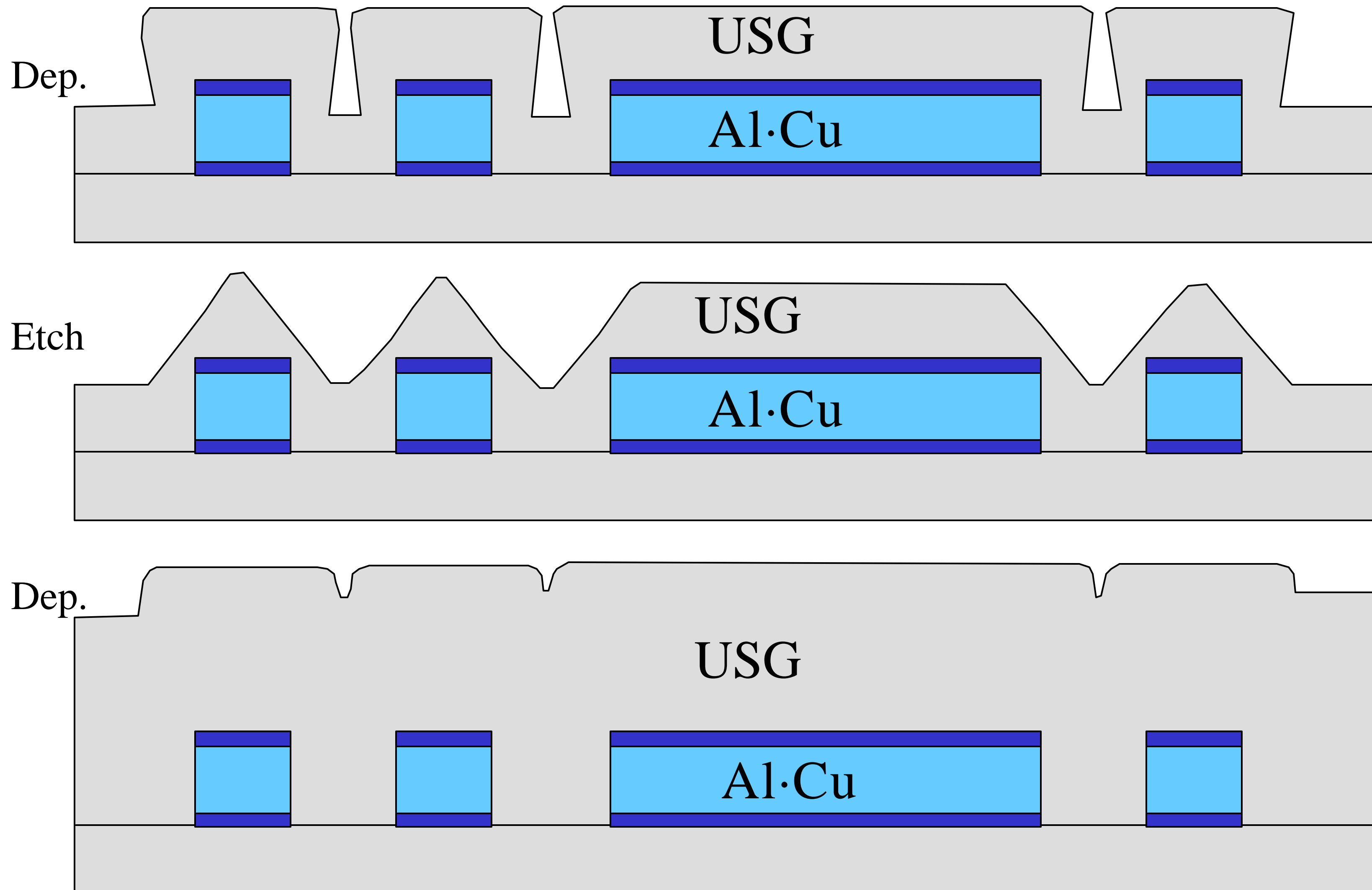
Void in PMD



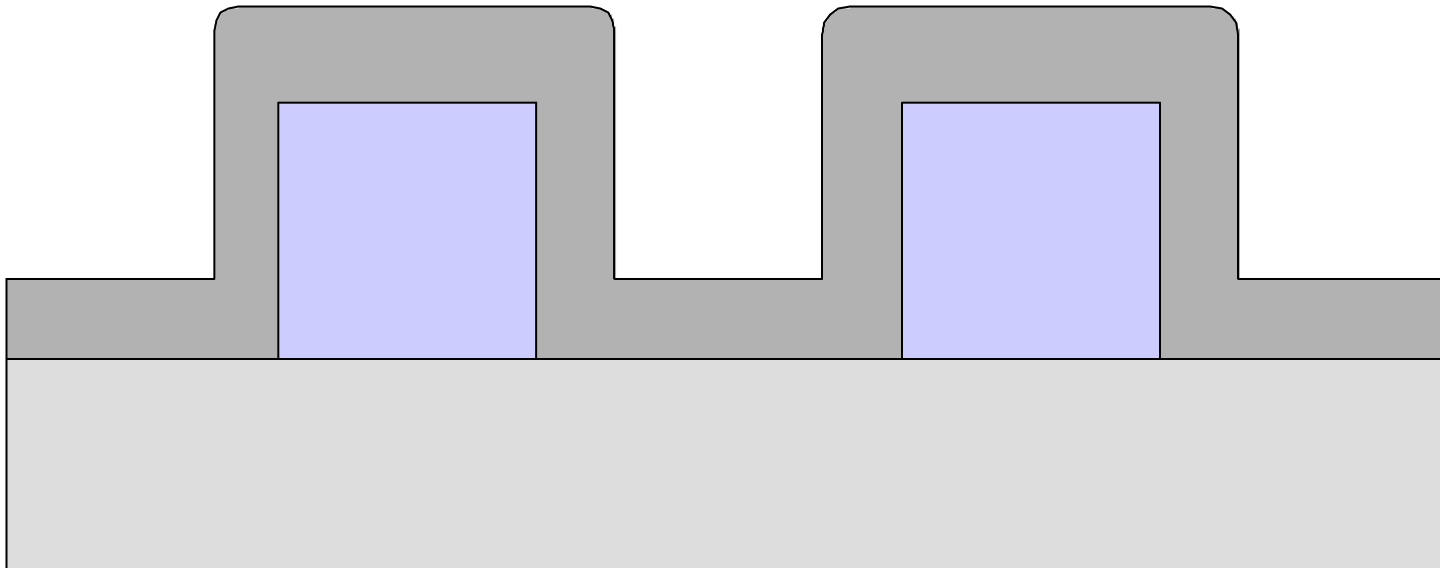
Unwanted W Line Between Gates



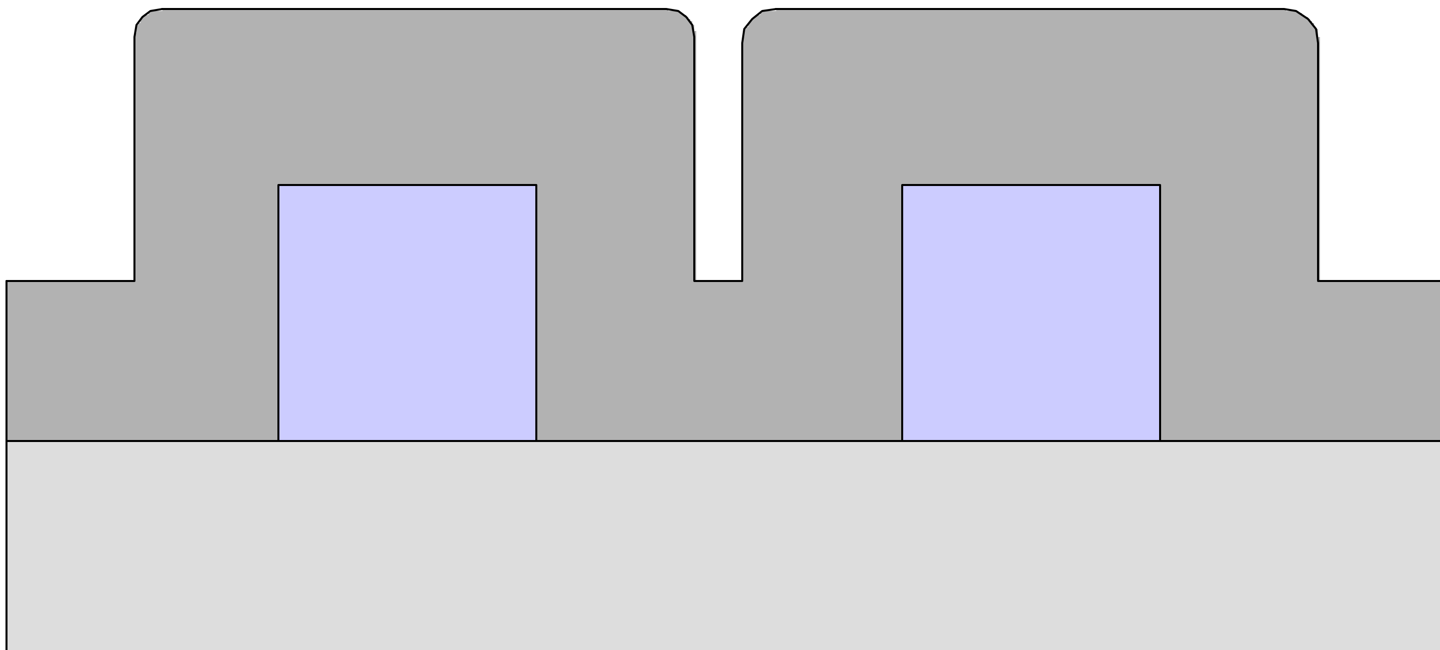
Deposition/Etchback/Deposition



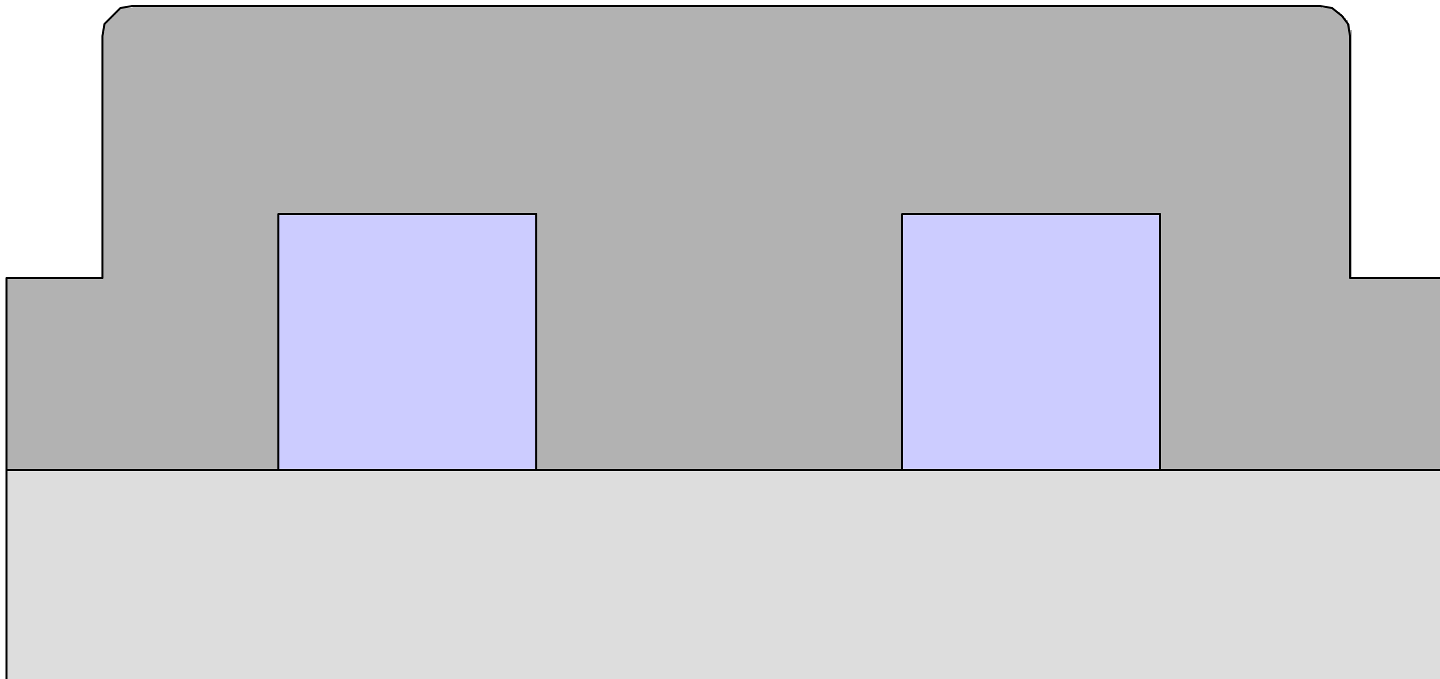
Conformal Deposition Gap Fill



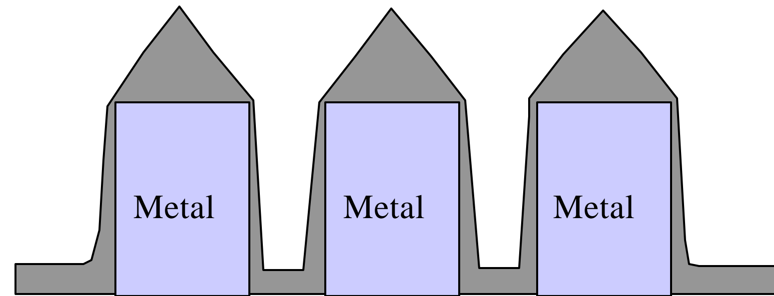
Conformal Deposition Gap Fill

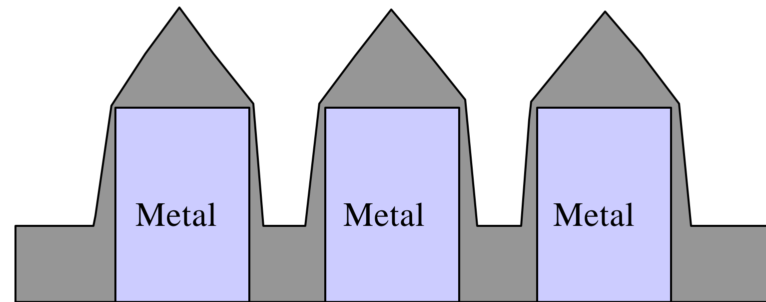


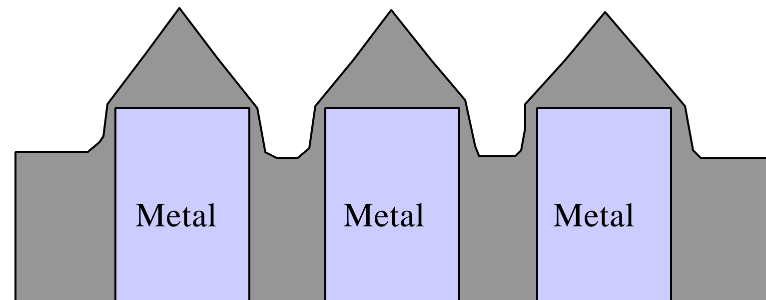
Conformal Deposition Gap Fill



HDP CVD Gap Fill







Surface Adsorption

- Determine precursors surface mobility
- Affect step coverage and gap fill

- Physical adsorption (physisorption)
- Chemical adsorption (chemisorption)

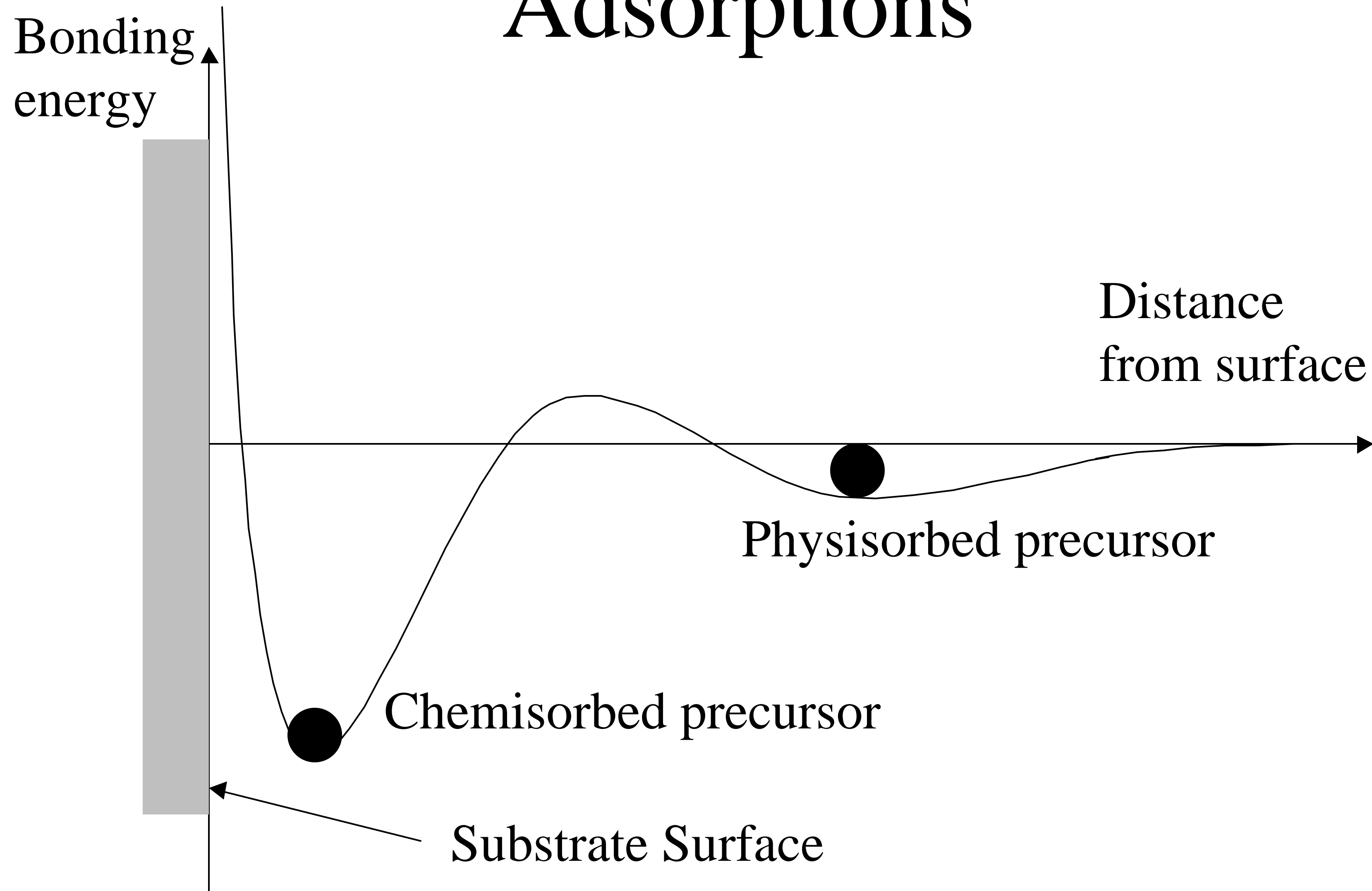
Chemisorption

- Actual chemical bonds between surface atom and the adsorbed precursor molecule
- Bonding energy usually exceeding 2 eV
- Low surface mobility
- Ion bombardment with10 to 20 eV energy in PECVD processes can cause some surface migration of chemisorbed precursors

Physisorption

- Weak bond between surface and precursor
- Bonding energy usually less than 0.5 eV
  - Hydrogen bonding
  - Van der Waals forces
- Ion bombardment and thermal energy at 400 °C can cause migration of physisorbed precursors
- High surface mobility

Adsorptions



Dielectric CVD Precursors

- Silane (SiH_4)
- TEOS (tetra-ethyl-oxy-silane, $Si(OC_2H_5)_4$)

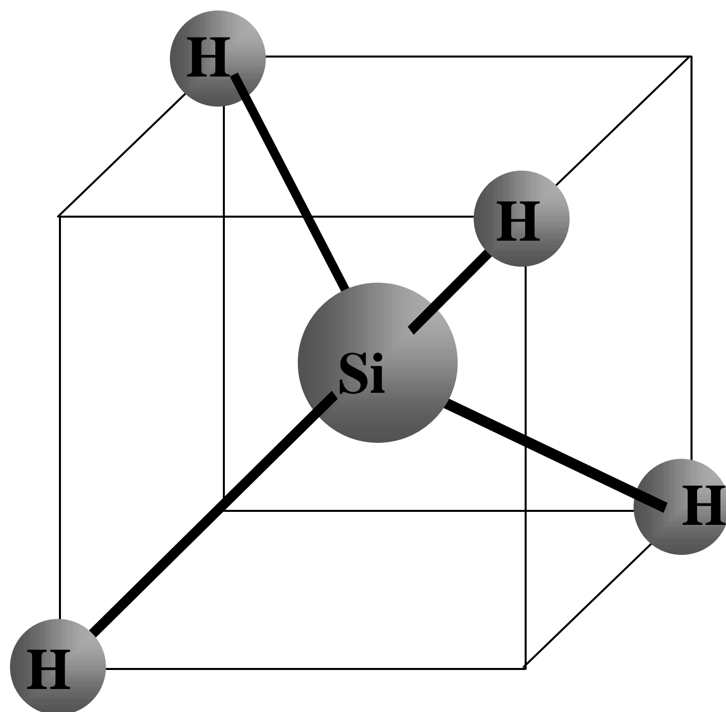
CVD Precursor: Silane

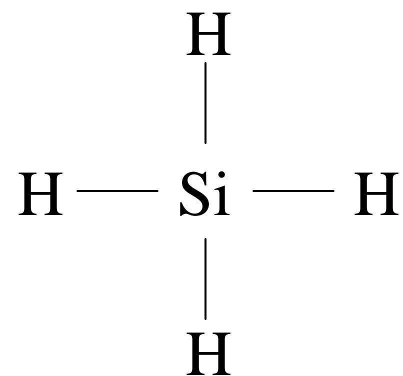
- Dielectric CVD
  - PECVD passivation dielectric depositions
  - PMD barrier nitride layer
  - Dielectric anti reflective coating (DARC)
  - High density plasma CVD oxide processes
- LPCVD poly-Si and silicon nitride
- Metal CVD
  - W CVD process for nucleation step
  - Silicon source for WSi_x deposition

Dielectric CVD Precursor: Silane

- Pyrophoric (ignite itself), explosive, and toxic
- Open silane line without thoroughly purging can cause fire or minor explosion and dust line

Structure of Silane Molecule





CVD Precursor Adsorption: Silane

- Silane molecule is perfectly symmetrical
- Neither chemisorb nor physisorb
- Fragments of silane, SiH_3, SiH_2, or SiH, can easily form chemical bonds with surface
- Low surface mobility, overhangs and poor step coverage

CVD Precursor Adsorption: TEOS

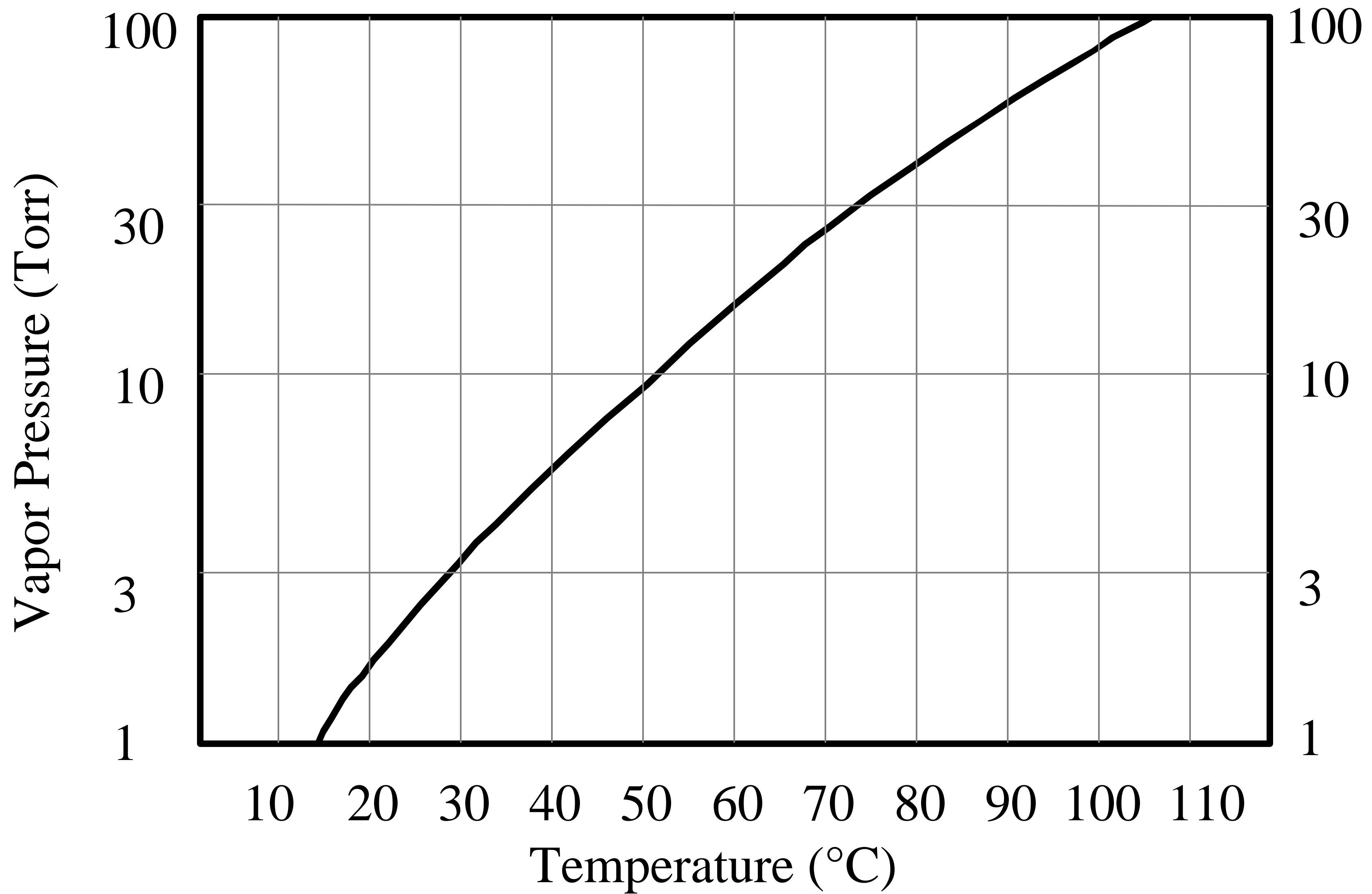
- TEOS (tetra-ethyl-oxy-silane, $Si(OC_2H_5)_4$)
- Big organic molecule
- TEOS molecule is not perfectly symmetric
- Can form hydrogen bond and physisorb
- High surface mobility
- Good step coverage, conformality, and gap fill
- Widely used for oxide deposition

TEOS Molecule

TEOS Applications

- STI, sidewall spacer, PMD, and IMD
- Most dielectric CVD processes are TEOS based oxide processes

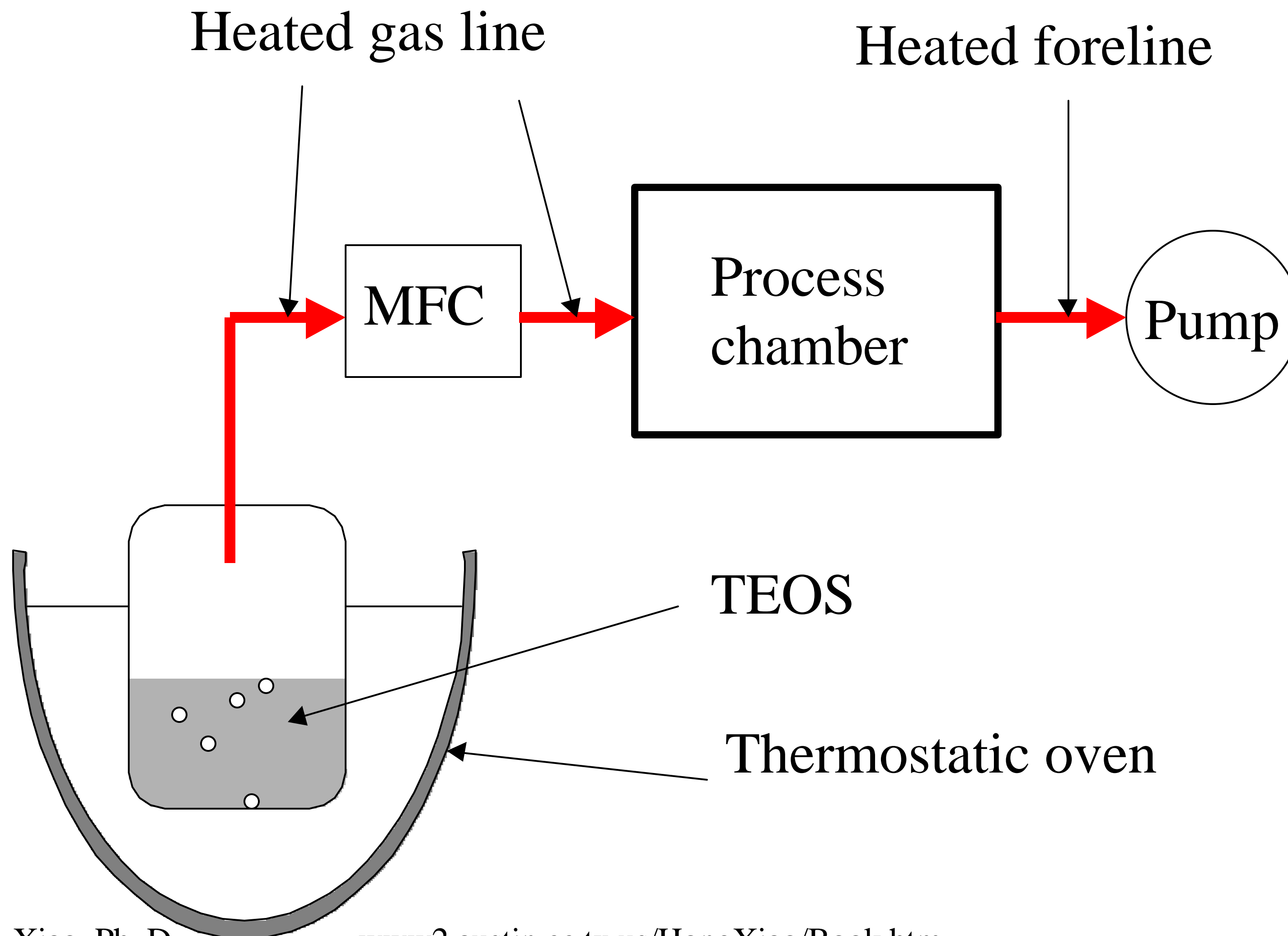
TEOS Vapor Pressure



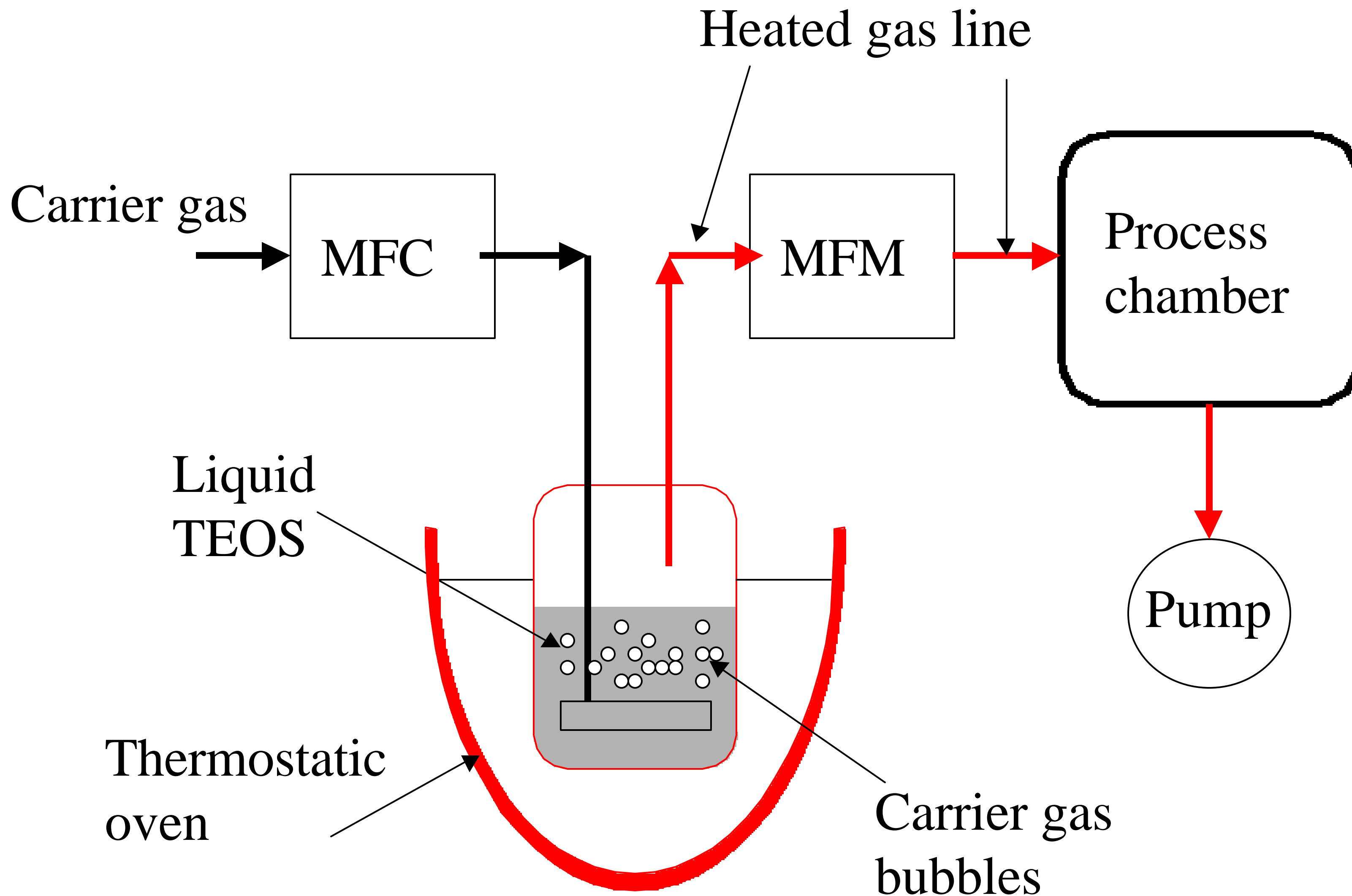
TEOS Delivery

- A liquid at room temperature with boiling point at the sea level is 168 °C
  - As a reference, boiling point of water (H_2O) at sea level is 100 °C
- Need delivery system to send its vapor to process chamber
- Boiler, bubbler, and injection systems

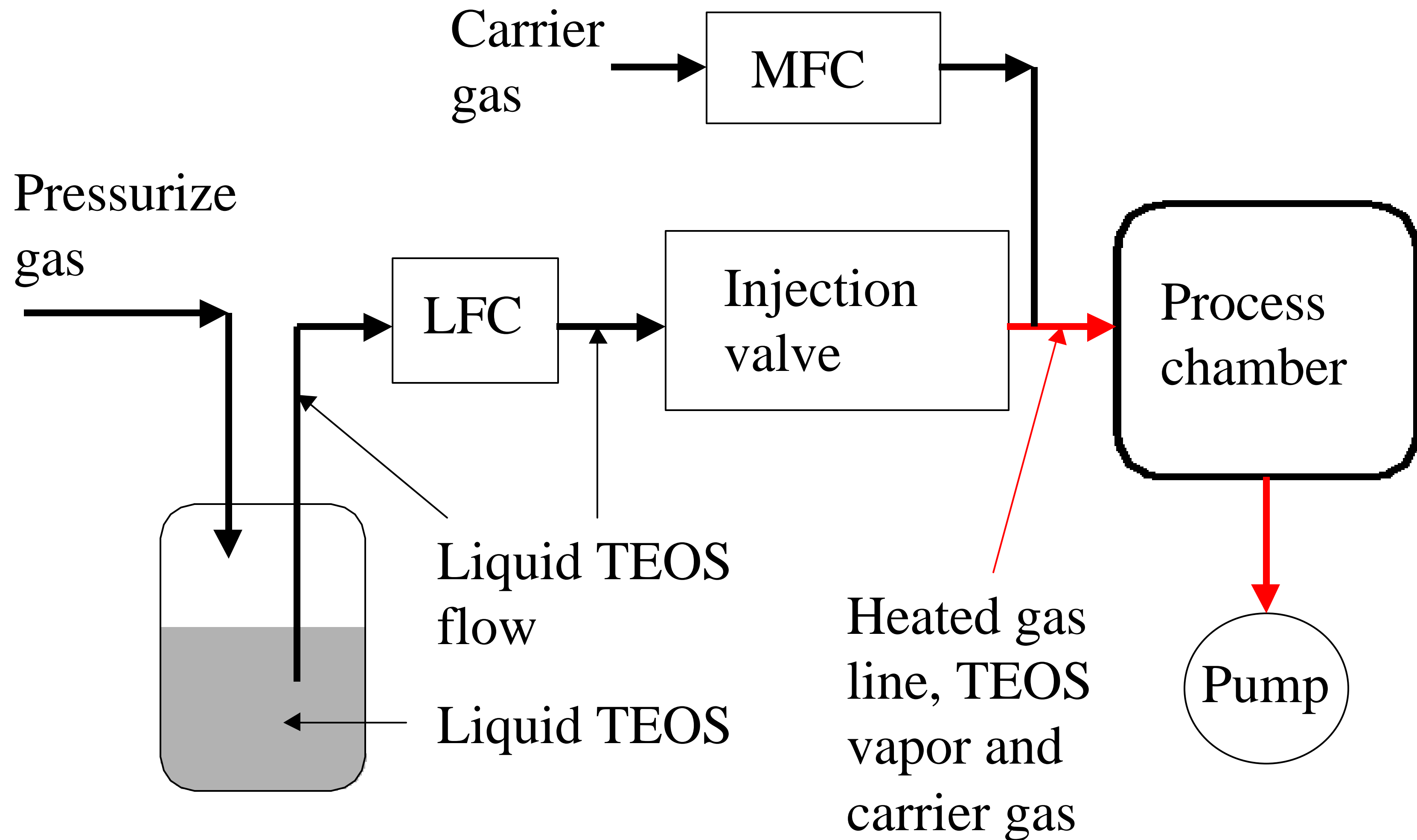
Boiler System



Bubbler System



Injection System



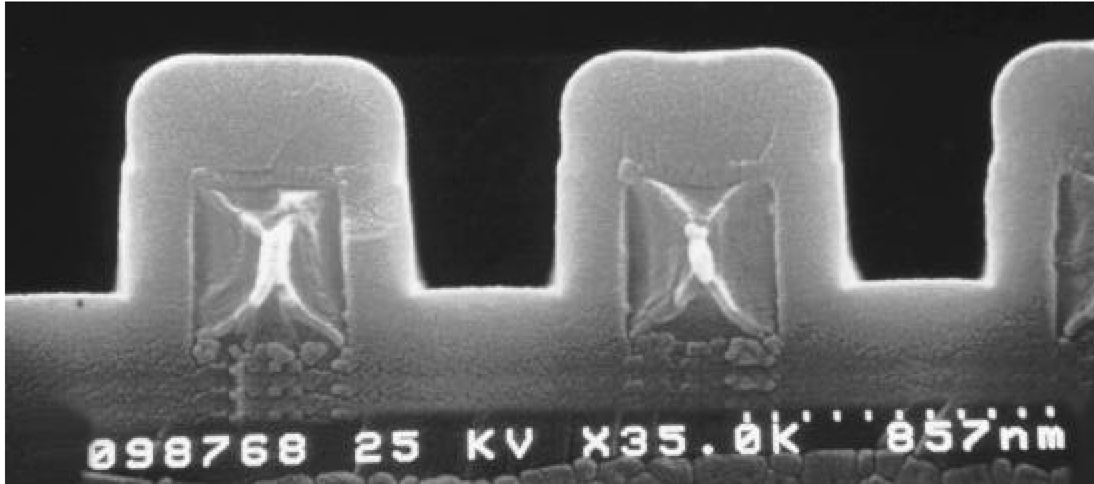
Sticking Coefficient

- The probability that precursor atom forms chemical bond with surface atom in one collision
- Can be calculated by comparing the calculated deposition rate with 100% sticking coefficient and the measured actual deposition rate

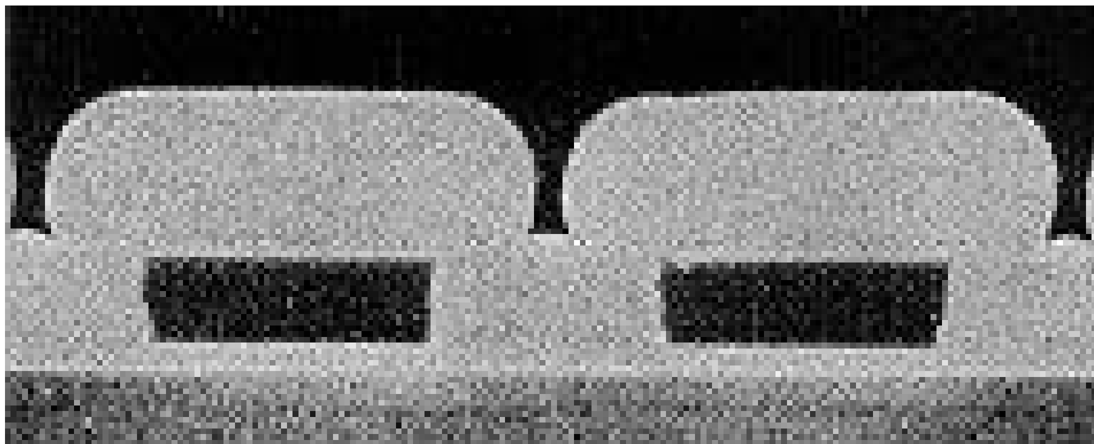
Sticking Coefficient

Precursors	**Sticking Coefficient**
SiH_4	3×10^{-4} to 3×10^{-5}
SiH_3	0.04 to 0.08
SiH_2	0.15
SiH	0.94
TEOS	10^{-3}
WF_6	10^{-4}

Step Coverage of TEOS and Silane Oxide



TEOS



Silane

Question

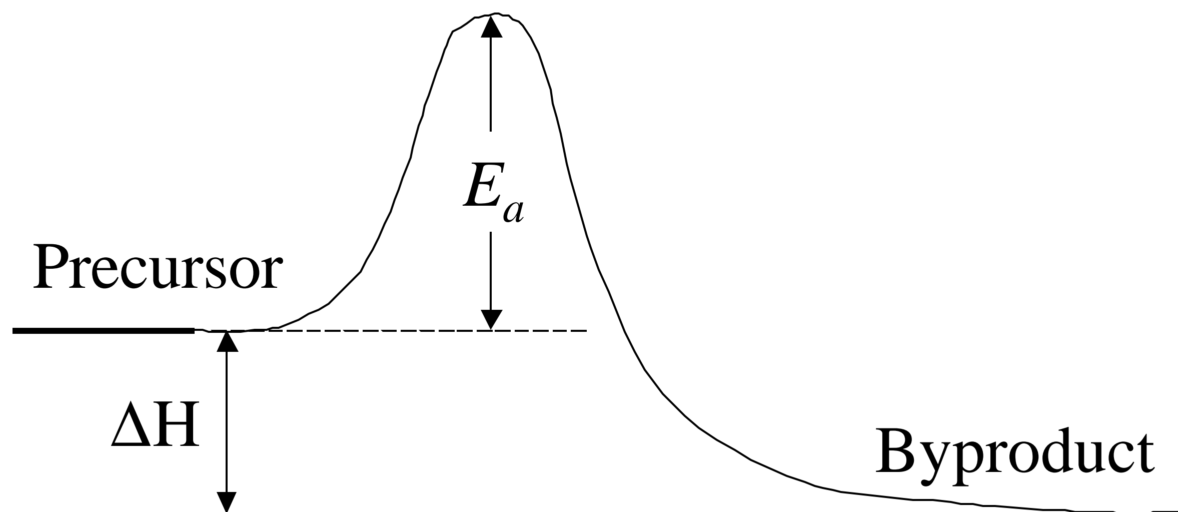
- Why don't people apply TEOS as the silicon source gas for the silicon nitride deposition to get better step coverage for the nitride film

Answer

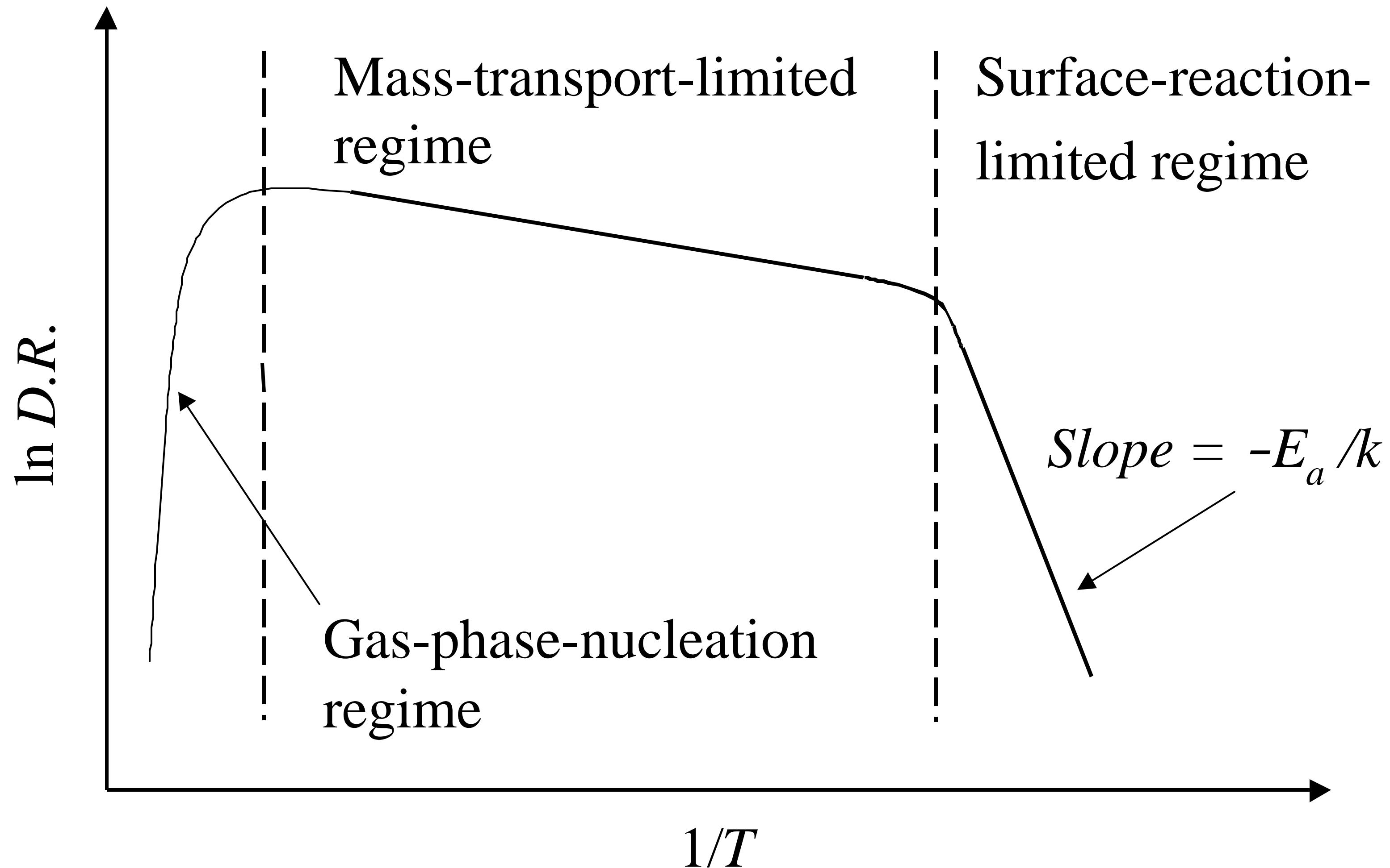
- In the TEOS molecule, the silicon atom is bonded with four oxygen atoms. It is almost impossible to strip all oxygen atoms and have silicon bonded only with nitrogen. Therefore, TEOS is mainly used for the oxide deposition and the nitride deposition normally uses silane as the silicon source gas

Chemical Reaction Rate

$$C.R. = A \exp(-E_a/kT)$$



Deposition Regimes



Surface-Reaction-Limited Regime

- Chemical reaction rate can’t match precursor diffusion and adsorption rates; precursors pile up on the substrate surface and wait their turn to react.

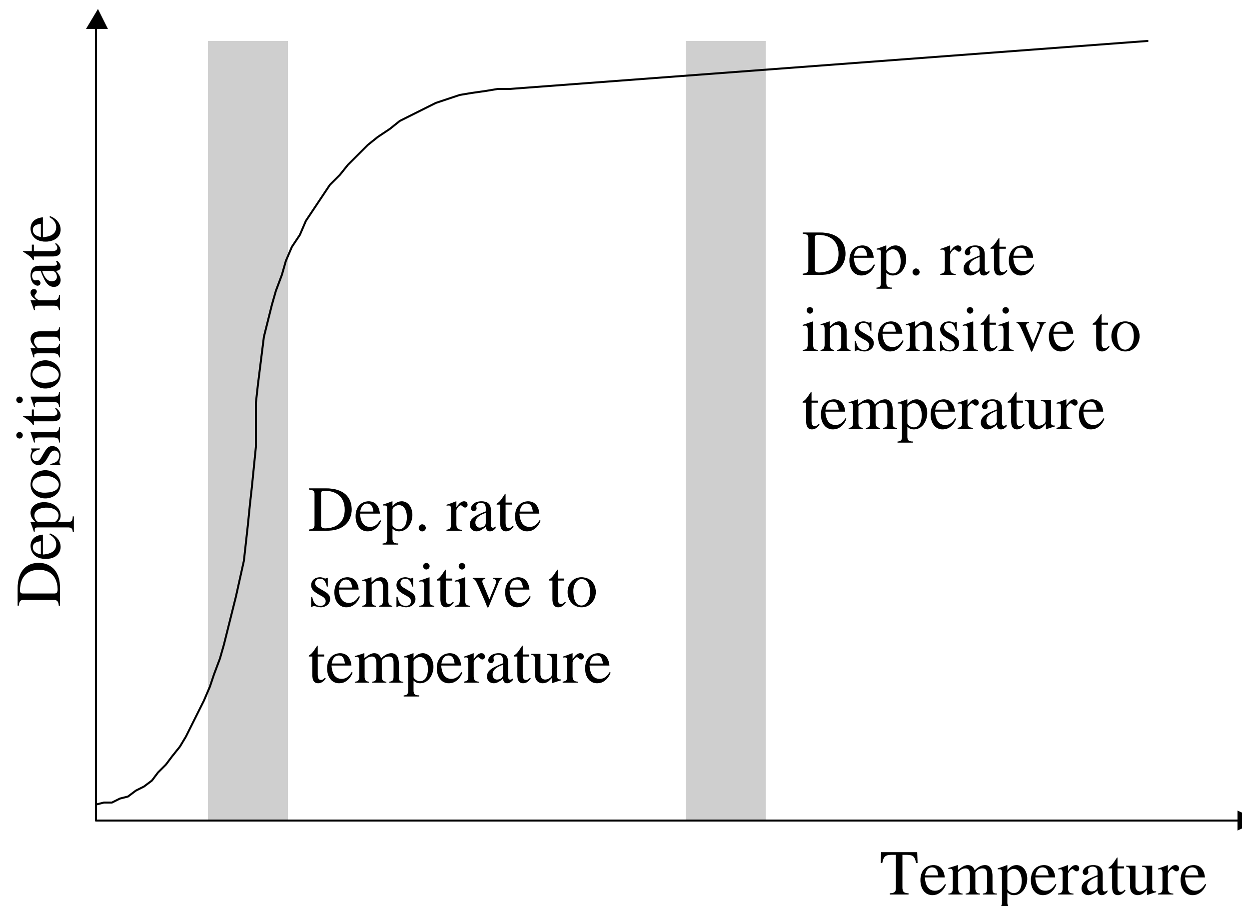
$$D.R. = C.R. [B] [C] [\,]\ldots$$

- Deposition rate is very sensitive to temperature

Mass-Transport-Limited Regime

- When the surface chemical reaction rate is high enough, the chemical precursors react immediately when they adsorb on the substrate surface.
- *Deposition rate = D dn/dx [B] [C] [ ]…*
- Deposition rate is insensitive to temperature
- Mainly controlled by gas flow rates

Deposition Rage Regimes



CVD Reactor Deposition Regime

- Most single wafer process reactors are designed in mass-transport-limited regime
- It is easier to control the gas flow rate
- Plasma or unstable chemicals such as ozone are used to achieve mass-transport-limited-regime at relatively low temperature

Applications of Dielectric Thin film

- Shallow trench isolation (STI, USG)
- Sidewall Spacer (USG)
- Pre-metal dielectric (PMD, PSG or BPSG)
- Inter-metal dielectric (IMD, USG or FSG)
- Anti-reflection coating (ARC, SiON)
- Passivation dielectric (PD, Oxide/Nitride)

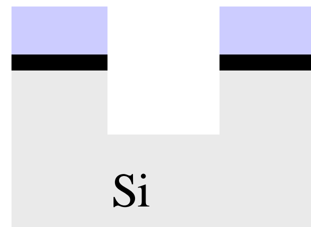
Dielectric CVD, Oxide and Nitride

Oxide (SiO_2)	**Nitride (Si_3N_4)**
Similar dielectric strength, > 1×10^7 V/cm	Similar dielectric strength, > 1×10^7 V/cm
Lower dielectric constant, $\kappa = 3.9$	Higher dielectric constant, $\kappa = 7.0$
Not a good barrier for moisture and mobile ion (Na^+)	Good barrier for moisture and mobile ion (Na^+)
Transparent to UV	Conventional nitride opaque to UV
Can be doped with P and B	

Shallow Trench Isolation (STI)

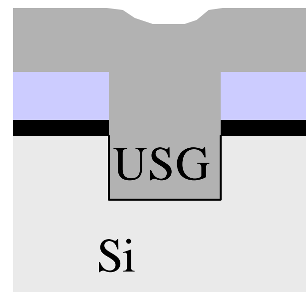
Grow pad oxide
Deposition nitride

Etch nitride, oxide and silicon

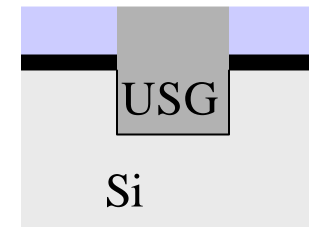


Grow barrier oxide

CVD USG trench fill

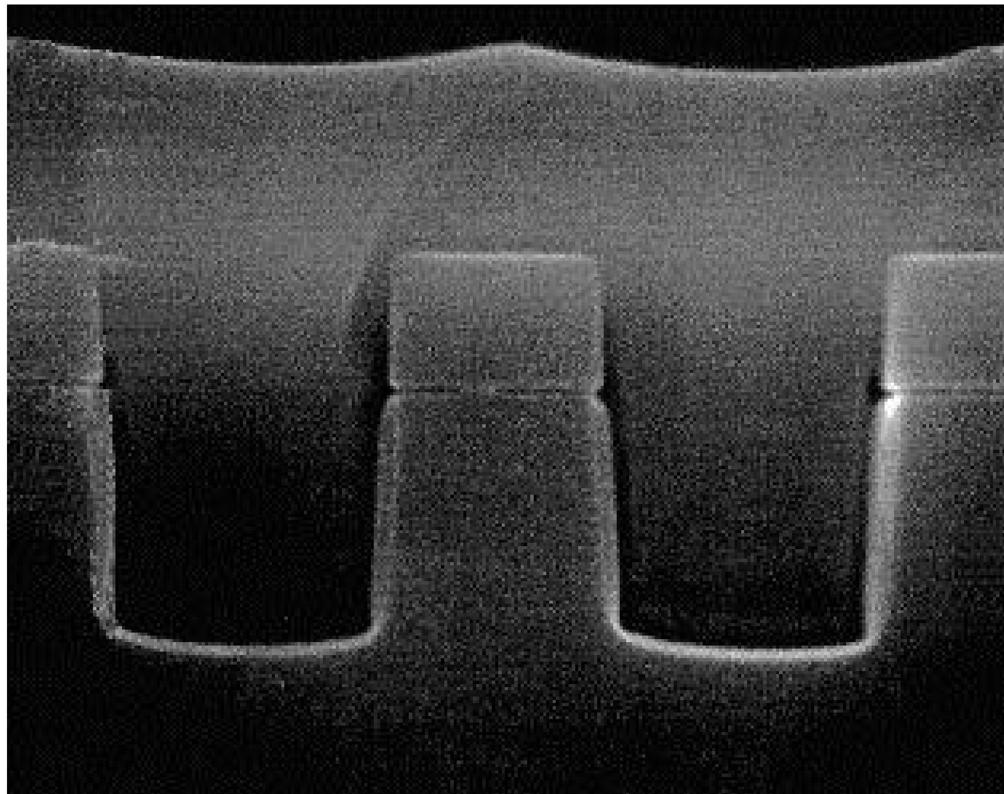


CMP USG
Anneal USG

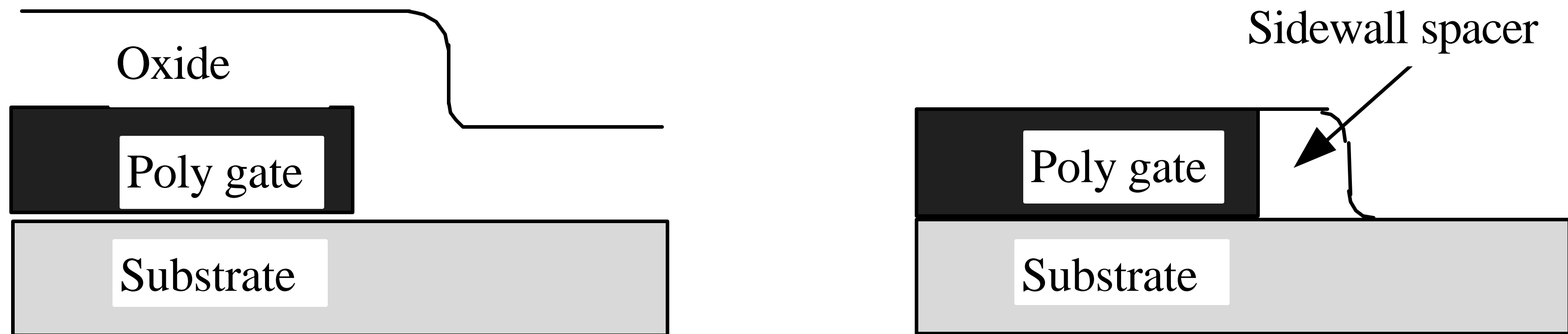


Strip nitride and oxide

Shallow Trench Isolation (STI)



Sidewall Spacer Formation

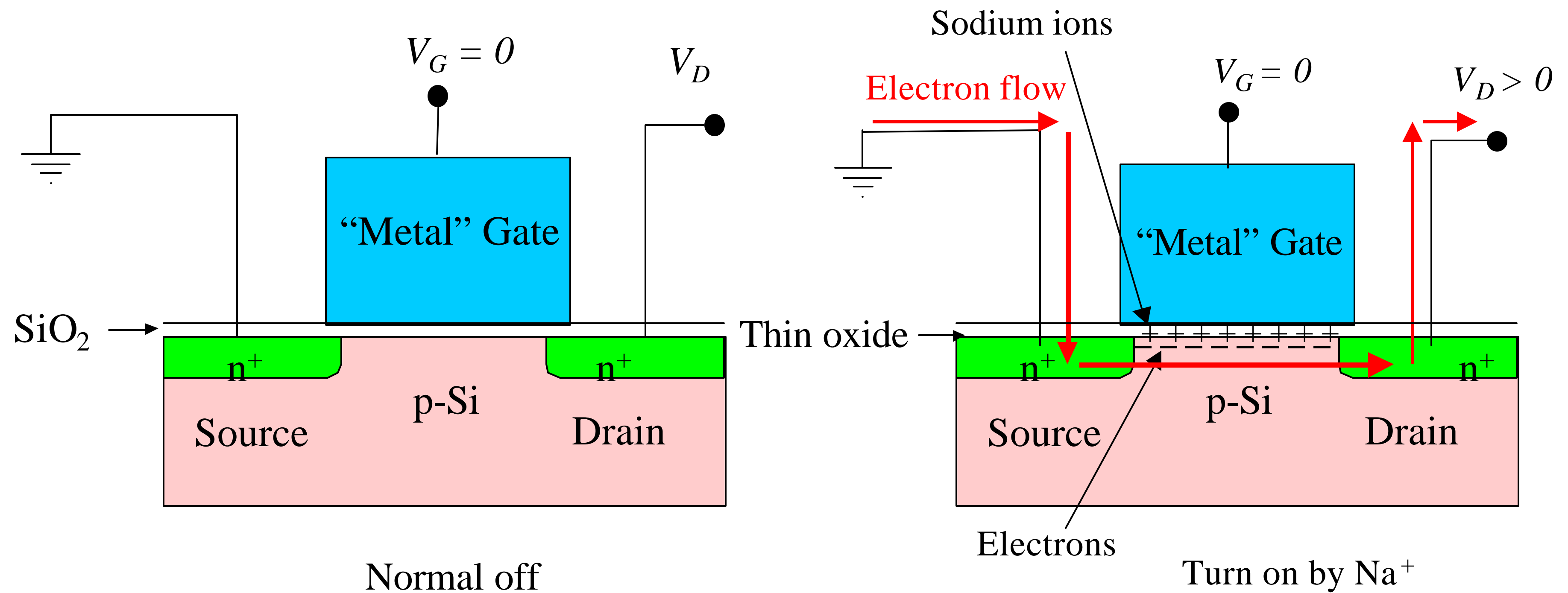


- Lightly doped drain (LDD)
- Self aligned silicide (Salicide)

PMD

- Doped oxide
- PSG or BPSG
- Phosphorus: gettering sodium and reduce flow temperature.
- Boron: further reduces flow temperature without excessive phosphorus

Sodium Ion Turn-on the MOSFET



PMD

- More phosphorus, lower reflow temperature
- >7wt% phosphorus, hygroscope

$$P_2O_5 + 3H_2O \rightarrow 2H_3PO_4$$

- H_3PO_4 etches aluminum causes metal corrosion
- Too much boron will cause crystallization of boric acid. H_3BO_3.
- Limit, P% + B% < 10%

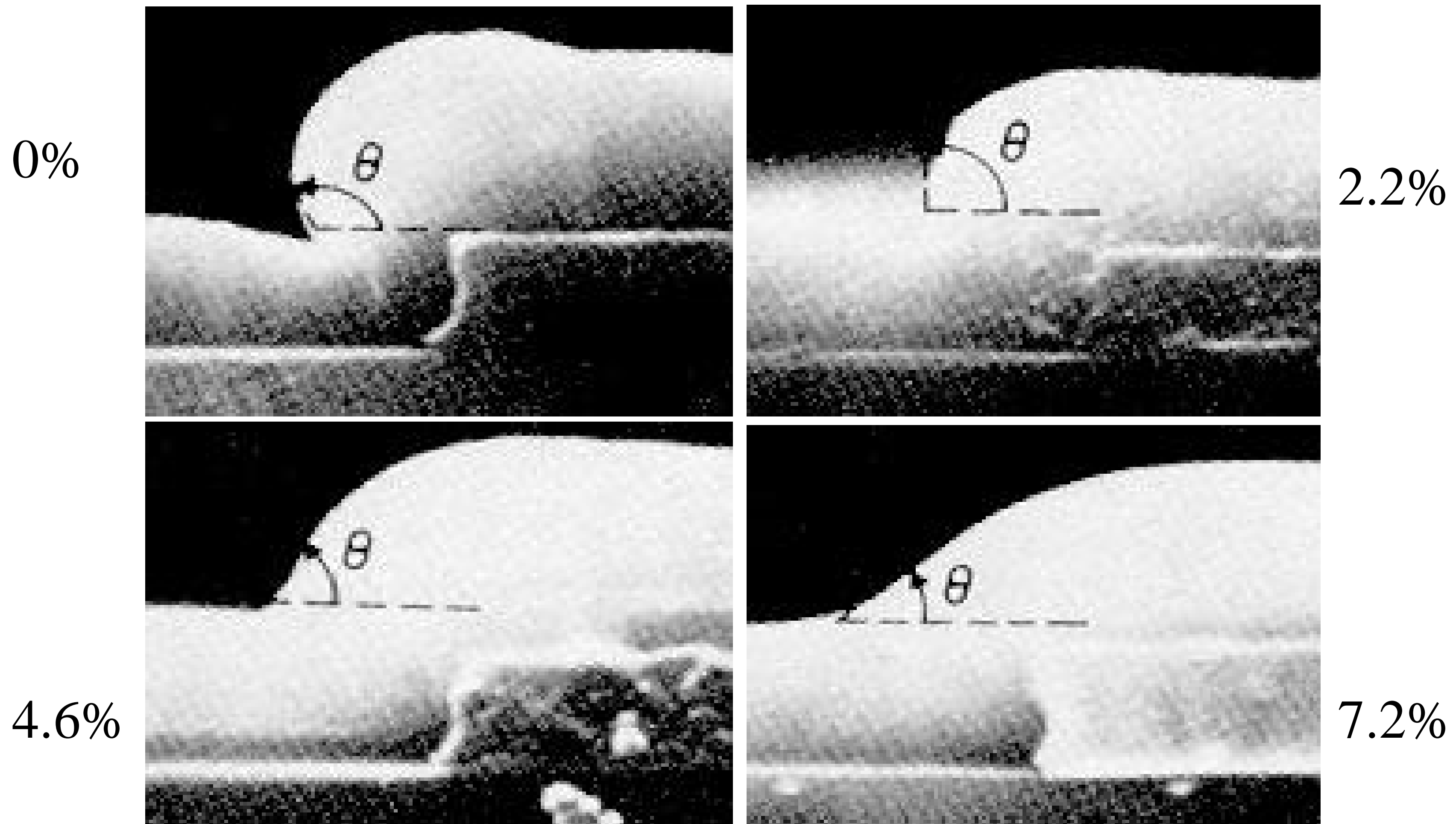
Question

- Silicon nitride is a better sodium barrier layer than silicon oxide. Why don't people just use nitride for PMD layer?

Answer

- Silicon nitride has higher dielectric constant
- Using nitride can cause longer *RC* time delay and reduce circuit speed
- A thin layer of nitride (~ 200 Å) is commonly used as a diffusion barrier layer in the PMD application
- Prevent diffusion of phosphorus and boron from BPSG diffusing into source/drain

PSG Reflow at 1100 °C, N_2, 20 min.

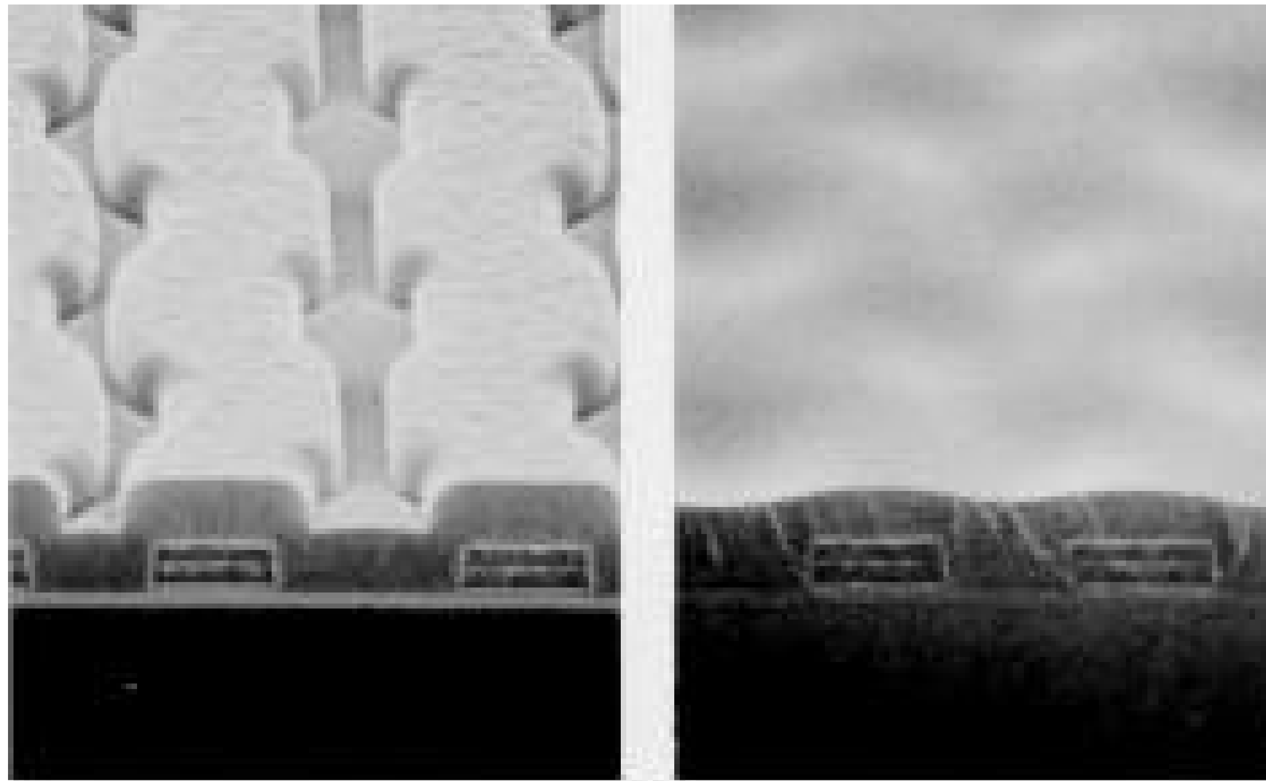


Source: *VLSI Technology*, by S.M. Sze

Some Facts about Sodium

Name	Sodium
Symbol	Na
Atomic number	11
Atomic weight	22.989770
Discoverer	Sir Humphrey Davy
Discovered at	England
Discovery date	1807
Origin of name	From the English word "soda" (the origin of the symbol Na comes from the Latin word "natrium")
Density of solid	0.968 g/cm^3
Molar volume	23.78 cm^3
Velocity of sound Electrical resistivity	3200 m/sec 4.7 $\mu\Omega\cdot$cm
Reflectivity	No data
Melting point	97.72 °C
Boiling point	882.85 °C
Thermal conductivity	140 $W\ m^{-1}\ K^{-1}$
Coefficient of linear thermal expansion	$71\times10^{-6}\ K^{-1}$
Applications	Major contaminant, needs to be strictly controlled
Main removal agent	HCl
Barrier materials used	Silicon nitride and PSG

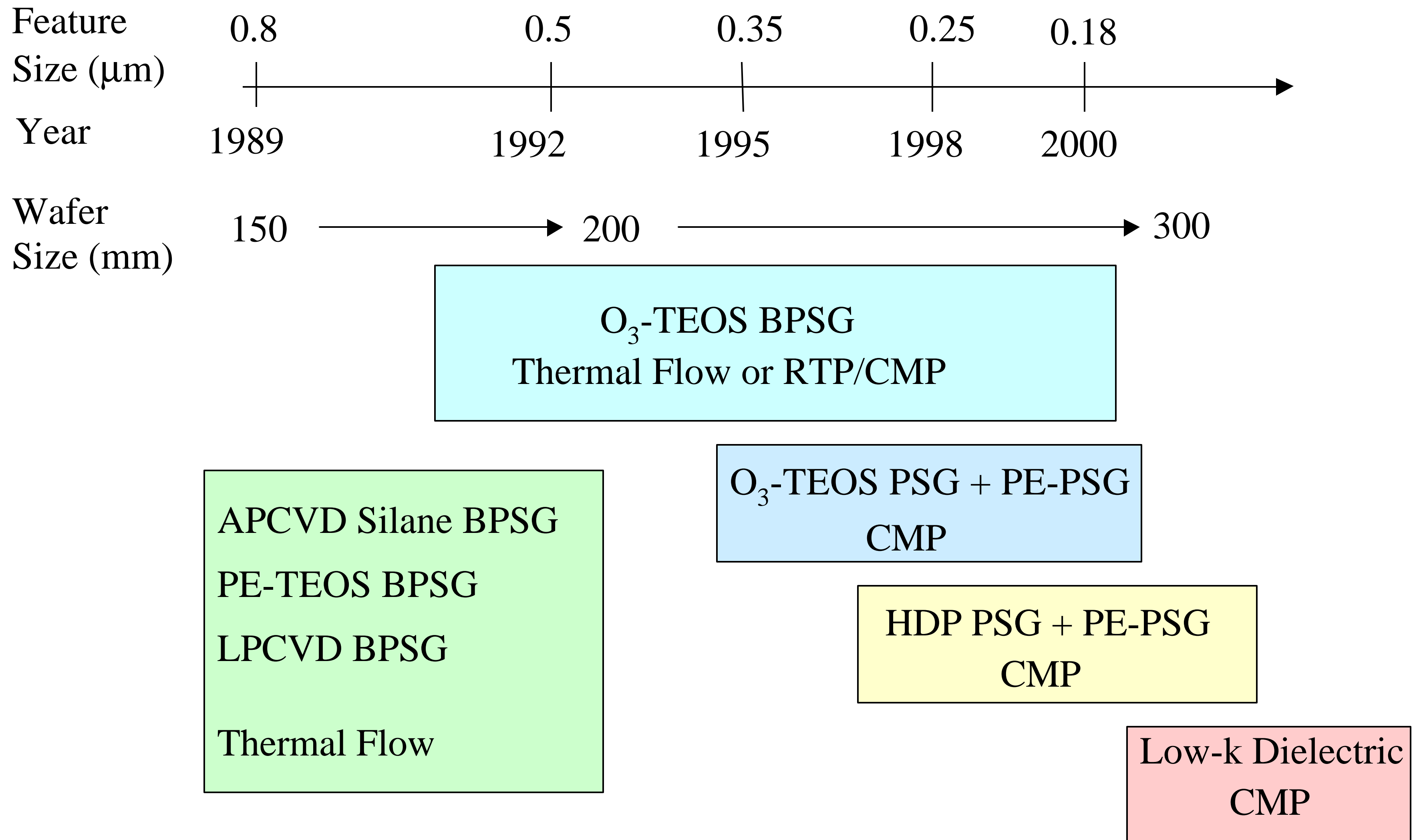
4×4 BPSG Reflow at 850 °C, 30 Minutes in N_2 Ambient



Development of PMD Processes

Dimension	PMD	Planarization	Reflow temperature
> 2 μm	PSG	Reflow	1100°C
2 - 0.35 μm	BPSG	Reflow	850 - 900°C
0.25 μm	BPSG	Reflow + CMP	750°C
0.18 μm	PSG	CMP	-

PMD Applications Roadmap

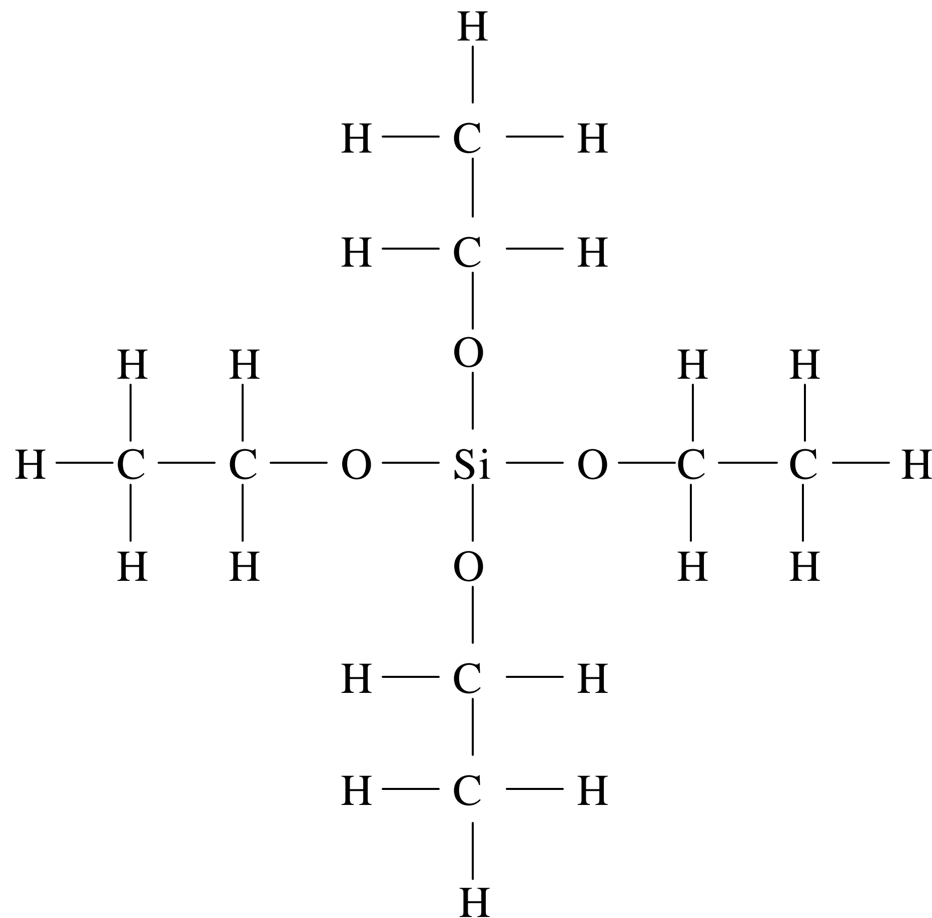


IMD

- Inter-metal dielectric
- Undoped silicate glass (USG) or FSG
- SOG
- Gap fill and planarization
- Temperature limited by metal melting
  - Normally 400 °C
- PE-TEOS, O_3-TEOS, and HDP

TEOS

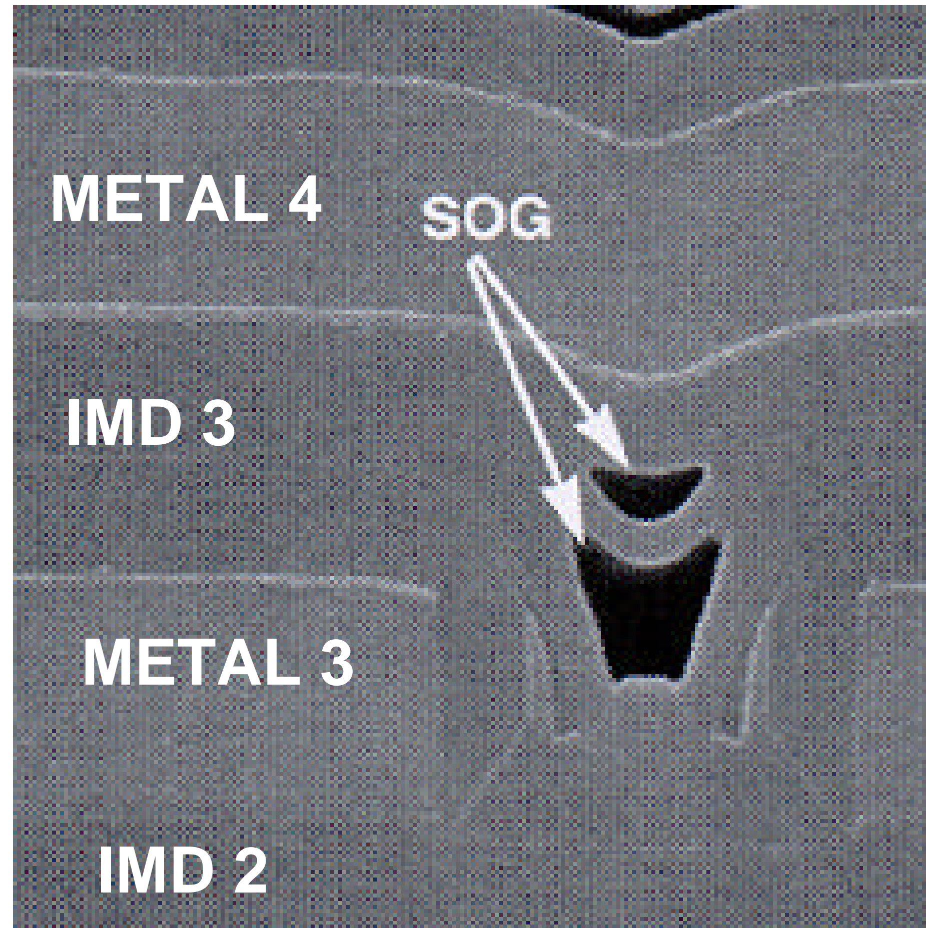
- Tetraethyloxysilane, $Si(OC_2H_5)_4$
- Liquid silicon source
- Commonly used for SiO_2 deposition
- Good step coverage and gap fill



PE-TEOS

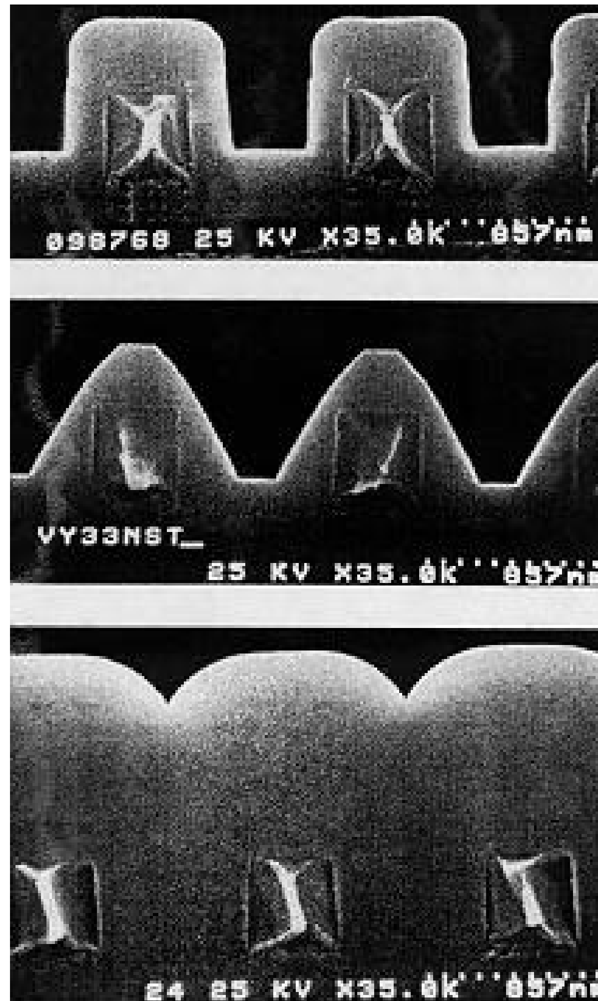
- Plasma-enhanced TEOS CVD processes
- TEOS and O_2
- Most commonly used dielectric CVD process
- Deposit USG at ~400 °C
- Mainly for IMD

Spin-on Glass (SOG) Processes



PE-TEOS

Photo courtesy:
Applied Materials



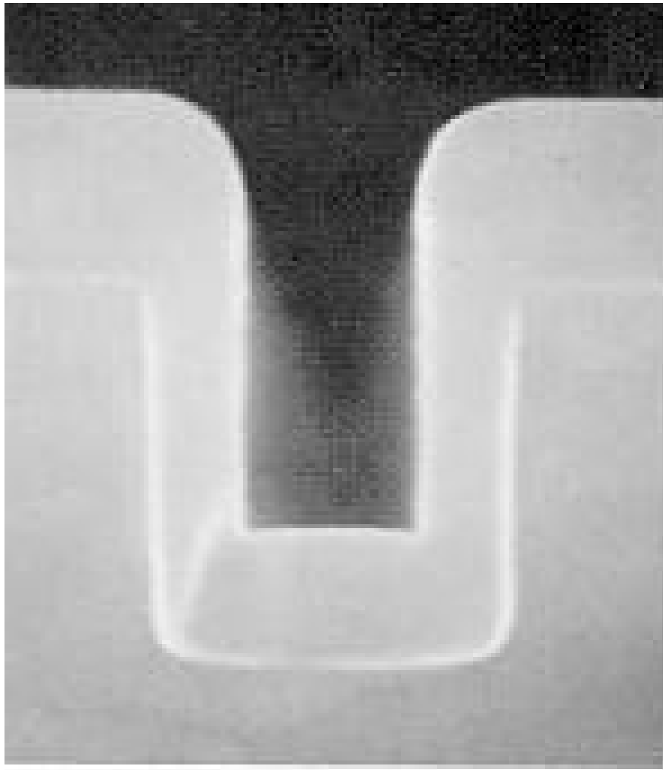
- PE-TEOS
- Sputtering etchback
- PE-TEOS

O_3-TEOS

- TEOS and Ozone
- $O_3 \rightarrow O_2 + O$ (half-life time: 86 hours at 22 °C, < 1ms at 400 °C)
- $O + TEOS \rightarrow USG$ + other volatile byproducts
- Excellent step coverage and gap fill.
- Applied for IMD and PMD

O_3-TEOS vs PE-TEOS

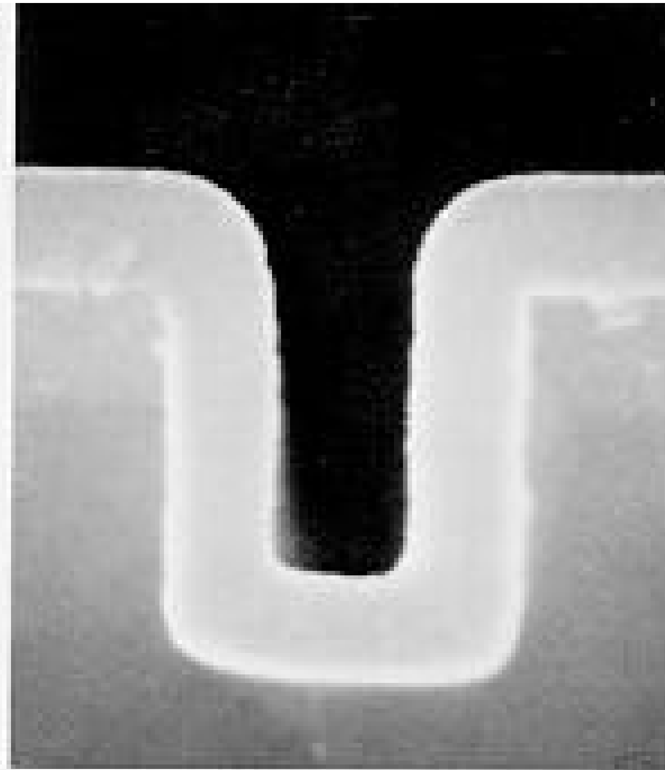
PE-TEOS



Step coverage: 50%

Conformality: 87.5%

Ozone-TEOS



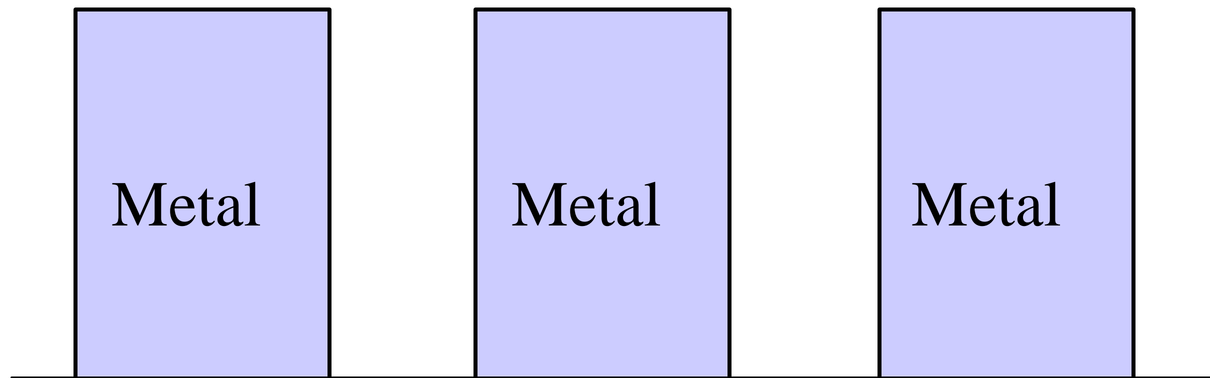
Step coverage: 90%

Conformality: 100%

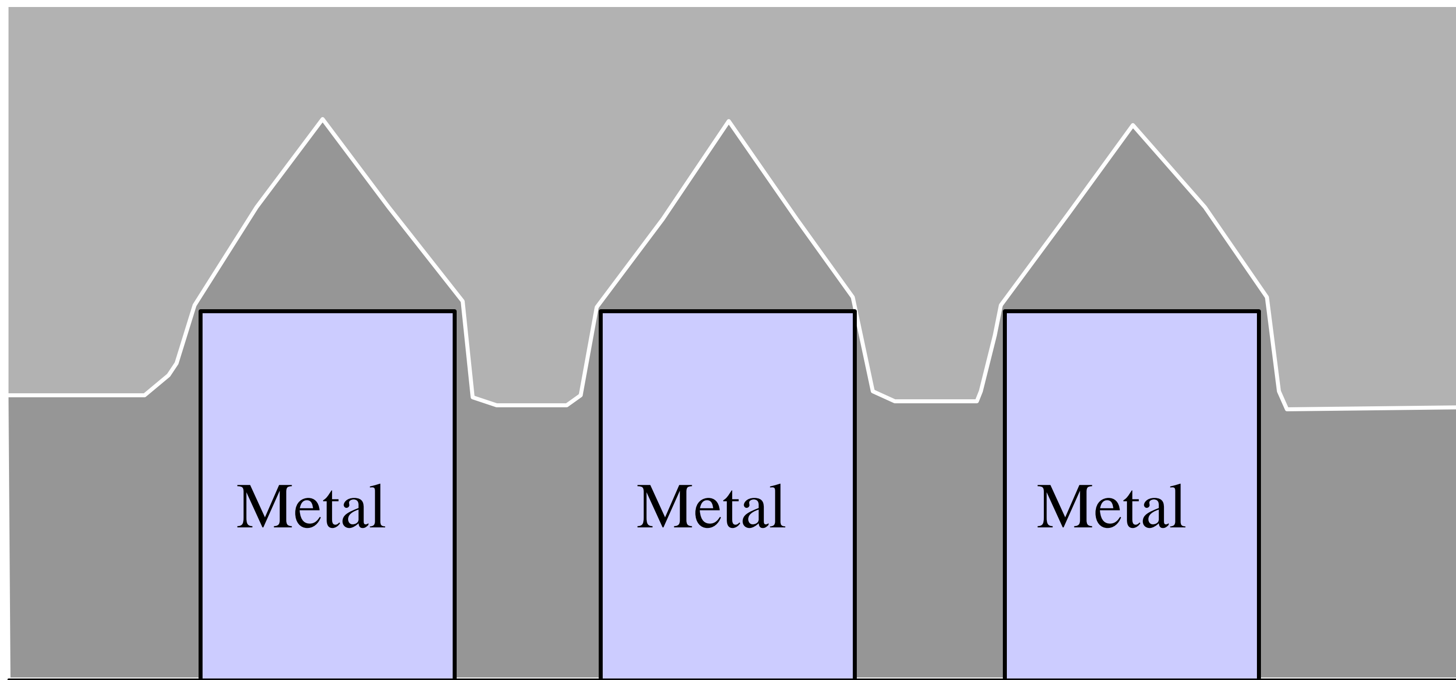
High Density Plasma CVD

- HDP-CVD: deposition and sputtering etch at the same time.
- USG for STI application
- USG and FSG for IMD applications
- PMD for PMD application

HDP-CVD, IMD Application



Oxide CMP



Passivation

- Nitride and oxide
- Nitride is very good barrier layer, oxide help nitride stick with metal
- Silane process
- NH_3, N_2 and nitrogen precursors, N_2O as oxygen precursor
- In-situ CVD process

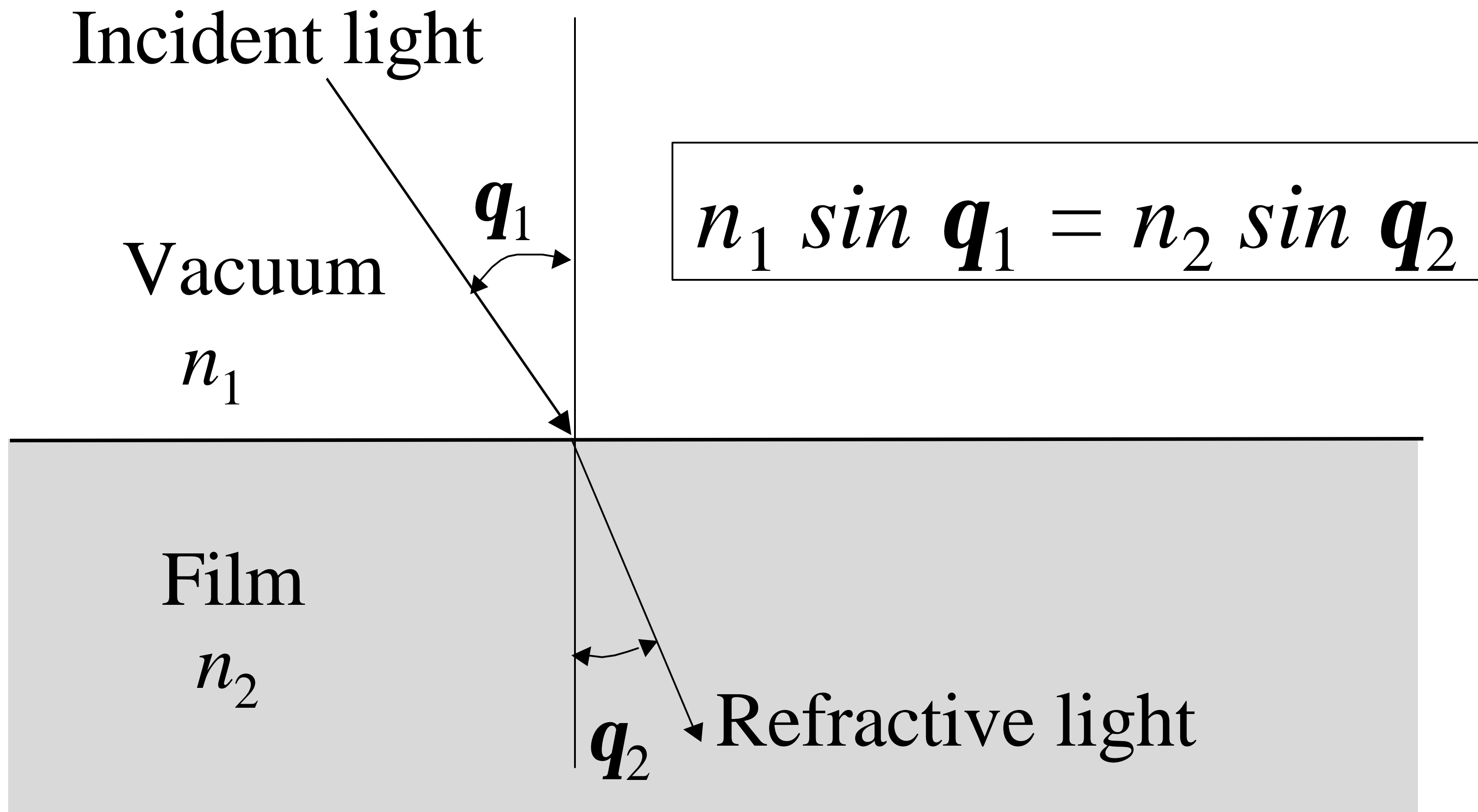
Dielectric Thin Film Characteristics

- Refractive index
- Thickness
- Uniformity
- Stress
- Particles

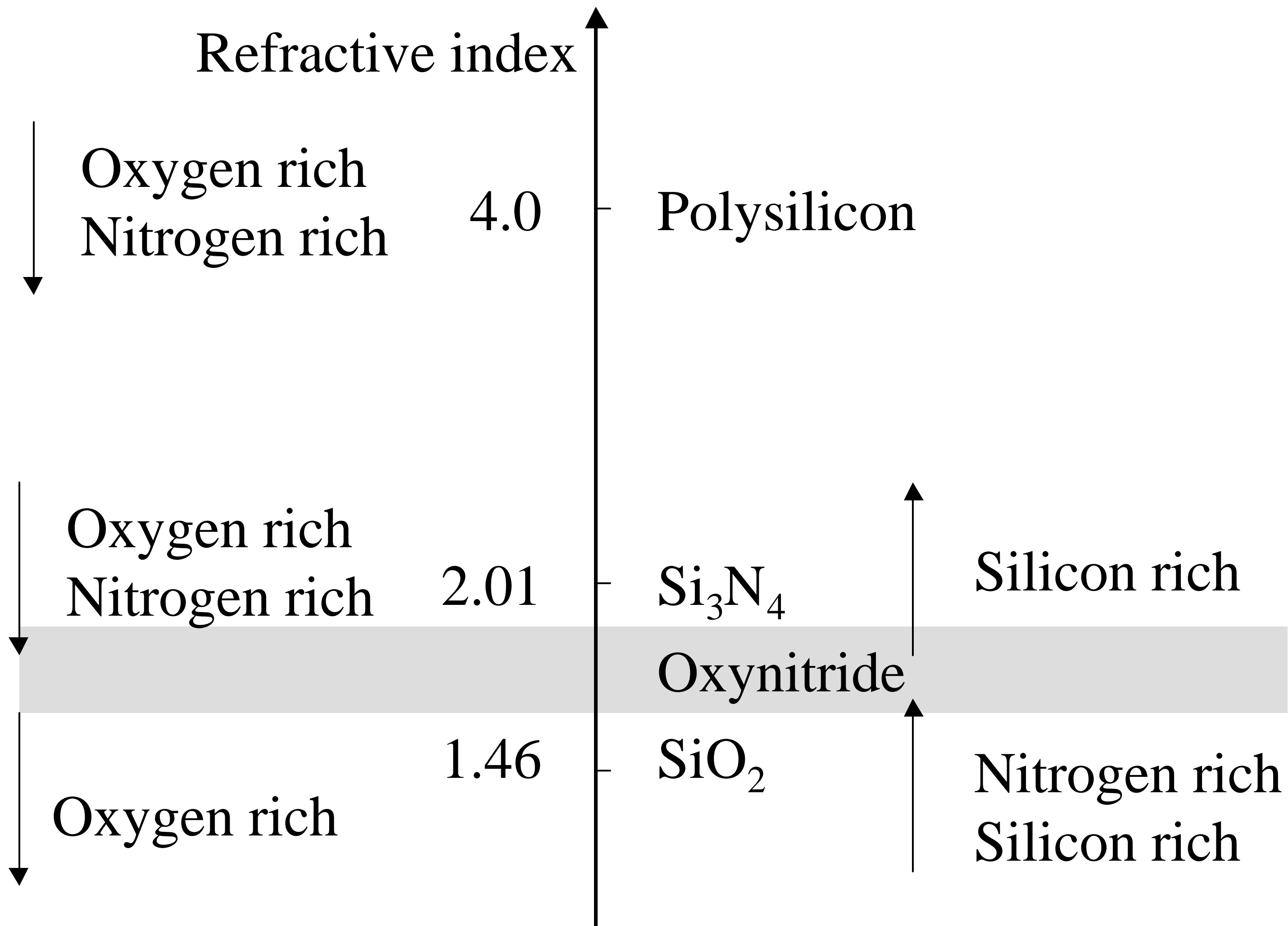
Refractive Index

$$\text{Refractive index, } n = \frac{\text{Speed of light in vacuum}}{\text{Speed of light in the film}}$$

Refractive Index



Film Information from R.I.



Ellipsometry R.I. Measurement

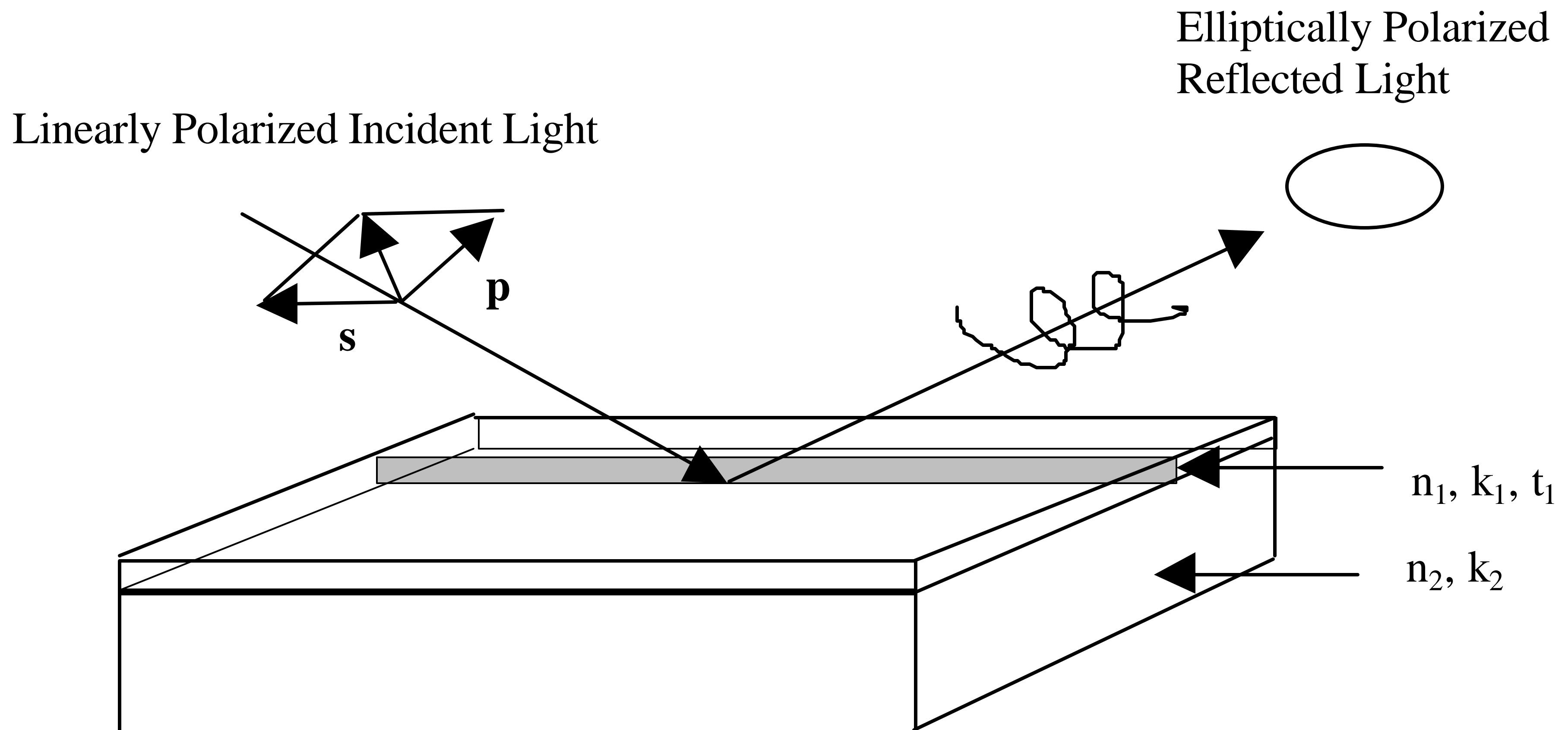
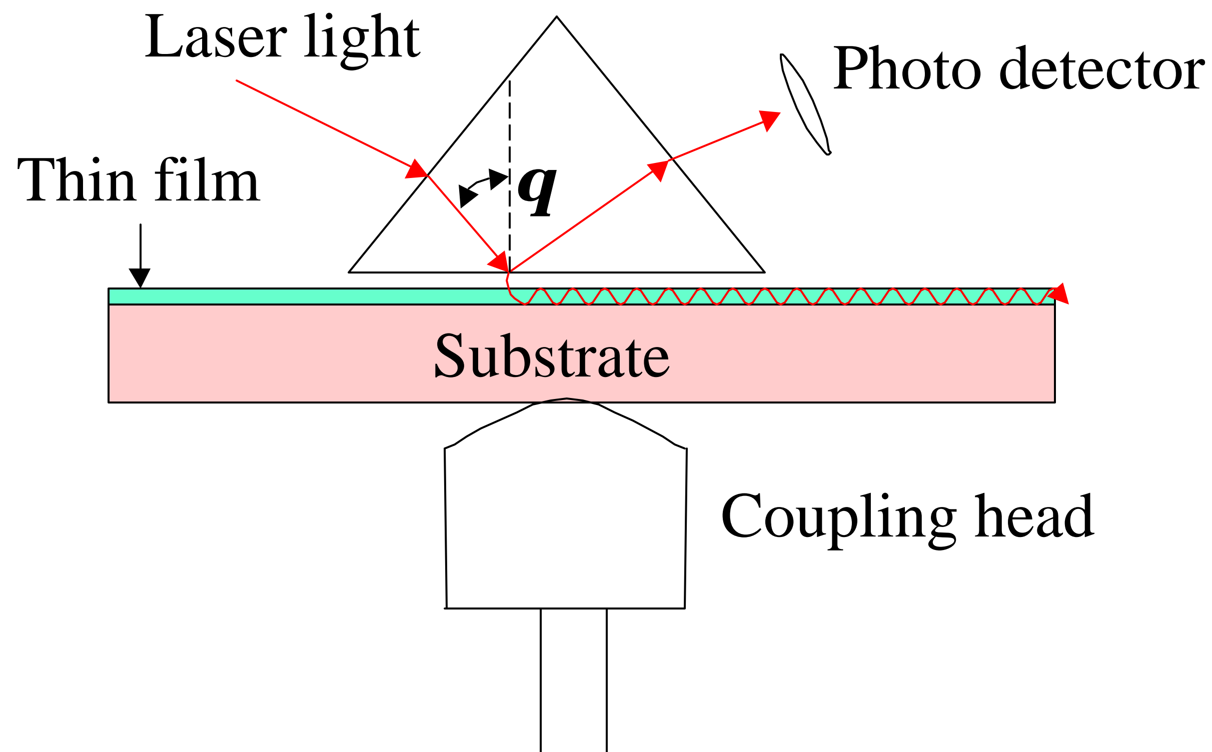
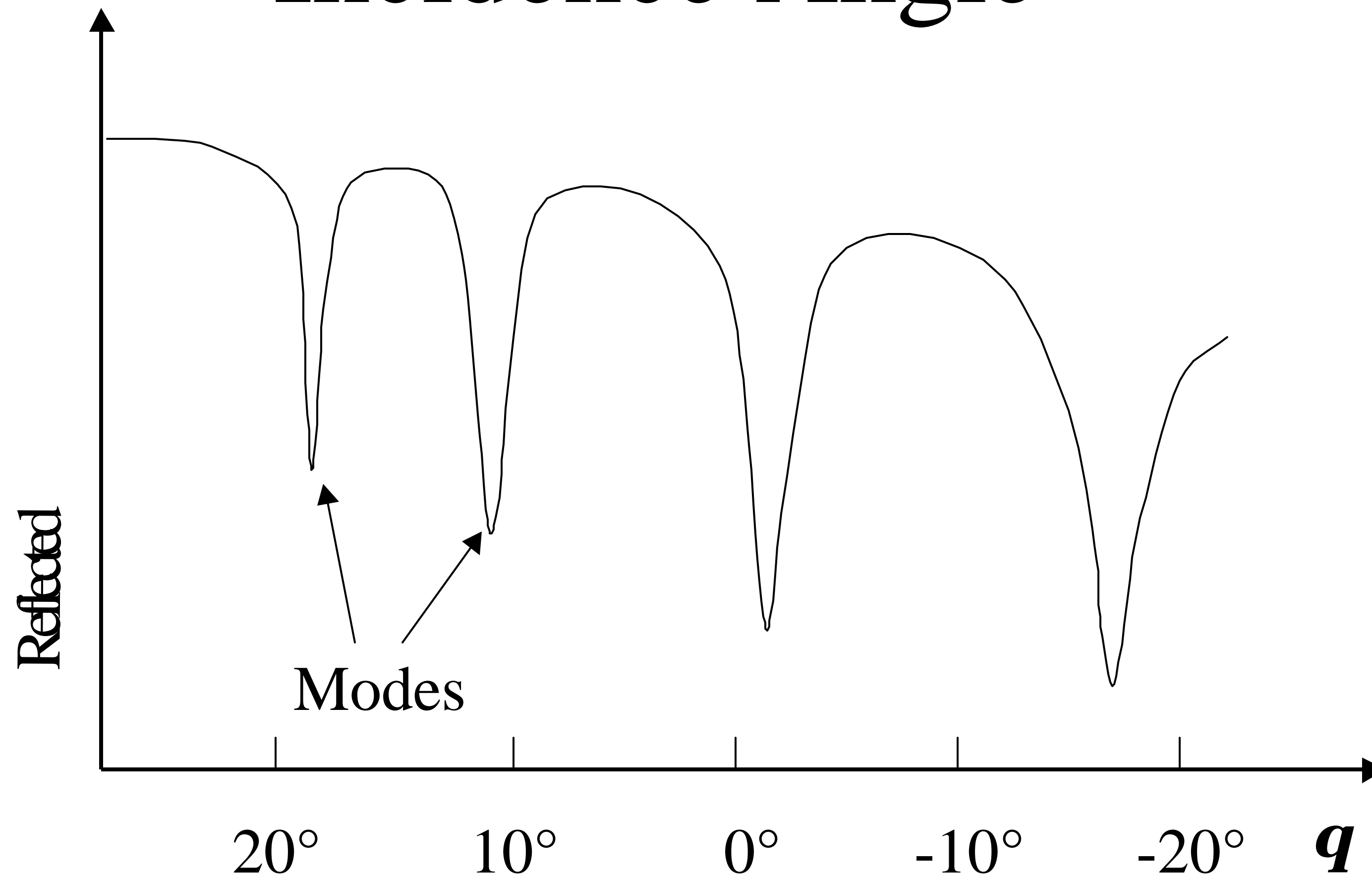


Illustration of Prism Coupler



Reflected Light Intensity vs. Incidence Angle



Metricon Model 2010 Prism Coupler

Comparison of the Two Methods

Ellipsometry

- Need know rough film thickness before hand
- Can measure thickness if R.I. is know

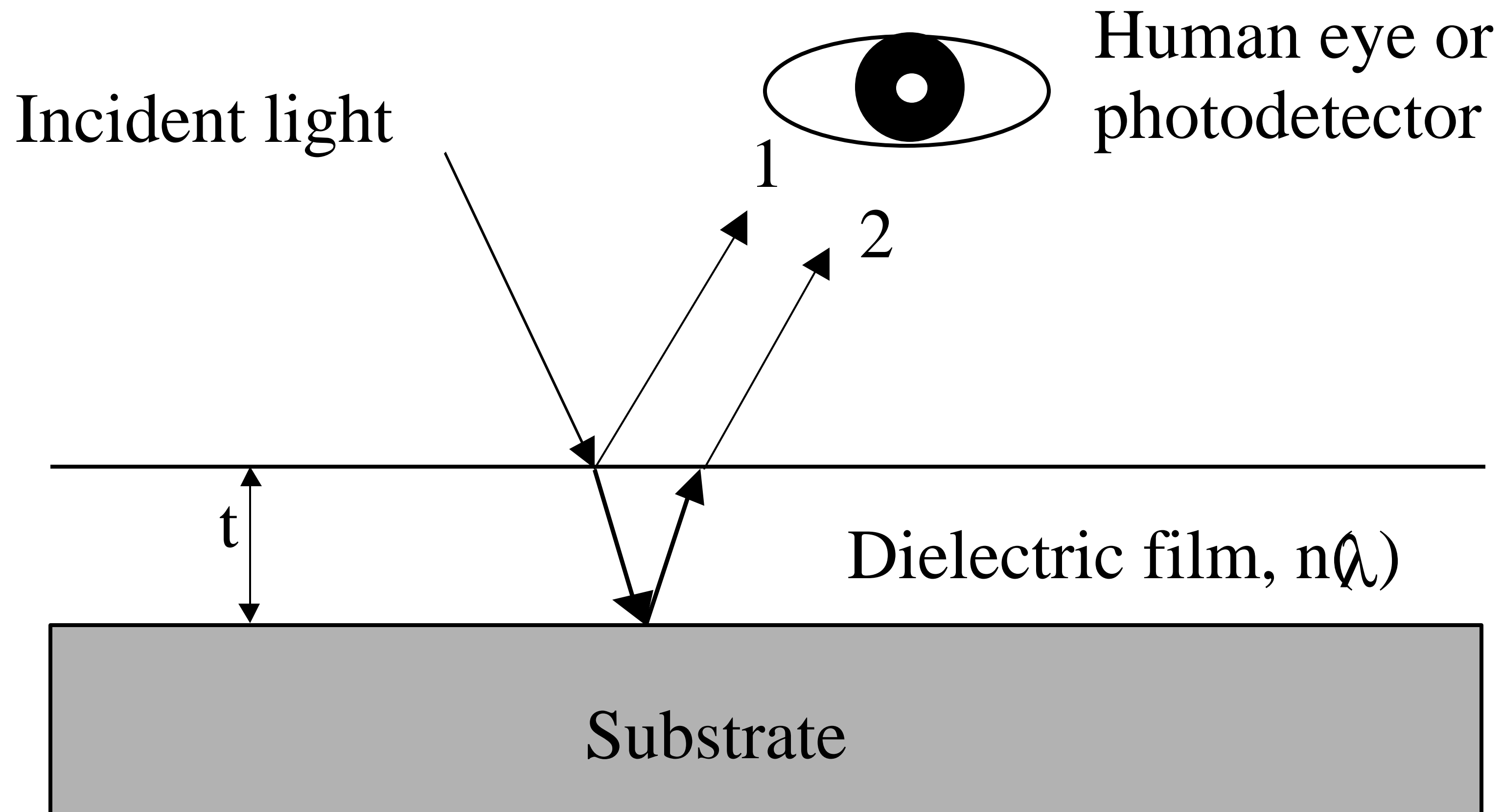
Prism coupler

- Need certain thickness of the film, > 3000 Å
- Can measure thickness if film thick enough to support enough modes

Thickness Measurement

- One of the most important measurements for dielectric thin film processes.
- Determines
  - Film deposition rate
  - Wet etch rate
  - Shrinkage

Dielectric Thin Film Thickness Measurement



Dielectric Thin Film Thickness Measurement

- Different thickness has different color
- Tilting wafer also changes the color

Question

- If you see some beautiful color rings on a wafer with a CVD dielectric layer, what is your conclusion?

Answer

- Color change indicates the dielectric thin film thickness change, thus we know the film with the color rings must have problem with thickness uniformity, which is most likely caused by a non-uniform thin film deposition process.

Question

- Why does the thin film color change when one look at the wafer from different angle?

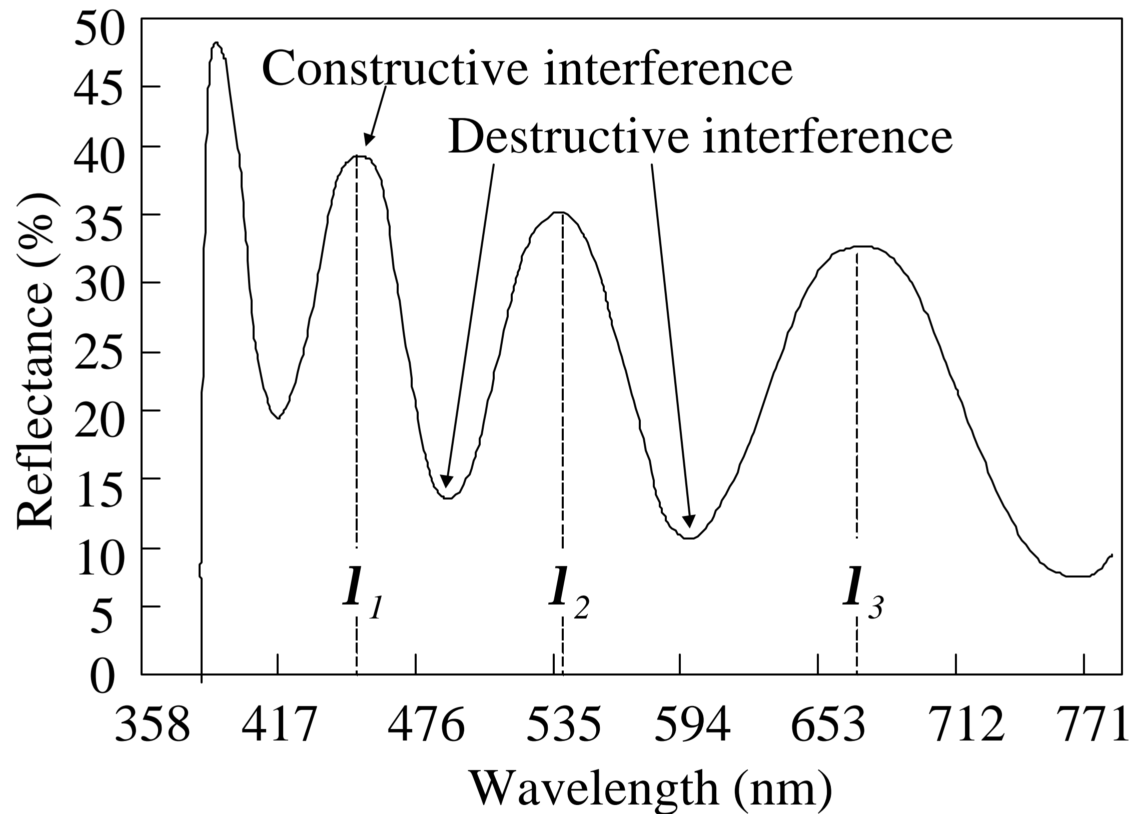
Answer

- When one looking at wafer from a different angle, phase shift will change, thus wavelength for constructive interference will change, which causes color change
- It is important to hold the wafer straight when using the color chart to measure film thickness
- Tilt wafer makes the film thickness thicker than it actually is

Spectroreflectometry

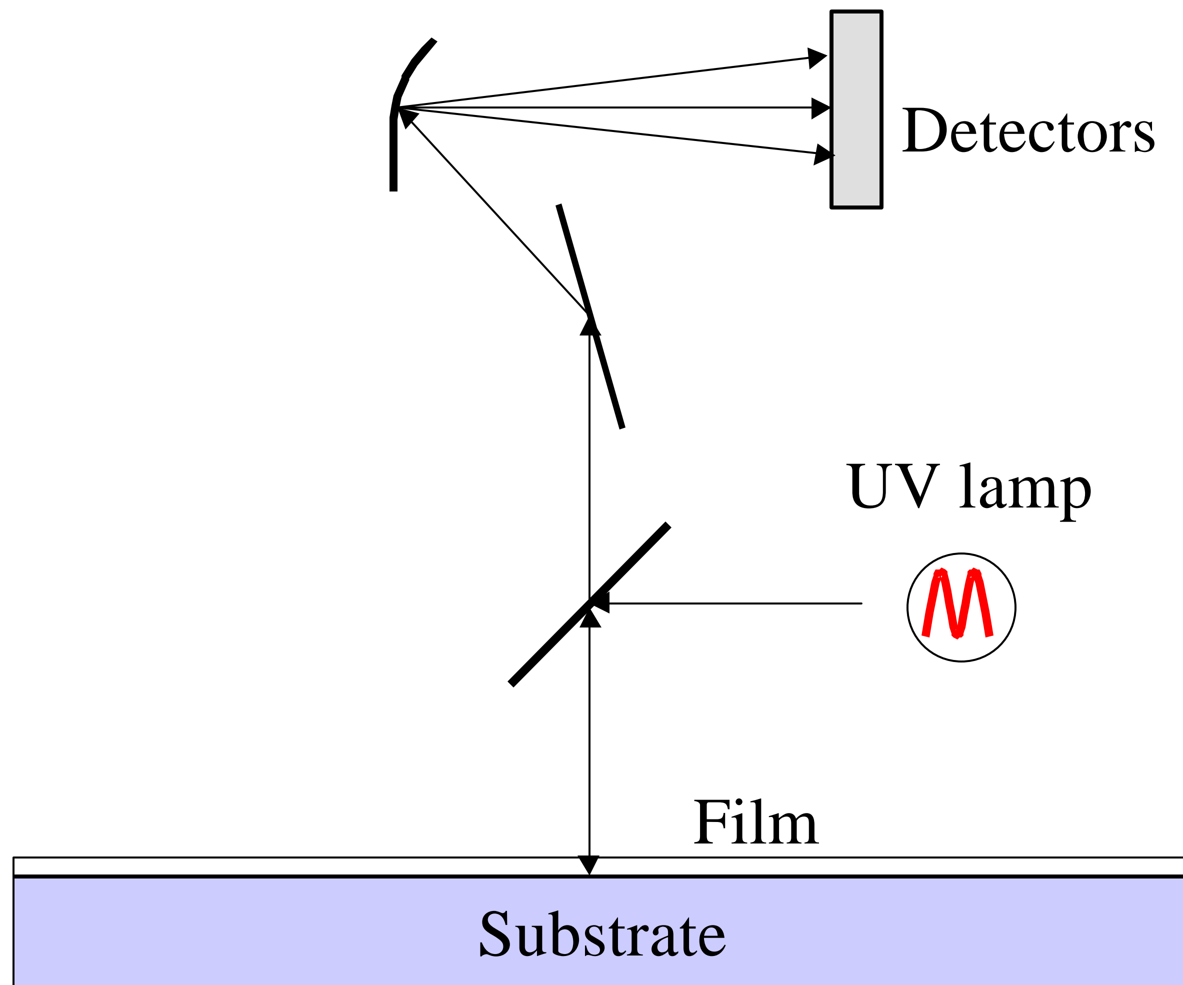
- Measure the reflected light intensity at different wavelengths
- Calculate thin film thickness from the relationship between reflected light intensity and wavelength.
- Photodetector is more sensitive than human eyes
- Spectroreflectometry can obtain much higher resolution and accuracy for the film thickness

Relation of Reflectance and Wavelength



$$\frac{1}{\lambda_m} - \frac{1}{\lambda_{m+1}} = \frac{1}{2nt}$$

Spectroreflectometry System



Question

- Many advance thin film thickness measurement tools allows user to choose the refractive index of the film. If someone mistakenly chooses the PE-TEOS USG film refractive index to measure O_3-TEOS USG films thickness, what will be the effect on the measurement result?

Answer

- Since the *nt* always coupled together
- A wrong *n* will cause wrong *t* measurement
- O_3-TEOS USG is a porous film and has a R.I., about 1.44
- Slightly lower than 1.46 of PE-TEOS USG
- Measured O_3-TEOS film thickness will be slightly thinner than its actual value

Deposition Rate

$$\text{Deposition Rate} = \frac{\text{Thickness of deposited film}}{\text{Deposition time}}$$

Wet Etch Rate

$$\text{Wet Etch Rate} = \frac{\text{Thickness change after etch}}{\text{Etch time}}$$

$$\text{Wet etch rate ratio} = \frac{\text{Thickness change of the CVD film}}{\text{Thickness change of the thermal oxide film}}$$

Uniformity

- Multi-point measurement
- Definition
- Average: $\bar{x} = \dfrac{x_1 + x_2 + x_3 + \cdots + x_N}{N}$
- Standard deviation:

$$\boldsymbol{s} = \sqrt{\frac{(x_1 - \bar{x})^2 + (x_2 - \bar{x})^2 + (x_3 - \bar{x})^2 + \cdots + (x_N - \bar{x})^2}{N - 1}}$$

- Standard deviation non-uniformity: $\boldsymbol{s}/\bar{x}$

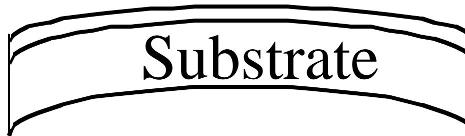
Stress

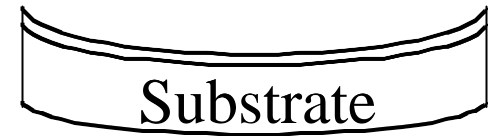
- Mismatch between different materials
- Two kinds of stresses, intrinsic and extrinsic
- Intrinsic stress develops during the film nucleation and growth process.
- The extrinsic stress results from differences in the coefficients of thermal expansion
- Tensile stress: cracking film if too high
- Compressive stress: hillock if too strong

Film Stress

Bare Wafer

After Thin Film Deposition

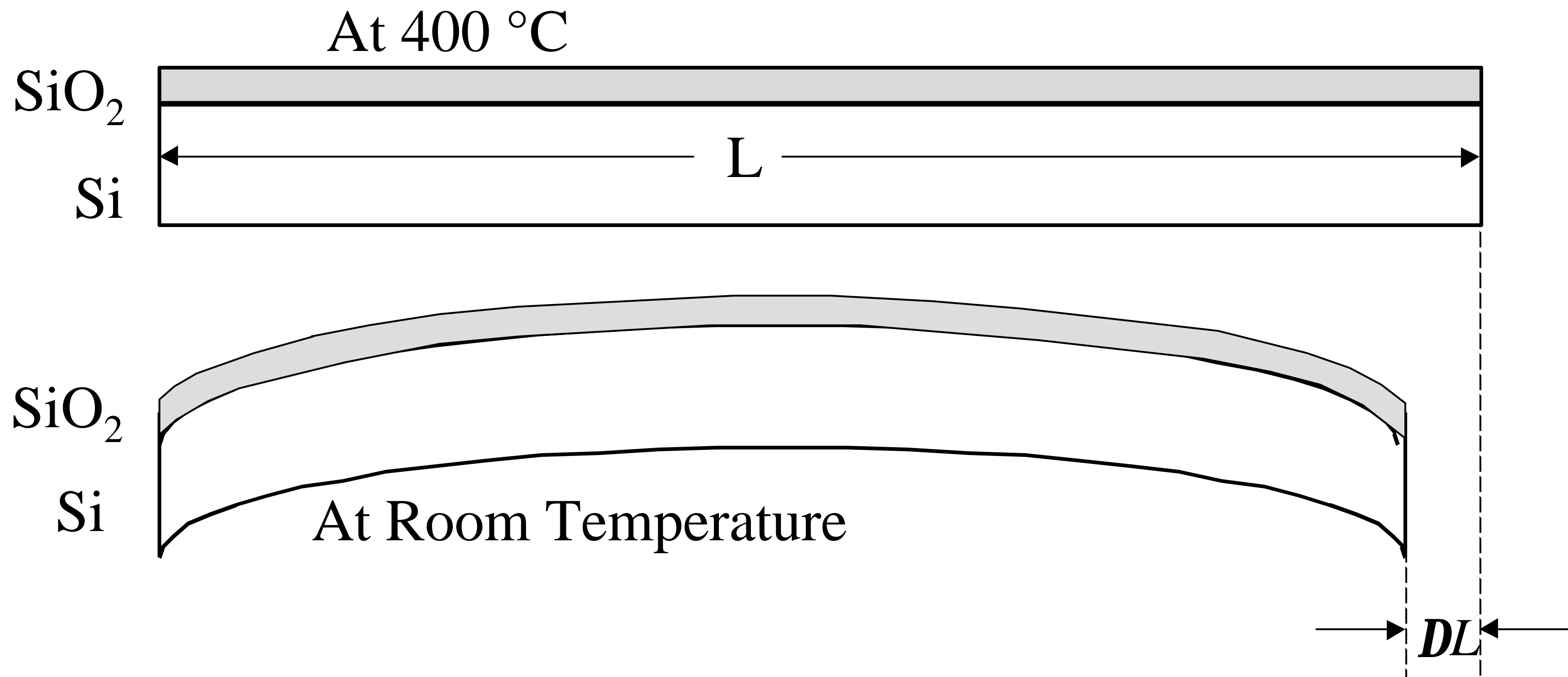




Compressive Stress
Negative curvature

Tensile Stress
Positive curvature

Illustration of Thermal Stress



$$DL = a\, DT\, L$$

Coefficients of Thermal Expansion

$\alpha(SiO_2) = 0.5\times10^{-6}\ °C^{-1}$

$\alpha(Si) = 2.5\times10^{-6}\ °C^{-1}$

$\alpha(Si_3N_4) = 2.8\times10^{-6}\ °C^{-1}$

$\alpha(W) = 4.5\times10^{-6}\ °C^{-1}$

$\alpha(Al) = 23.2\times10^{-6}\ °C^{-1}$

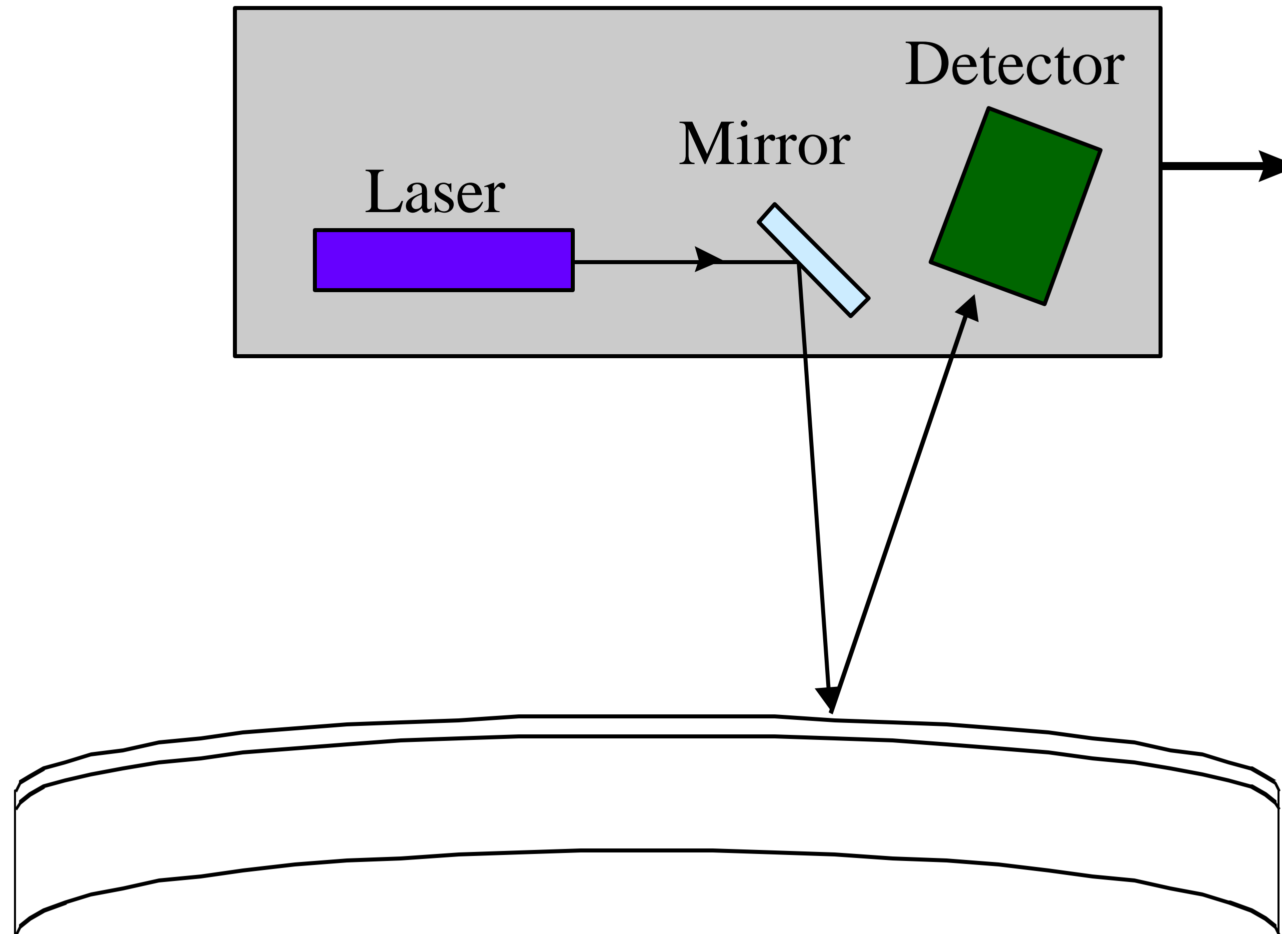
Stress Measurement

$$\boldsymbol{s} = \frac{E}{1-\boldsymbol{n}}\frac{h^2}{6t}\left(\frac{1}{R_2}-\frac{1}{R_1}\right)$$

Wafer curvature change before and after thin film deposition

Laser beam scans wafer surface, reflection light indicates the wafer curvature

Stress Measurement

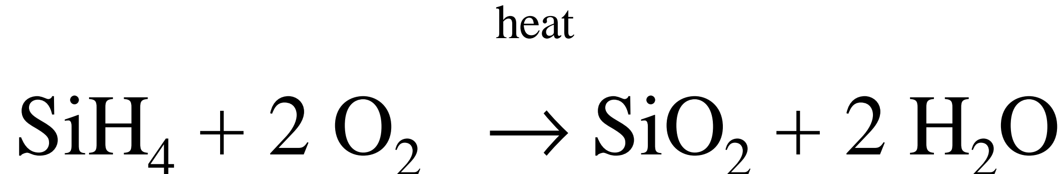


Dielectric CVD Processes

- Thermal Silane CVD Process
- Thermal TEOS CVD Process
- PECVD Silane Processes
- PECVD TEOS Processes
- Dielectric Etchback Processes
- O_3-TEOS Processes
- Spin-on Glass
- High Density Plasma CVD

Thermal Silane CVD Process

- Silane has been commonly used for silicon dioxide deposition with both APCVD and LPCVD process



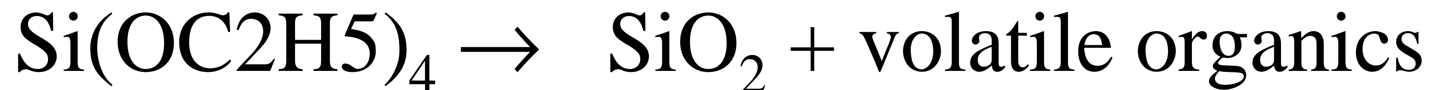
$$SiH_4 + 2\,O_2 \xrightarrow{\text{heat}} SiO_2 + 2\,H_2O$$

- APCVD normally uses diluted silane (3% in nitrogen) and LPCVD uses pure silane
- Not commonly used in the advanced fab

Thermal TEOS CVD Process

- TEOS: physisorption, high surface mobility
- TEOS film has better step coverage
- LPCVD TEOS dissociates at high temp:

700 °C

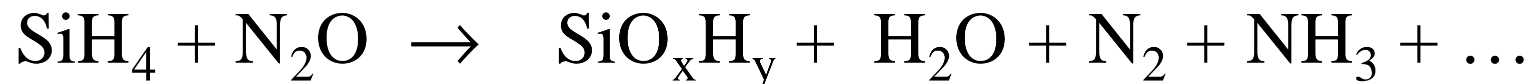


$$Si(OC2H5)_4 \rightarrow SiO_2 + \text{volatile organics}$$

- BPSG with TMB and TMP for PMD
- Temperature is too high for IMD

PECVD Silane Processes

- Silane and N_2O (laughing gas)
- Dissociation in plasma form SiH_2 and O
- Radicals react rapidly to form silicon oxide



$$SiH_4 + N_2O \xrightarrow[\text{heat}]{\text{plasma}} SiO_xH_y + H_2O + N_2 + NH_3 + \ldots$$

- Overflow N_2O, using SiH_4 flow to control deposition rate

Question

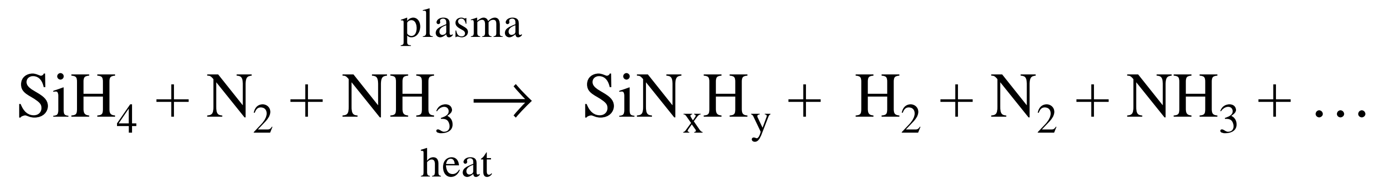
- Can we overflow silane and use nitrous oxide flow rate to controlled deposition rate?

Answer

- Theoretically we can, but practically no one should even try this
- It is very dangerous and not cost effective
- Overflowing silane will create a big safety hazard: fire and explosion
- Silane is more expensive than nitrous oxide

Passivation: Silicon Nitride

- Barrier layer for moisture and mobile ions
- The PECVD nitride
  - Low deposition temperature (<450ºC)
  - High deposition rate
  - Silane, ammonia, and nitrogen



$$SiH_4 + N_2 + NH_3 \xrightarrow[\text{heat}]{\text{plasma}} SiN_xH_y + H_2 + N_2 + NH_3 + \dots$$

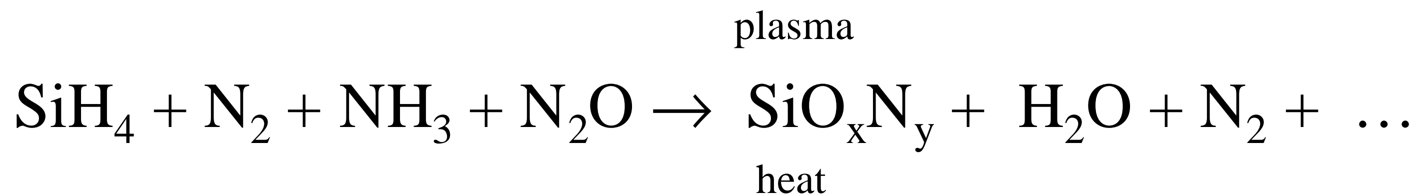
- Requires good step coverage, high dep. rate, good uniformity, and stress control

Passivation Dielectric Deposition

- Stabilization 1 (stabilize pressure)
- Oxide deposition (stress buffer for nitride)
- Pump
- Stabilization 2 (stabilize pressure)
- Nitride deposition (passivation layer)
- Plasma purging (eliminate SiH_4)
- Pump

EPROM Passivation Dielectric

- Need UV transparent passivation layer
- UV light can erase EPROM memory
- Oxynitride (SiO_xN_y) is commonly used
- Source gases: SiH_4, N_2, NH_3, and N_2O



$$SiH_4 + N_2 + NH_3 + N_2O \xrightarrow[\text{heat}]{\text{plasma}} SiO_xN_y + H_2O + N_2 + \ldots$$

- Properties in between oxide and nitride
  - UV transparent, and a fairly good barrier layer

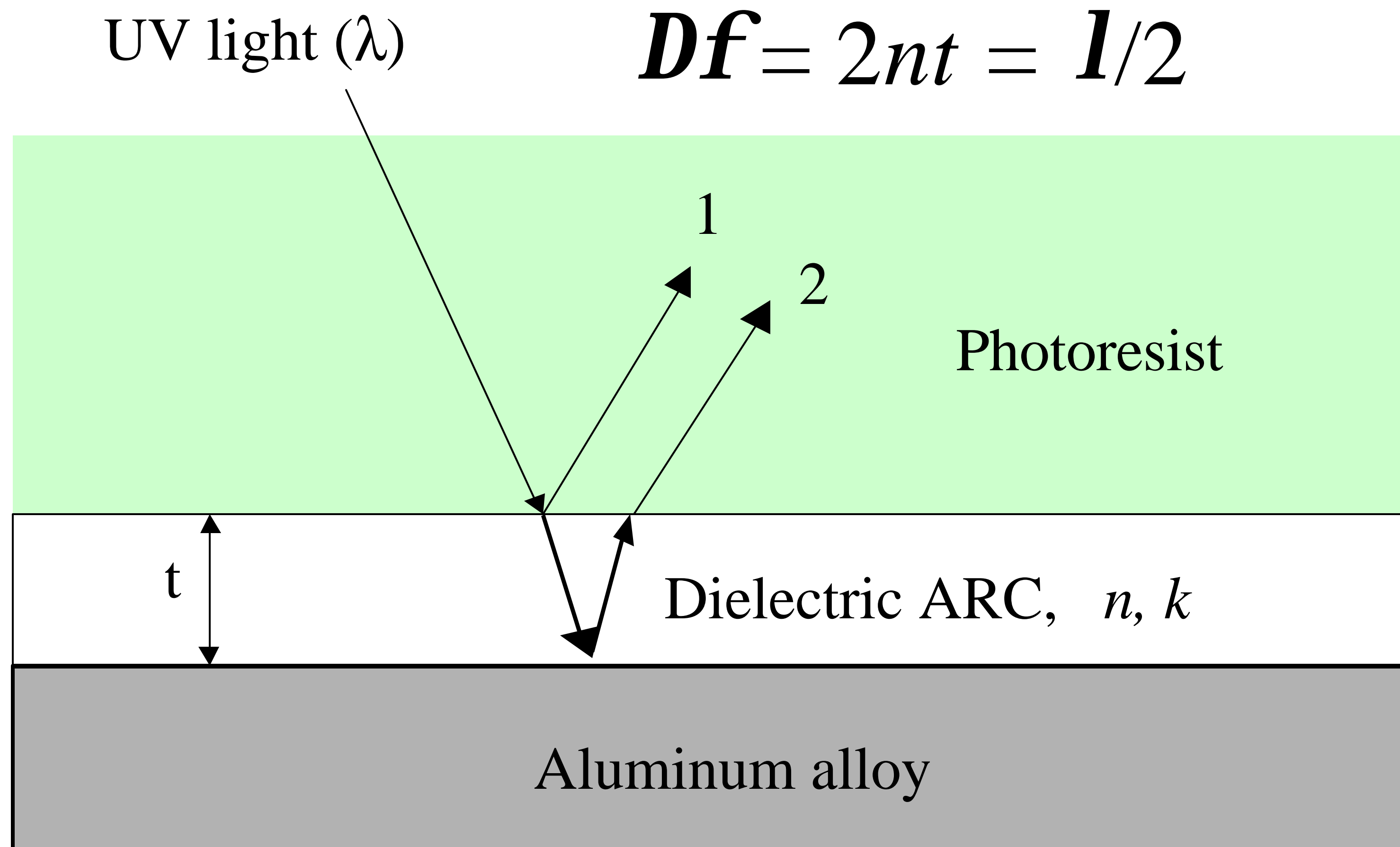
PMD Barrier Layer

- PSG or BPSG need a diffusion barrier layer
  - USG (need 1000 Å)
  - LPCVD nitride at ~700 ºC (~ 300 Å)
  - PECVD nitride at <550 ºC (< 200 Å)
- At higher temperature, PECVD nitride film has higher deposition rate, lower hydrogen concentration, and better film quality
- Possible in future: remote plasma CVD

Dielectric Anti-Reflective Coating

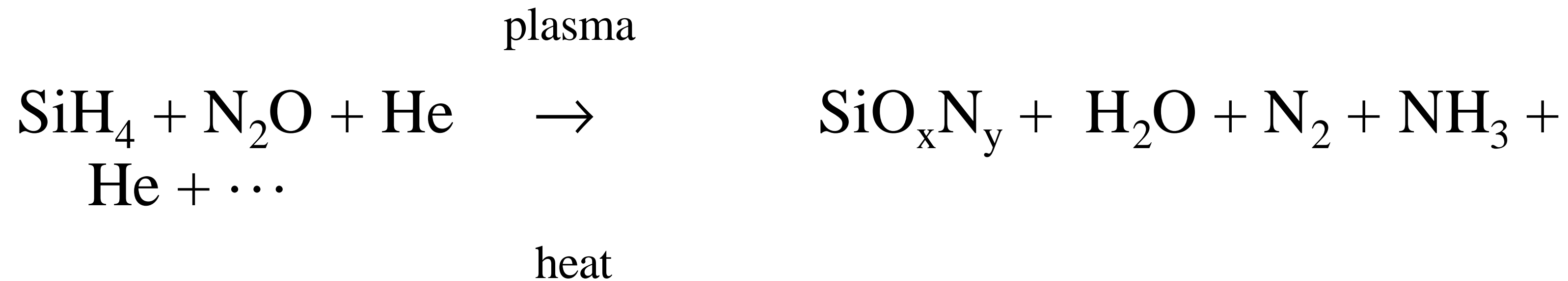
- High resolution for photolithography
- ARC layer is required to reduce the reflection
- Metallic ARC: TiN, 30% to 40% reflection
- No longer good enough for < 0.25 μm
- Dielectric ARC layer is used
  - Spin-on before photoresist coating
  - CVD

Dielectric Anti-Reflective Coating



Dielectric ARC

- PECVD silane process
- N_2O as oxygen and nitrogen source



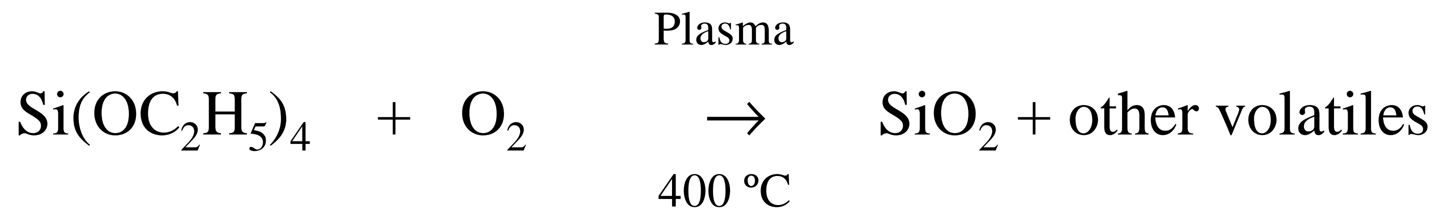
PE-TEOS

- Most widely used dielectric CVD process
- Fast
- Good uniformity
- Good step coverage

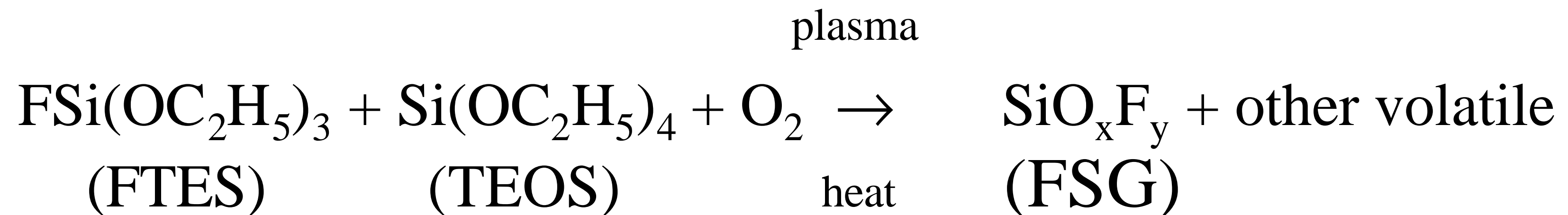
- Mainly used for IMD

PE-TEOS

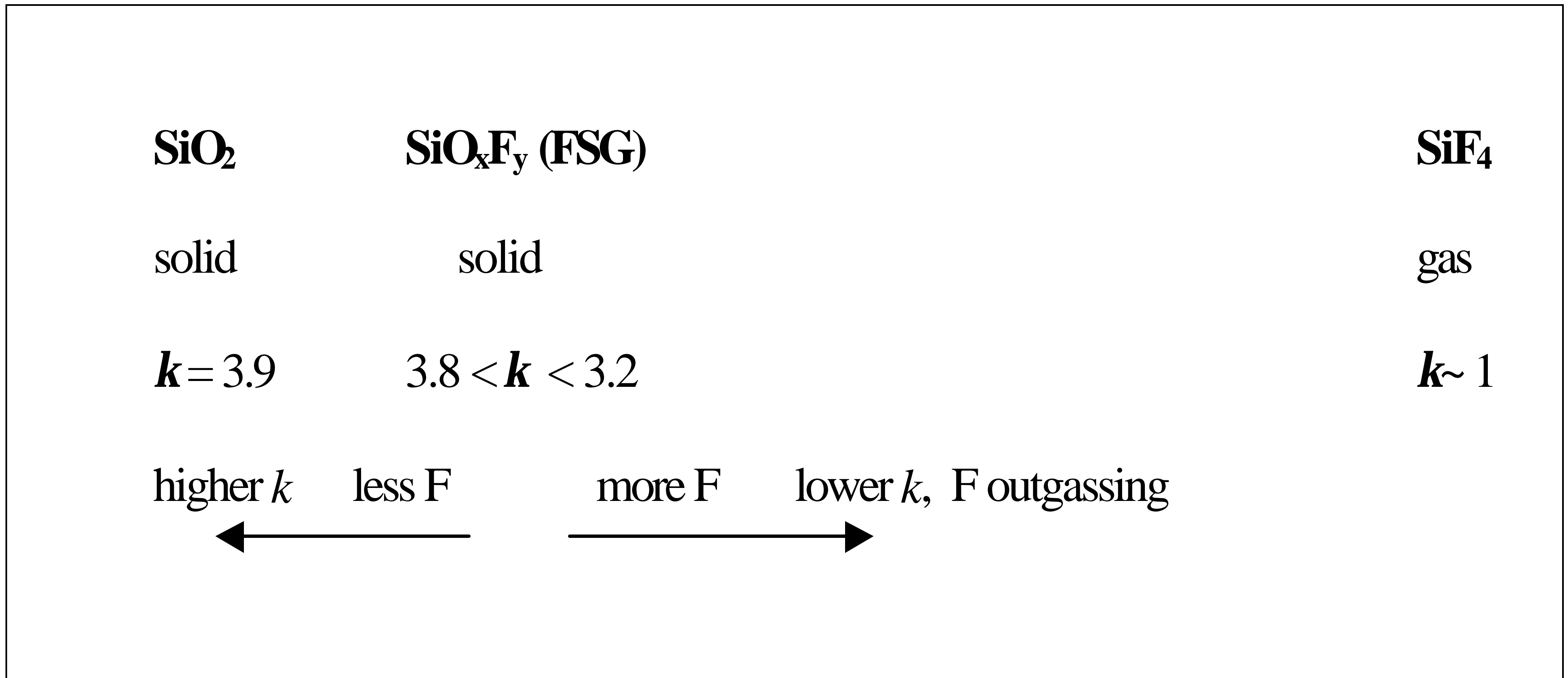
- USG process



- FGS process



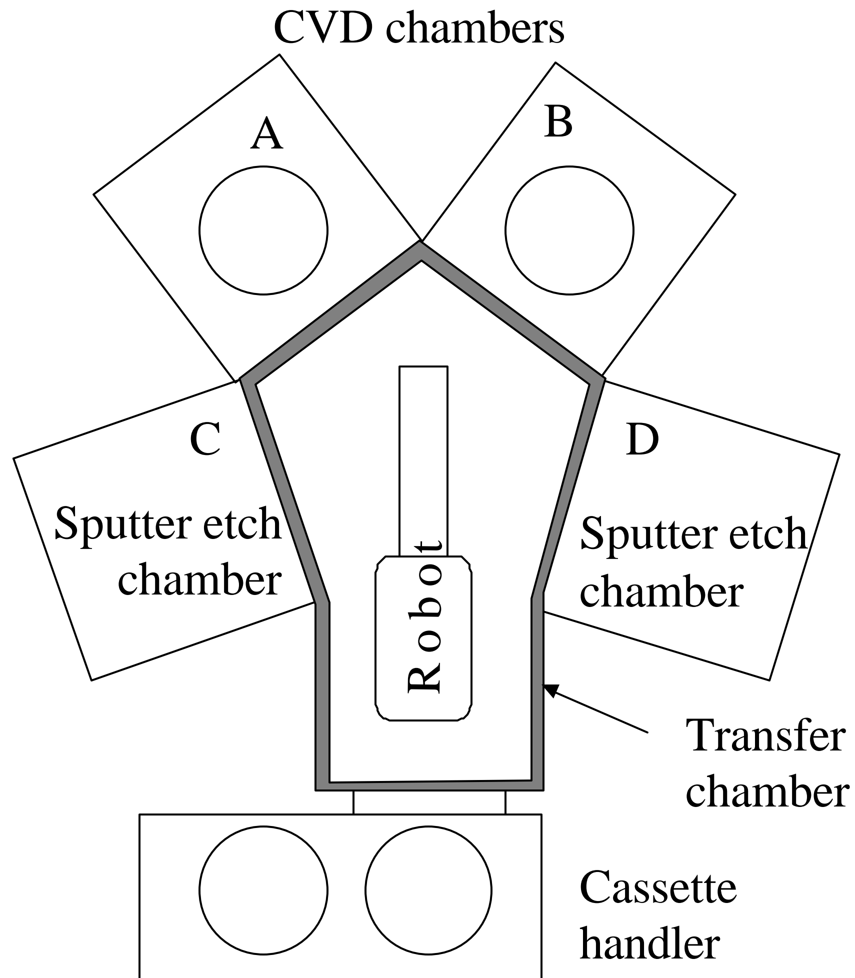
FSG Process Trends

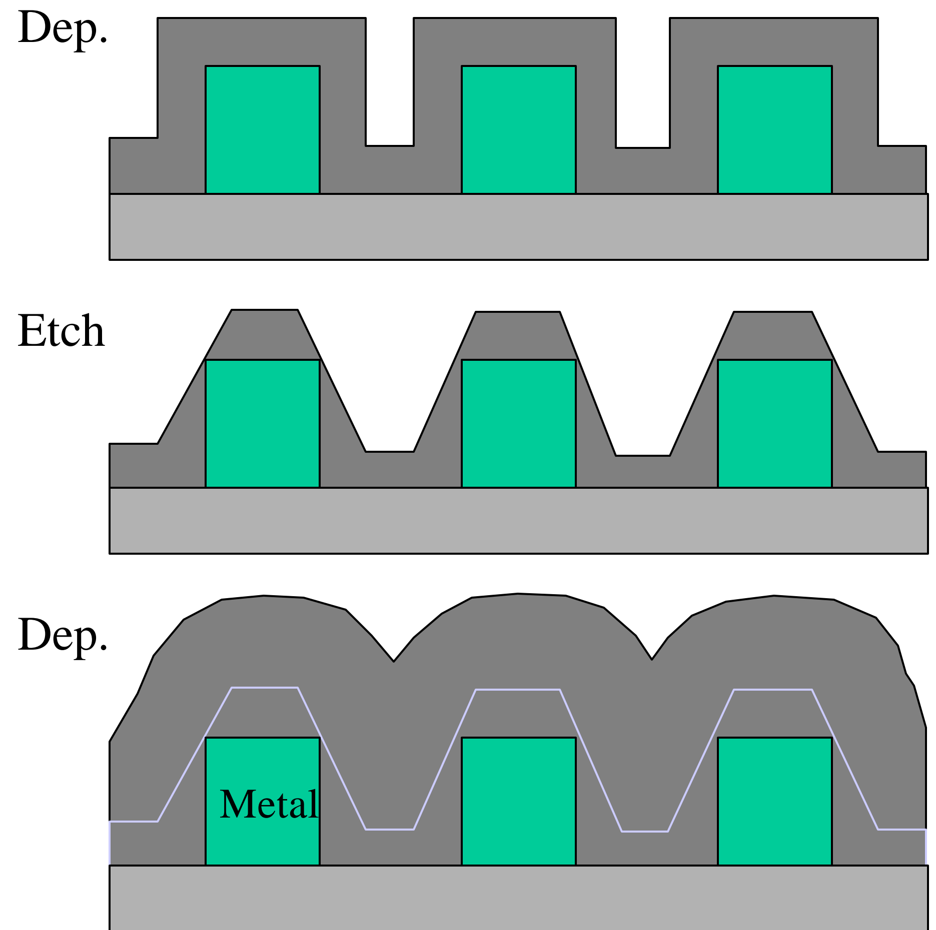


Dielectric Etchback Processes

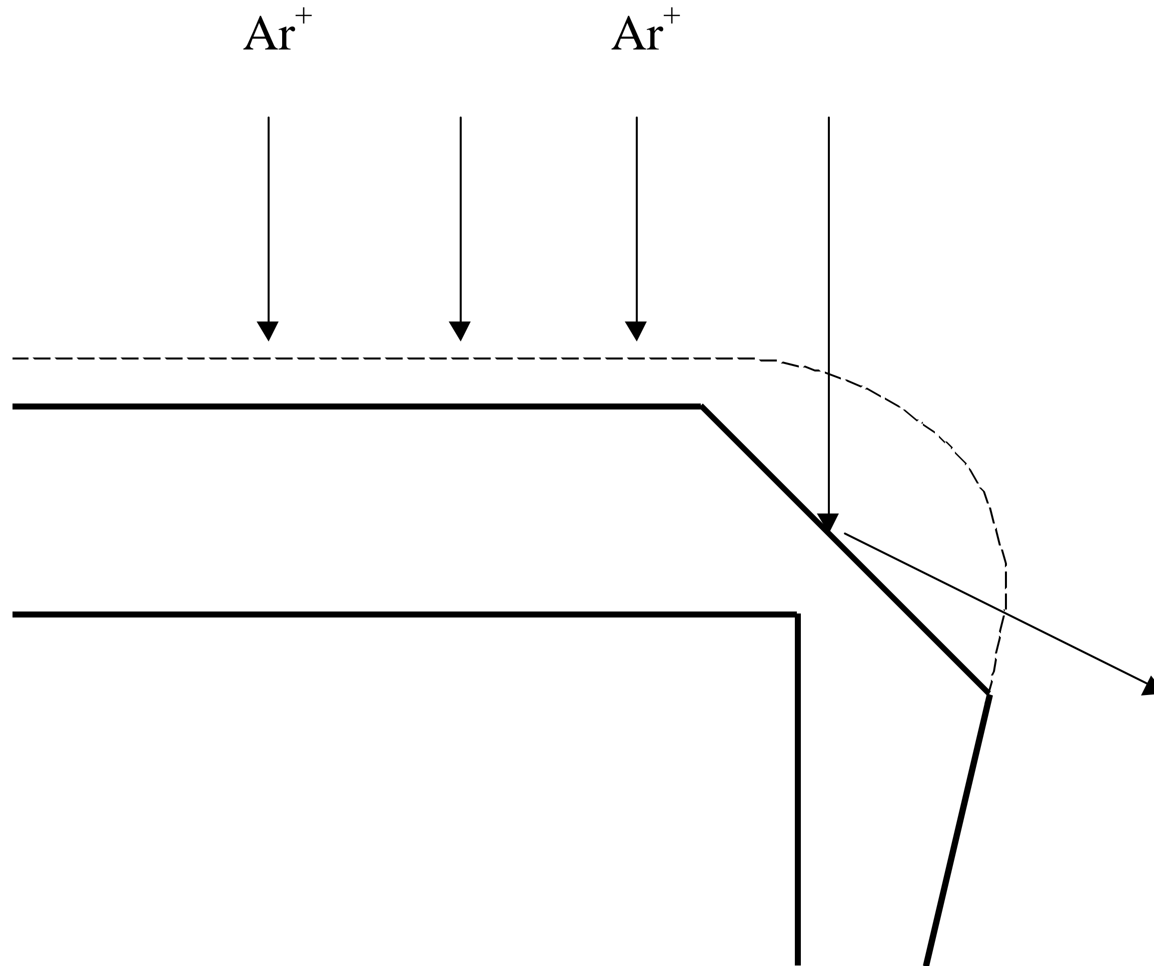
- Gap fill and planarization
- Performed in thin film bay with DCVD
- Cluster tool
- In-situ dep/etch/dep process

In-situ Dep/Etch/Dep Process





Sputtering Corner Chopping



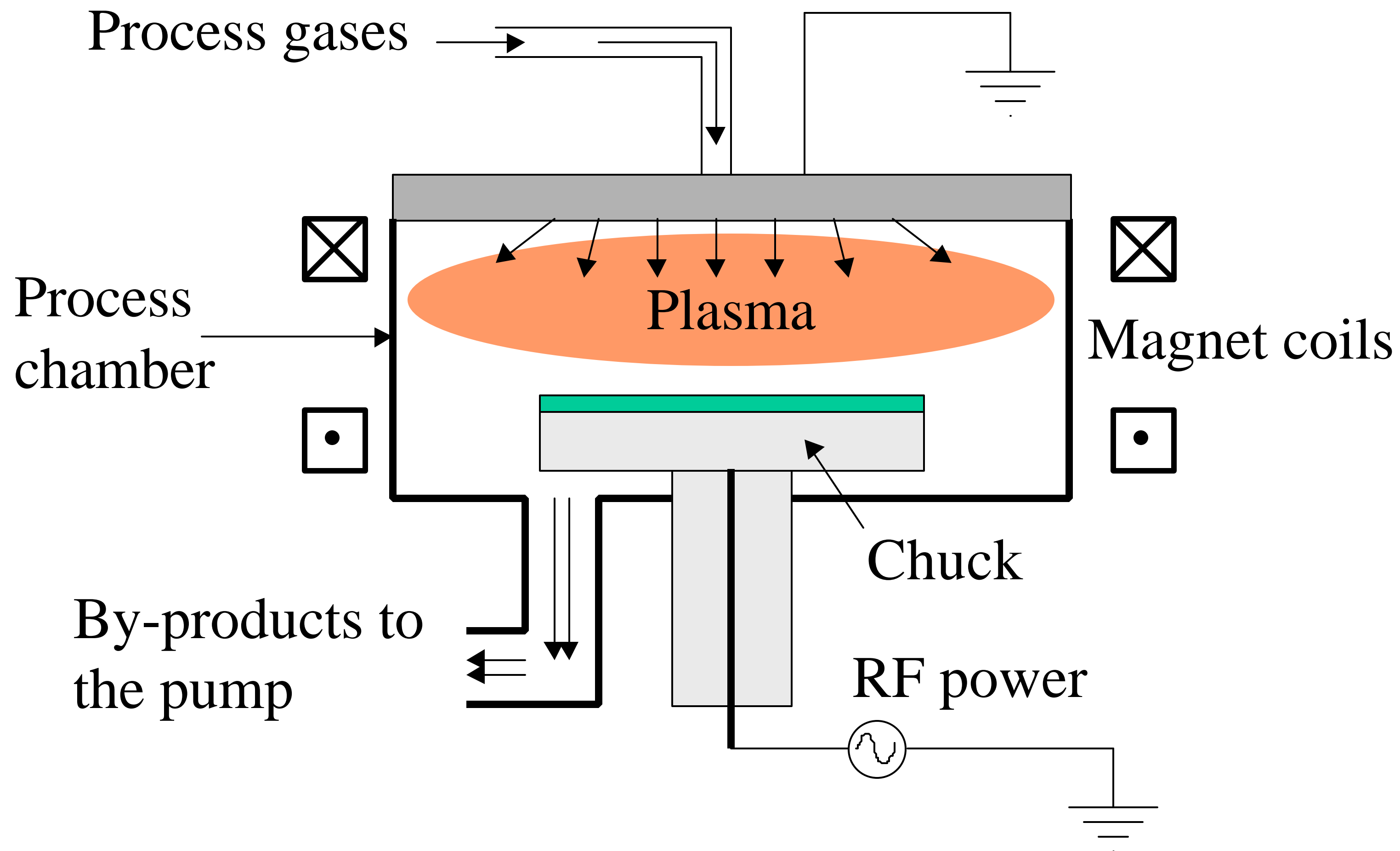
Question

- Why does sputtering etch process usually use argon as the process gas?

Answer

- It is inert, heavy, and relative inexpensive
- The atomic weight of argon is 40, compared with silicon's 28 and helium's 4
- Argon is the third most abundant element in earth atmosphere (~ 1%) only after nitrogen (78%) and oxygen (20%)
- Can be purified directly from condensed air

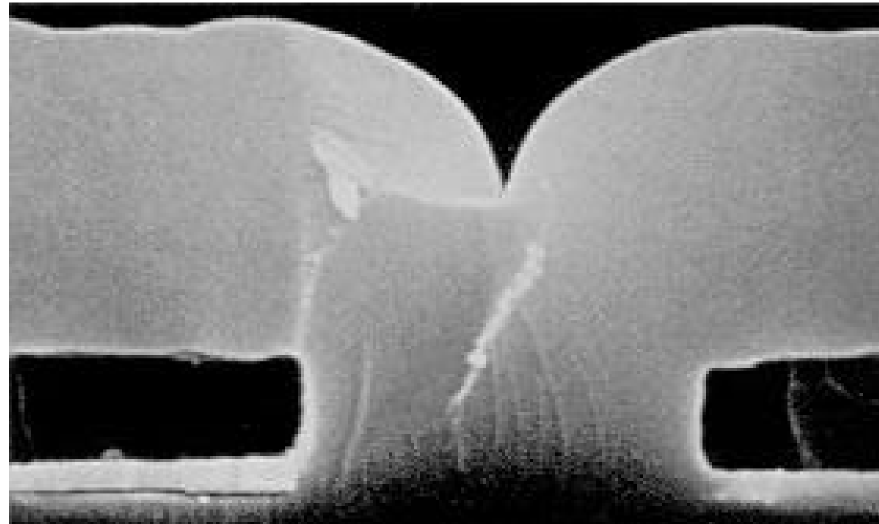
Schematic of Sputtering Etch Chamber



Reactive Etch Back

- CF_4 and O_2
- Heavy bombardment with chemical reaction
- Applications
  - Planarize dielectric surface
  - SOG etch back

Reactive Etch Back Planarization



2 μm PE-TEOS oxide deposition

1 μm planarization etchback

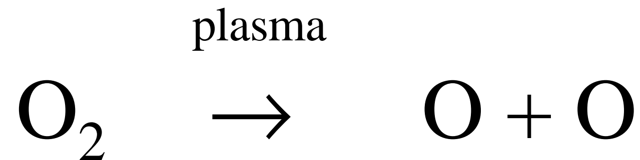
O_3-TEOS Processes

- Ozone is a very unstable molecule,

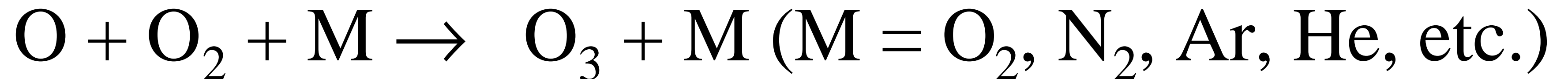
- At 400 °C, half-lifetime of O_3: < 1ms
- Used as carrier of free oxygen radicals
- Ozone reacts with TEOS form silicon oxide
- Excellent conformality and gap fill capability
- Sub-micron IC chip applications
- APCVD and SA-CVD

Ozone Generation

Lighting, corona discharge

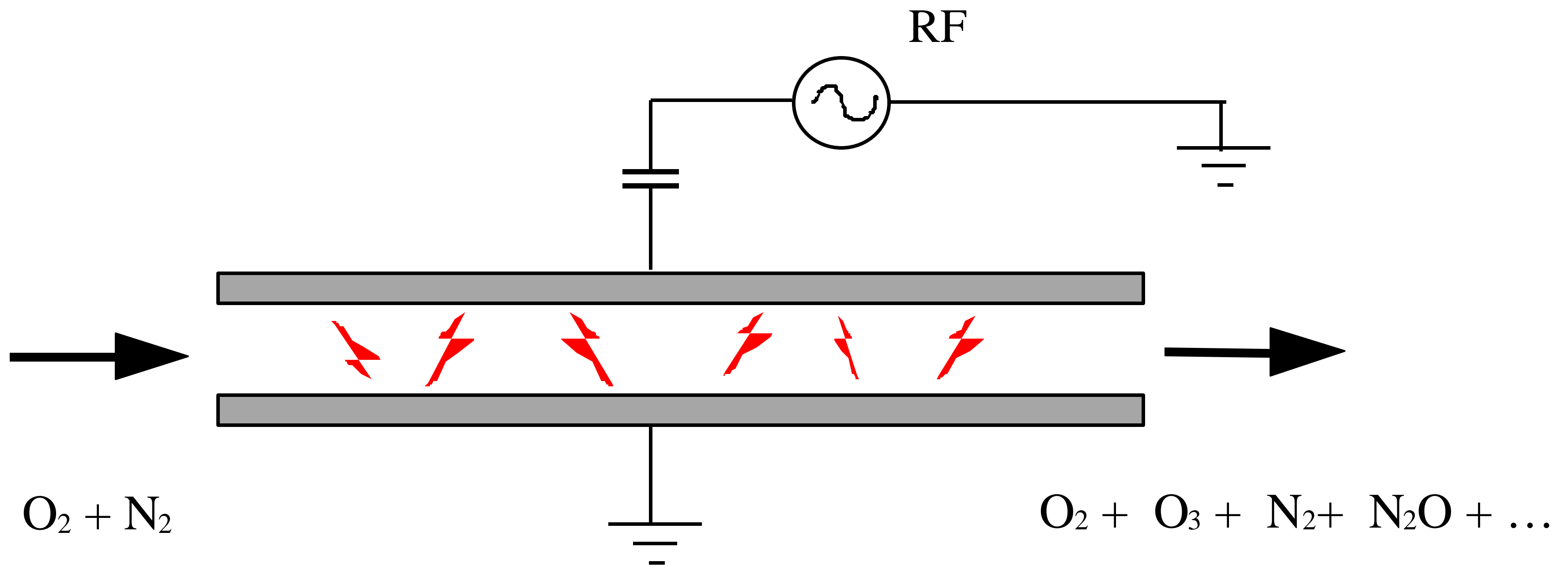


$$O_2 \xrightarrow{\text{plasma}} O + O$$



$$O + O_2 + M \rightarrow O_3 + M \ (M = O_2, N_2, Ar, He, etc.)$$

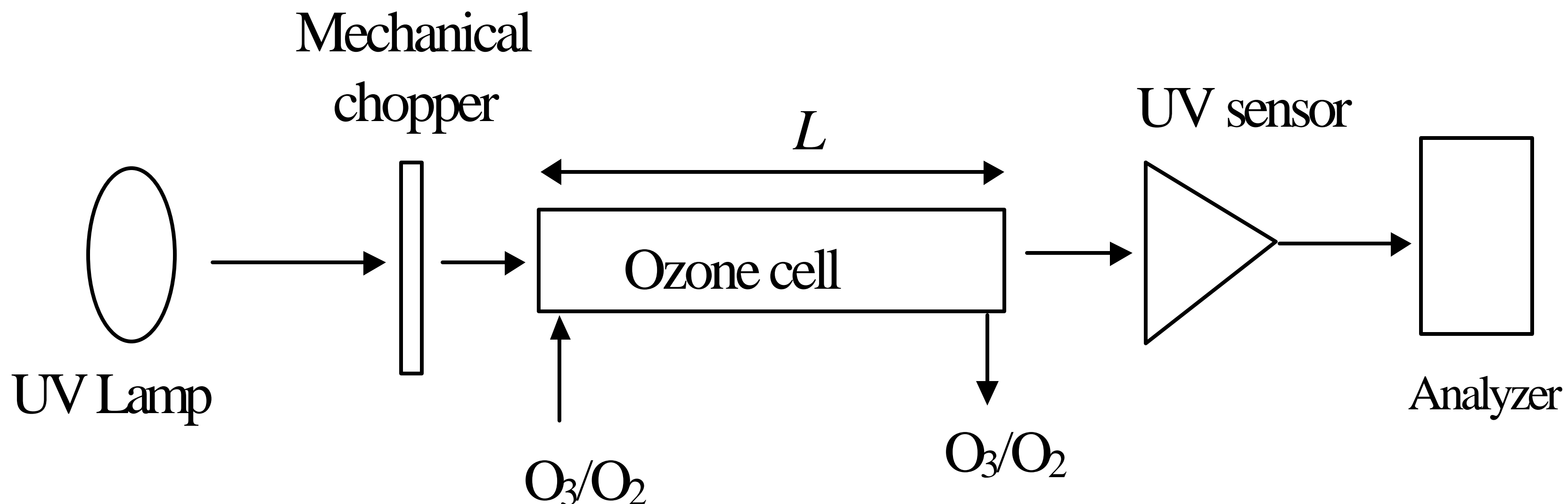
Illustration of Ozonator



Ozone Concentration Monitoring

Monitored by UV absorption (Beer-Lambert law):

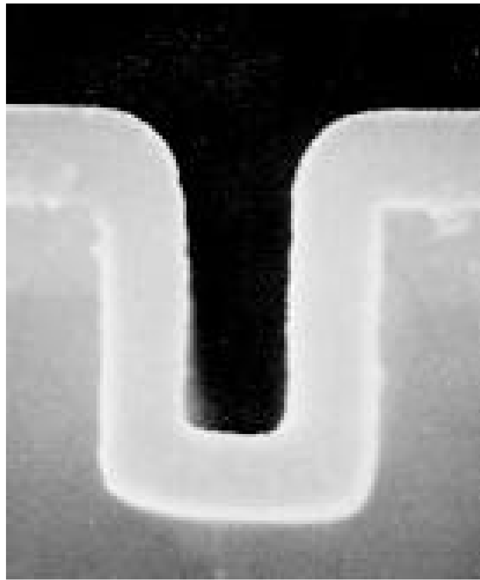
$$I = I_0 \, exp(-XCL)$$



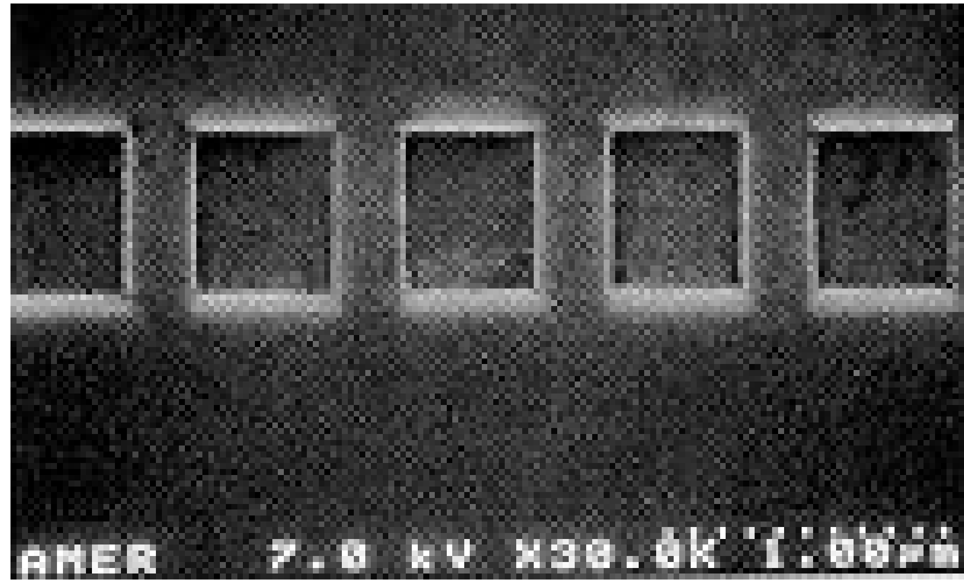
O_3-TEOS USG Process

- $TEOS + O_3 \xrightarrow{heat} SiO_2$ + volatile organics
- Main applications
  - STI (higher temperature, ~ 550 °C)
  - IMD (~ 400 °C)

O_3-TEOS USG

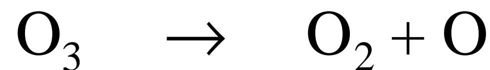


Step coverage

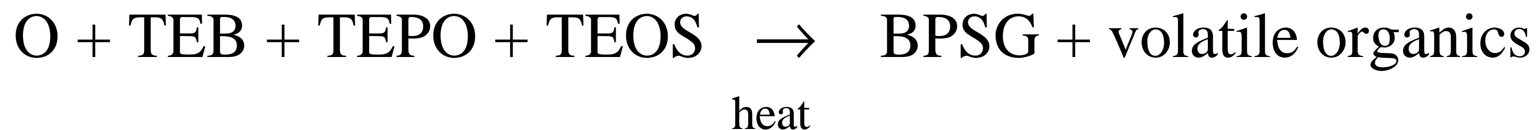


Gap fill

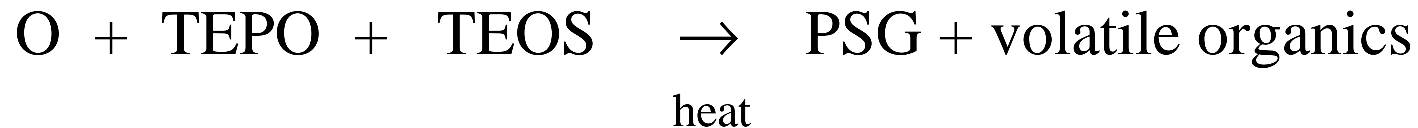
O_3-TEOS BPSG and PSG Process



$$O_3 \rightarrow O_2 + O$$



$$O + TEB + TEPO + TEOS \xrightarrow[heat]{} BPSG + \text{volatile organics}$$



$$O + TEPO + TEOS \xrightarrow[heat]{} PSG + \text{volatile organics}$$

- Main application
  - PMD

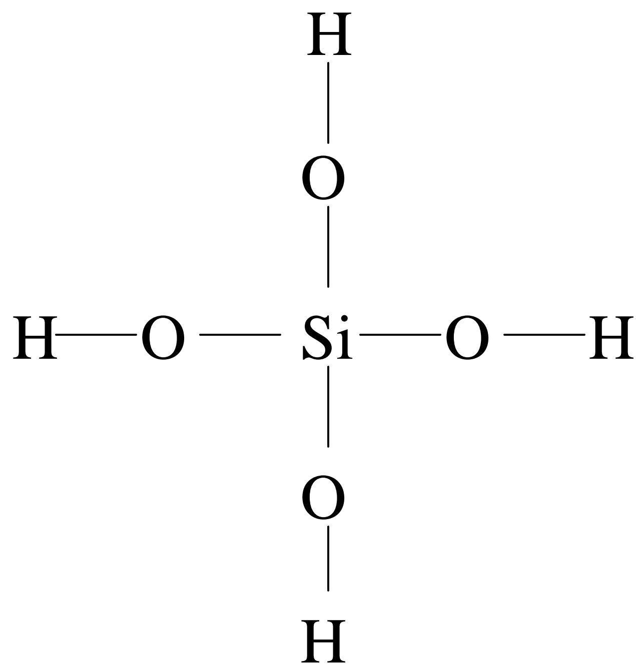
O_3-TEOS BPSG

SACVD BPSG for 0.25 μm gap and 4:1 A/R.

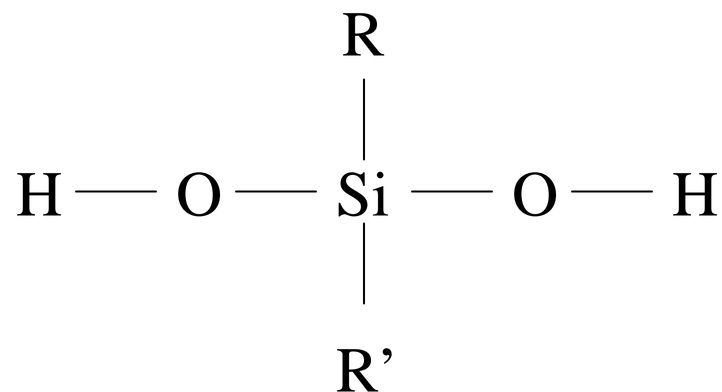
Spin-on Glass (SOG)

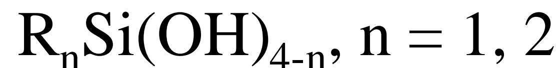
- Similar to PR coating and baking process
- People in fab like familiar technologies
- IMD gap fill and planarization
- Two kinds of spin-on glass:
  - Silicate
  - Siloxane

Spin-on Glass: Silicate and Siloxane



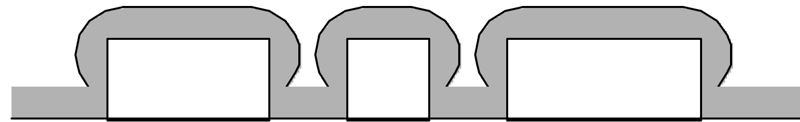
Silicate



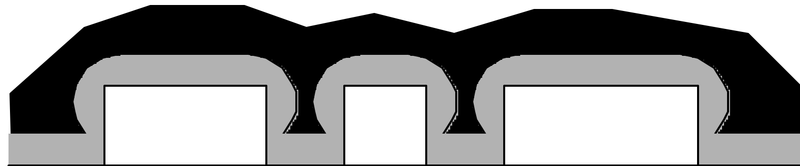


Siloxane

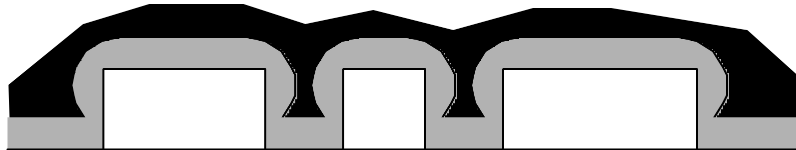
Spin-on Glass Process Steps



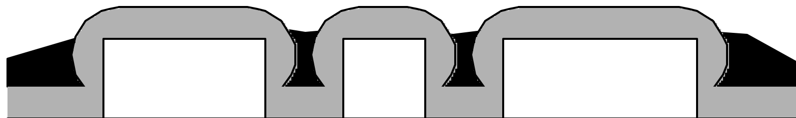
PECVD USG barrier layer



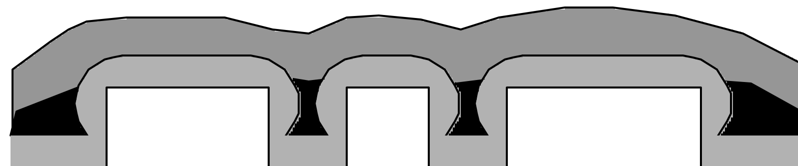
Spin-on glass



SOG cure



SOG etchback



PECVD USG cap

High-Density Plasma CVD

- Dep/etch/dep gap fill needs two chambers
- Narrower gaps may need more dep/etch cycles to fill
- A tool can deposit and sputtering etch simultaneously would be greatly helpful
- The solution: HDP-CVD

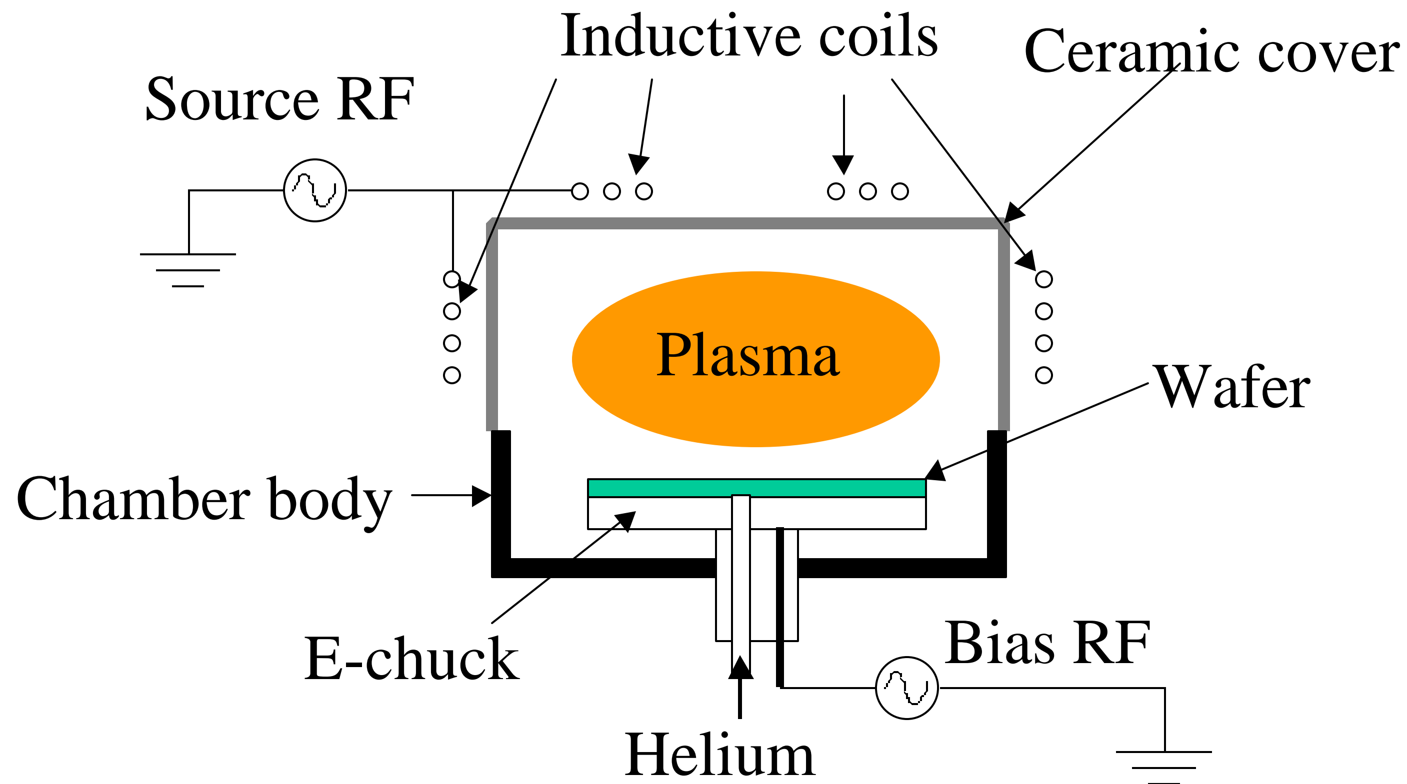
Question

- With the feature size shrinking, metal line width and gap between metal lines becomes smaller. However the metal line height doesn't shrink accordingly, which causes larger gap aspect ratio.
- Why doesn’t shrink metal line height accordingly to keep the same aspect ratio and easier for dielectric gap fill?

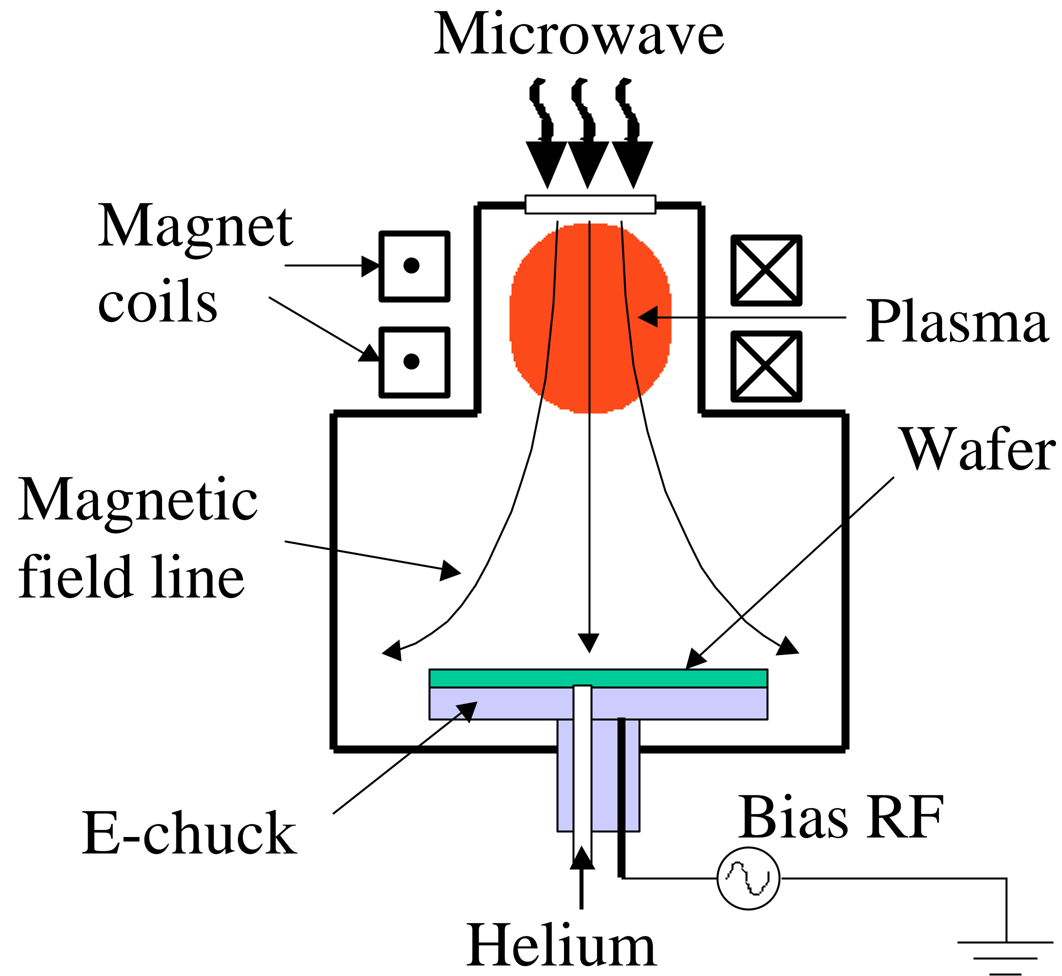
Answer

- Metal line resistance $R = \mathbf{r}\ l/wh$.
- If h also reduces accordingly to l and w, resistance will increase accordingly
- Therefore, line has to keep the same height

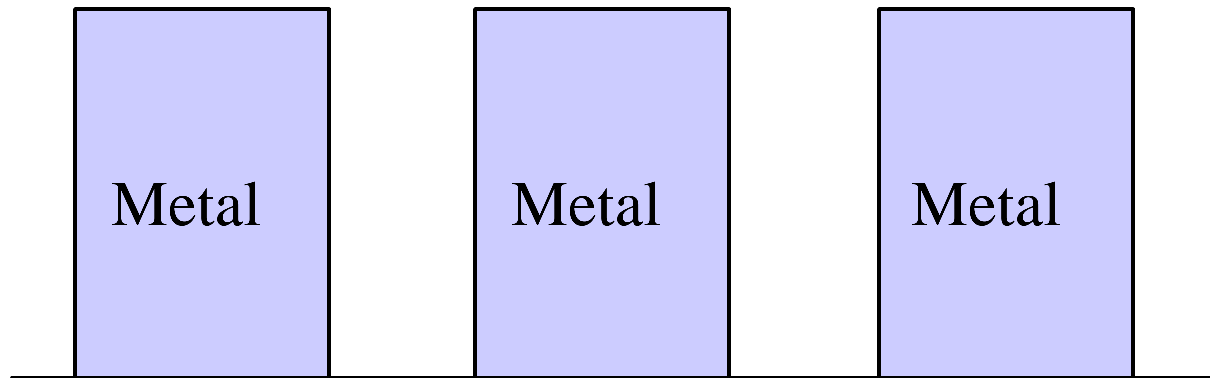
Inductively Coupled Plasma Chamber



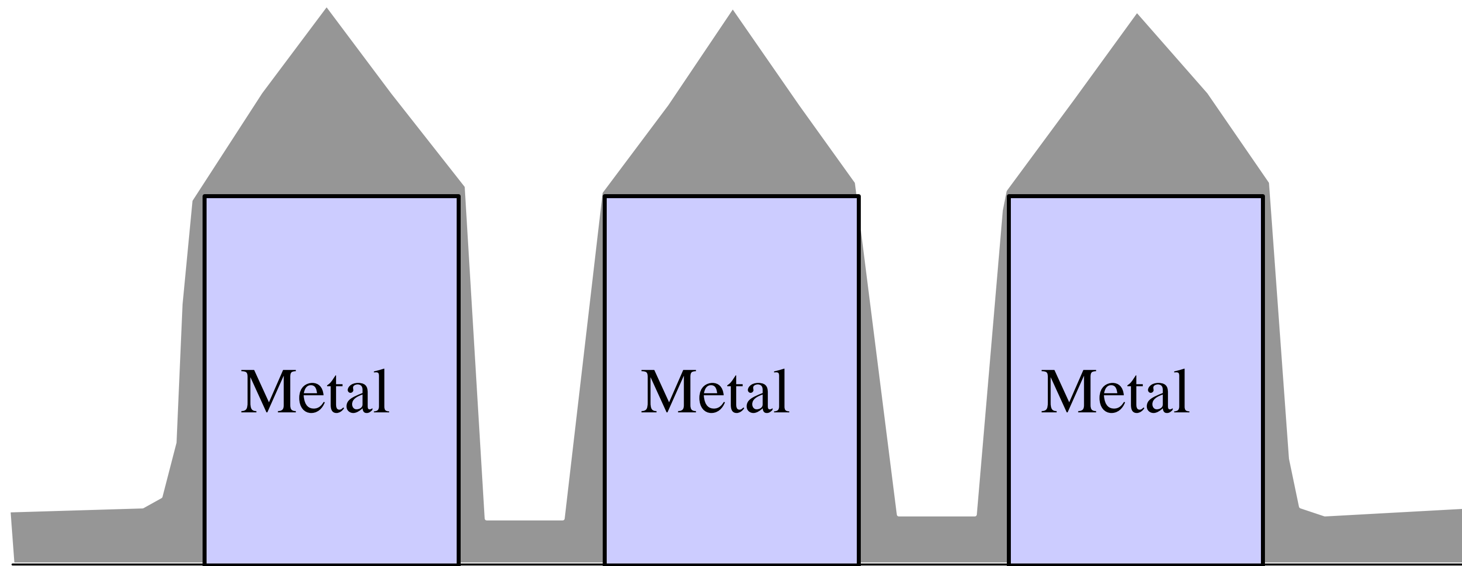
ECR Chamber



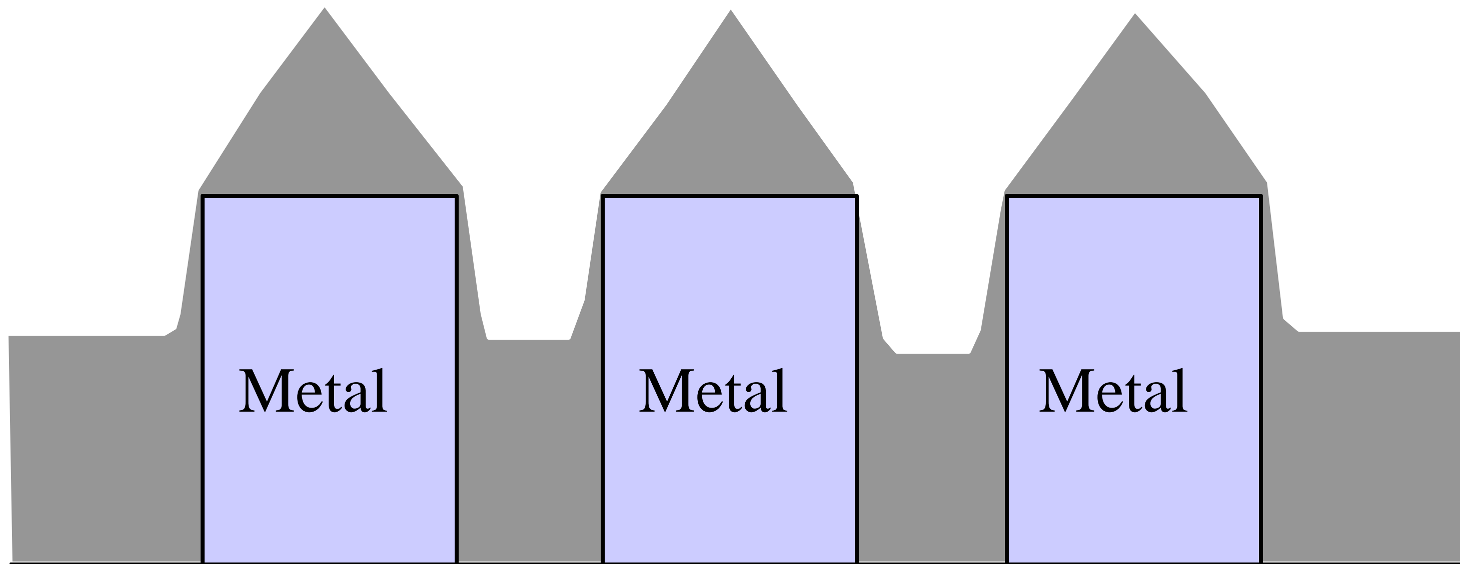
HDP-CVD, IMD Application



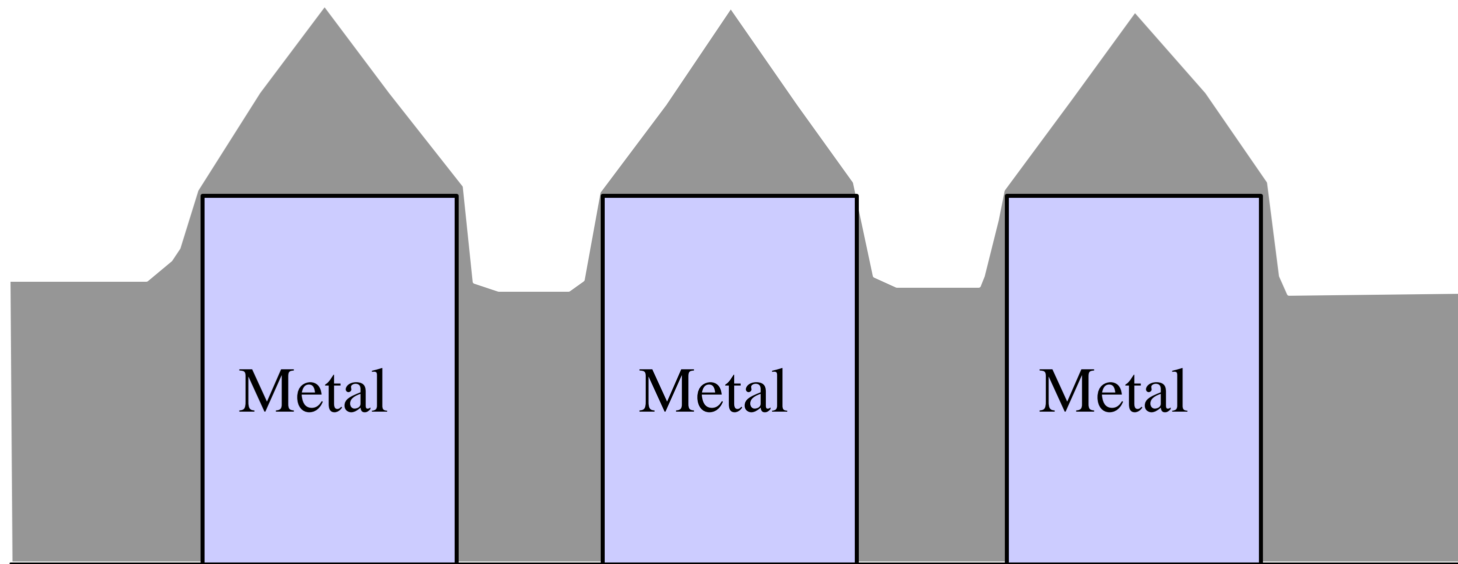
HDP-CVD, Deposition



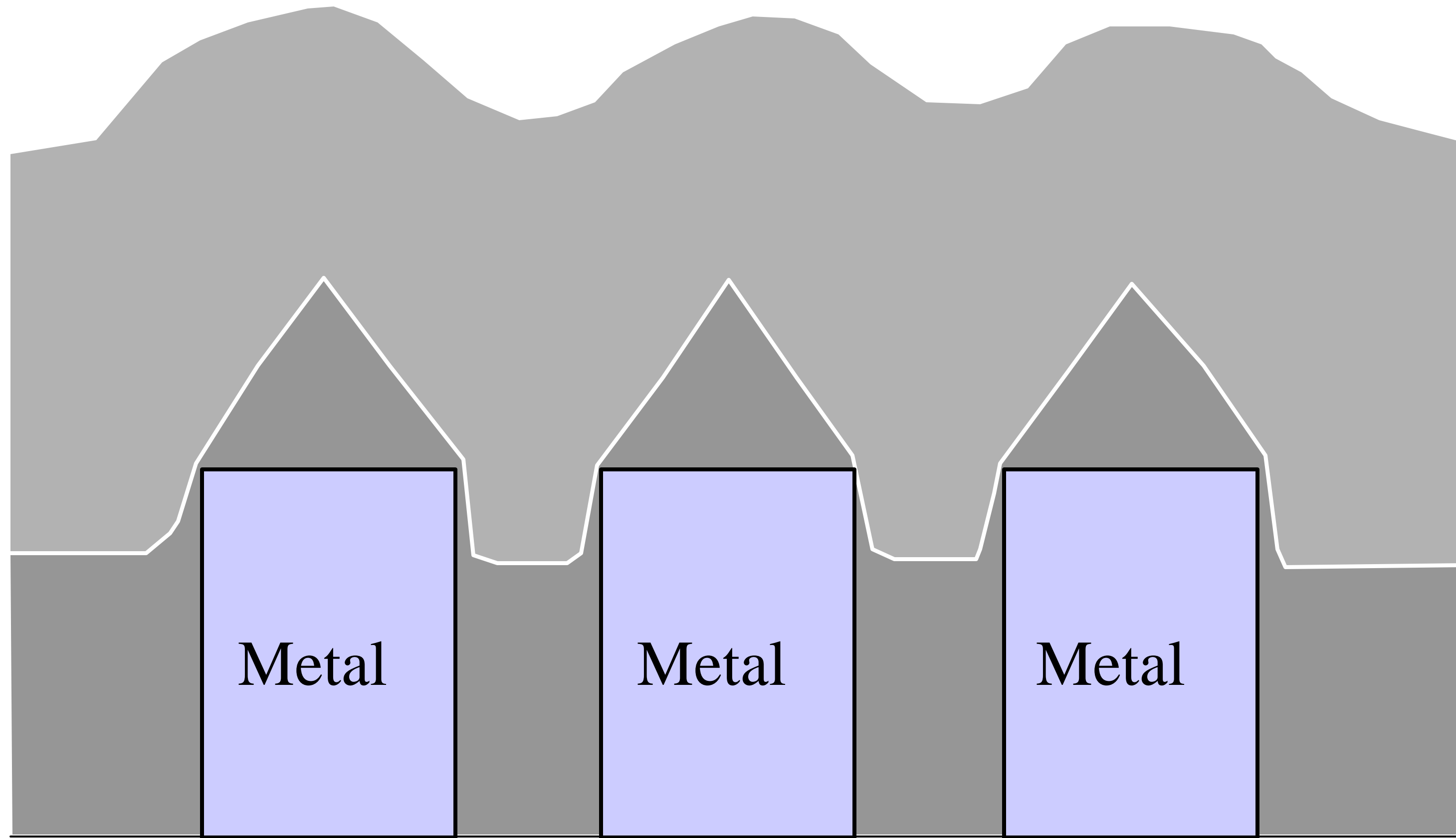
HDP-CVD, Deposition



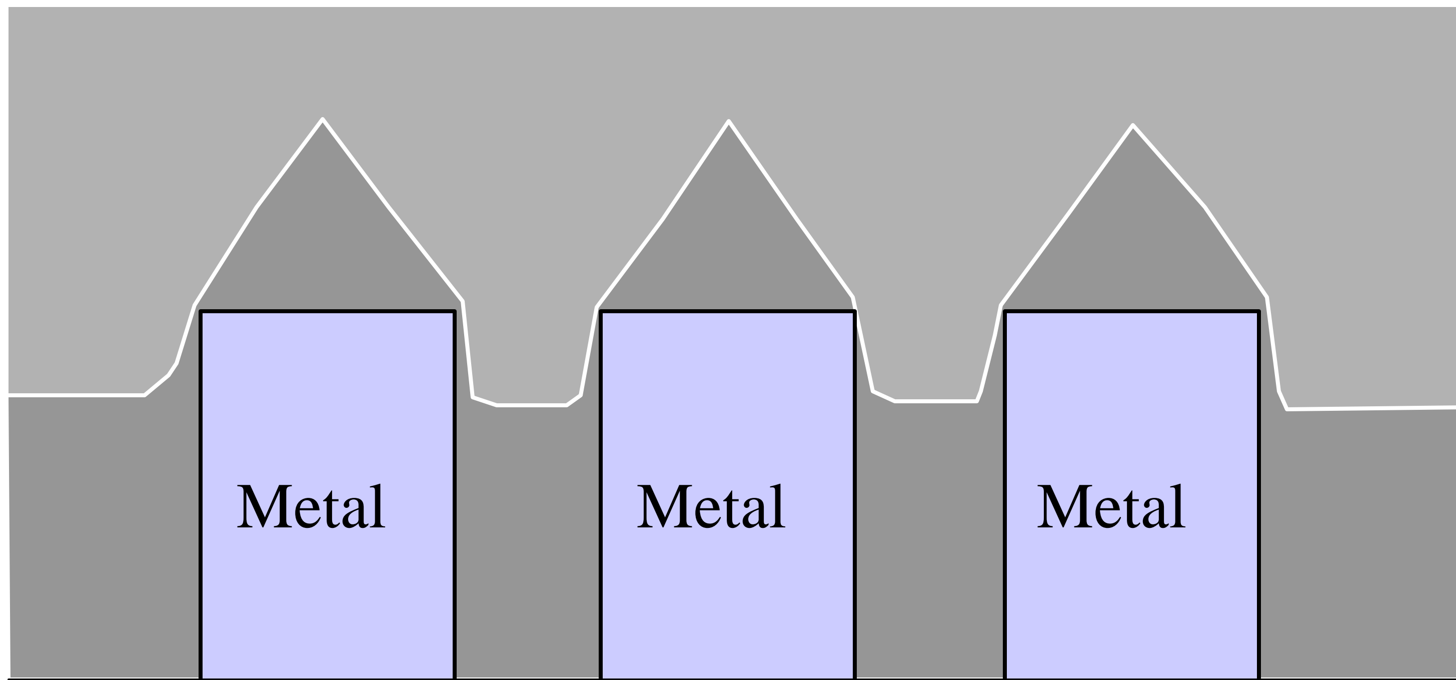
HDP-CVD, Deposition



PE-TEOS Deposition



Oxide CMP



HDP-CVD Processes

- For IMD Applications

- USG $SiH_4 + O_2 + Ar \rightarrow USG + H_2O + Ar + \ldots$

- FSG $SiH_4 + SiF_4 + O_2 + Ar \rightarrow FSG + volatiles$

- For PMD Applications

- PSG $SiH_4 + PH_3 + O_2 + Ar \rightarrow PSG + volatiles$

Question

- Why is silane instead of TEOS used as the silicon source gas for the HDP CVD oxide process?

Answer

- For HDP CVD processes, step coverage is no longer an important factor for the gap fill
- Heavy ion bombardment always keeps gap tapered and deposition is bottom up.
- Using silane can save the costs and hassles related with vapor delivery system of the liquid TEOS source.

Dielectric CVD Chamber Clean

- During dielectric CVD process, dielectric thin film will be deposited on everything inside chamber
- Need to routinely clean the chamber to prevent particulate contamination problems.
- For DCVD, more time for clean than dep.
- RF plasma clean and remote plasma clean

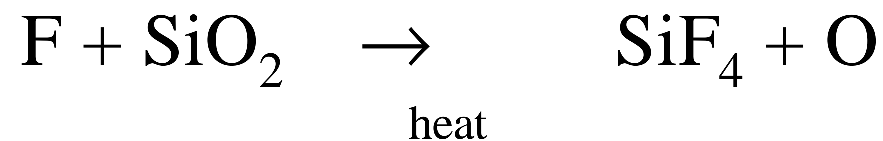
RF Plasma Clean

- Plasma clean process remove dielectric film on the process kits and chamber wall
- Fluorocarbon such as CF_4, C_2F_6 and C_3F_8
- In some case NF_3 is also used
- In plasma, fluorocarbon will be dissociated
- Free fluorine, F, will be generated
- F removes silicon oxide and silicon nitride

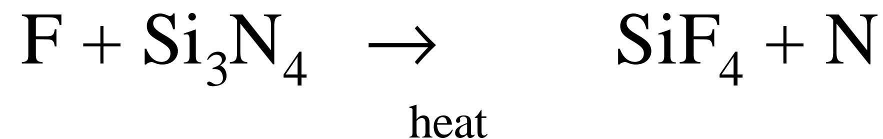
RF Clean Chemistry

plasma

plasma



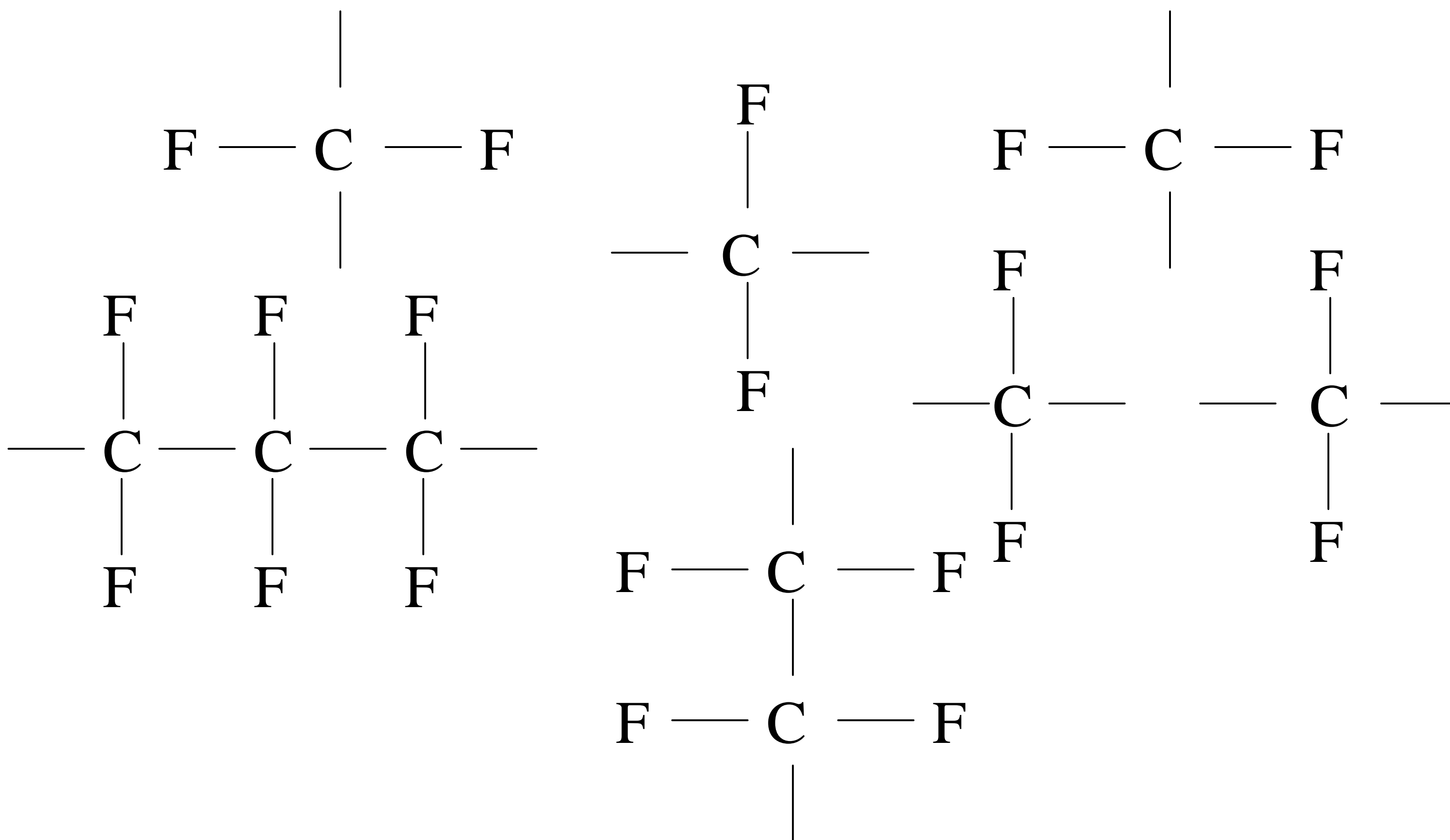
plasma



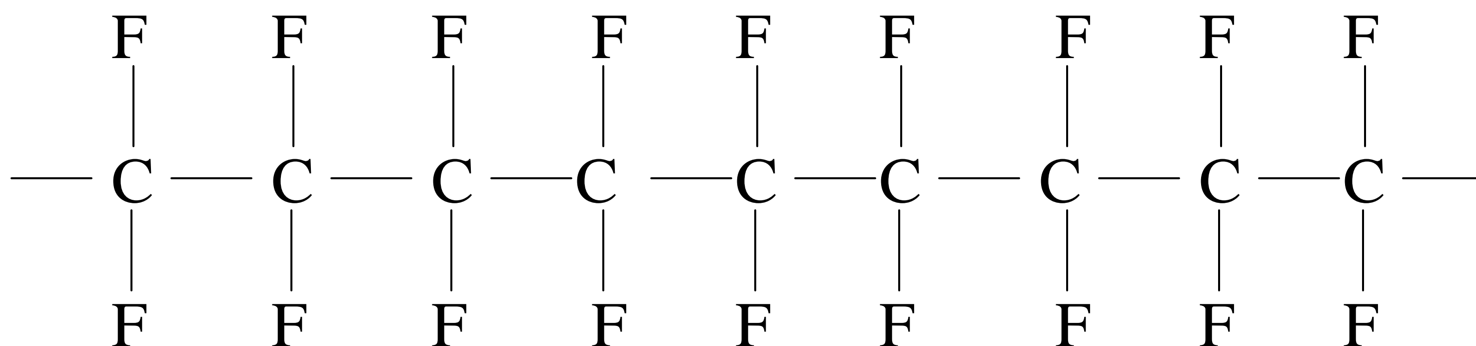
RF Clean Chemistry

- In plasma clean processes, oxygen source gases such as N_2O and O_2 are used with fluorocarbon to react with carbon and free more fluorine radicals
- Increase F/C ratio, keep it > 2
- Prevent carbon fluoride polymerization, and increases the clean efficiency

CF_2 and Reconnection



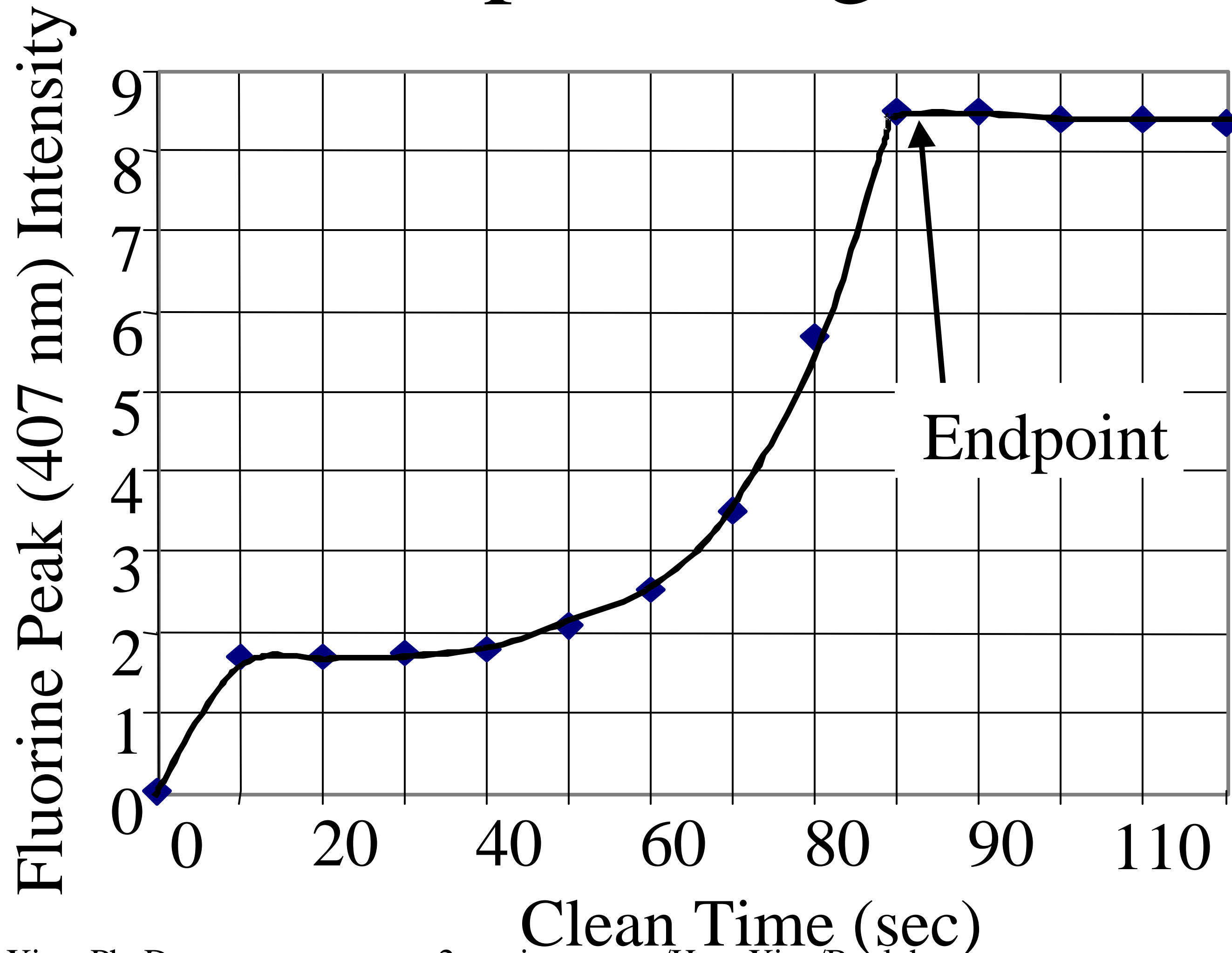
Polymerization, Teflon Deposition



RF Clean Endpoint

- Excitation-relaxation cause glow
- Different gases have different colors of light
- Information of chemical components in plasma
- Monitor line emission to control clean process

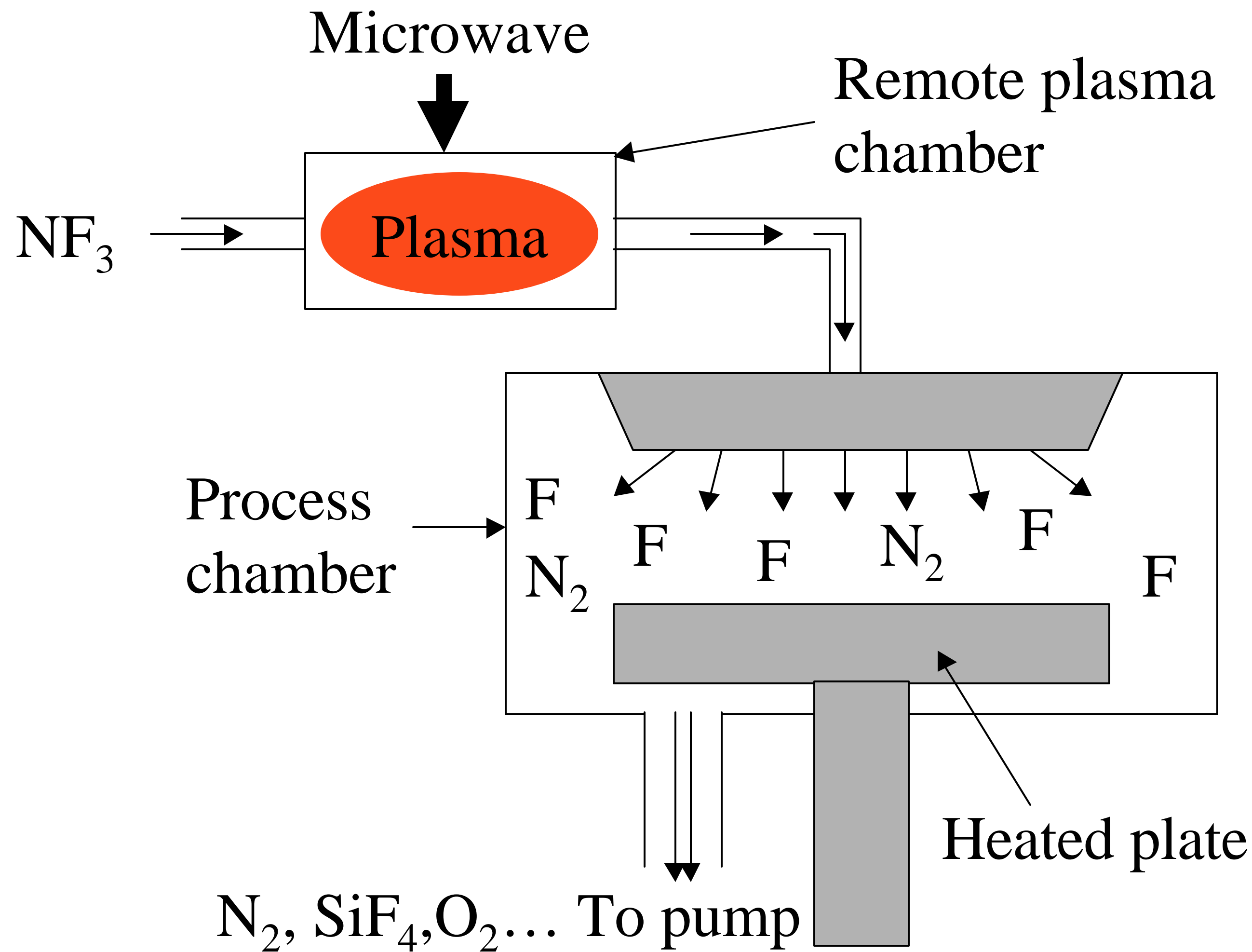
Endpoint Signal



Remote Plasma Clean

- RF Plasma clean
  - Ion bombardment
  - Cause damage on chamber parts
- Remote plasma clean
  - No ion bombardment
  - More gentle on chamber parts
  - Longer part lifetime
  - Less “green house” gas emission

Illustration of Remote Plasma Clean



Remote Plasma Clean

- Microwave (MW) power, NF_3 as fluorine source
- 99% of NF_3 dissociated in MW plasma
- Free fluorine reacts with the film in chamber
  - No plasma inside process chamber
  - No ion bombardment
  - Prolongs their lifetime
- Disadvantages:
  - Less maturity, higher cost, and using NF_3
  - Can not use optical endpoint system, may need FTIR system to achieve the automatic process endpoint.

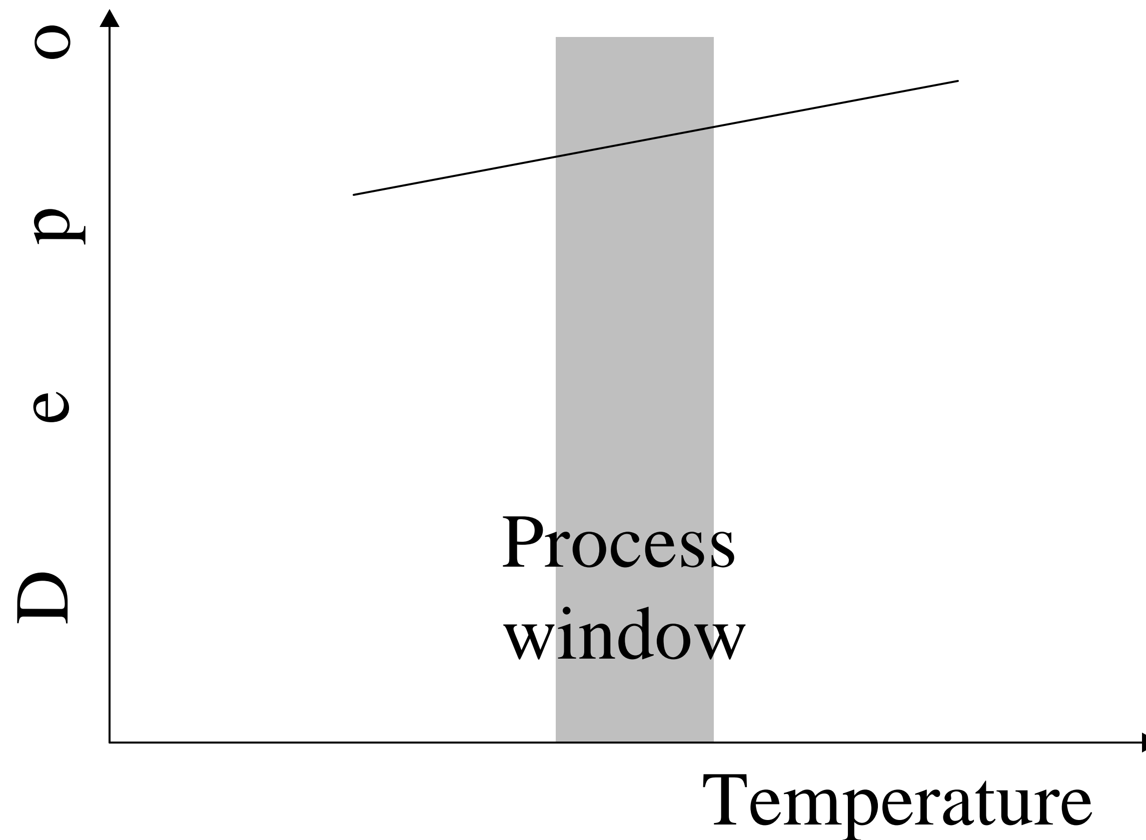
Process Trends and Troubleshooting

- Process response to input parameters change
- Help to determine the root cause if some wrong

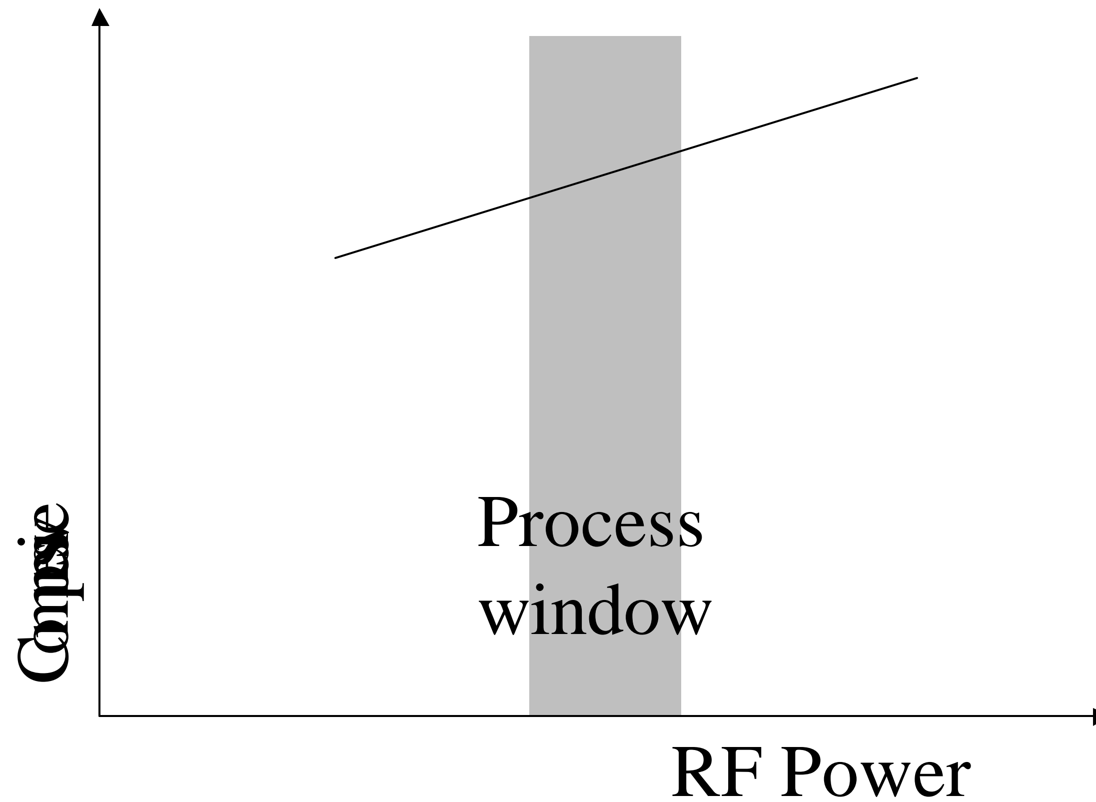
Silane PECVD Process Trends

- Increasing temperature increases deposition rate
  - Higher diffusion rate of precursors in boundary layer
- Increasing temperature improves deposited step coverage and film quality
- PMD uses a higher temperature
- IMD and PD, normally not exceed 400 ºC

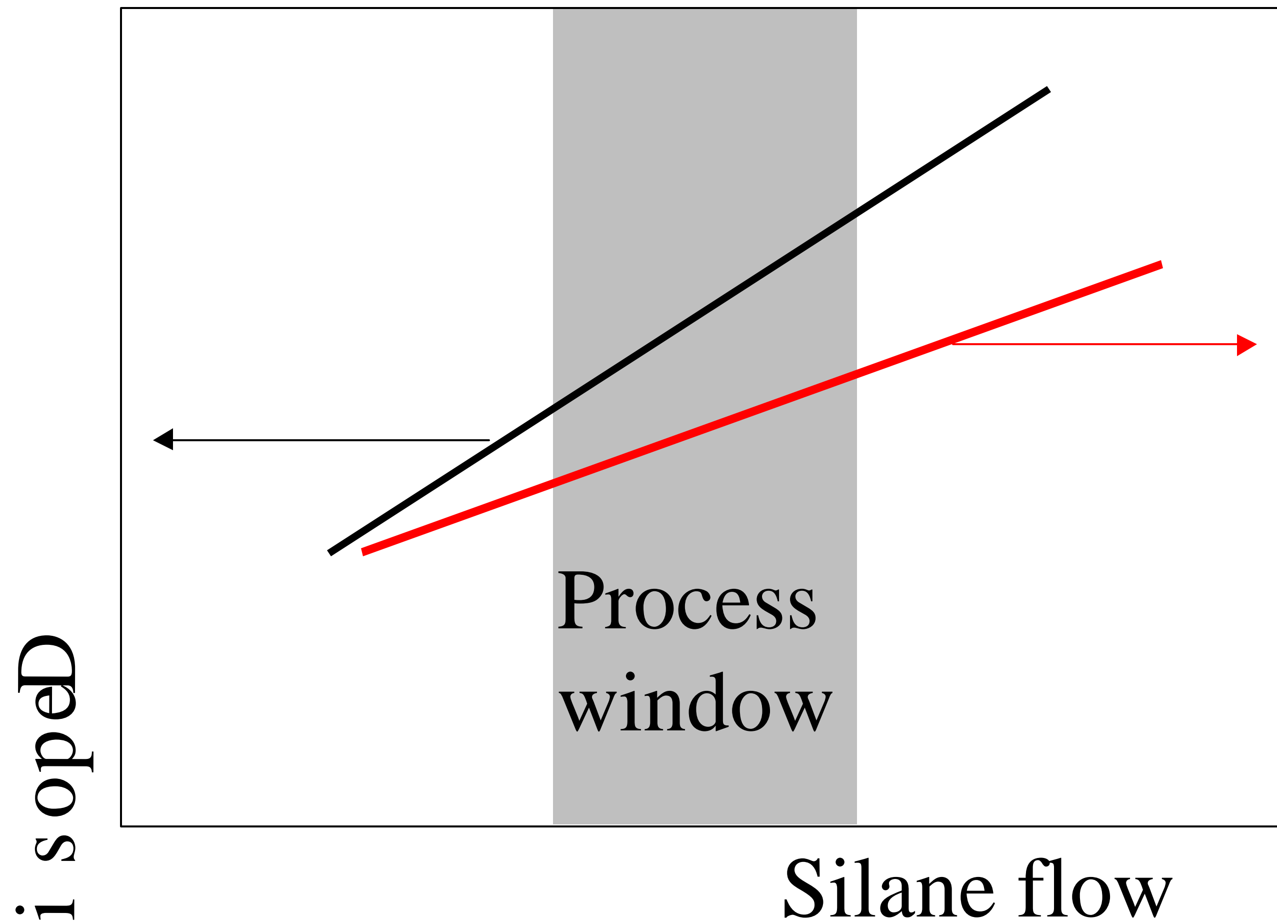
Deposition Rate and Temperature



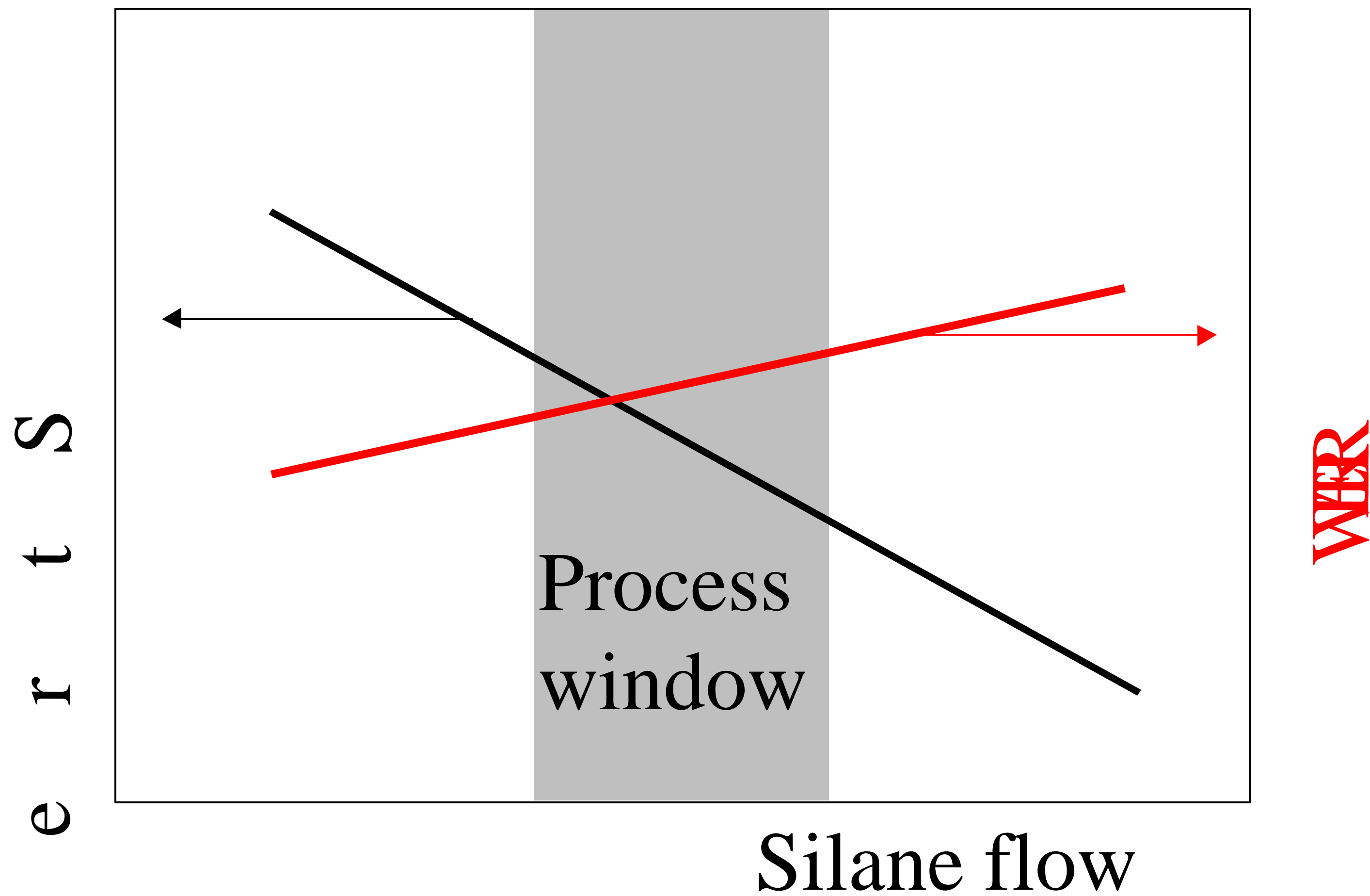
Stress and RF Power



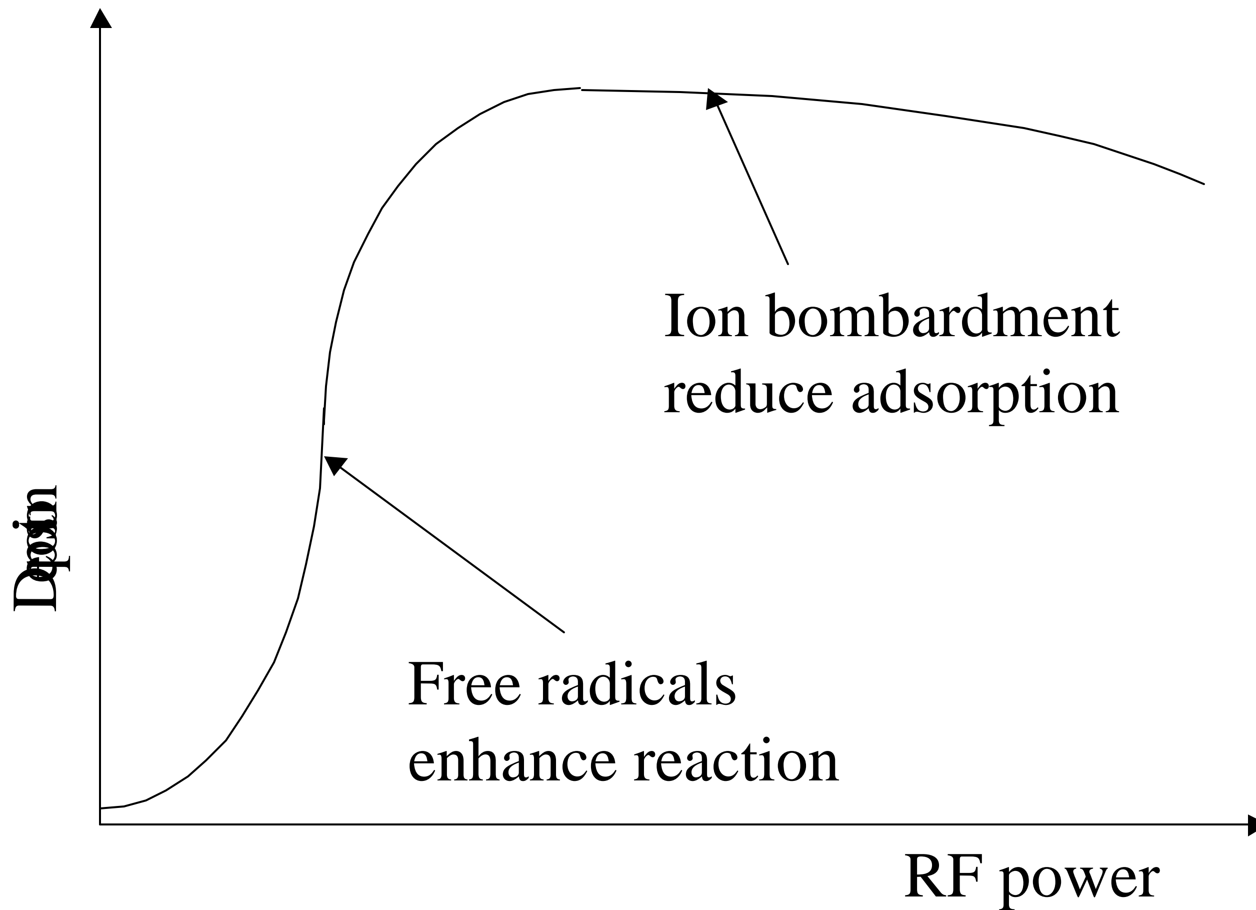
Silane PECVD Process Trends



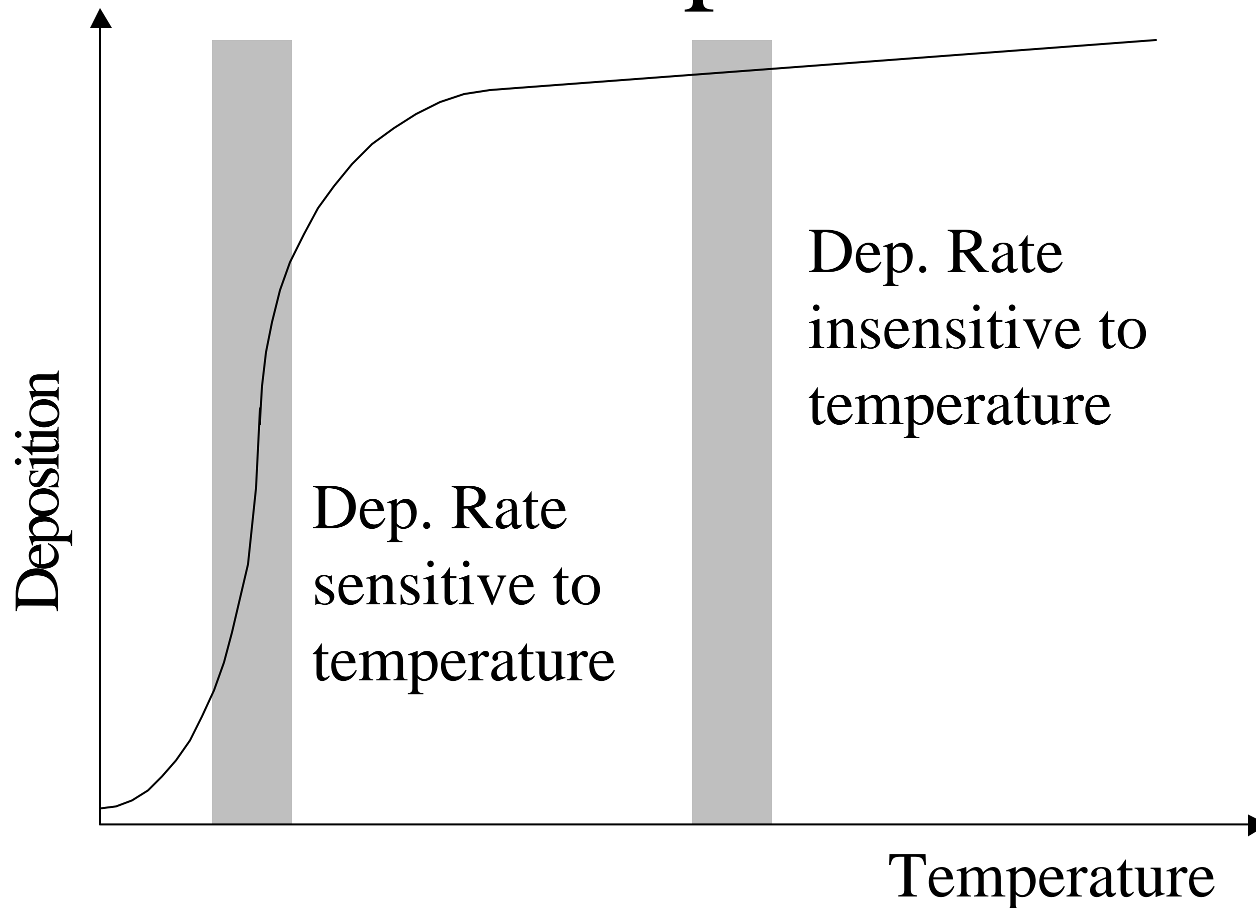
Silane PECVD Process Trends



Relationship of Deposition Rate and RF Power



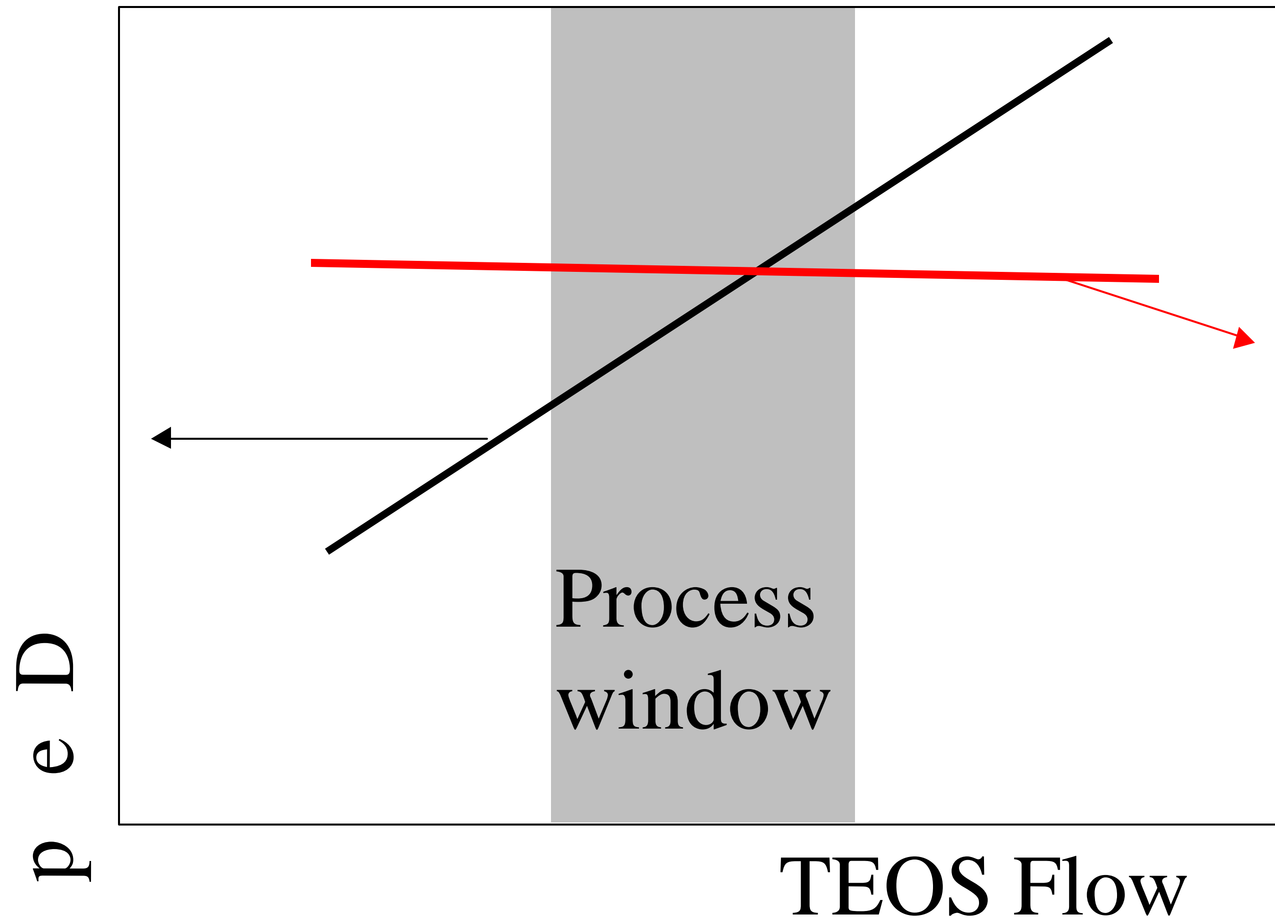
Relationship of Deposition Rate and Temperature



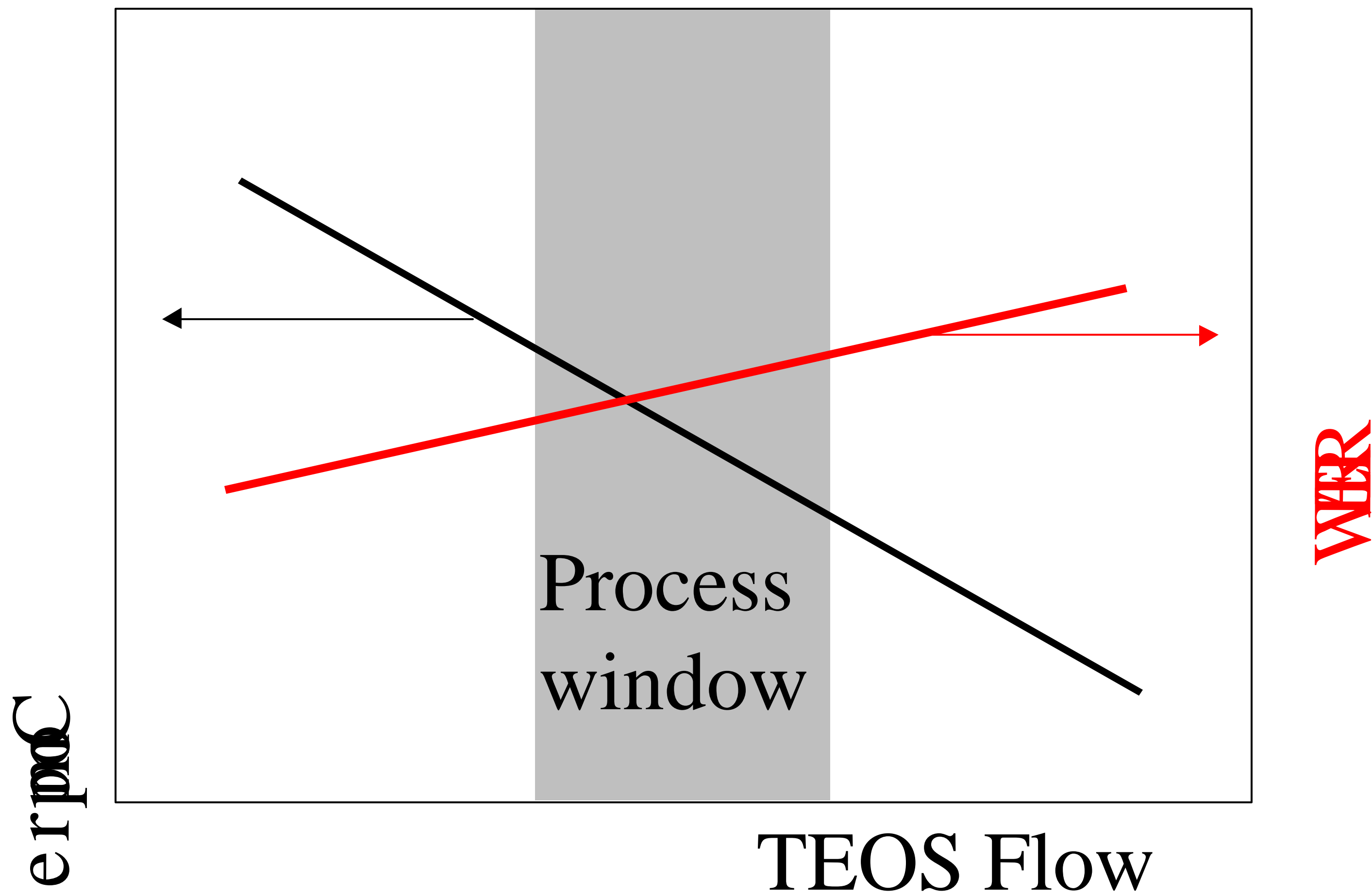
PE-TEOS Trends

- RF power↑: dep rate↑↓, compressive stress↑
  - In process window, dep rate go down
- Temperature↑: dep rate↑↓
  - In process window, dep rare go down
- TEOS flow↑: dep rate↑, compressive stress↓

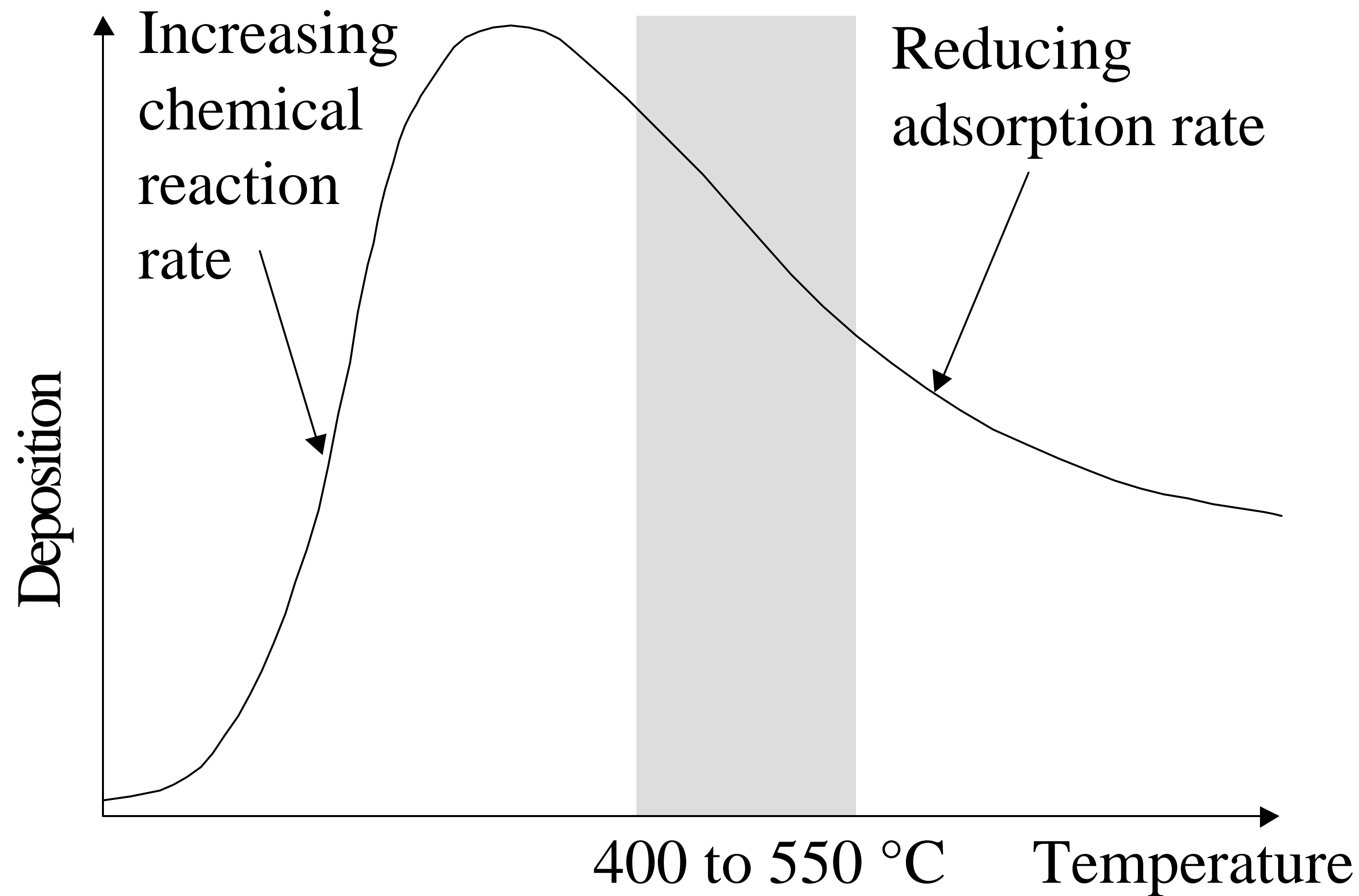
PE-TEOS Trends: TEOS Flow Rate



PE-TEOS Trends: TEOS Flow Rate



PE-TEOS Trends: Temperature



O_3-TEOS Trends

- Temperature↑: dep rate↑↓
  - In process window, dep rare go down
- TEOS flow↑: dep rate↑

Question

- For both PE- and O_3- TEOS processes, the maximum deposition rate can be achieved at about 250 ºC. Why do the IMD TEOS processes normally operate about 400 ºC and PMD and STI processes deposited even higher temperature (~ 550 ºC)?

Answer

- At higher deposition temperature, film quality is higher and step coverage is better

Troubleshooting

- Learned from hand-on experience
- Sudden process change, either suddenly goes wrong, or gradually goes wrong and suddenly comes back,
- Someone should check what has changed between good process and the bad process, or vice versa.

Troubleshooting

- Check metrology tool first and make sure the right recipe is used.
- If one measure PE-TEOS film with nitride recipe, measured thickness would be significantly thinner
- If nothing is wrong with metrology tool, then check whether the process recipe has been changed.

Troubleshooting

- Process always has problems at end of shift
- Someone should work cross shifts to find out what had been changed during shift change
- Something must be changed that put the process back to normal at the beginning of the next shift
- It most likely is the source of problems as the process gradually goes wrong at end of the shift

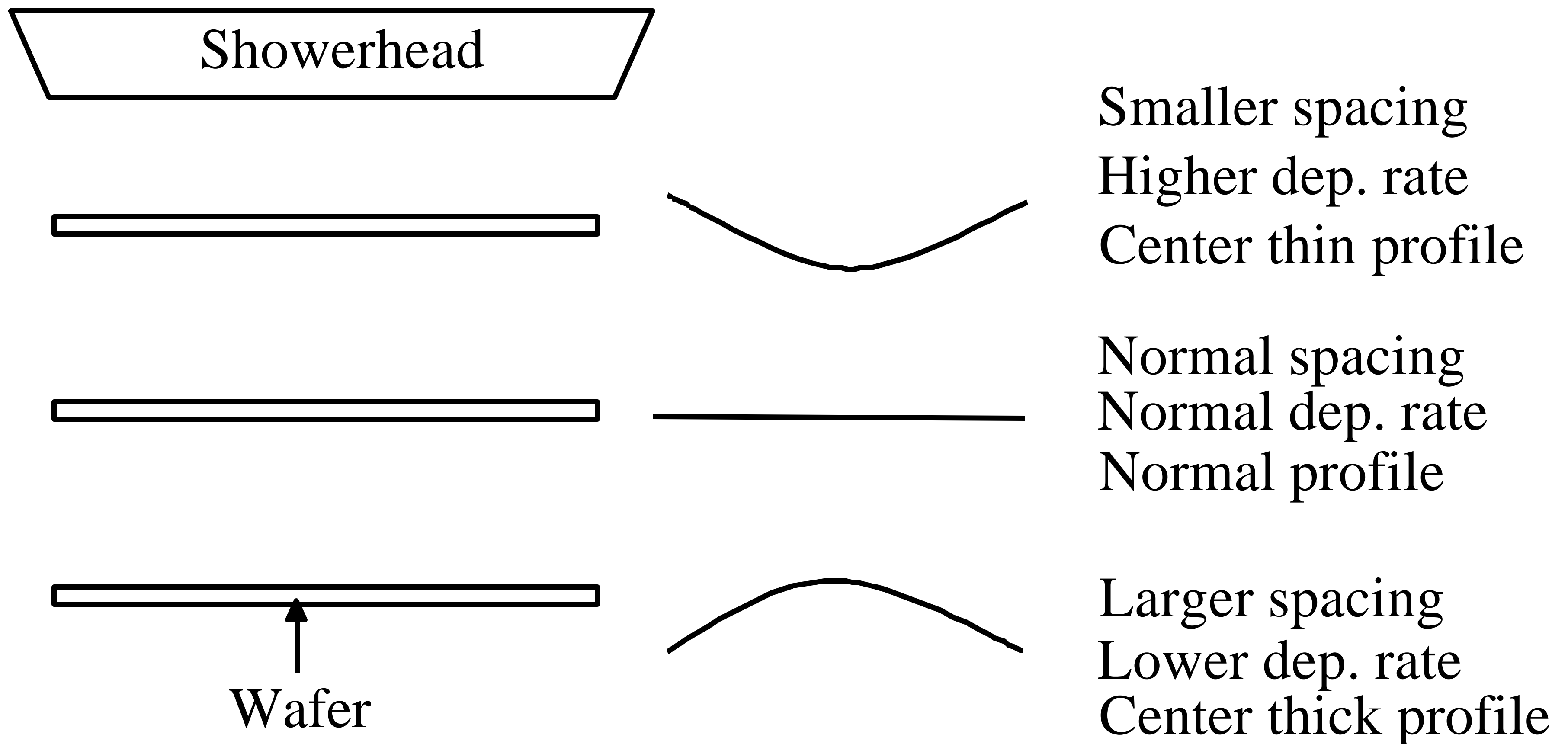
Troubleshooting

- Most dielectric CVD processes operate in mass-transport-limited regime
- Deposition rate is mainly determined by gas flow rate, usually silane and TEOS flow rate
- Very likely that deposition rate problems are related with silane or TEOS flow rate
- Mass flow controller and liquid flow controller

Troubleshooting: Non-uniformity

- Uniformity is determined by flow pattern
- If non-uniformity pattern is center symmetric
  - Adjusted spacing of the wafer and showerhead
  - Or changing the carrier gas flow rate
    - Helium flow for TEOS processes
    - Nitrogen flow for nitride process

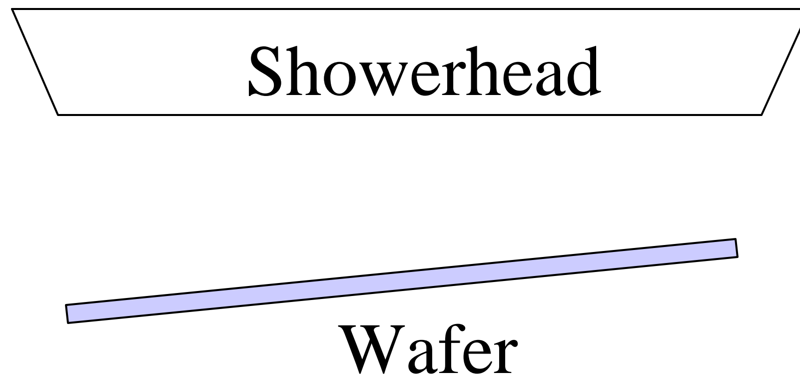
Spacing and Film Profile

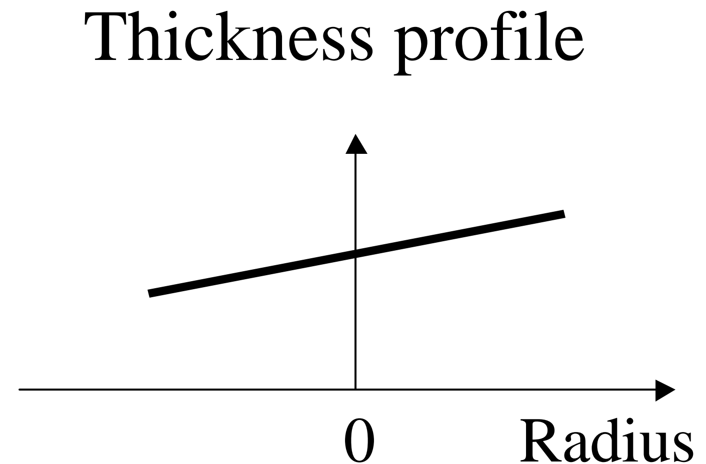


Troubleshooting: Non-uniformity

- If the non-uniformity is side-to-side
- Check wafer leveling or centering
- Leak check of slip valve of the chamber

Leveling and Side-to-side Profile





Future Trends

- HDP-CVD USG for STI
- Nitride or O_3-TEOS oxide for sidewall spacer
- PECVD or RPCVD for PMD barrier nitride
- HDP-CVD PSG for PMD
- CMP for planarization
- Low-κ dielectric for IMD
- Silicon oxide/nitride as passivation dielectric

Future Trends

- High-κ gate dielectric
- Possible candidates: TiO_2, Ta_2O_5, and HfO_2
- CVD and RTA

Future Trends: Low-κ Dielectrics

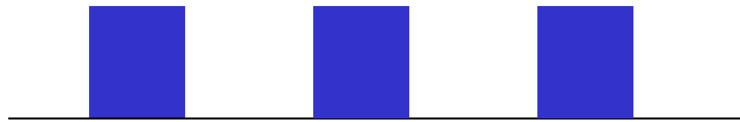
- Need to reduce *RC* time delay
  - low-κ reduces *C* and copper reduces *R*
- Require high thermal stability, high thermal conductivity, and process integration capability
  - CVD
    - CSG (C_xSi_yO, κ ~ 2.5 - 3.0) and α-CF (C_xF_y, κ ~ 2.5 – 2.7)
  - Spin-on dielectrics (SOD)
    - Hydrogen silsequioxane (HSQ, κ ~ 3.0),
    - Porous SOD such as xerogels (κ ~ 2.0 - 2.5)

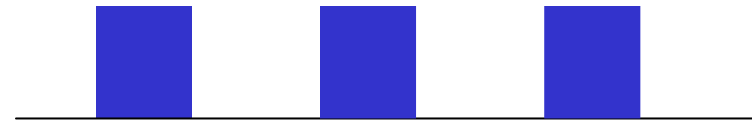
Future Trends: Low-κ Dielectrics

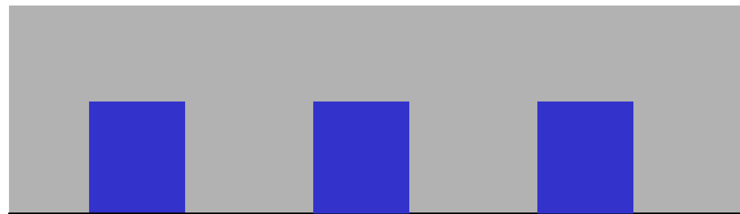
- Damascene process
- Copper metallization

- No gap fill, no planarization problem
- Main challenge: Integrate low-κ with copper metallization

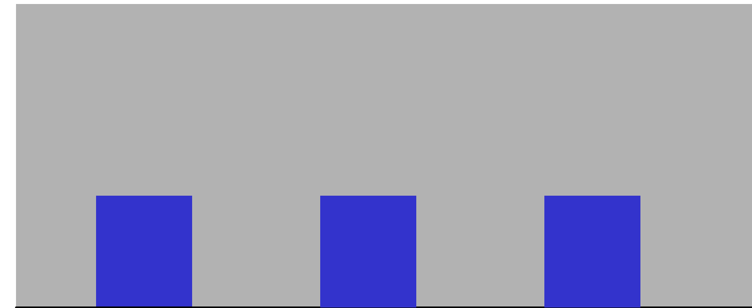
Interconnection Processes



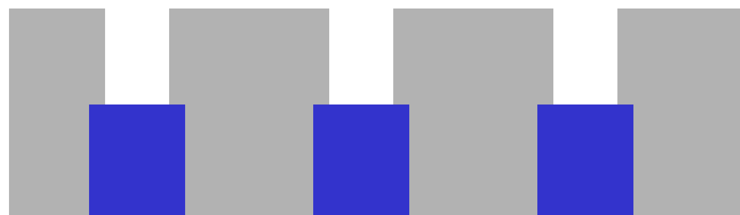




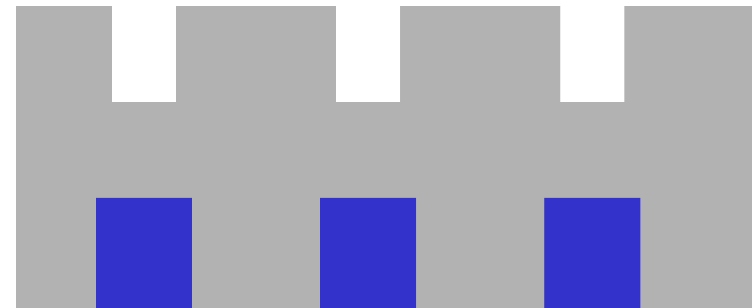
Dielectric deposition/planarization



Dielectric deposition/planarization

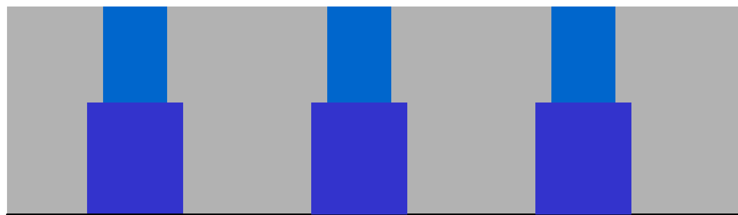


Via etch

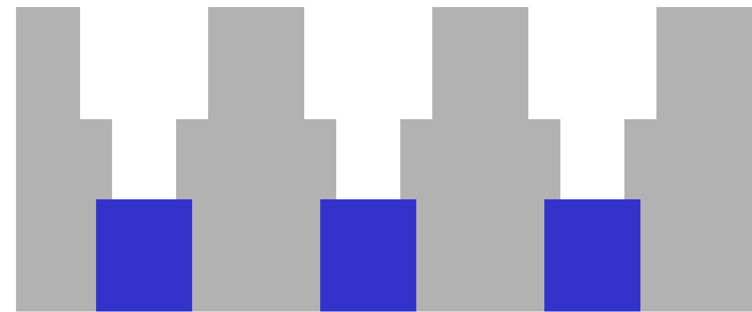


Via etch

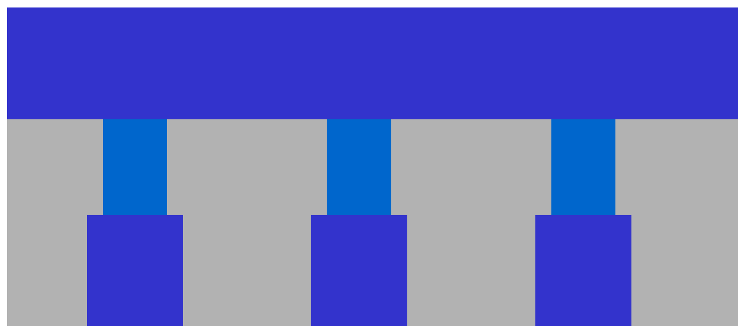
Interconnection Processes



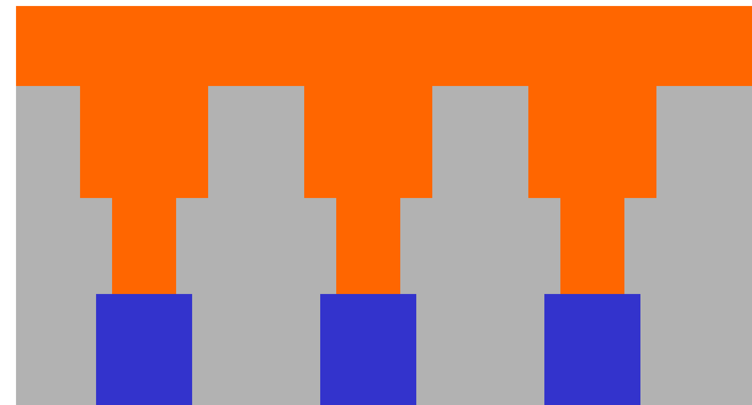
Via fill and polish



Trench etch

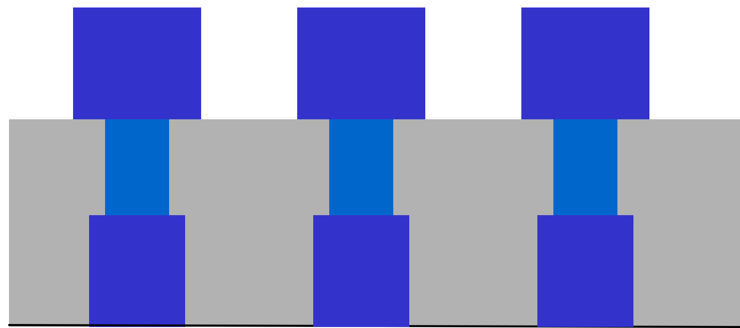


Metal deposition

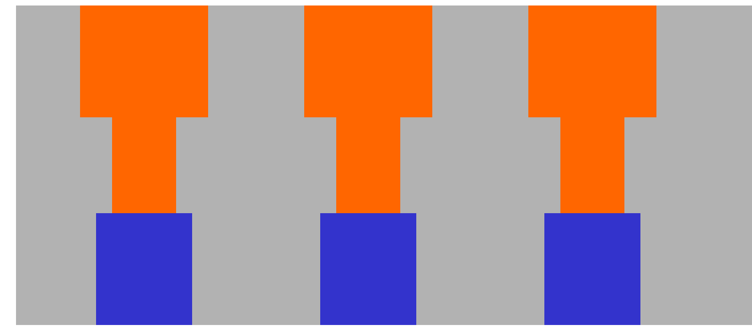


Metal deposition

Interconnection Processes



Metal etch



Metal polish

Summary

- Applications of dielectric thin film are STI, sidewall spacer, PMD, IMD and PD, in which IMD application is the dominant one
- Silicon oxide and silicon nitride are the two most commonly used dielectric materials

Summary

- Basic CVD process sequence: introducing precursor, precursor diffusion and adsorption, chemical reaction, gaseous byproducts desorption and diffusion
- Surface-reaction-limited regime
- Mass-transport-limited (MTL) regime
  - Most dielectric CVD reactors operate in MTL regime

Summary

- PMD uses PSG or BPSG, temperature are limited by thermal budget
- IMD mainly uses USG or FSG, temperature is limited by aluminum melting point
- PD usually uses both oxide and nitride

Summary

- Silane and TEOS are the two silicon sources for dielectric CVD processes
- O_2, N_2O, and O_3 are main oxygen precursors
- NH_3 and N_2 are the main nitrogen sources
- Fluorine chemistry is commonly used for dielectric CVD chamber dry clean
  - CF_4, C_2F_6, C_3F_8 and NF_3 are the most commonly used fluorine source gases

Summary

- Argon sputtering process is used for dep/etch/dep gap fill application
- CF_4/O_2 etchback is used for planarization
- Compressive stress (~100 MPa) is favored for the dielectric thin film

Summary

- HDP CVD
  - SiH_4 and O_2 to deposit oxide
  - Ar for sputtering
  - High aspect ratio gap fill
  - ICP and ECR: most commonly used HDP sources
- Low-κ and copper for future interconnection
- High-κ dielectric for gate or DRAM capacitor

Chapter 11
Metallization

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Objectives

- Explain device application of metallization
- List three most commonly used metals
- List three different metallization methods
- Describe the sputtering process
- Explain the purpose of high vacuum in metal deposition processes

Metallization

- Definition
- Applications
- PVD vs. CVD
- Methods
- Vacuum
- Metals
- Processes
- Future Trends

Metallization

- Processes that deposit metal thin film on wafer surface.

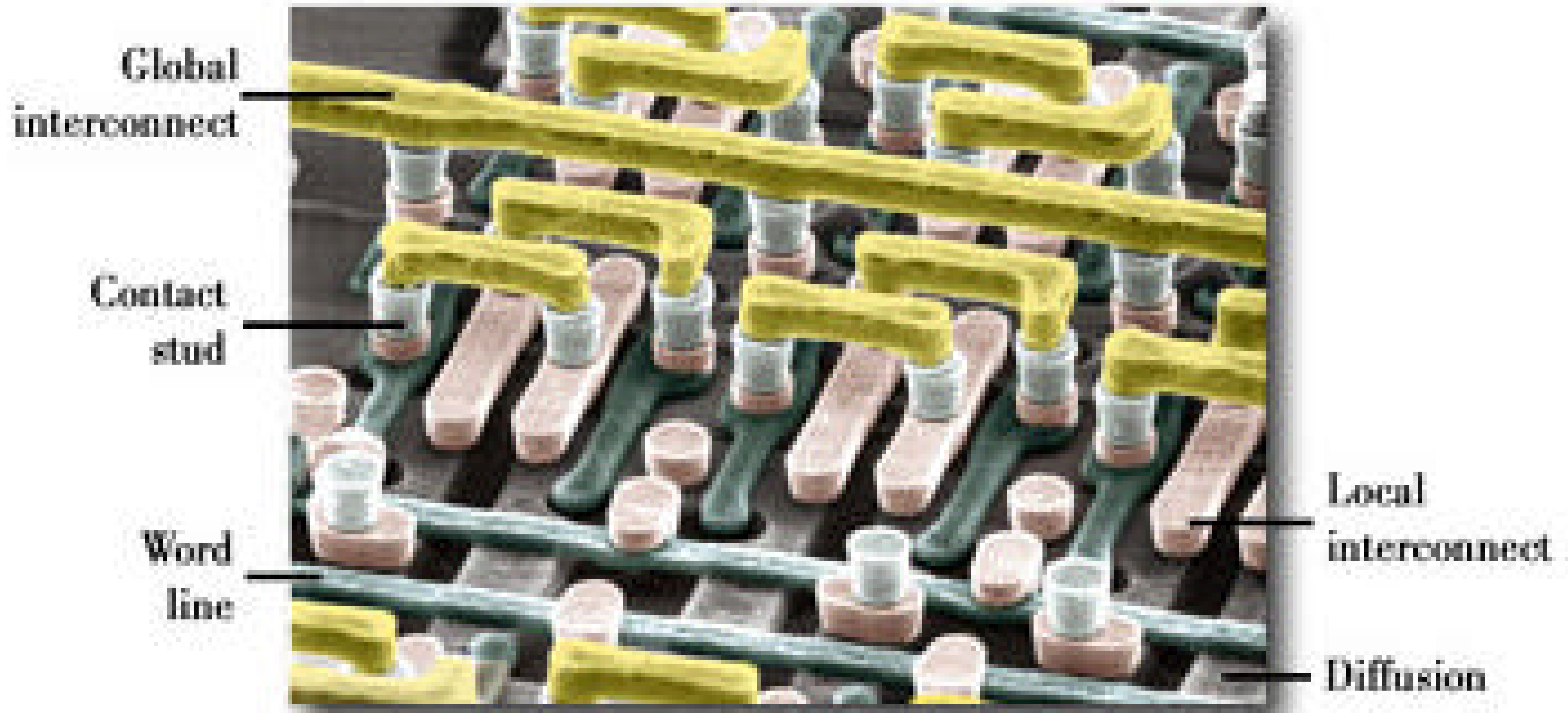
Applications

- Interconnection
- Gate and electrodes
- Micro-mirror
- Fuse

CMOS: Standard Metallization

Ti/TiN
TiN, ARC
$TiSi_2$
Metal 1, Al•Cu
W
BPSG
n^+
n^+
p^+
p^+
P-Well
N-Well
P-epi
P-wafer

Applications: Interconnection



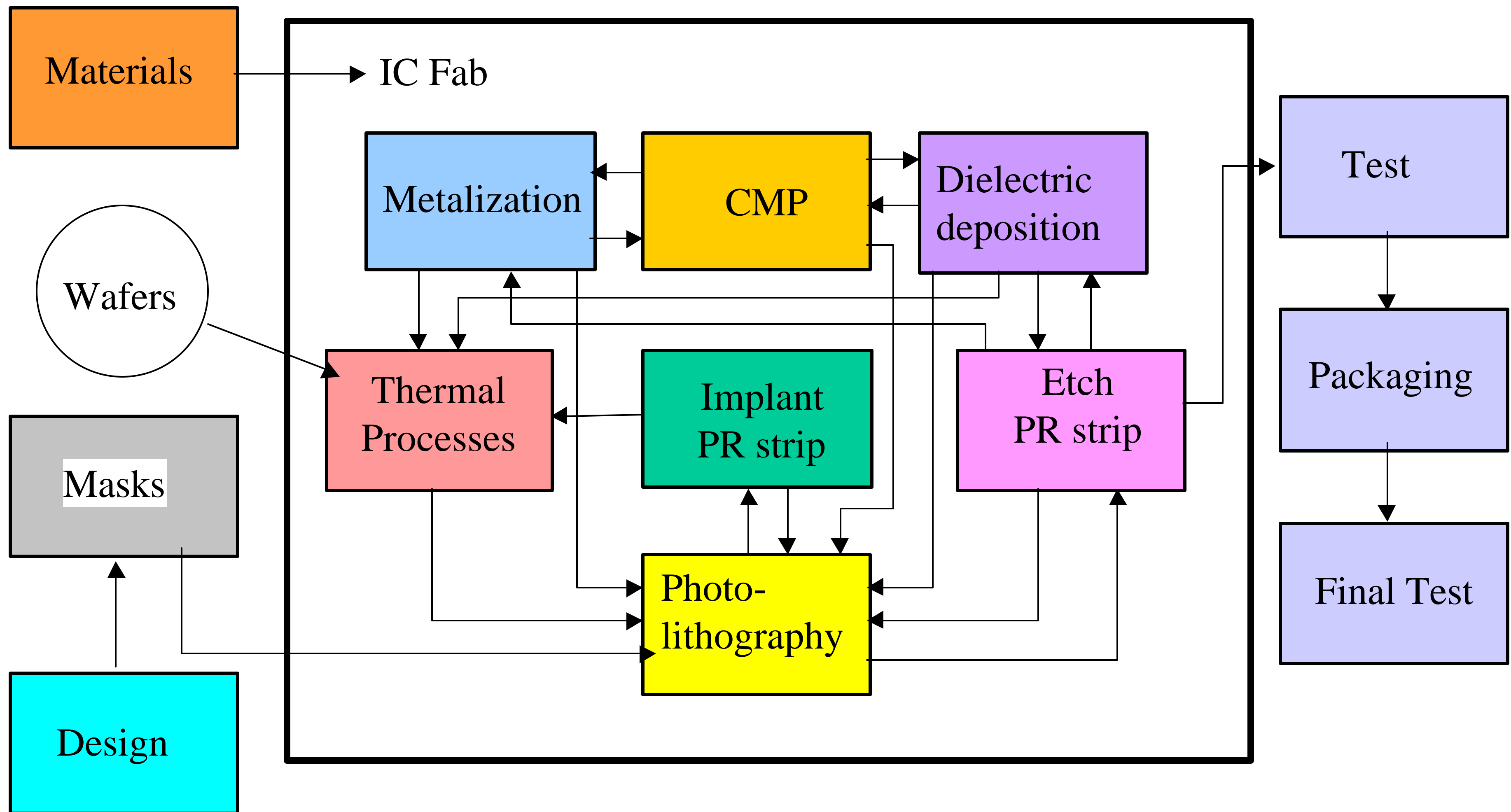
Applications: Interconnection

- Dominate the metallization processes
- Al-Cu alloy is most commonly used
- W plug, technology of 80s and 90s
- Ti, welding layer
- TiN, barrier, adhesion and ARC layers
- The future is --- Cu!

Copper Metallization

Ti/TiN
SiN
$CoSi_2$
Ta or TaN
M1
Cu
FSG
Cu
Cu
FSG
PSG
W
STI
n^+
n^+
USG
p^+
p^+
P-Well
N-Well
P-Epi
P-Wafer

Wafer Process Flow



Applications: Gate and Electrode

- Al gate and electrode
- Polysilicon replace Al as gate material
- Silicide
  - WSi_2
  - $TiSi_2$
  - $CoSi_2$, $MoSi_2$, $TaSi_2$, …
- Pt, Au, …as electrode for DRAM capacitors

Q & A

- Can we reduce all dimensions of metal interconnection line at the same ratio?

- $R=\rho\, l/wh$. When we shrink all dimensions (length l, width w, and height h) accordingly to the shrinking of the device feature size, resistance R increases,
- Slower circuit and more power consumption

Applications: Micro-mirror

- Digital projection display
- Aluminum-Titanium Alloy
- Small grain, high reflectivity
- “Home Theater”

Applications: Fuse

- For programmable read-only memory (PROM)
- High current generates heat which melt thin Al line and open the circuit
- Polysilicon also being used as fuse materials

Conducting Thin Films

Conducting Thin Films

- Polysilicon
- Silicides
- Aluminum alloy
- Titanium
- Titanium Nitride
- Tungsten
- Copper
- Tantalum

Polysilicon

- Gates and local interconnections
- Replaced aluminum since mid-1970s
- High temperature stability
  - Required for post implantation anneal process
  - Al gate can not use form self-aligned source/drain
- Heavily doped
- LPCVD in furnace

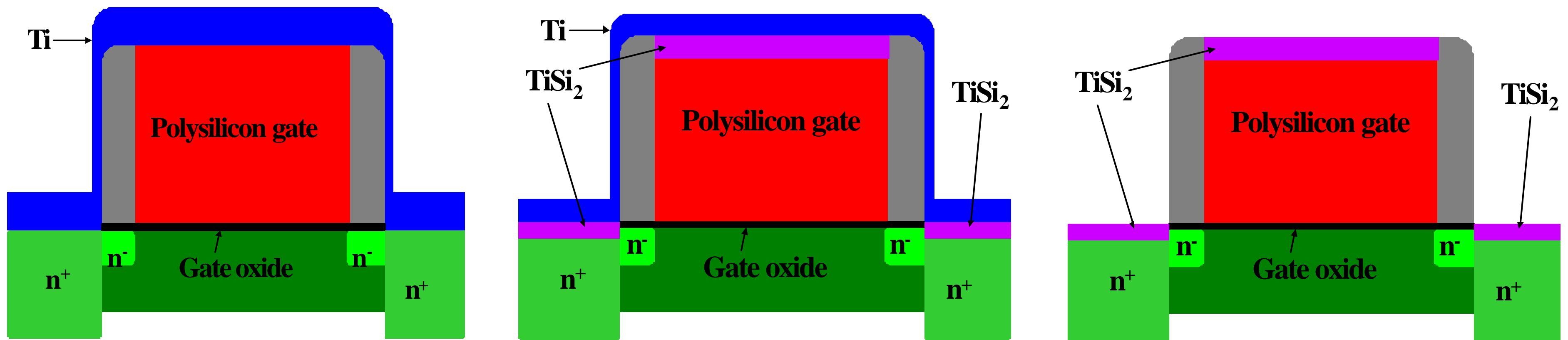
Silicide

- Much lower resistivity than polysilicon
- $TiSi_2$, WSi_2, and $CoSi_2$ are commonly used

Salicide

- $TiSi_2$ and $CoSi_2$
  - Argon sputtering removes the native oxide
  - Ti or Co deposition
  - Annealing process forms silicide
  - Ti or Co don’t react with SiO_2, silicide is formed at where silicon contacts with Ti or Co
  - Wet strips unreacted Ti or Co
  - Optional second anneal to increase conductivity

Self-aligned Titanium Silicide Formation



Titanium deposition

Silicide annealing

Titanium wet striping

Tungsten Silicide

- Thermal CVD process
  - WF_6 as the tungsten precursor
  - SiH_4 as the silicon precursor.
- Polycide stack is etched
  - Fluorine chemistry etches WSi_x
  - Chlorine chemistry etches polysilicon
- Photoresist stripping
- RTA increases grain size and conductivity

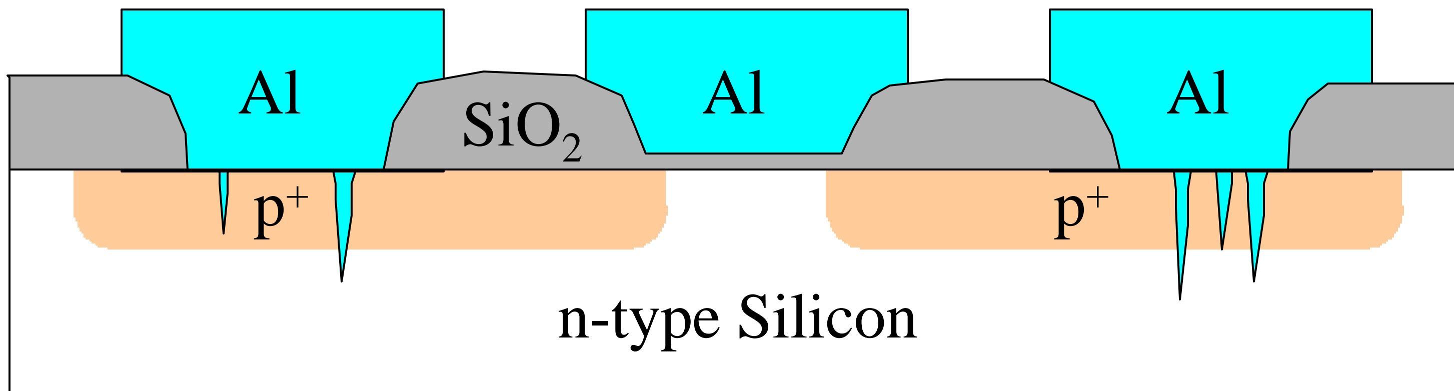
Aluminum

- Most commonly used metal
- The fourth best conducting metal
  - Silver 1.6 μΩ·cm
  - Copper 1.7 μΩ·cm
  - Gold silver 2.2 μΩ·cm
  - Aluminum 2.65 μΩ·cm
- It was used for gate before mid-1970

Aluminum-Silicon Alloy

- Al make direct contact with Si at source/drain
- Si dissolves in Al and Al diffuses into Si
- Junction spike
  - Aluminum spikes punctuate doped junction
  - Short source/drain with the substrate
- ~1% of Si in Al saturates it
- Thermal anneal at 400 °C to form Si-Al alloy at the silicon-aluminum interface

Junction Spike



Electromigration

- Aluminum is a polycrystalline material
- Many mono-crystalline grains
- Current flows through an aluminum line
- Electrons constantly bombards the grains
- Smaller grains will start to move
- This effect is called electromigration

Electromigration

- Electromigration tear the metal line apart
- Higher current density in the remaining line
  - Aggravates the electron bombardment
  - Causes further aluminum grain migration
  - Eventually will break of the metal line
- Affect the IC chip reliability
- Aluminum wires: fire hazard of old houses

Electromigration Prevention

- When a small percent of copper is alloyed with aluminum, electromigration resistance of aluminum significantly improved
- Copper serves as “glue” between the aluminum grains and prevent them from migrating due to the electron bombardment
- Al-Si-Cu alloy was used
- Al-Cu (0.5%) is very commonly

Aluminum Alloy Deposition

- PVD
  - Sputtering
  - Evaporation
    - Thermal
    - Electron beam
- CVD
  - Dimethylaluminum hydride [DMAH, $Al(CH_3)_2H$]
  - Thermal process

PVD vs. CVD

- CVD: Chemical reaction on the surface
- PVD: No chemical reaction on the surface

- CVD: Better step coverage (50% to ~100%) and gap fill capability
- PVD: Poor step coverage (~ 15%) and gap fill capability

PVD vs. CVD

- PVD: higher quality, purer deposited film, higher conductivity, easy to deposit alloys

- CVD: always has impurity in the film, lower conductivity, hard to deposit alloys

Some Facts About Aluminum

Name	Aluminum
Symbol	Al
Atomic number	13
Atomic weight	26.981538
Discoverer	Hans Christian Oersted
Discovered at	Denmark
Discovery date	1825
Origin of name	From the Latin word "alumen" meaning "alum"
Density of solid	2.70 g/cm^3
Molar volume	10.00 cm^3
Velocity of sound	5100 m/sec
Hardness	2.75
Electrical resistivity	2.65 μΩ cm
Reflectivity	71%
Melting point	660 C
Boiling point	2519 C
Thermal conductivity	235 $W\ m^{-1}\ K^{-1}$
Coefficient of linear thermal expansion	23.1 $10^{-6}\ K^{-1}$
Etchants (wet)	H_3PO_4, HNO_4, CH_3COOH
Etchants (dry)	Cl_2, BCl_3
CVD Precursor	$Al(CH_3)_2H$

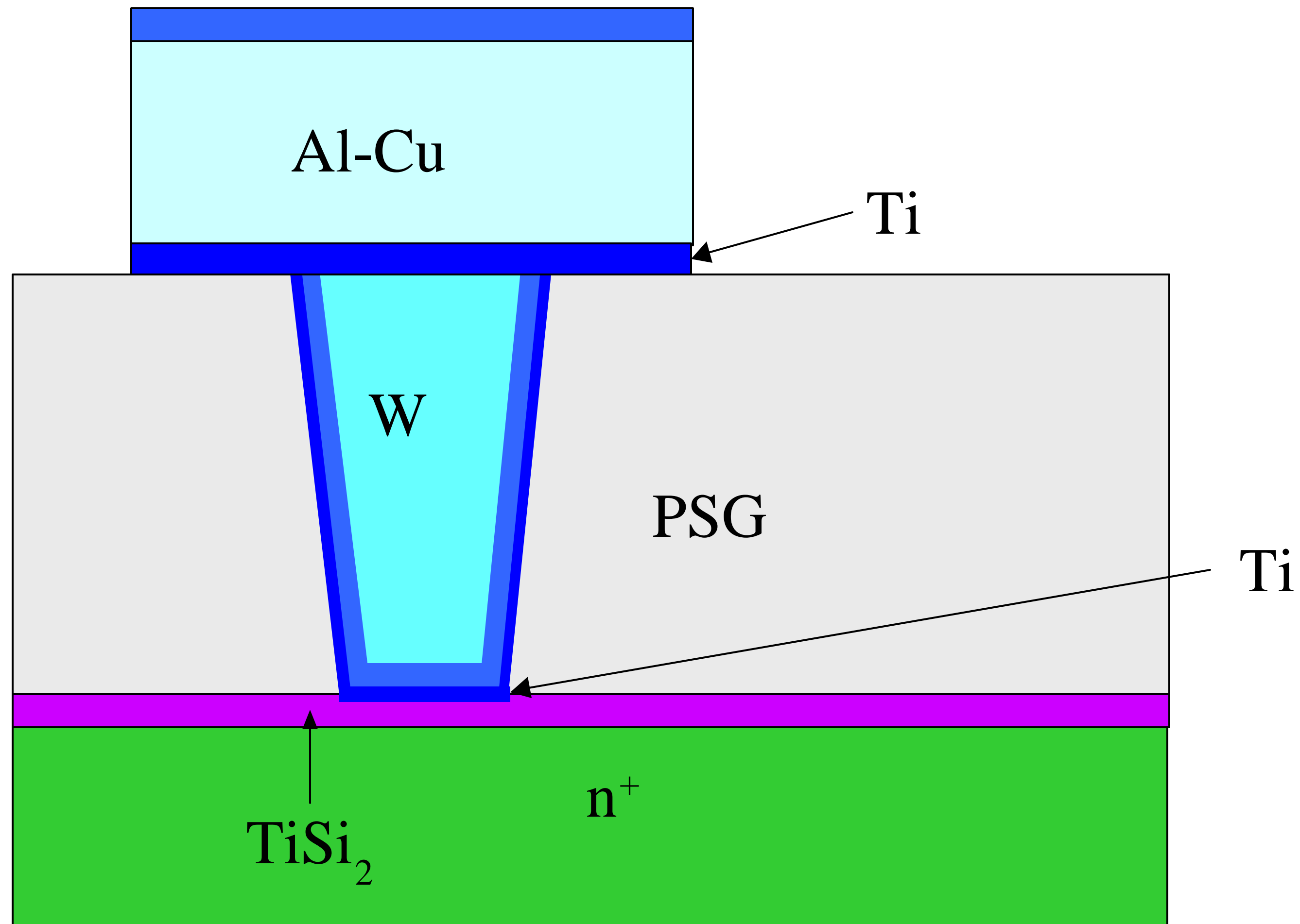
Titanium

- Applications
  - Silicide formation
  - Titanium nitridation
  - Wetting layer
  - Welding layer

Welding Layer

- Reduce contact resistance.
  - Titanium scavenges oxygen atoms
  - Prevent forming high resistivity WO_4 and Al_2O_3.
- Use with TiN as diffusion barrier layer
  - Prevent tungsten from diffusing into substrate
  -

Applications of Titanium



Some Face About Titanium

Name	Titanium
Symbol	Ti
Atomic number	22
Atomic weight	47.867
Discoverer	William Gregor
Discovered at	England
Discovery date	1791
Origin of name	Named after the "Titans", (the sons of the Earth goddess in Greek mythology)
Density of solid	4.507 g/cm^3
Molar volume	10.64 cm^3
Velocity of sound	4140 m/sec
Hardness	6.0
Electrical resistivity	40 $\mu\Omega$ cm
Melting point	1668 C
Boiling point	3287 C
Thermal conductivity	22 $W\ m^{-1}\ K^{-1}$
Coefficient of linear thermal expansion	8.6 $10^{-6}\ K^{-1}$
Etchants (wet)	H_2O_2, H_2SO_4
Etchants (dry)	Cl_2, NF_3
CVD Precursor	$TiCl_4$

Titanium Nitride

- Barrier layer
  - prevents tungsten diffusion
- Adhesion layer
  - help tungsten to stick on silicon oxide surface
- Anti-reflection coating (ARC)
  - reduce reflection and improve photolithography resolution in metal patterning process
  - prevent hillock and control electromigration
- Both PVD and CVD

Titanium Nitride PVD

- Barrier layer, adhesion layer and ARC
- Reactive sputtering a Ti target with Ar and N_2
  - N_2 molecules dissociate in plasma
  - Nitrogen free radials (N)
  - N reacts with Ti and form TiN layer on Ti surface
  - Ar ions sputter TiN off and deposit them on the wafer surface

Titanium Nitride CVD

- Barrier layer and adhesion layer
- Better step coverage than PVD
- Metal organic process (MOCVD)
  - ~350 °C
  - TDMAT, $Ti[N(CH_3)_2]_4$
  - Via application

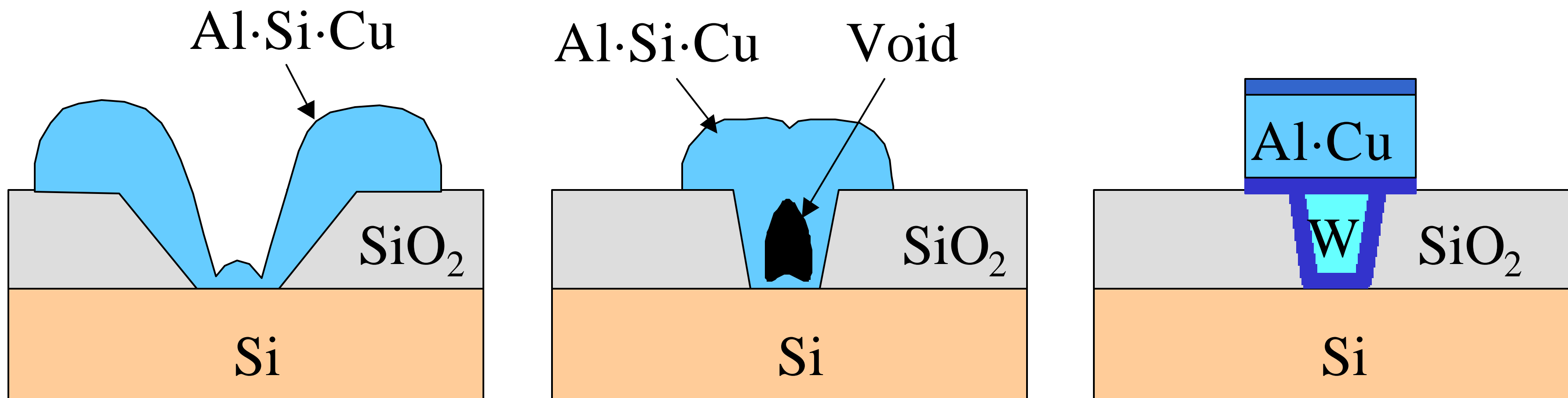
Titanium Nitridation

- Titanium PVD
- Nitridation of titanium surface with ammonia
- Rapid thermal process

Tungsten

- Metal plug in contact and via holes
- contact holes become smaller and narrower
- PVD Al alloy: bad step coverage and void
- CVD W: excellent step coverage and gap fill
- higher resistivity: 8.0 to 12 μΩ·cm compare to PVD Al alloy (2.9 to 3.3 μΩ·cm)
- only used for local interconnections and plugs

Evolution of Contact Processes



Widely tapered contact hole, PVD metal fill

Narrow contact hole, void with PVD metal fill

Narrow contact hole, WCVD for tungsten plug

Tungsten CVD

- WF_6 as the tungsten precursor
- React with SiH_4 to form nucleation layer
- React with H_2 for bulk tungsten deposition
- Needed a TiN layer to adhere on oxide

Some Facts About Tungsten

Name Symbol	Tungsten W
Atomic number Atomic weight	74 183.84
Discoverer	Fausto and Juan Jose de Elhuyar
Discovered at	Spain
Discovery date	1783
Origin of name	From the Swedish words "tung sten" meaning "heavy stone". W comes from "wolfram", named after the tungsten mineral wolframite.
Density of solid	19.25 g/cm^3
Molar volume	9.47 cm^3
Velocity of sound	5174 m/sec
Hardness	7.5
Reflectivity	62%
Electrical resistivity	5 μΩ·cm
Melting point	3422 °C
Boiling point	5555 °C
Thermal conductivity Coefficient of linear thermal expansion Etchants (wet)	170 W m^{-1} K^{-1} 4.5×10^{-6} K^{-1} KH_2PO_4, KOH, and $K_3Fe(CN)_6$; boiling H_2O
Etchants (dry) CVD Precursor	SF_6, NF_3, CF_4, etc. WF_6

W Plug and TiN/Ti Barrier/Adhesion Layer

Copper

- Low resistivity (1.7 μΩ·cm),
  - lower power consumption and higher IC speed
- High electromigration resistance
  - better reliability
- Poor adhesion with silicon dioxide
- Highly diffusive, heavy metal contamination
- Very hard to dry etch
  - copper-halogen have very low volatility

Copper Deposition

- PVD of seed layer
- ECP or CVD bulk layer
- Thermal anneal after bulk copper deposition
  - increase the grain size
  - improving conductivity

Some Facts About Copper

Name	Copper
Symbol	Cu
Atomic number	29
Atomic weight	63.546
Discoverer Discovered at	Copper had been used by human being since ancient time, long before any written history.
Discovery date	
Origin of name	From the Latin word "cuprum" meaning the island of "Cyprus"
Density of solid	8.92 g/cm^3
Molar volume	7.11 cm^3
Velocity of sound Hardness Reflectivity	3570 m/sec 3.0 90%
Electrical resistivity	1.7 μΩ·cm
Melting point	1084.77 °C
Boiling point	5555 °C
Thermal conductivity	400 W m^{-1} K^{-1}
Coefficient of linear thermal expansion	16.5×10^{-6} K^{-1}
Etchants (wet)	HNO_4, HCl, H_2SO_4
Etchants (dry)	Cl_2, needs low pressure and high temperature
CVD Precursor	(hfac)Cu(tmvs)

Tantalum

- Barrier layer
- Prevent copper diffusion
- Sputtering deposition

Some Facts About Tantalum

Name	Tantalum
Symbol	Ta
Atomic number Atomic weight	73 180.9479
Discoverer	Anders Ekeberg
Discovered at	Sweden
Discovery date	1802
Origin of name	From the Greek word "Tantalos" meaning "father of Niobe" due it close relation to niobium in the Periodic Table
Density of solid	16.654g/cm^3
Molar volume	7.11 cm^3
Velocity of sound	3400 m/sec
Hardness	3.0
Reflectivity	90%
Electrical resistivity	12.45μΩ·cm
Melting point	2996 °C
Boiling point	5425°C
Thermal conductivity	57.5 W m^{-1} K^{-1}
Coefficient of linear thermal expansion	6.3×10^{-6} K^{-1}

Cobalt

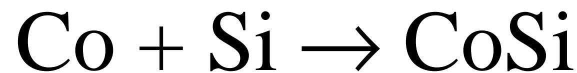
- Mainly used for cobalt silicide ($CoSi_2$).
- Normally deposited with a sputtering process

Cobalt Silicide

- Titanium silicide grain size: ~ 0.2 μm
- Can't be used for 0.18 mm gate
- Cobalt silicide will be used
- Salicide process

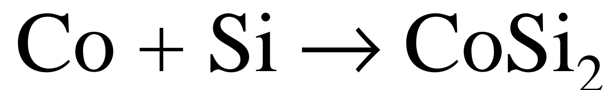
Cobalt Silicide: Process

- Pre-deposition argon sputtering clean
- Cobalt sputtering deposition
- First anneal, 600 °C



$$Co + Si \rightarrow CoSi$$

- Strip Unreacted cobalt
- Second anneal, 700 °C



$$Co + Si \rightarrow CoSi_2$$

Some Facts About Cobalt

Name	Tantalum
Symbol	Co
Atomic number	27
Atomic weight	180.9479
Discoverer	Georg Brandt
Discovered at	Sweden
Discovery date	1735
Origin of name	From the German word "kobald" meaning "goblin" or evil spirit
Density of solid	8.900 g/cm^3
Molar volume	6.67 cm^3
Velocity of sound	4720 m/sec
Hardness	6.5
Reflectivity	67%
Electrical resistivity	13 $\mu\Omega \cdot cm$
Melting point	1768 K or 1495 °C
Boiling point	3200 K or 2927 °C
Thermal conductivity	100 $W\ m^{-1}\ K^{-1}$
Coefficient of linear thermal expansion	$13.0 \times 10^{-6}\ K^{-1}$

Metal Thin Film Characteristics

Metal Thin Film Measurements

- Thickness.
- Stress
- Reflectivity
- Sheet resistance

Metal Thin Film Thickness

- TEM and SEM
- Profilometer
- 4-point probe
- XRF
- Acoustic measurement

TEM and SEM

- Cross section
- TEM: very thin film, few hundred Å
- SEM: film over thousand Å

Q & A

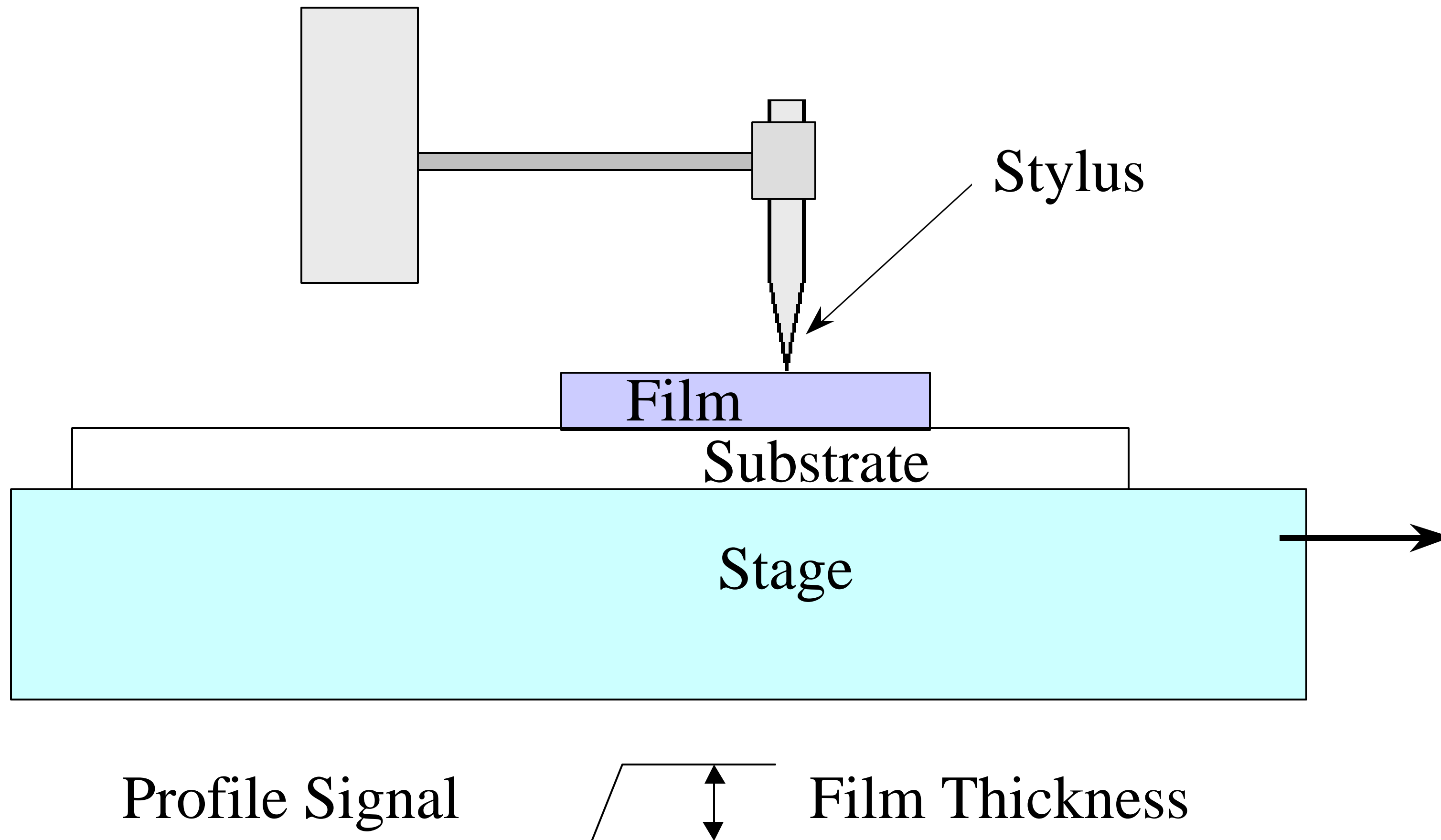
- Why is SEM photo is always in black and white?

- Intensity of the secondary electron emission
  - strong or weak signals
  - photo image: bright and dim, black and white
- SEM photo can be painted after it has been analyzed

Profilometer

- Thicker film (> 1000 Å),
- Patterned etch process prior to measurement
- Stylus probe senses and records microscopic surface profile

Schematic of Stylus Profilometer



Four-point Probe

- Measure sheet resistance
- Commonly used to monitor the metal film thickness by assuming the resistivity of the metal film is a constant all over the wafer surface

Acoustic Measurement

- New technique
- Directly measure opaque thin film thickness
- Non-contact process, can be used for production wafer

Acoustic Measurement

- Laser shots on thin film surface
- Photo-detector measures reflected intensity
- 0.1 ps laser pulse heat the spot up 5 to 10 °C
- Thermal expansion causes a sound wave
- It propagates in the film and reflects at the interface of the different materials
- The echo causes reflectivity change when it reaches the thin film surface.

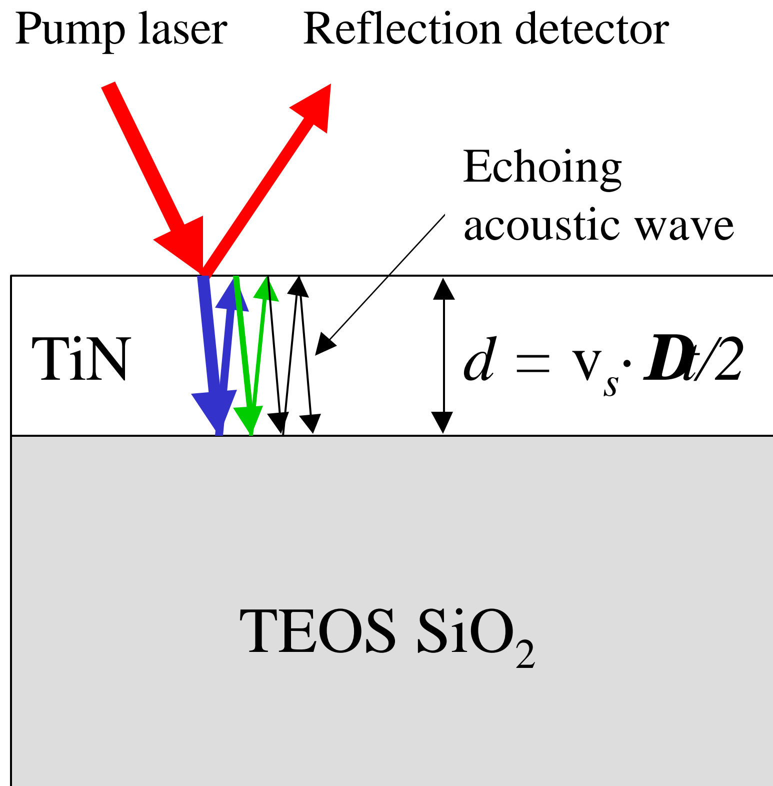
Acoustic Measurement

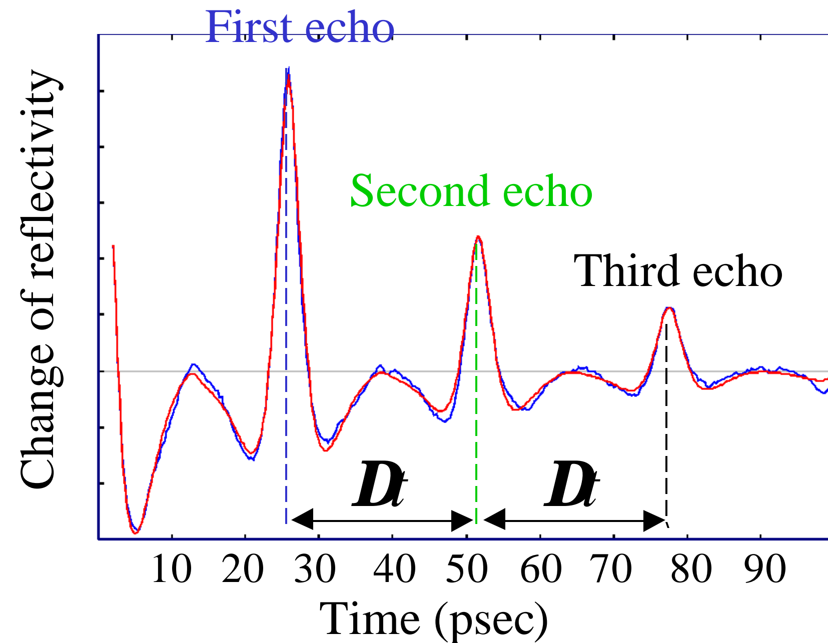
- Acoustic wave echoes back and forth in film
- The film thickness can be calculated by

$$d = V_s \, \boldsymbol{D}t/2$$

- V_s is speed of sound and $\boldsymbol{D}t$ is time between reflectivity peaks
- The decay rate the echo is related to the film density.
- Multi-layer film thickness

Acoustic Method Measurement





TiN Thickness

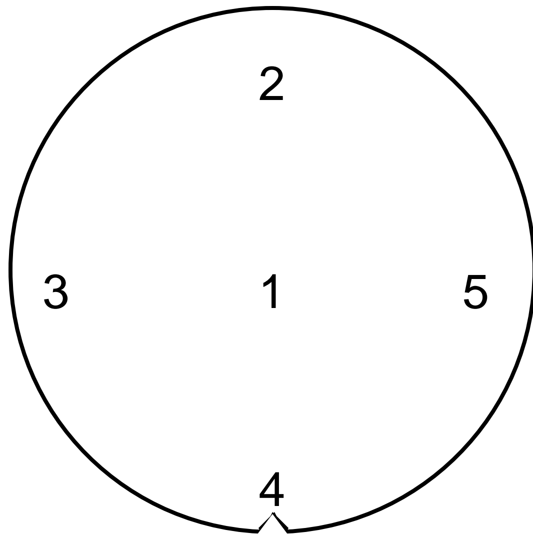
- $d = V_s \cdot \boldsymbol{D}t/2$
- Sound velocity in TiN film V_s = 95 Å/ps
- $\boldsymbol{D}t$ » 25.8 ps

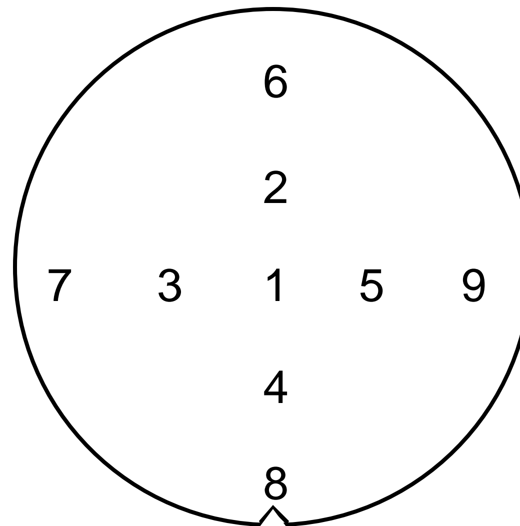
- d = 1225 Å

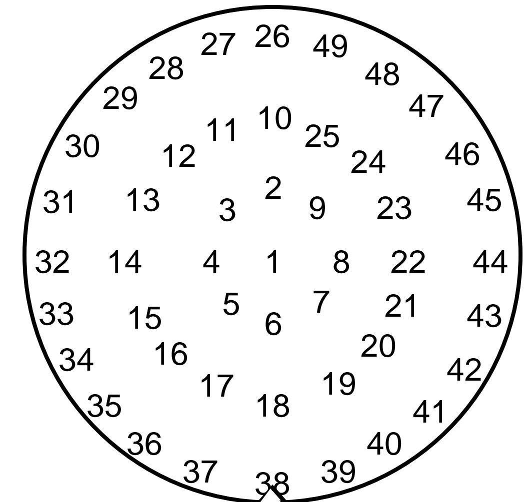
Uniformity

- The uniformity, in fact it is non-uniformity, of the thickness, sheet resistance, and reflectivity are routinely measured during the process development and for the process maintenance.
- It can be calculated by measuring at multiple locations on a wafer

Mapping Patterns for Uniformity Measurement







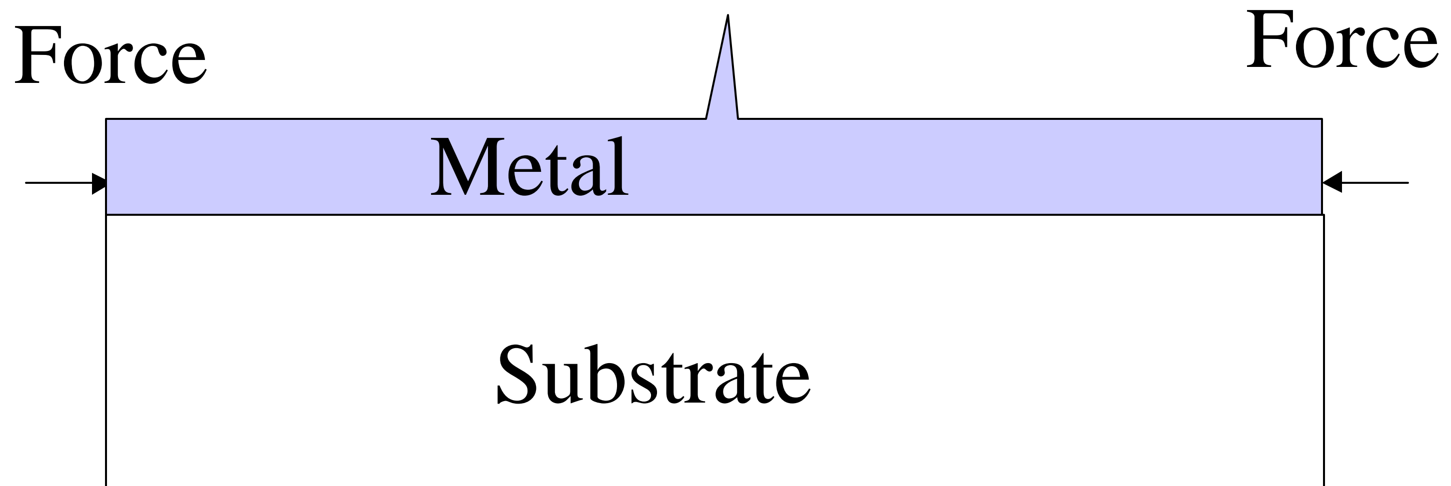
Uniformity

- Most commonly used non-uniformity definition: 49-point, 3σ standard deviation
- Clearly define non-uniformity
  - For the same set of data, different definitions causes different results
- 5-point and 9-point are commonly used in production

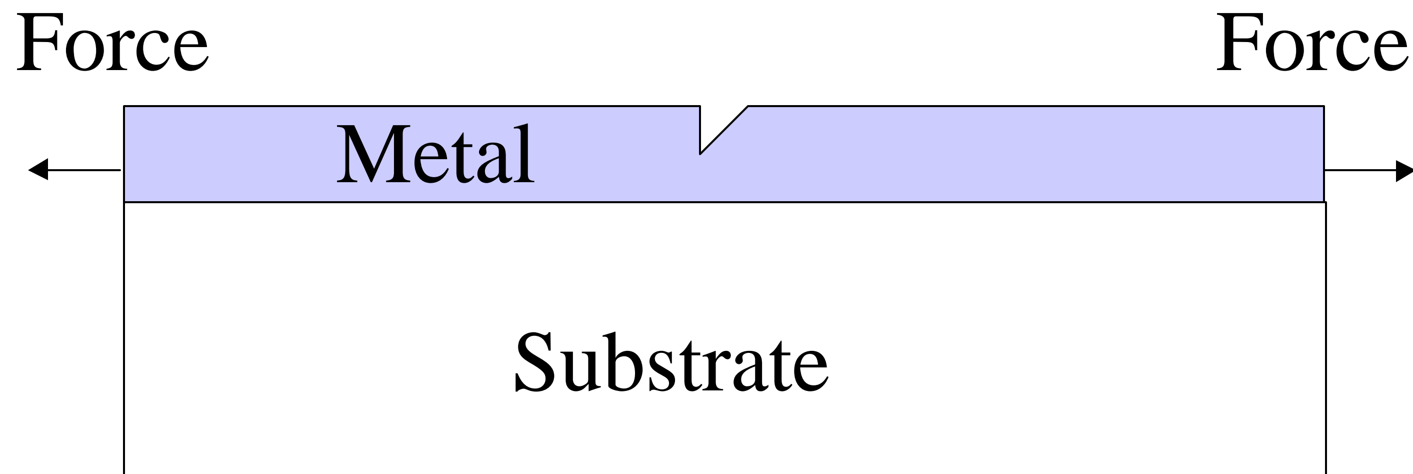
Stress

- Caused by mismatching between film and substrate
- Compressive and tensile
- High compressive stress causes hillocks
  - short metal wires between different layers
- High tensile stress causes cracks or peels

Compressive Stress Causes Hillock



Tensile Stress Causes Crack



Favorable Stress

- Aluminum has higher thermal expansion rate than silicon

  $\alpha_{Al} = 23.6\times10^{-6}\ K^{-1}, \quad \alpha_{Si} = 2.6\times10^{-6}\ K^{-1}$
- It favor tensile stress at room temperature
- Stress becomes less tensile when wafer is heated up later
  - metal annealing (~ 450 °C)
  - dielectric deposition (~ 400 °C)

Q & A

- Why does silicon oxide film favor compressive stress at room temperature?

- Silicon oxide has lower thermal expansion rate ($\alpha_{SiO2} = 0.5\times10^{-6}\ K^{-1}$) than the silicon
- If it has tensile stress at room temperature, it will become more tensile when the wafer is heated up in later processes

Reflectivity

- Reflectivity change indicates drift of process
- A function of film grain size and surface smoothness
- Larger grain size film has lower reflectivity
- Smoother metal surface has higher reflectivity
- Easy, quick and non-destructive
- Frequently performed in semiconductor fabs

Sheet Resistance

- 4-point probe
- Widely used to determine film thickness
- Assuming resistivity is the same on wafer
- Faster and cheaper than the profilometer, SEM, and acoustic measurement

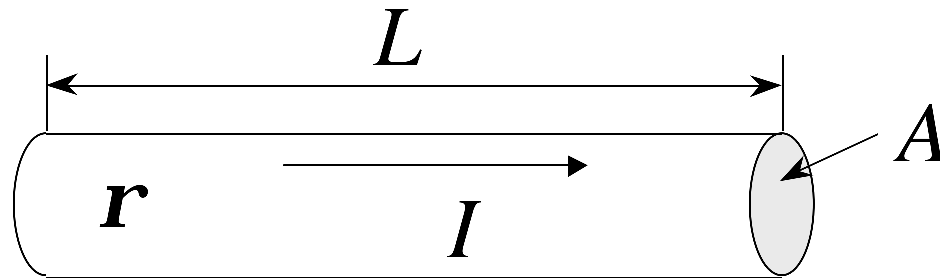
Sheet Resistance

- Sheet resistance (R_s) is a defined parameter

$$R_s = \boldsymbol{r}/t$$

- By measuring R_s, one can calculate film resistivity (ρ) if film thickness t is known, or film thickness if its resistivity is known

Resistance of a Metal Line

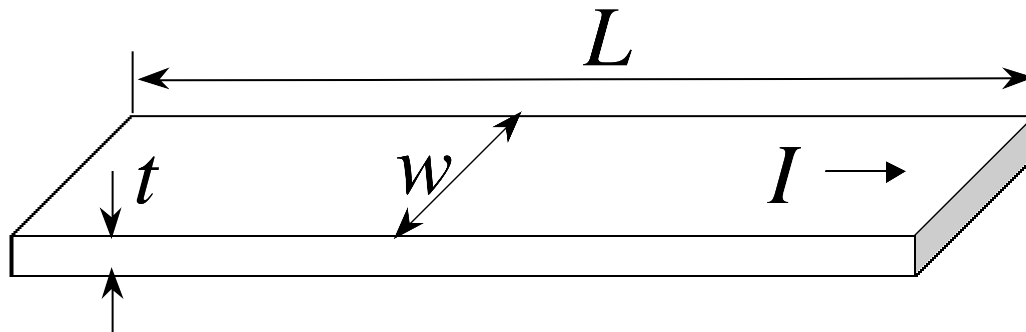


$$R = \boldsymbol{r}\,\frac{L}{A}$$

R = Resistance, ρ = Resistivity

L = Length, A = Area of line cross-section

Sheet Resistance Concepts



Apply current I and measure voltage V,

Resistance: $R = V/I = \boldsymbol{r}L/(wt)$

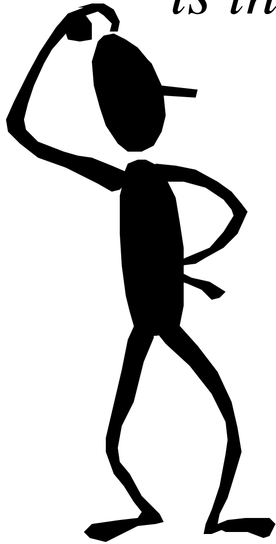
For a square sheet, $L = w$, so $R = \boldsymbol{r}/t = R_s$

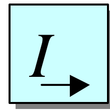
Unit of R_s: ohms per square (Ω/❒)

Sheet Resistance

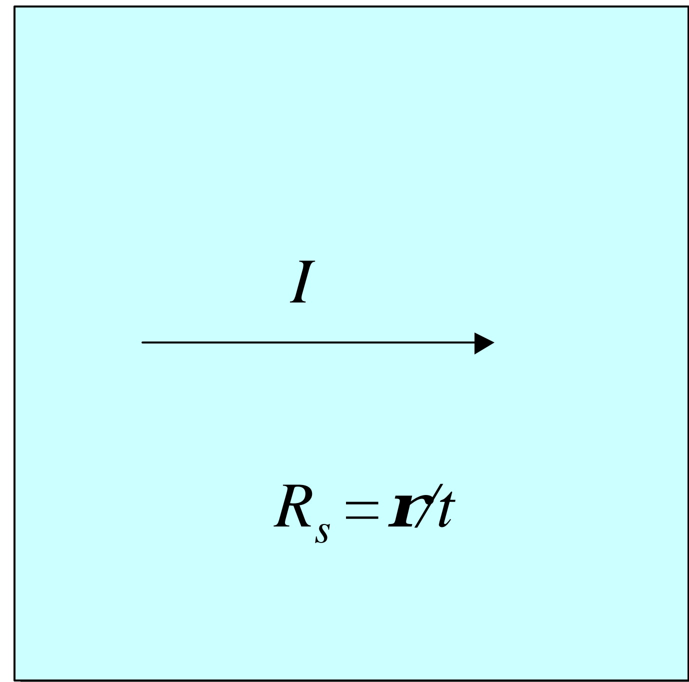
Sheet Resistance

Are you sure their resistance is the same?



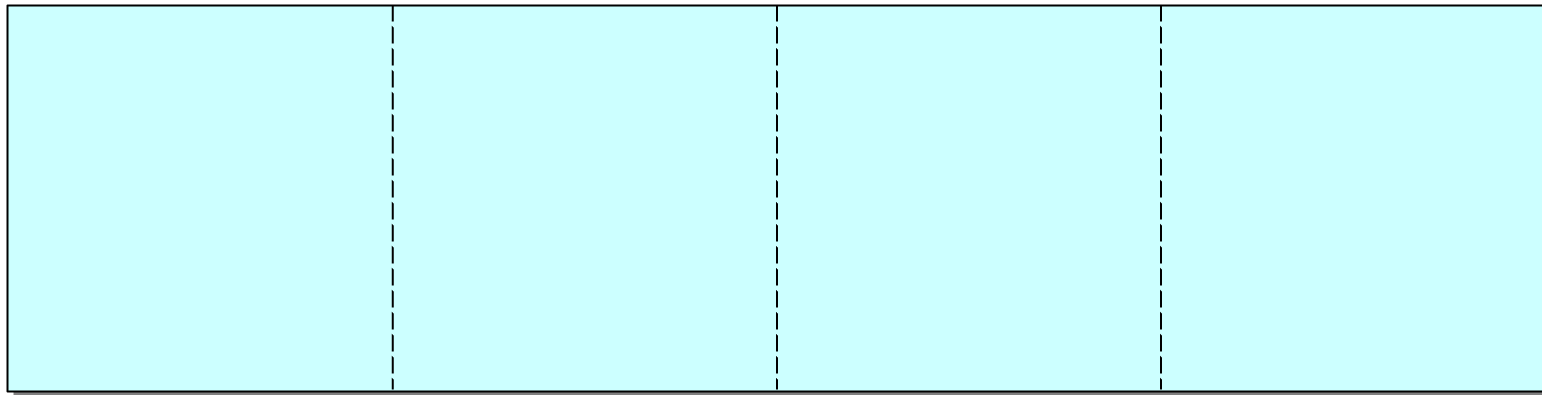


$R_s = \rho / t$

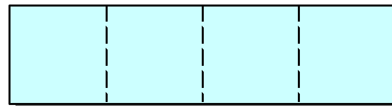


Sheet Resistance

For this two conducting lines patterned from the same metal thin film with the same length-to-width ratios, are their line resistance the same?



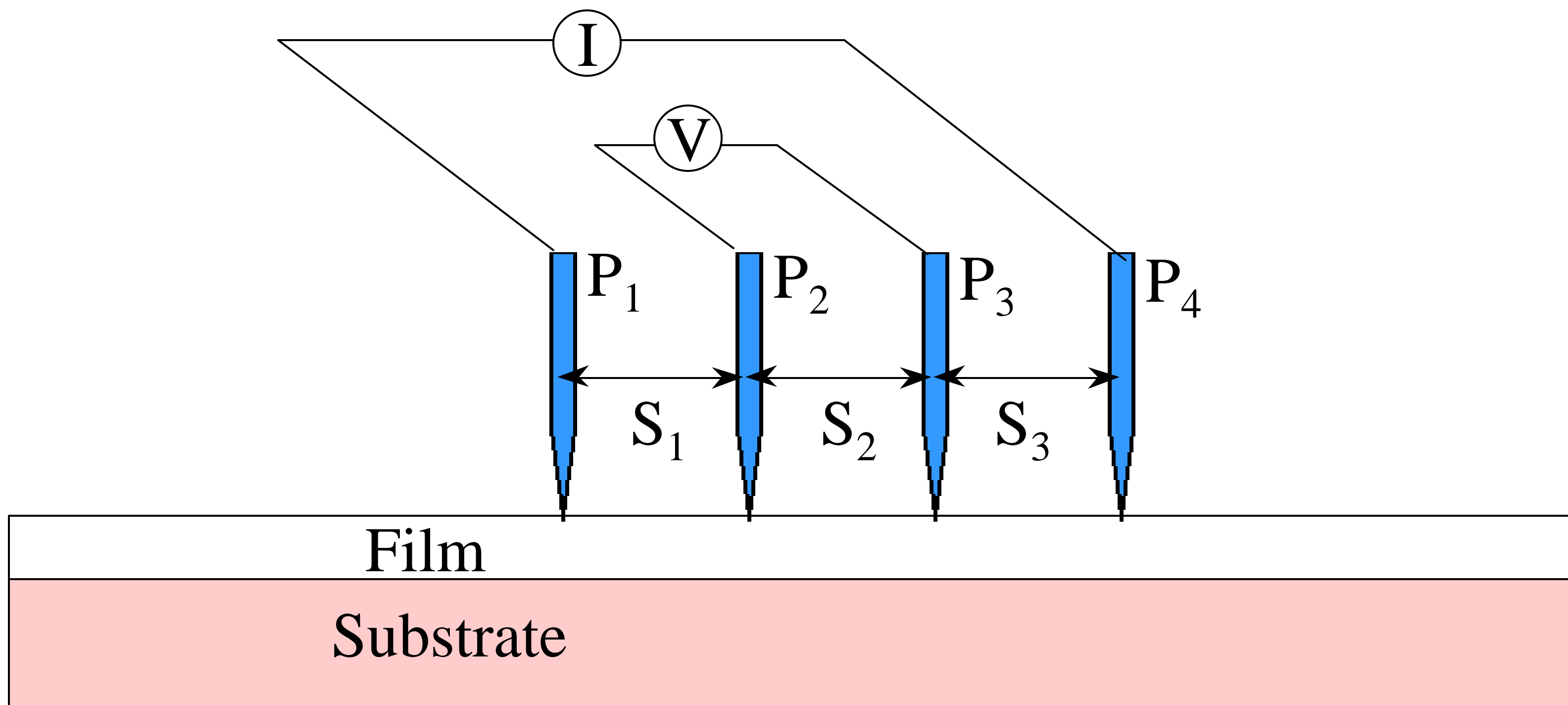
Yes.



Four-point Probe

- Commonly used tool for sheet resistance
- A current is applied between two pins and voltage is measured between other two pins
  - If current I is between P_1 and P_4, $\boldsymbol{R_s = 4.53\ V/I}$, V is voltage between P_2 and P_3
  - If current I is between P_1 and P_3, $\boldsymbol{R_s = 5.75\ V/I}$, V is voltage between R_2 and R_4
- Both configurations are used in measurement

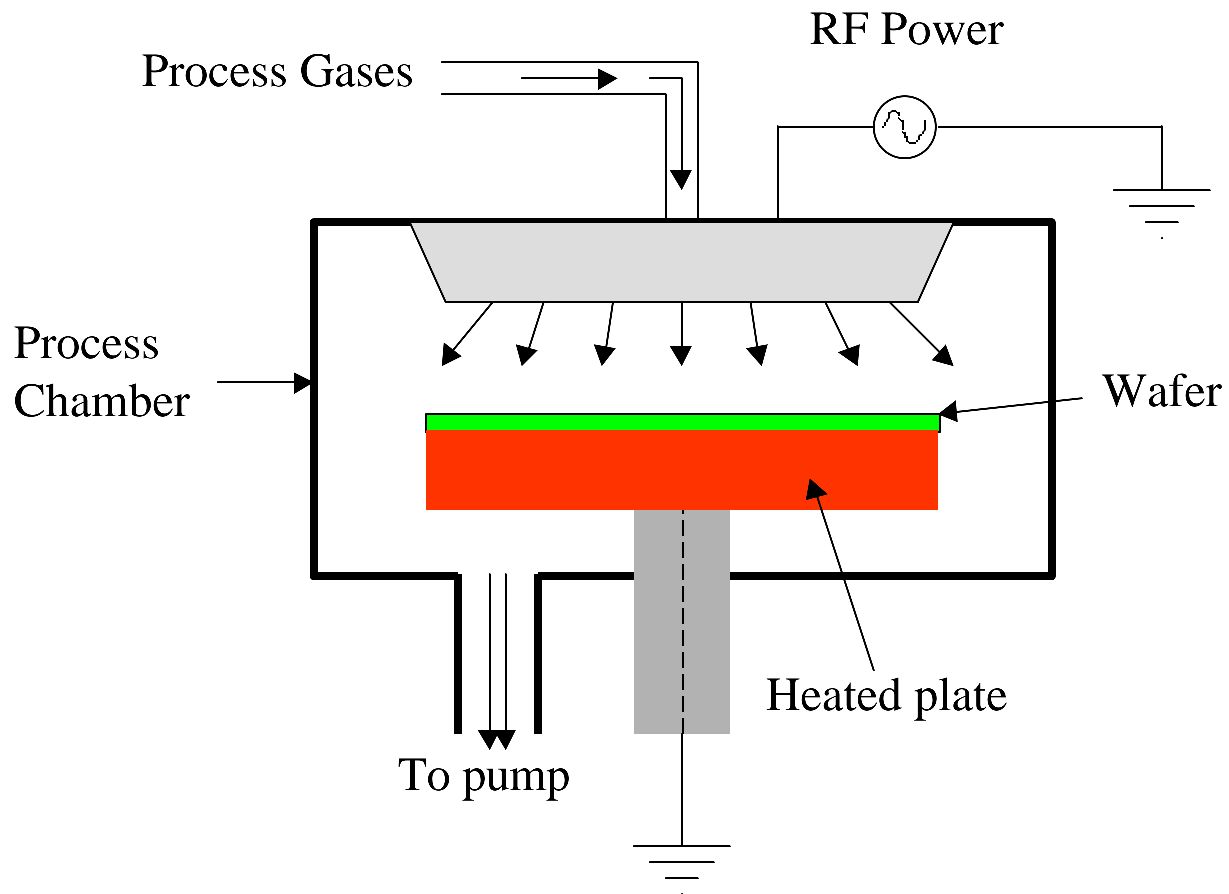
Four-Point Probe Measurement



Metal CVD

- Widely used to deposit metal
- Good step coverage and gap fill capability
  - can fill tiny contact holes to make connections between metal layers.
- Poorer quality and higher resistivity than PVD metal thin films.
  - Used for plugs and local interconnections
  - Not applied for global interconnections

Metal CVD Chamber



Metal CVD

- W, WSi_x, Ti, and TiN
- Thermal process, heat provides free energy needed for the chemical reaction
- RF system is used for plasma dry clean of the process chamber

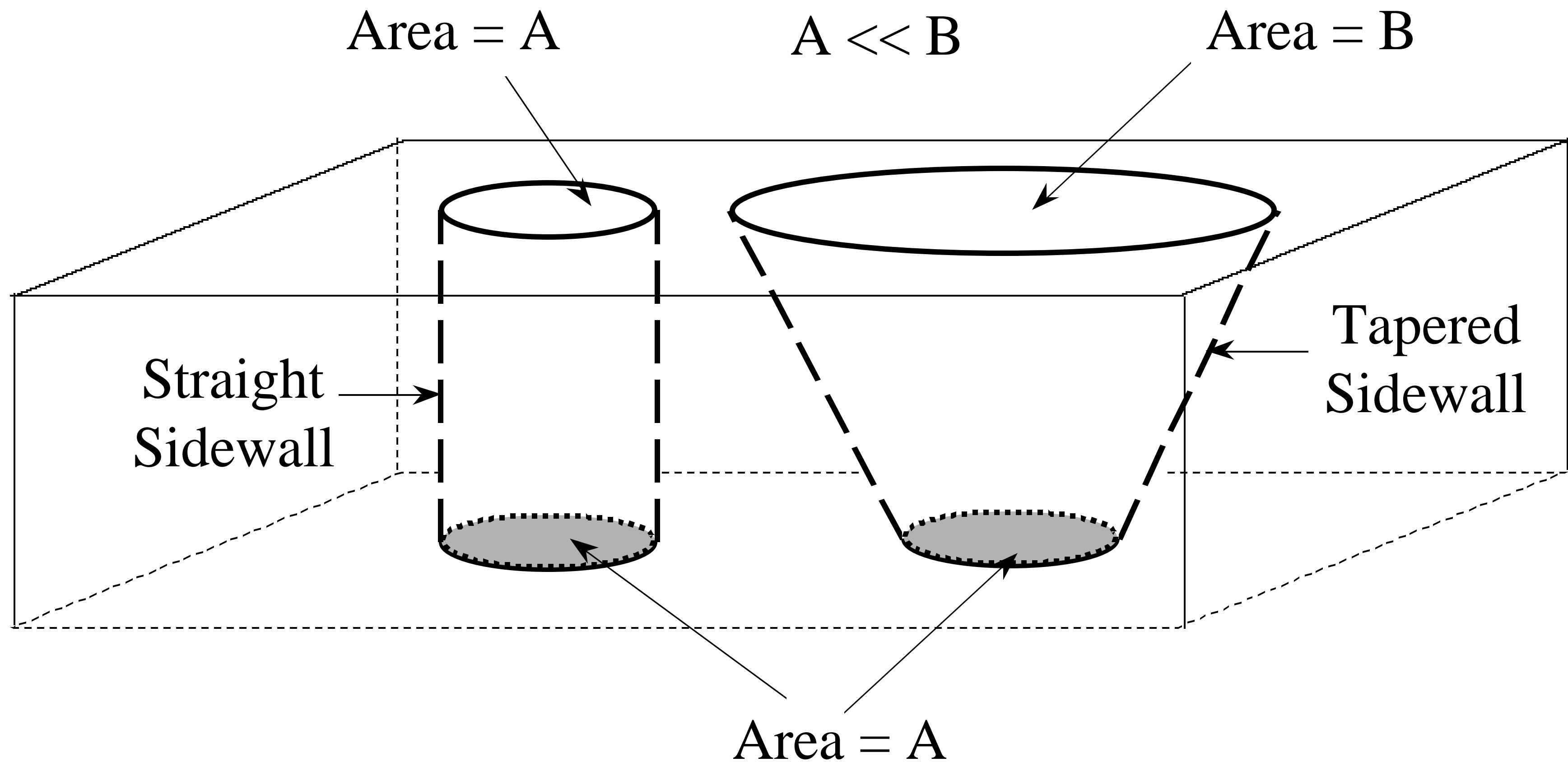
Metal CVD Process Steps

- Wafer into the chamber
- Slip valve closes
- Set up pressure and temperature, with secondary process gas(es)
- All process gases flow in, start deposition
- Termination of the main process gas. Secondary process gas(es) remain on
- Termination of all process gases
- Purge chamber with nitrogen
- Slip valve opens and robot pull wafer out

Metal CVD Chamber Clean Steps

- Chamber pumps down
- Set up pressure and temperature
- RF turns on. Start plasma and clean process
- RF turns off. Chamber is purged
- Set up pressure and temperature, with secondary process gas(es)
- Flows main process gas to deposit the seasoning layer
- Terminate the main process gas
- Terminate all process gases
- Purge chamber with nitrogen
- Chamber is ready for the next deposition

Vertical and Tapered Contact Holes



Tungsten CVD Basics

Tungsten source gas: tungsten hexafluoride (WF_6)

Additional reactant: hydrogen (H_2)

Temperature: 400 - 475 °C

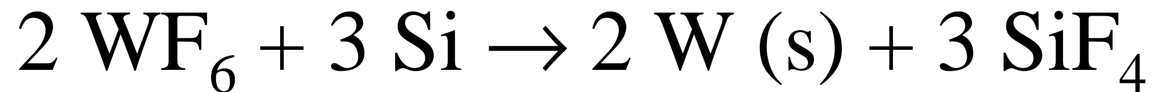
Step Coverage is 100 %

Typical W CVD Process

- Wafer transferred to chamber
- Pressure and gas flows (H_2, SiH_4) established
- Nucleation takes place (silane reduction of WF_6)
- Pressure and gas flows changed for bulk deposit
- Bulk deposit takes place (H_2 reduction of WF_6)
- Chamber pumped and purged
- Wafer transferred out of chamber

W CVD Reactions

Nucleation on silicon

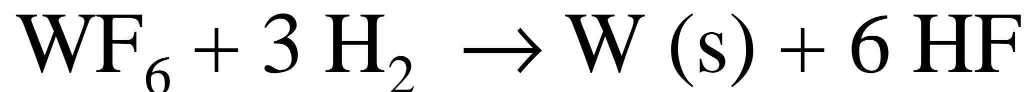


$$2\ WF_6 + 3\ Si \rightarrow 2\ W\ (s) + 3\ SiF_4$$

Nucleation on glue layer

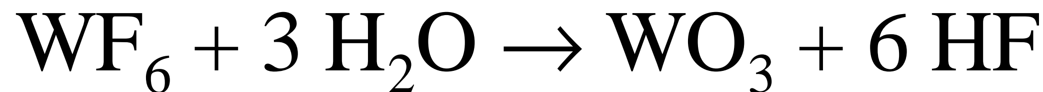
$$2\ WF_6 + 3\ SiH_4 \rightarrow 2\ W\ (s) + 3\ SiF_4 + 6\ H_2$$

Bulk deposit



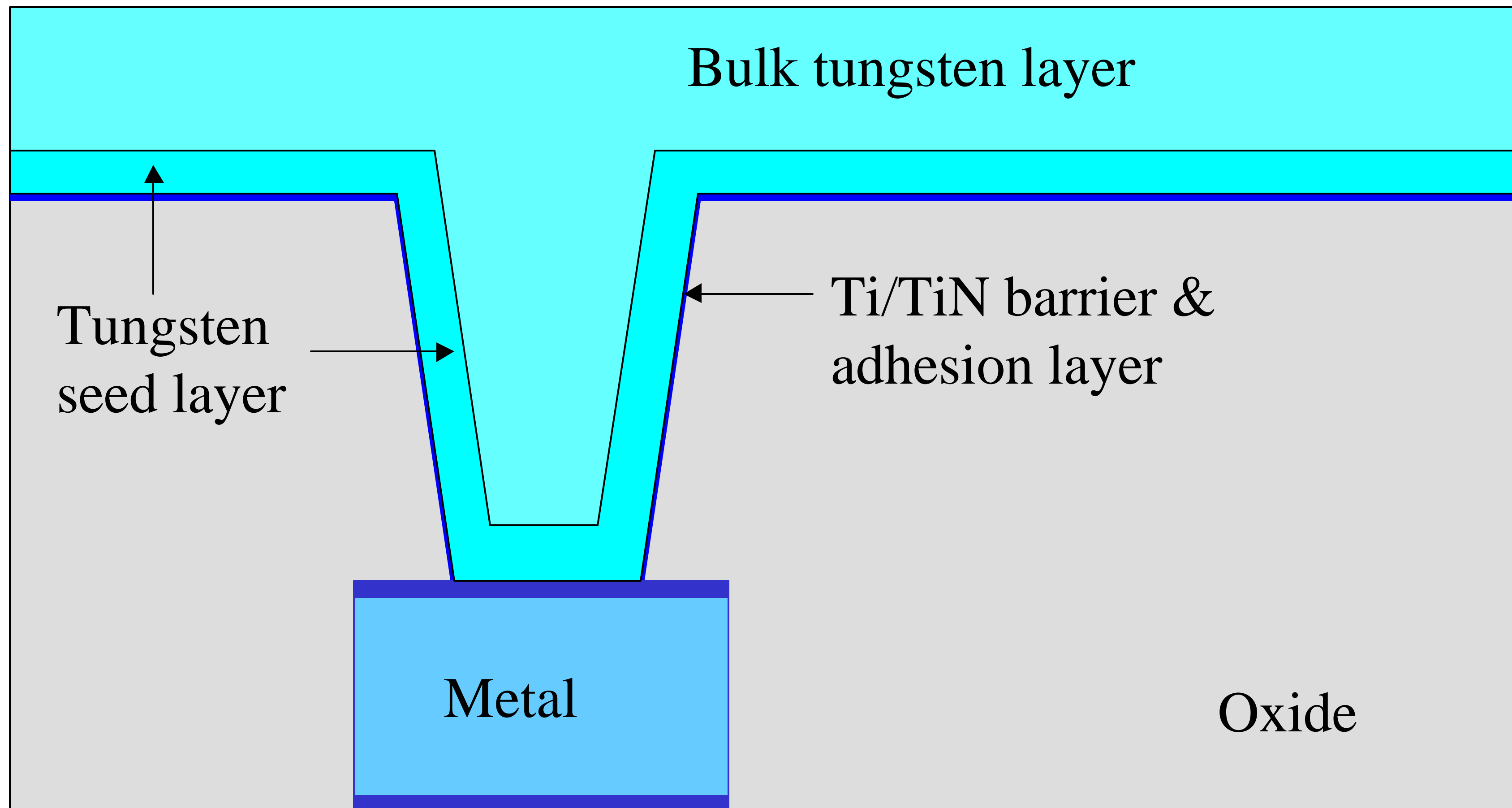
$$WF_6 + 3\ H_2 \rightarrow W\ (s) + 6\ HF$$

WF_6 reaction with moisture



$$WF_6 + 3\ H_2O \rightarrow WO_3 + 6\ HF$$

Tungsten Seed and Bulk Layers



Tungsten Silicide

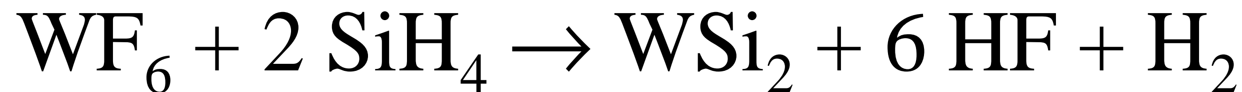
- CVD and RTP
- WF_6 and SiH_4 as CVD source gases
- Anneal after gate etch
- Less popular than TiS_2 due to higher resistivity

Tungsten Silicide

- Sate and local interconnection applications
- Silicon sources: SiH_4 and SiH_2Cl_2 (DCS)
- Tungsten precursor is WF_6
- SiH_4/WF_6: lower temperature, ~ 400 °C,
- DCS/WF_6: higher temperature, ~ 575 °C

Tungsten Silicide: CVD

300 to 400 °C



- Wider process window, more matured process

500 to 600 °C

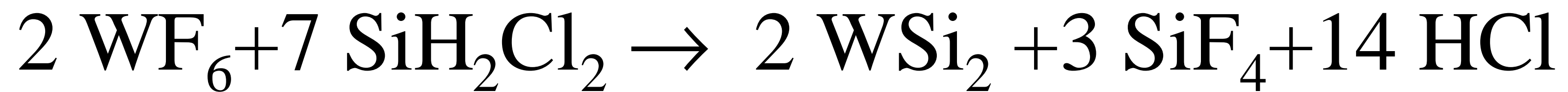
- Better step coverage
- Less fluorine integration

Silane-Based WSi_x

$$WF_6 + 2\ SiH_4 \rightarrow WSi_2(s) + 6\ HF + H_2$$

- Very similar to the nucleation step of the tungsten CVD process.
- Different flow rate ratio of SiH_4/WF_6
  - lower than 3:1, tungsten deposition
  - larger than 10:1 tungsten silicide deposition

DCS-Based WSi_x

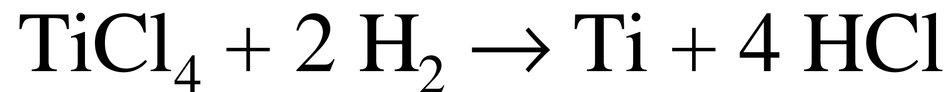


$$2\,WF_6 + 7\,SiH_2Cl_2 \rightarrow 2\,WSi_2 + 3\,SiF_4 + 14\,HCl$$

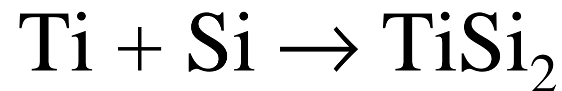
- Requires higher deposition temperature,
- Higher deposition rate
- Better step coverage
- Lower fluorine concentration
- Less tensile stress
  - less film peeling and cracking

Titanium CVD

- High temperature (~ 600 °C)
- CVD Ti can react with Si to form $TiSi_2$ simultaneously during the Ti deposition



$$TiCl_4 + 2\ H_2 \rightarrow Ti + 4\ HCl$$

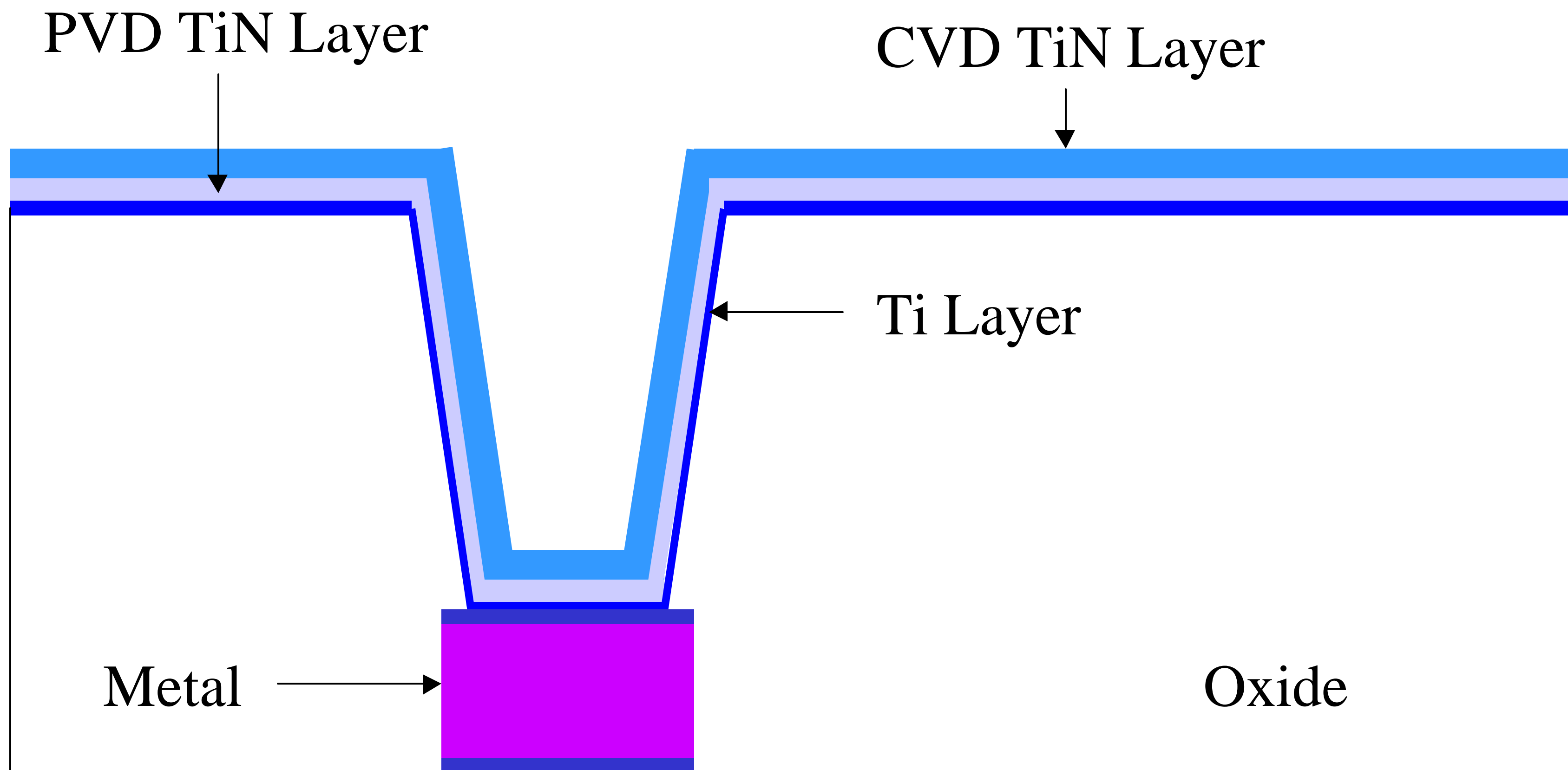


$$Ti + Si \rightarrow TiSi_2$$

Titanium Nitride CVD

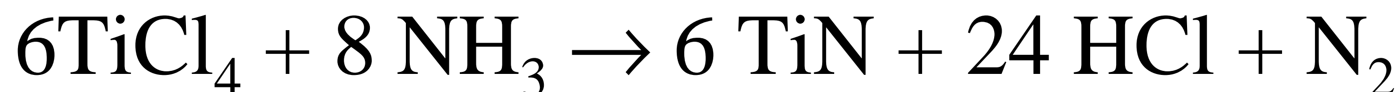
- Barrier/glue layer for the tungsten plug
- Better sidewall step coverage
- A thin layer of (~200 Å) usually is applied for the contact/via holes after PVD Ti and TiN deposition

CVD PVD and CVD TiN Layers



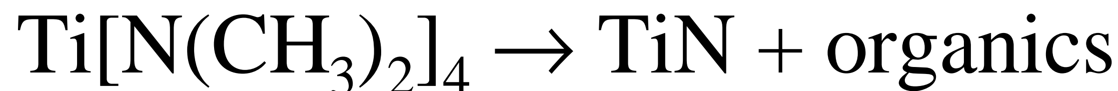
CVD TiN

- Inorganic chemistry: $TiCl_4$ and NH_3 at 400 to 700 °C:



$$6TiCl_4 + 8\ NH_3 \rightarrow 6\ TiN + 24\ HCl + N_2$$

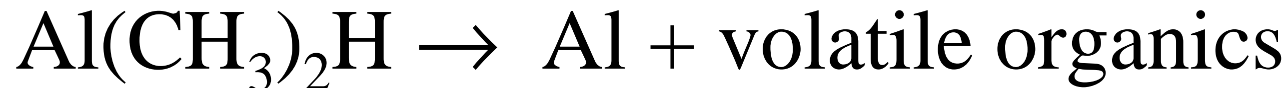
- MOCVD at 350 °C and 300 mTorr:



$$Ti[N(CH_3)_2]_4 \rightarrow TiN + \text{organics}$$

CVD Aluminum

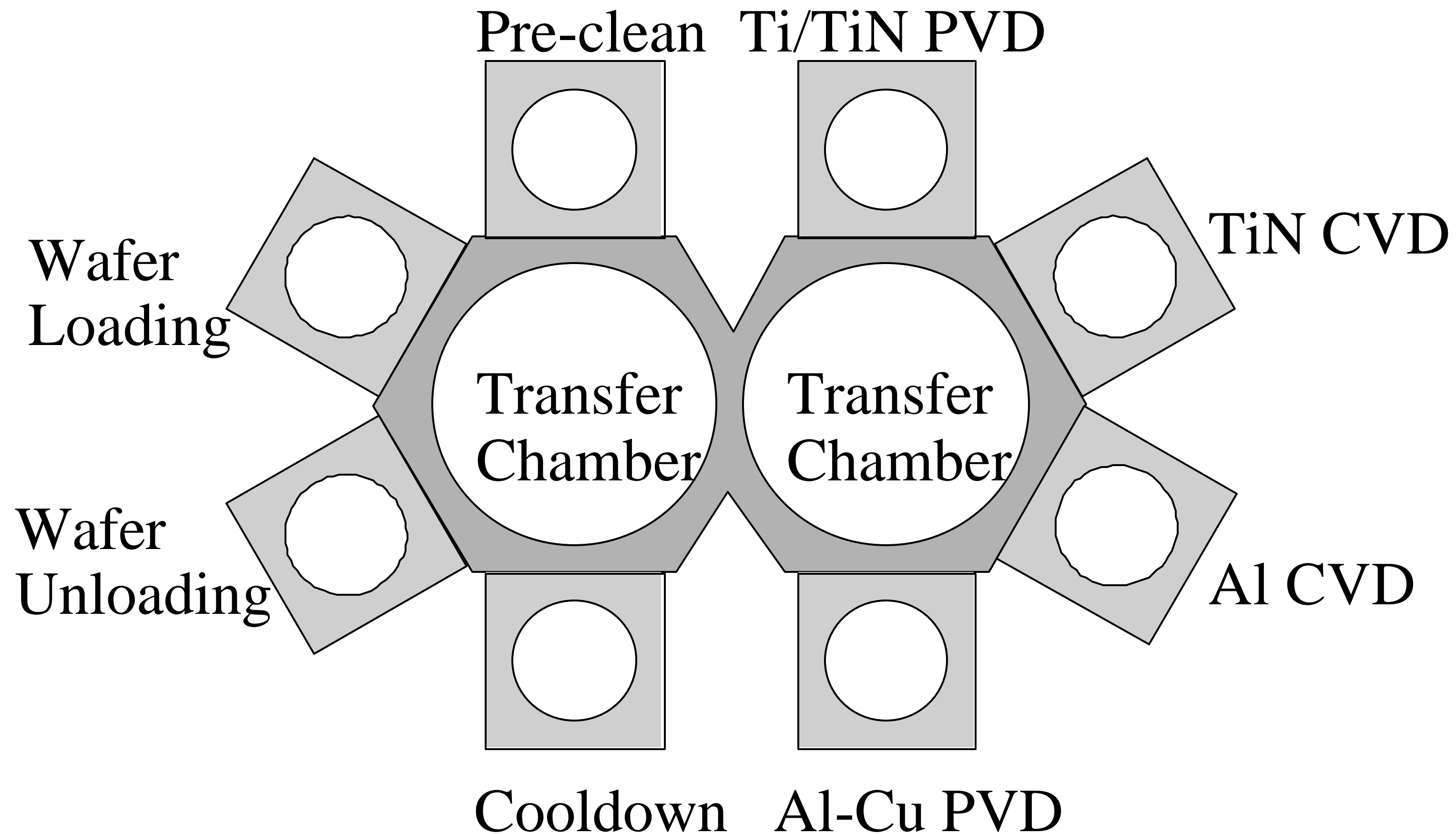
- R&D to replace tungsten plug
- Dimethylaluminum hydride (DMAH), $Al(CH_3)_2H$
- At about 350 °C, DMAH dissociates and deposits aluminum



$$Al(CH_3)_2H \rightarrow Al + \text{volatile organics}$$

- Difficult to incorporate ~1% Cu needed for electromigration resistance

Cluster Tool, Aluminum CVD/PVD



Aluminum CVD/PVD

- Ti/TiN barrier/glue layer deposition
- Al CVD via fill, Al alloy PVD, TiN PVD
  - No need for W and W etch back

- Not a matured technology
- Hard to compete with copper metallization

Physical Vapor Deposition

PVD

- Vaporizing solid materials
- Heating or sputtering
- Condensing vapor on the substrate surface
- Very important part of metallization

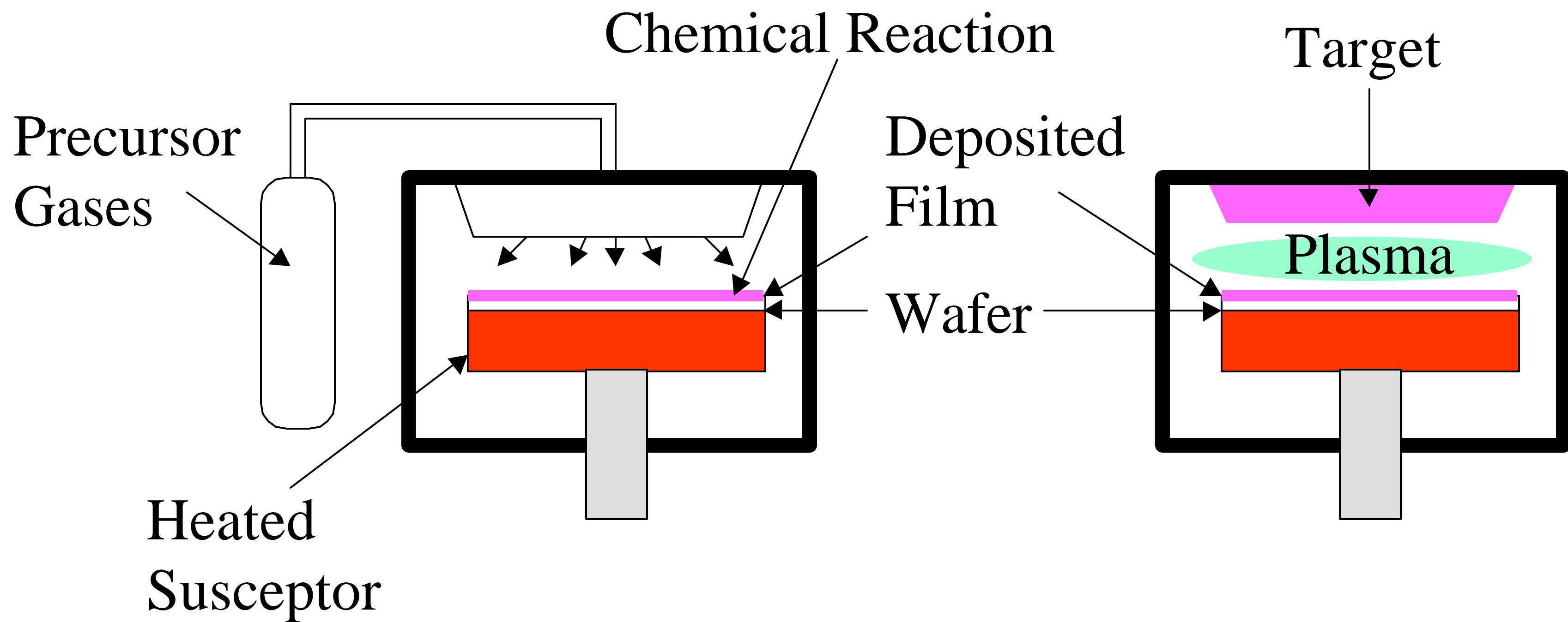
PVD vs. CVD

• PVD	Start with P
• CVD	Start with C

PVD vs. CVD: Sources

• PVD	Solid materials
• CVD	Gases or vapors

CVD vs. PVD



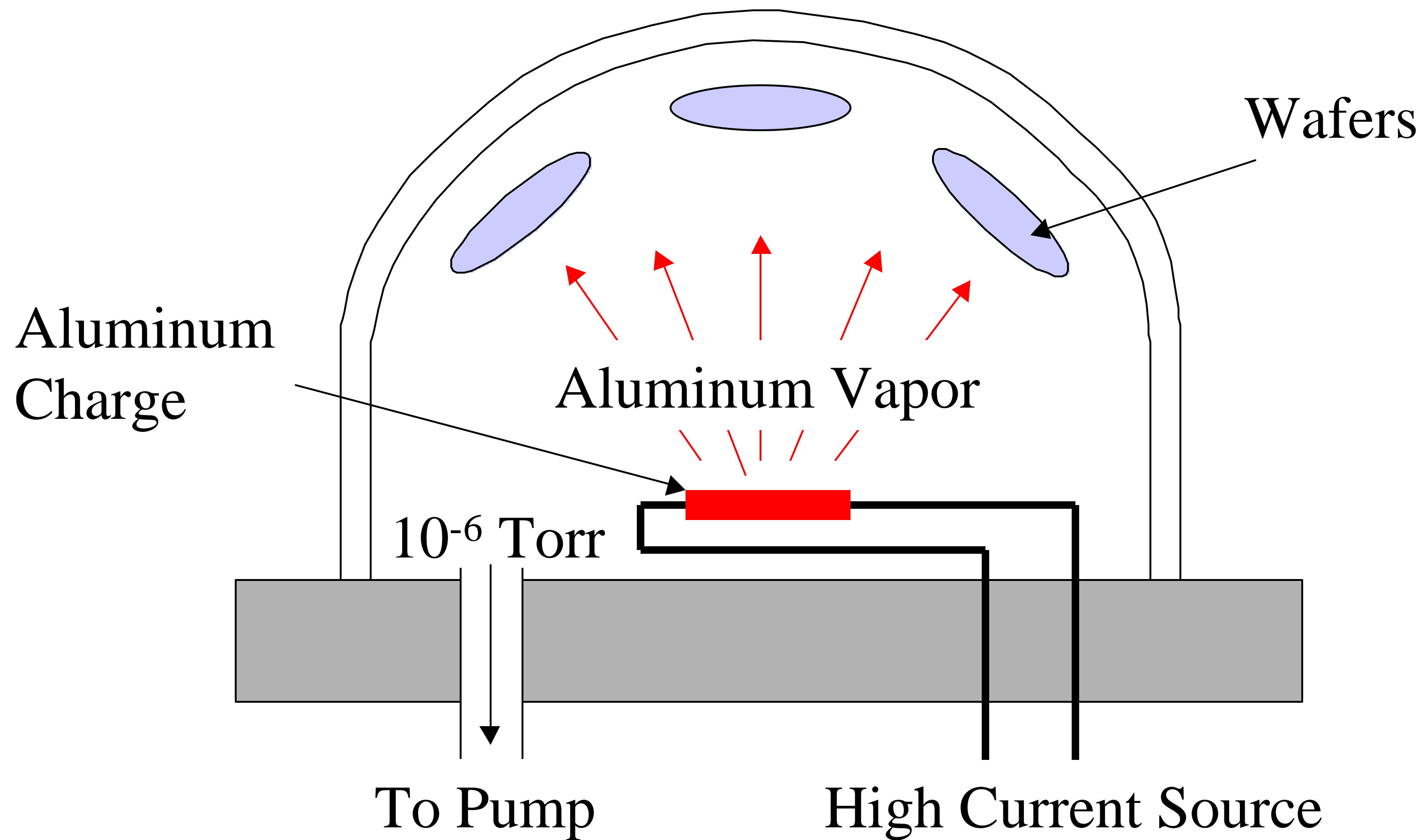
PVD Methods

- Evaporation
- Sputtering

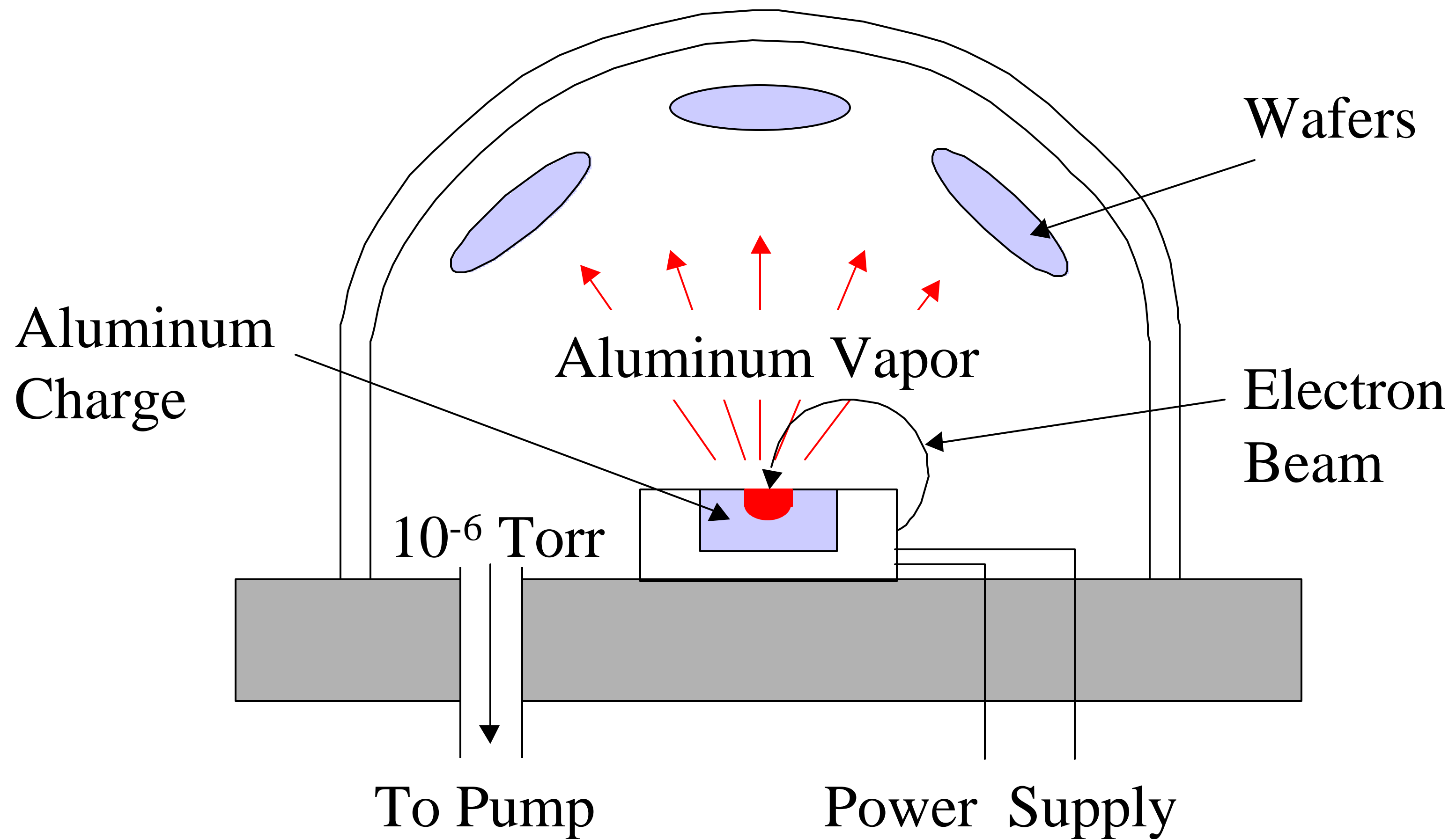
PVD Methods: Evaporation

- Filaments
- Flash hot plate
- Electron beam

Thermal Evaporator



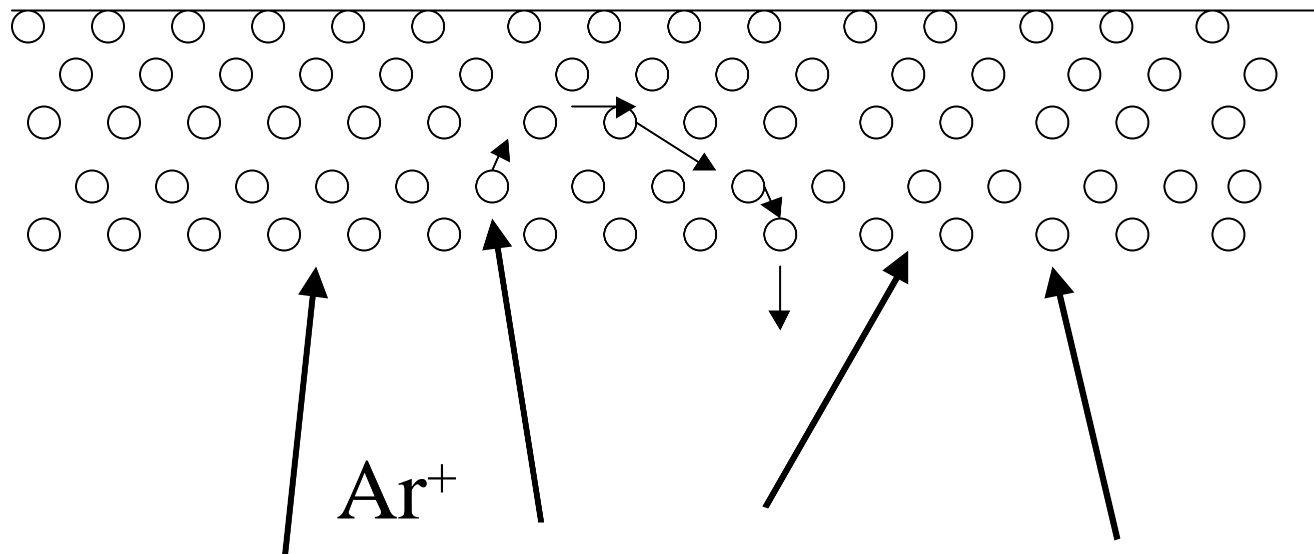
Electron Beam Evaporator



PVD Methods: Sputtering

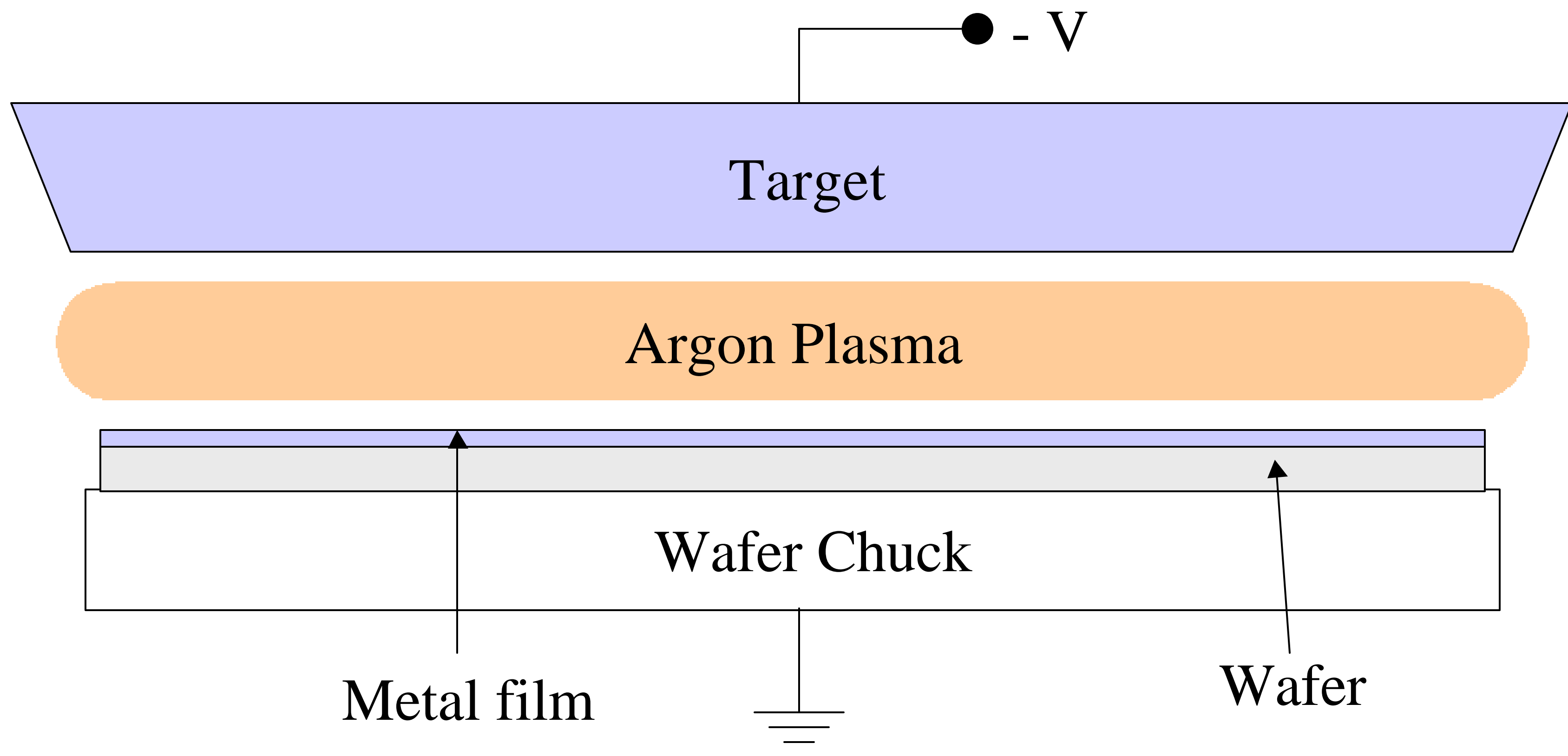
- DC Diode
- RF Diode
- **Magnetron**

Sputtering

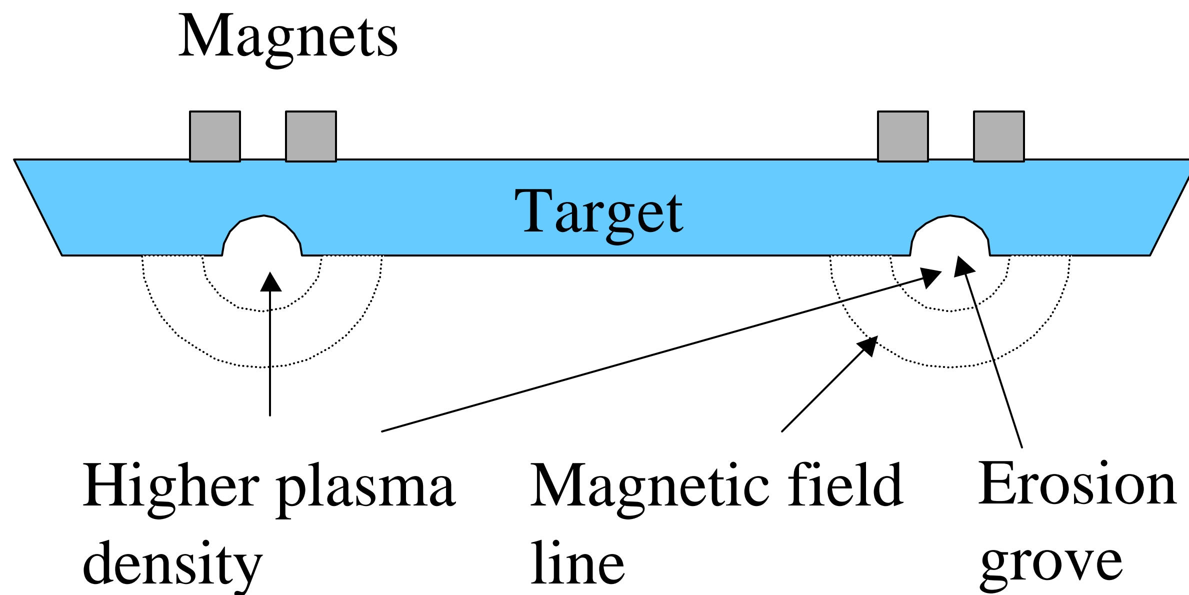


Momentum transfer will dislodge surface atoms off

DC Diode Sputtering



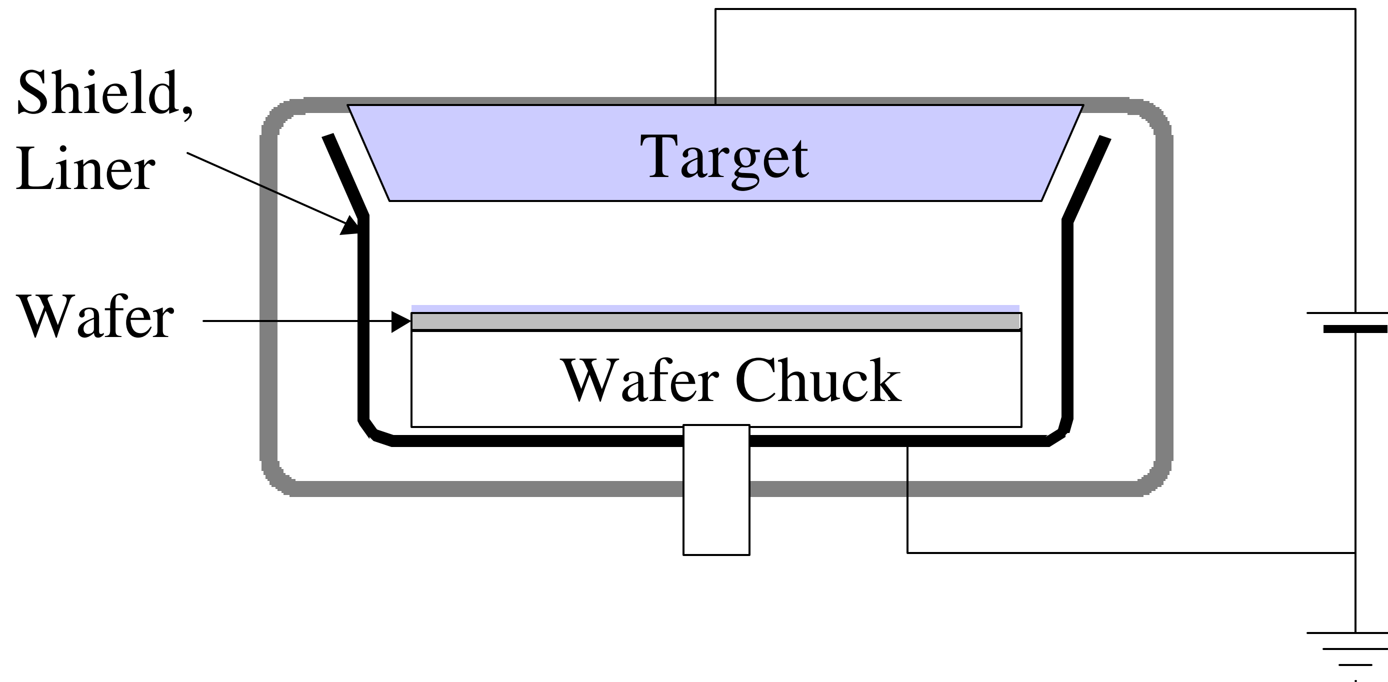
Schematic of Magnetron Sputtering



Magnetron Sputtering

- Most widely used PVD system
- More sputter from grove
- Better uniformity cross wafer

PVD Chamber with Shield



Applications of Argon

- Sputtering deposition
- Sputtering etch
  - pre-clean to remove native oxide before metal deposition
  - Taper opening for dielectric gap fill
- Patterned etch
  - dielectric to enhance bombardment and damaging effect

Properties of Argon

- Inert
- Relatively heavy
- Abundance
  - about 1% in atmosphere
  - low cost

Some Facts About Argon

Name	Argon
Symbol	Ar
Atomic number	18
Atomic weight	39.948
Discoverer	Sir William Ramsay, Lord Rayleigh
Discovered at	Scotland
Discovery date	1894
Origin of name	From the Greek word "argos" meaning "inactive"
Molar volume	$22.56\ cm^3$
Speed of sound	319 m /sec
Refractive index	1.000281
Electrical resistivity	N/A
Melting point Boiling point	-189.2 °C -185.7 °C
Thermal conductivity	$0.01772\ W\ m^{-1}\ K^{-1}$

Sputtering vs. Evaporator

Sputtering

- Purer film
- Better uniformity
- Single wafer, better process control
- Larger size wafer

Evaporator

- More impurities
- Batch process
- Cheaper tool

PVD Vacuum Requirement

- Residue gases on the vacuum chamber wall
  - H_2O, …
- Water can react with Al to form Al_2O_3
- Affects conductivity of interconnections
- Only way to get rid of H_2O: reach ultra high vacuum, 10^{-9} Torr

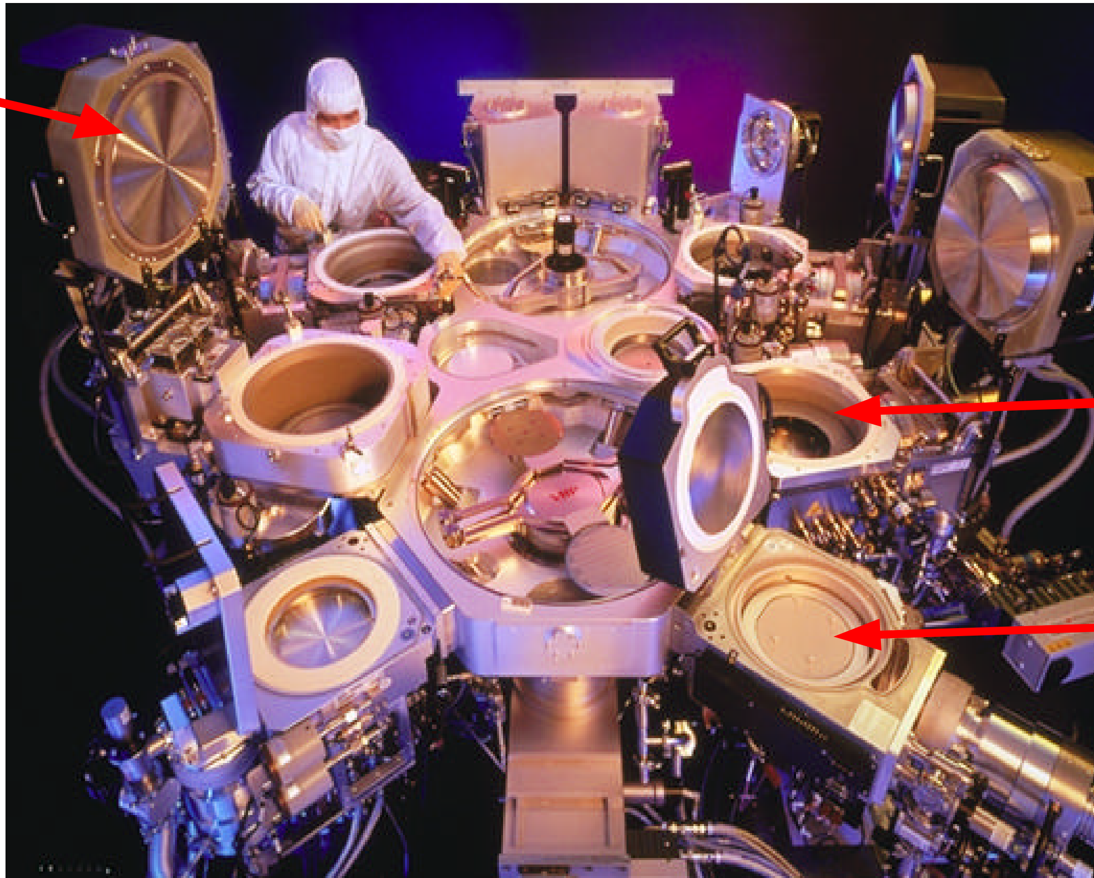
PVD Vacuum Requirement

- Cluster tool
- Staged vacuum
- Loading station: 10^{-6} Torr
- Transfer chamber: 10^{-7} to 10^{-8} Torr
- Deposition chamber: 10^{-9} Torr

PVD Vacuum: Pumps

- Wet pump (oil diffusion pump): atm to 10^{-3} Torr, phasing out from fabs.
- Rough pump: atm to 10^{-5} Torr
- Turbo pump: 10^{-2} to 10^{-7} Torr
- Cryo pump: to 10^{-10} Torr
- Ion pump: to 10^{-11} Torr

Endura® PVD System



Contact/Via Process

- Degas
- Pre-clean
- Ti PVD
- TiN PVD
- TiN CVD
- N_2-H_2 plasma treatment
- W CVD

Aluminum Interconnection Process

- Degas
- Pre-clean
- Ti PVD
- Al-Cu PVD
- TiN PVD

Copper Interconnection Process

- Degas
- Pre-clean
- Ta PVD
- Cu seed PVD

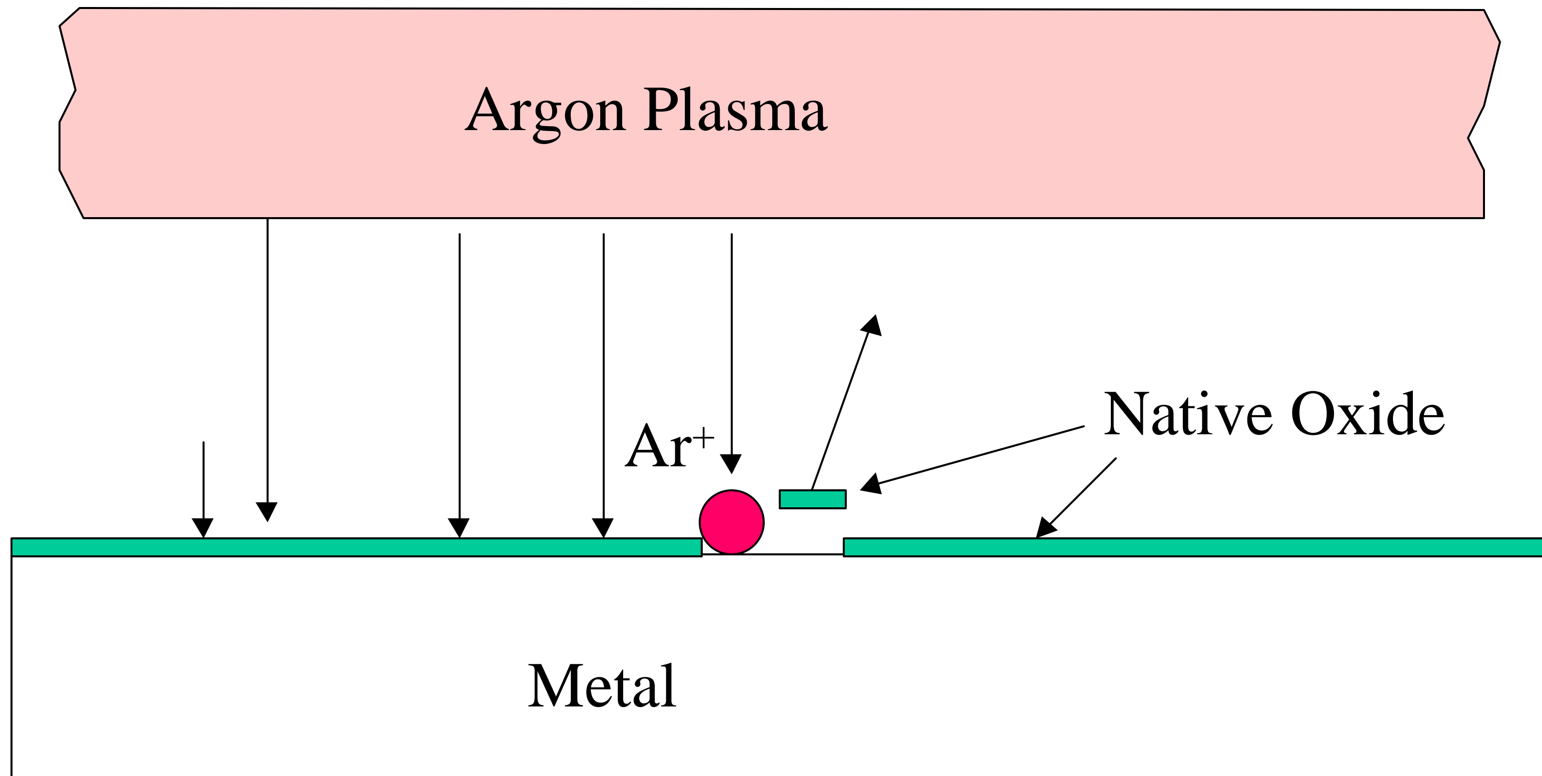
Degas

- Heat wafer to drive away gases and moisture on wafer surface
- Outgassing can cause contamination and high resistivity of deposited metal film

Pre-clean

- Remove the native oxide
- Reduce the contact resistance
- Sputtering with argon ions
- RF plasma

Pre-clean Process



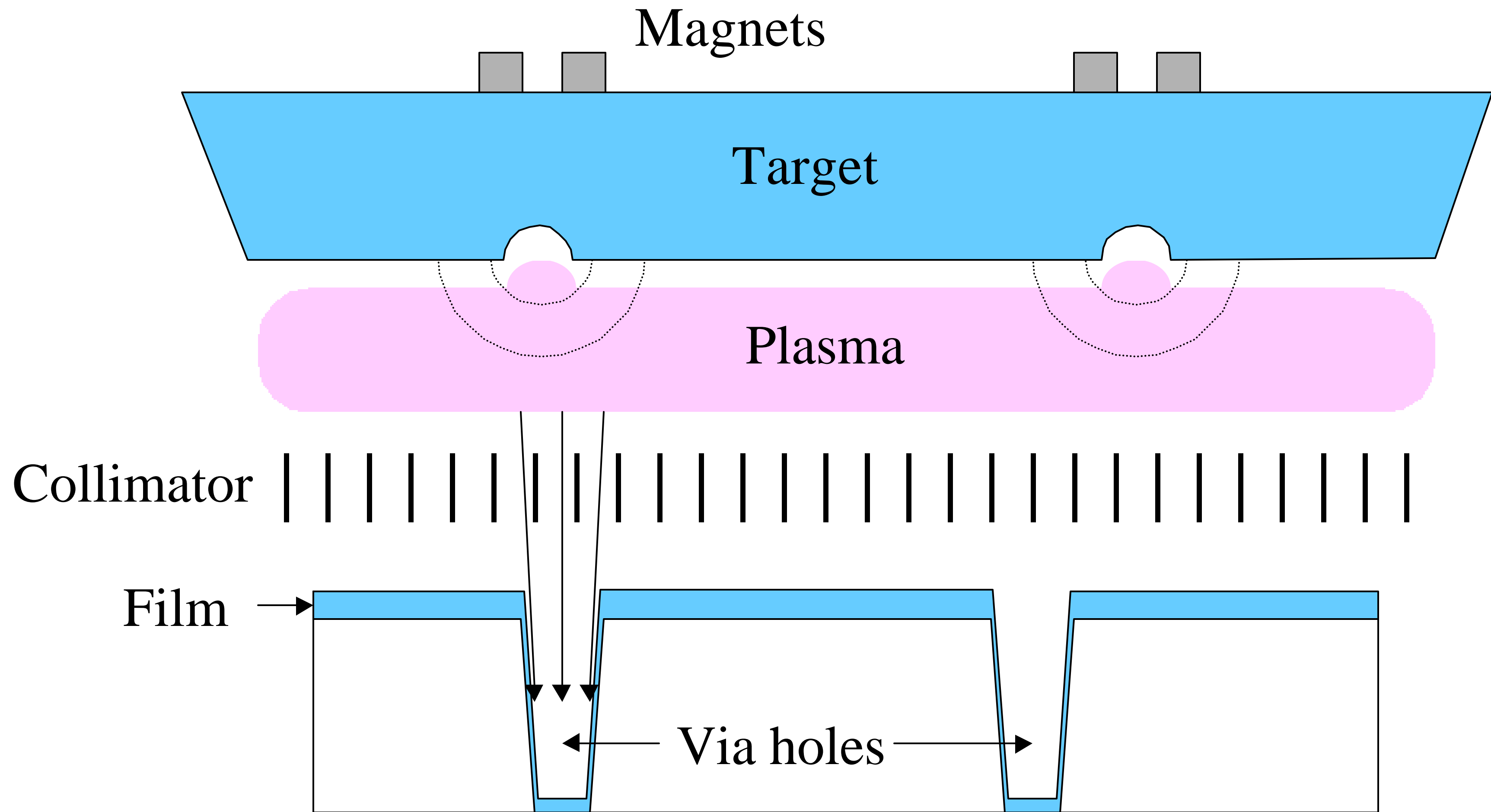
Titanium PVD

- Reduce contact resistance
- Larger grain size with low resistivity
- Wafer normally is heated to about 350 °C during the deposition process to
- Improve the surface mobility
- Improve step coverage

Collimated Sputtering

- Used for Ti and TiN deposition
- Collimator allows metal atoms or molecules to move mainly in vertical direction
- Reach the bottom of narrow contact/via holes
- Improves bottom step coverage

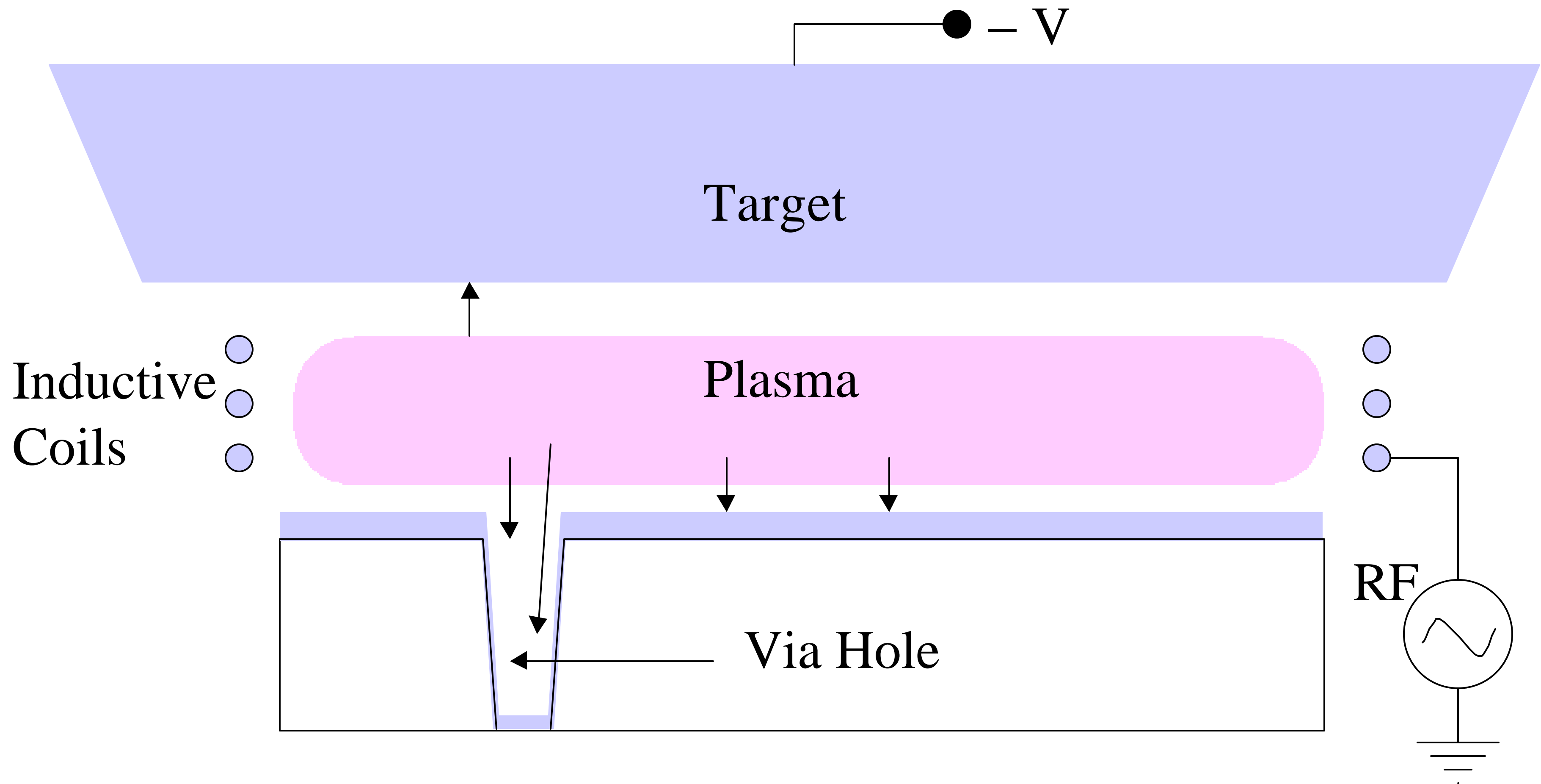
Collimated Sputtering



Metal Plasma System

- Ti, TiN, Ta, and TaN deposition
- Ionize metal atoms through inductive coupling of RF power in the RF coil
- Positive metal ions impact with the negatively charged wafer surface vertically
- Improving bottom step coverage
- Reduce contact resistance

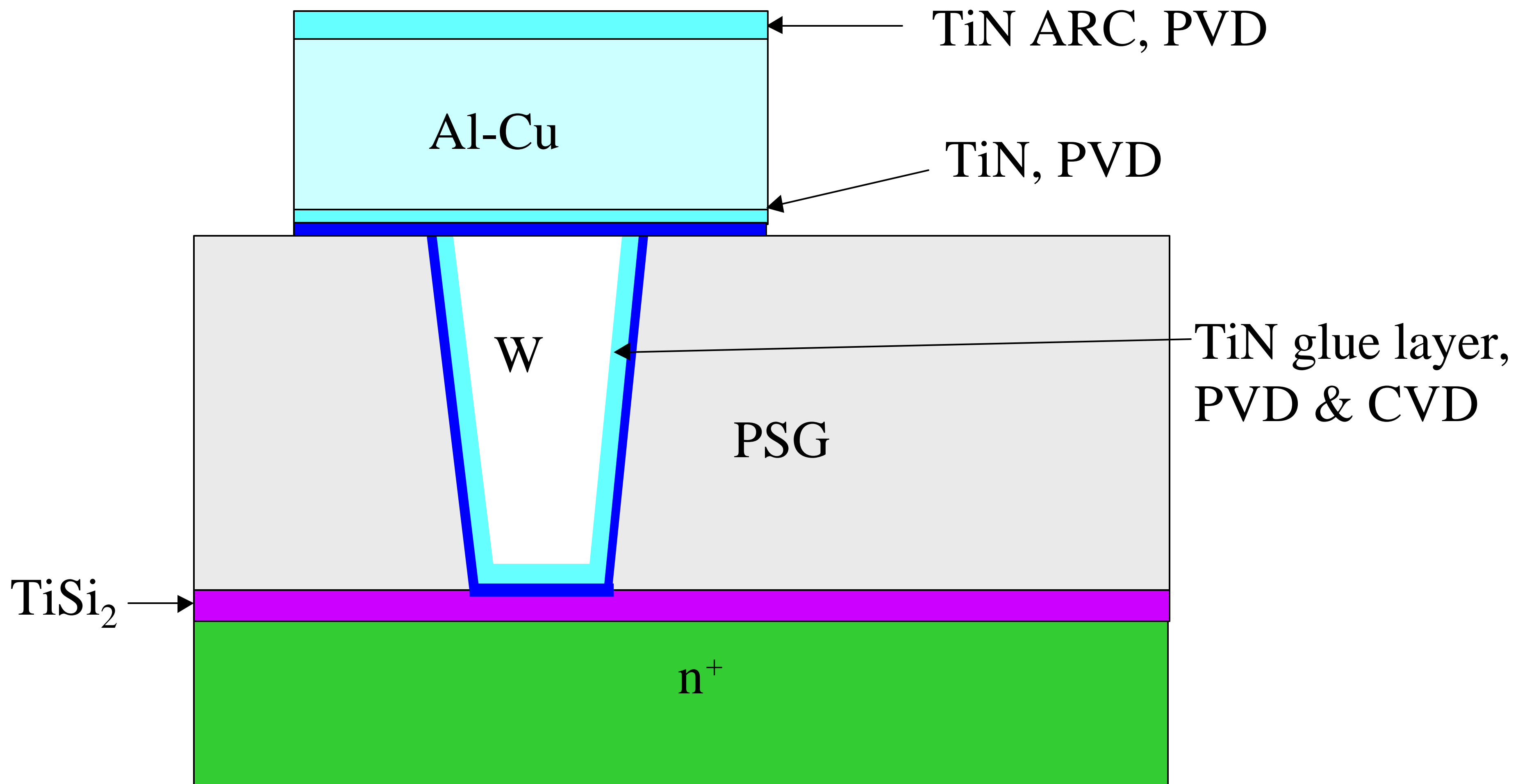
Ionized Metal Plasma



Titanium Nitride PVD

- Reactive sputtering process
- Ar and N_2
- N_2 molecules dissociate in plasma
- Free nitrogen radicals react with Ti to form a thin layer of TiN on target surface.
- Argon ions sputter the TiN from the target surface and deposit it on the wafer surface

Three Applications of TiN



Al-Cu PVD

- Ultra high vacuum to remove moisture and achieve low film resistivity.
- Cluster tool with staged vacuum
- dry pumps, turbo pumps and cryopump
- A cryopump can help a PVD chamber to reach up to 10^{-10} Torr base pressure by freezing the residue gases in a frozen trap

Al-Cu PVD

- Standard process and hot aluminum process
- Standard process: Al-Cu over tungsten plug after Ti and TiN deposition
- Normally deposit at ~ 200 °C
- Smaller grain size, easier to etch
- Metal annealing to form larger grain size
  - lower resistivity
  - high EMR

Al-Cu PVD

- Hot aluminum process
- fill contact and via holes, reduces contact resistance
- Several process steps:
  - Ti deposition
  - Al-Cu seed layer is deposited at low <200°C
  - Bulk Al-Cu layer is deposited at higher temperatures (450°C to 500°C)

Copper Metallization

Copper

- Better conductor than aluminum
- Higher speed and less power consumption
- Higher electromigration resistance
- *Diffusing freely in silicon and silicon dioxide, causing heavy metal contamination, need diffusion barrier layer*
- *Hard to dry etch, no simple gaseous chemical compounds*

Copper

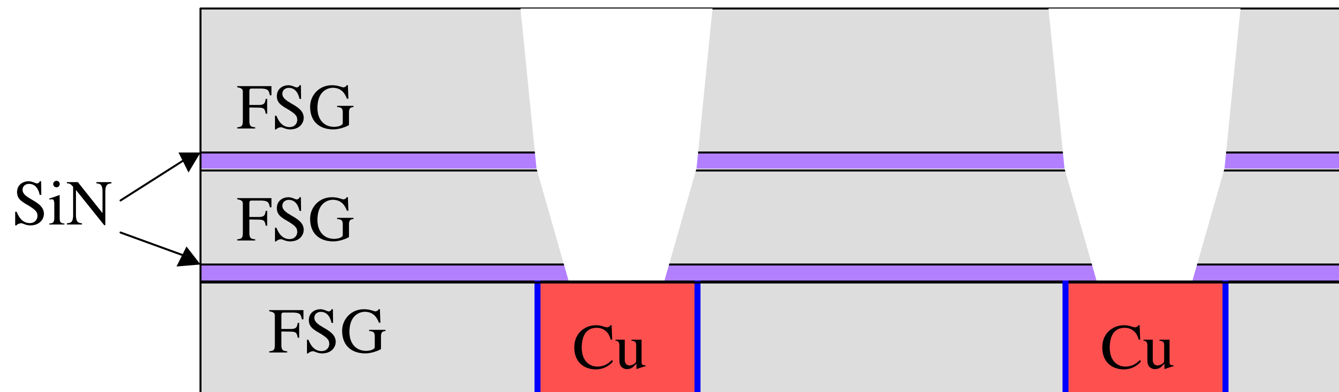
- Damascene process with CMP
- Ta and/or TaN as barrier layer
- Start using in IC fabrication

Copper

- Pre-deposition clean
- PVD barrier layer (Ta or TaN, or both)
- PVD copper seed layer
- Electrochemical plating bulk copper layer

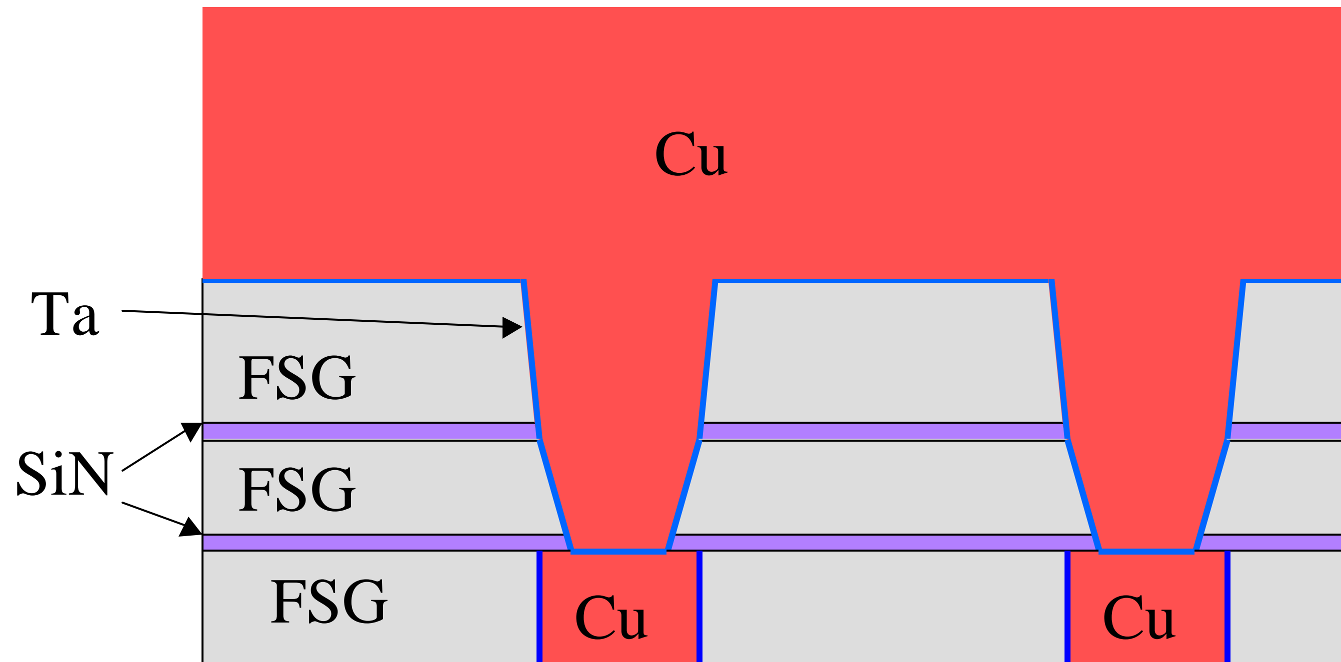
- Thermal anneal to improve conductivity

Etch trenches and via holes

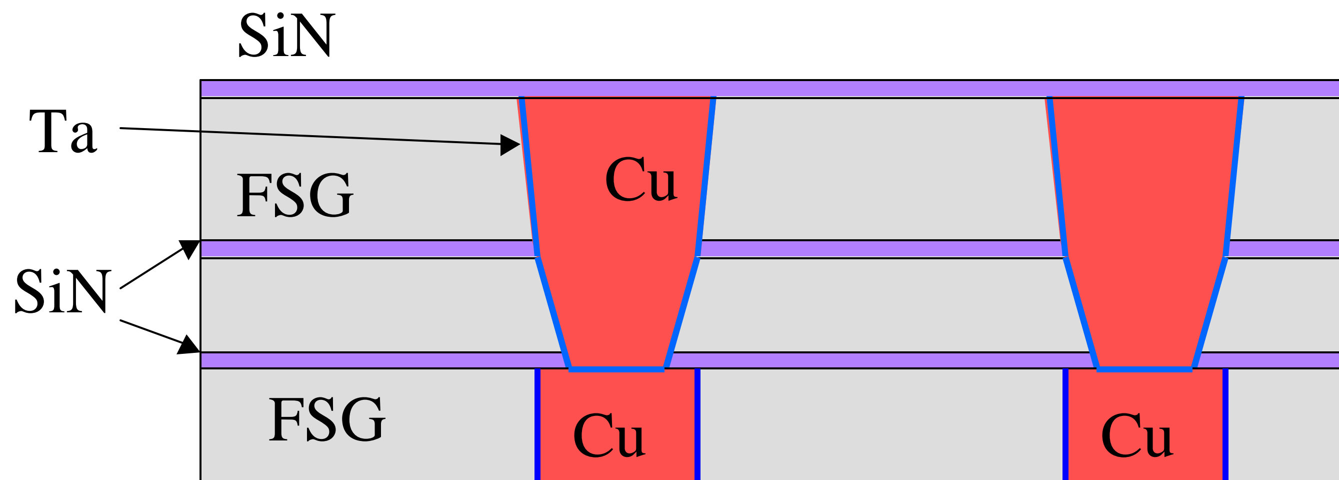


Tantalum Barrier Layer and Copper Seed Layer Deposition

Electrochemical Plating Copper

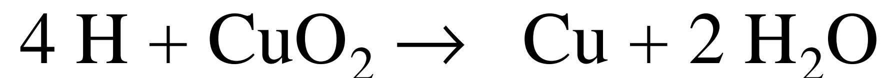


CMP Copper and Tantalum, CVD Nitride



Pre-clean

- Argon sputtering pre-deposition clean
  - Commonly used
  - Possible copper contamination due to sputtering
- Chemical pre-clean
  - H_2 and He plasma
  - H radicals react with CuO_2



$$4\,H + CuO_2 \rightarrow Cu + 2\,H_2O$$

Barrier Layer

- Copper diffusion into silicon can cause device damaging
- Need barrier layer
- Ti, TiN, Ta, TaN, W, WN,
- Few hundred Å Ta is commonly used
- Combination of Ta and TaN in near future

Copper Seed Layer

- PVD copper layer (500 to 2000 Å)
- Nucleation sites for bulk copper grain and film formation.
- Without seed layer
  - No deposition
  - or deposition with very poor quality and uniformity

Copper Seed Layer

- Copper vapor can be easily ionized
- Low pressure, long MFP
- Copper ions throw into via and trench
  - good step coverage and smooth film surface
- Very narrow via hole, PVD copper will be in trouble due to its poor step coverage
- CVD copper process may be needed

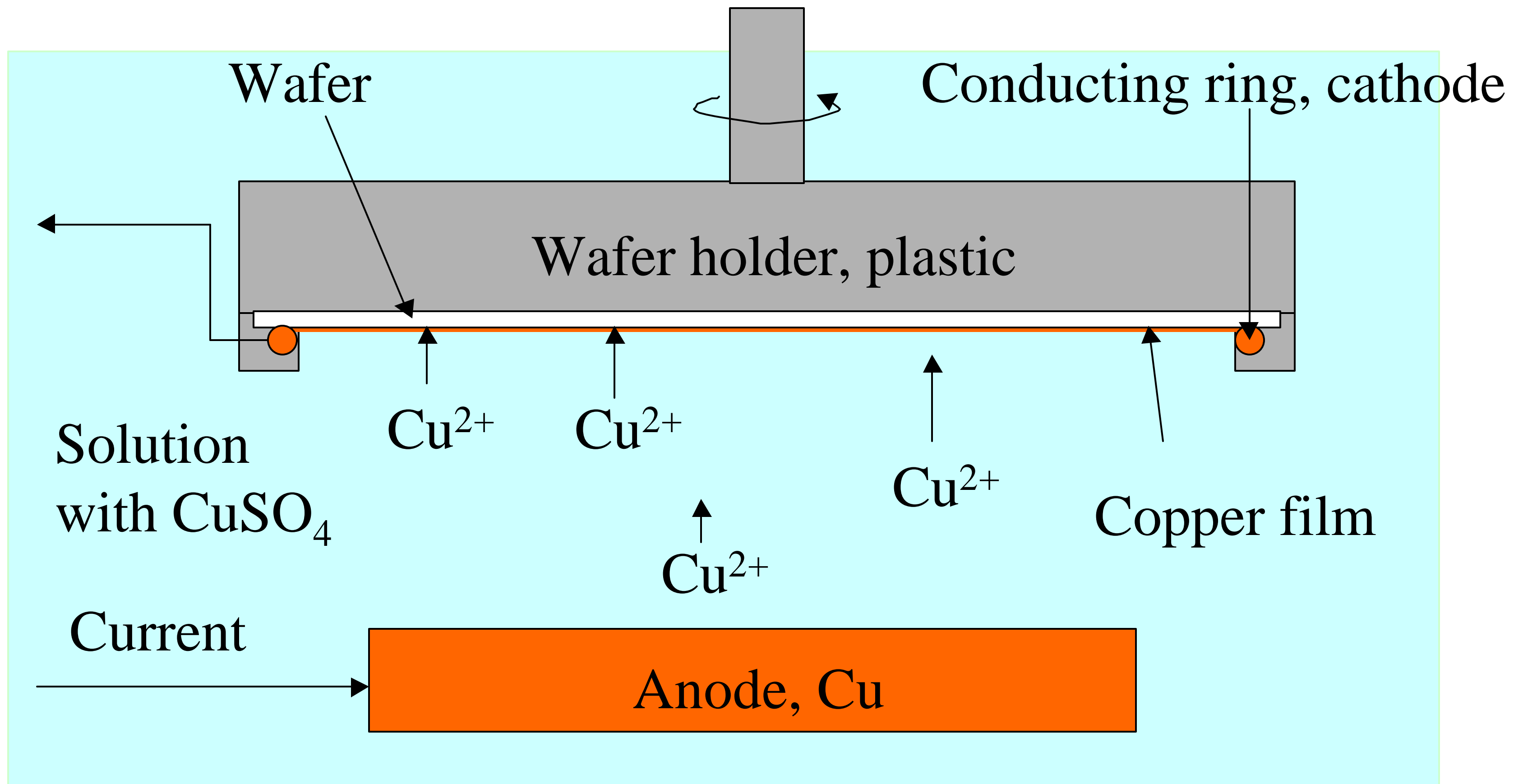
Electrochemical Plating (ECP)

- Old technology
- Still used in hardware, glass, auto, and electronics industries.
- Recently introduced in IC industry
- Bulk copper deposition
- Low-temperature process
- Compatible with low-κ polymeric dielectric

Electrochemical Plating (ECP)

- $CuSO_4$ solution
- Copper anode
- Wafer with copper seed layer as cathode
- Fixed electric current
- Cu^{2+} ion diffuse and deposit on wafer

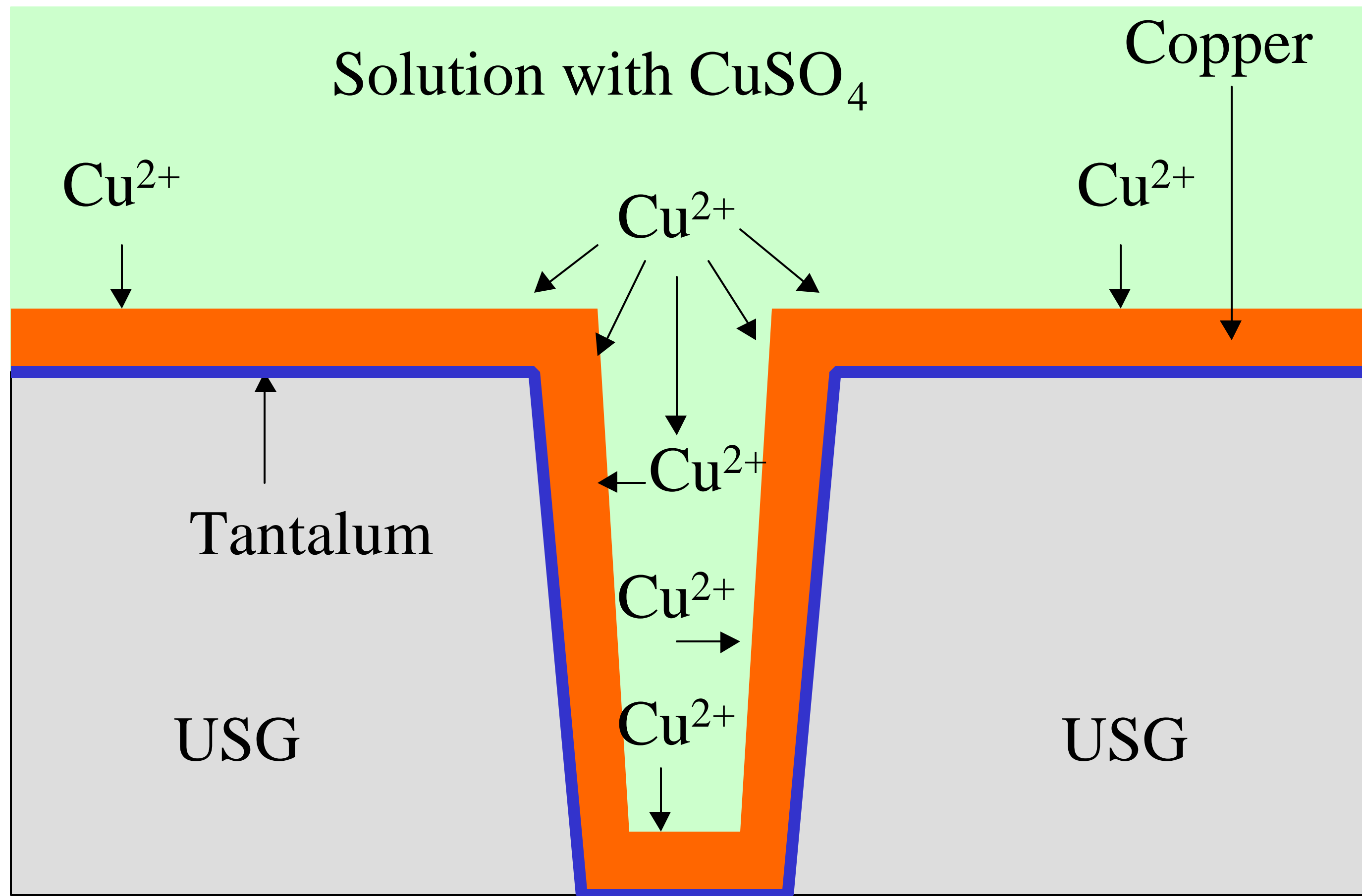
Copper Electrochemical Plating



Via and Trench Fill

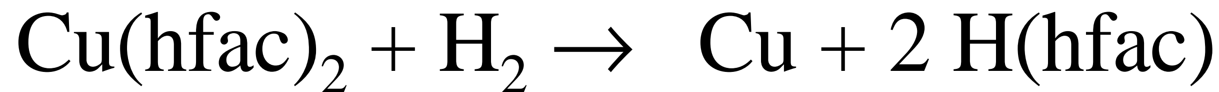
- To achieve better gap-fill, pulse current with large forward amperage and small reversed amperage is used.
- Reversed current removes copper, which reduces overhang of the gap.
- Similar to dep/etch/dep process
- Additives reduces deposition on the corner to improve the via fill capability

Electrochemical Plating Via Fill



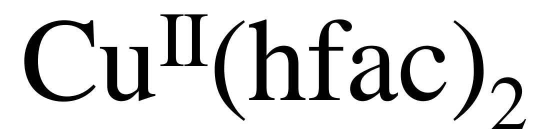
Copper CVD

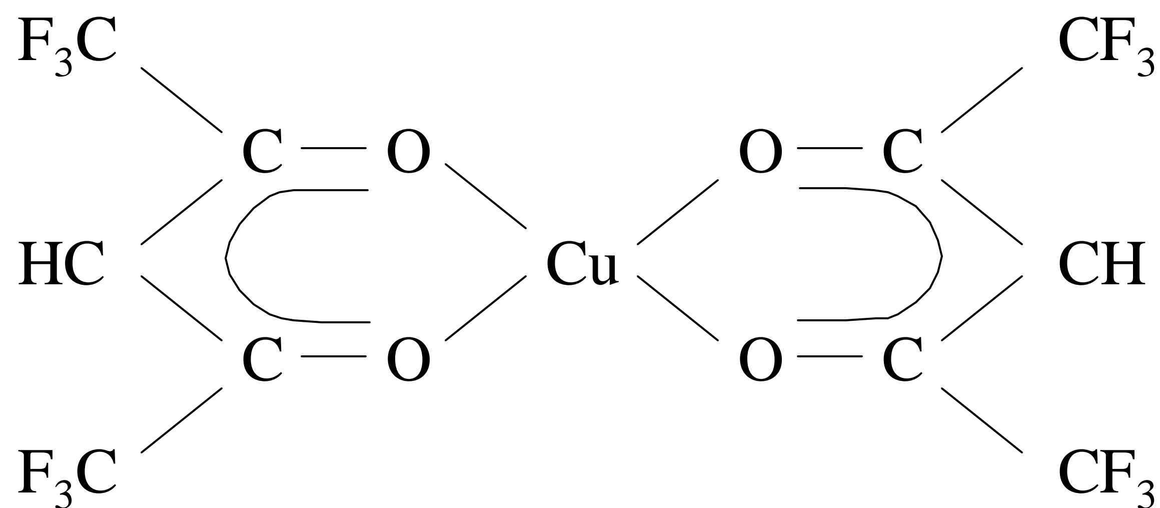
- bis-hexafluoroacetyl-acetonate copper, or $Cu(hfac)_2$



$$Cu(hfac)_2 + H_2 \rightarrow Cu + 2\ H(hfac)$$

- 350 to 450 °C
- Too high for polymeric low-κ dielectric


Cu(II)(hfac)2


F3C
C
O
O
C
CF3
HC
Cu
CH
C
O
O
C
F3C
CF3

Copper CVD

- Organiometallic compound
- Cu(hfac)(tmvs): $C_{10}H_{13}CuF_6O_2Si$

$$2\ Cu(hfac)(tmvs) \rightarrow Cu + Cu(hfac)_2 + 2\ tmvs$$

- Thermal process ~ 175 °C, 1 to 3 Torr
- Excellent step coverage and gap fill capability

Copper CVD

- Cu(hfac)(vtms) process is the the more promising copper CVD process.
- Tough competition from the production-proven copper ECP process
- PVD/CVD copper seed layer deposition

Summary

- Mainly application: interconnection
- CVD (W, TiN, Ti) and PVD (Al-Cu, Ti, TiN)
- Al-Cu alloy is still dominant
- Need UHV for Al-Cu PVD
- W used as plug
- Ti used as welding layer
- TiN: barrier, adhesion and ARC layers
- The future: Cu and Ta/TaN

Chapter 12
Chemical Mechanical Polishing

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www2.austin.cc.tx.us/HongXiao/Book.htm

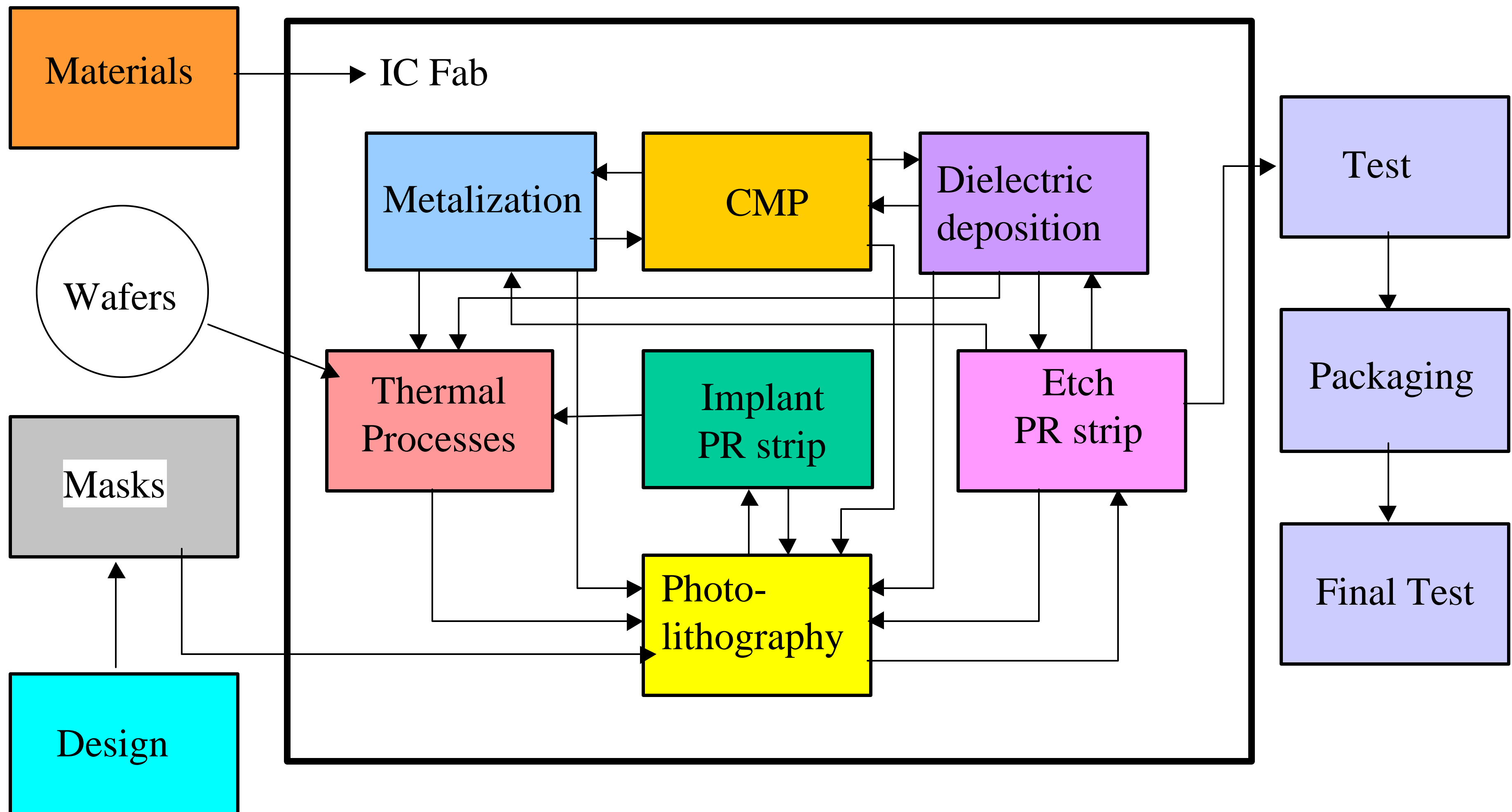
Objectives

- List applications of CMP
- Describe basic structure of a CMP system
- Describe slurries for oxide and metal CMP
- Describe oxide CMP process.
- Describe metal polishing process.
- Explain the post-CMP clean

Overview

- Multi layer metal interconnection
- Planarization of dielectric layers
- Depth of focus require flat surface to achieve high resolution
- The rough dielectric surface can also cause problems in metallization

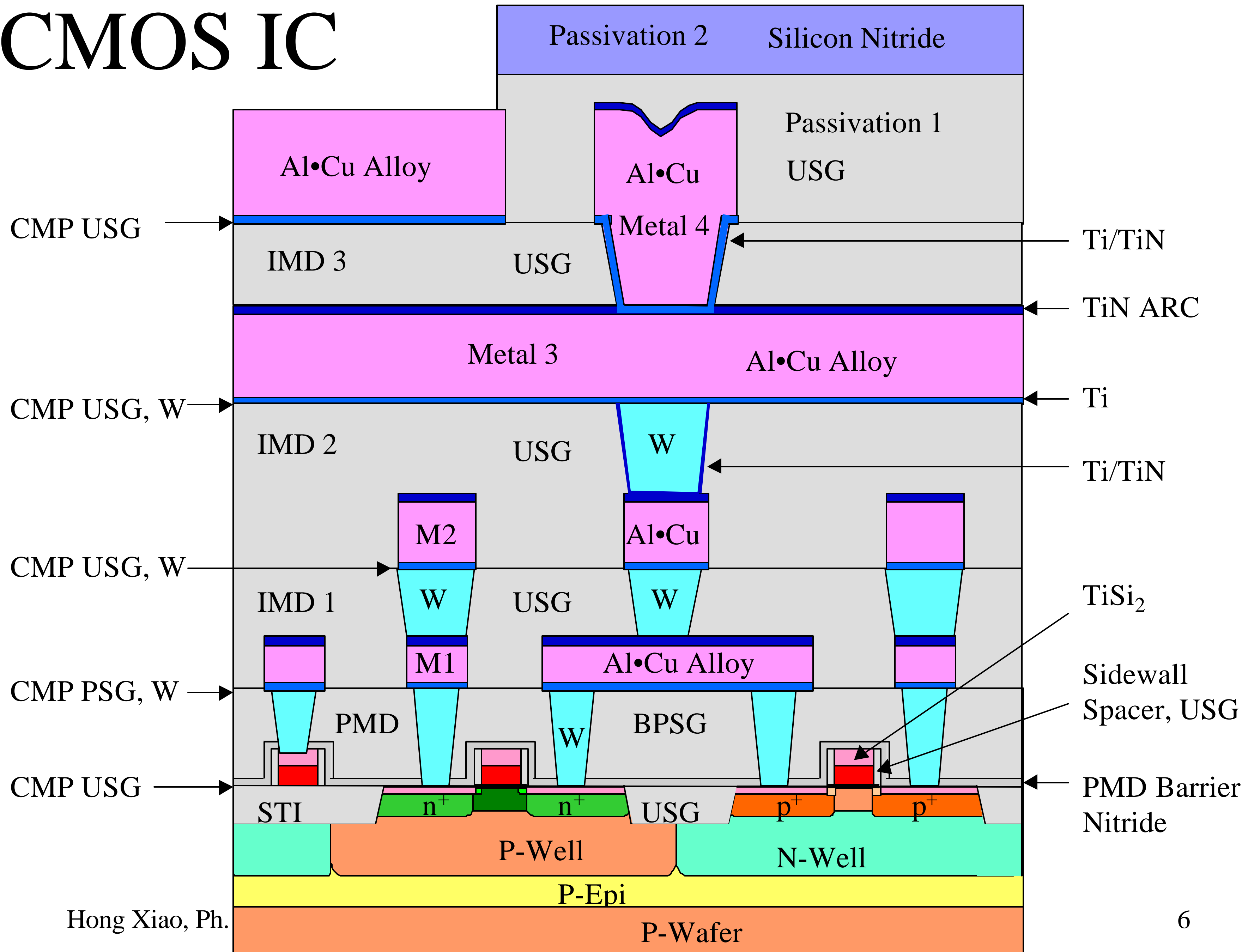
Wafer Process Flow



Tungsten CMP

- Tungsten has been used to form metal plugs
- CVD tungsten fills contact/via holes and covers the whole wafer.
- Need to remove the bulk tungsten film from the surface
- Fluorine based plasma etchback processes
- Tungsten CMP replaced etchback

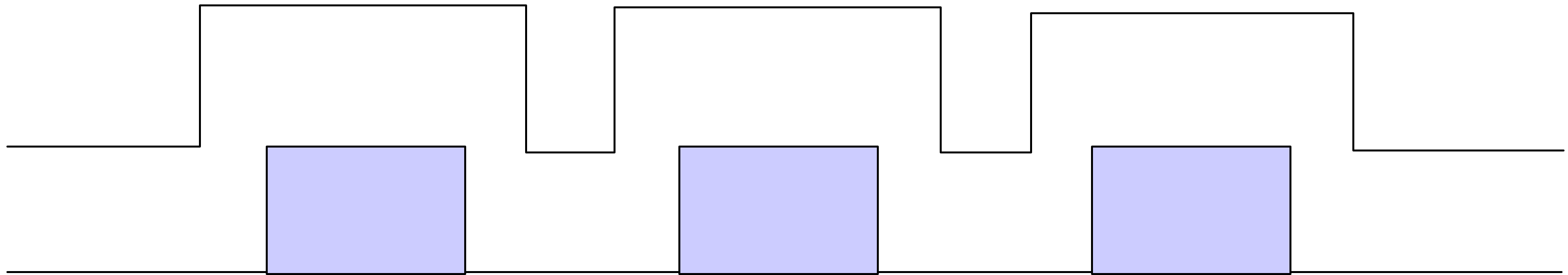
CMOS IC



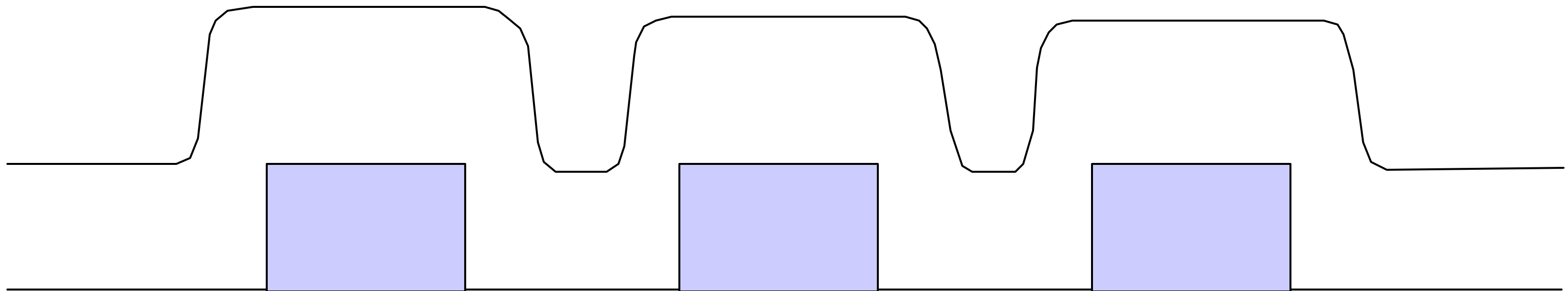
Definition of Planarization

- Planarization is a process that removes the surface topologies, smoothes and flattens the surface
- The degree of planarization indicates the flatness and the smoothness of the surface

Definition of Planarization

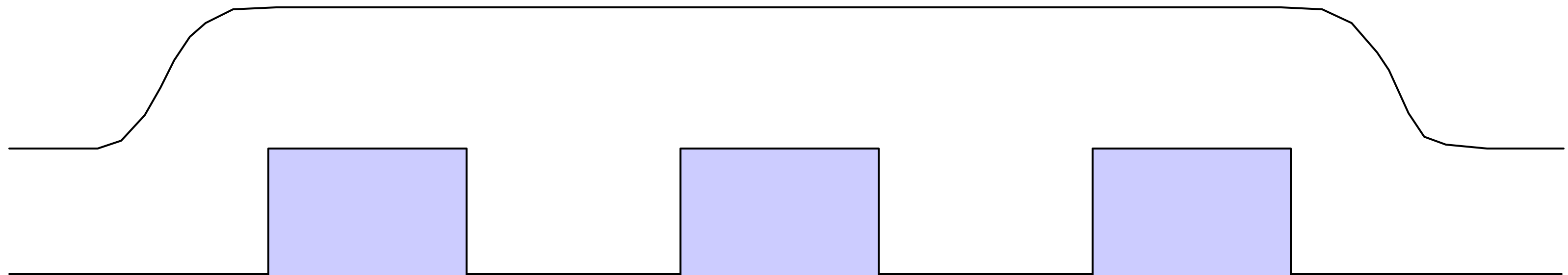


Completely Conformal Film, No Planarization

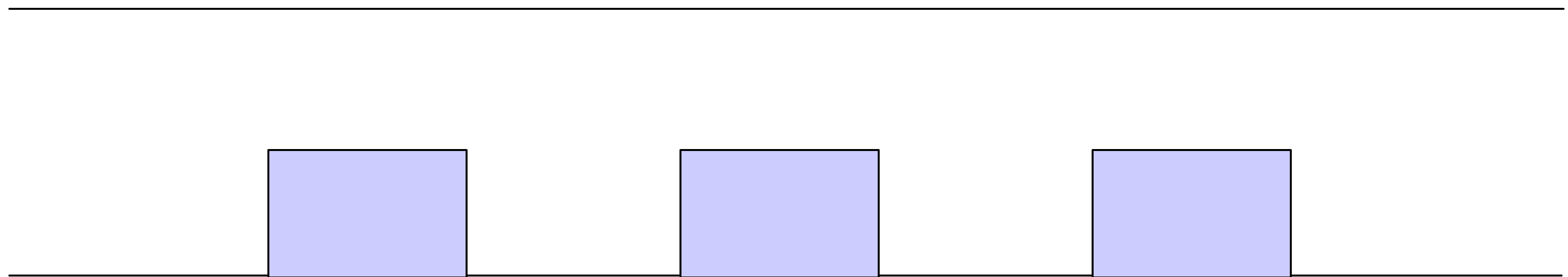


Conformal and Smooth, No Planarization

Definition of Planarization



Partial Planarization

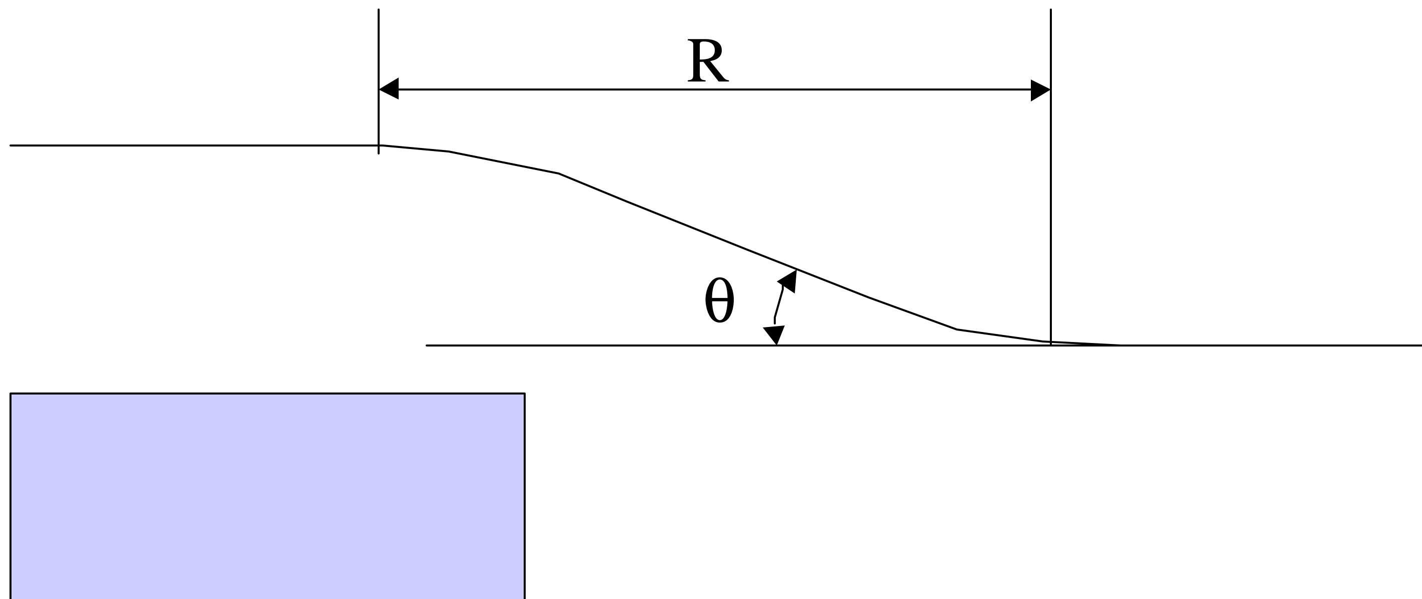


Global Planarization

Degrees of Planarity

Planarity	R(μm)	θ
Surface Smoothing	0.1 to 2.0	> 30
Local Planarization	2.0 to 100	30 to 0.5
Global Planarization	> 100	< 0.5

Definition of Planarity



Planarization

- Smoothing and local planarization can be achieved by thermal flow or etchback
- Global planarization is required for the feature size smaller than 0.35 μm, which can only be achieved by CMP

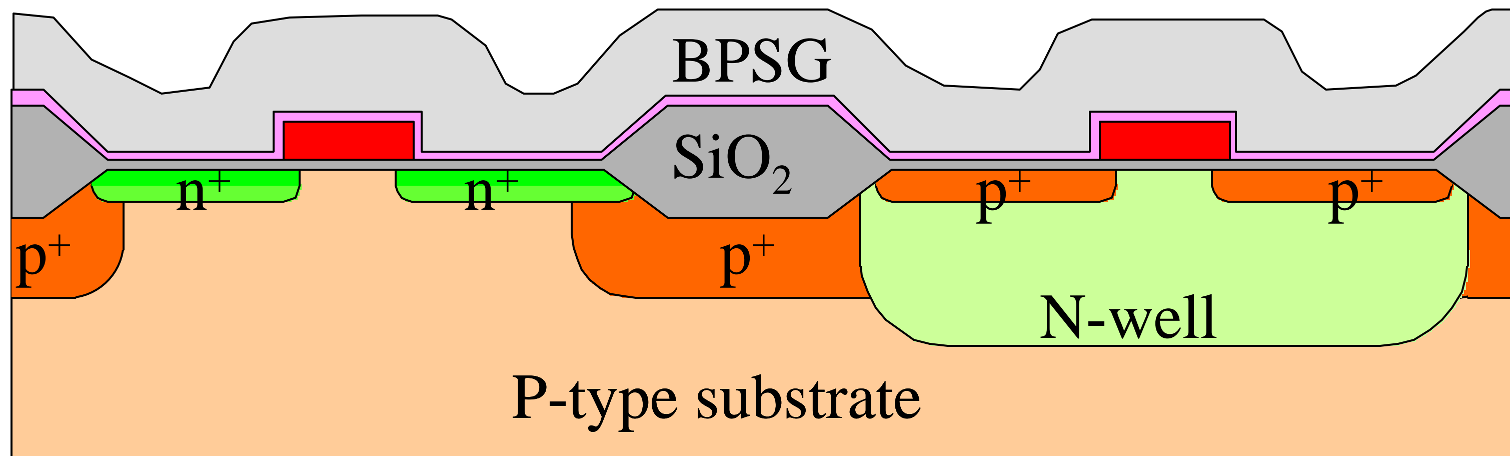
Other Planarization Methods

- Thermal flow
- Sputtering etchback
- Photoresist etchback,
- Spin-on glass (SOG) etchback

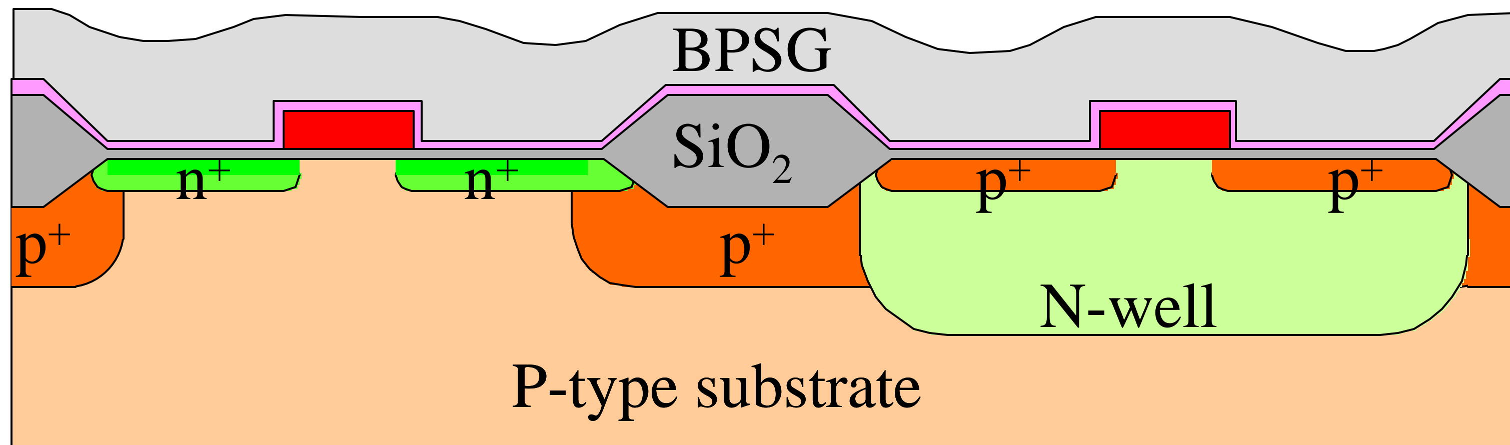
Thermal Flow

- Dielectric planarization
- Pre-metal dielectric
- High temperature, ~1000 °C
- PSG or BPSG, become soft and start to flow due to the surface tension
- Smooth and local planarization

As Deposited



After Thermal Flow



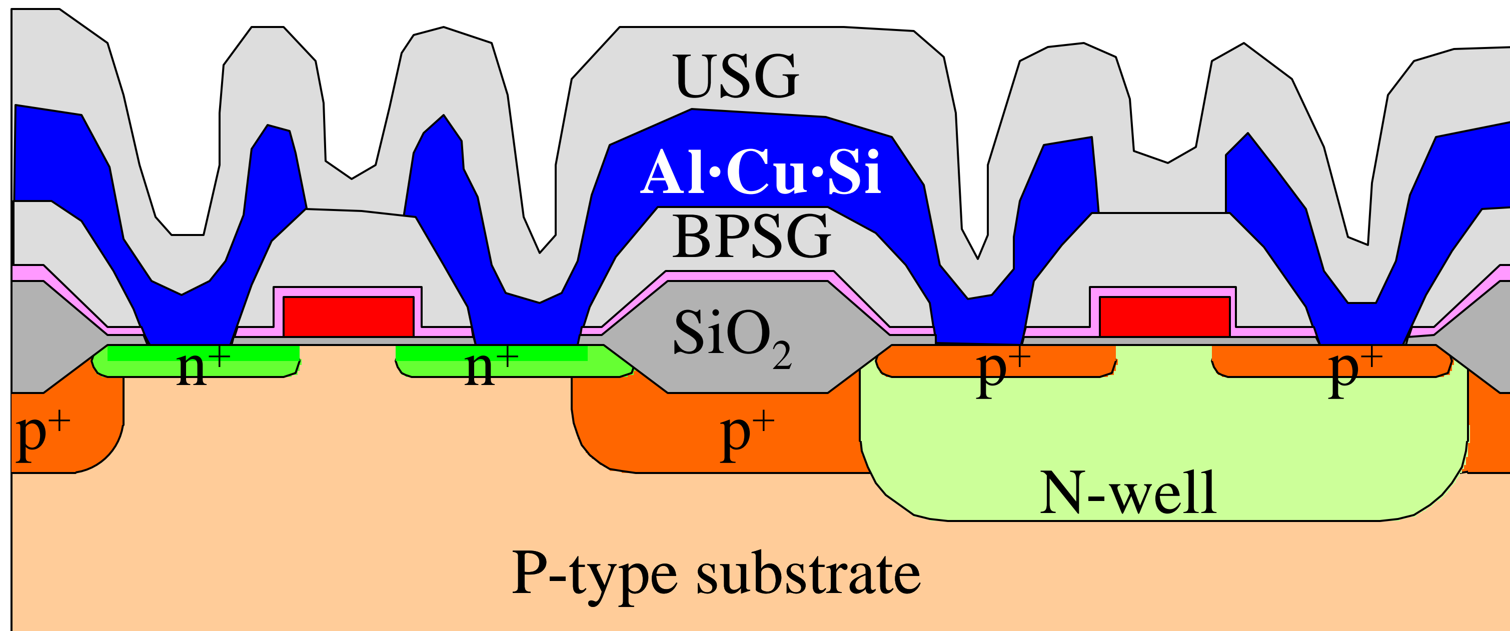
Etch Back

- Reflow temperature is too high for IMD
  - can melt aluminum
- Other planarization method is needed for IMD
- Sputtering etch back and reactive etch back

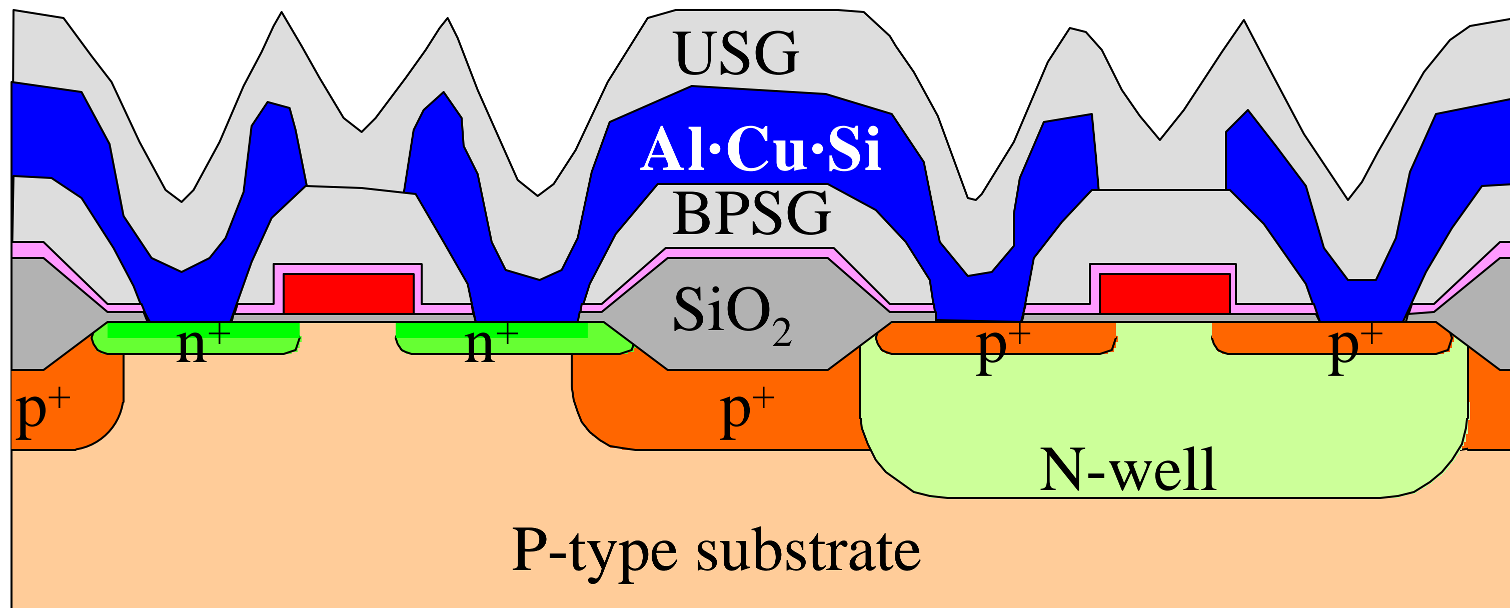
Etch Back

- Argon sputtering etchback chip off dielectric at corner of the gap and taper the openings
- Subsequent CVD process easily fills the gap with a reasonable planarized surface
- Reactive ion etchback process with CF_4/O_2 chemistry further planarizes the surface

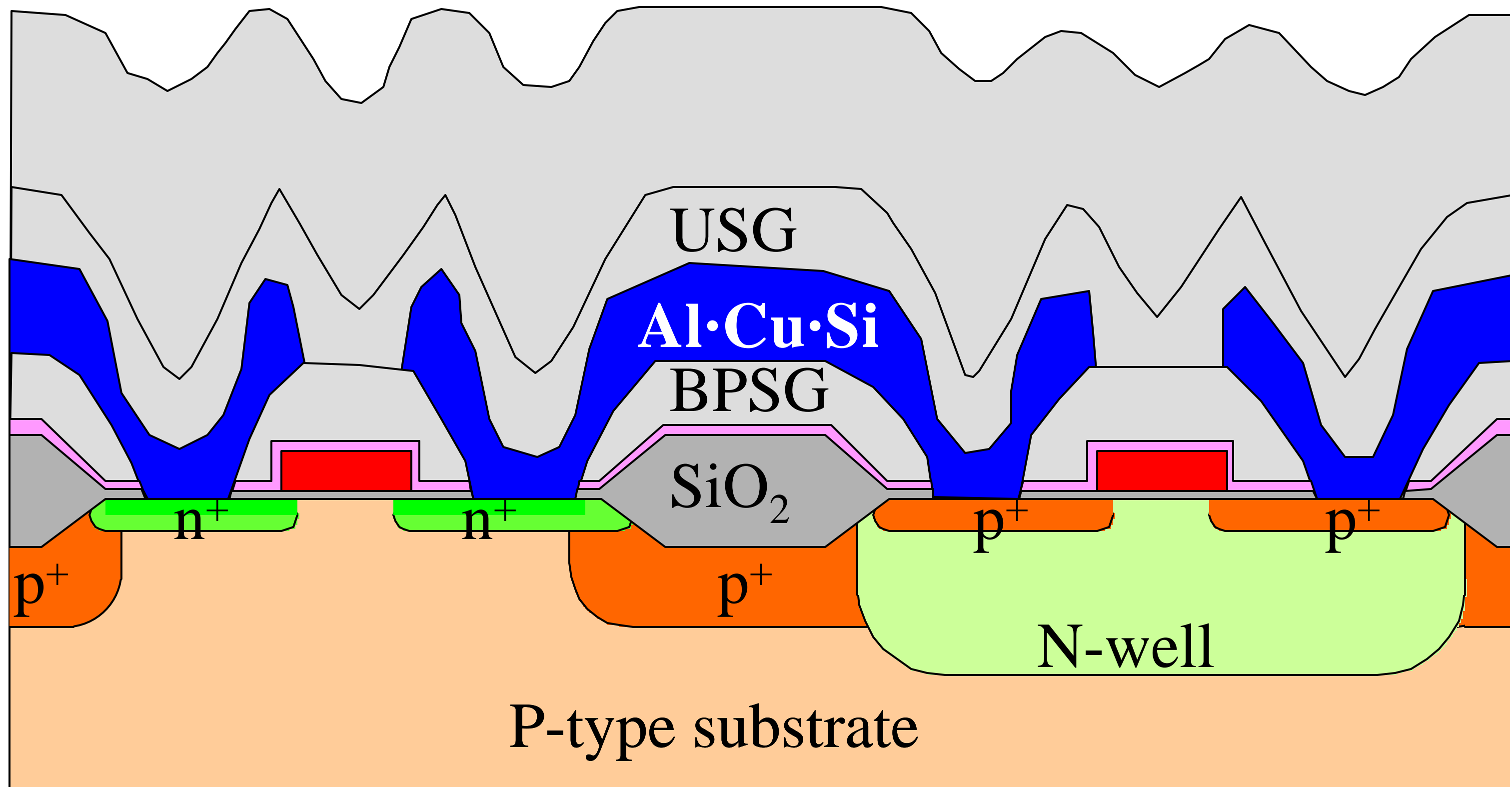
CVD USG



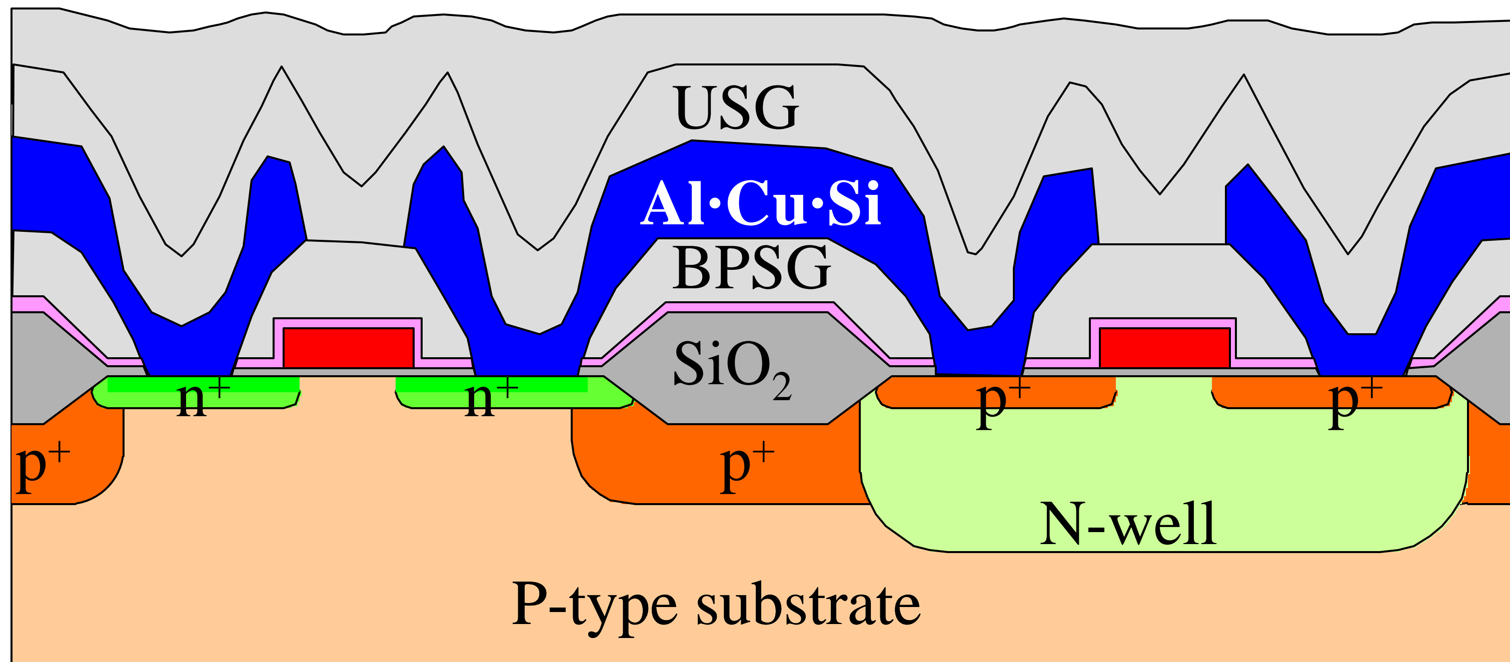
Sputtering Etch Back of USG



CVD USG



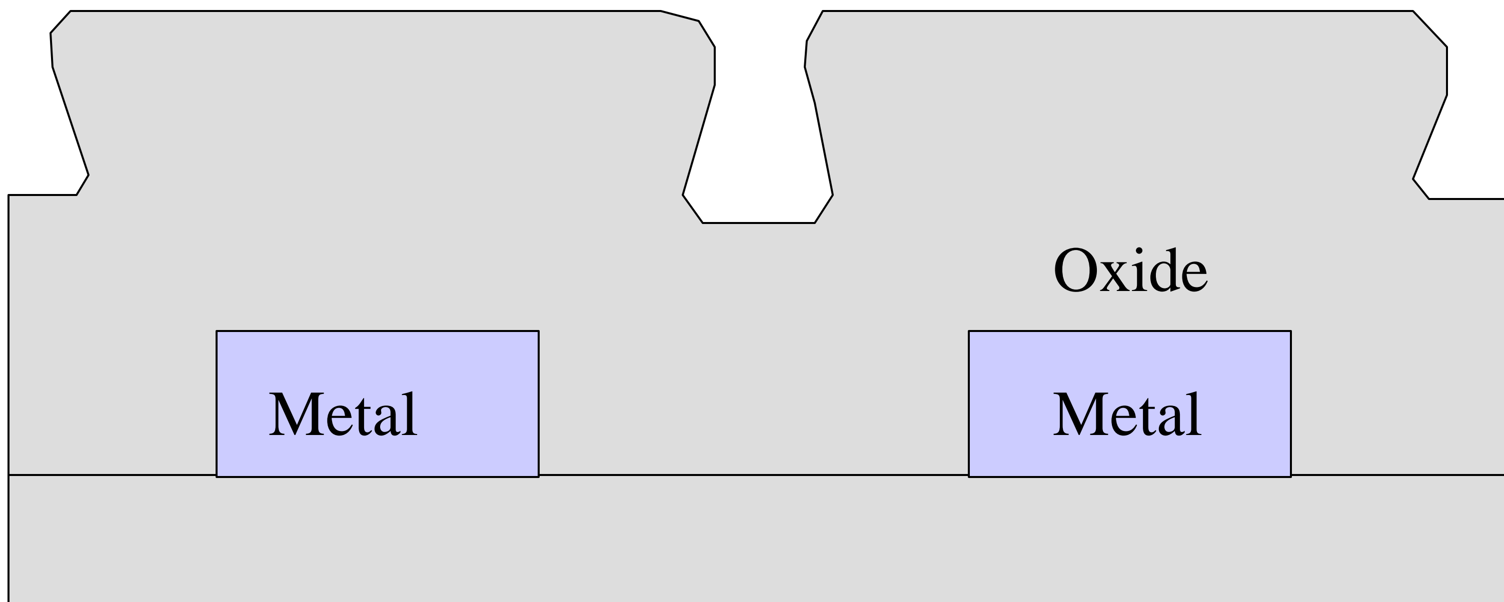
Reactive Etch Back of USG



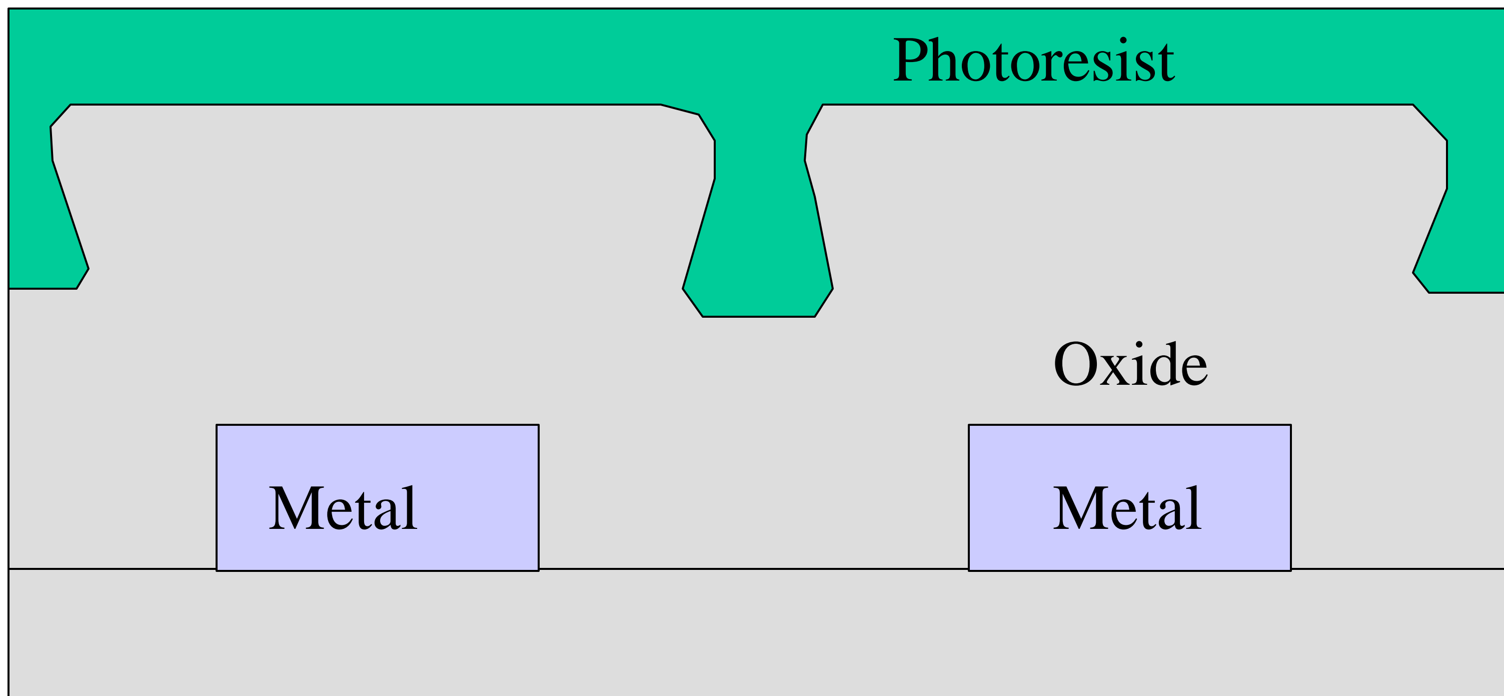
Photoresist Etchback

- PR spin-coats can baking
- Planarized solid thin film on wafer surface
- Plasma etch process with CF_4/O_2 chemistry
- Oxide etched by F and PR by O
- Adjusting CF_4/O_2 flow ratio allows 1:1 of oxide to PR selectivity.
- Oxide could be planarized after etchback

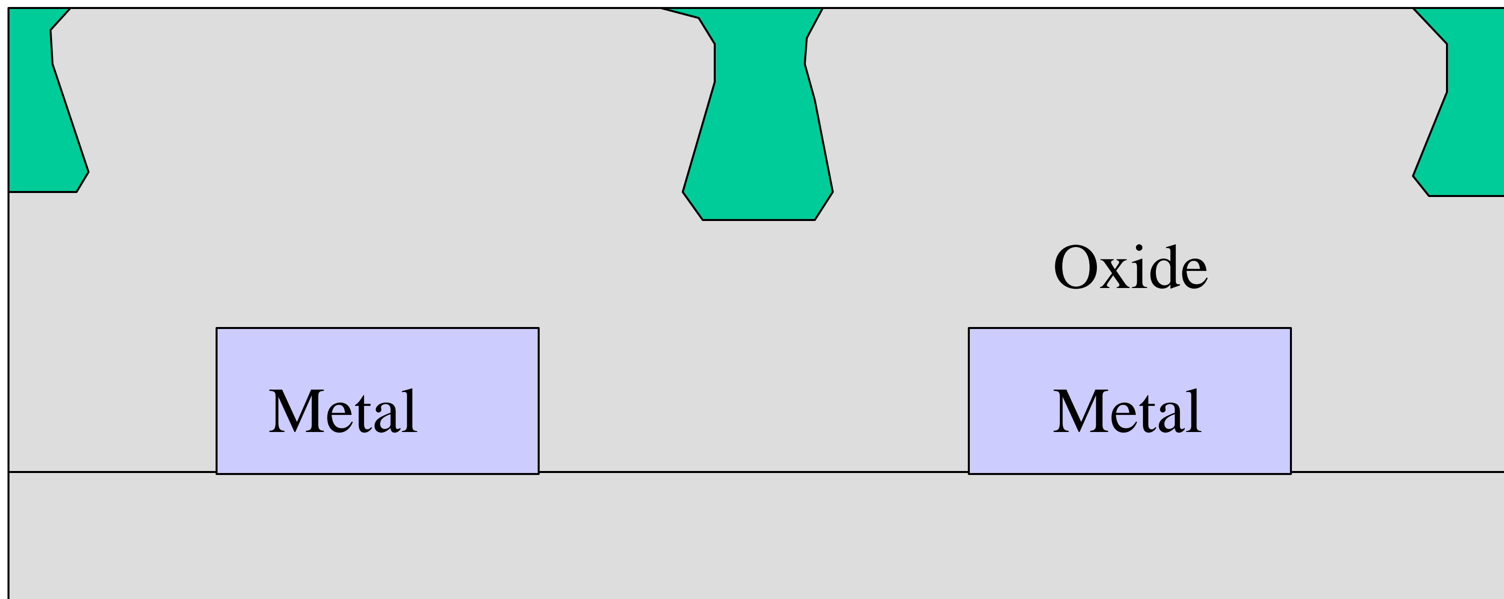
After Oxide Deposited



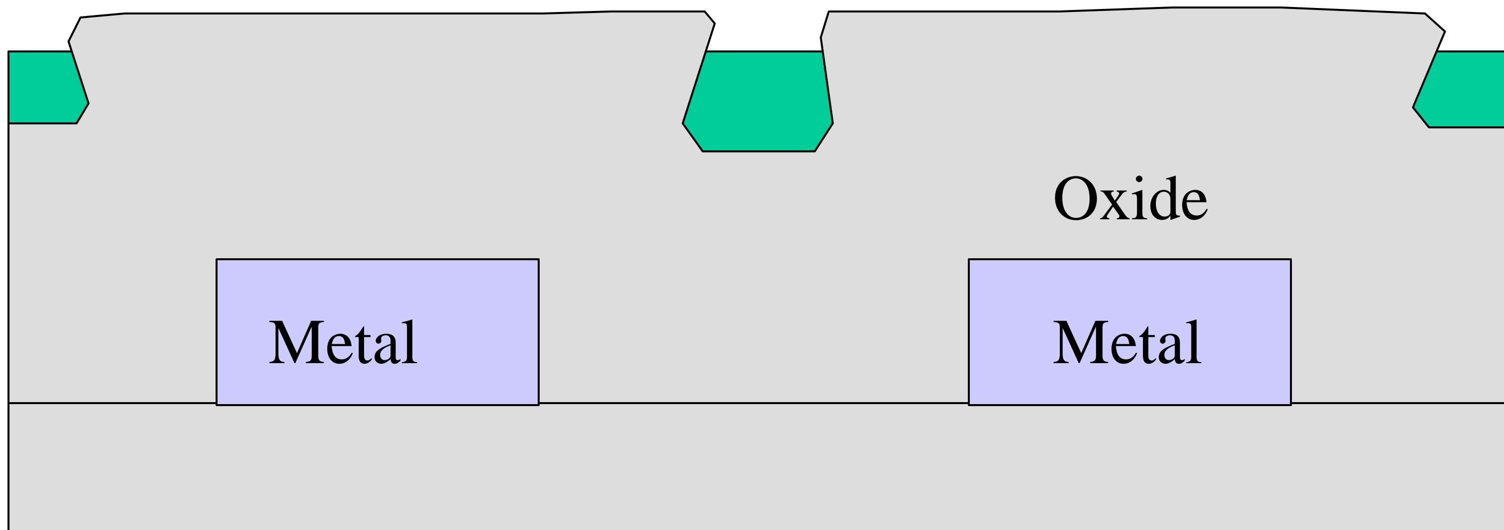
Photoresist Coating and Baking



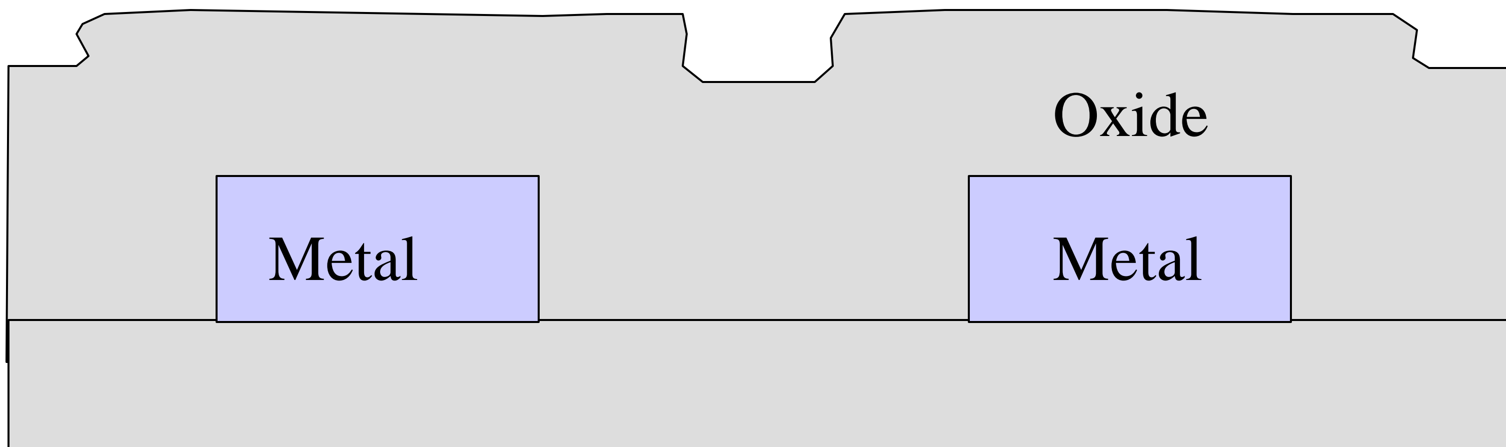
Photoresist Etchback



Photoresist Etchback



Photoresist Etchback



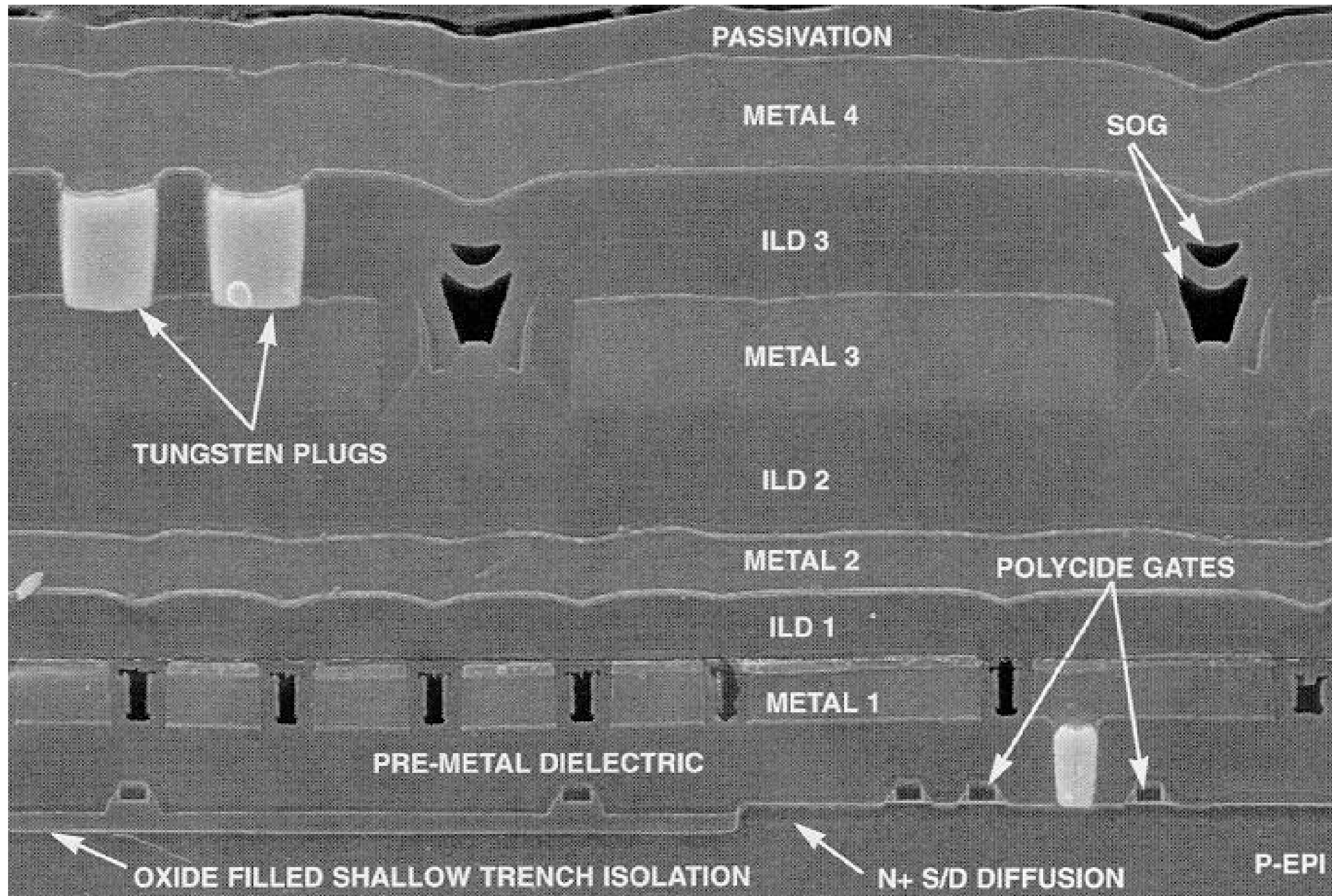
Photoresist Etchback

- When F etch oxide, O will be released
- Higher PR etch rate due to extra oxygen
- PR etchback can't planarize very well
- After the PR etchback, dielectric film surface is flatter than it is just deposited.
- In some cases, more than one PR etchback is needed to achieve required flatness

SOG Etchback

- SOG replaces PR
- Advantage: some SOG can stay on the wafer surface to fill the narrow gaps
- PECVD USG liner and cap layer
- USG/SOG/USG gap fill and surface planarization
- Sometimes, two SOG coat, cure and etchback processes are used

SOG Etchback



Necessity of CMP

- Photolithography resolution $R = K_1\lambda/NA$
- To improve resolution, $NA\uparrow$ or $\lambda\downarrow$
- $DOF = K_2\lambda/2(NA)^2$, both approaches to improve resolution reduce DOF
- DOF is about 2,083 Å for 0.25 μm and 1,500 Å for 0.18 μm resolution.
- Here we assumed K_1=K_2, λ=248 nm (DUV), and NA=0.6

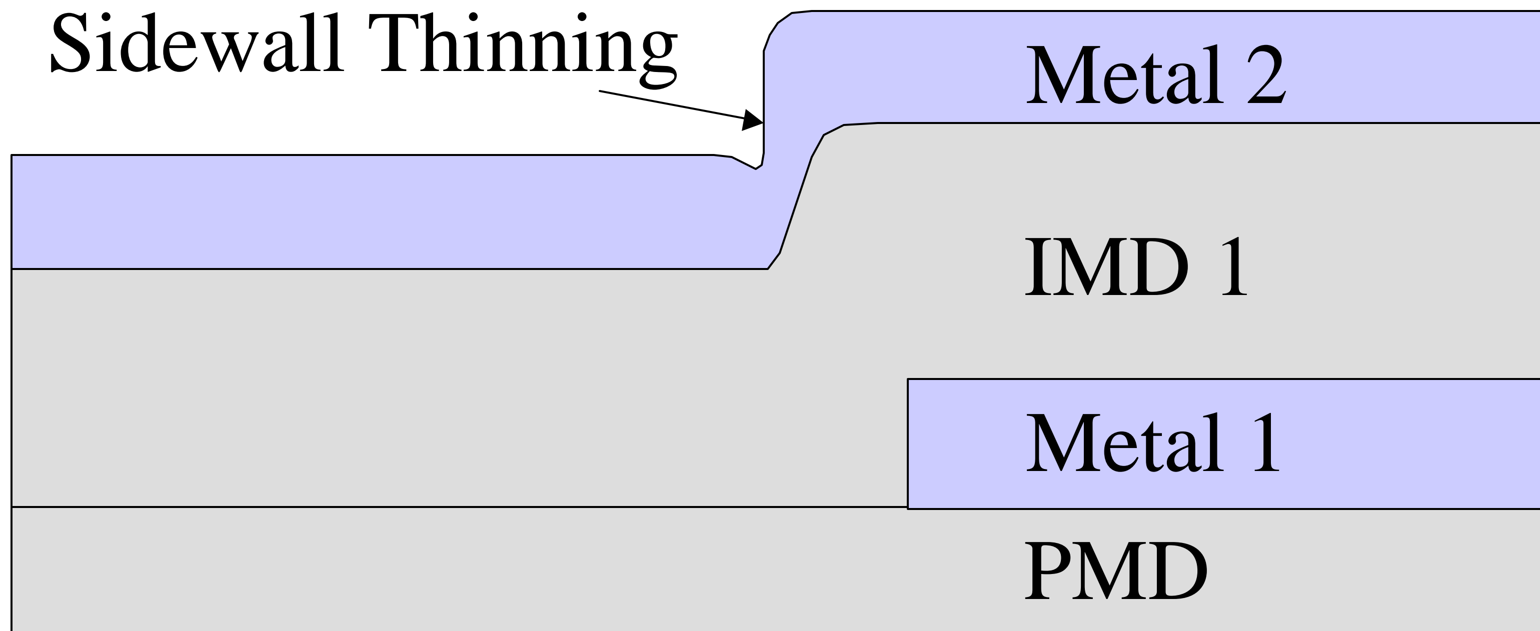
Necessity of CMP

- 0.25 μm pattern require roughness < 2000 Å
- Only CMP can achieve this planarization
- When feature size > 0.35 μm, other methods can be used

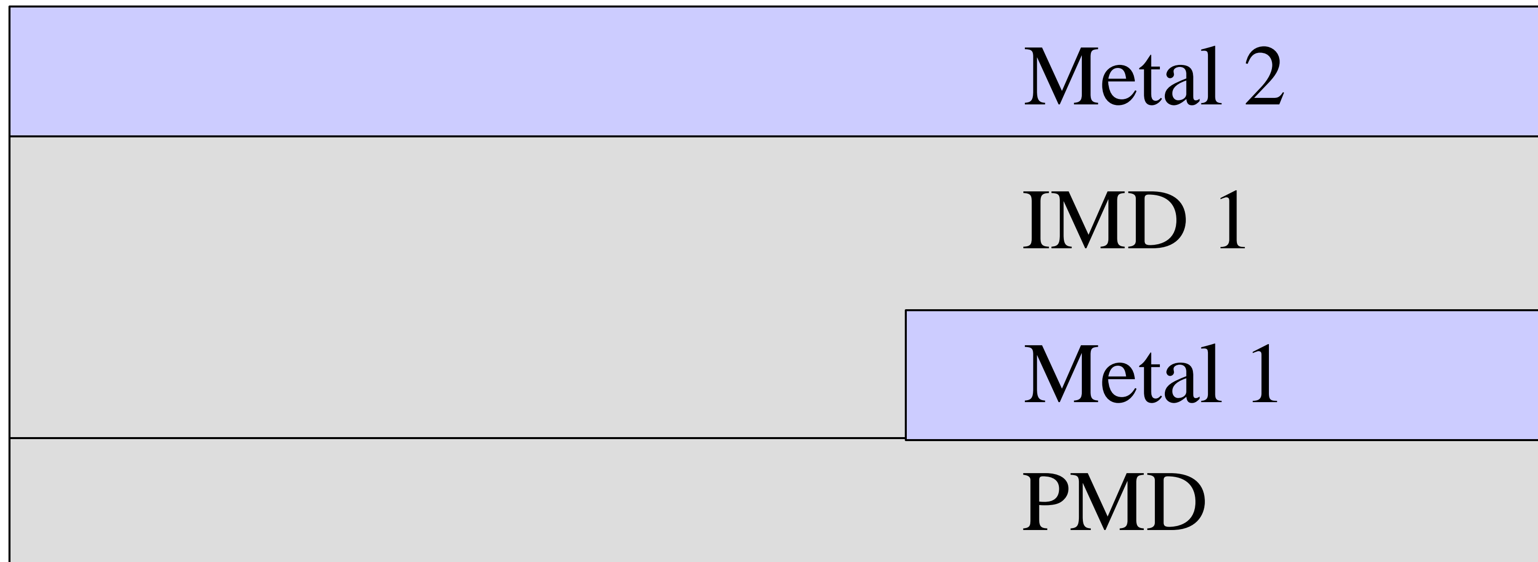
Advantages of CMP

- Planarized surface allows higher resolution of photolithography process
- The planarized surface eliminates sidewall thinning because of poor PVD step coverage

Metal Line Thinning Due to the Dielectric Step



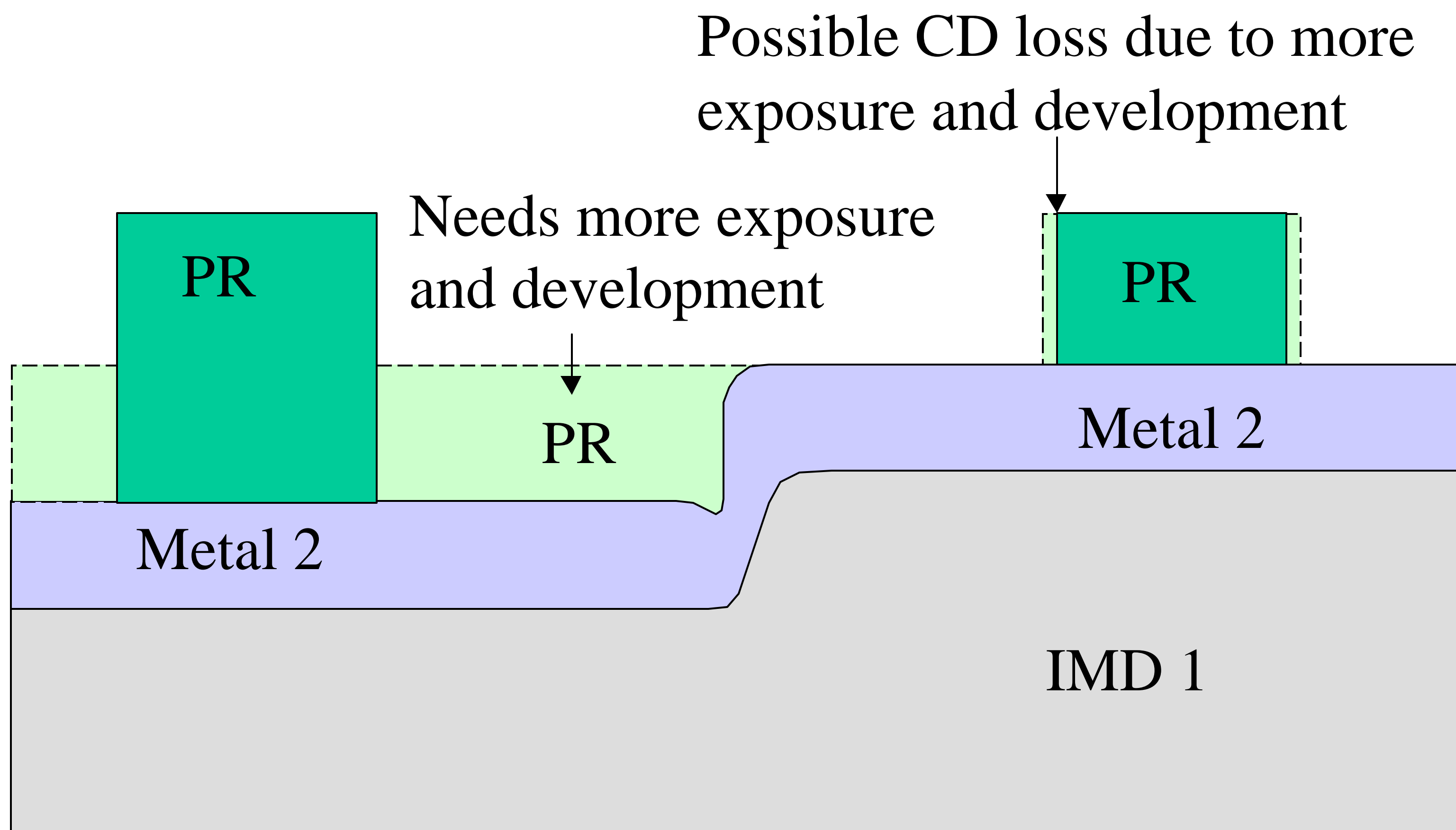
Planarized Dielectric Surface, no Metal Line Thinning Effect



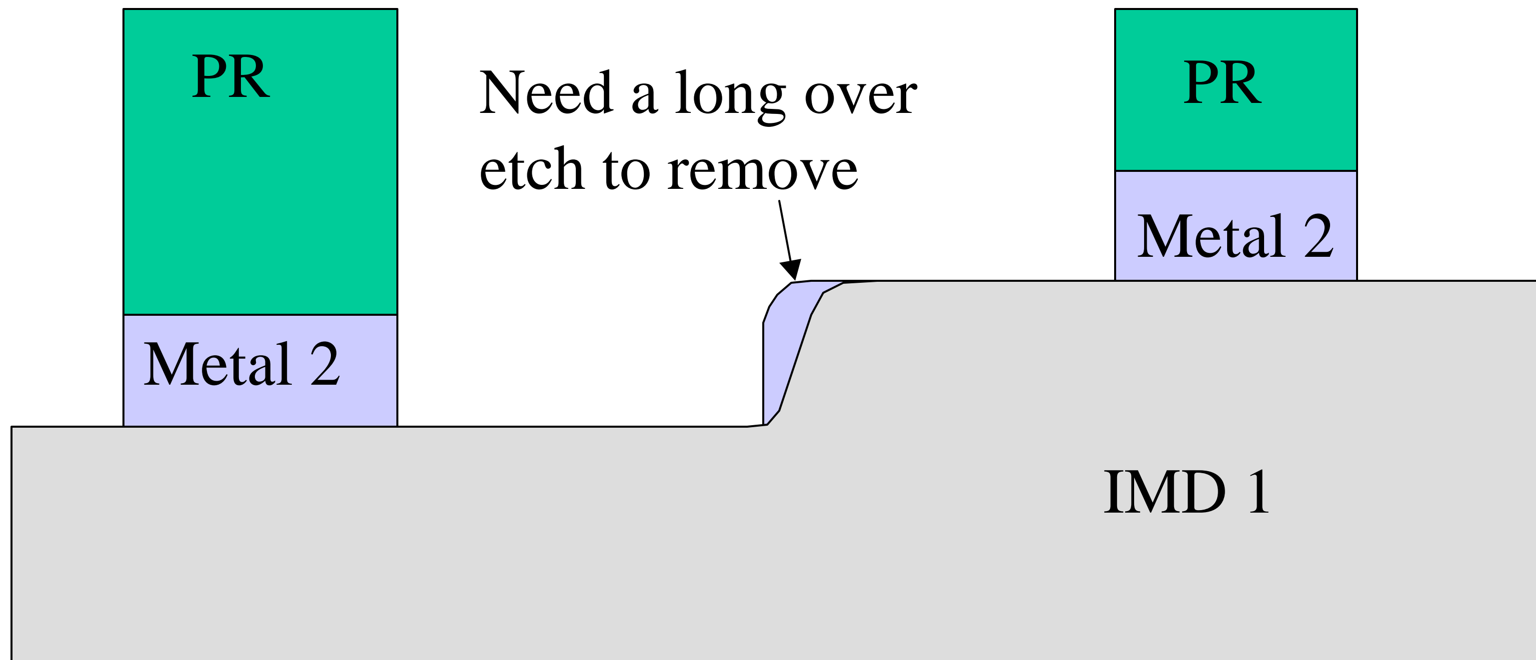
Advantages of CMP

- Eliminate the requirement of excessive exposure and development to clear the thicker photoresist regions due to the dielectric steps
  - This improves the resolution of via hole and metal line pattering processes
- Uniform thin film deposition
  - Reduce required over etch time
  - Reduce chance of undercut or substrate loss

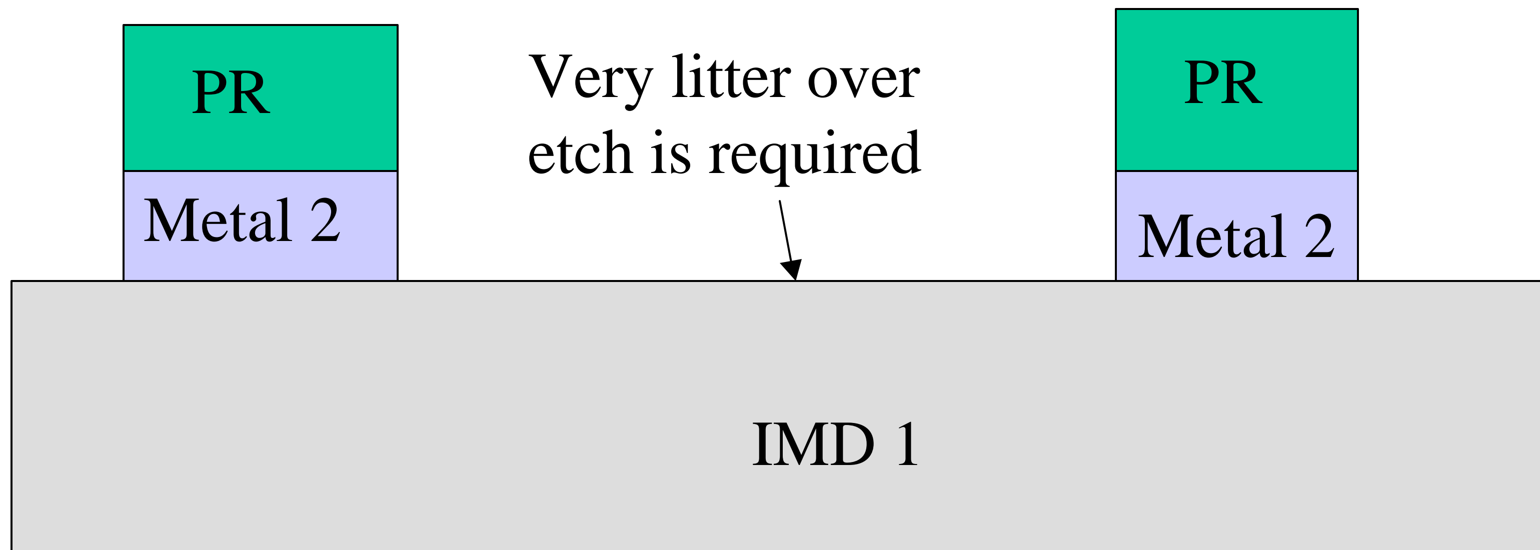
Over Exposure and Over Development



Rough Surface, Long Over Etch



Flat Surface, Short Over Etch



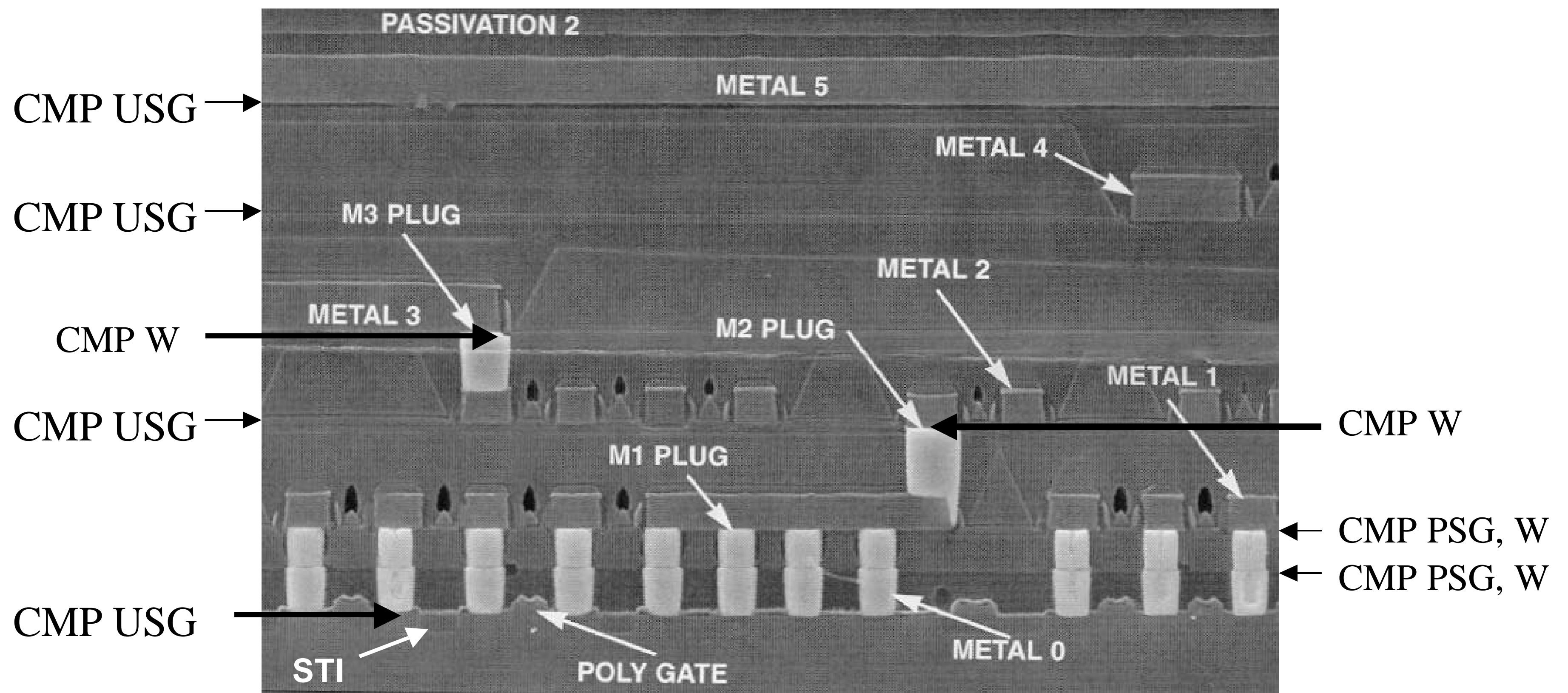
Advantages of CMP

- CMP reduce defect density, improve yield
  - Reducing the process problems in thin film deposition, photolithography, and etch.
- CMP also widens IC chip design parameters
- CMP can introduce defects of its own
- Need appropriate post-CMP cleaning

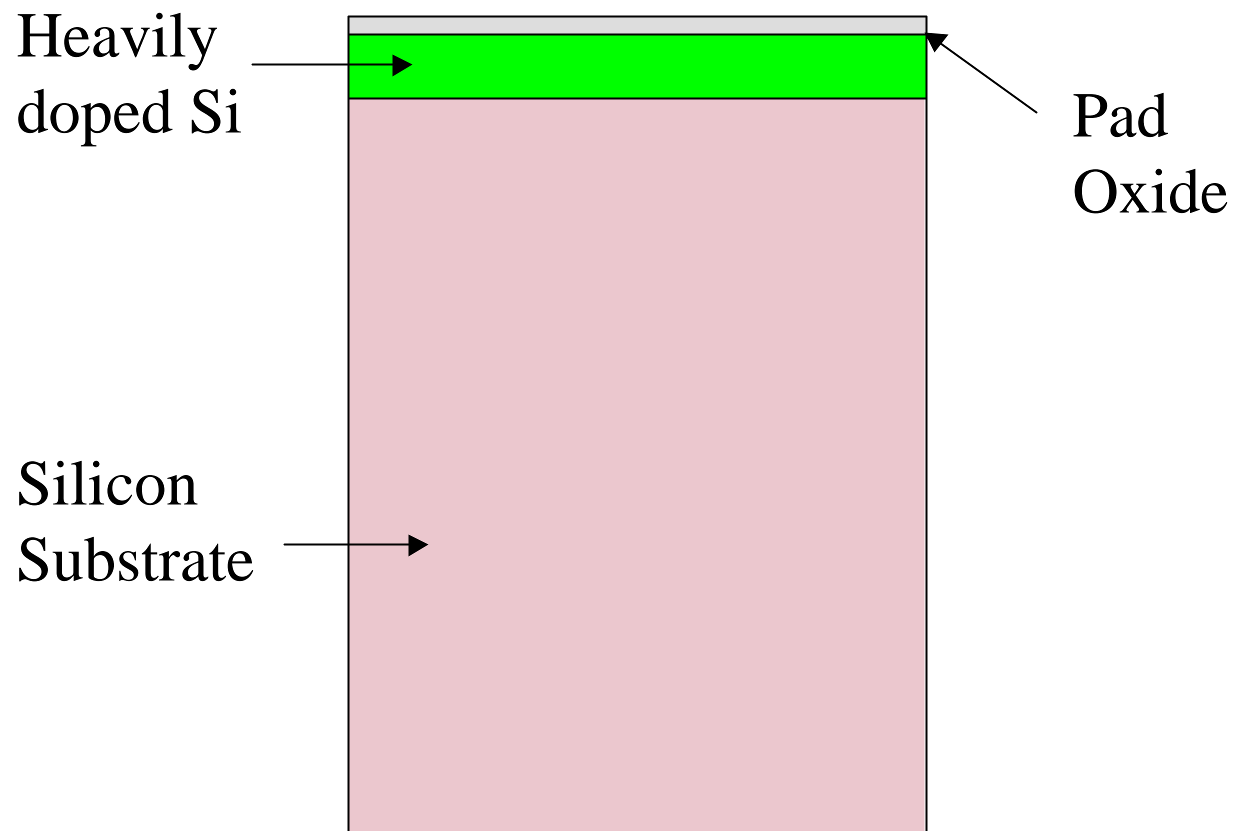
Applications of CMP

- STI formation
- Dielectric layer planarization
  - PMD and IMD
- Tungsten plug formation
- Deep trench capacitor

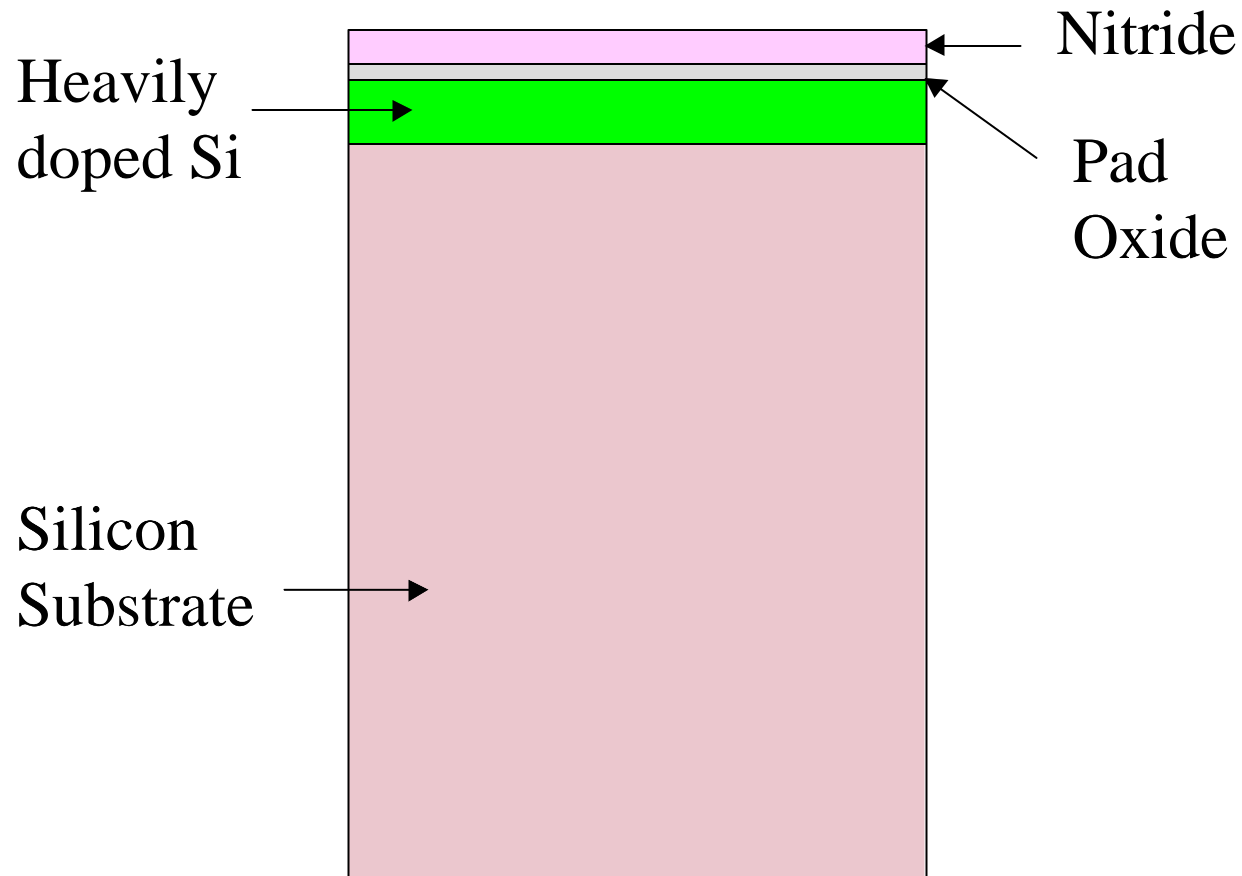
Applications of CMP



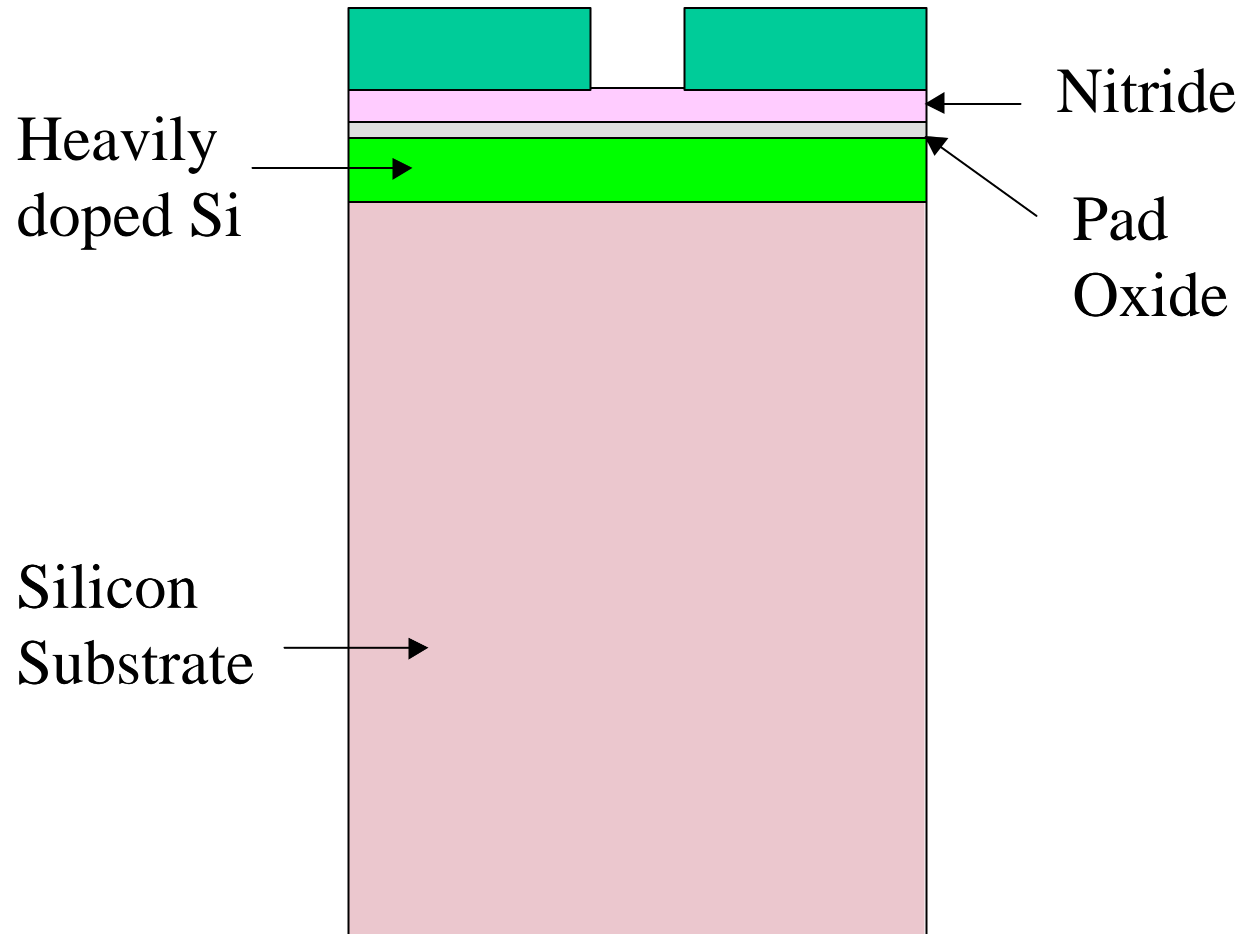
Deep Trench Capacitor



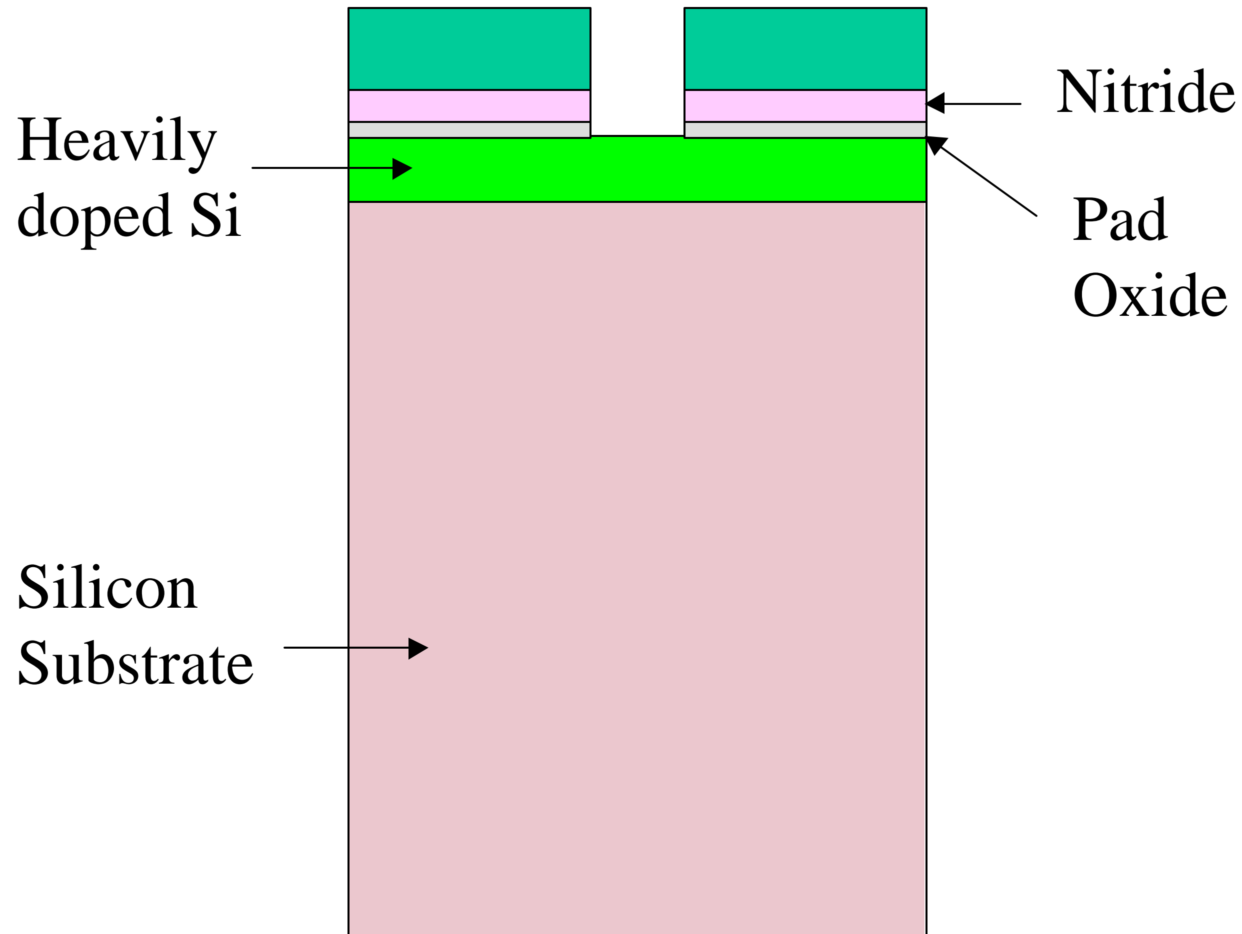
Deep Trench Capacitor



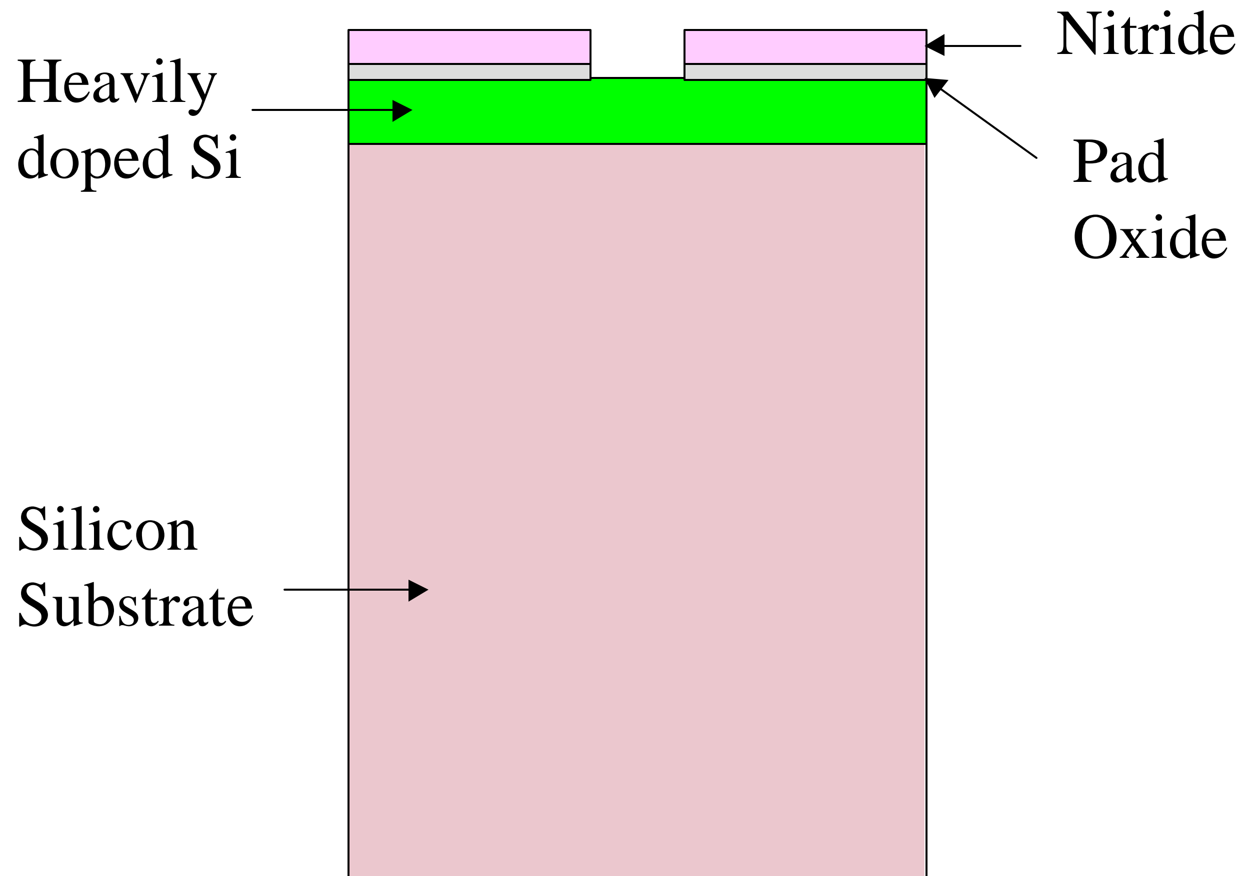
Deep Trench Capacitor



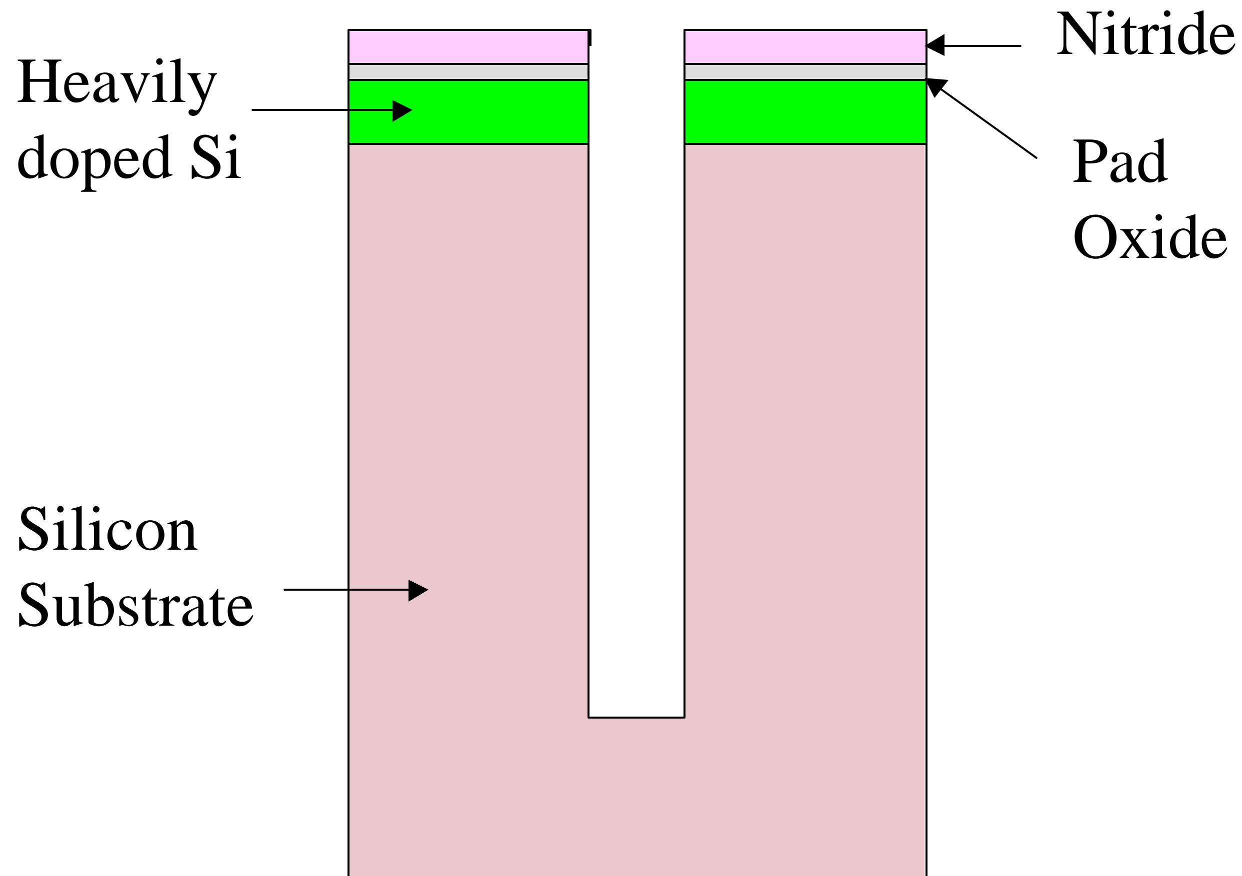
Deep Trench Capacitor



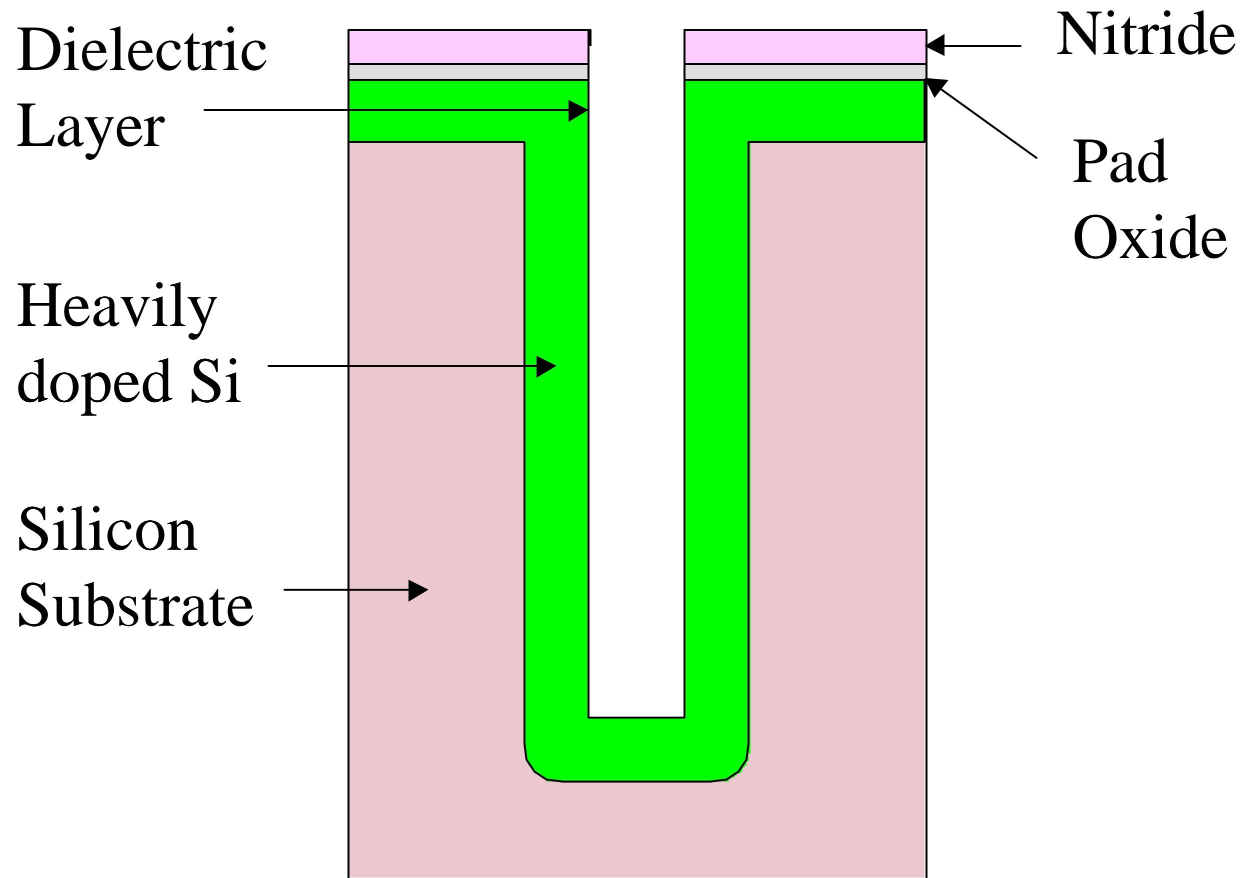
Deep Trench Capacitor



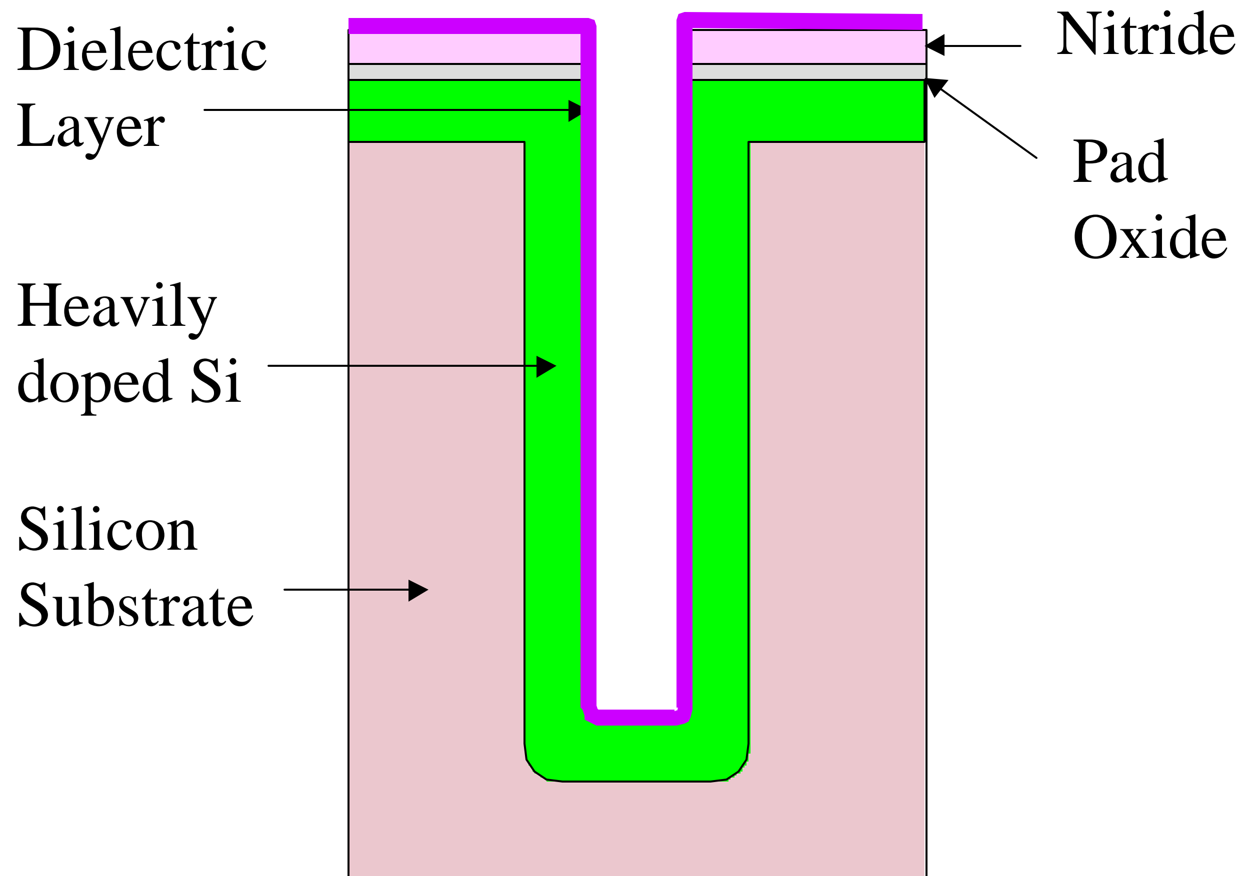
Deep Trench Capacitor



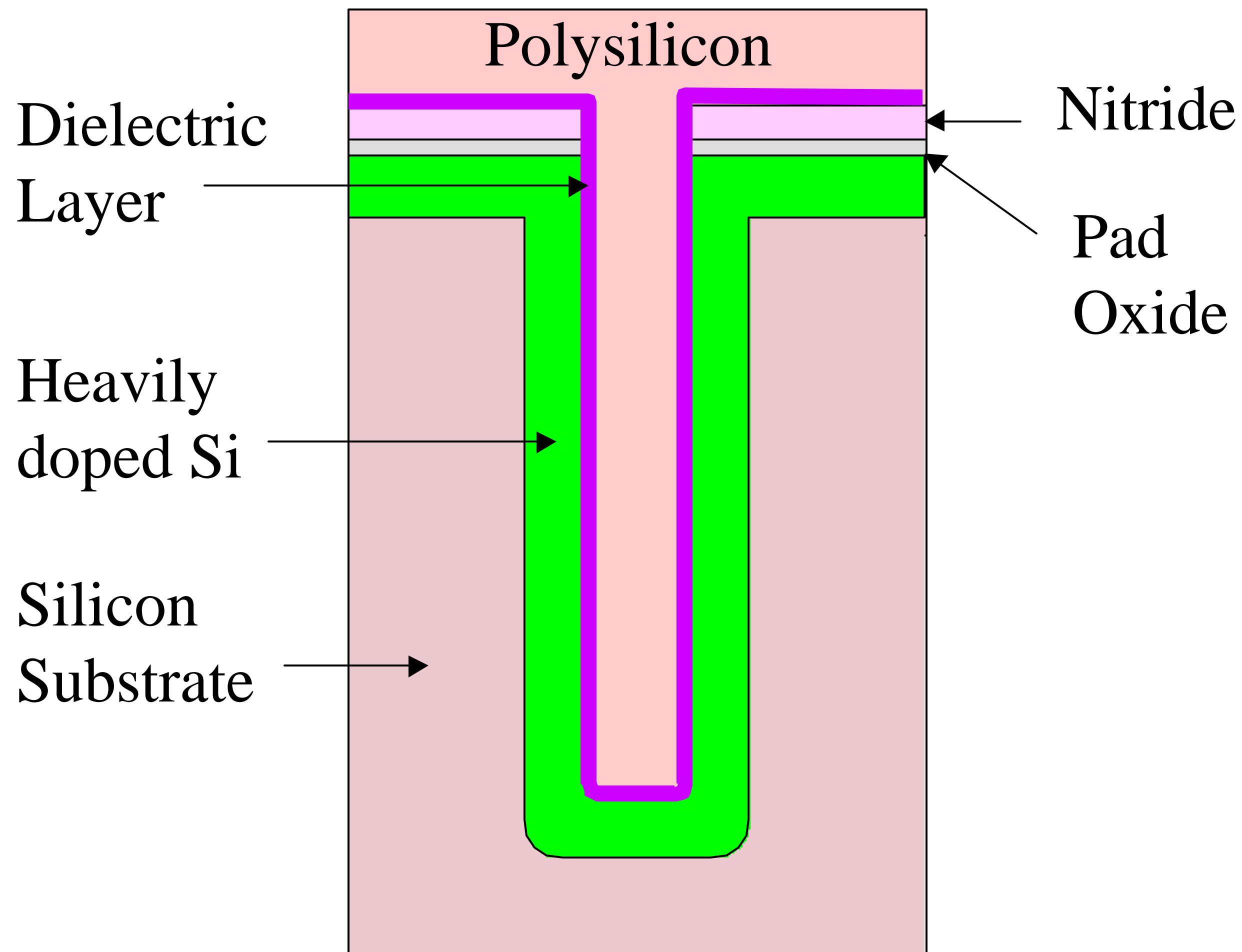
Deep Trench Capacitor



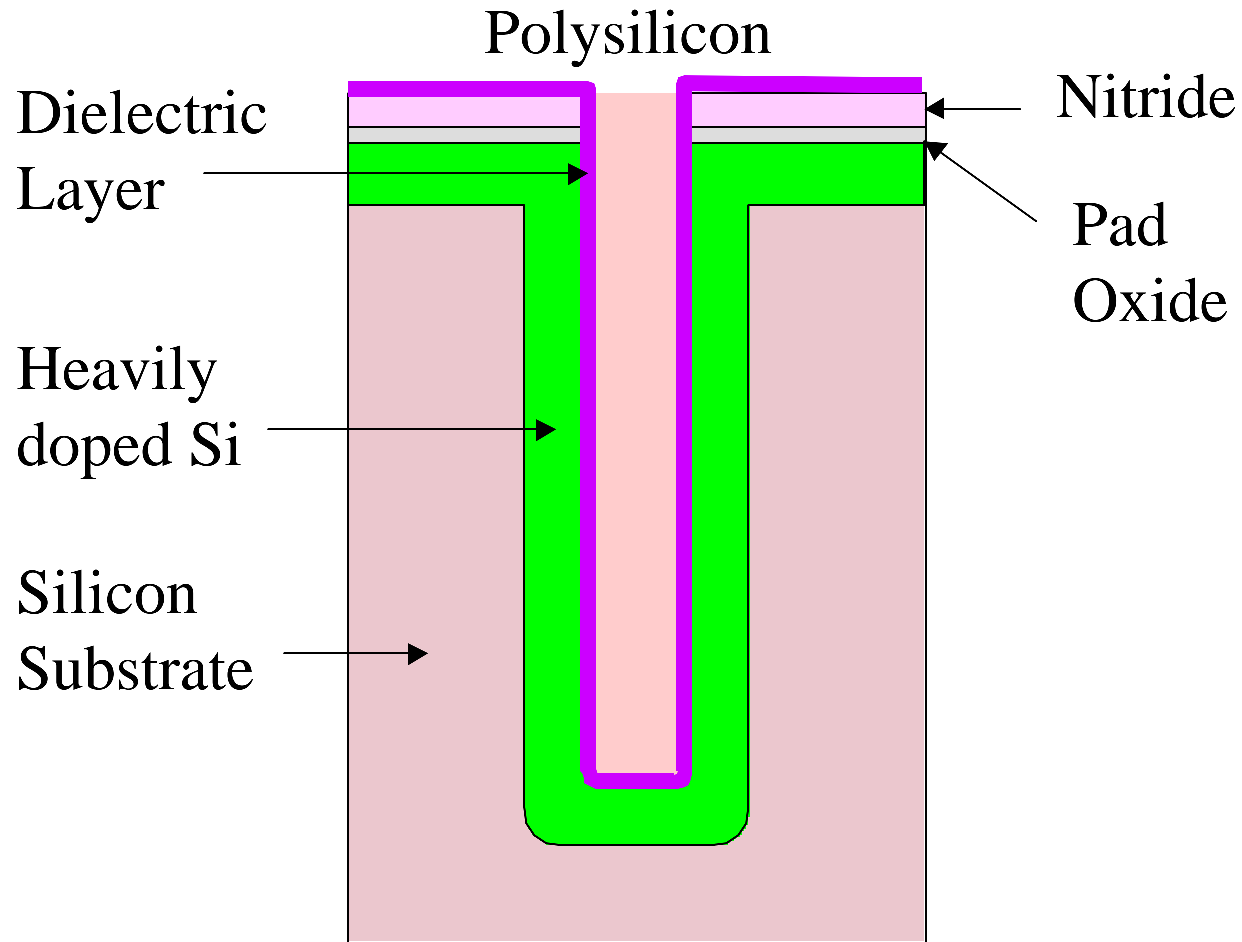
Deep Trench Capacitor



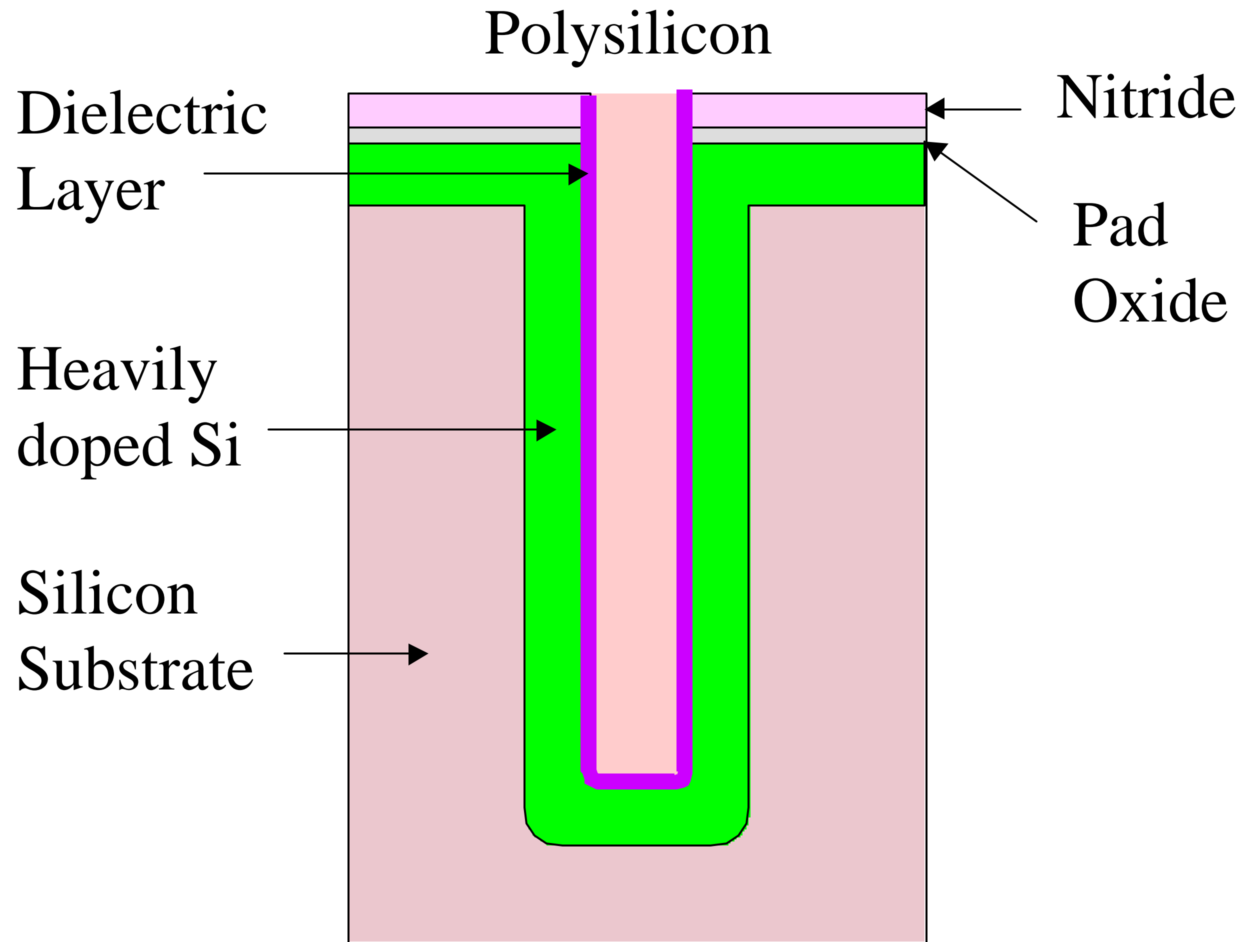
Deep Trench Capacitor



Deep Trench Capacitor



Deep Trench Capacitor



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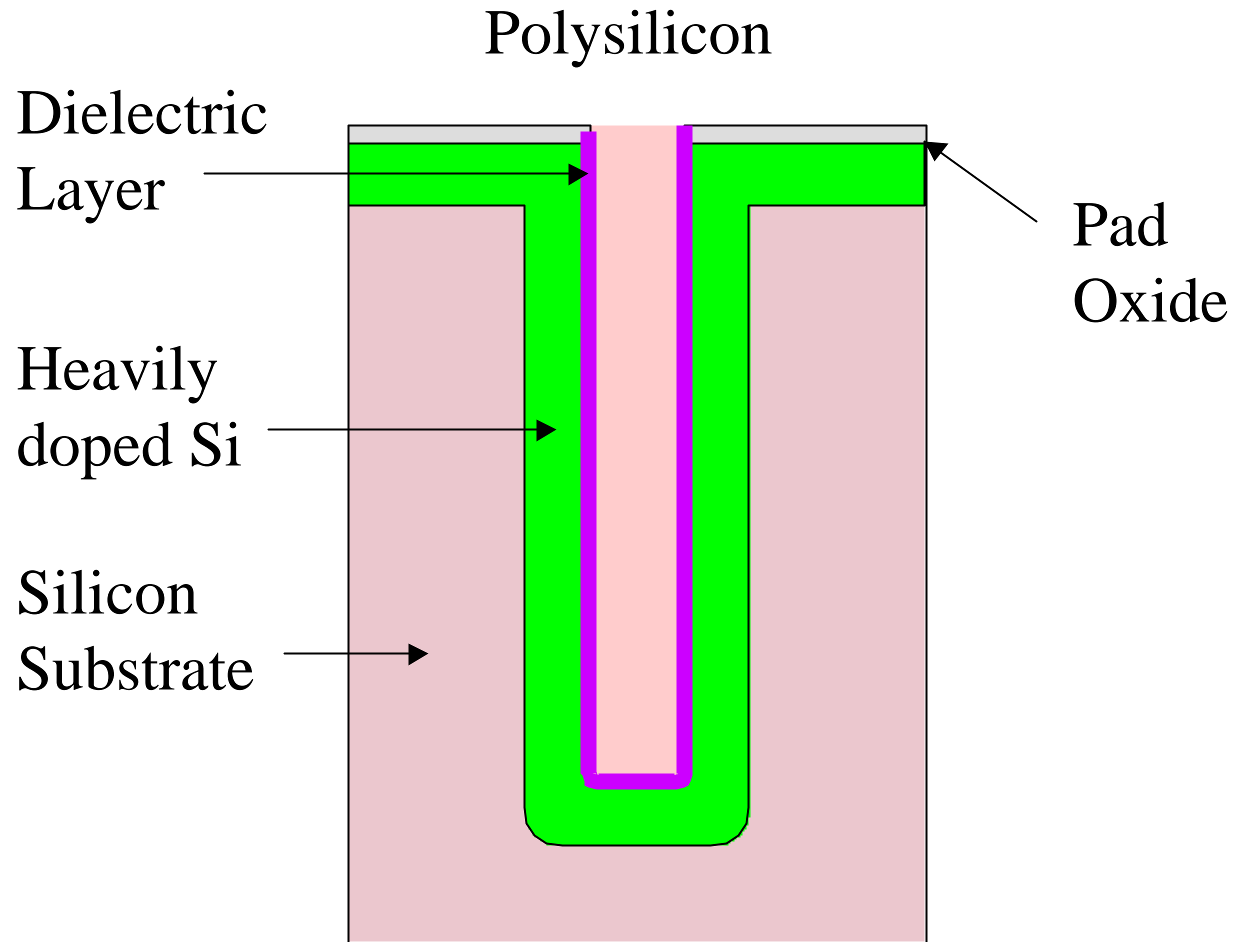
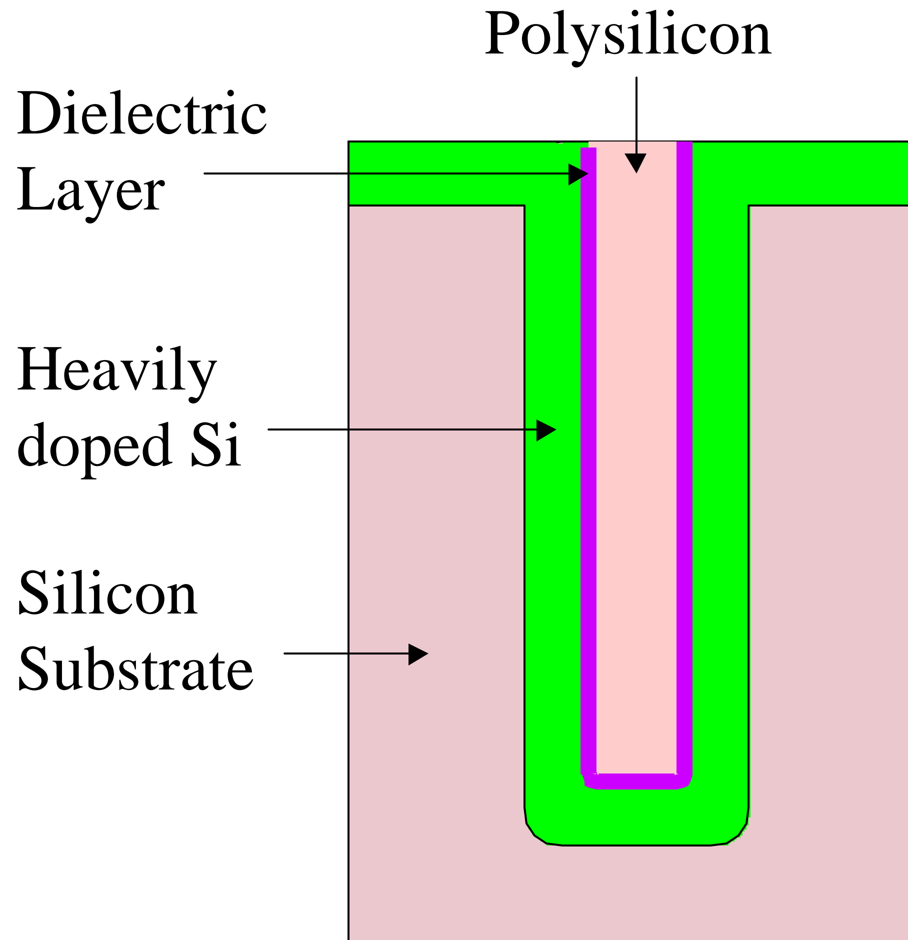


Deep Trench Capacitor



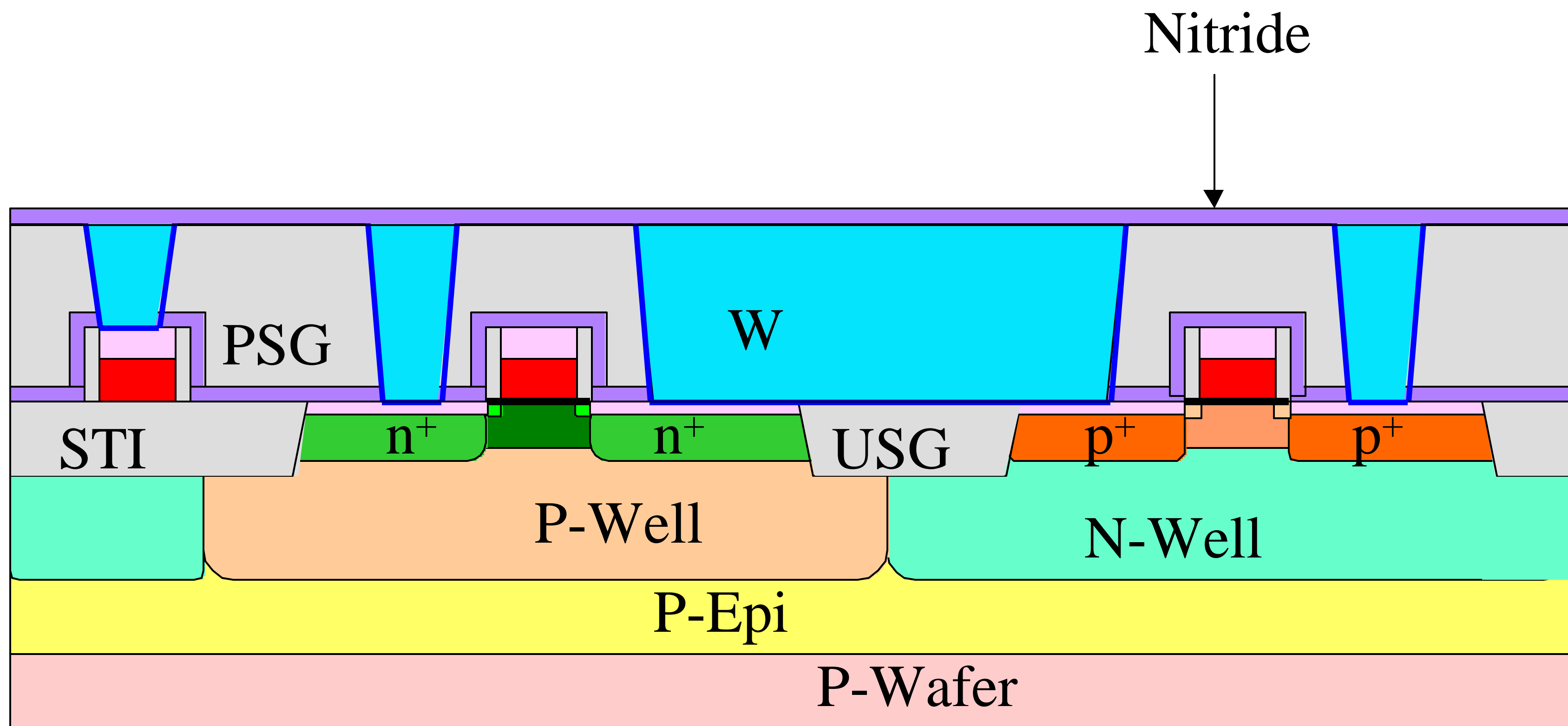
Applications of CMP

- Copper interconnection.
- Copper is very difficult to dry etch,
- Dual damascene: process of choice
- Tungsten plug is a damascene process

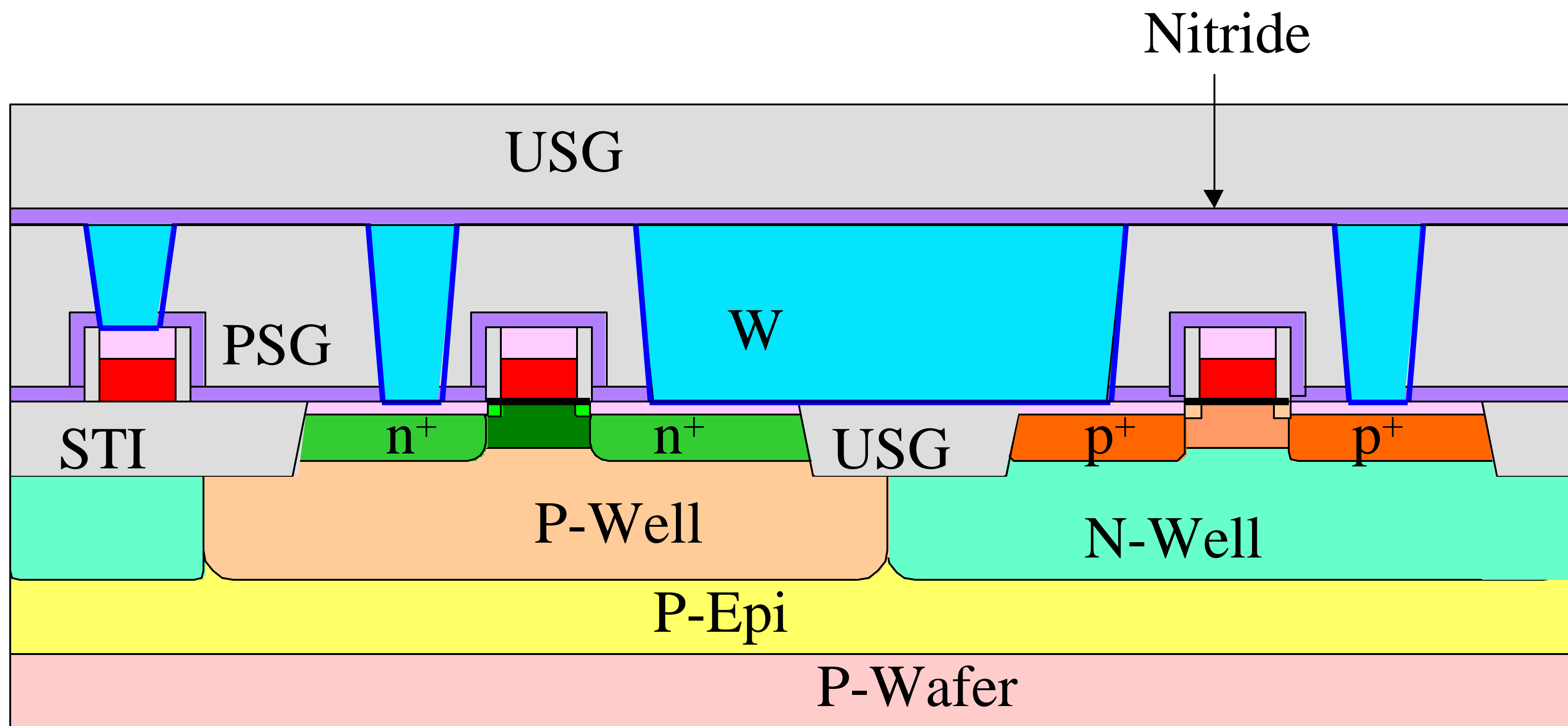
Applications of CMP

- It uses two dielectric etch processes,
  - one via etch and one trench etch
- Metal layers are deposition into via holes and trenches.
- A metal CMP process removes copper and tantalum barrier layer
- Leave copper lines and plugs imbedded inside the dielectric layer

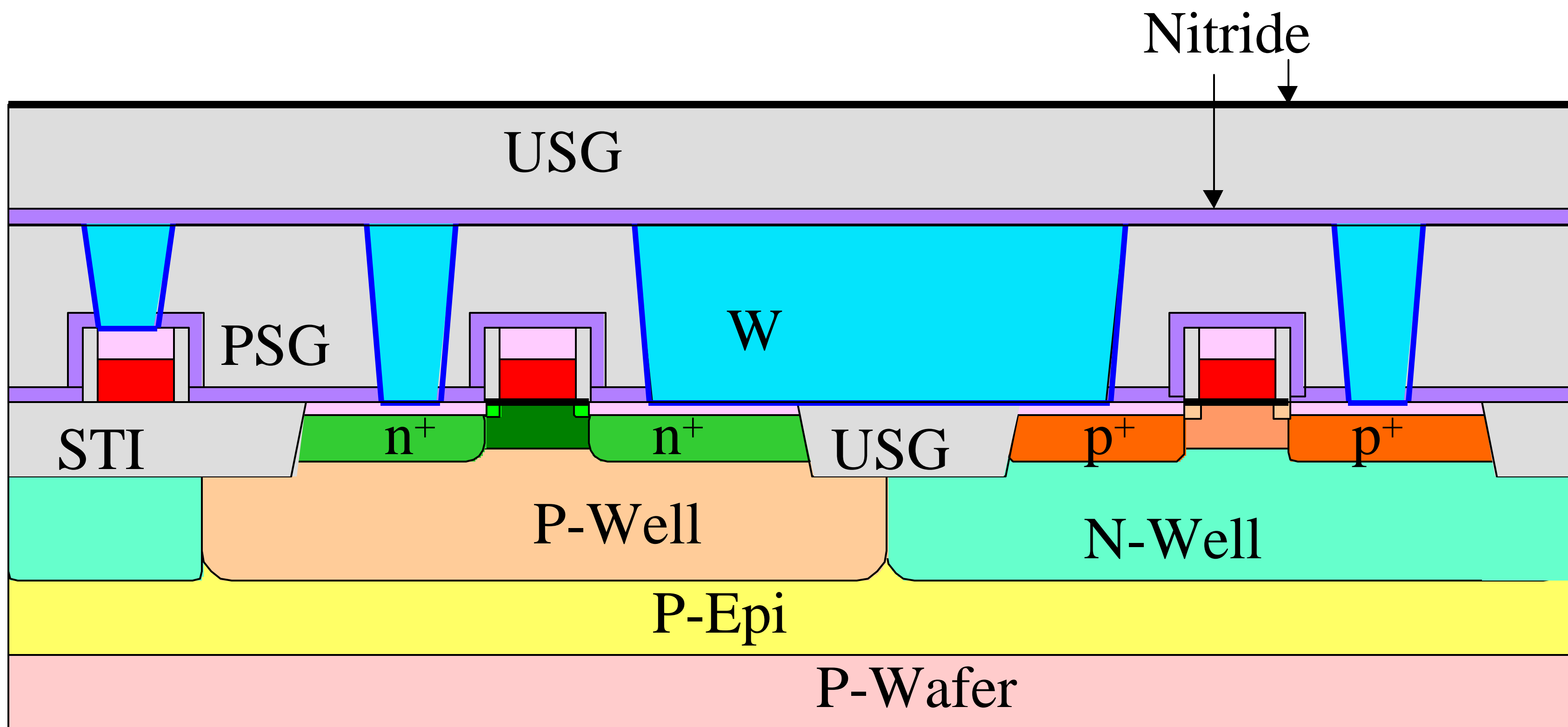
PECVD Nitride



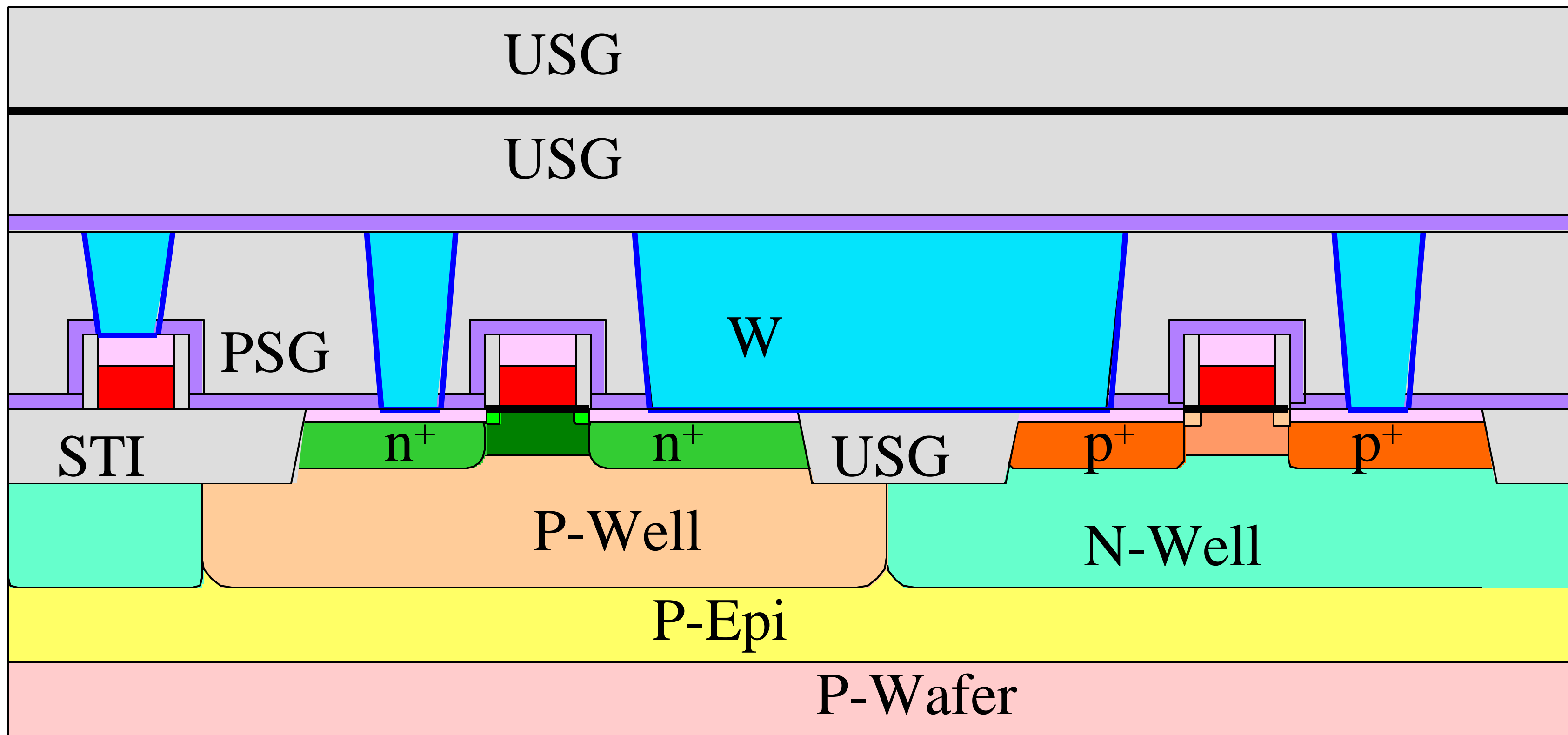
PECVD USG



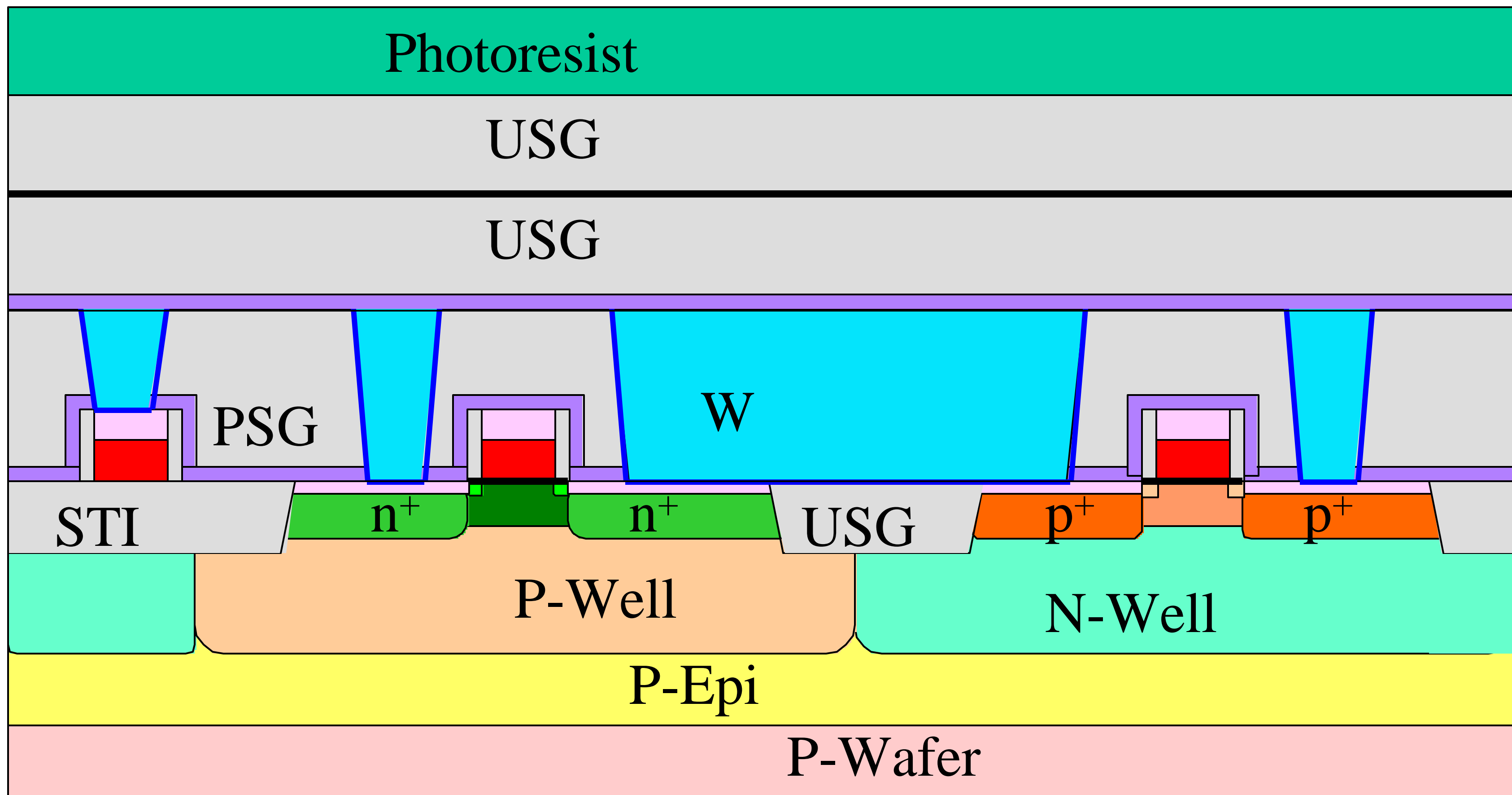
PECVD Etch Stop Nitride



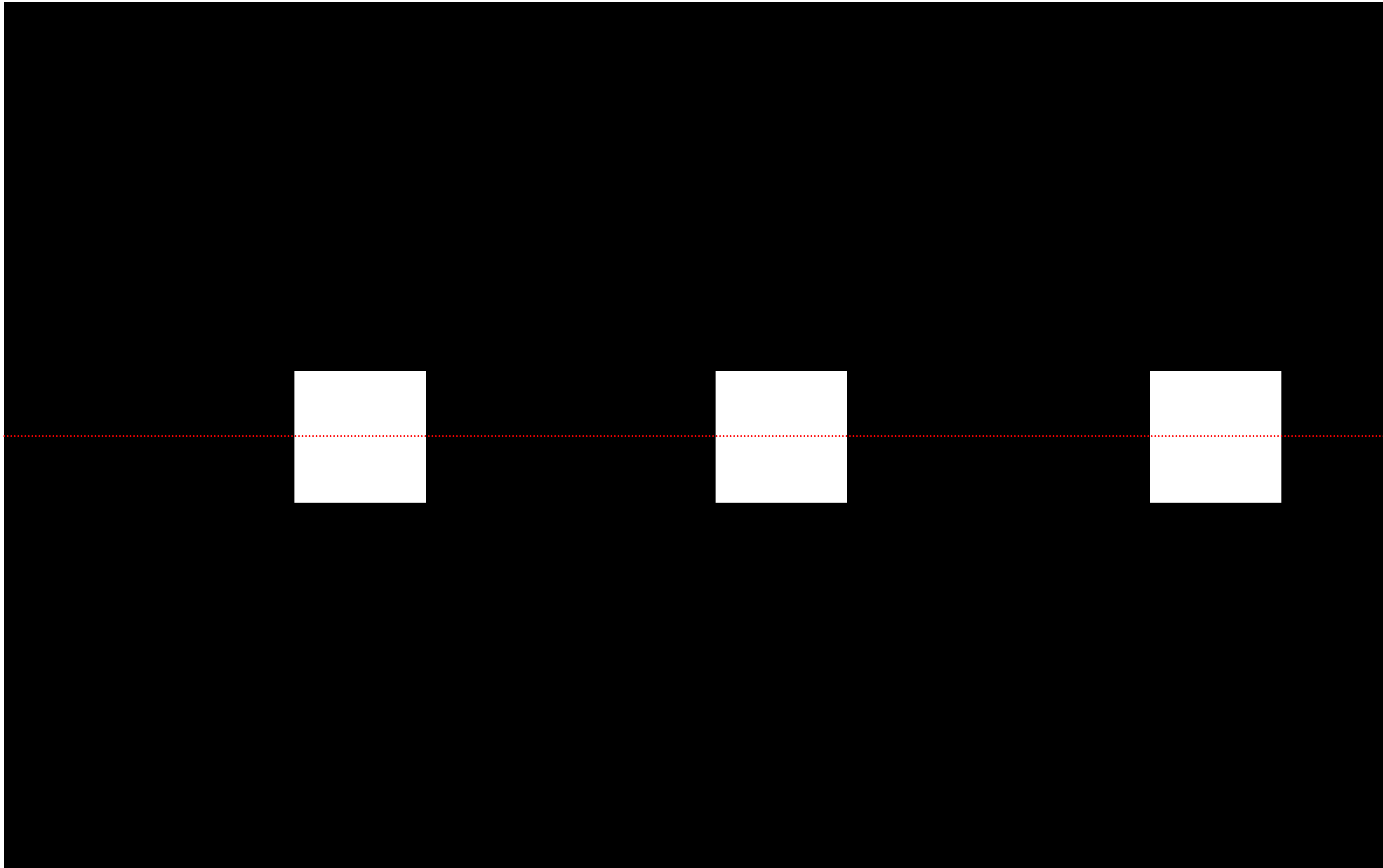
PECVD USG



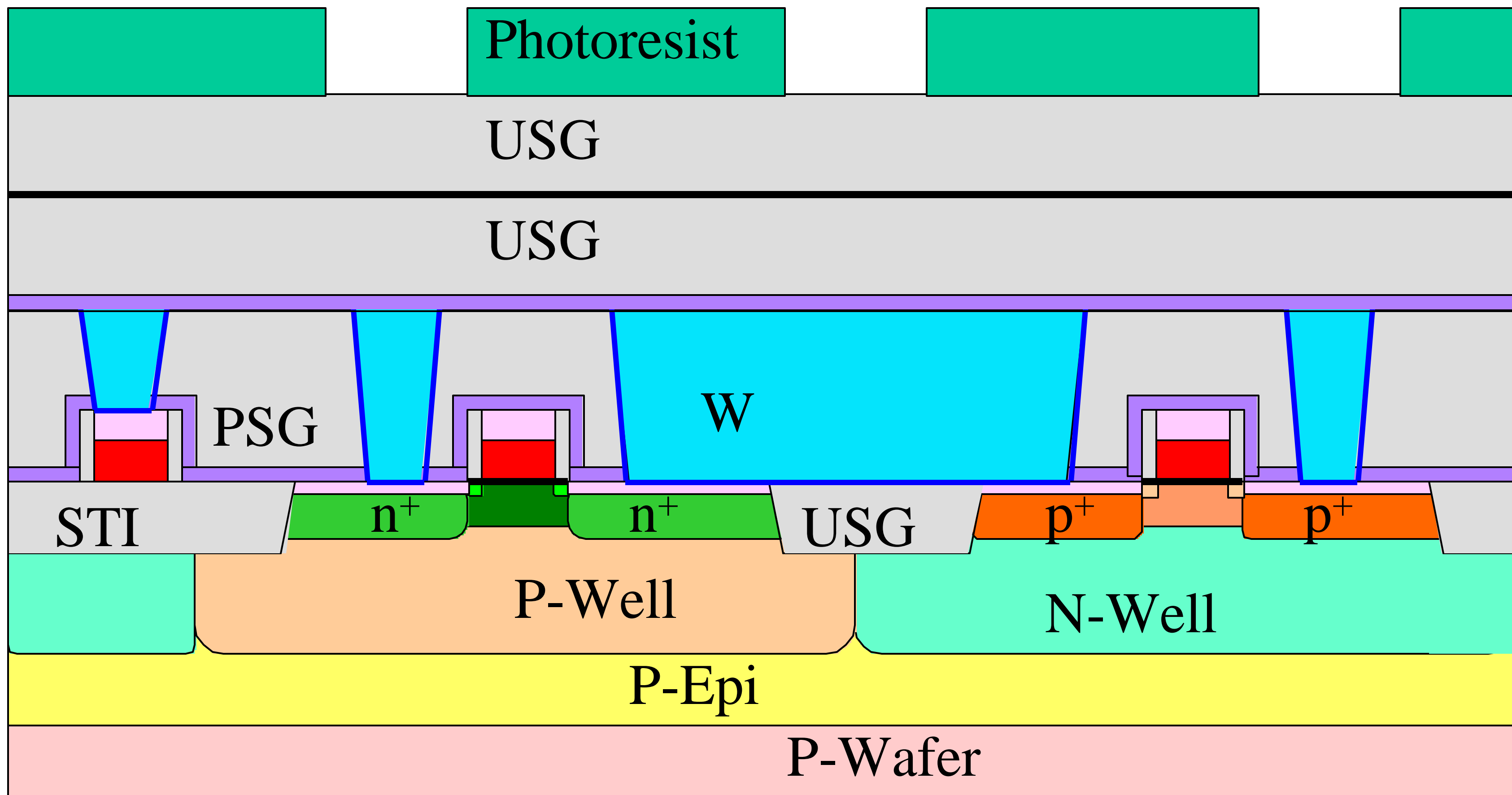
Photoresist Coating



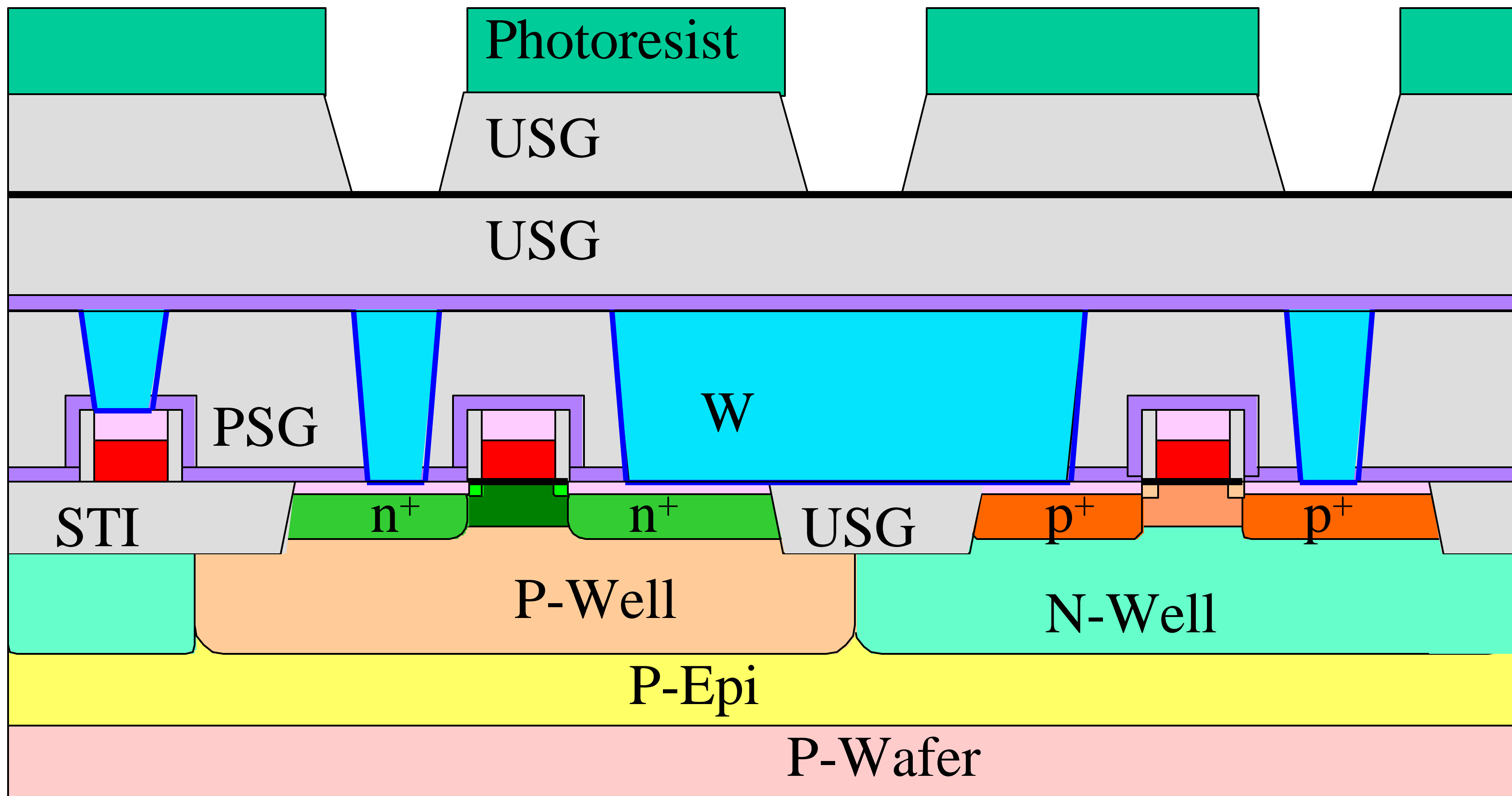
Via 1 Mask



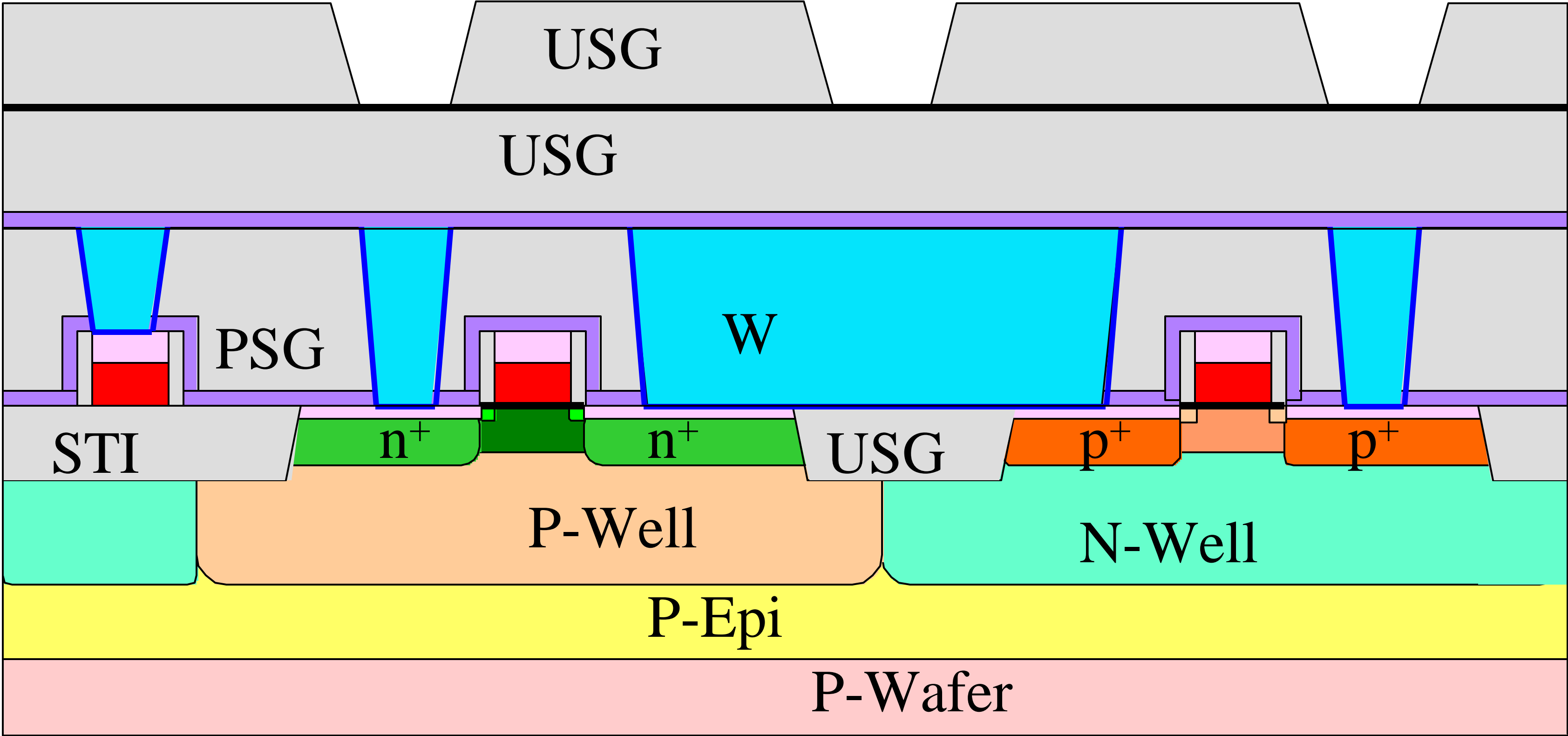
Via 1 Mask Exposure and Development



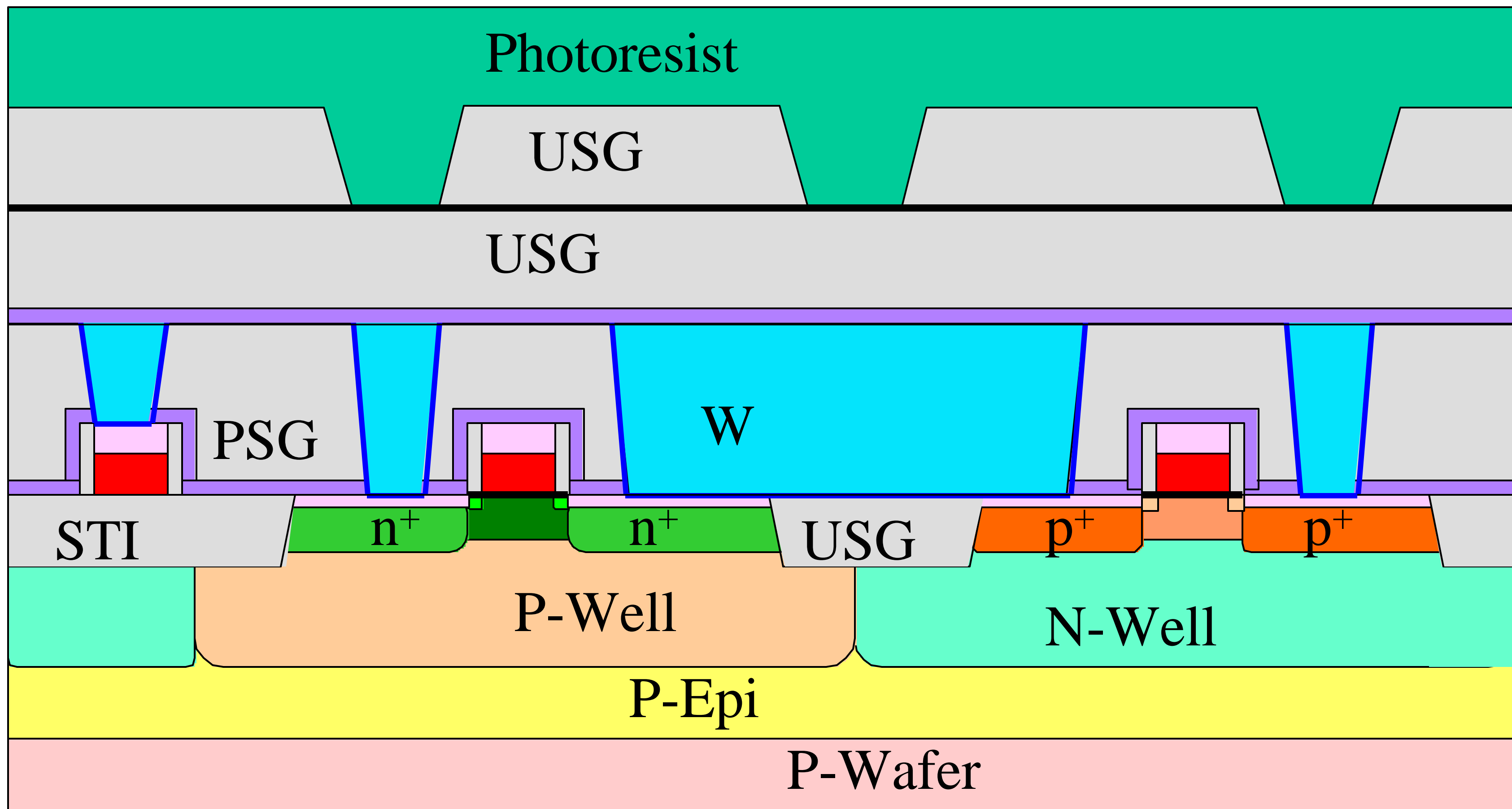
Etch USG, Stop on Nitride



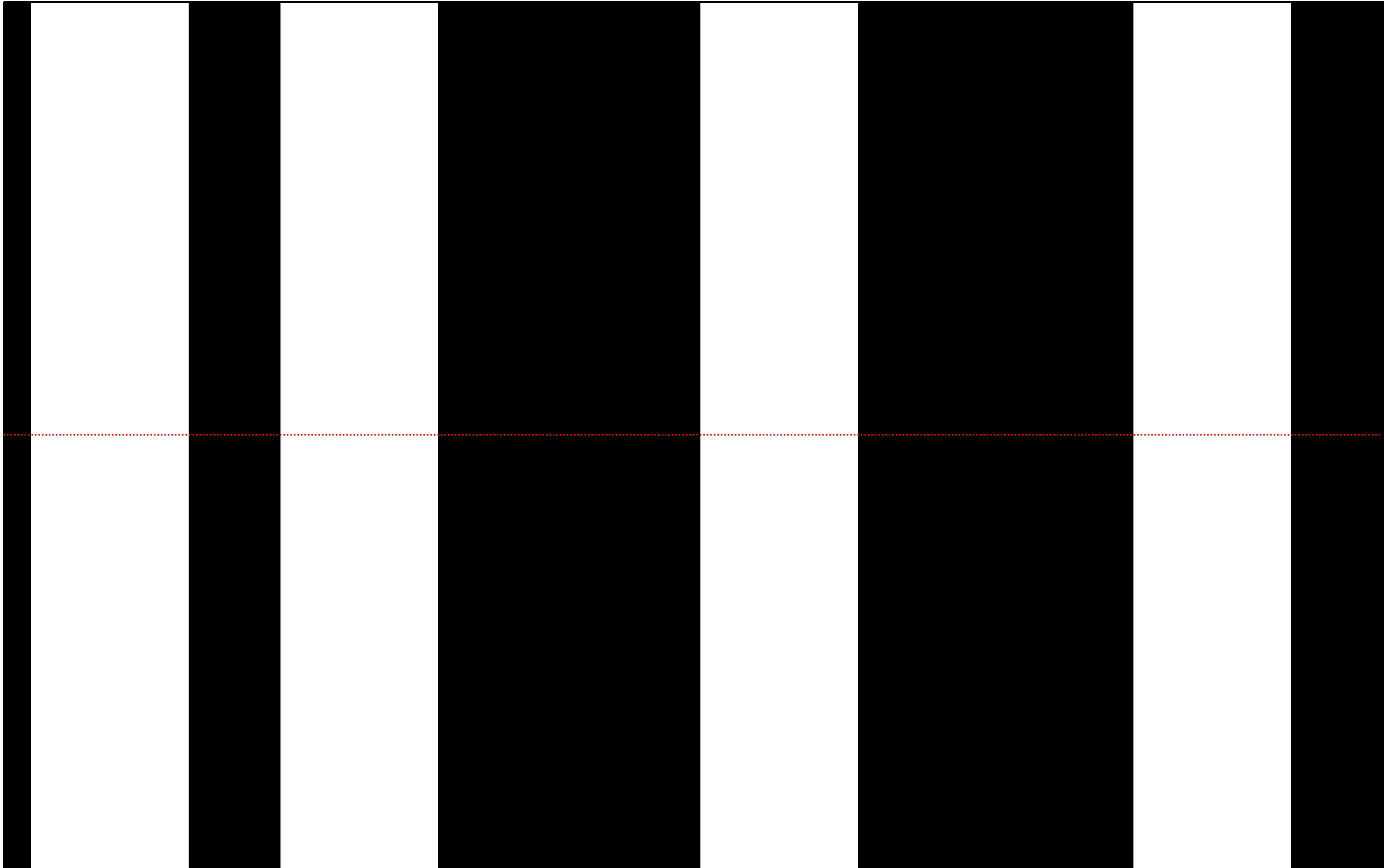
Strip Photoresist



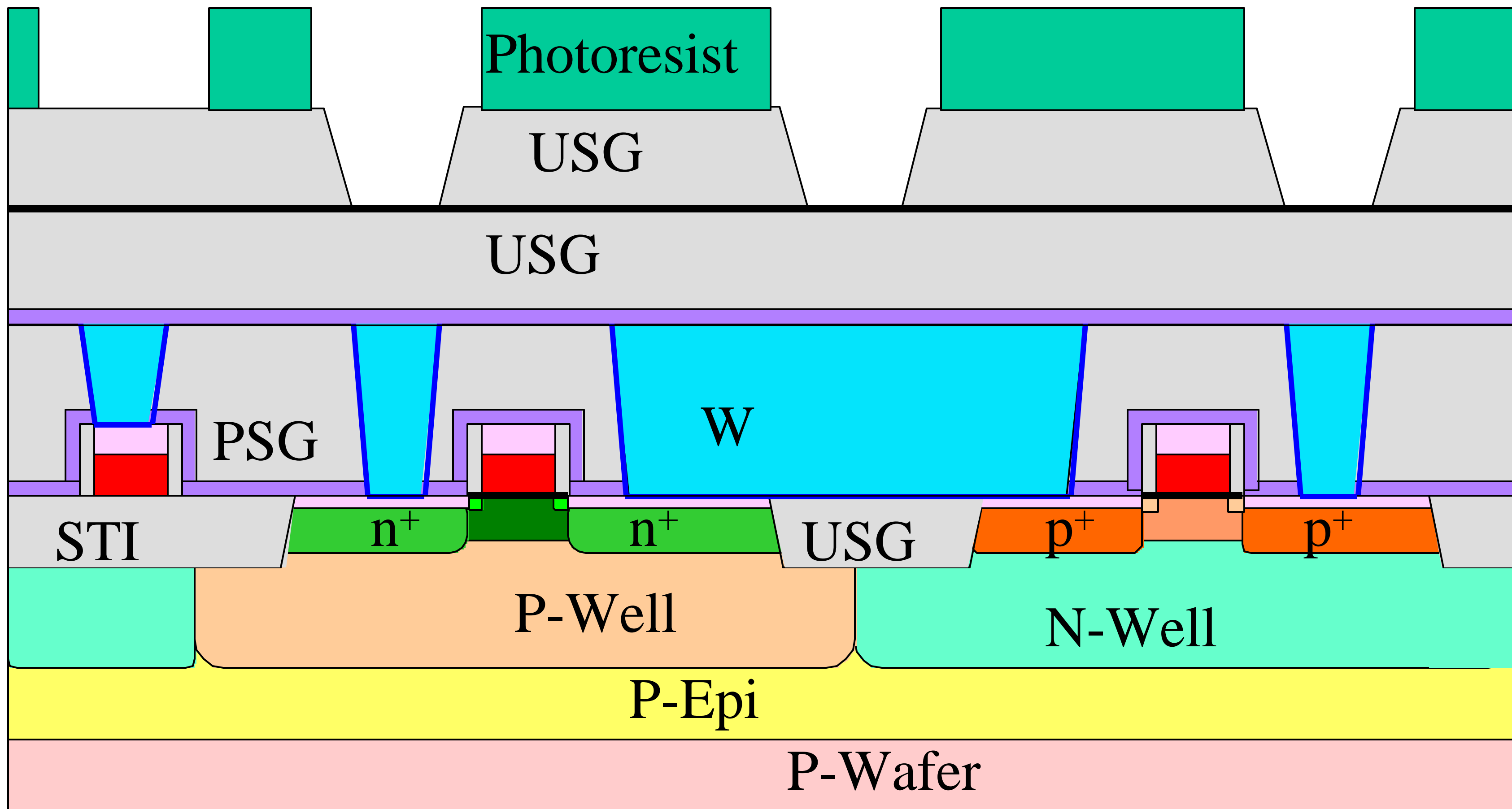
Photoresist Coating



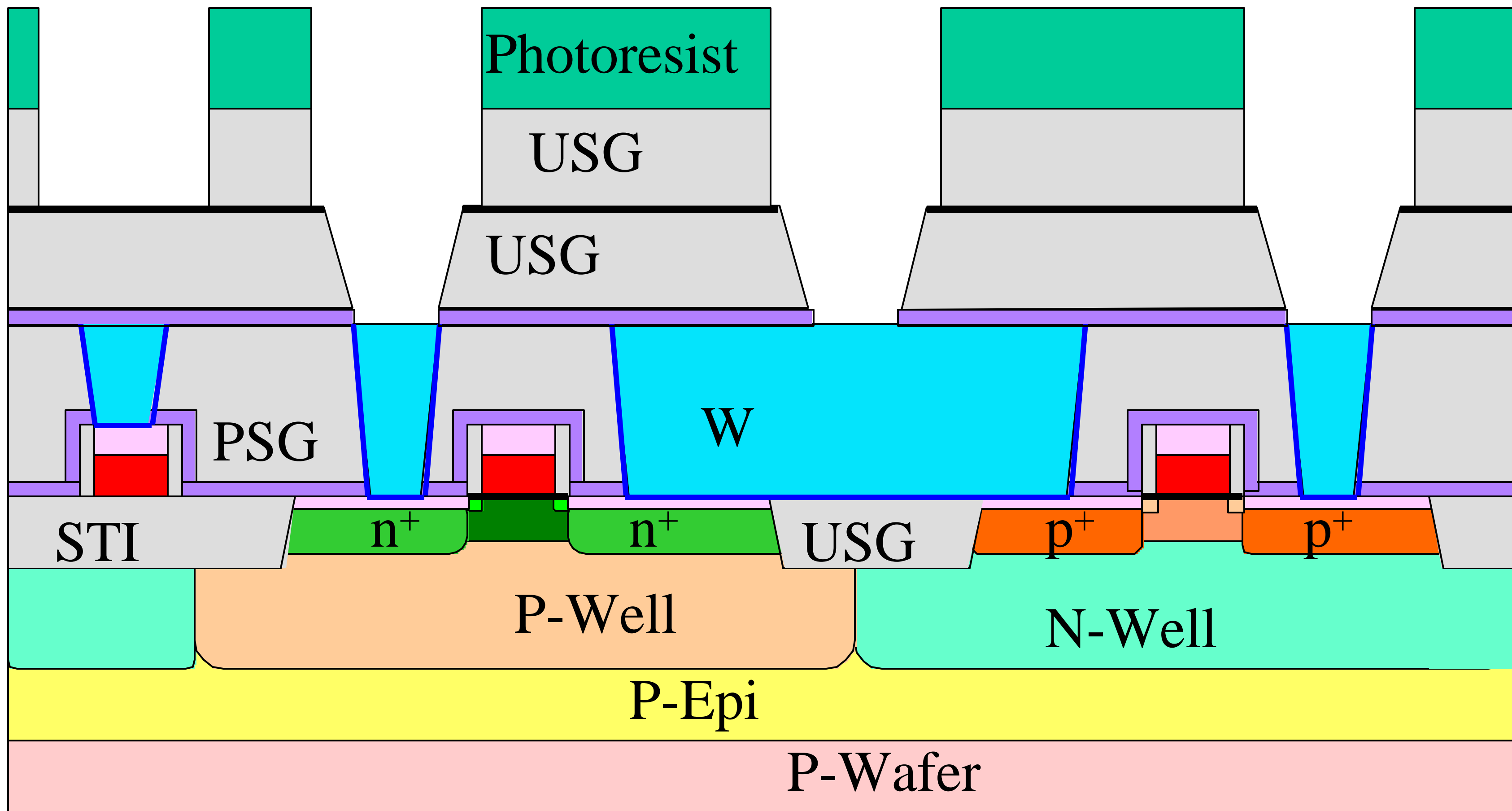
Metal 1 Mask



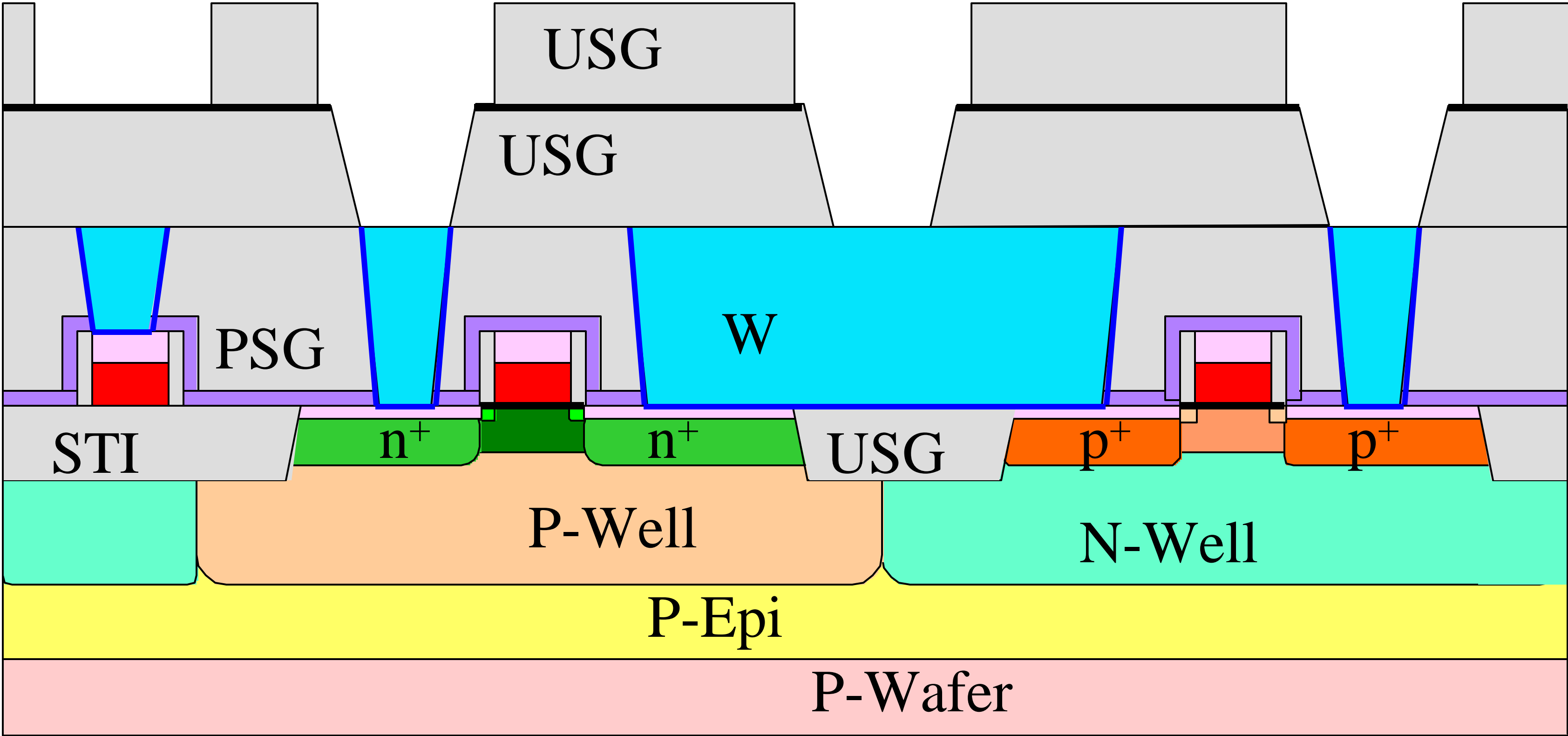
Metal 1 Mask Exposure and Development



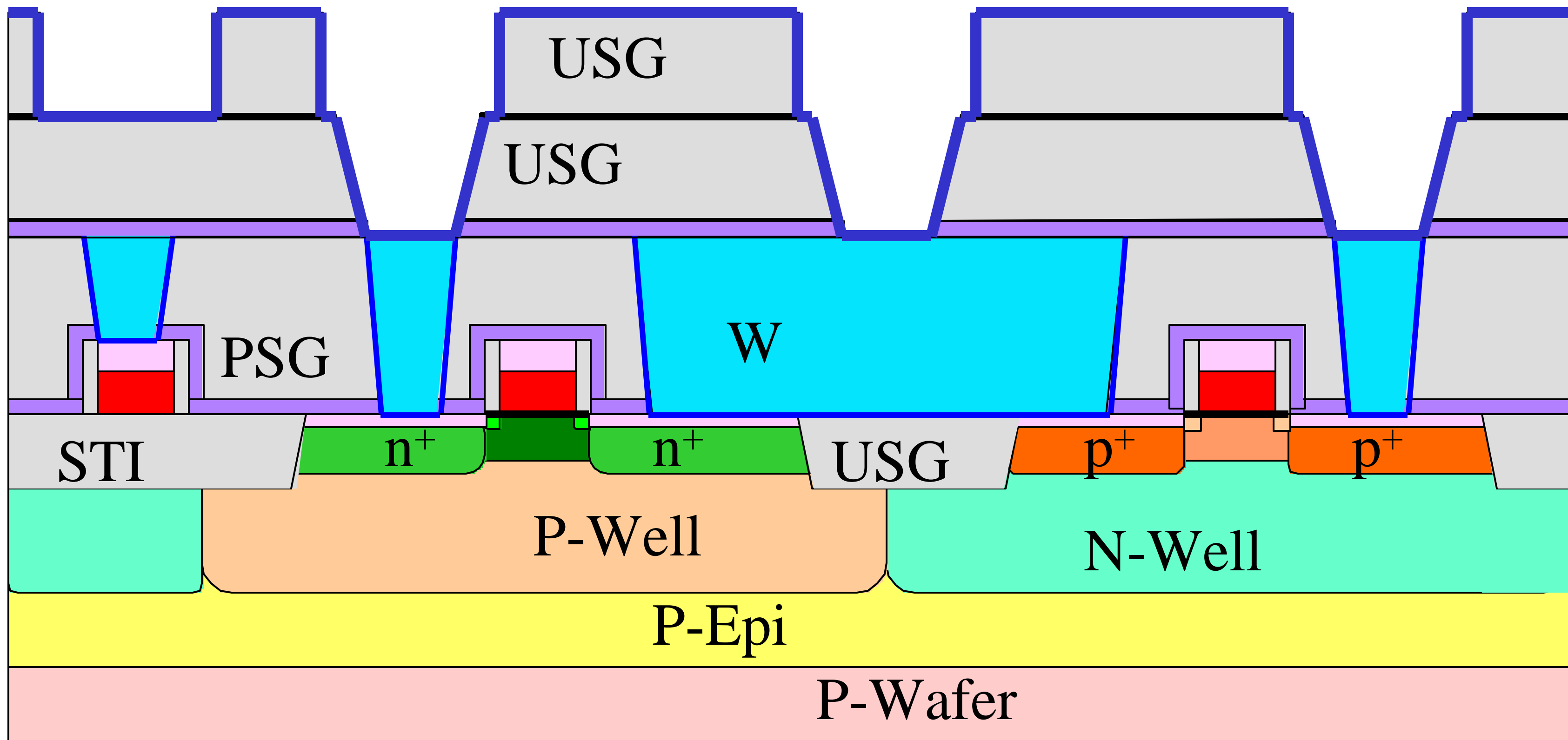
Etch USG and Nitride



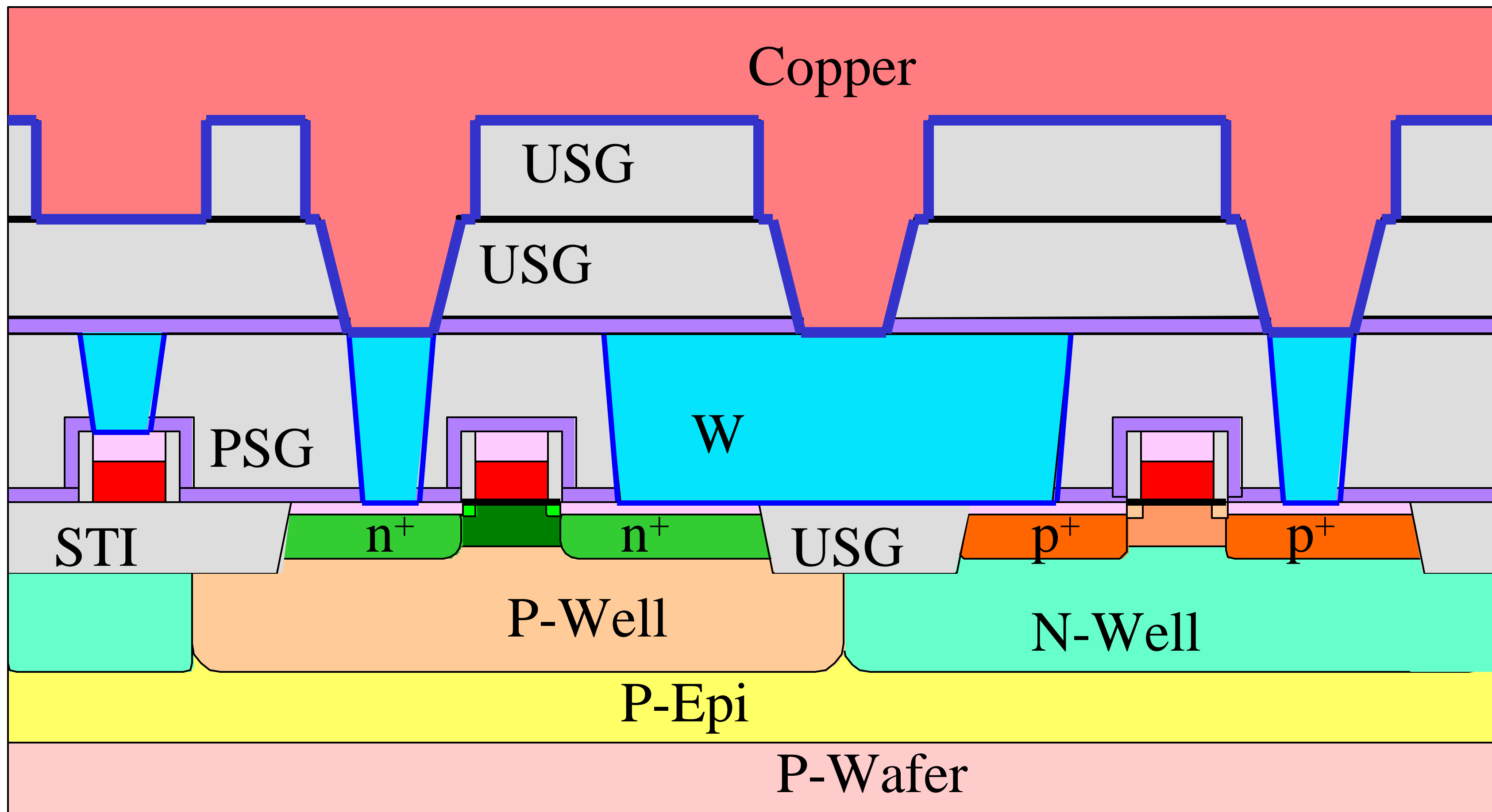
Strip Photoresist



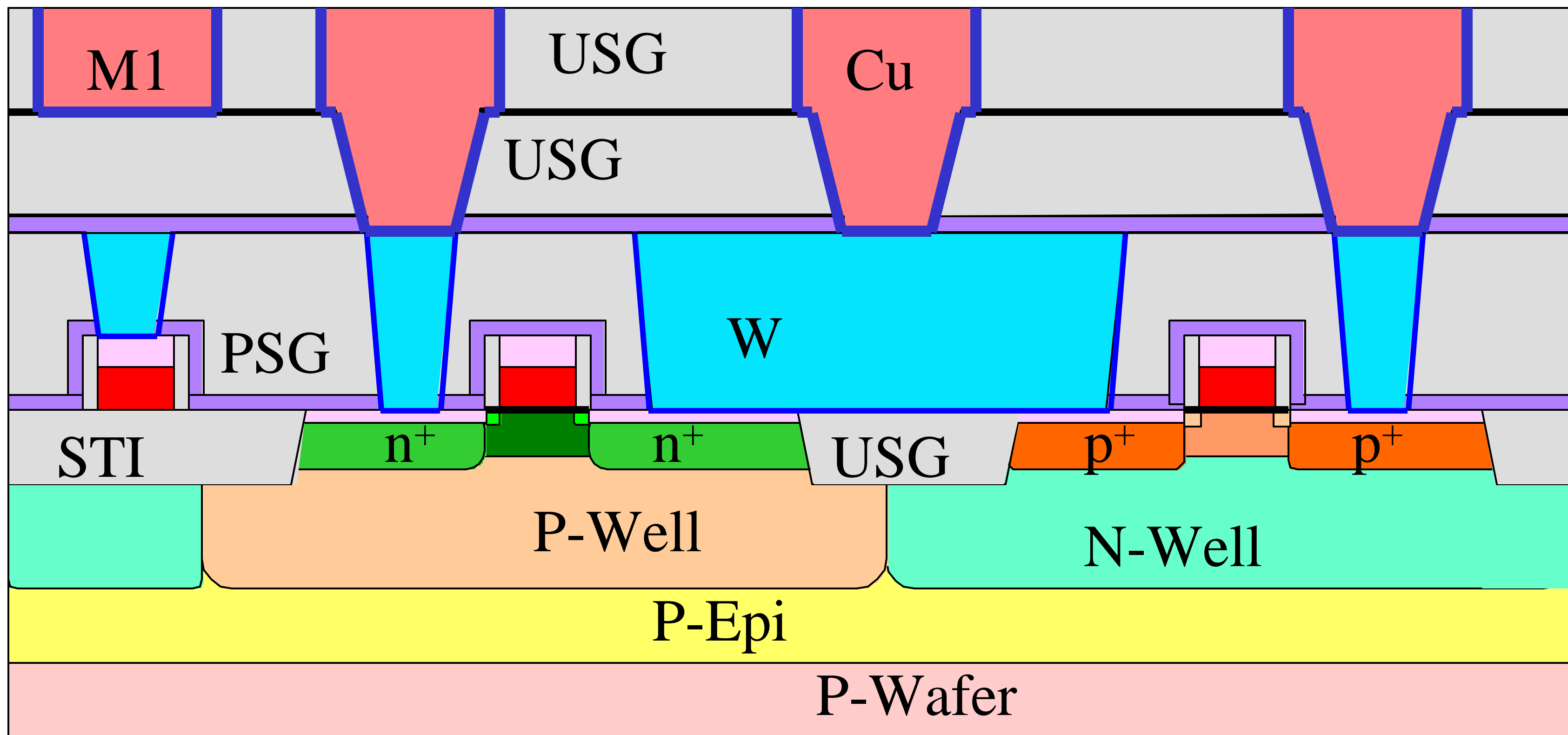
Deposit Tantalum Barrier Layer



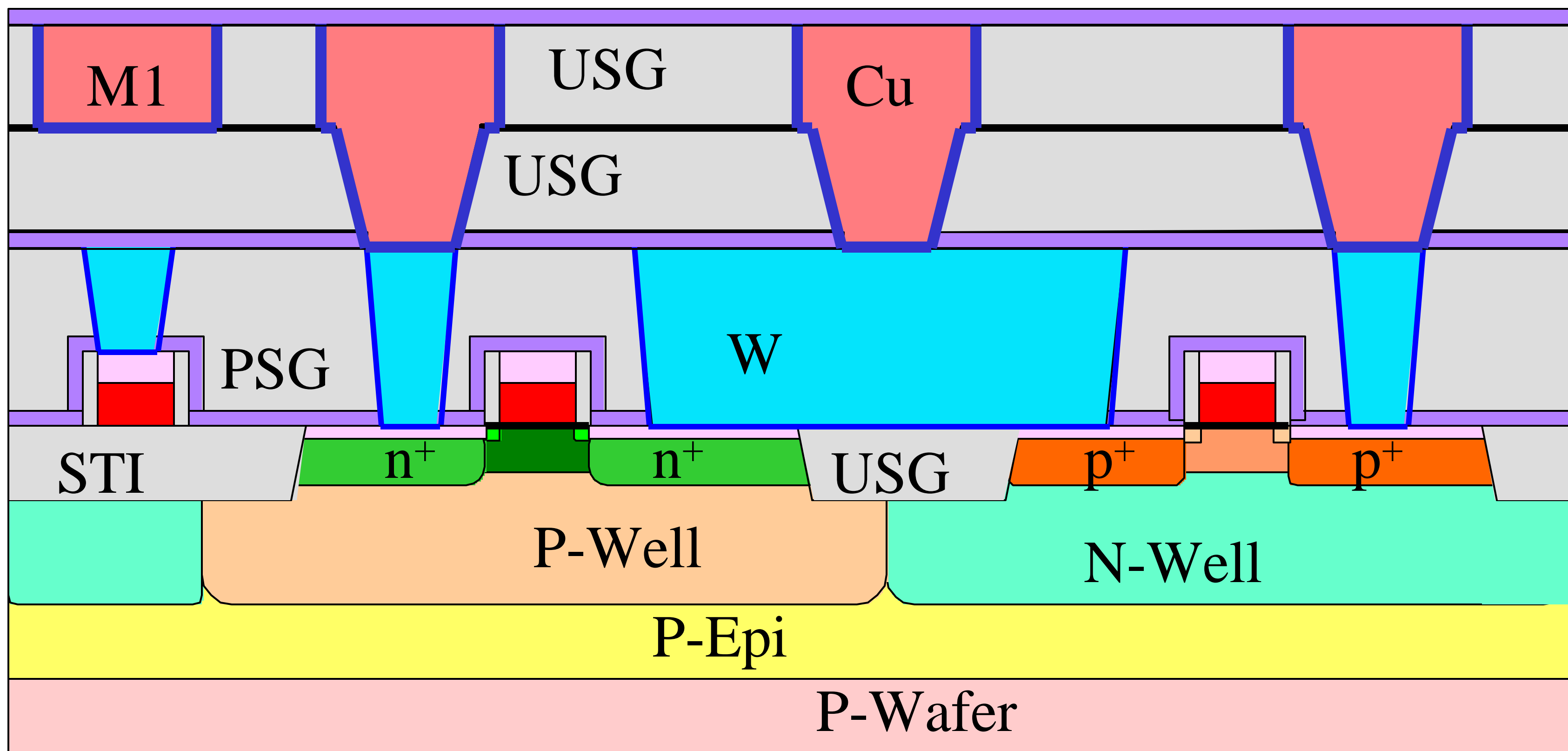
Deposit Copper



CMP Copper and Tantalum



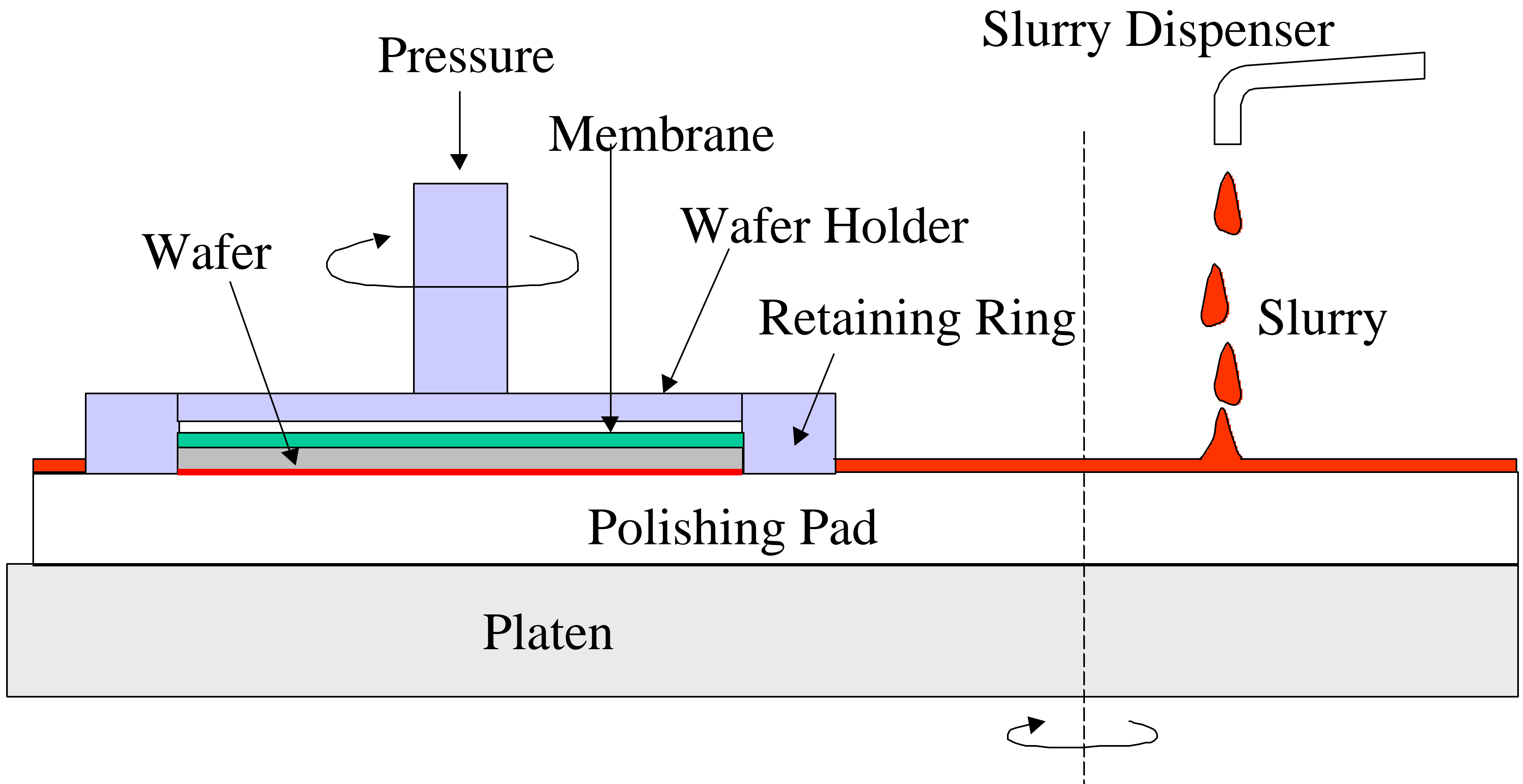
PECVD Seal Nitride



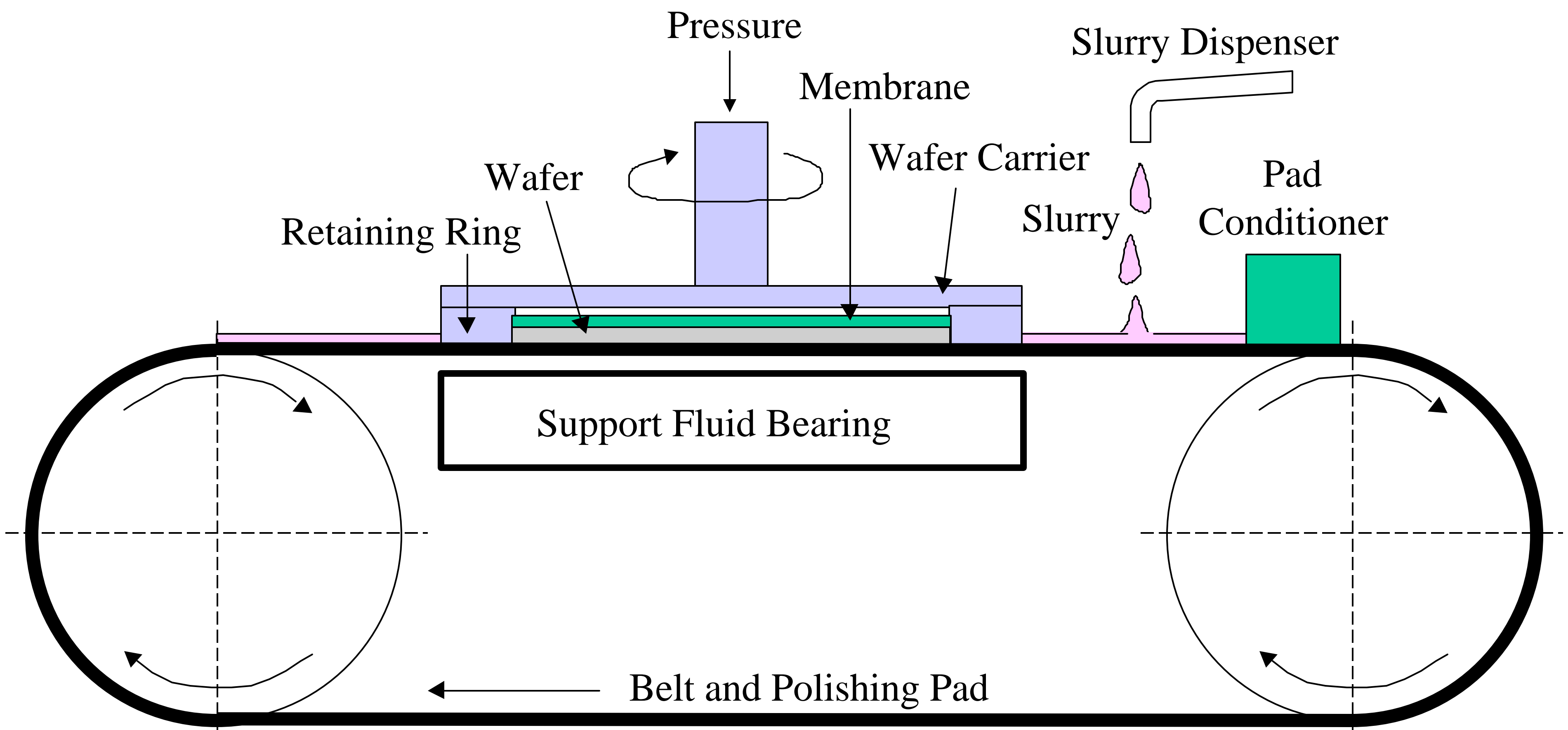
CMP Hardware

- Polishing pad
- Wafer carrier
- Slurry dispenser

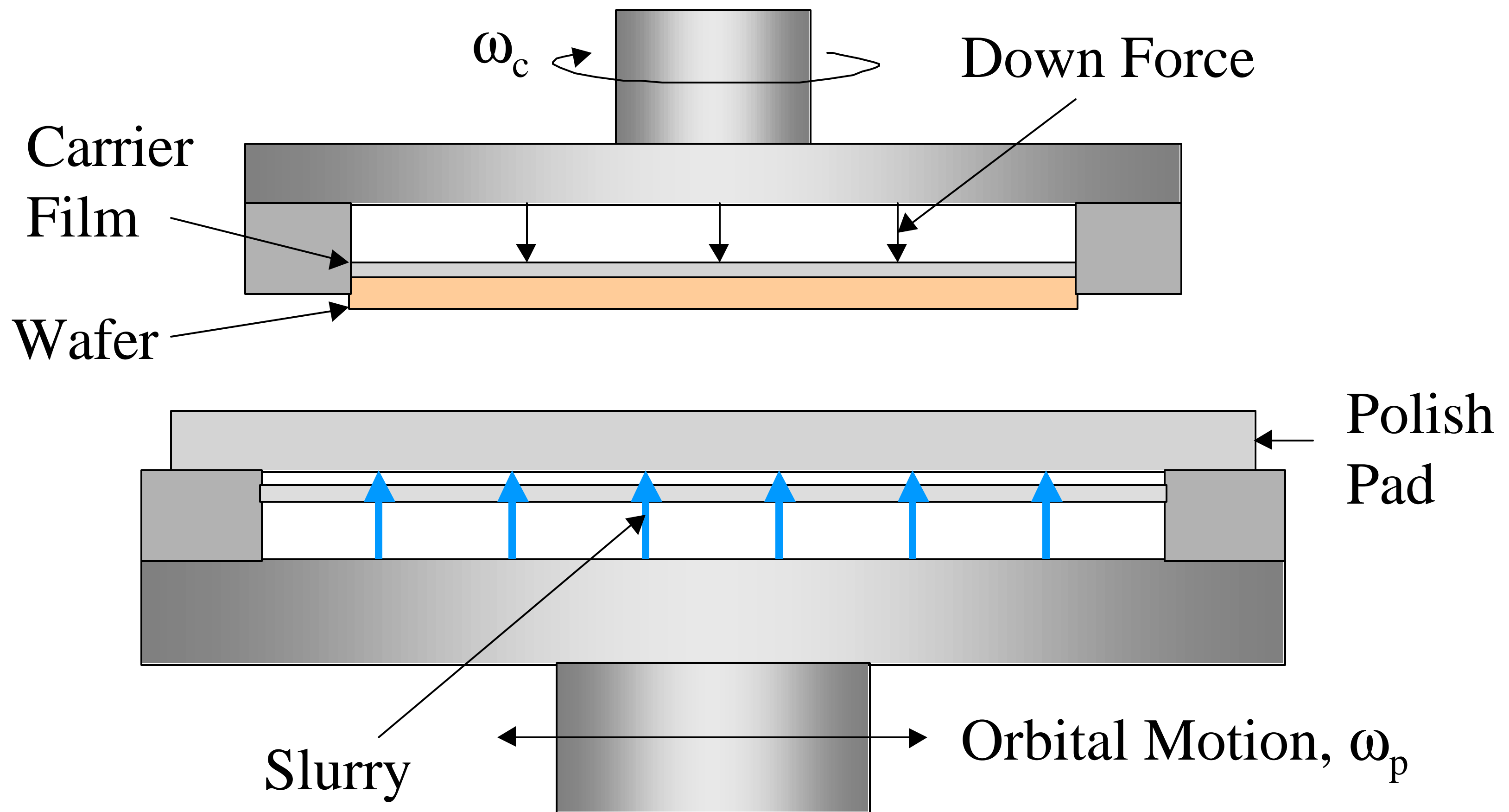
Chemical Mechanical Polishing



Linear Polishing System



Orbital Polishing



Polishing Pad

- Porous, flexible polymer material
  - cast, sliced polyurethane or urethane coated polyester felt
- Pad directly affects quality of CMP process
- Pad materials: durable, reproducible, compressible at process temperature
- Process requirement: high topography selectivity to achieve surface planarization

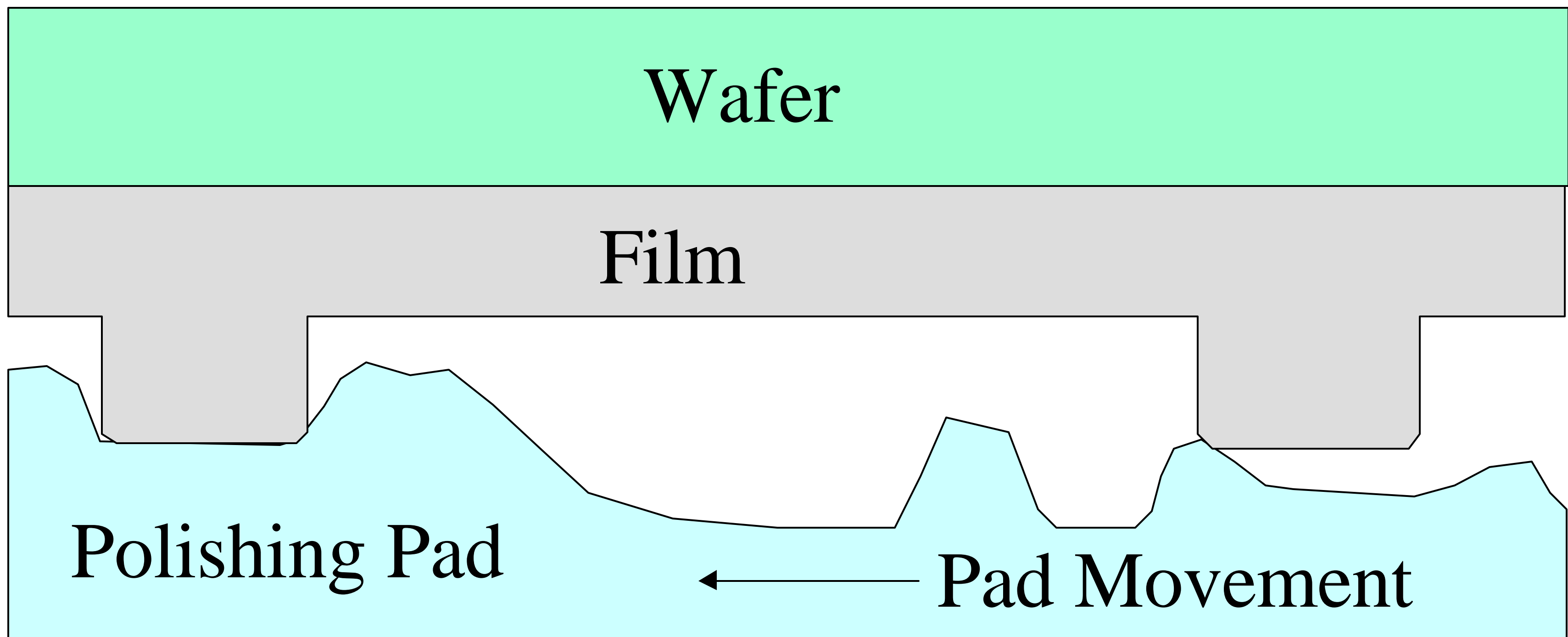
Polishing Pad Hardness

- Harder polishing pad: higher removal rate and better within die (WID) uniformity
- Softer pad: better within wafer (WIW) uniformity.
- Hard pads easier to cause scratches.
- The hardness is controlled by pad chemical compositions or by cellular structure.

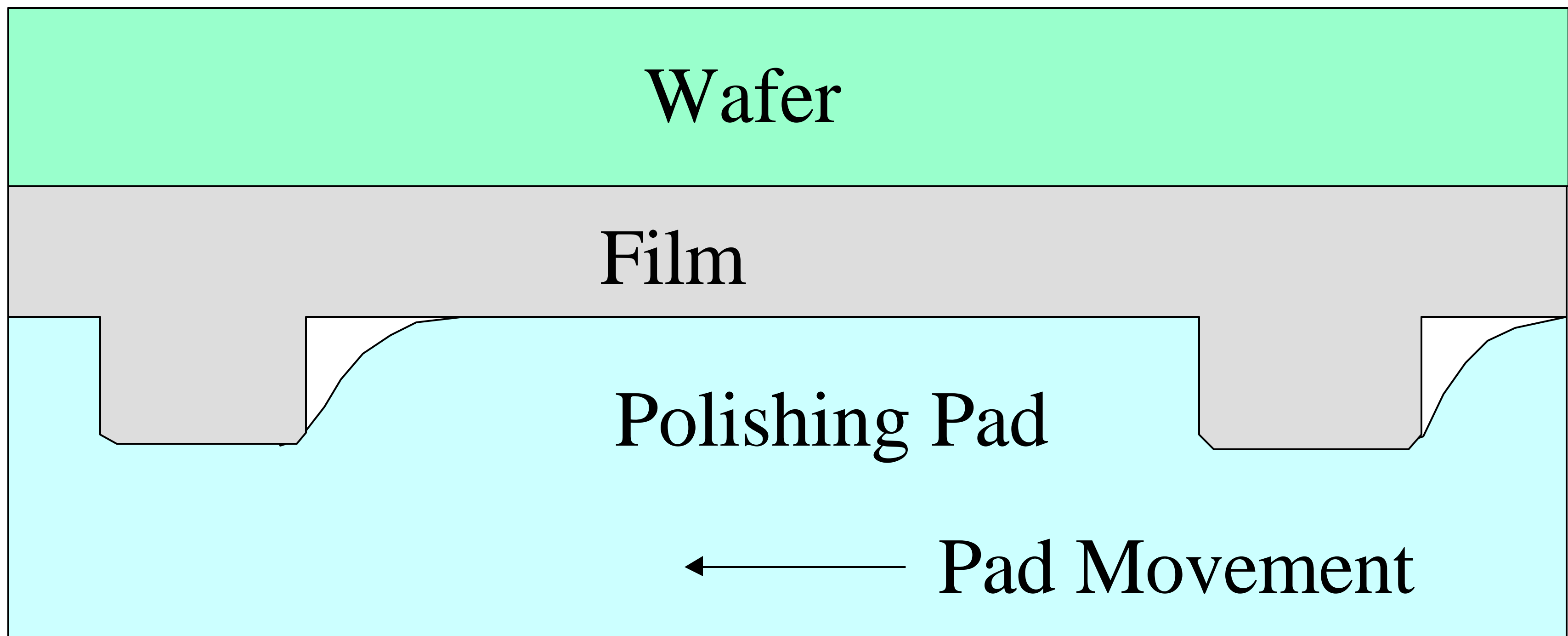
Polishing Pad

- Cells absorb polishing slurry
- Filler improve mechanical properties
- Polishing pad surface roughness determines the conformality range.
  - Smoother pad has poorer topographical selectivity less planarization effect.
  - Rougher pad has longer conformality range and better planarization polishing result

Hard Rough Pad



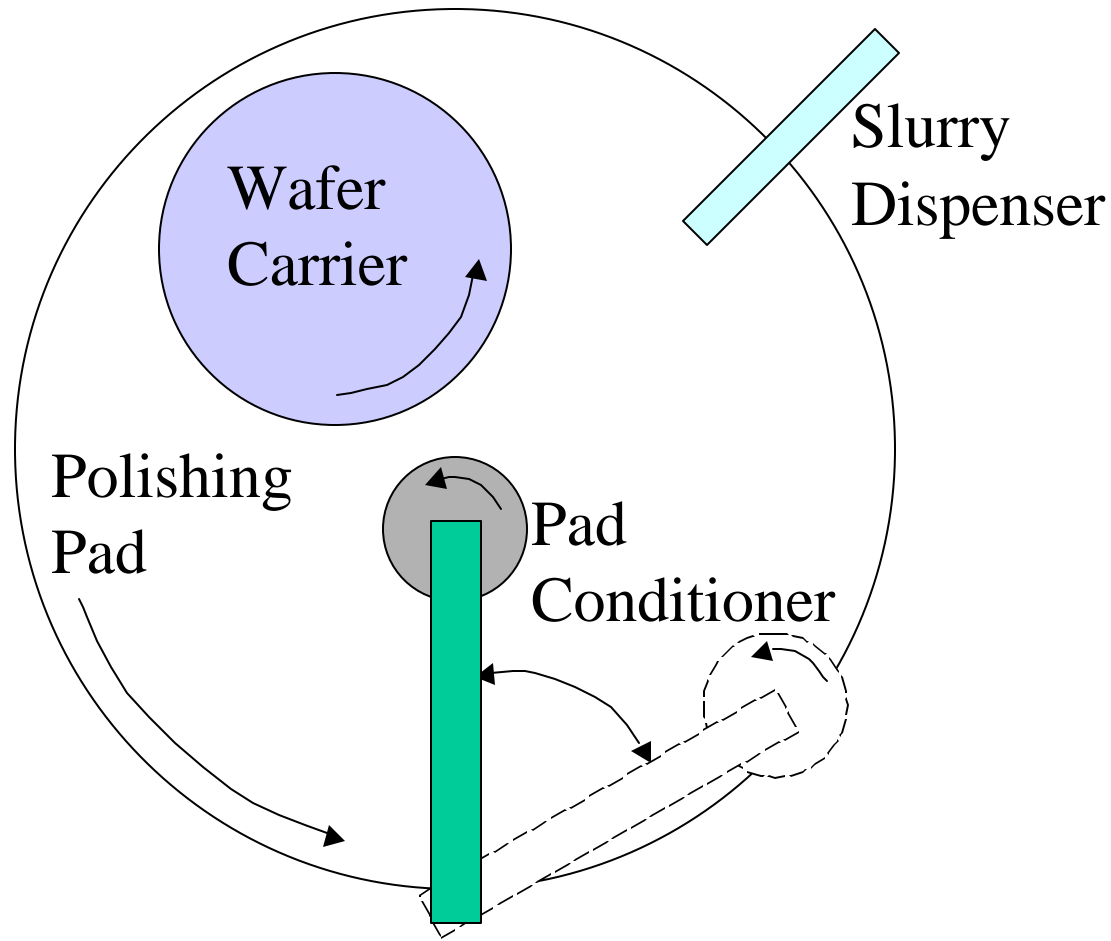
Soft Smooth Pad



Pad Conditioning

- Pad becomes smoother due to the polishing
- Need to recreate rough pad surface
- In-situ pad conditioner for each pad
- The conditioner resurfaces the pad
- Removes the used slurry
- Supplies the surface with fresh slurry

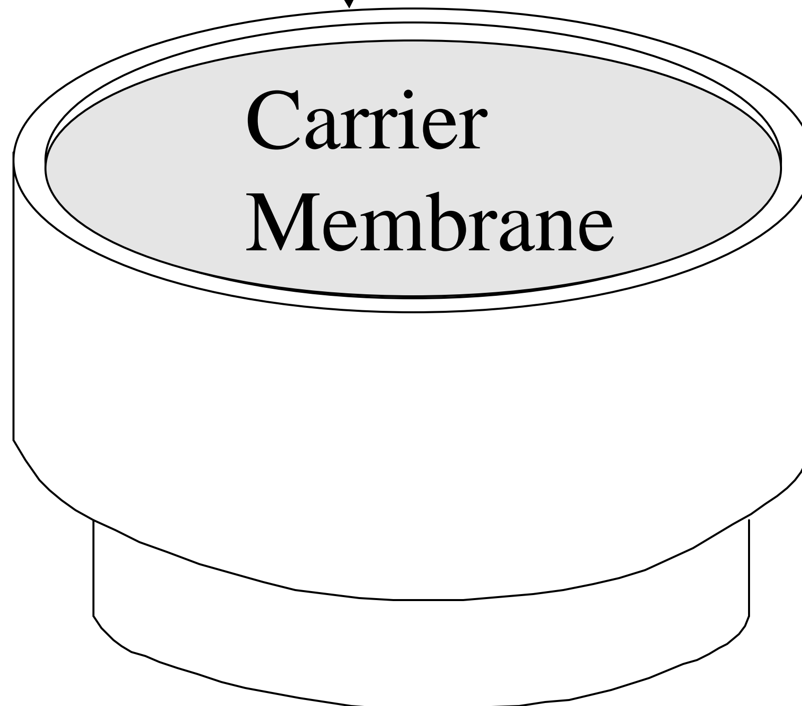
Polishing Pad and Pad Conditioner



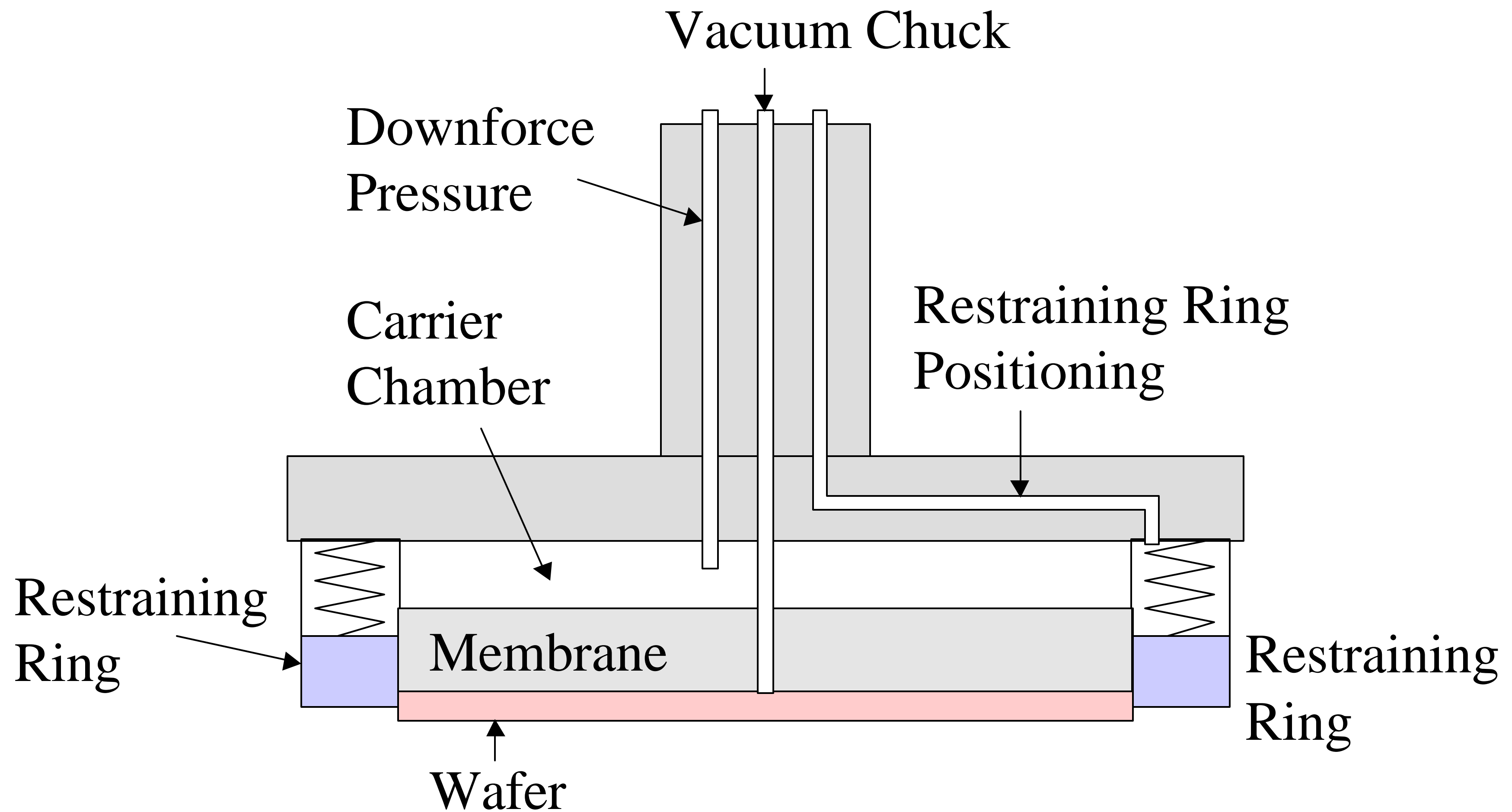
Polishing Head

- Polishing head is also called wafer carrier
- It consists of a polishing head body
- Retaining ring
- Carrier membrane
- Down force driving system

Polishing Head



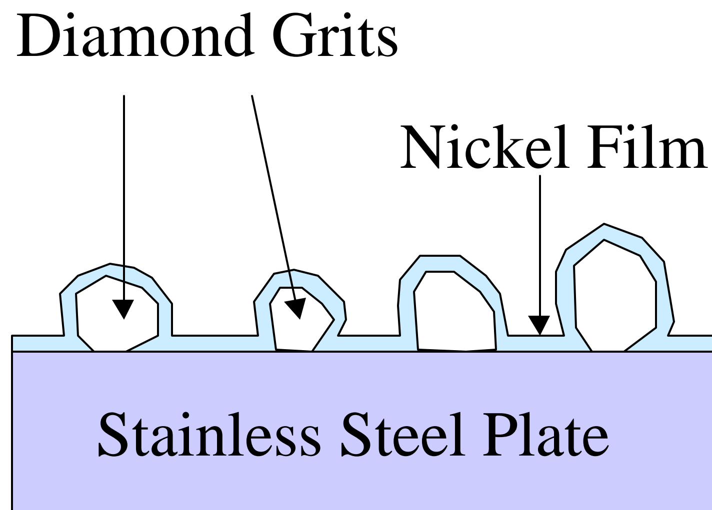
Schematic of Polishing Head



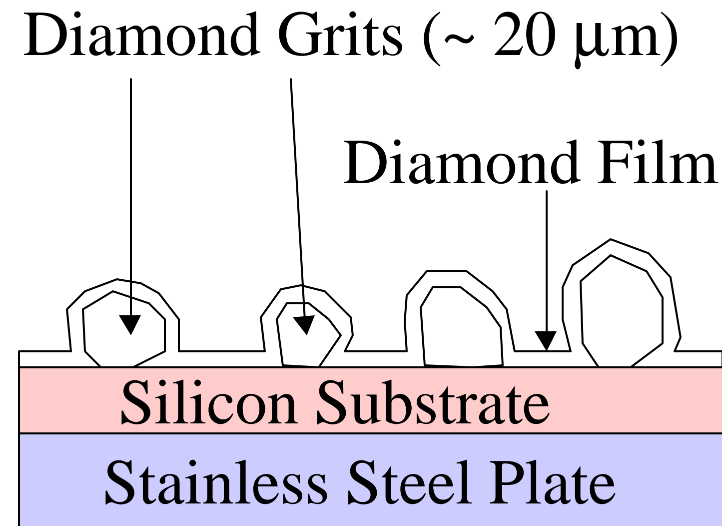
Pad Conditioner

- Sweeps across the pad to increase surface roughness required by planarization and removes the used slurry
- Conditioner is a stainless steel plate coated with nickel-plated diamond grits
- Diabond CMP conditioner: stainless steel plate coated with CVD diamond film plated diamond grids

Surface of CMP Conditioners



Conventional



Diabond

CMP Slurries

- Chemicals in the slurry react with surface materials, form chemical compounds that can be removed by abrasive particles
- Particulate in slurry mechanically abrade the wafer surface and remove materials
- Additives in CMP slurries help to achieve desired polishing results

CMP Slurries

- CMP slurries work just like toothpaste
- Chemicals kill gems, remove tartar, and form protection layer on the teeth
- Particles abrade away unwanted coating from tooth surface during tooth brushing

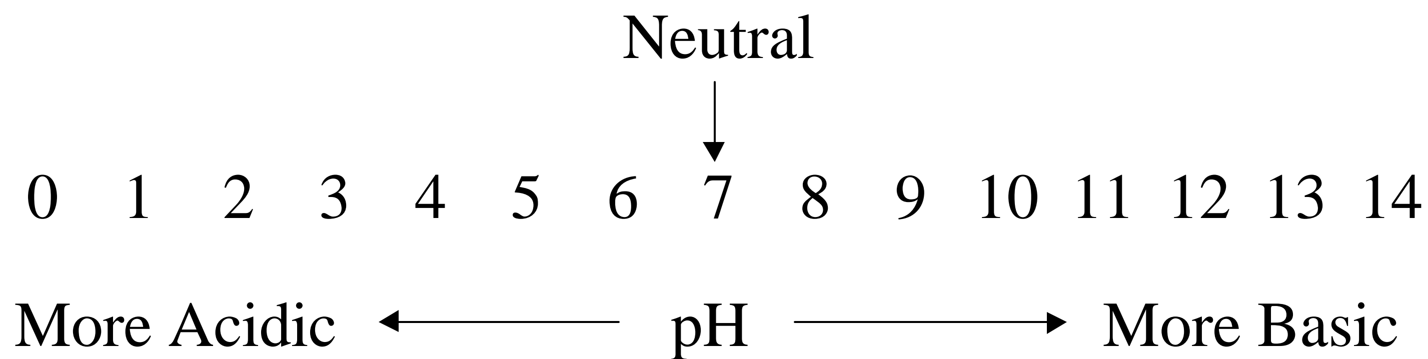
CMP Slurries

- Water-based chemicals with abrasive particles and chemical additives
- Different polishing processes require different slurries
- Slurry can impact removal rate, selectivity, planarity and uniformity
- Slurries always are engineered and formulated for a specific application.

CMP Slurries

- Oxide slurry: alkaline solution with silica
- Metal slurry: acidic solution with alumina
- Additives control the pH value of slurries
  - oxide, pH at 10 to 12
  - metal, pH at 6 to 2

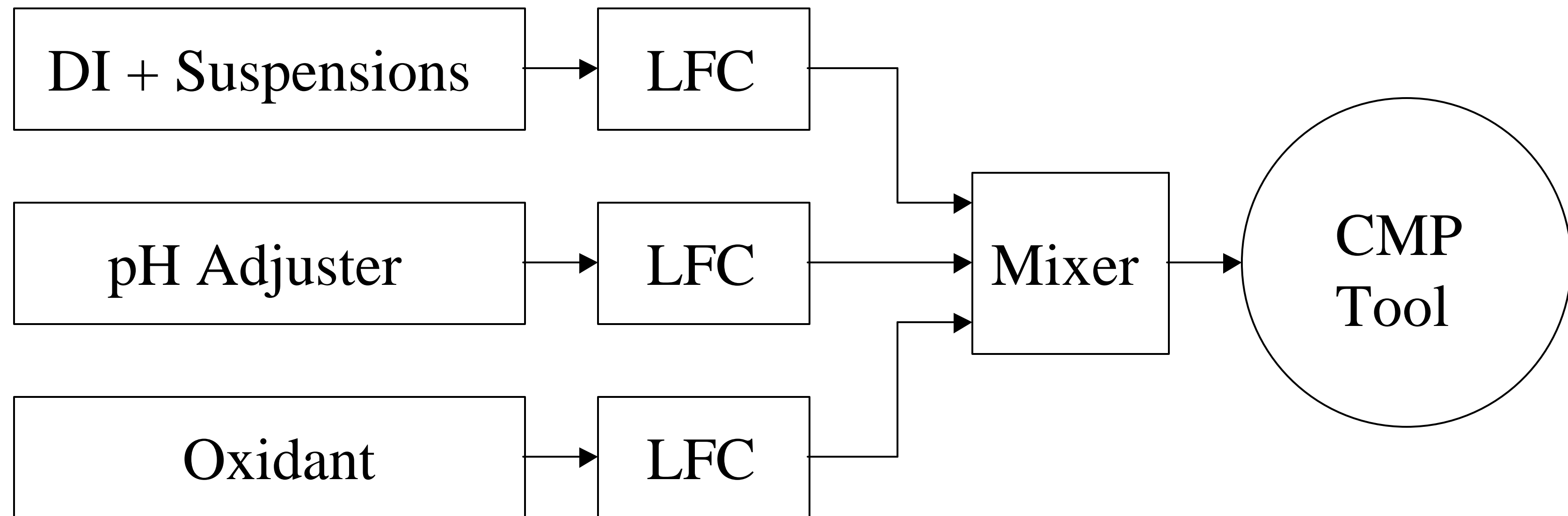
pH Values



Slurry Delivery

- Slurry components are stored separately
  - DI water with particulate
  - additives for pH control
  - oxidants for metal oxidation
- Flow to a mixer to mix at required ratio

Slurry Flow



LFC: liquid flow controller

Oxide Slurry

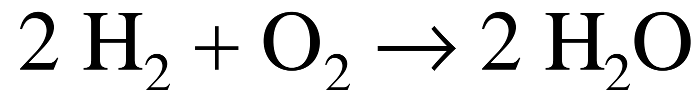
- Based on experience of optical industry, which polish silicate glass to make lenses and mirrors for a long time
- Oxide slurry is a colloidal suspension of fine fumed silica (SiO_2) particles in water
- KOH is used to adjust the pH at 10 to 12
- NH_4OH can also be used

Oxide Slurry

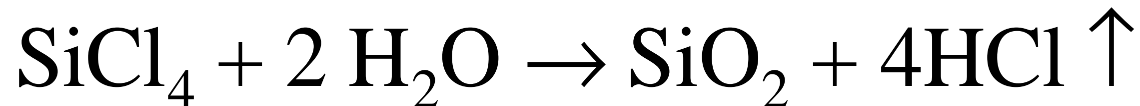
- Abrasives: fumed silica particles
- Normally contain ~ 10% solids
- Shelf lifetime of up to 1 year with proper temperature control

Fumed Silica

- Fumed silica particles are formed in a vapor phase hydrolysis of $SiCl_4$ in a hydrogen-oxygen flame

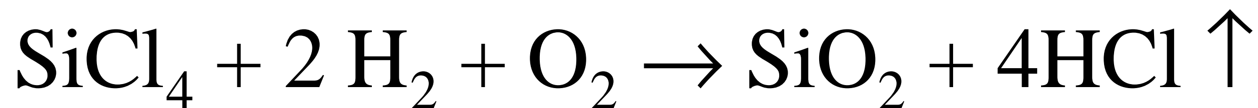


$$2\ H_2 + O_2 \rightarrow 2\ H_2O$$



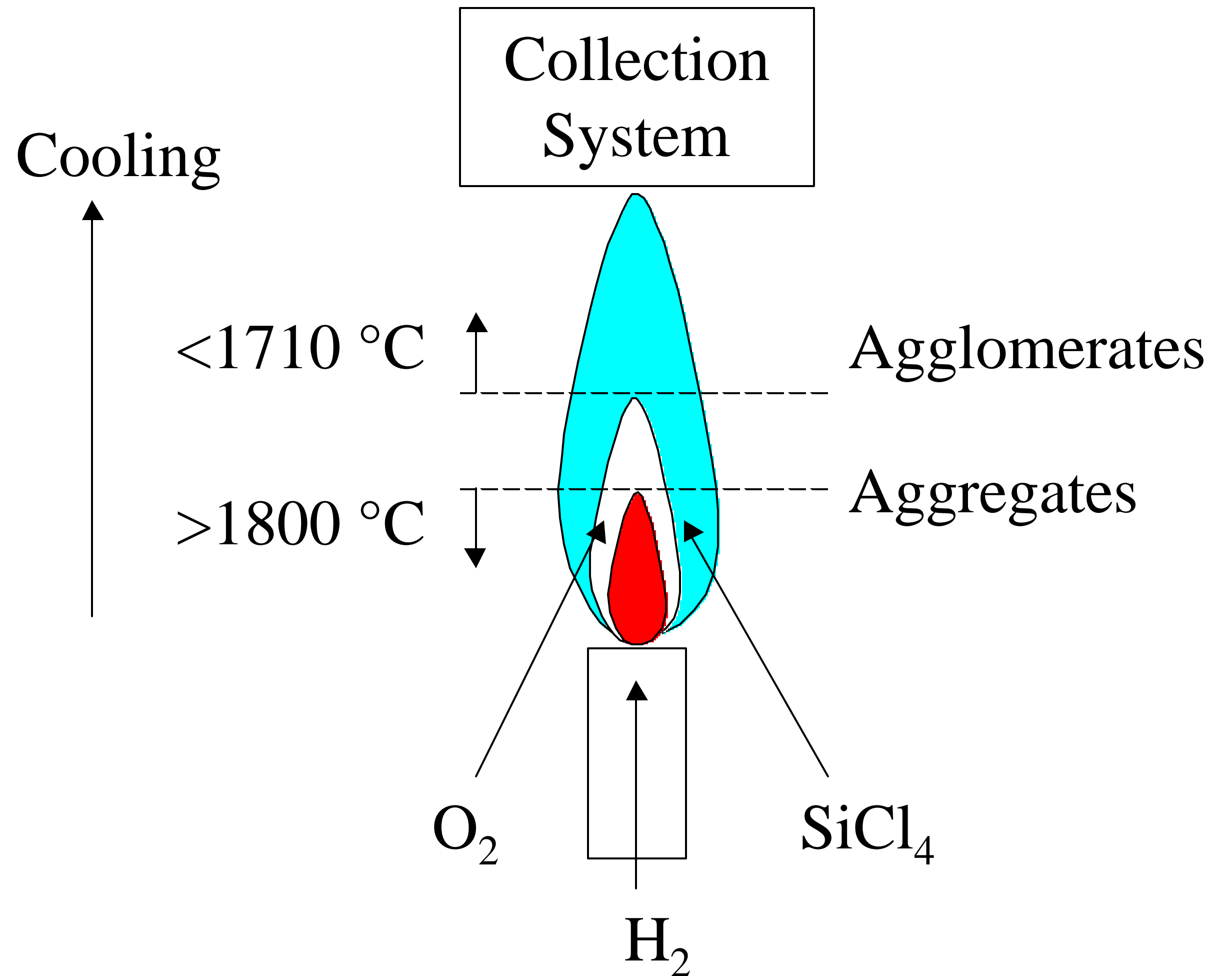
$$SiCl_4 + 2\ H_2O \rightarrow SiO_2 + 4HCl \uparrow$$

- Overall reaction

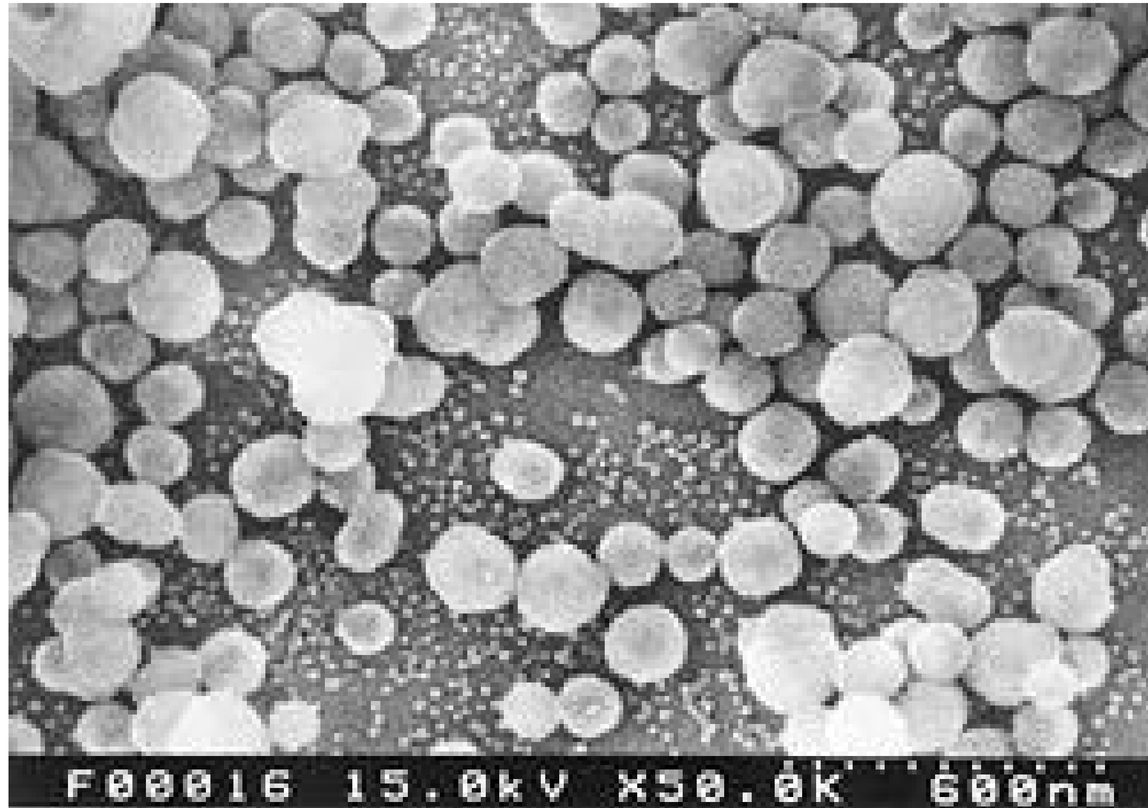


$$SiCl_4 + 2\ H_2 + O_2 \rightarrow SiO_2 + 4HCl \uparrow$$

Fumed Silica Particle Formation



Fumed Silica Particles



Courtesy of Fujimi Corporation

Metal Polishing Slurry

- Metal CMP process is similar to the metal wet etch process
  - Oxidant reacts with metal to form oxide
  - Metal oxide is removed
  - Repeat metal oxidation and oxide removal

Metal Polishing Slurry

- The metal CMP slurries usually are pH-adjusted suspensions of alumina (Al_2O_3)
- The slurry pH controls the two competing metal removal mechanisms
  - metal corrosive wet etching
  - metal oxidation passivation

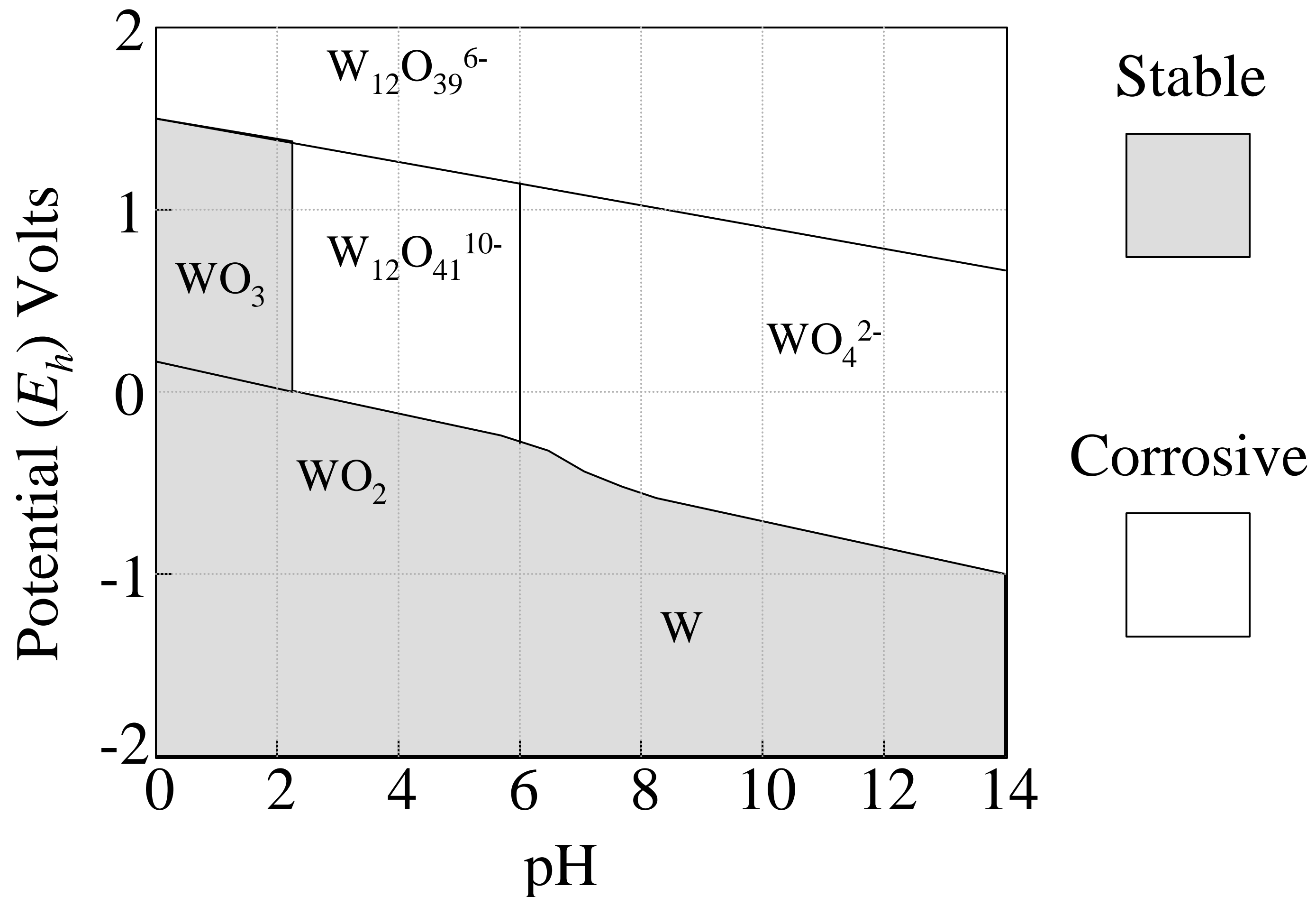
Metal Polishing Slurry

- Different metal oxides have different solubility
- If oxide is soluble, wet etch will dominate
  - Not favored: isotropic with no topographic selectivity
- If oxide is insoluble, it blocks further oxidation
  - Particles mechanically abrade oxide layer
  - Repeating metal oxidation and oxide abrasion
  - favorable: high surface topographic selectivity
- The pH value controls oxidation process

Tungsten Slurry

- Pourbaix diagram
- When pH < 2, tungsten is in passivation regime
- Tungsten can form passivation oxide WO_3 with pH lower than 4 in the presence of an oxidant
  - Oxidants: potassium ferricyanid ($K_3Fe(CN)_6$), ferric nitrade ($Fe(NO_3)_3$), and H_2O_2
- For a higher pH, the soluble $W_{12}O_{41}^{10-}$, WO_4^{2-}, and $W_{12}O_{39}^{6-}$ ions can be formed, cause wet etch

Pourbaix Diagram for Tungsten



Tungsten Slurry

- Adjusting slurry pH allows low wet etch rates and chemical-mechanical polish removal
- Tungsten slurries normally are quite acidic with pH level from 4 to 2.
- Tungsten slurries have lower solid contents and much shorter shelf lifetime.
- Tungsten slurries require mechanical agitation prior to and during delivery to the CMP tools

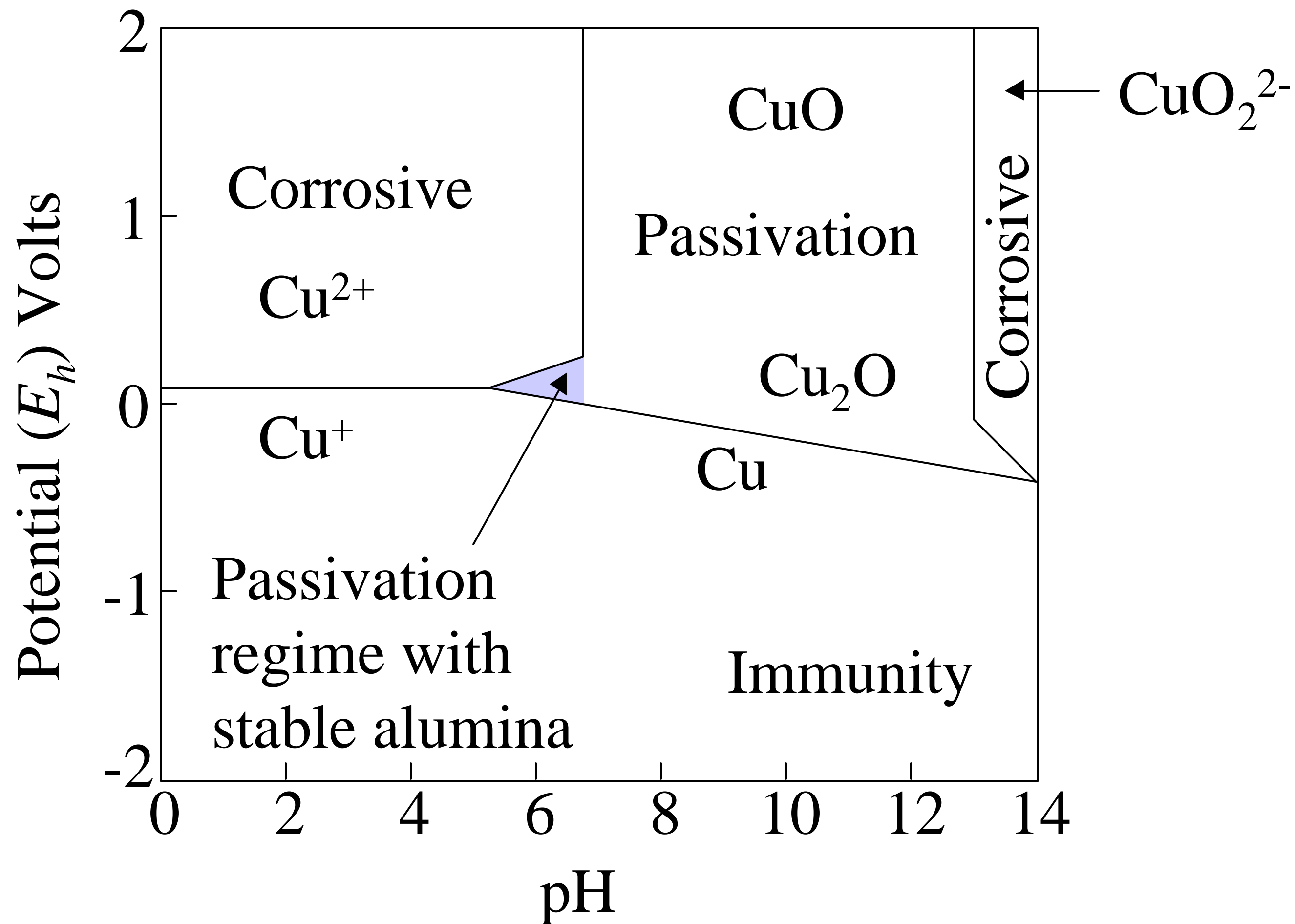
Aluminum Slurry

- Water-based acidic solutions
- H_2O_2 as oxidant,
- Alumina as abrasives.
- Limited shelf lifetime
- H_2O_2 molecule is unstable
- Aluminum CMP is not popularly used
  - Hard to compete with copper metallization

Copper Slurry

- Acidic solutions
- Oxidants: hydrogen peroxide (H_2O_2), ethanol (HOC_2H_5) with nitric acid (HNO_4), ammonium hydroxide (NH_4OH) with potassium ferri- and ferro-cyanide, or nitric acid with benzotriazole
- Alumina as abrasives

Pourbaix Diagram for Copper



Copper Slurry

- Need colloidally stable slurry to achieve consistent polishing process results
- A colloidally stable alumina suspension can be achieved at pH just below 7.
- Only a small window for copper slurries to achieve both electrochemical passivation and colloidally stable suspension of aqueous alumina particles

CMP Basics

- Removal rate
- Uniformity
- Selectivity
- Defects

Removal Rate

- Mechanical removal rate R was found by Preston
- The Preston equation can be expressed as

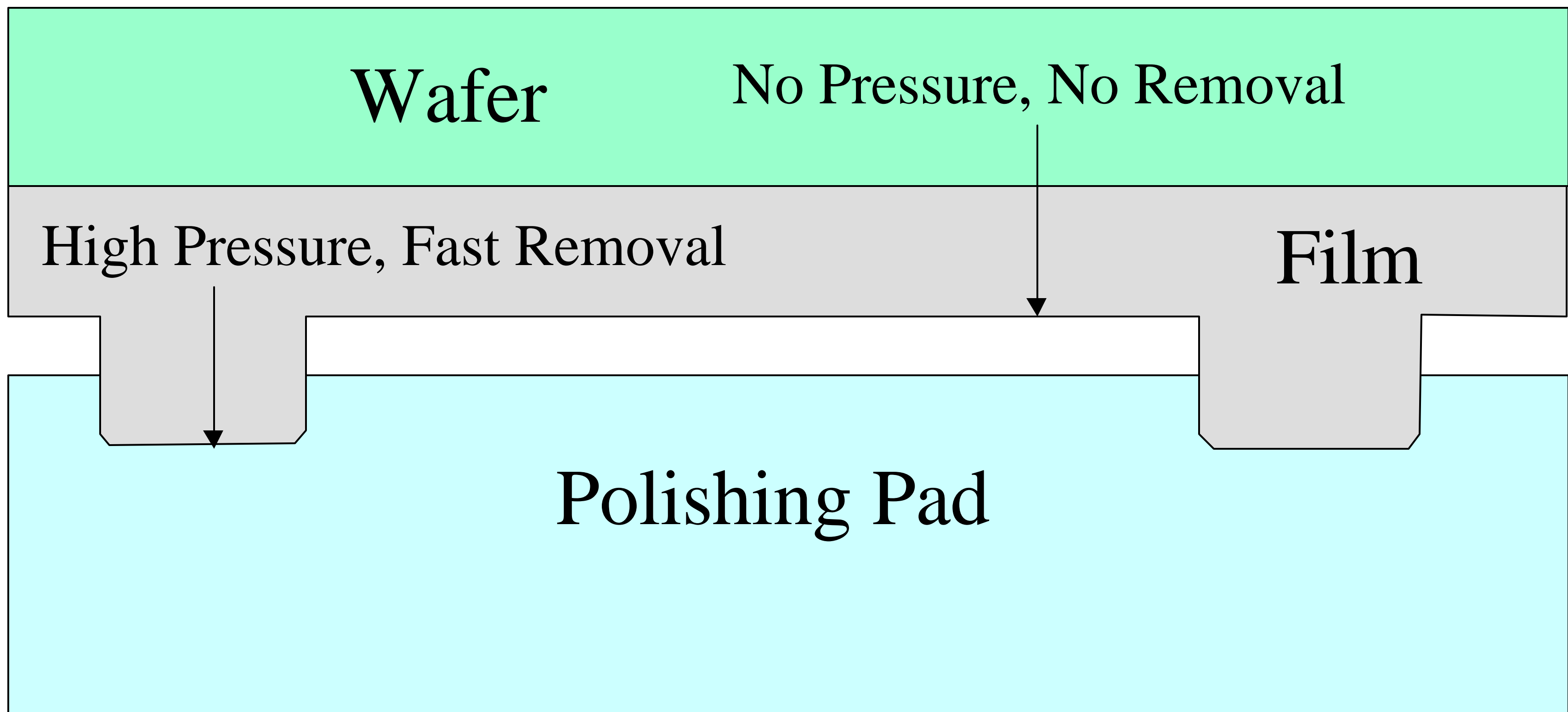
$$R = K_p \cdot p \cdot \Delta v$$

- p is the polishing pressure
- K_p is the Preston coefficient
- Δv is relative velocity of wafer and pad

Removal Rate

- Preston equation works very well for the bulk film polishing processes
- The protruding portions on a rough surface have higher polishing pressure
- Removal rate of protruding parts is higher
- This helps to remove surface topography and planarize the surface

Protruding Parts with Higher Pressure



Removal Rate

- Thickness difference before and after CMP divided by CMP time
- Multiple measurement for uniformity
- Test wafer, blanket film
- Daily tool qualification

Uniformity

- Usually 49-point, 3σ standard deviation as the definition of the uniformity for the CMP process qualifications
- Changes of the film thickness before and after CMP process is monitored
- For the production wafers, uniformity after CMP process is monitored
- Normally use 9 or 13 points measurement

Uniformity

- Both WIW and WTW uniformity can be affected by the polish pad condition, down force pressure distribution, relative speed, restraining ring positioning, and the shape of the wafers.
- By using harder pad and lower pressure a good global uniformity can be achieved
- Lower pressure, lower removal rate, affect throughput

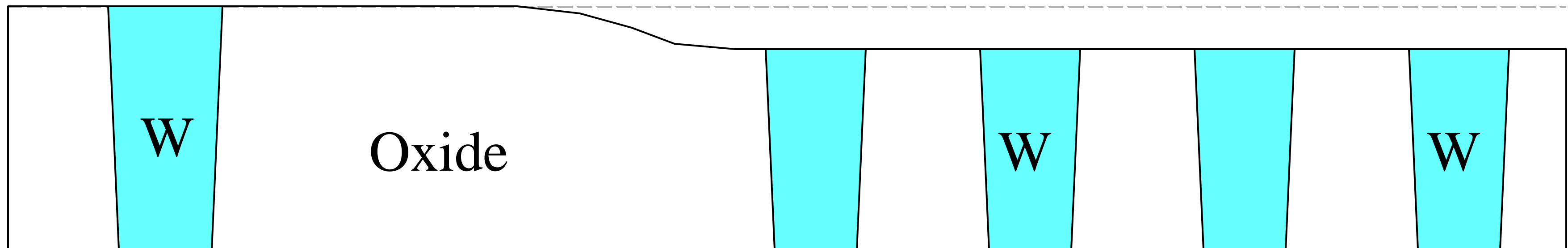
Selectivity

- Ratio of removal rates of different materials
- Affect CMP defects, such as erosion or dishing
- The slurry chemistry is the primary factor that affects removal selectivity of CMP process
- STI oxide CMP require high oxide to nitride selectivity, from 100:1 to 300:1
- Because only polish oxide, selectivity is not important in PMD and IMD CMP processes

Selectivity

- For tungsten CMP process, selectivity to oxide and titanium nitride is very important.
- Usually tungsten to TEOS oxide selectivity is very high, from 50 to 200
- Slurry chemistry, oxidant
- Selectivity is also related to the pattern density
- higher pattern density, lower removal selectivity
  - lead to erosion of the tungsten and oxide film

Erosion Caused by High Pattern Density



IC Layout and Erosion

- IC design layout can directly affect the erosion problems
- By designing opening area less than 30% of the chip surface, it can help to solve the erosion problem

Defects

- CMP removes defects and improves yield
- Introduce some new defects
  - scratches, residual slurry, particles, erosion, and dishing.
- Large foreign particles and hard polish pad can cause scratches
  - Tungsten fill the scratches in oxide surface cause short circuit and reduce the IC yield.

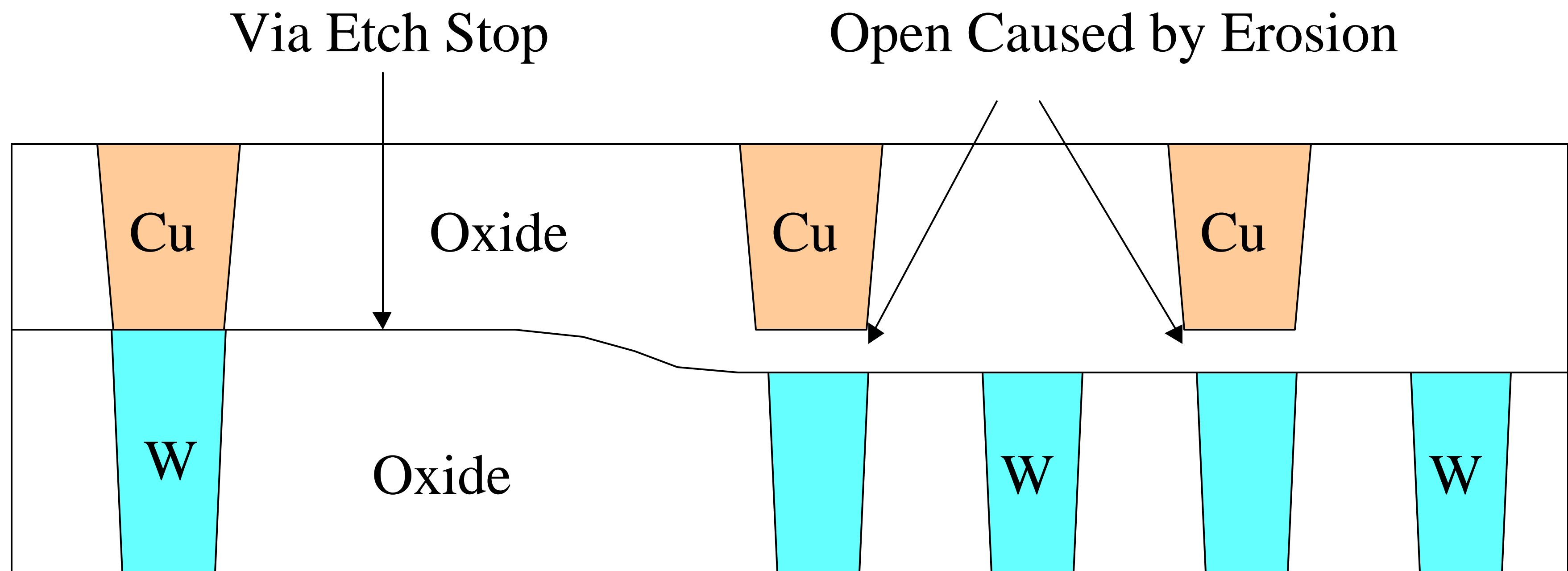
Defects

- Improper down force pressure, worn pad, inadequate pad conditioning, particle surface attraction, and slurry drying
- Slurry residue on the wafer surface and cause contamination
- Post-CMP clean is very important to remove slurry residue and improve process yield

Erosion

- Increases depth of via holes
- Incomplete via hole etch
- Open loop between the different layers in the next dual damascene interconnection

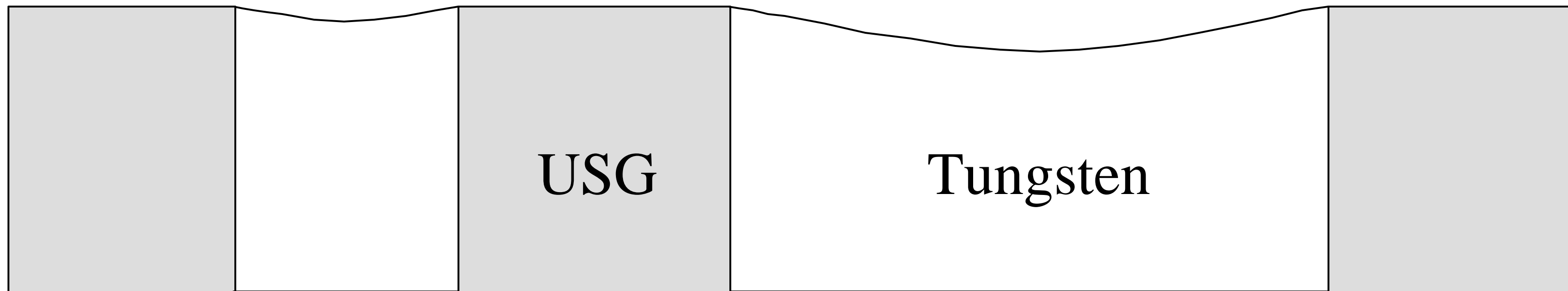
Circuit Opening Caused by Erosion



Dishing Effect

- Usually happens at a larger opening area
  - large metal pads
  - STI oxide in the trenches.
- More materials are removed from the center
- Cross-section view looks like a dish

Dishing Effect



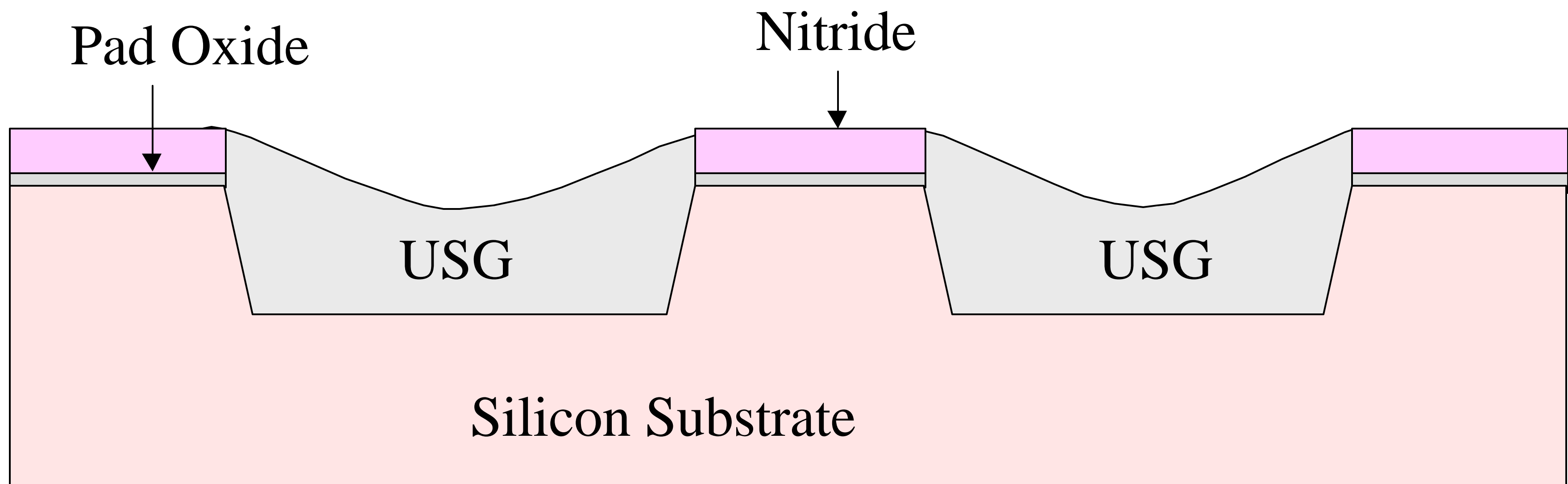
Dishing/Erosion and Selectivity

- Both dishing and erosion effects are related to the removal selectivity
- Tungsten CMP process,
  - If tungsten to oxide selectivity is too high, more tungsten removal, cause dishing and recessing
  - If the selectivity is not high enough, both oxide and tungsten will be polished, causes erosion

Dishing/Erosion and Selectivity

- Oxide CMP with high selectivity of oxide to nitride can cause oxide dishing during the oxide overpolishing step of the oxide CMP in the STI formation

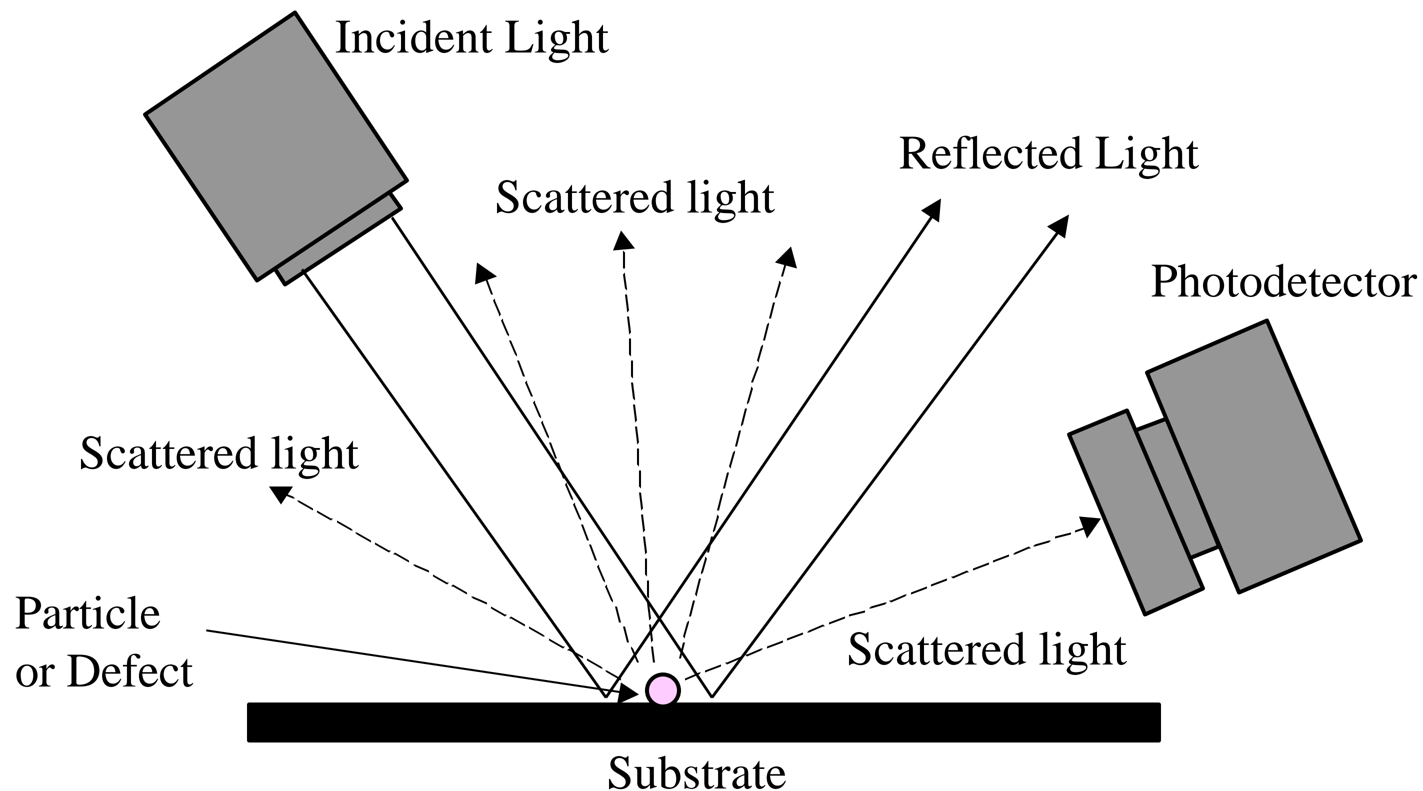
Dishing Effect of STI USG



Particles and Defects

- Particles and defects cause irregular topography on wafer surface
- Scattering incident light
- Monitor particles and defects by detecting the scattered light

Particle Detection By Light Scattering



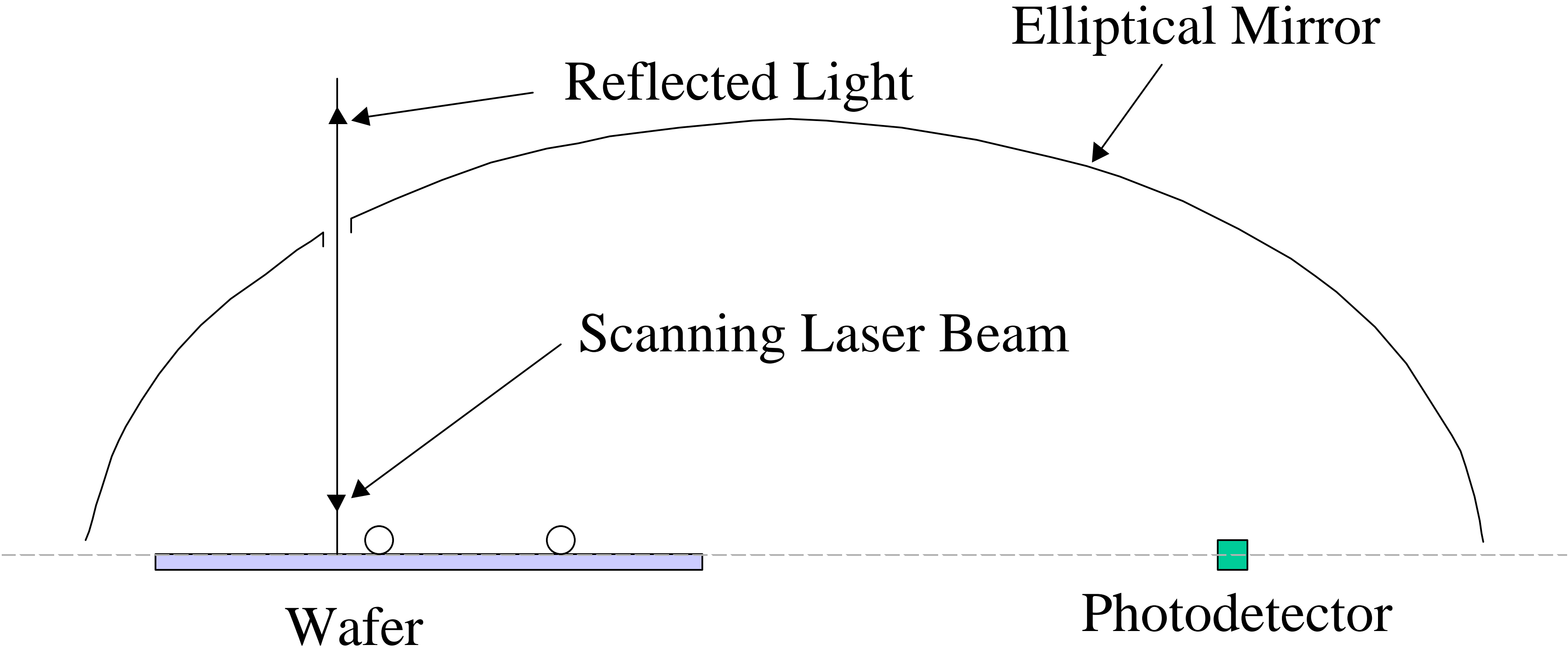
Particle Measurement

- Intensity of the scattered light is very weak
- Elliptical mirror is used to collect the light
- Elliptical curve has two focuses
- Light from one focus reflects to another focus

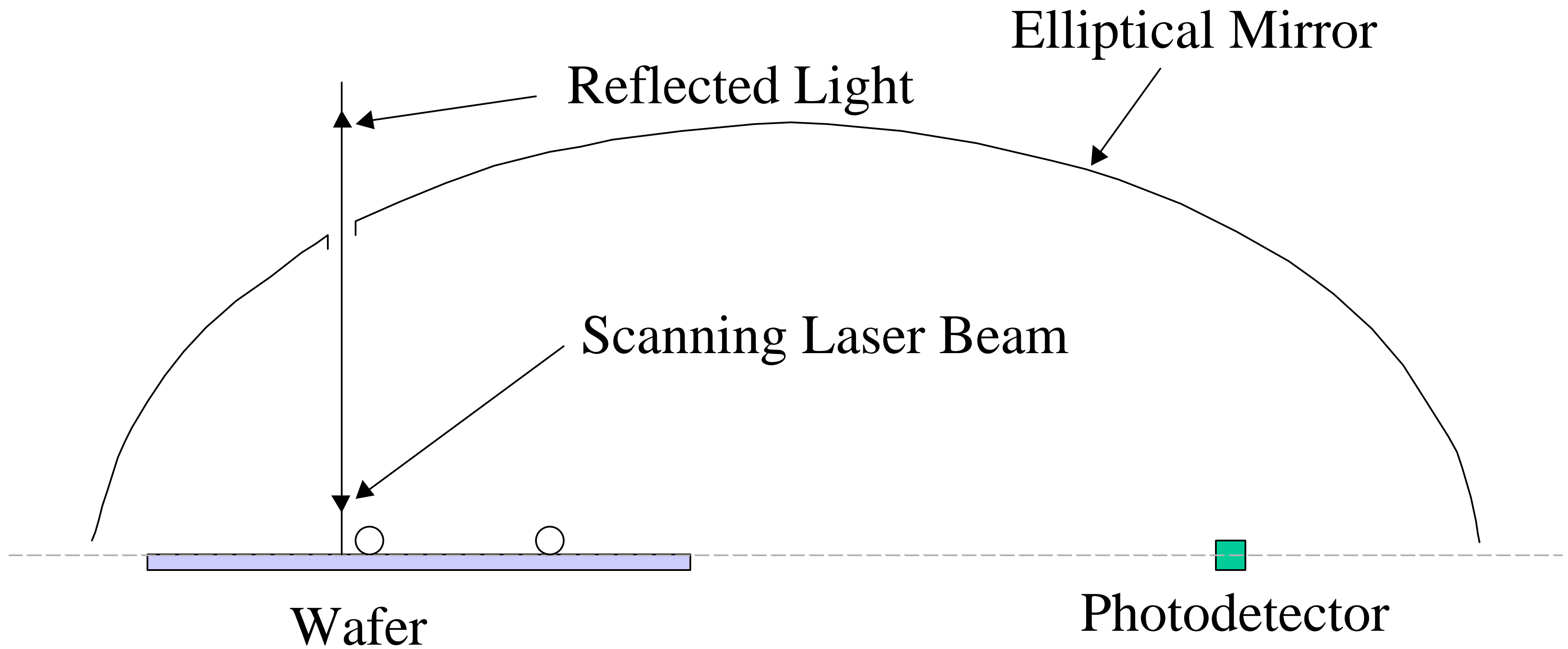
Particle Measurement

- Laser beam scans wafer surface vertically at one focus of elliptical mirror and a photo-detector is placed at another focus
- Moving wafer, and collecting scattered light to detect tiny particles and defects
- Mapping particle/defect locations on the wafer surface

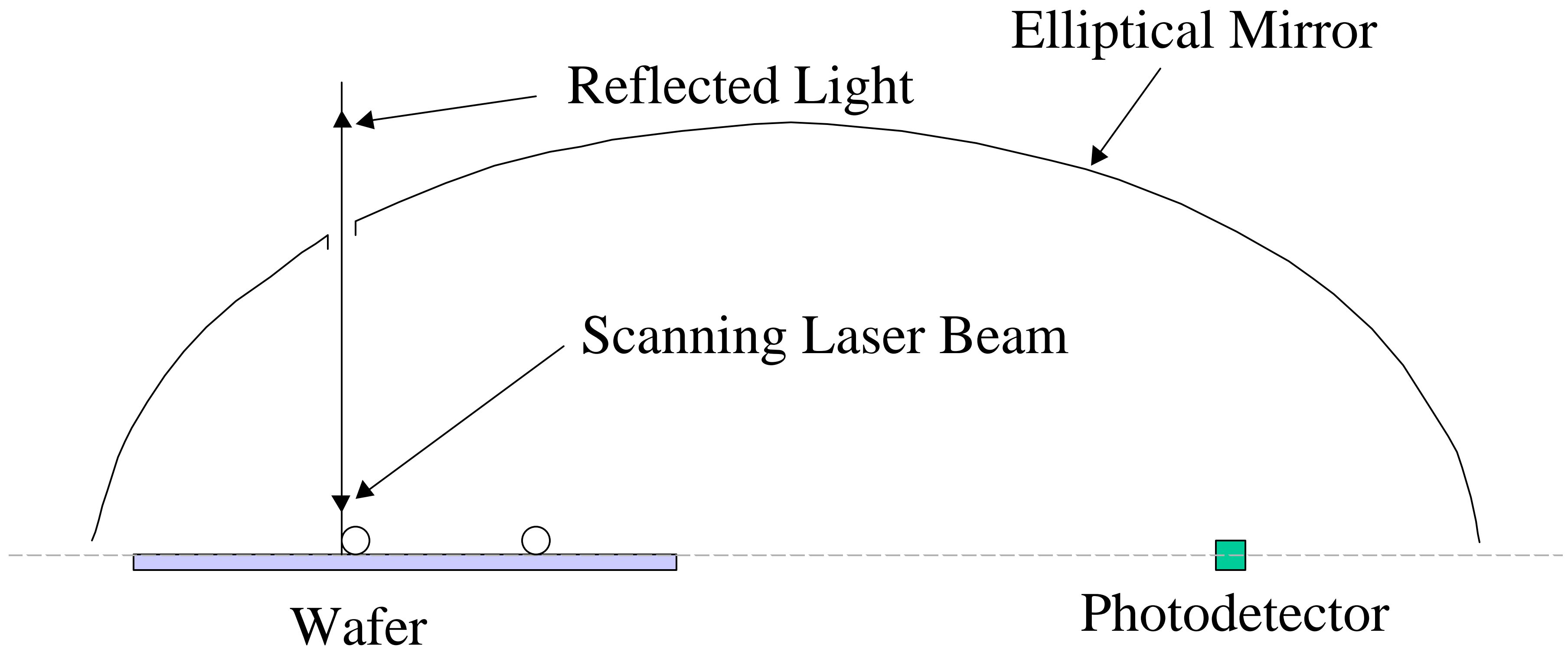
Laser Scan



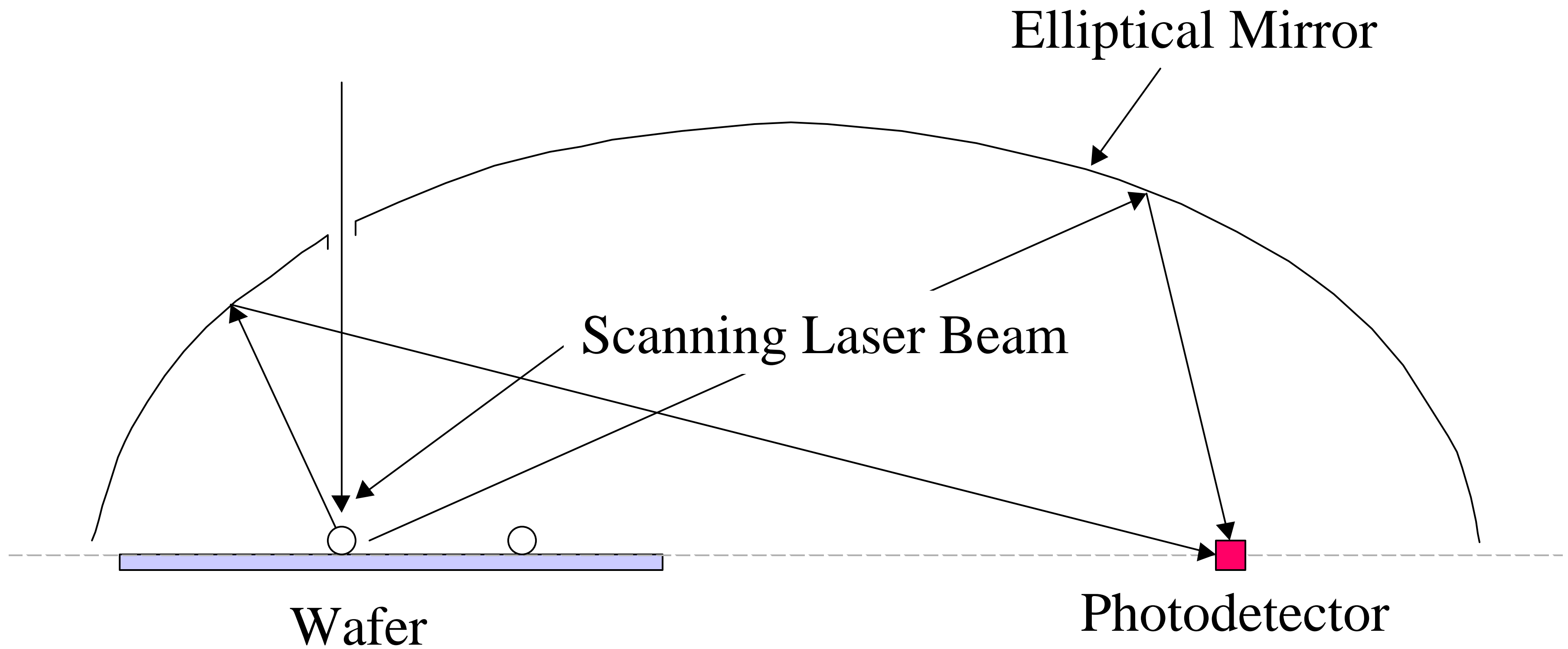
Particle Measurement



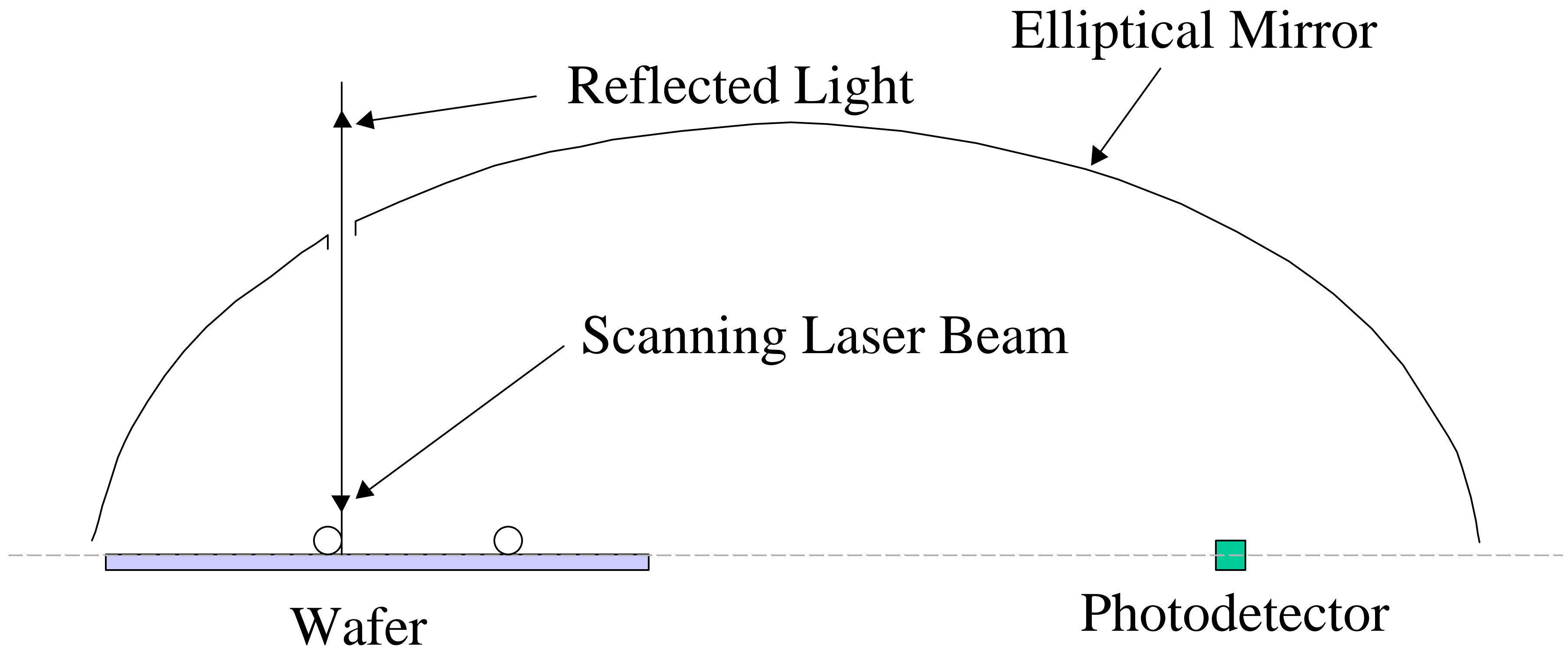
Particle Measurement



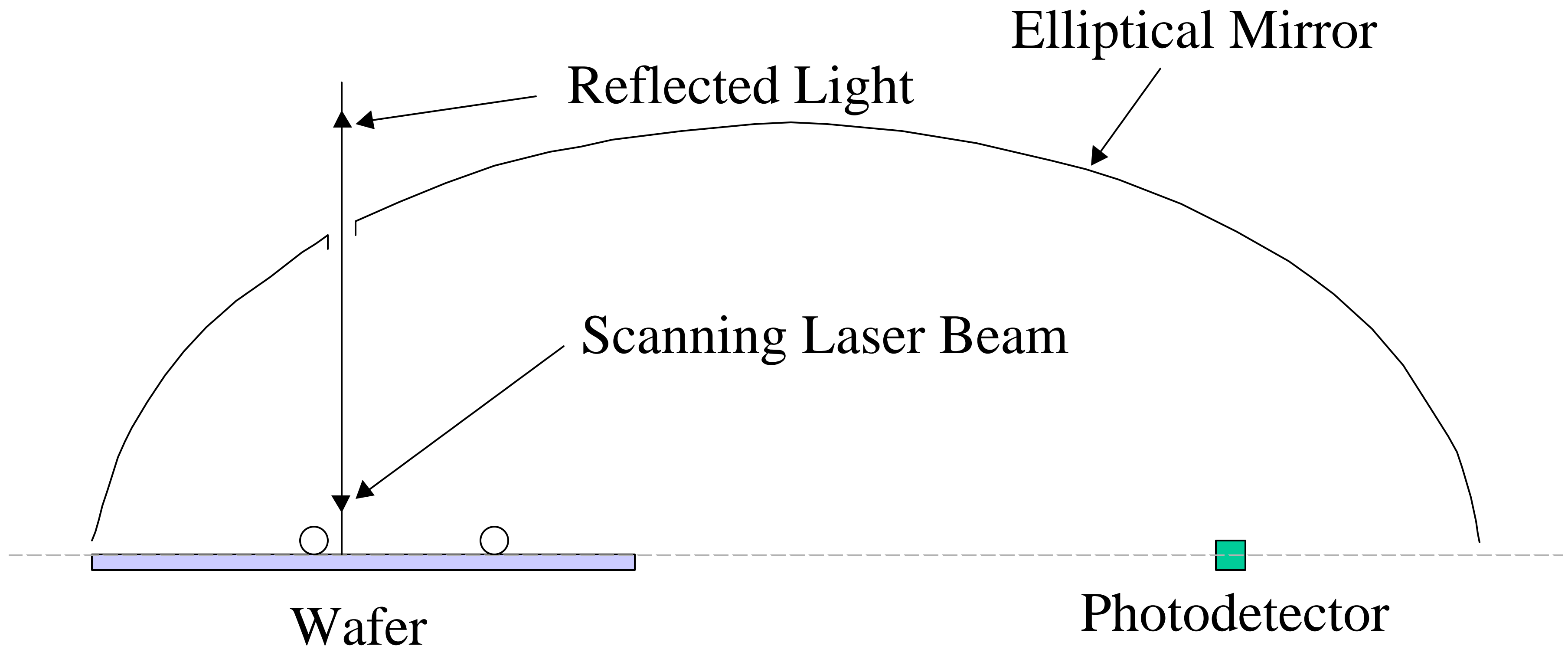
Particle Measurement: Particle 1



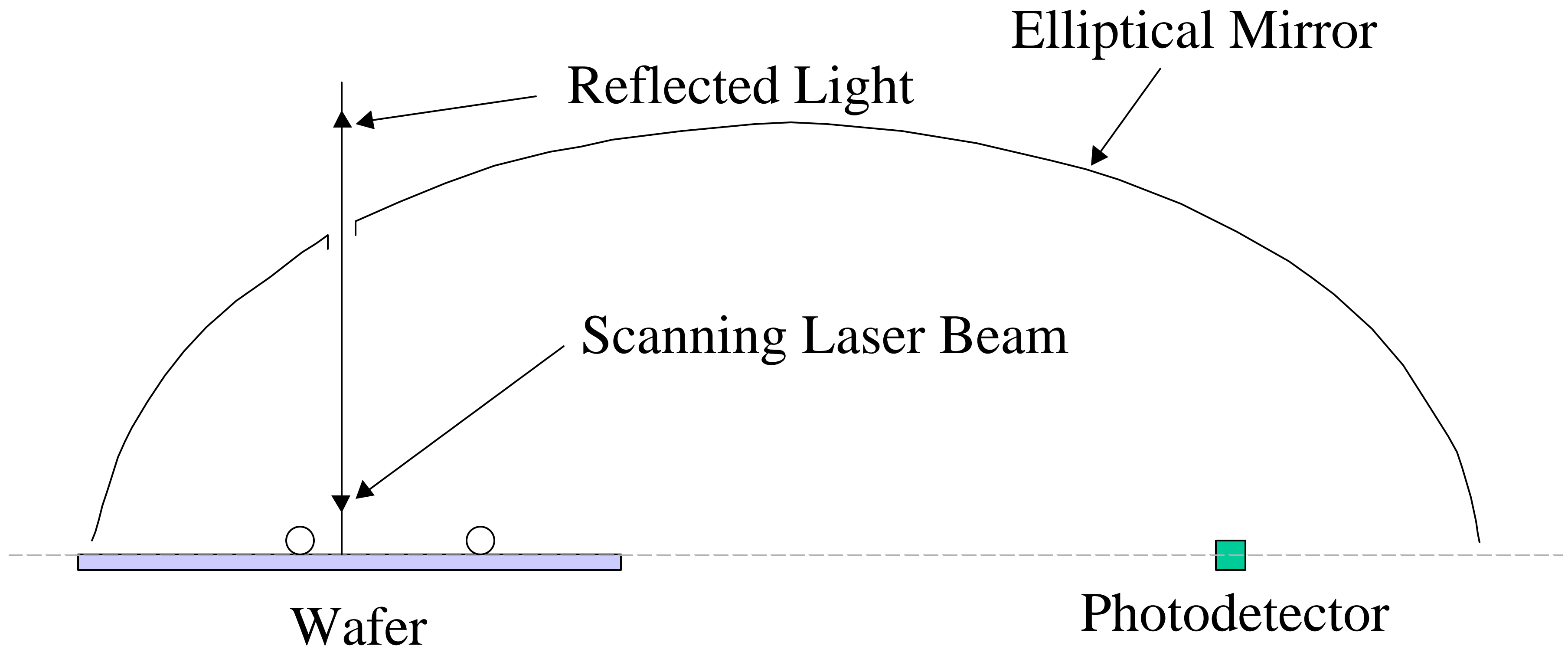
Particle Measurement



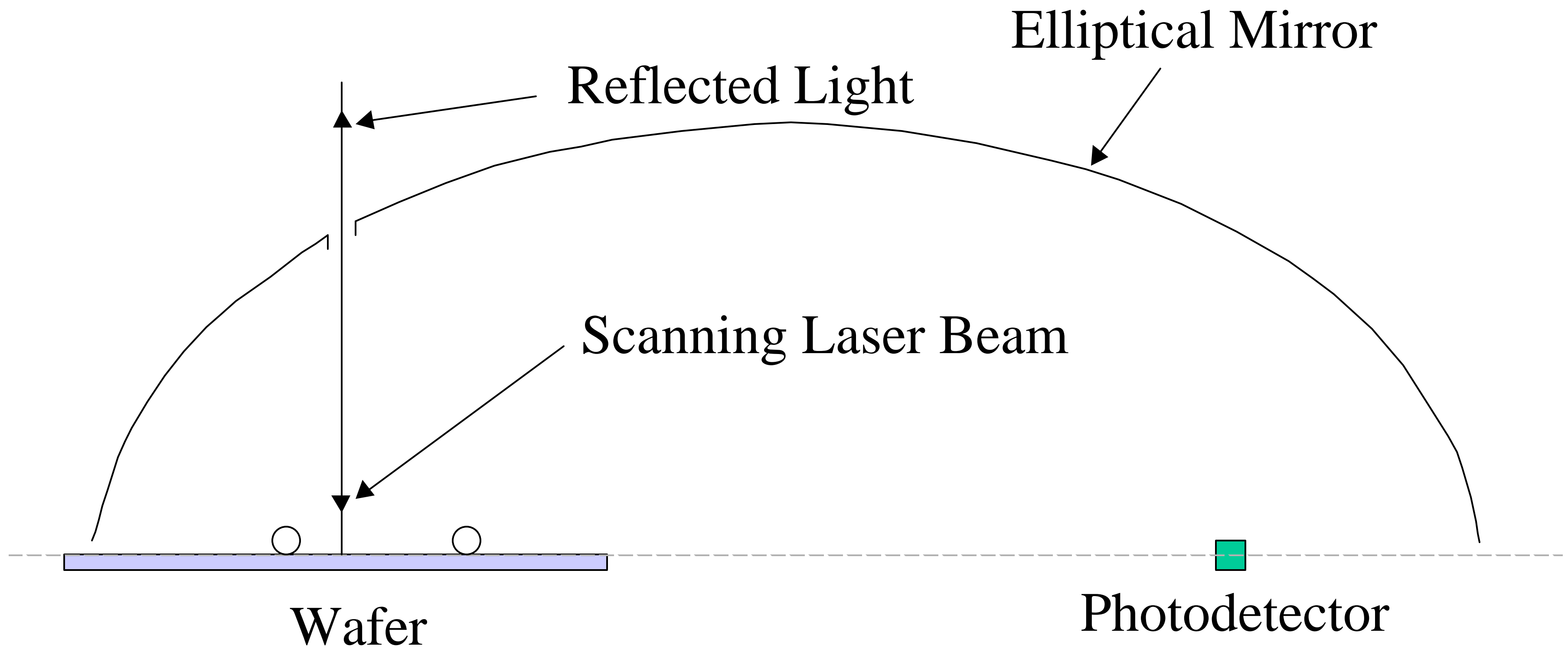
Particle Measurement



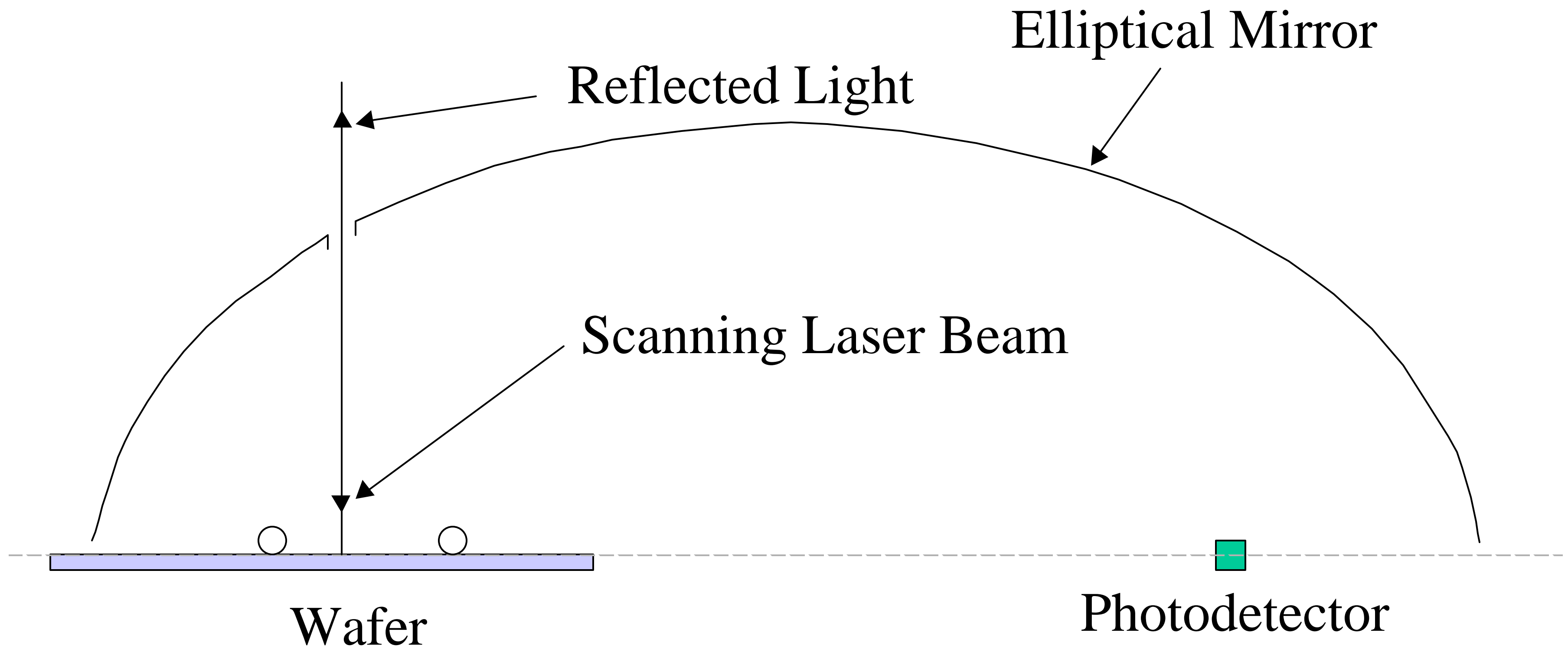
Particle Measurement



Particle Measurement



Particle Measurement



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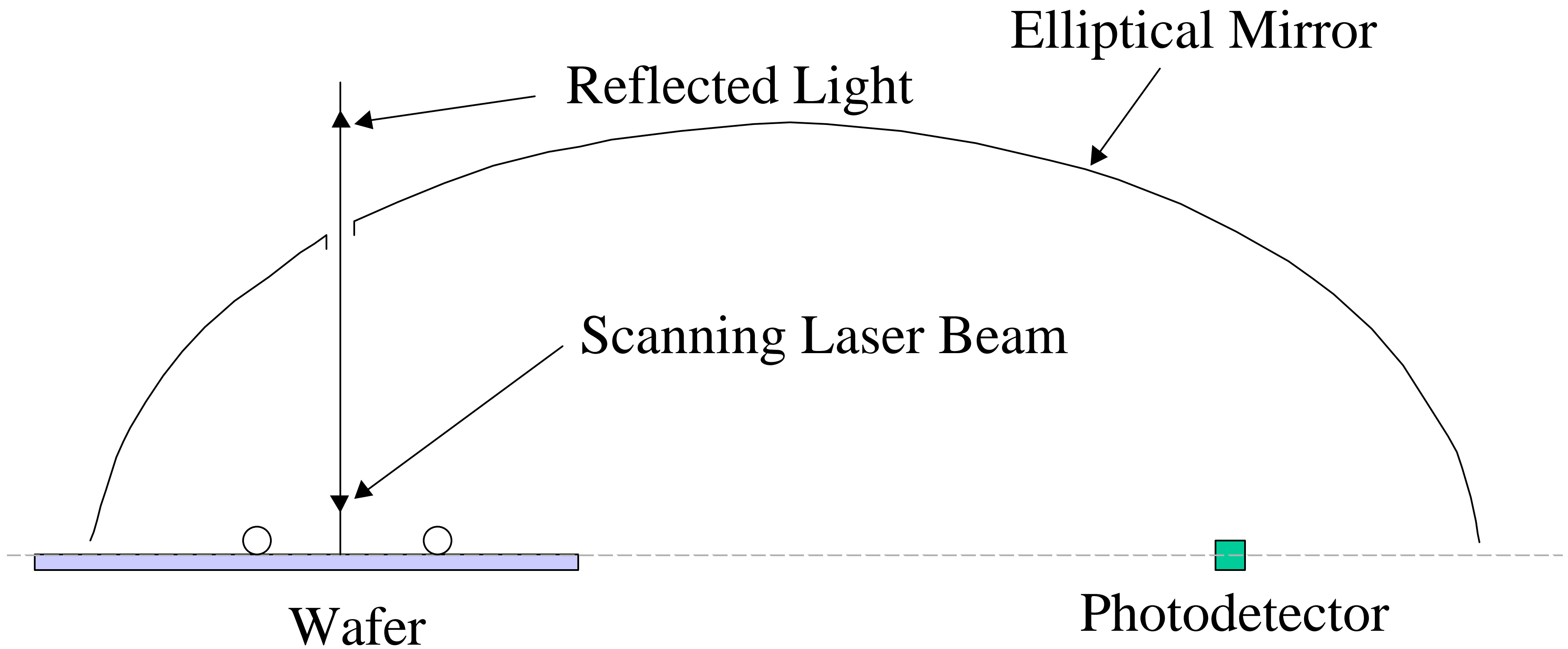

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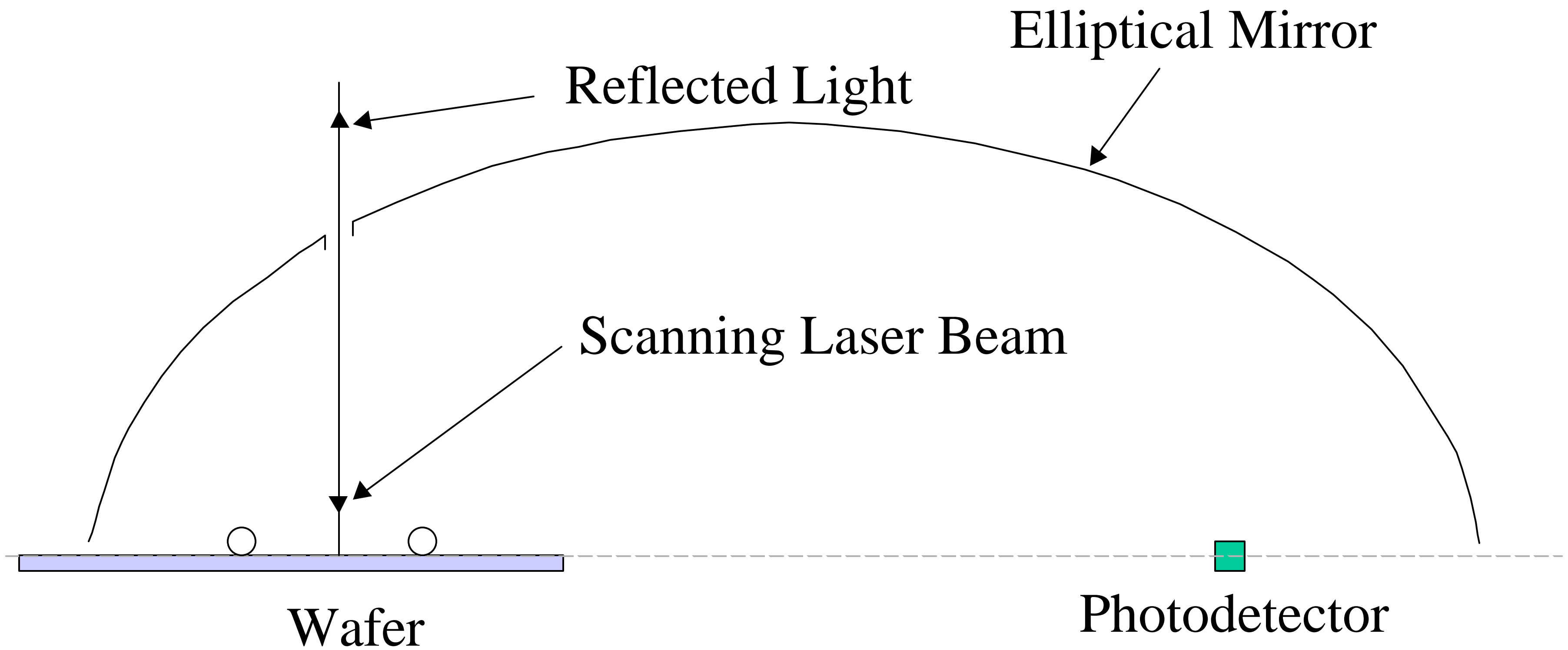

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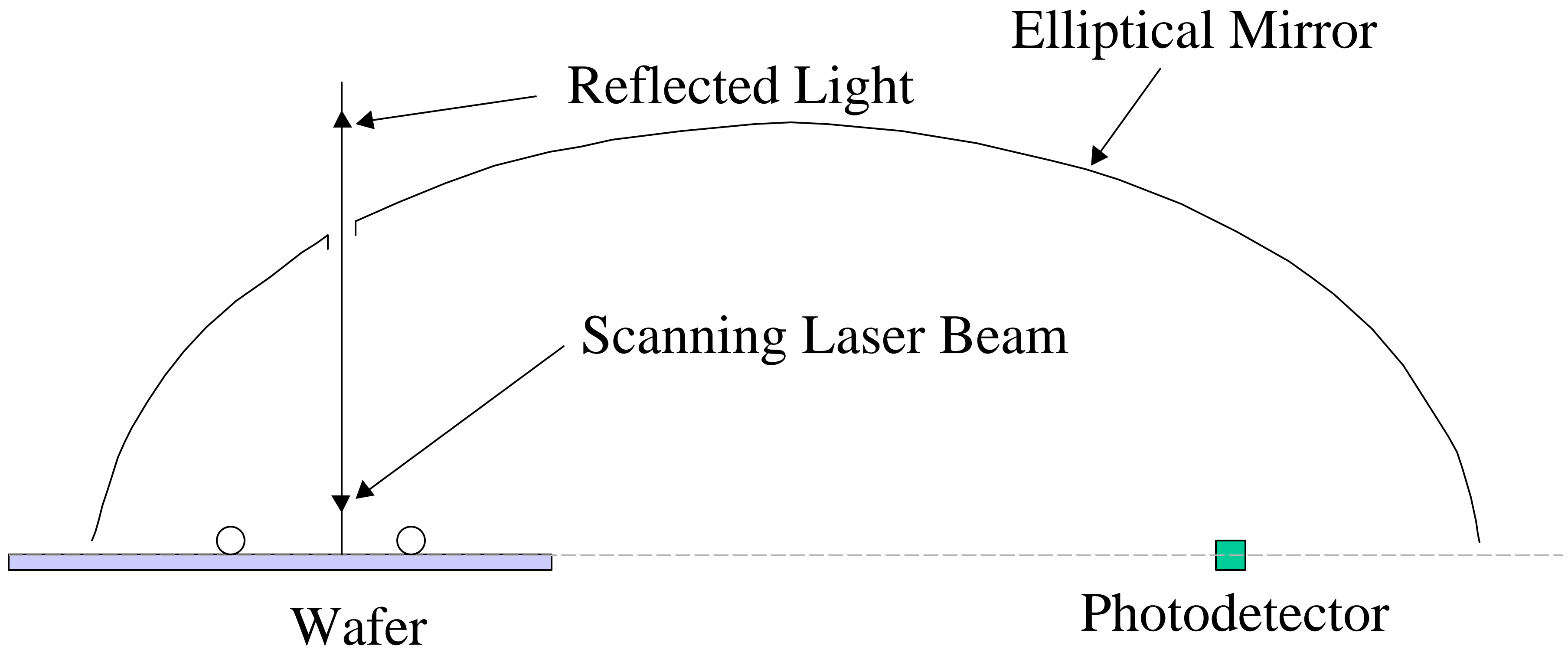

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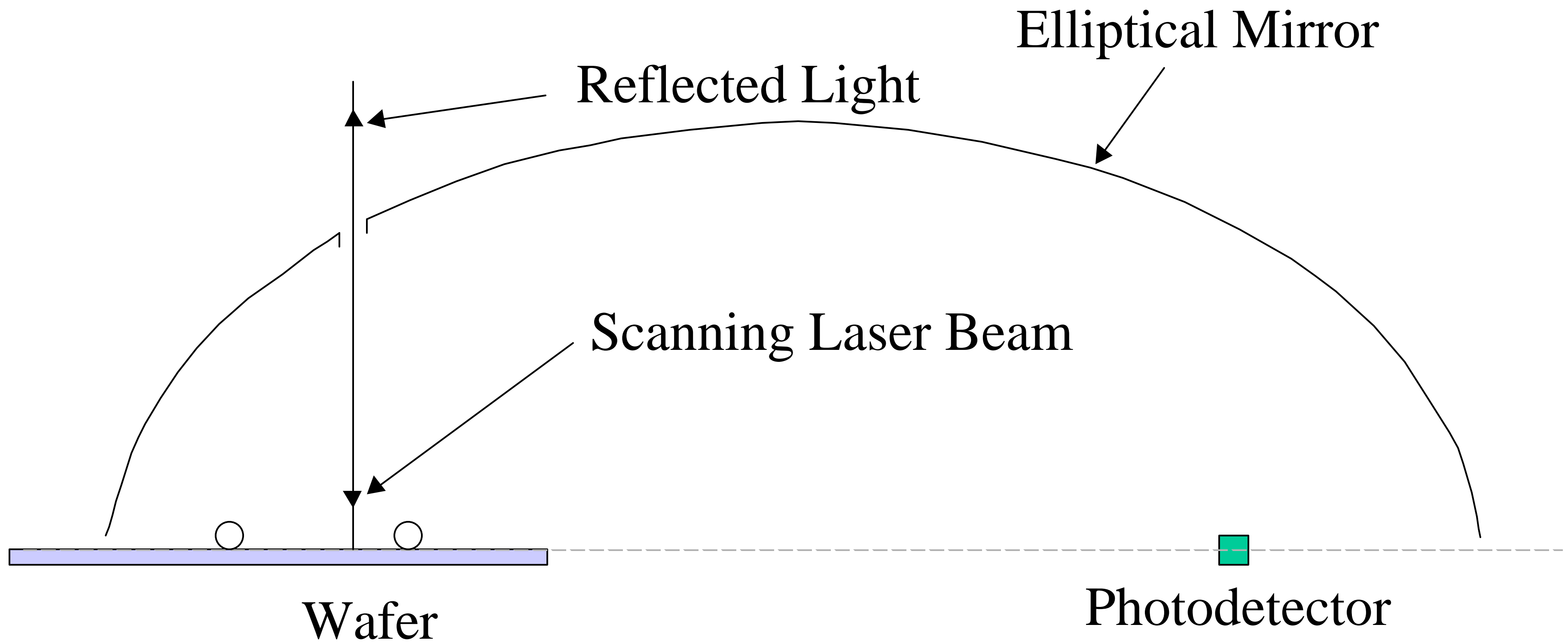

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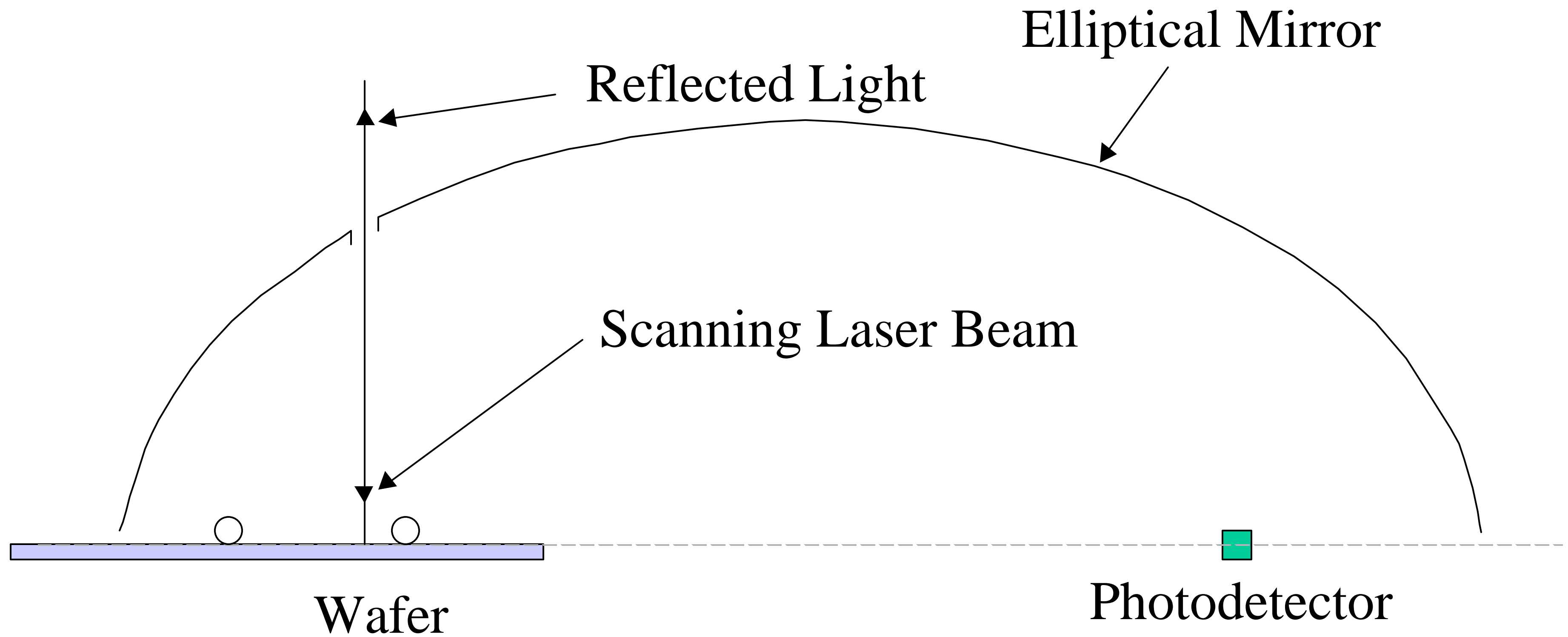

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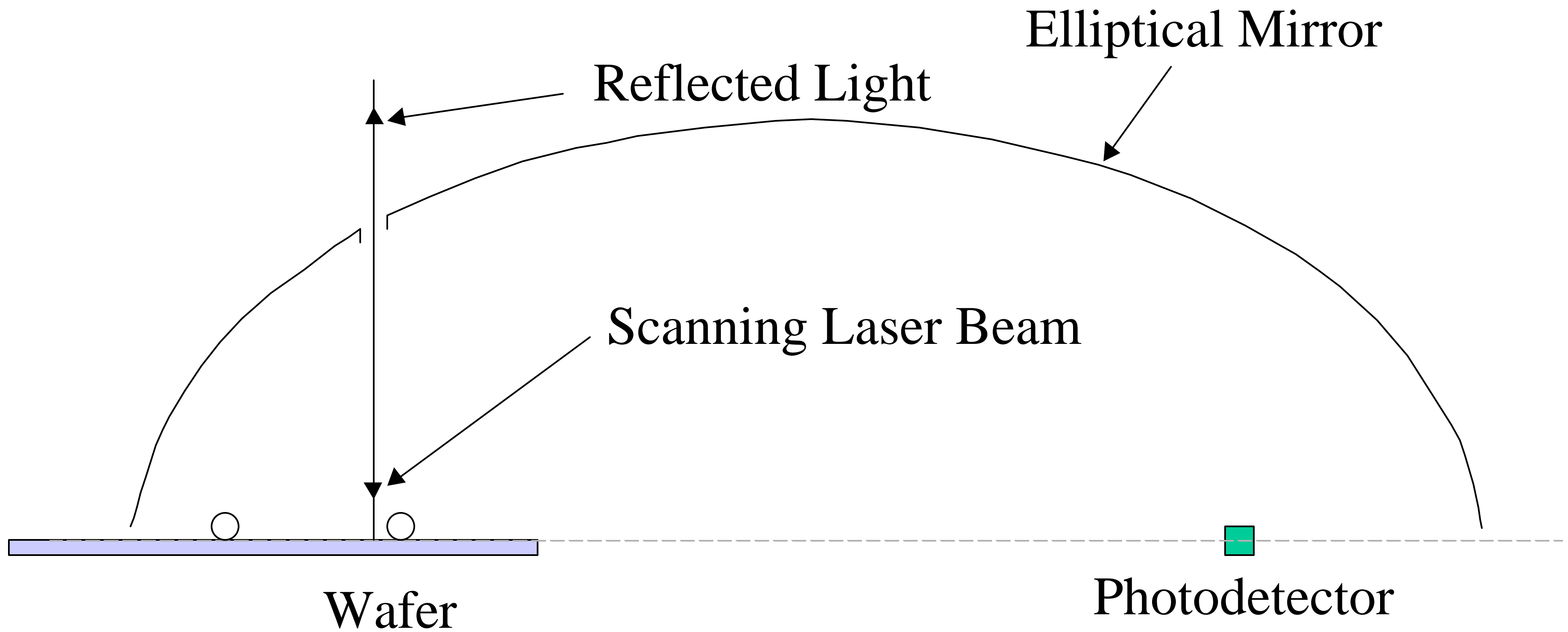

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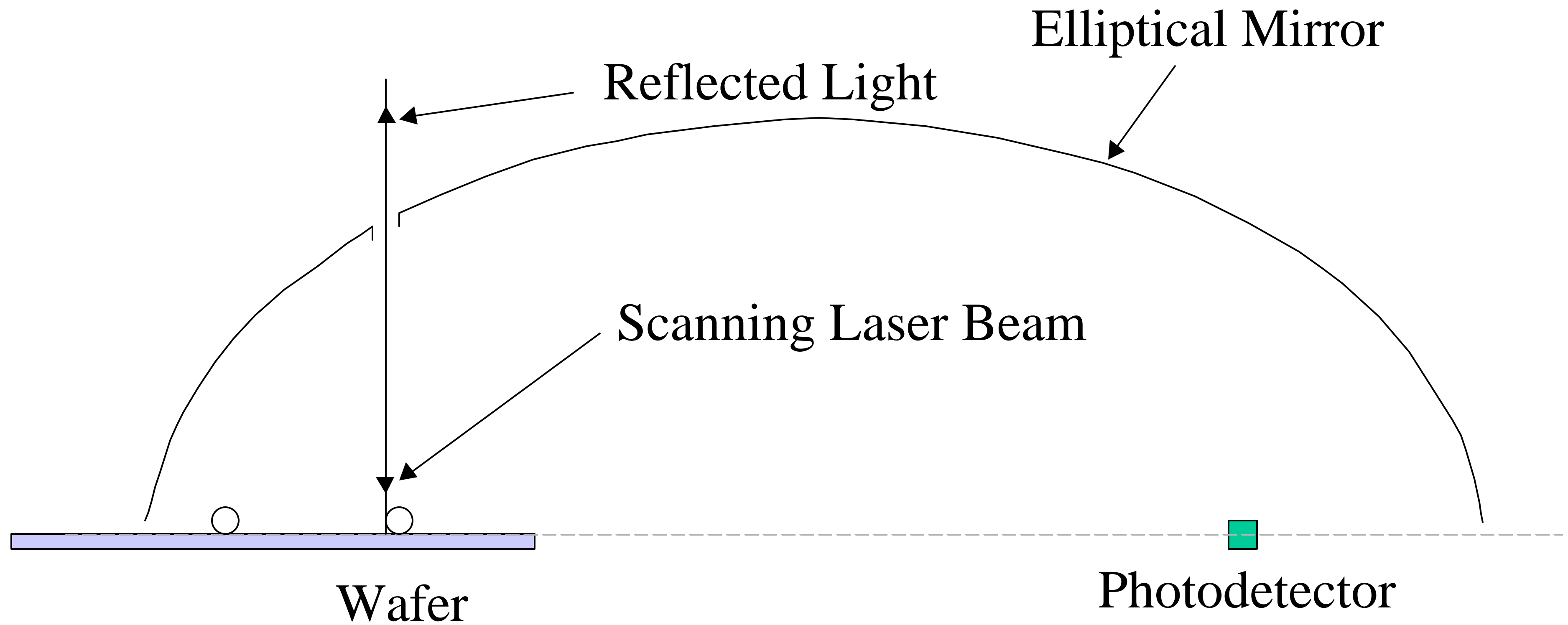
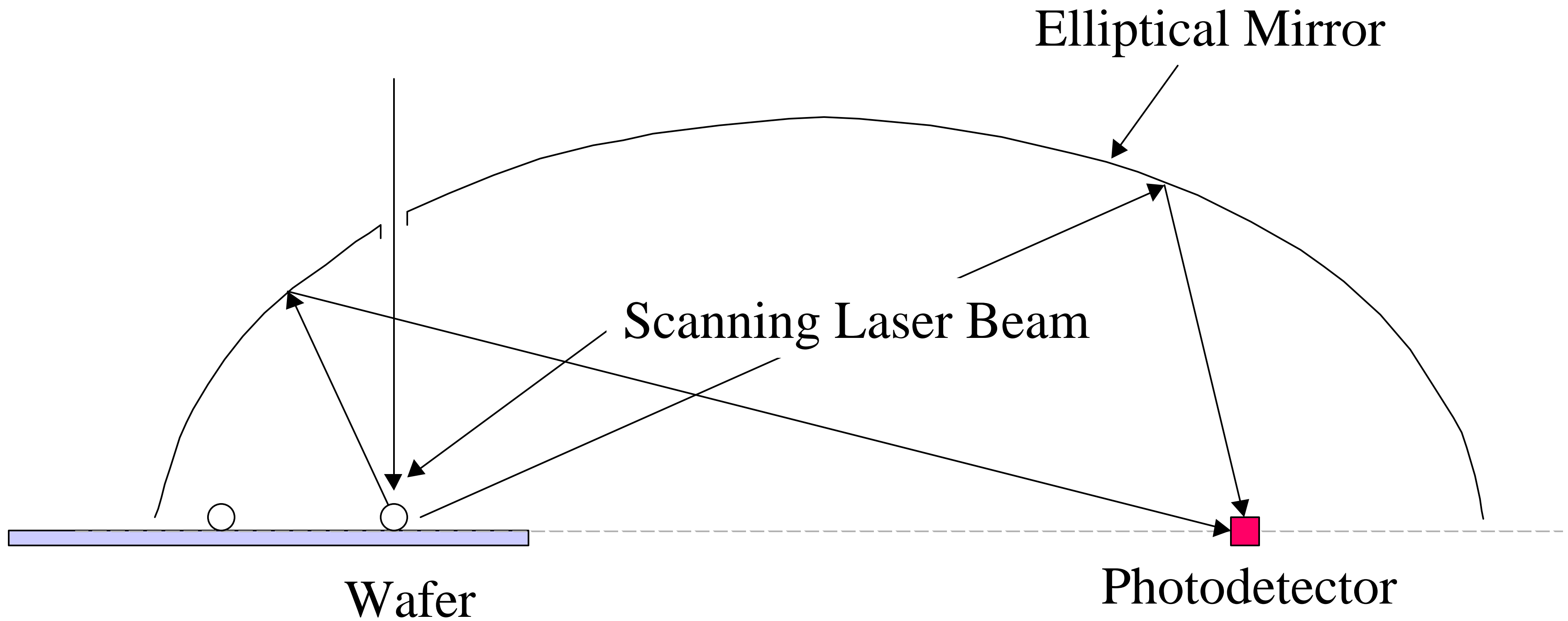
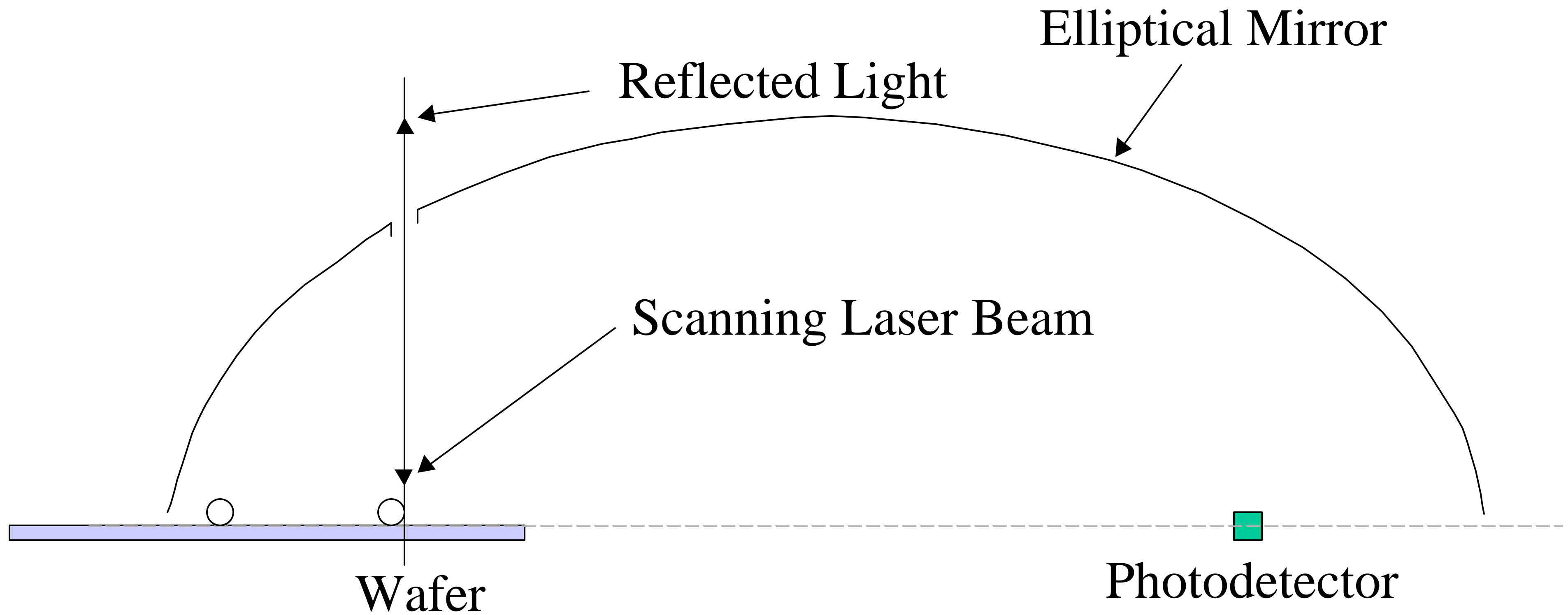


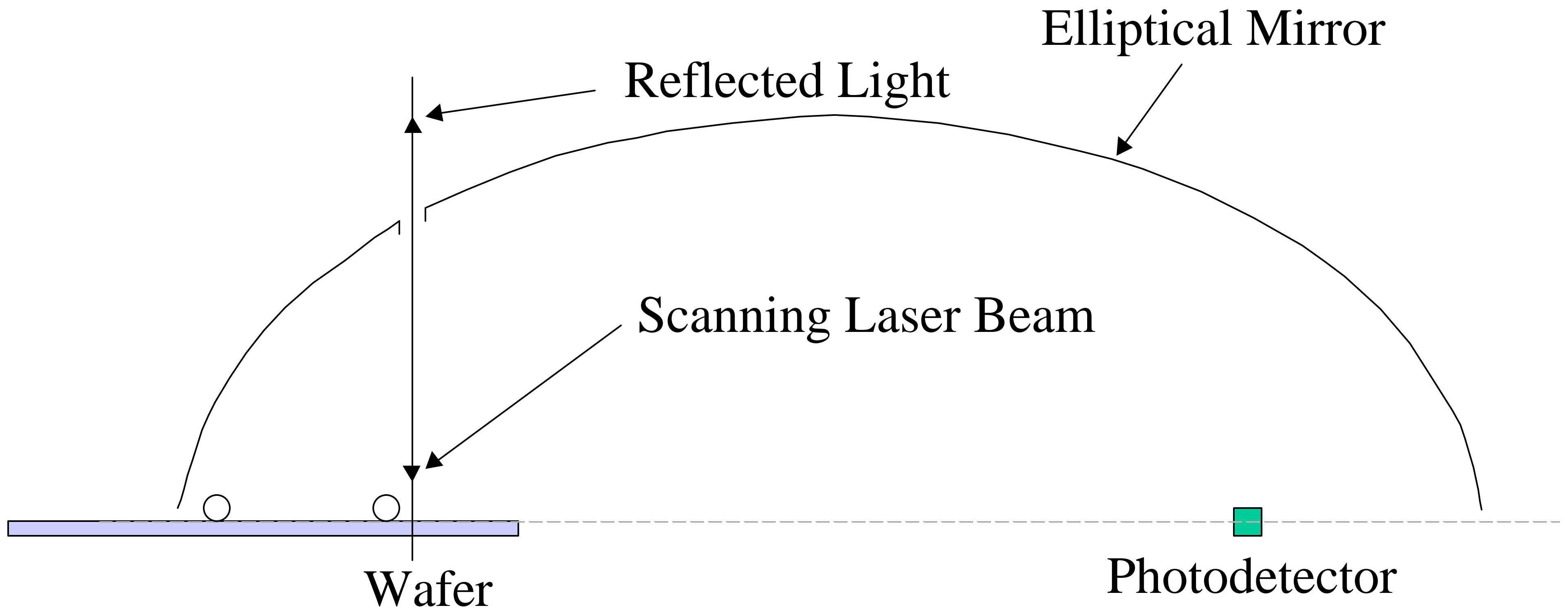
Particle Measurement, Particle 2



Particle Measurement



Particle Measurement



CMP Processes

- Oxide removal mechanism
- Metal removal mechanisms
- Endpoint methods

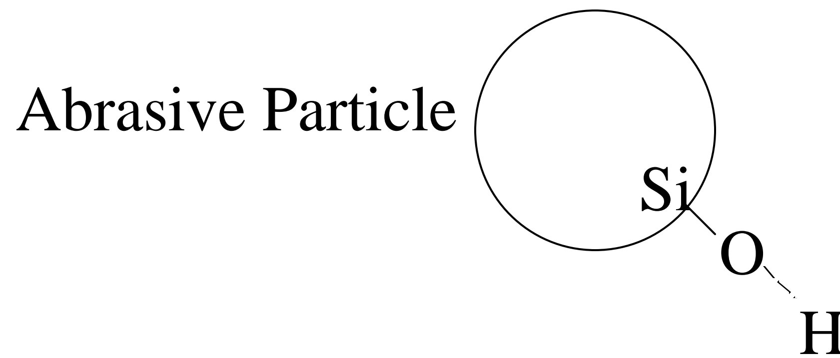
Oxide CMP

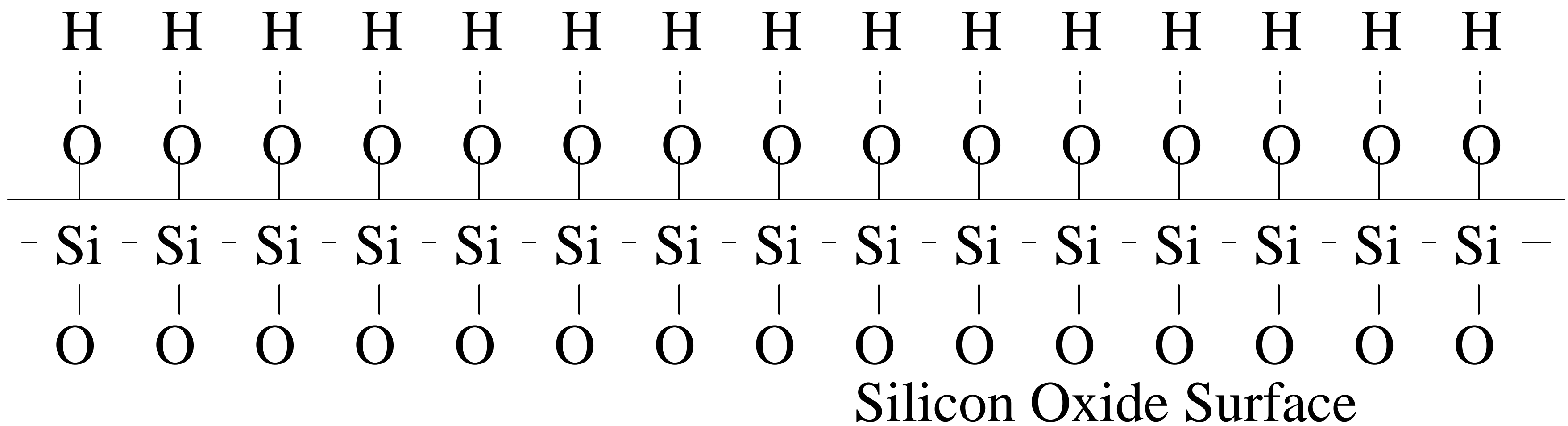
- Early development in the mid-1980s in IBM
- Combined knowledge and experience of glass polishing and silicon wafer polishing

Oxide CMP

- Hydroxyls on both film and silica surfaces
- Form hydrogen bonds of silica and surface
- Form molecular bonds of silica and surface
- Mechanical removal of the particles bonded with wafer surface
- Tear away atoms or molecule from film on wafer surface

Oxide CMP





Oxide CMP, Hydrogen Bond

Abrasive Particle

Si

O

H

H H H H H H H H H H H H H H H

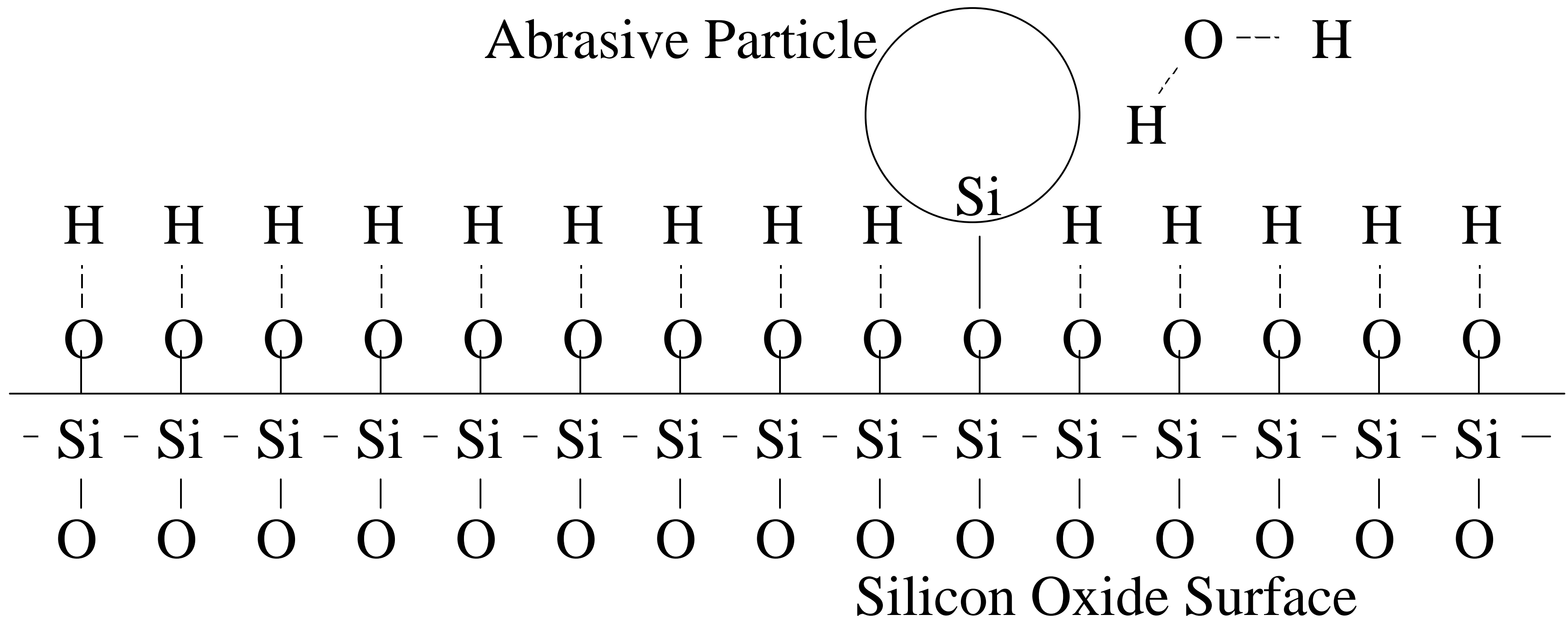
O O O O O O O O O O O O O O O

– Si – Si – Si – Si – Si – Si – Si – Si – Si – Si – Si – Si – Si – Si – Si –

O O O O O O O O O O O O O O O

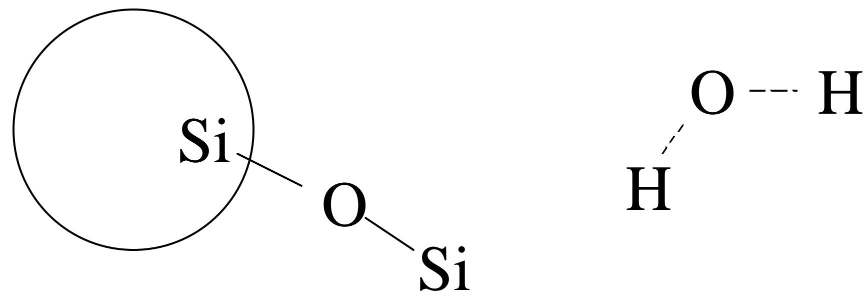
Silicon Oxide Surface

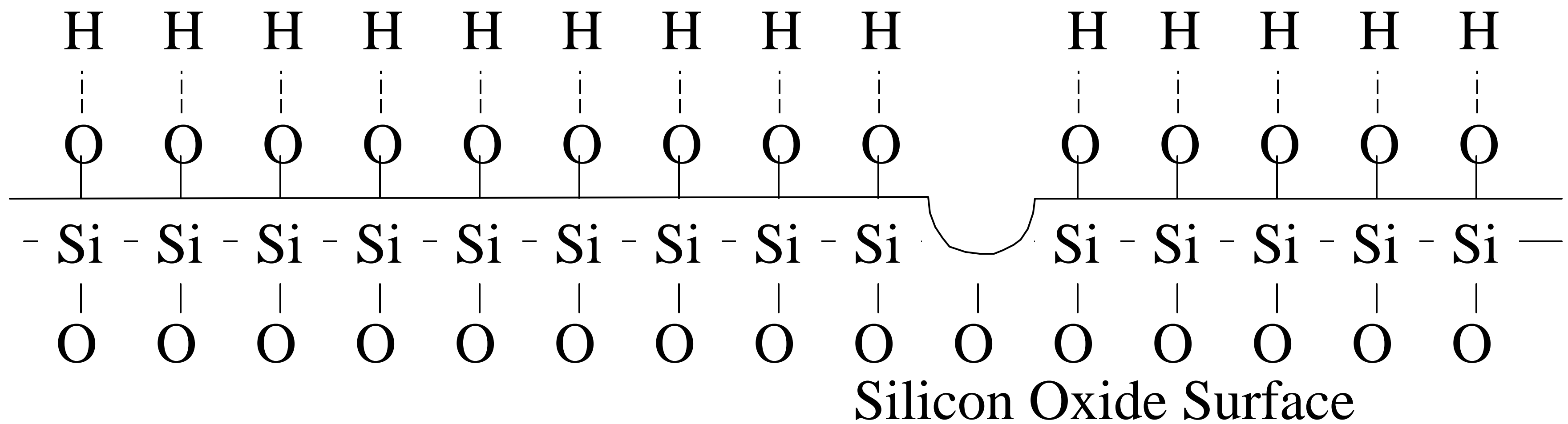
Oxide CMP, Molecule Bond



Oxide CMP, Removal of Oxide

Abrasive Particle



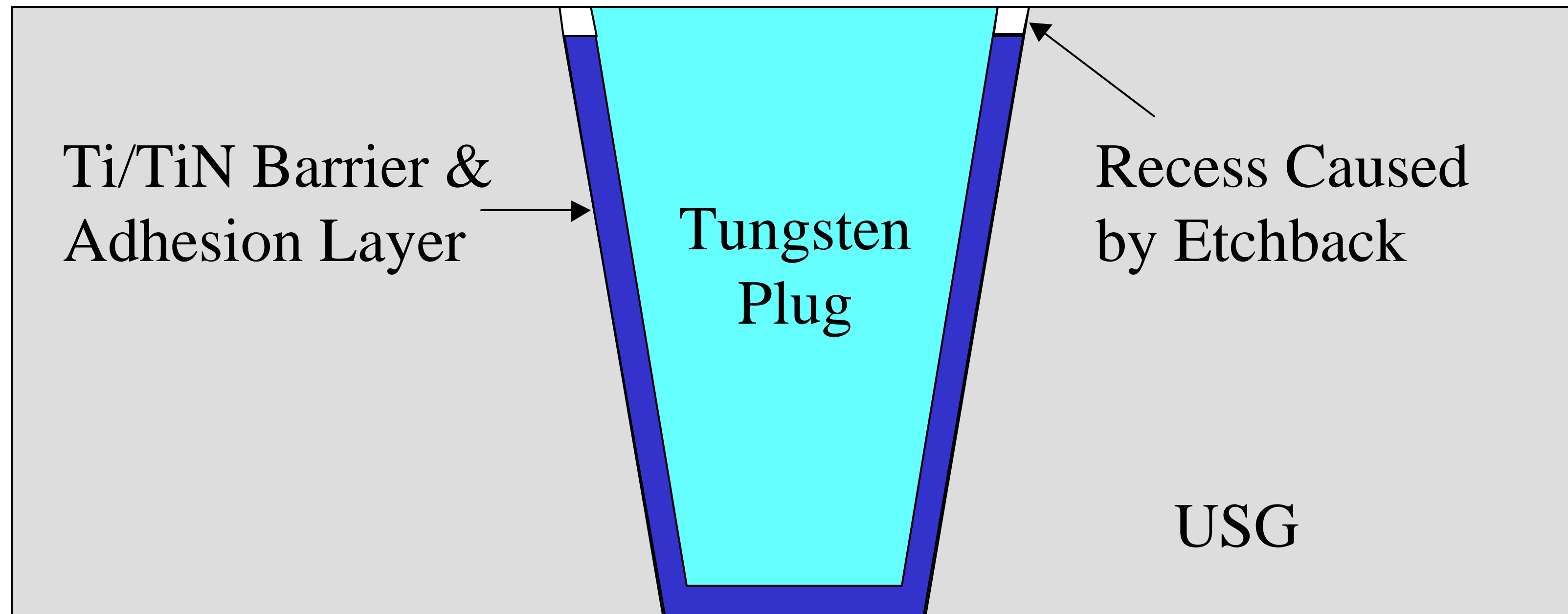


Silicon Oxide Surface

Tungsten CMP

- Form plugs to connect metal lines between different layers
- Tungsten etch back and Tungsten CMP
  - Fluorine based tungsten RIE etchback
    - In-situ with tungsten CVD process in a cluster tool
    - Recessing of the Ti/TiN barrier/adhesion layer due to the aggressive fluorine chemical etch of Ti/TiN and affects the chip yield
  - Tungsten CMP: winner for higher yield

Recess of Ti/TiN due to W Etchback

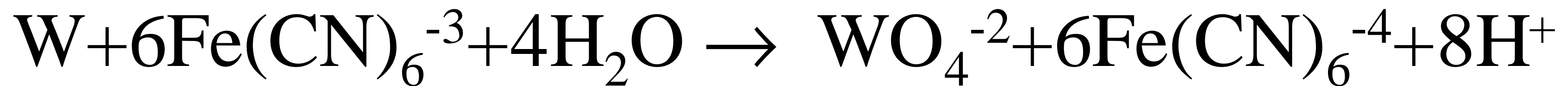


Tungsten CMP

- Two completing removal mechanisms
- Wet etch: a pure chemical process
  - Unfavorable
- Passivation oxidation and oxide abrading: chemical and mechanical process
  - Favorable
- Controlled by pH value of slurry

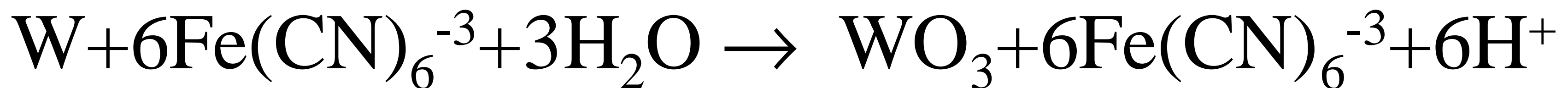
Tungsten CMP

- Potassium ferricyanide, $K_3Fe(CN)_6$, is used as both etchant and oxidant
- The wet etch chemistry can be expressed



$$W + 6Fe(CN)_6^{-3} + 4H_2O \rightarrow WO_4^{-2} + 6Fe(CN)_6^{-4} + 8H^+$$

- The competing passivation oxidation reaction

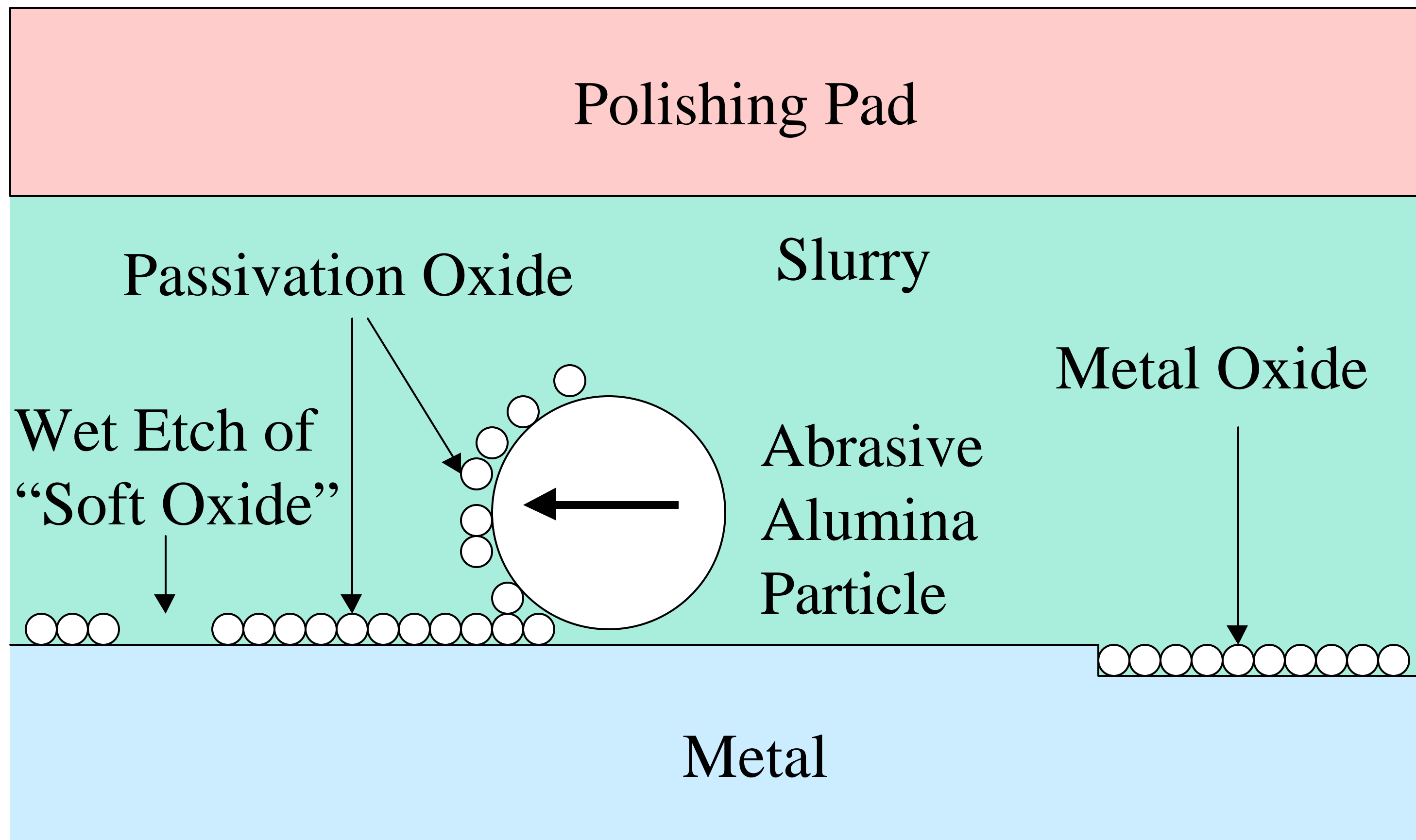


$$W + 6Fe(CN)_6^{-3} + 3H_2O \rightarrow WO_3 + 6Fe(CN)_6^{-3} + 6H^+$$

Tungsten CMP

- Normally tungsten CMP uses two step process
- The first step remove bulk W with slurry pH < 4,
- The second step remove TiN/Ti stacked barrier/adhesion layer with slurry pH > 9

Metal CMP Process



Copper CMP

- Difficult to plasma etch copper
  - Lack of volatile inorganic copper compounds
- Copper CMP key process in copper metallization process
- H_2O_2, or HNO_4 can be used as oxidant
- Alumina particulate is used for abrasion

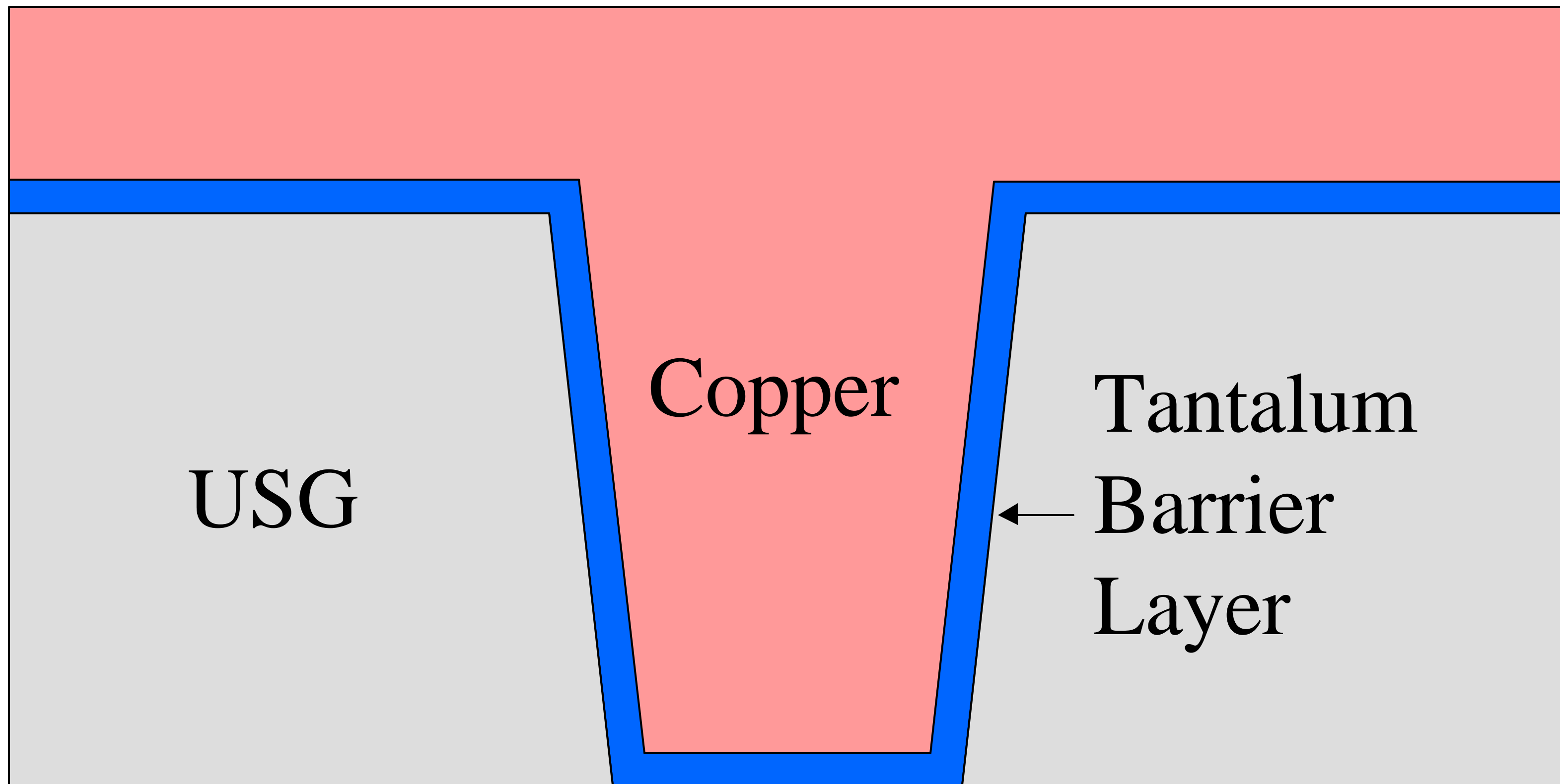
Copper CMP

- CuO_2 is porous and can't form a passivation layer to stop further copper oxidation
- Additive is needed to enhance passivation
- NH_3 is one of additives used in slurry
- Other additives such as NH_4OH, ethanol or benzotriazole can also be used as complexing agents to reduce wet etch effect

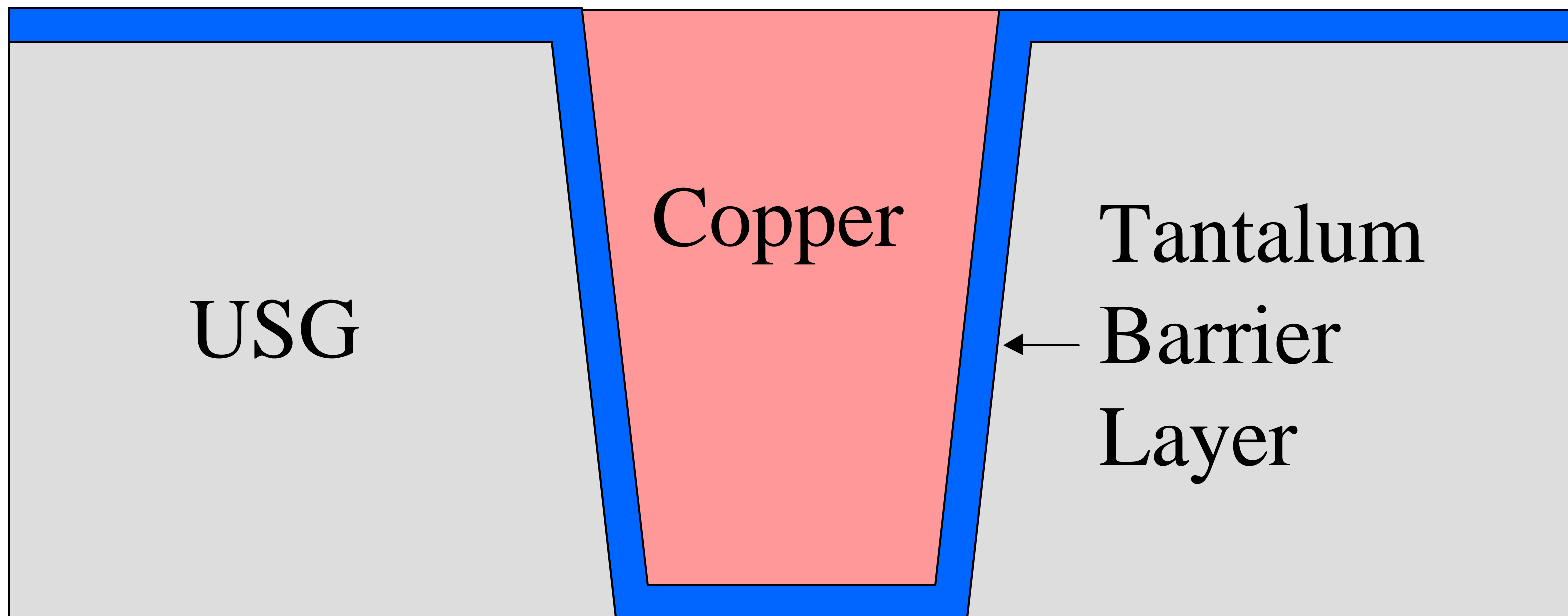
Copper CMP

- Dual-damascene copper metallization
- Both bulk Cu and barrier Ta layer need to be removed by the CMP process.
- Cu slurry can't effectively remove Ta, the lengthy over polishing step for Ta removal can cause copper recess and dishing effects

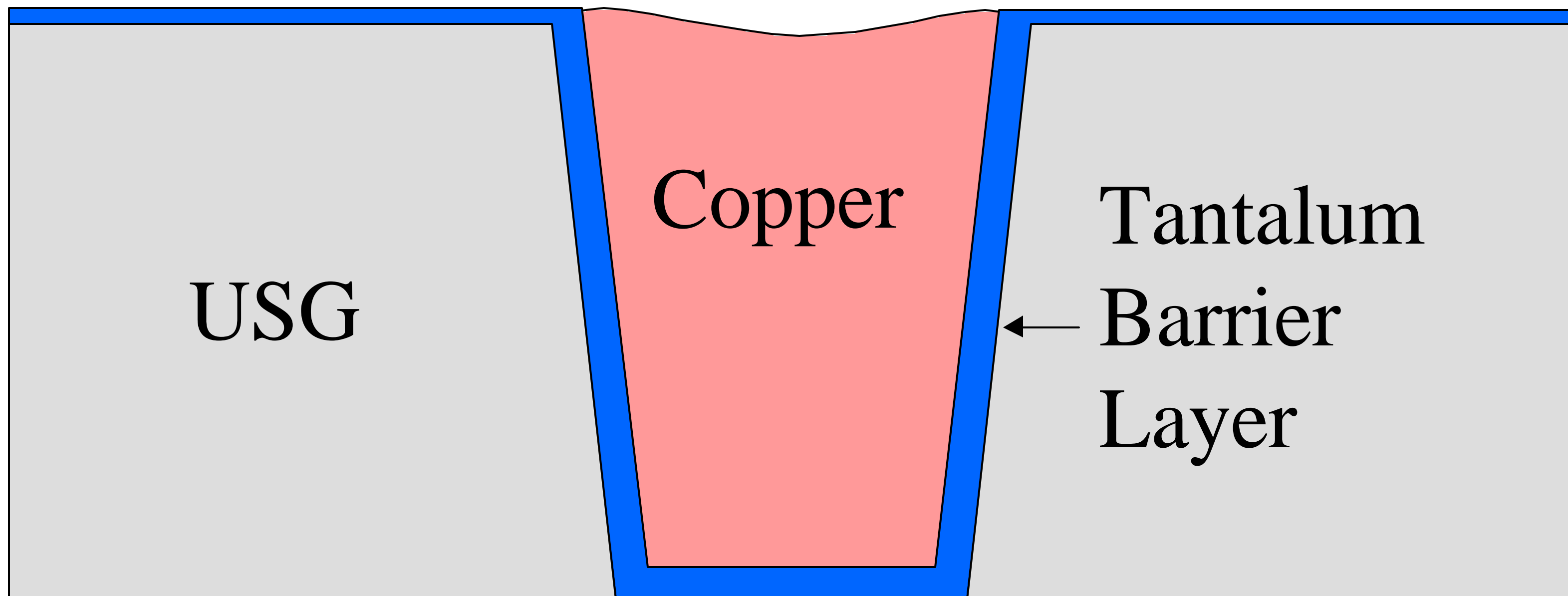
Copper Deposition



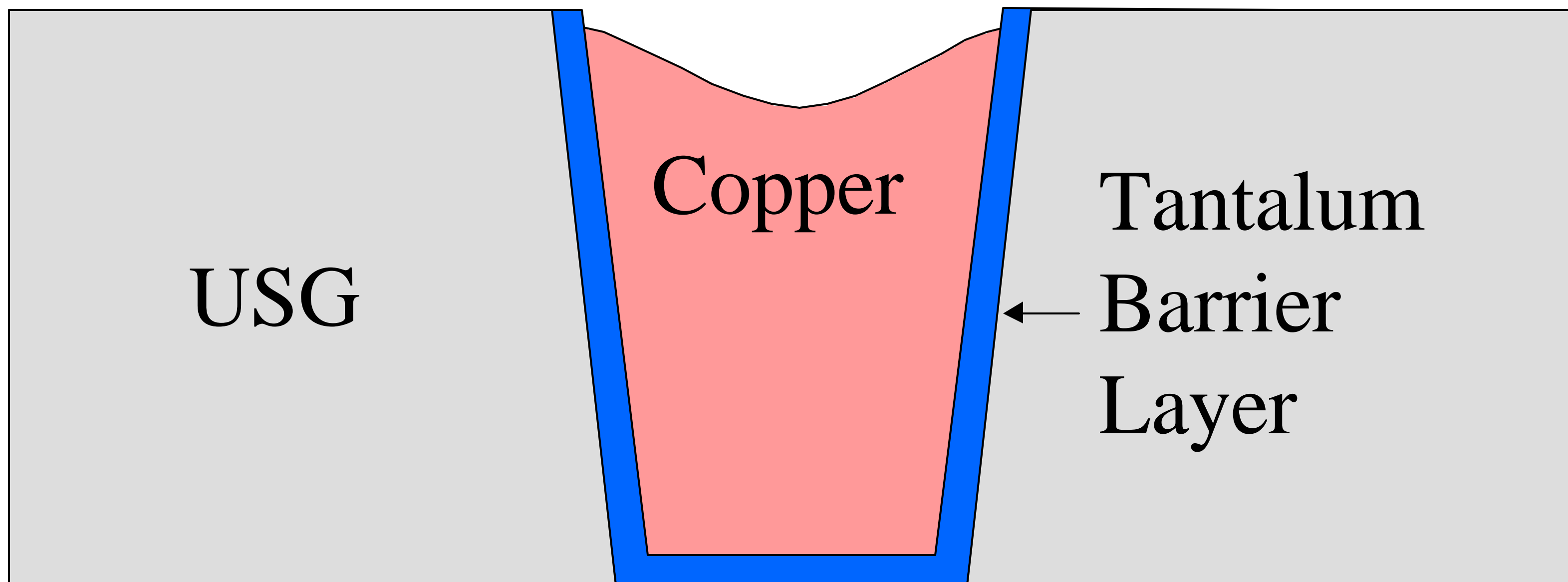
Copper CMP



Over Polish to Remove Tantalun



Copper Dishing and Recessing



Copper CMP

- Two-slurry polishing
- The first slurry remove bulk copper layer
- The second slurry remove Ta barrier layer
- The two-slurry CMP process reduces
  - Copper recessing and dishing
  - Oxide erosion
- Multiple polishing platens greatly simplifies multi-slurry CMP processing

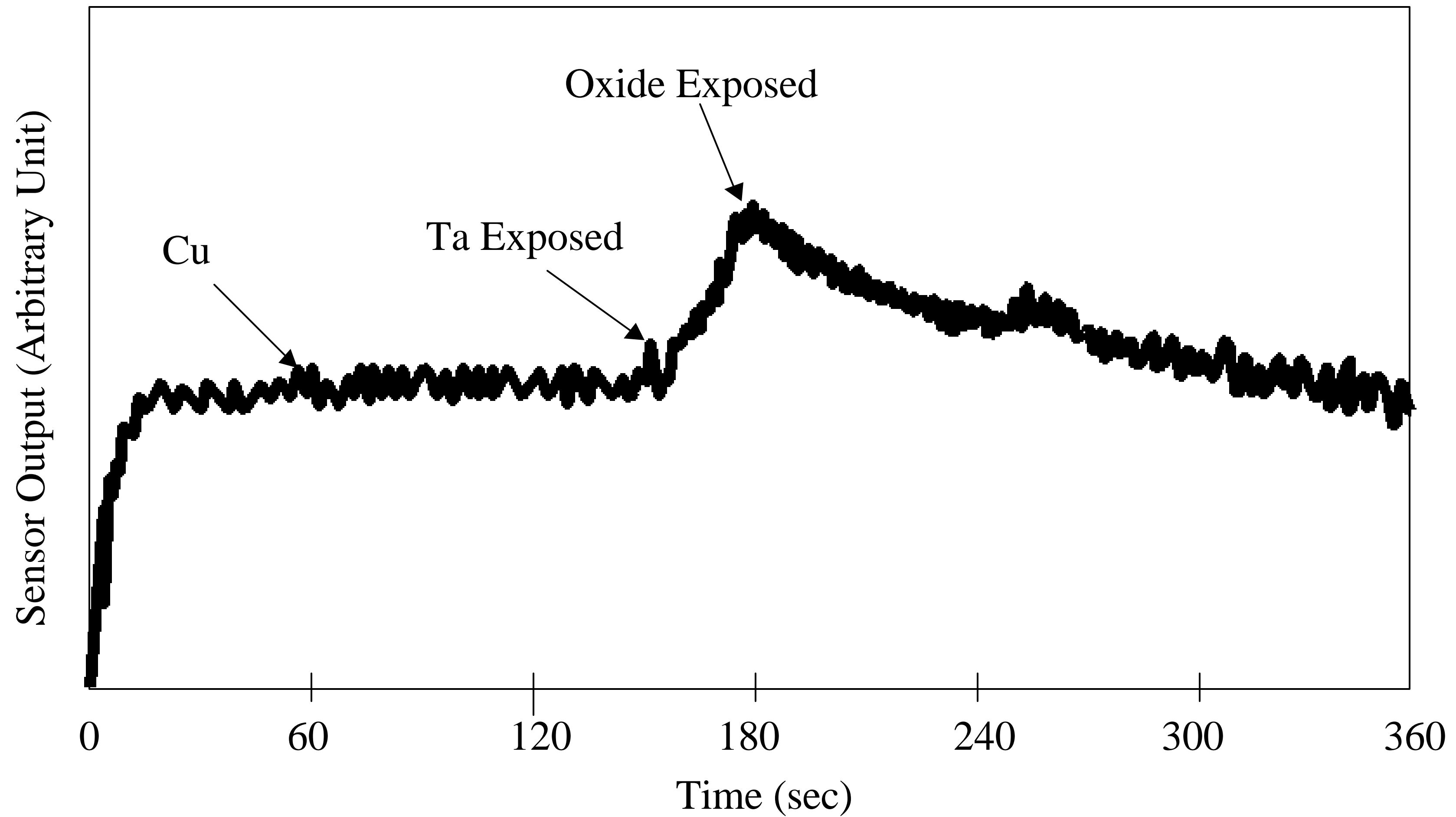
CMP Endpoint Detection

- Monitoring the motor current
- Optical measurement

Motor Current CMP Endpoint

- When CMP process closing to end, polish pad start to contact and polish underneath layer
- Friction force start to change
- Current of the polish head rotary motor will change to keep constant pad rotation rate
- Monitoring the change of motor current can find endpoint of the CMP process

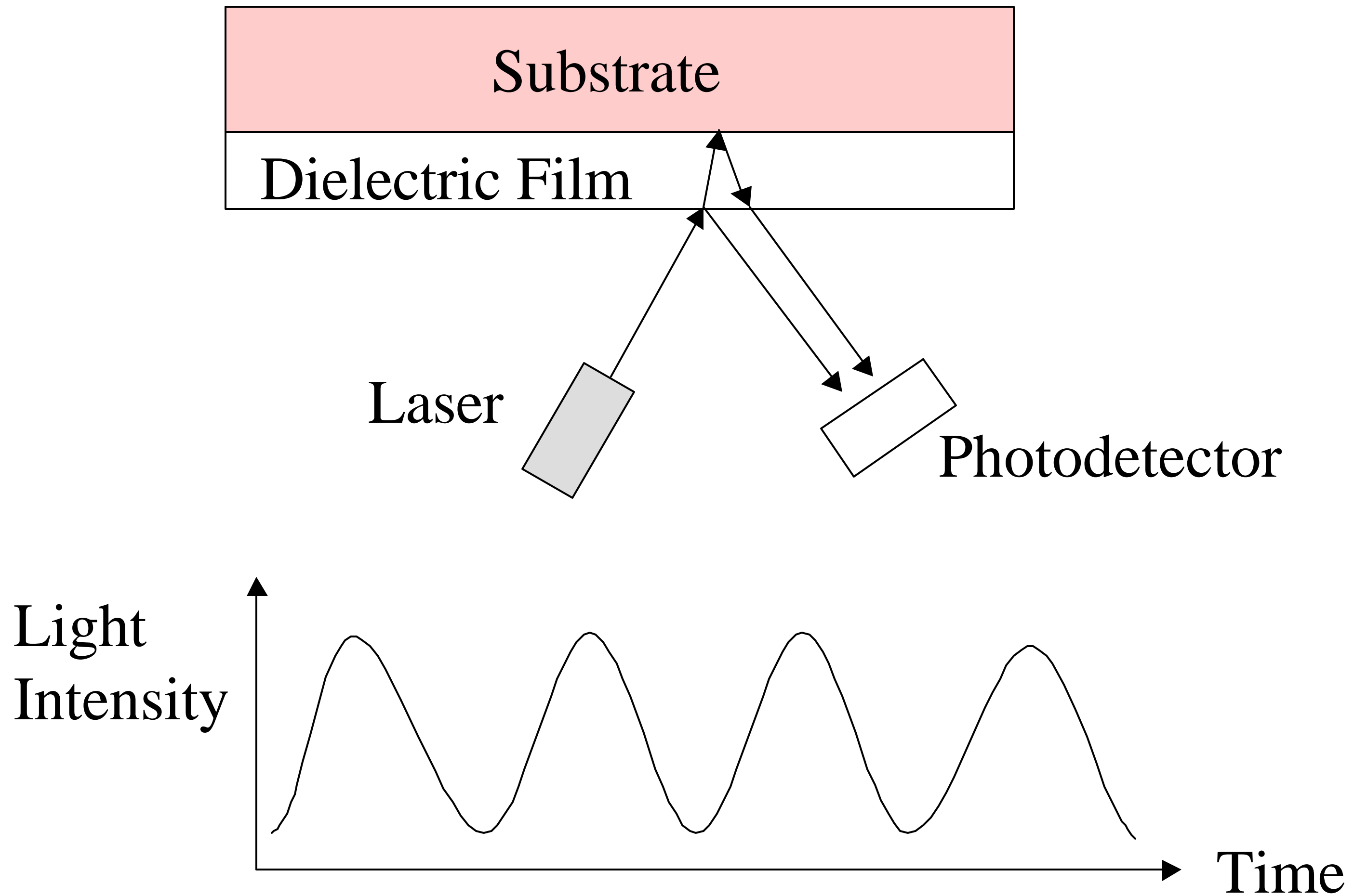
Motor Current During Copper CMP



Optical Endpoint: Dielectric

- Endpoint by either thickness measurement
- Reflected lights interfere with each other
- Constructive and destructive interference
- Change of the film thickness causes the periodically changes of interference state
- Dielectric film thickness change can be monitored by the change of reflection light

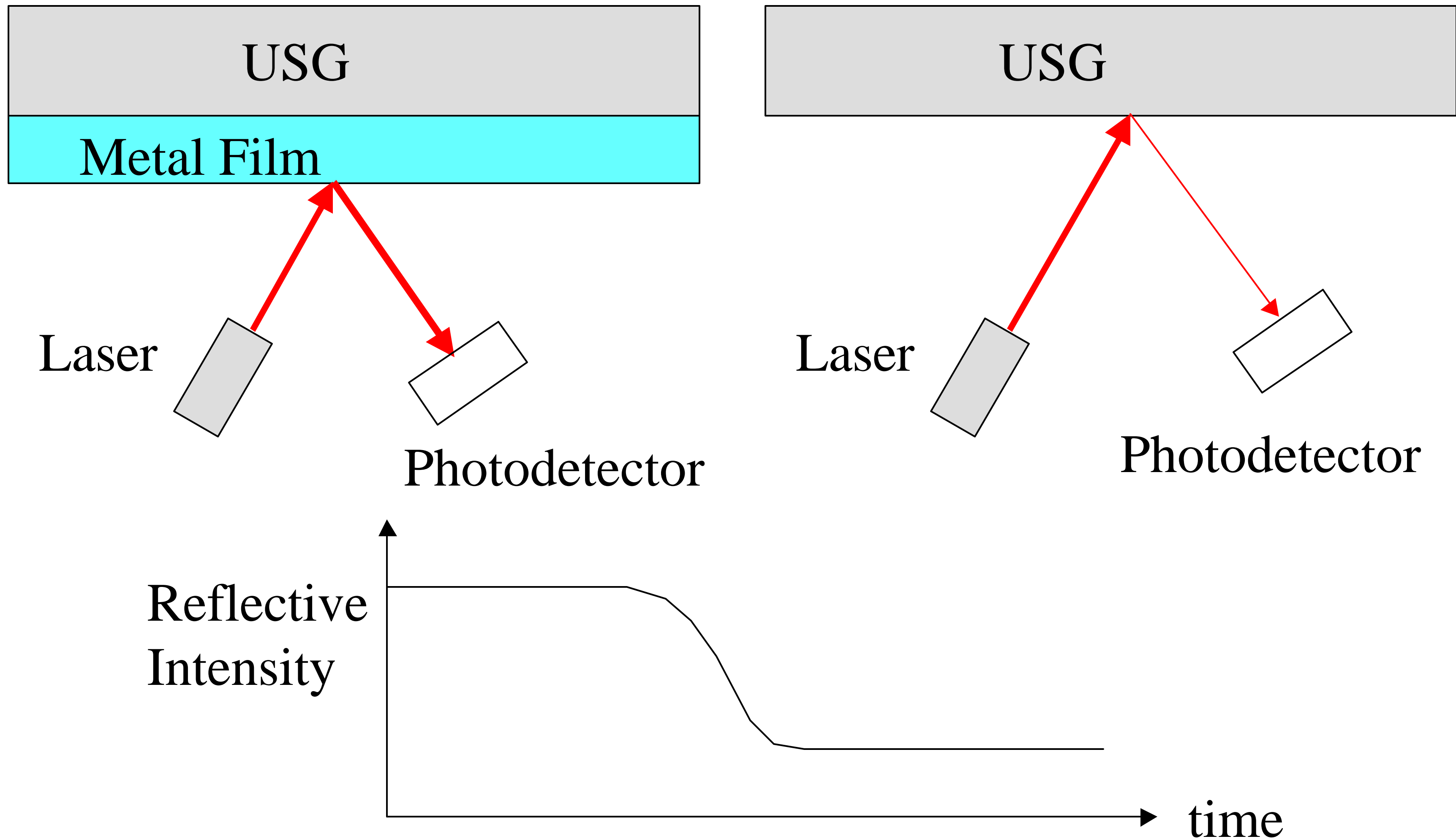
Endpoint of Dielectric CMP



Optical Endpoint: Metal

- The change of reflectivity can be used for metal CMP process endpoint
- Usually metal surface has high reflectivity
- Reflectivity significantly reduces when metal film is removed
- Trigger endpoint

Endpoint of Metal CMP



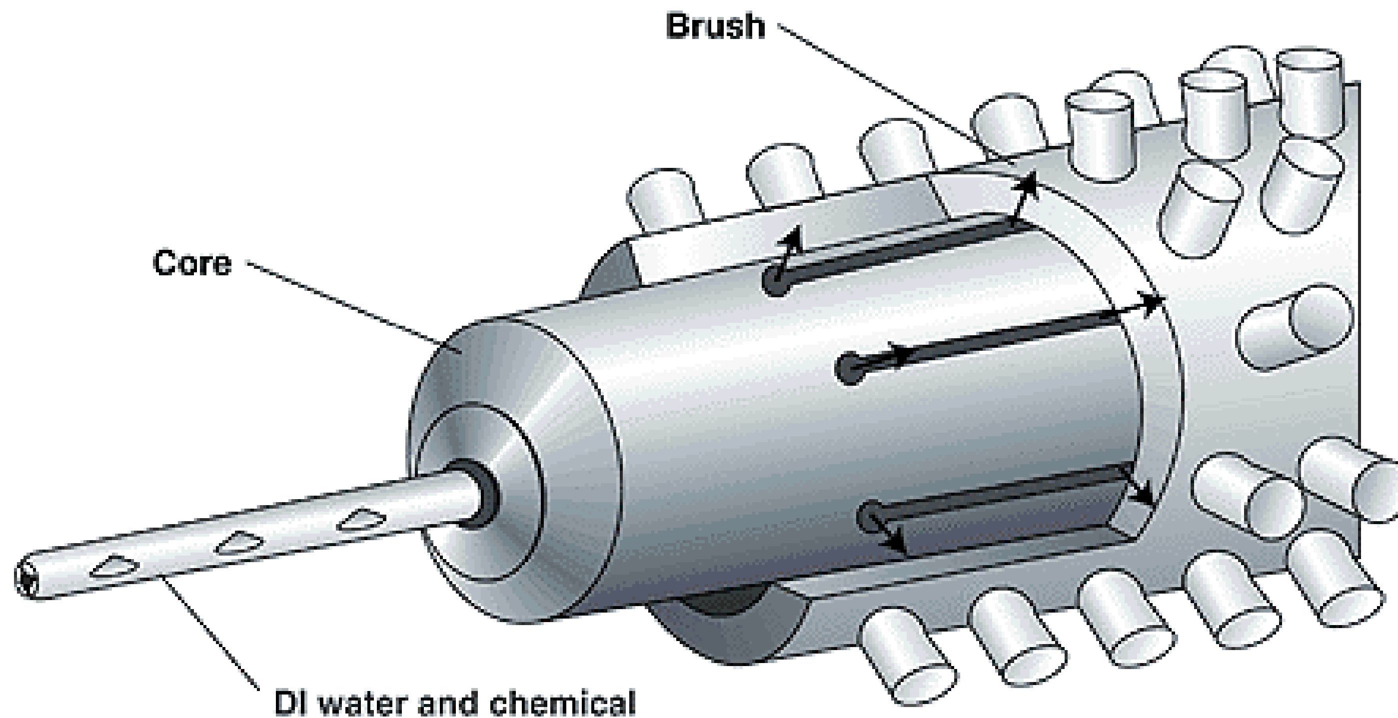
Post CMP Clean

- Post-CMP cleaning need remove both particles and other chemical contaminants
- Otherwise, defect generation and low yield
- Mechanical scrubbing cleaners with DI water
- Larger DI water volume, higher brush pressure high cleaning efficiency
- Three basic steps: clean, rinse, and dry

Post CMP Clean

- Usually brush is made of porous polymers, allows chemicals to penetrate through it and deliver to wafer surface
- Double-sided scrubbers are used in the post-CMP clean process

Brush System



Post CMP Clean

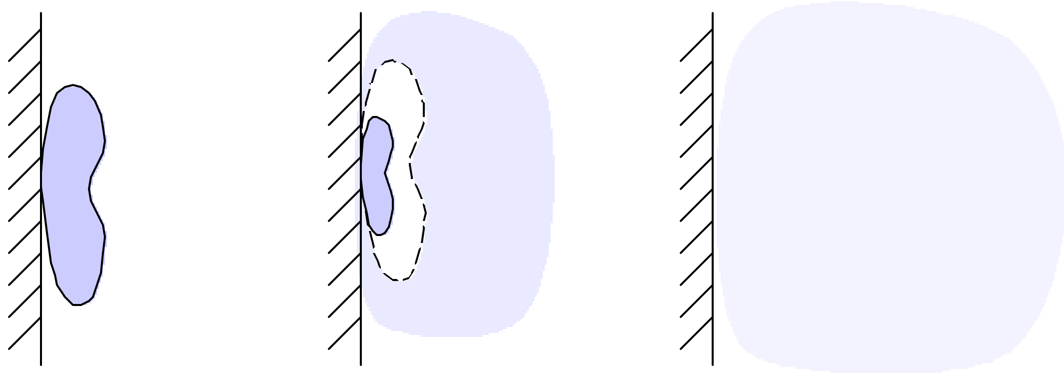
- Slurry particles can chemically bond to atoms on wafer surface if slurry dried
- Chemical additives, such as NH_4OH, HF or surfactants is needed to remove bonded particles by weakening or breaking the bonds
- Additives also help particles diffuse away from the surface

Post CMP Clean

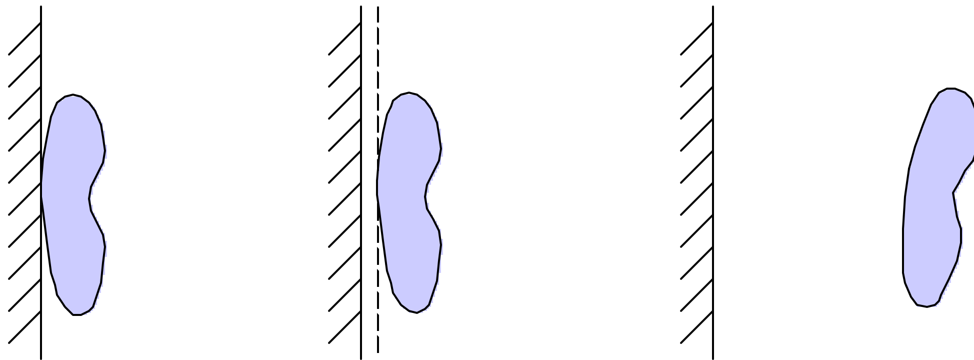
- Chemical solution is also used to adjust the wafer and particle surface charges so that electrostatic repulsion keeps particles from re-deposition on the surface
- Acidic solutions can be used to oxidize and dissolve organic or metal particles

Particle Removal Mechanisms

Acidic Solution: Oxidation and Dissolution



Alkaline Solution: Surface Etch and Electrostatic Repulsion



Post Oxide CMP Clean

- Silica particles adhere to or embedded in oxide surface
- Usually an alkaline chemical, NH_4OH, is used for post oxide CMP clean
- The alkaline solution charges both silica particles and oxide surface negatively
- Electrostatic force expels particles from the surface

Post Oxide CMP Clean

- HF is used to remove particles with strong molecule bonds with surface,
- Breaking the bonds, dissolving silica particles and some oxide surface
- Megasonics (MHz ultrasound wave) is commonly used to release shock waves that help dislodge the particles
- DI water rinse

Post Tungsten CMP Clean

- Tungsten slurries are much harder to remove than oxide slurries.
- DI wafer with NH_4OH is commonly used
- $Fe(NO_3)_3$ as the oxidant results in high Fe^{3+} ion concentration in the solution.
- The Fe^{3+} ion interacts with OH^- to form $Fe(OH)_3$ particulate that grow to 1 micron

Post Tungsten CMP Clean

- The $Fe(OH)_3$ particles can cause high surface defect density and contaminates the brush
- Commonly called *brush loading*
- The defect caused by $Fe(OH)_3$ particles can be reduced by using 100:1 HF clean
- DI water rinse

Wafer Drying

- Residue-free drying process
- Physically removal, without water evaporation
  - Evaporation drying cause contamination by leaving dissolved chemicals in DI water behind
- Most commonly used technique: spin-drying
  - Centrifugal force drives water out the wafer
- Ultra-clean dry air or nitrogen flow remove water from wafer center

Wafer Drying

- Vapor drying
  - Ultra-pure solvent with high vapor pressure
  - Most commonly used: isopropyl alcohol (C_3H_8O, IPA)
  - Displace water from the wafer surface

Dry-in Dry-out CMP

- Integrated CMP and post-CMP clean systems
- Allow so-called “dry-in dry-out” process
- CMP, post-CMP clean, and wafer drying processes in one sequence
- Improve process through put and yield

Process Issues

- CMP process is a relatively new process
- Very limited process details are available
- The main concerns for CMP processes
  - Polishing rate, planarization capability, within die uniformity, within wafer uniformity, wafer to wafer uniformity, removal selectivity, defects and contamination control

Process Issues: Polish Rate

- Polish rate affected by
  - Downforce pressure
  - Pad hardness
  - Pad condition
  - Applied slurry
  - Rotation speed

Process Issues: Planarization

- Planarization capability is mainly determined by the stiffness and surface condition of the polish pad.

Process Issues: Uniformity

- Uniformity affected by
  - Polish pad condition,
  - Down force pressure,
  - Relative speed of the wafer to the polish pad,
  - Curvature of wafers, which is related to film stress
- Downforce pressure distribution is the most important knob to control the CMP uniformity

Process Issues: Removal Selectivity

- Mainly controlled by the slurry chemistry
- Also related to the pattern density
  - determined by the design layout.

Process Issues: Defects

- There are many different kinds of defects, which relate with many different process parameters

Process Issues: Contamination Control

- Contamination Control:
  - Isolate CMP bay from other processing areas
  - Restrict movement between CMP bay and other area
- Dedicate copper CMP tools
  - Avoid copper contamination of the silicon wafer
  - Copper contamination can cause unstable performance of MOSFETs and ruin the IC chips

Process Issues: Contamination Control

- IF slurry has spilled, it is very important to **immediately** wash and clean it thoroughly
- Dried slurry leaves huge amount of tiny particles, which is easy to airborne can become a source of particle contamination.

Future Trends

- More widely used copper CMP
- Copper and low-κ dielectric interconnection
  - low-κ dielectric CMP
  - Copper and barrier layer CMP processes with high selectivity to low-κ dielectric
- DRAM applications: CMP processes involve with polysilicon and high-κ dielectric

Summary

- Main applications of CMP are dielectric planarization and bulk film removal
  – STI, PMD and IMD planarization, tungsten plugs, and dual damascene copper interconnections.
- Need CMP for <0.25 μm features patterning due to depth-of-focus requirement
- Advantages of CMP: high-resolution patterning, higher yield, lower defect density

Summary

- A CMP system usually consists of wafer carrier, a polishing pad on a rotating platen, a pad conditioner, and a slurry delivery system
- Oxide slurries: alkaline solutions at 10< pH < 12 with colloidal suspension silica abrasives
- Tungsten slurries are acidic solutions at 4< pH < 7 with alumina abrasives
- Copper slurries: acidic with alumina abrasives

Summary

- The important factors of CMP processes:
  - Polish rate, planarization capability, selectivity, uniformities, defects and contamination controls
- Polish rate affects by: downforce pressure, pad stiffness, pad surface condition, relative speed between pad and wafer, and slurry type.
- CMP uniformity affects by down force pressure distribution, pad stiffness, and pad condition

Summary

- The removal selectivity is mainly determined by the slurry chemistry
- Oxide CMP process: silica particles form chemical bonds with surface atoms and abrade removal of materials from the surface
- Two metal removal mechanisms in metal CMP process: wet etch and passivation/abrade

Summary

- Endpoint detections
  - Optical
    - Thickness measurement for dielectric film
    - Reflectivity measurement for metal film
  - Motor current
- Post-CMP clean reduce defects and improve yield

Chapter 13
Process Integration

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Objectives

- List three isolation methods
- Describe sidewall spacer process and application
- Explain the V_T adjustment implantation
- Name three conductors used for MOSFET gate
- List three metals used for interconnection process
- List basic steps for copper metallization process
- Identify the material most commonly used as final passivation layer for an IC chip

Introduction

- It takes up to 30 masks and several hundreds process steps to finish an IC chip fabrication.
- Every step is related to other steps.
- CMOS processes
  - Front-end:
    - well formation, isolation, and transistor making
  - Back-end
    - Interconnection and passivation

Wafer Preparation

- CMOS IC chips commonly used <100> wafer
- Bipolar and BiCMOS chips usually use with <111> wafers orientation.
- 1960 to mid-1970s, mainly PMOS, n-type wafer
- After mid-1970s, mainly NMOS, p-type wafer
- CMOS developed from NMOS process, for historical reason more fabs use p-type wafer

NMOS and CMOS Processes

- The simplest NMOS IC processing had five mask steps: activation, gate, contact, metal, and bonding pad
- The early CMOS IC processing added three more mask steps: n-well (for p-type substrate), activation, gate, n-source/drain, p-source/drain, contact, metal, and bonding pad
- Both processes used p-type wafers

NMOS

Aluminum Silicon Alloy

Nitride

PSG

PSG

PSG

Field Oxide

Field Oxide

Poly Si

n^+

n^+

p-Silicon

Gate Oxide

CMOS of the Early 1980s

Nitride
USG
Al·Cu·Si
BPSG
SiO_2
Poly Si Gate
Nitride
LOCOS
n^+ n^+ p^+ p^+
p^+ p^+
N-well
P-type substrate
Gate Oxide
Isolation Implantation

Epitaxy Silicon Layer

- Bipolar transistors and BiCMOS chips require epitaxial silicon layer to form a buried layer
  - Some power devices even require wafers made by floating zone method
- When CMOS chip speed is not very high, it doesn't need the epitaxy layer
- High-speed CMOS chips need epitaxy layer

Epitaxy Silicon Layer

- Silicon wafers made by the CZ method always have some oxygen because quartz crucible
- Oxygen can reduce carrier lifetime and slow down the device
- The epitaxy silicon layer creates an oxygen-free substrate and help to achieve high device speed

Epitaxy Silicon Layer

- RCA clean to remove contaminants
- Anhydrate HCl dry clean helps to remove mobile ions and the native oxide
- Epitaxy growth: high temperature CVD
  - silicon source: SiH_4 or SiH_2Cl_2, or $SiHCl_3$
  - H_2 as process, carrier, and purge gas
  - AsH_3 or PH_3 as n-type dopant gas,
  - B_2H_6 as p-type dopant gas

Wafers Used for IC fabrication

- Advanced CMOS IC chips normally use p-type <100> single crystal silicon wafers with p-type epitaxial layer
- Bipolar IC chips usually use <111> wafers

Well Formation

- Single well
- Self-aligned twin well
- Double photo twin well

Single Well

- Early CMOS IC processing
- N-well on p-type wafer
- P-well on n-type wafer
- High energy, low current ion implantation
- Thermal anneal and drive-in

N-well Formation

Wafer clean

Screen oxide grow

Well mask

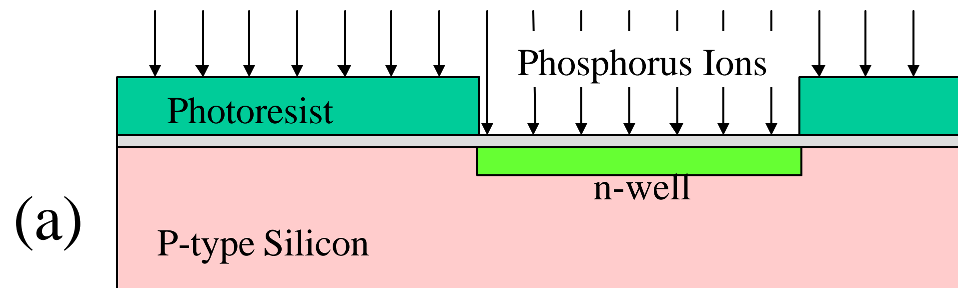
<u>Ion implantation</u> (a)

Photoresist strip

<u>Anneal and drive-in</u> (b)

Screen oxide strip (c)

(a)



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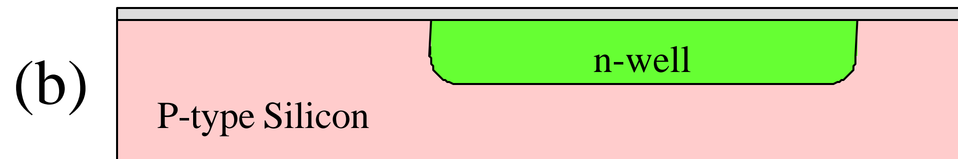

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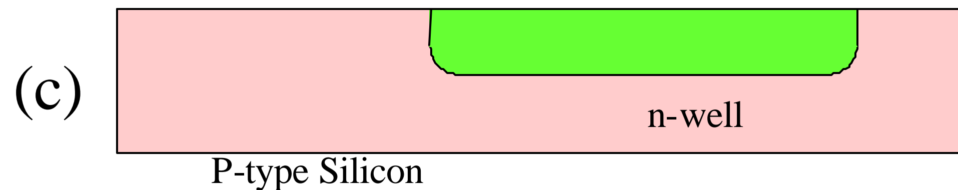
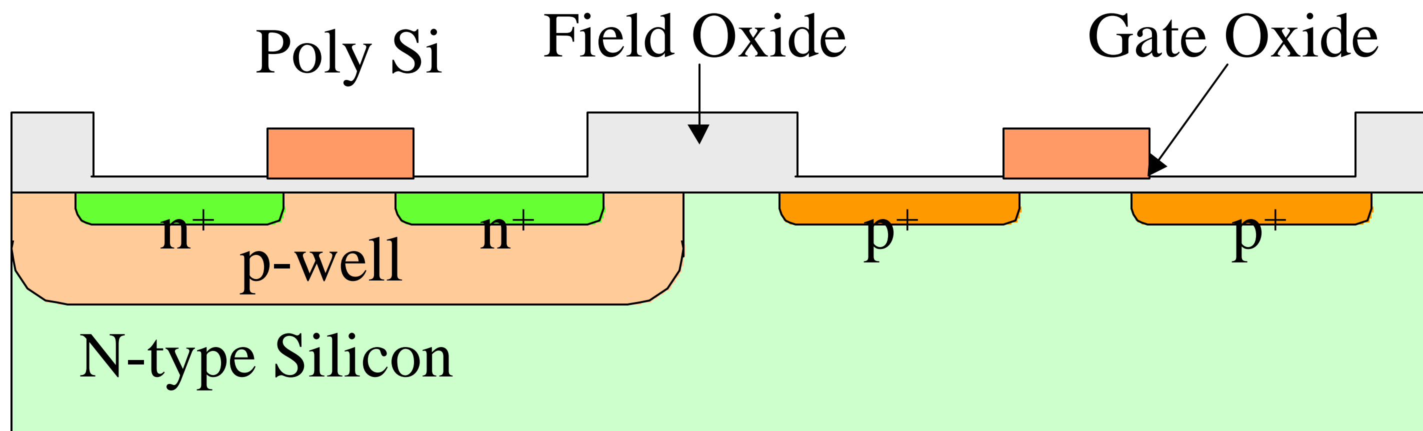
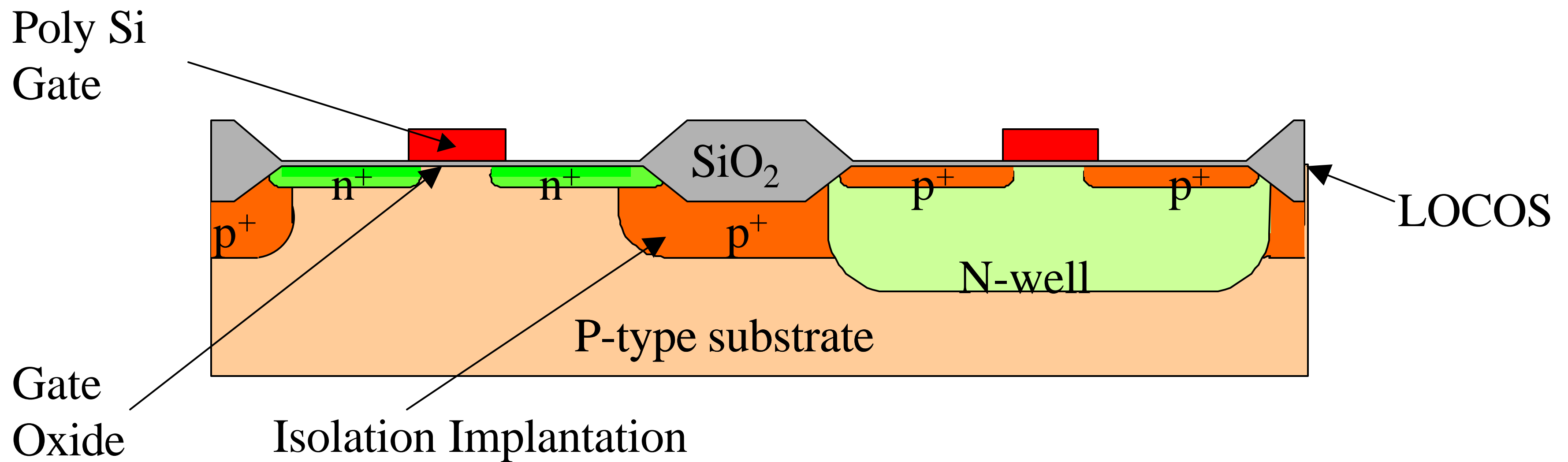


CMOS with P-well



CMOS with N-well

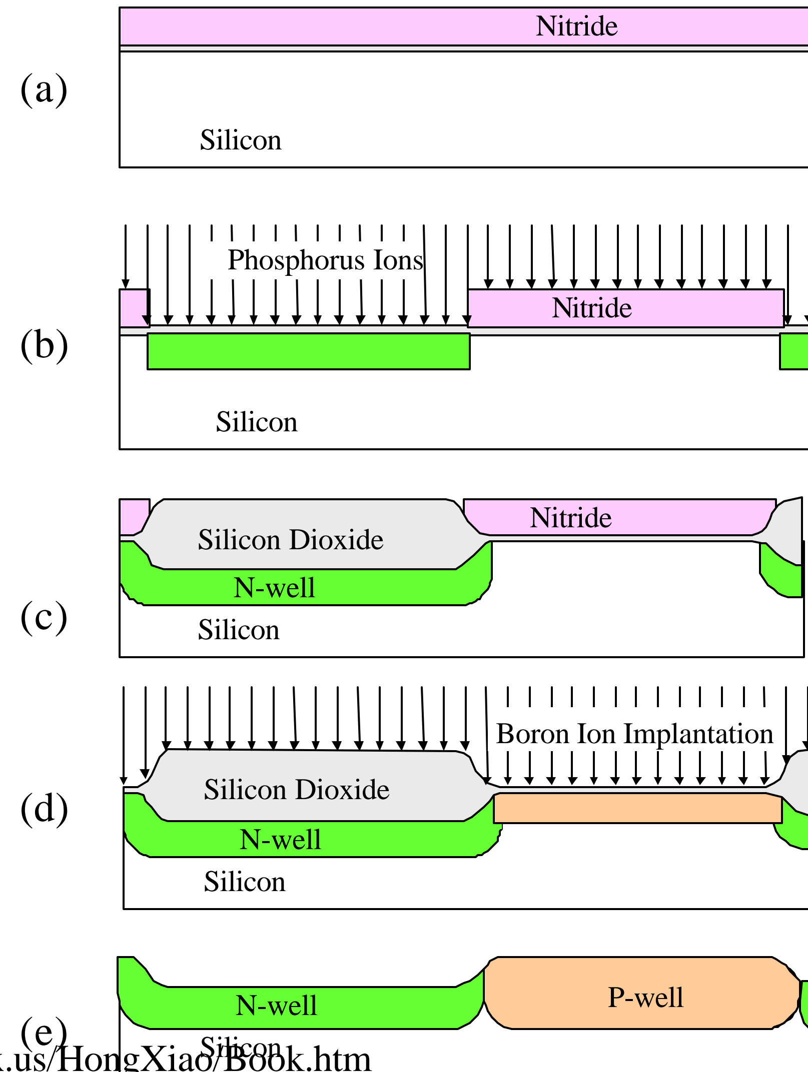


Self-aligned Twin Well

- More flexibility for the designers
- Self-aligned process save a mask step
- LPCVD Si_3N_4 is a very dense layer
- Block ion implantation on p-well
- Prevent oxidation on p-wee
- Oxide grown on n-well block p-well ion implantation

Self-aligned Twin Well

- •Wafer clean
- •Grow pad oxide
- •Deposit nitride (a)
- •N-well mask
- •Etch nitride
- •Strip photoresist
- •N-well implantation (b)
- •Anneal/drive-in and oxidation (c)
- •Strip nitride
- •P-well implantation (d)
- •Anneal and drive
- •Strip pad oxide (e)



Self-aligned Twin Well

- Advantage: reduce a photo mask step
  - Reduce cost
  - Improve IC chip yield.
- Disadvantage: wafer surface is not flat
  - n-well always has lower level than p-well
  - Affect photolithography resolution
  - Affect thin film deposition

Self-aligned Twin Well

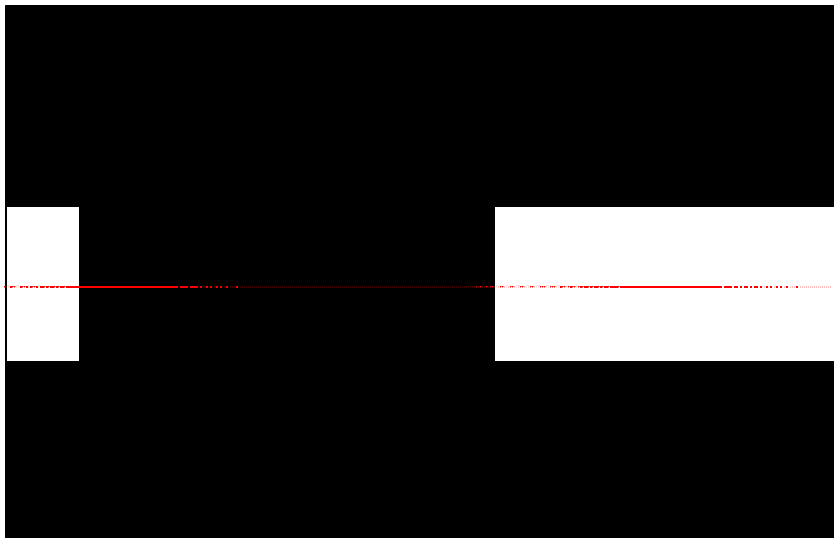
- N-well implant first
- Phosphorus diffuses slower than boron in single silicon
- If p-well implant first, boron in p-well could diffuse out of control during n-well anneal and drive-in

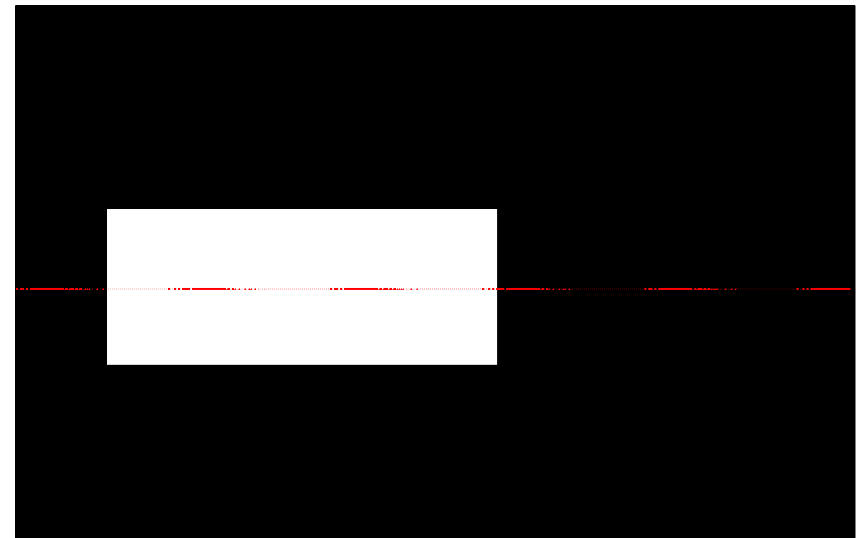
Twin Well

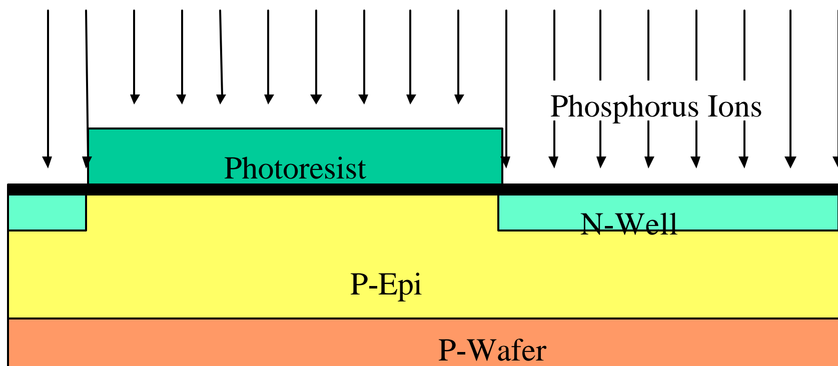
- Two mask steps
- Flat surface
- Common used in advanced CMOS IC chip

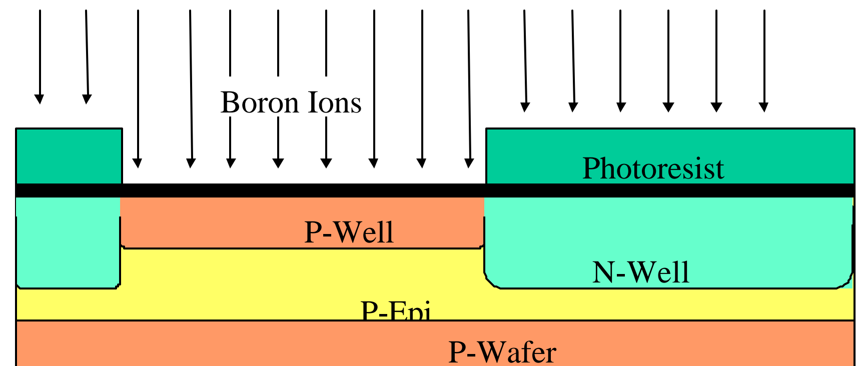
- High energy, low current implanters
- Furnaces annealing and driving-in

Twin Well









Isolations

- Blanket field oxide
- Local oxidation of silicon (LOCOS)
- Shallow trench isolation (STI)

Blanket Field Oxide

- Early years of IC industry
- Simple and strait forward
- Oxidation and etch
- Thickness is determined by V_{FT},
- V_{FT} >> V to prevent cross-talking

LOCOS Formation

Wafer clean

Grow pad oxide

LPCVD nitride (a)

Mask 1, LOCOS

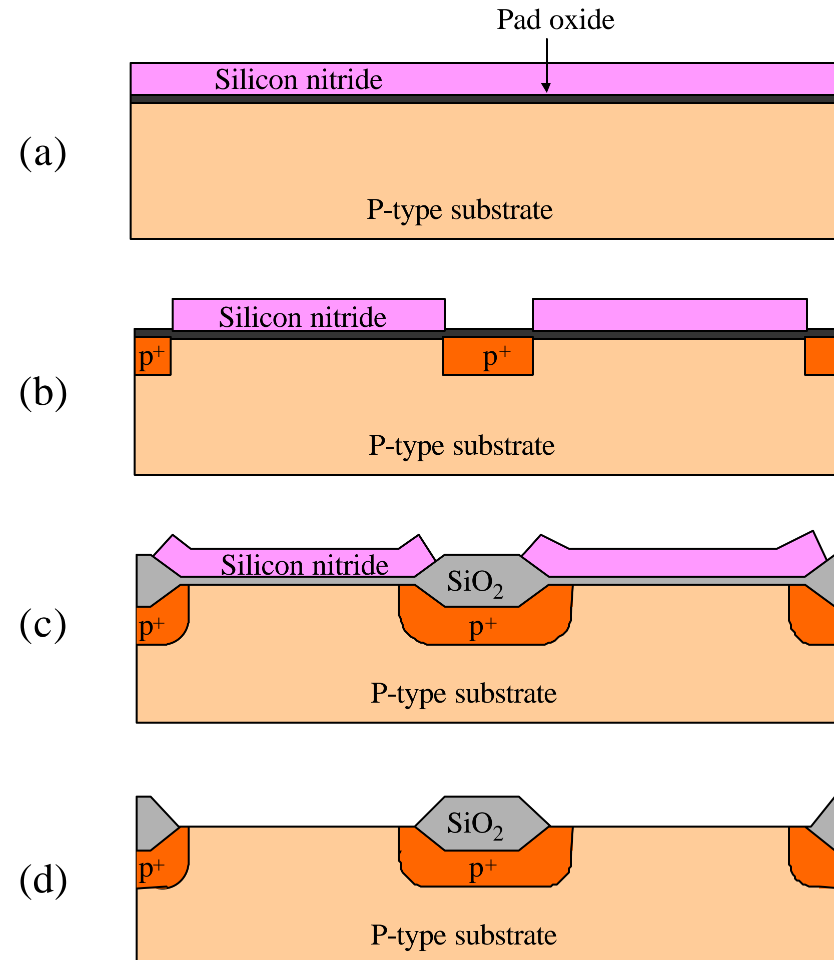
Etch nitride

Strip photoresist

Isolation implantation, boron (b)

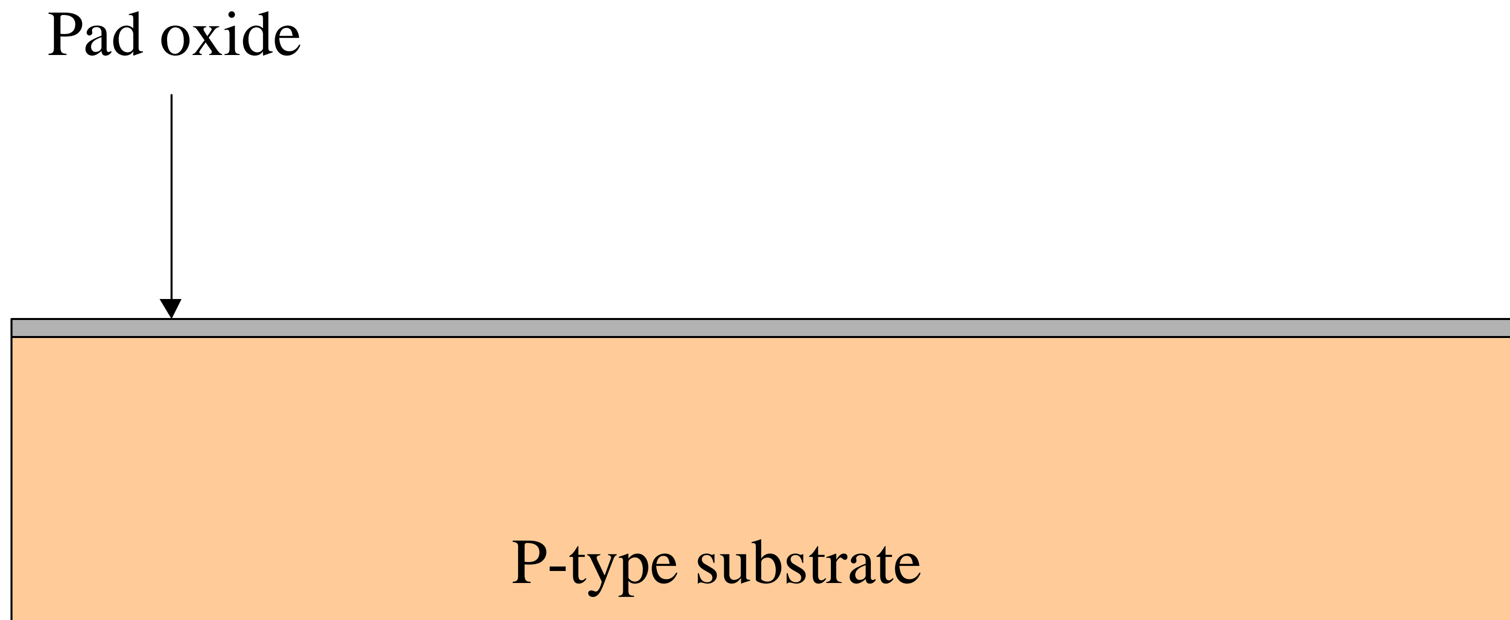
Wet oxidation, LOCOS formation (c)

Strip nitride and pad oxide (d)

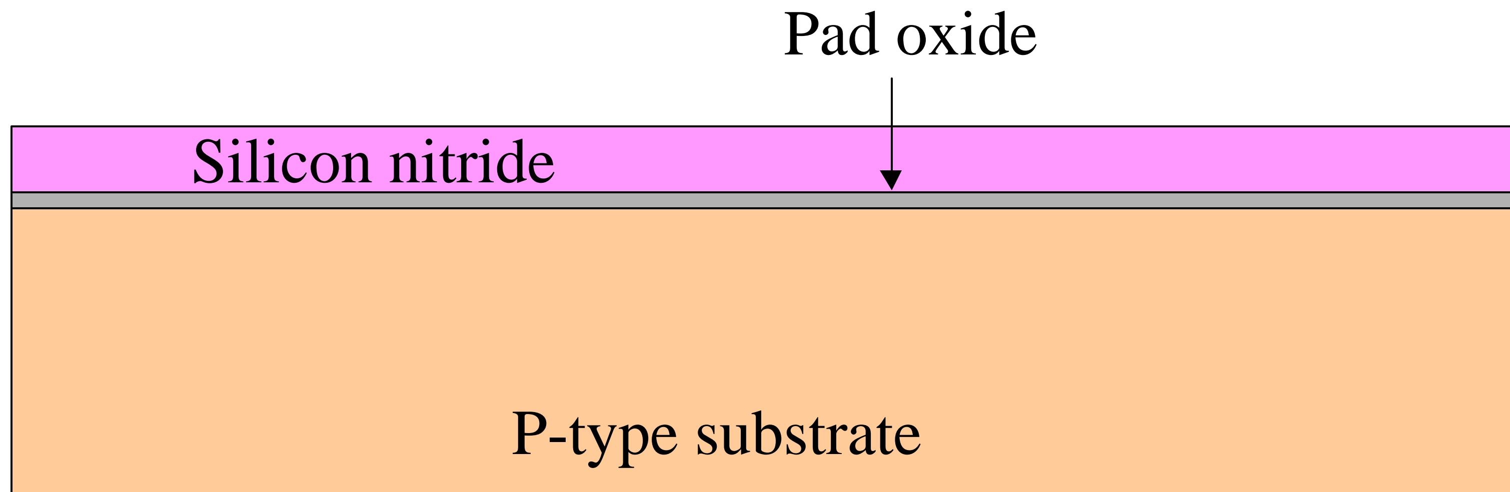


Wafer Clean

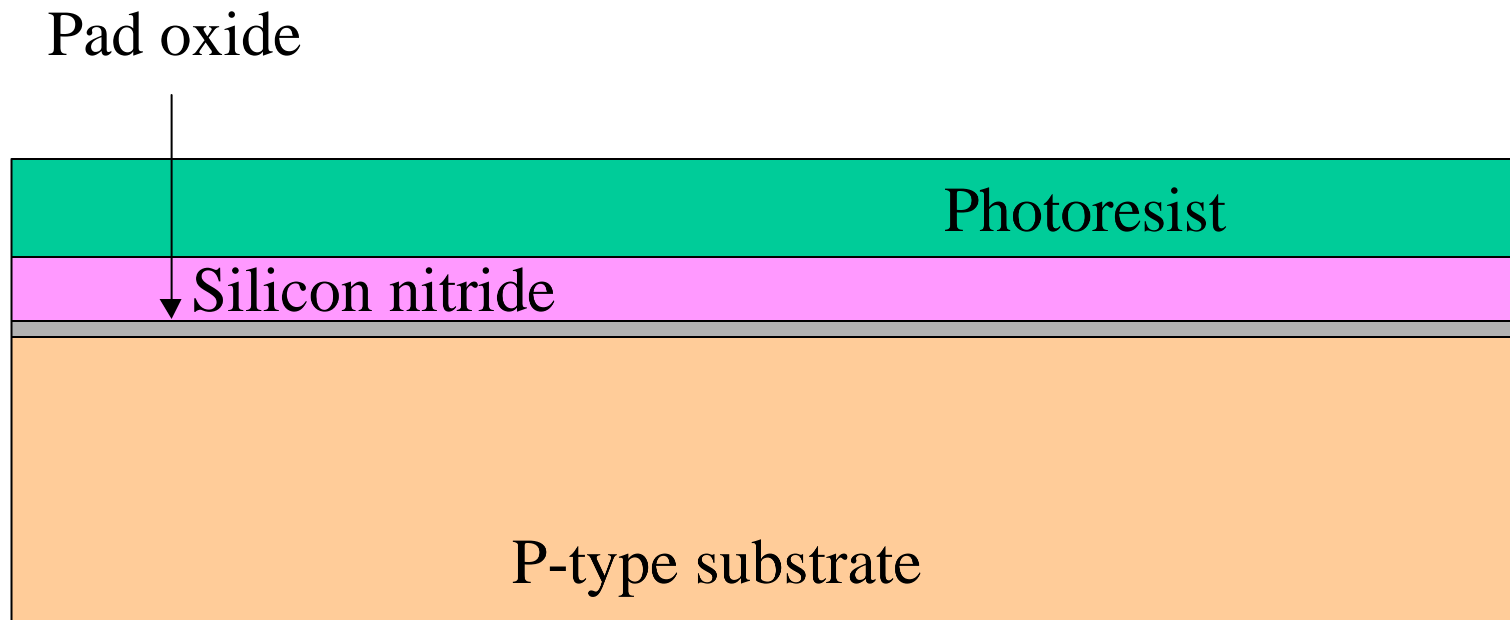
Pad Oxidation



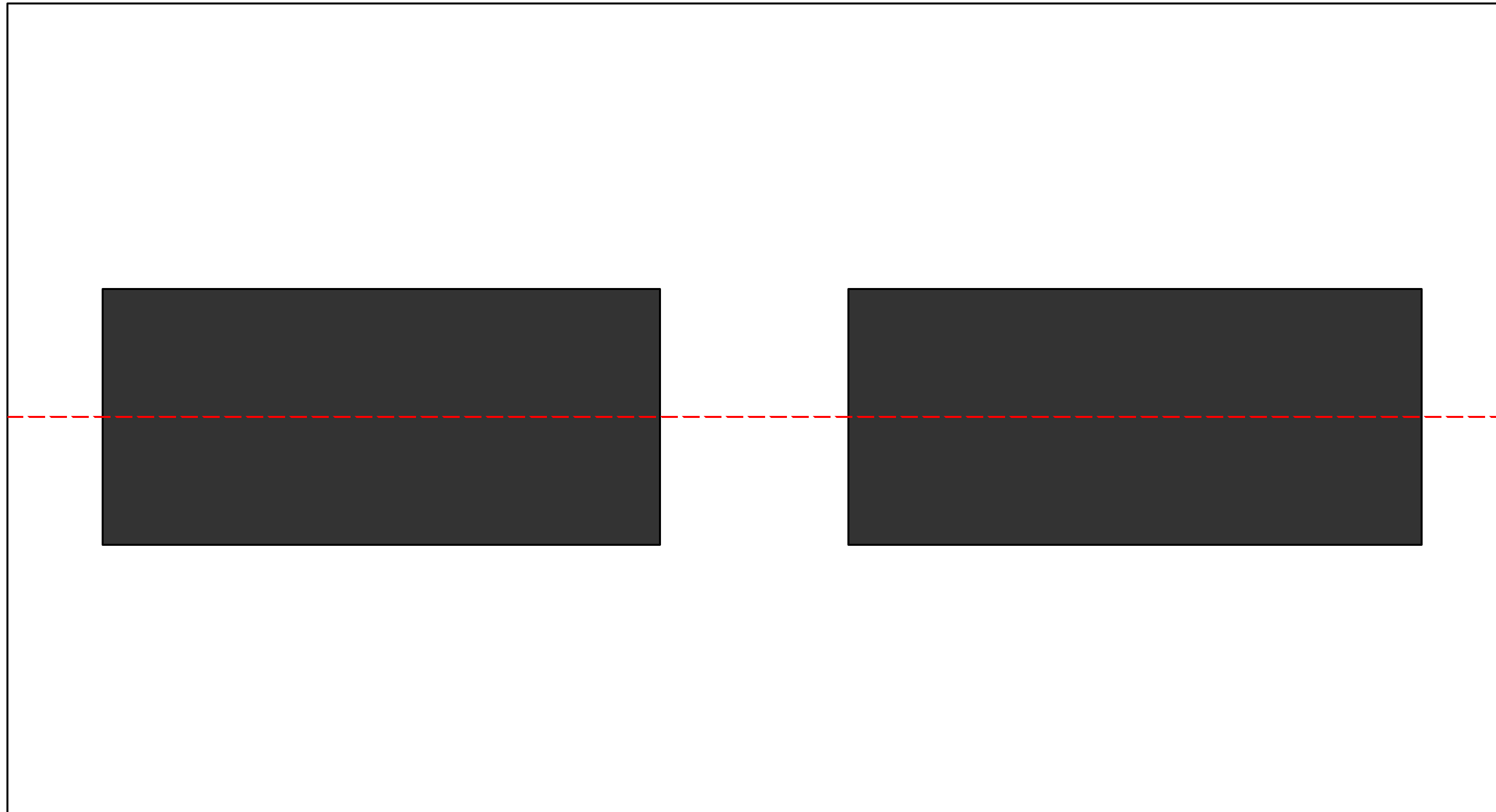
LPCVD Nitride



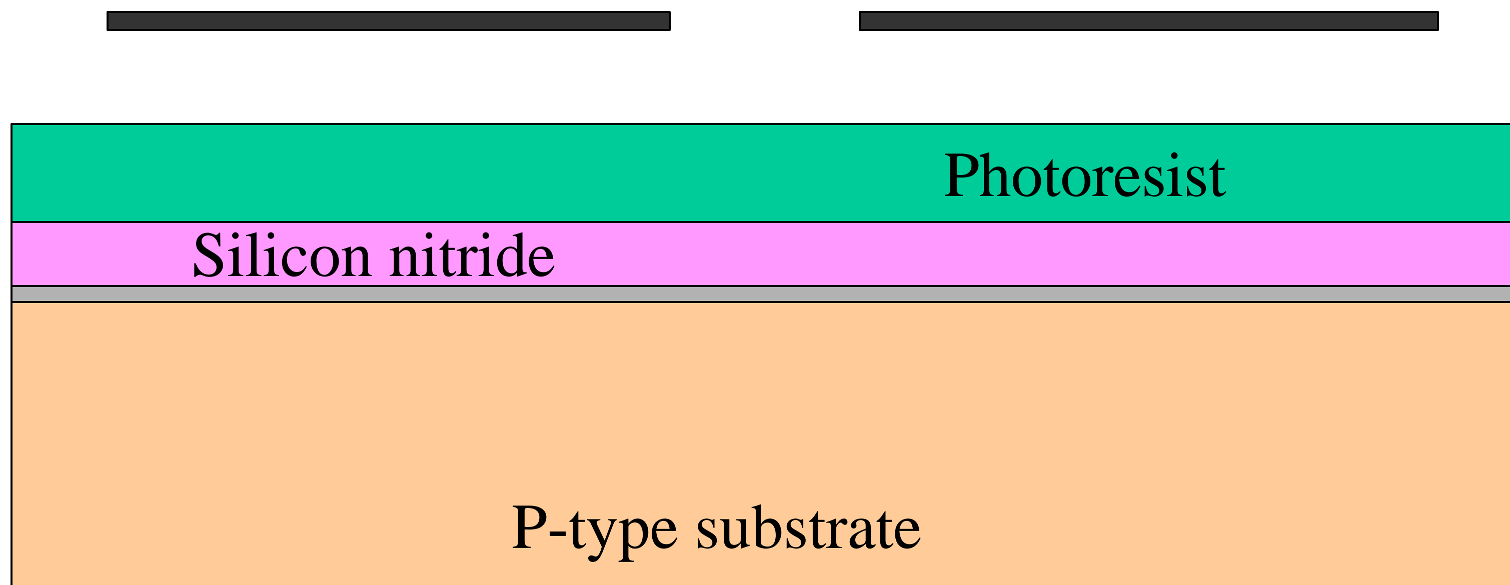
Photoresist Coating



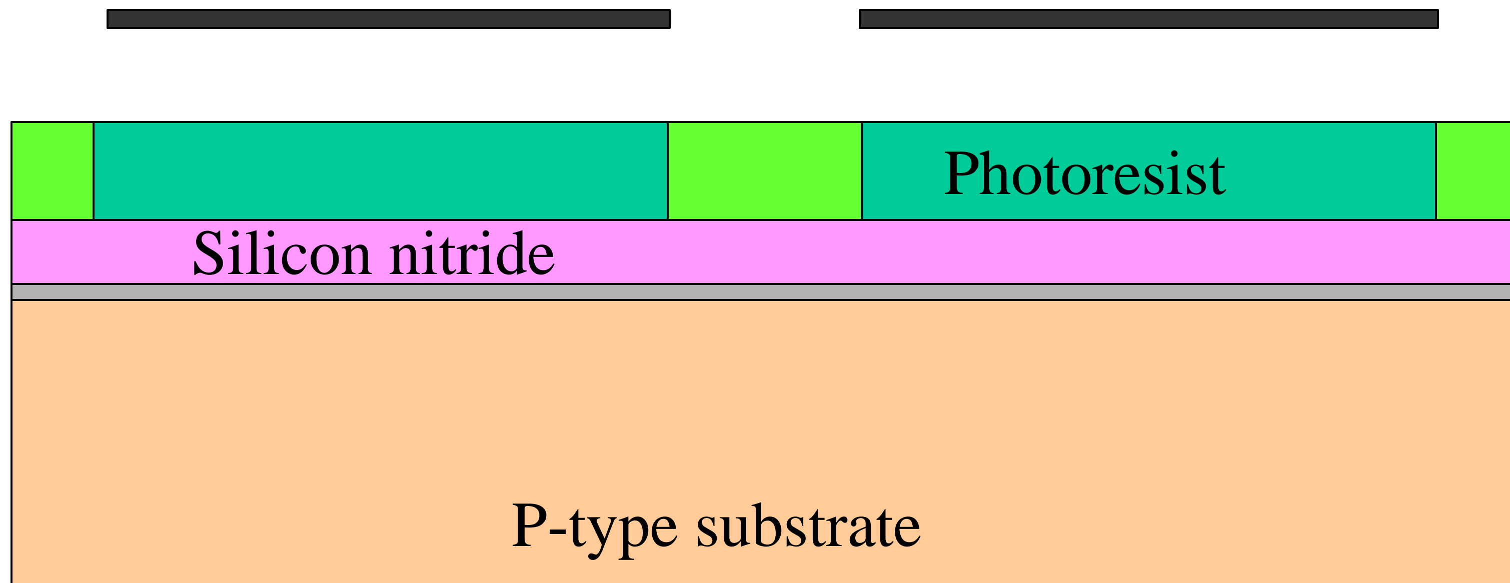
LOCOS Mask



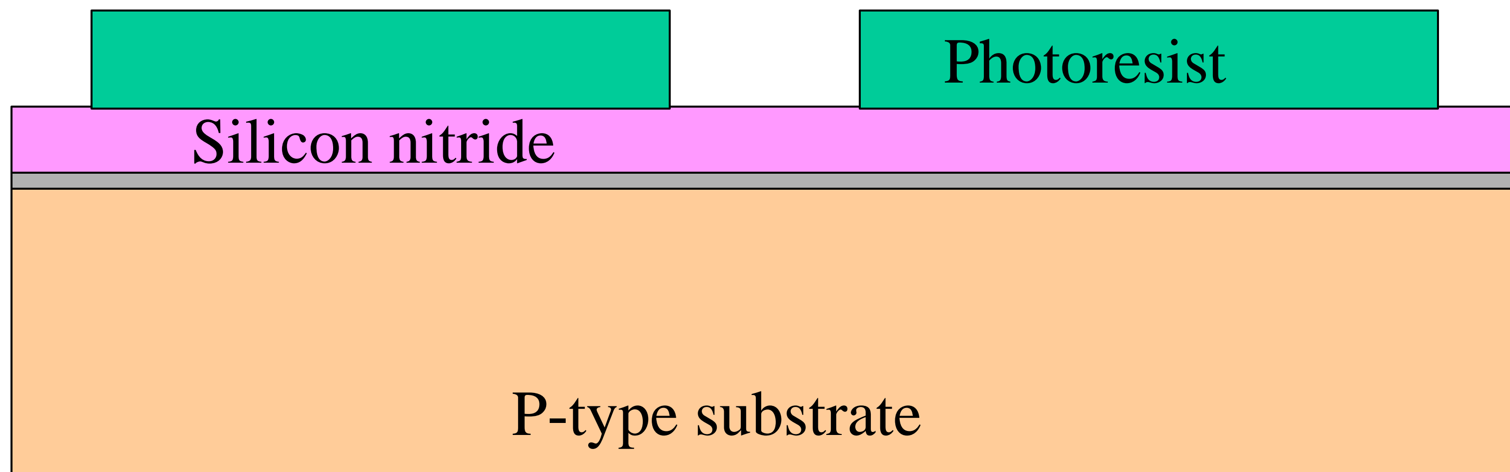
LOCOS Mask



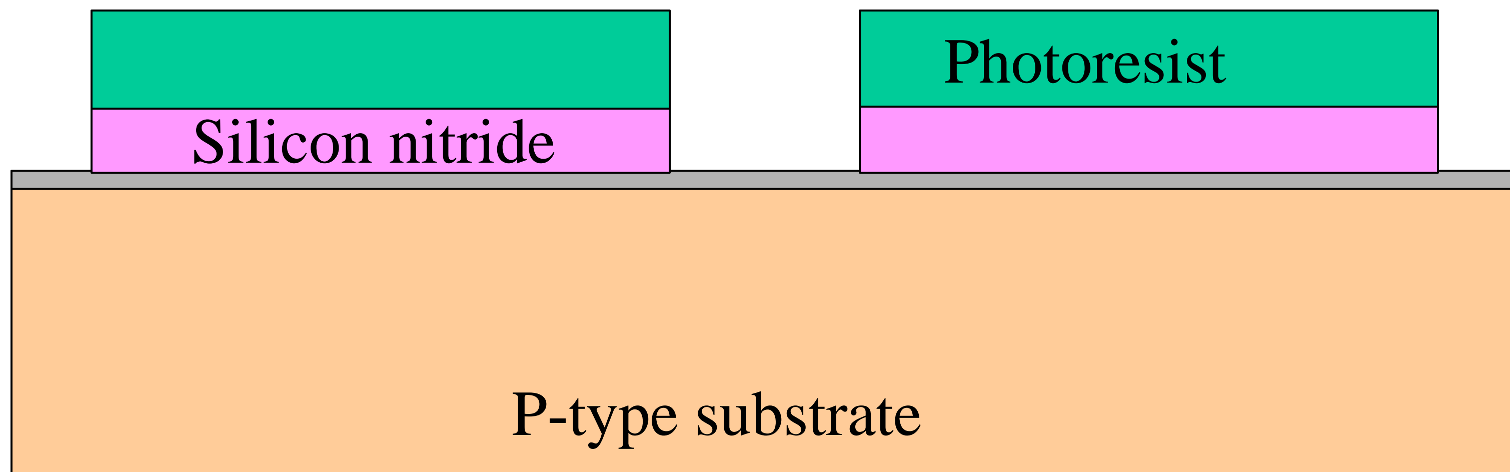
LOCOS Mask Exposure



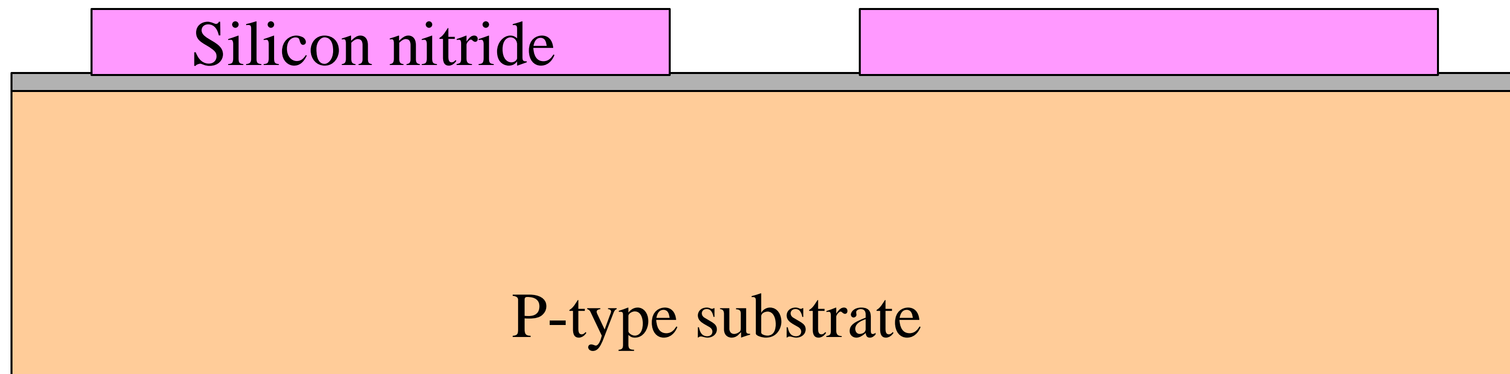
Development



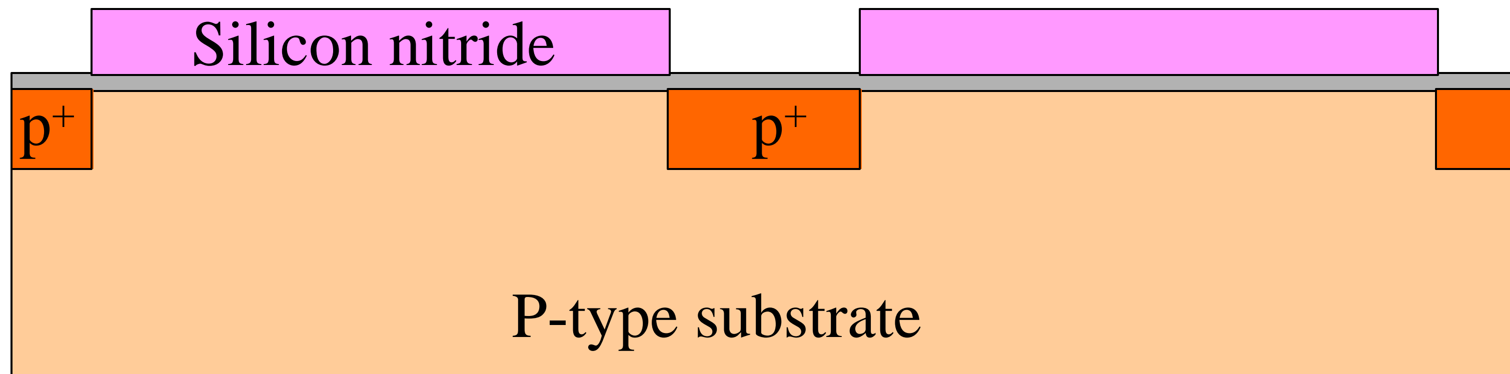
Etch Nitride



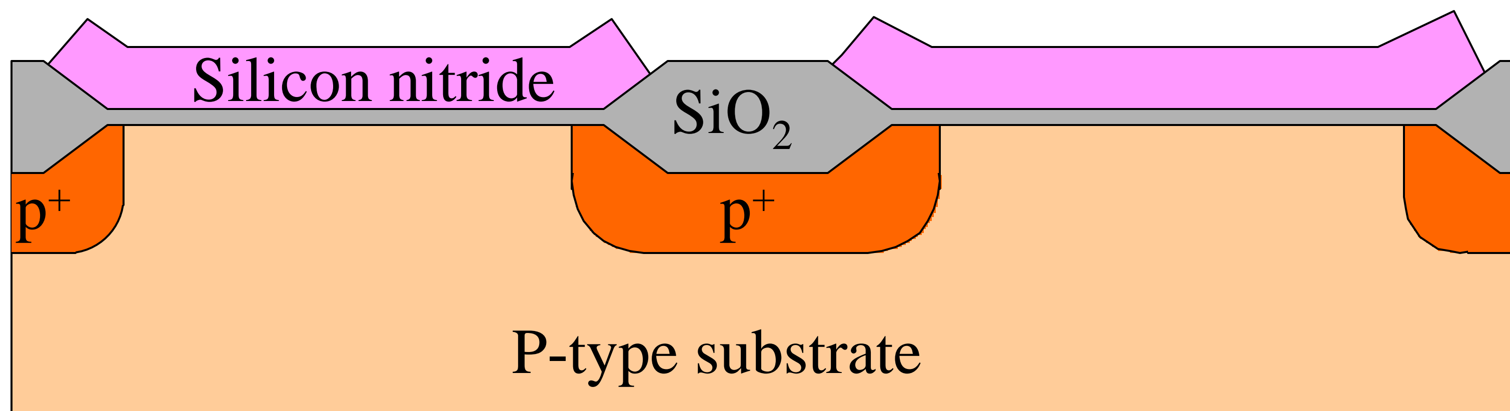
Strip Photoresist



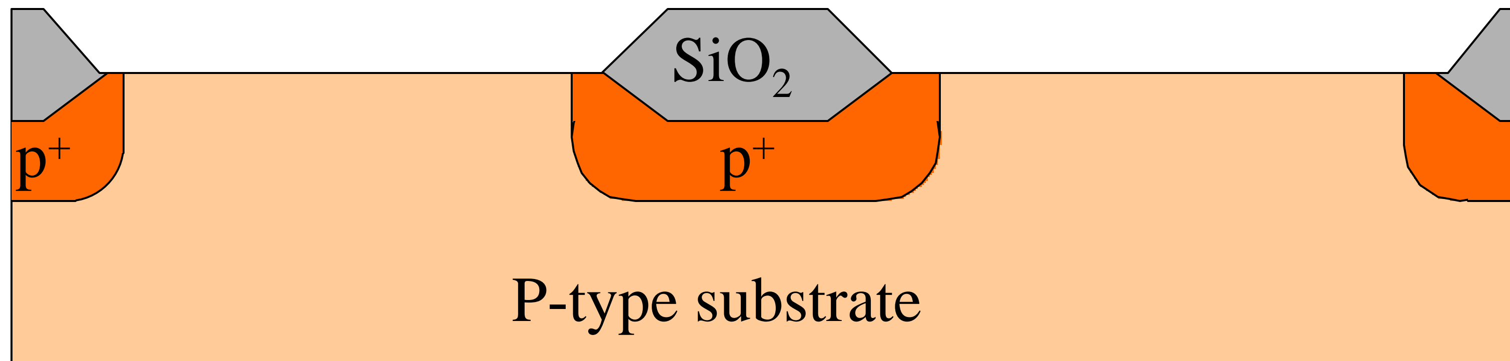
Isolation Implantation



Thermal Oxidation



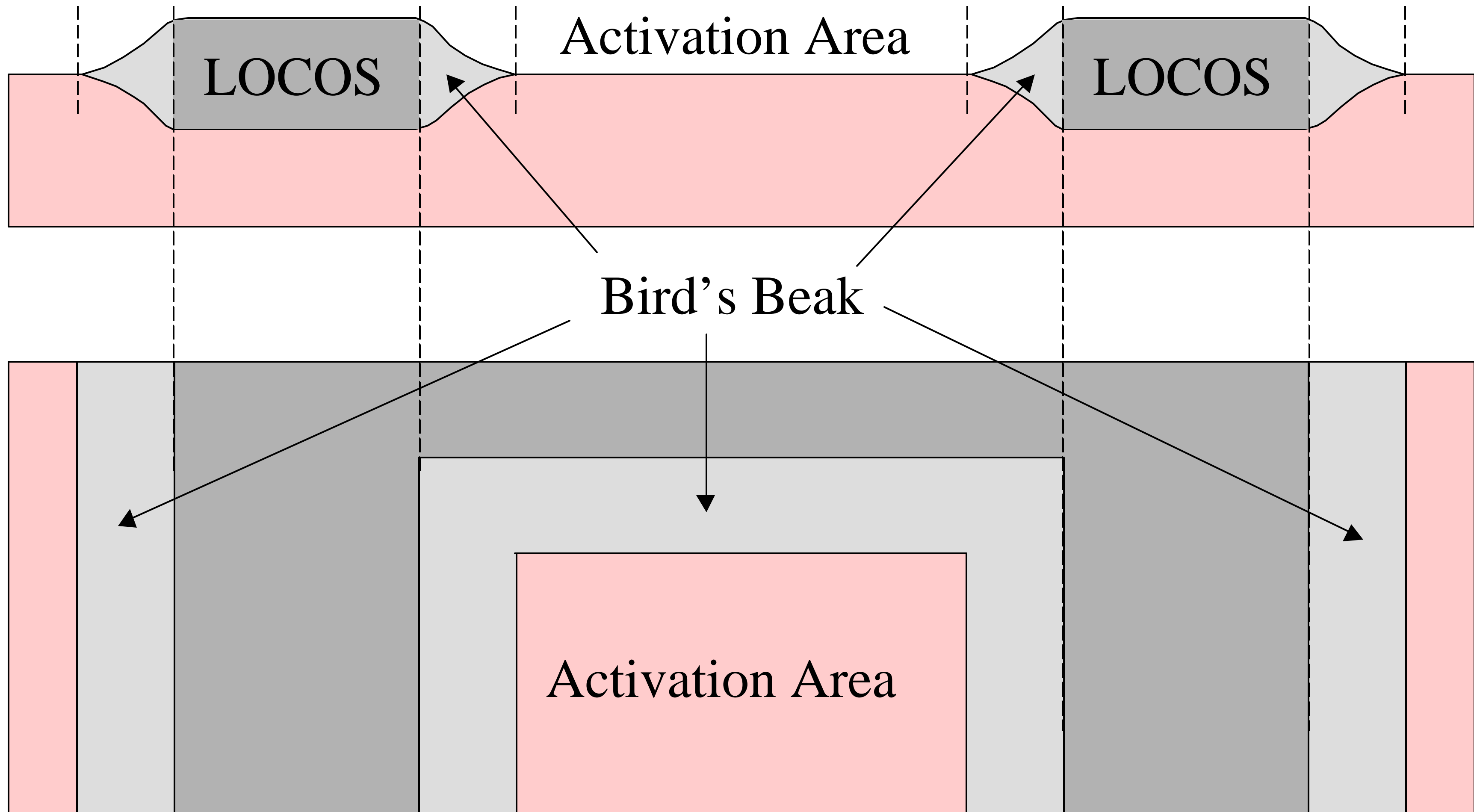
Strip Nitride



Problem of LOCOS

- Bird’s beak
  - Oxygen diffuse isotropically in silicon dioxide
  - Oxide grow underneath nitride
  - Waste surface area
- Uneven surface
  - Oxide grow above the silicon surface
  - Affect photolithography and thin film deposition

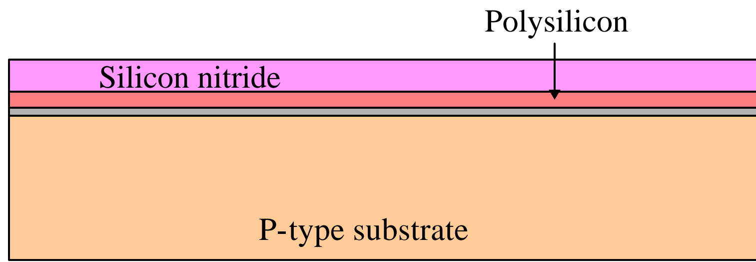
Bird’s Beak of LOCOS



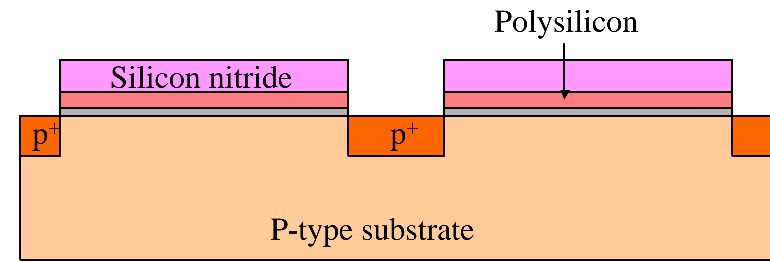
Poly Buffered LOCOS (PBL)

- Reducing “bird’s beak”
- Deposit polysilicon before LPCVD nitride
- Poly-Si consumes lateral diffusing oxygen
- Reduce “bird’s beak” to 0.1 to 0.2 μm.

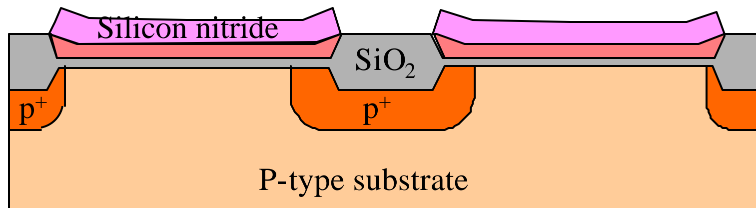
Poly Buffered LOCOS



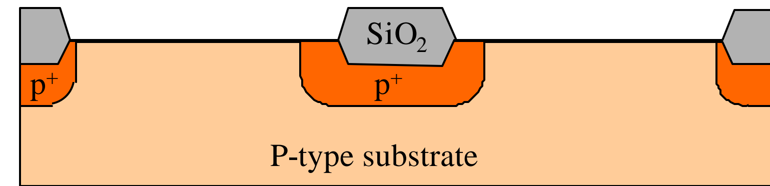
Pad oxidation, poly and nitride LPCVD



Nitride, poly, and oxide etch, B implantation



Oxidation



Strip pad oxidation, poly and nitride

Shallow Trench Isolation (STI)

- LOCOS and PBL work fine when feature size > 0.5 μm
- Intolerable when feature < 0.35 μm
- Silicon etch and oxidation of trench was researched to reduce oxide encroachment
- Process was then developed with CVD oxide trench fill

STI and LOCOS

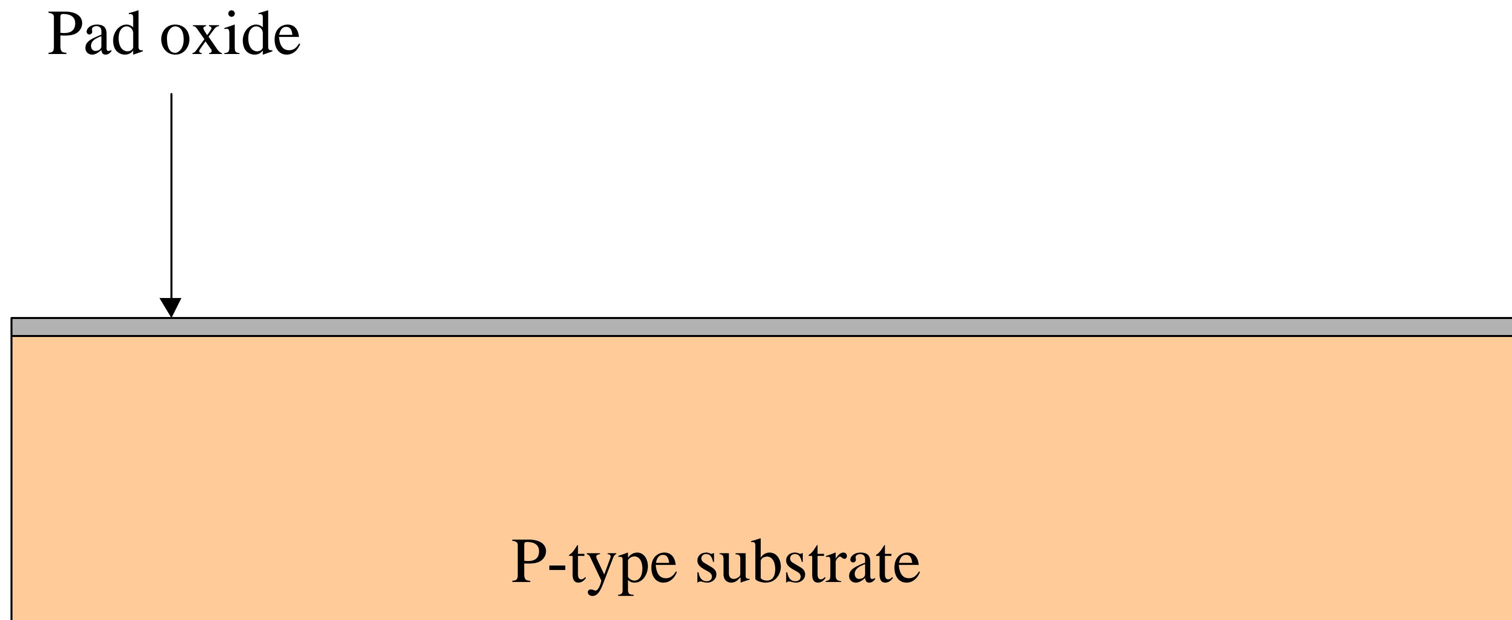
- STI
  - No bird's beak
  - Smoother surface
  - More process steps
- LOCOS
  - Simpler, cheaper, and production proven
  - Used in IC fabrication until feature < 0.35 μm

STI and LOCOS

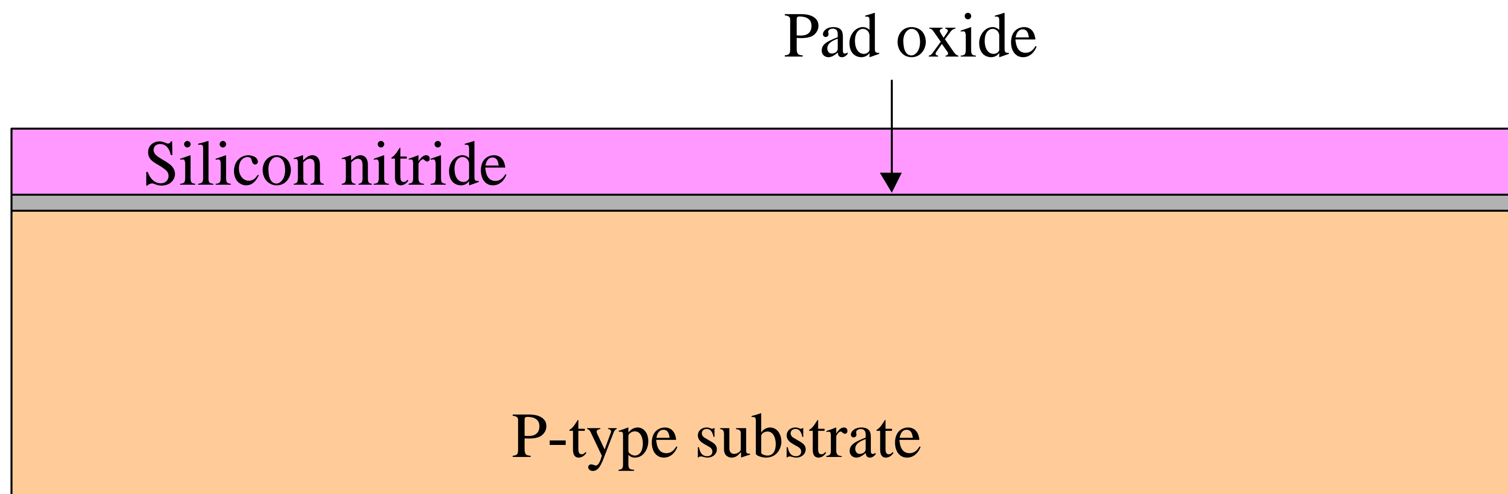
- Early STI process
  - Oxide etch back
  - CF_4/O_2 chemistry
  - Endpoint by C-N line
- Advanced STI process: oxide CMP
  - Better process control
  - Higher yield

Early STI: Wafer Clean

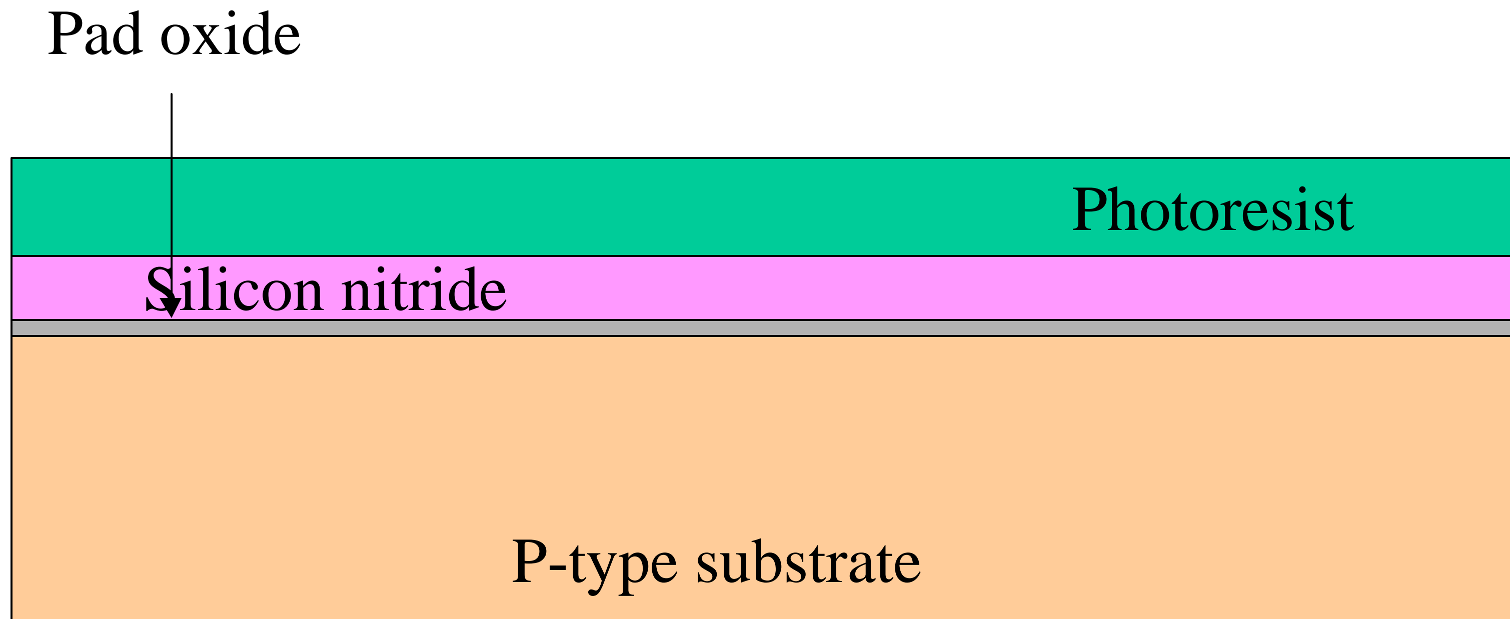
Early STI: Grow Pad Oxide



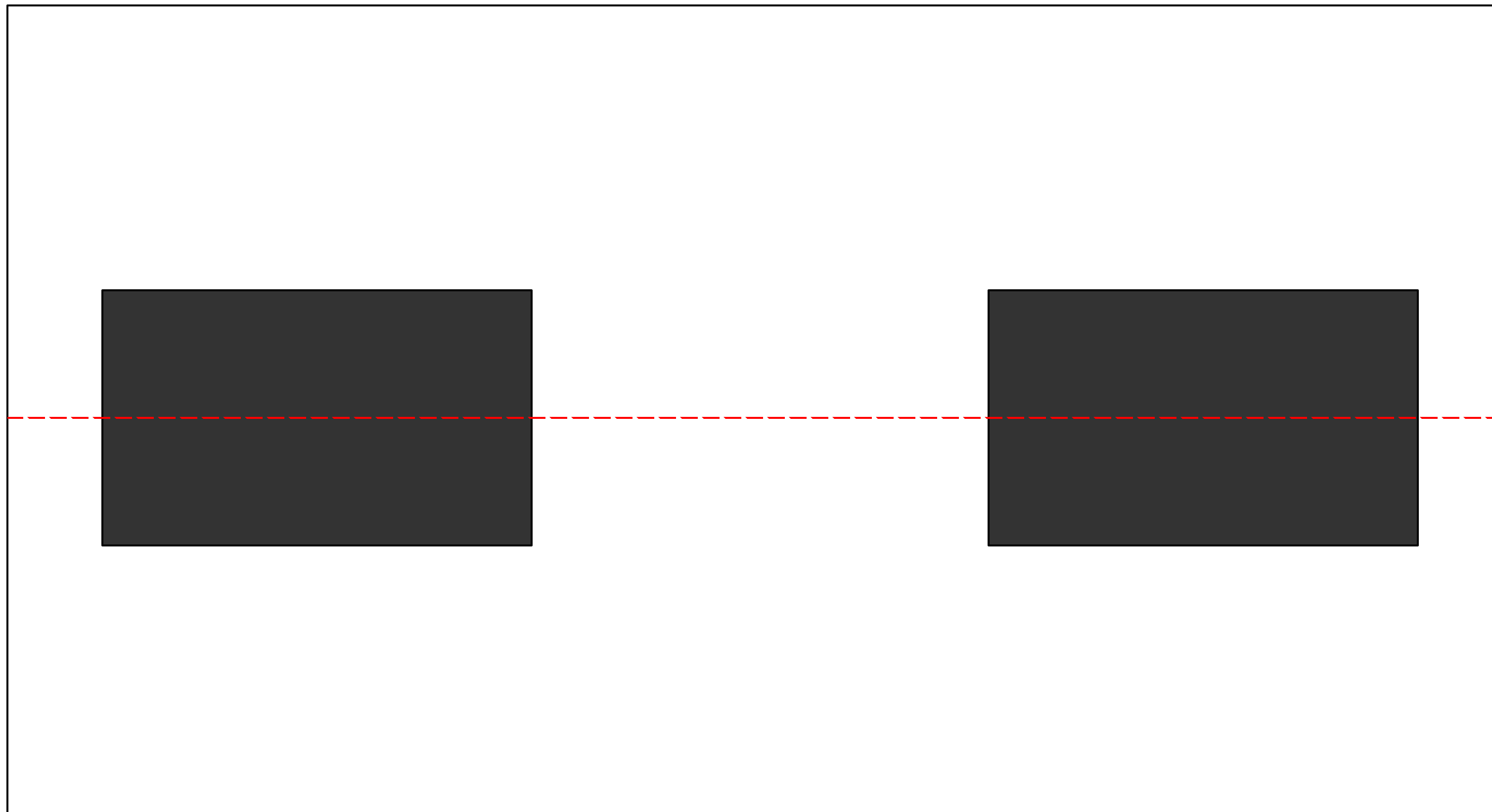
Early STI: LPCVD Silicon Nitride



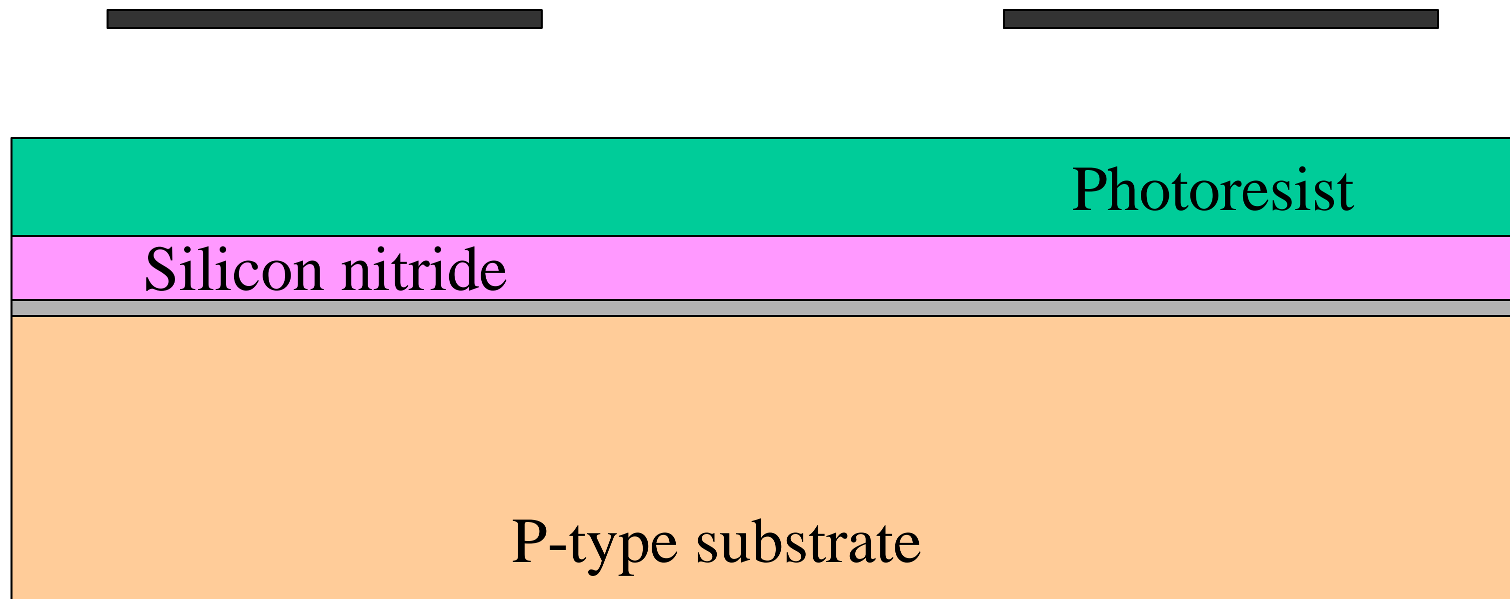
Early STI: Photoresist Coating



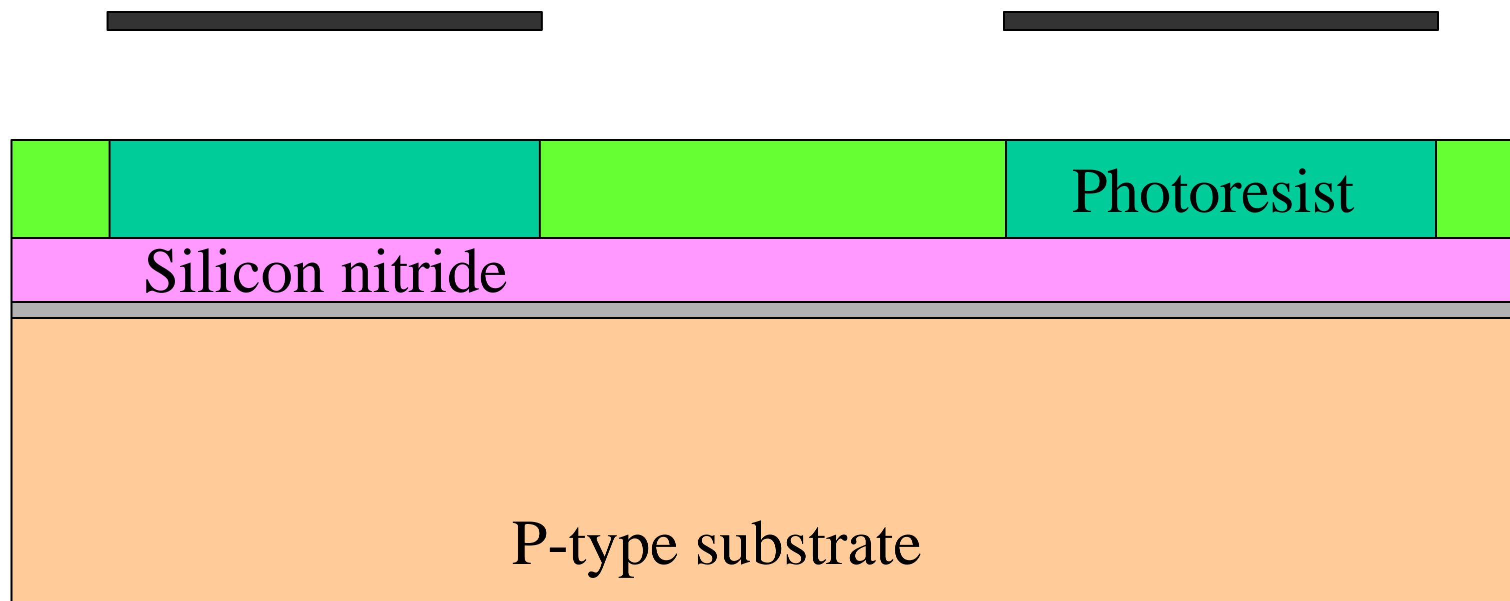
Early STI: STI Mask



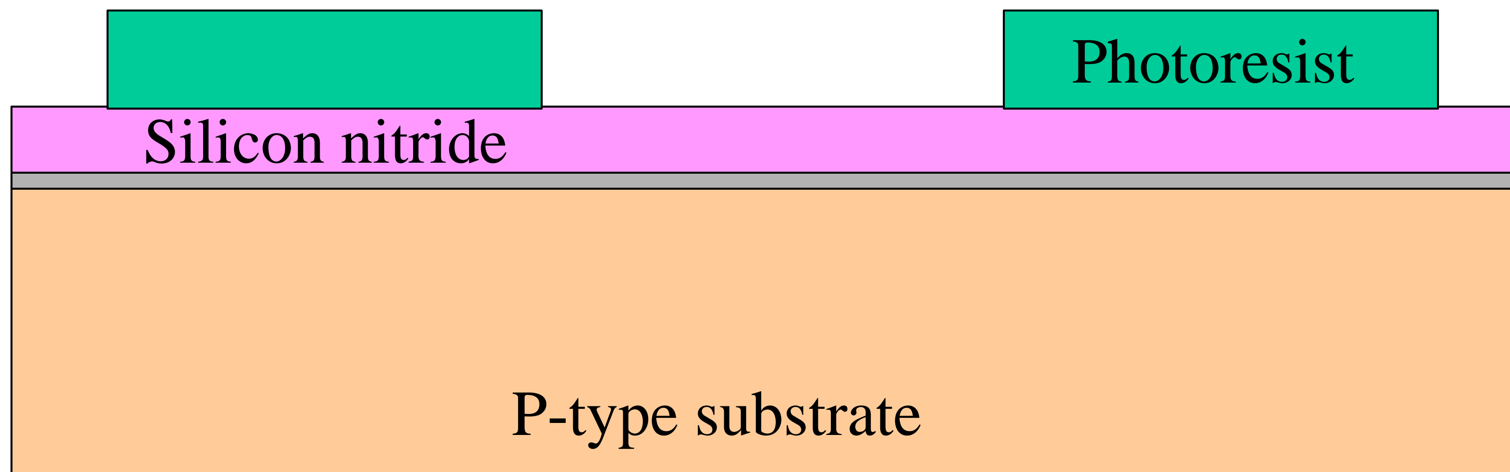
Early STI: STI Mask Alignment



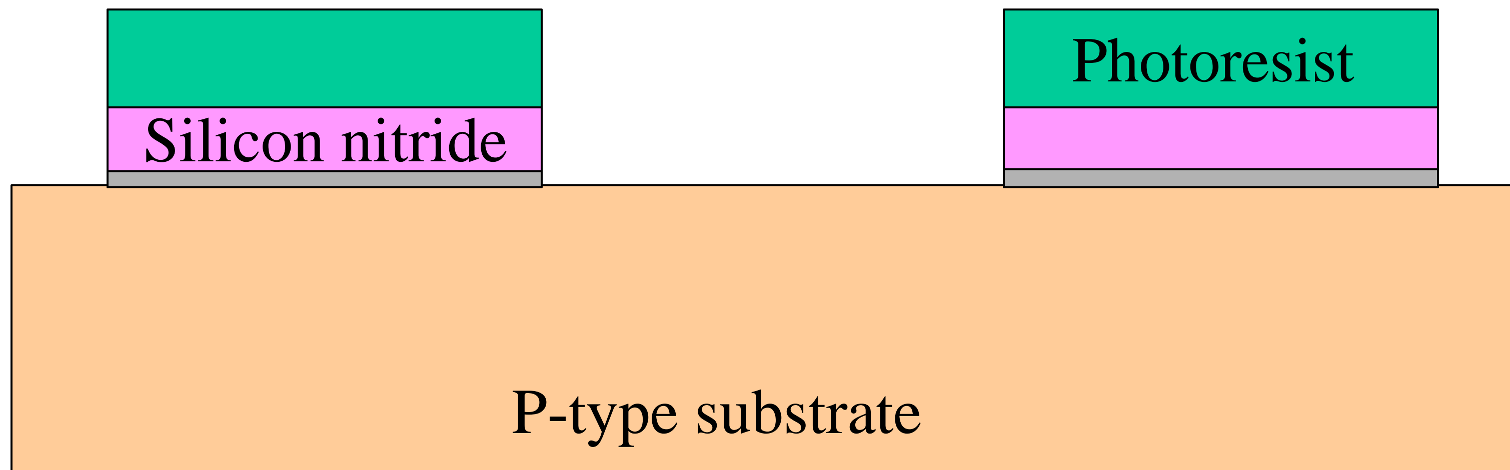
Early STI: STI Mask Exposure



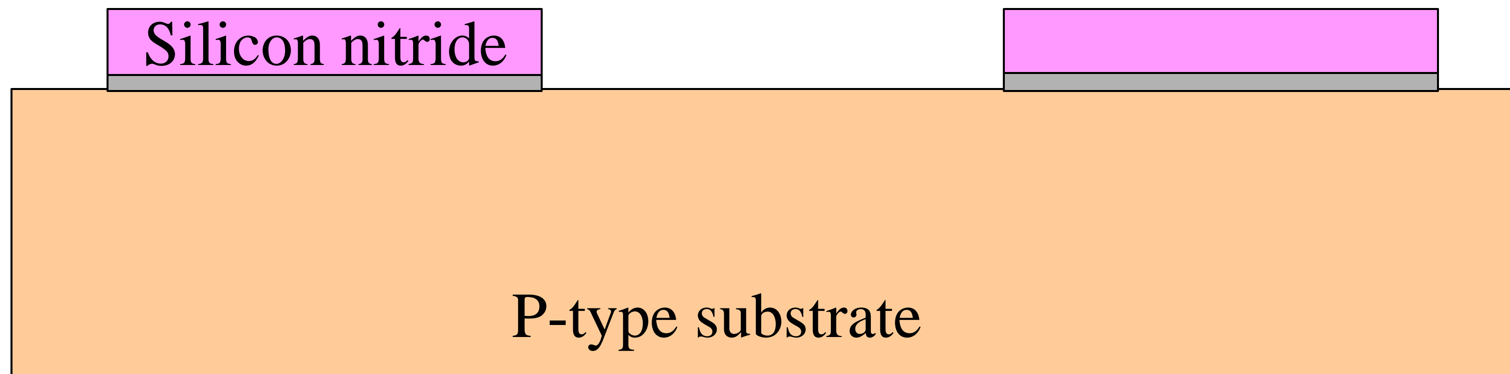
Early STI: Development



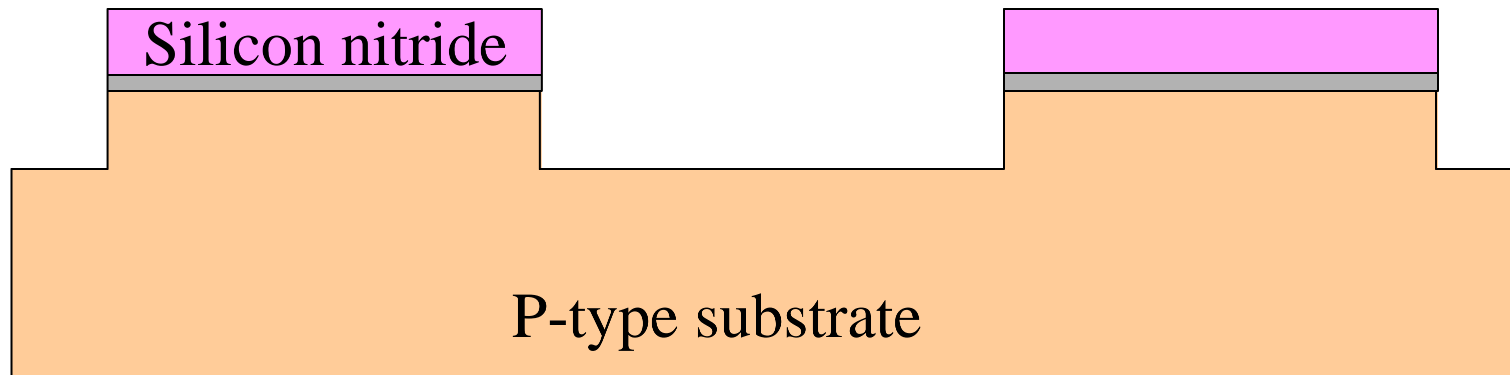
Early STI: Etch Nitride and Pad Oxide



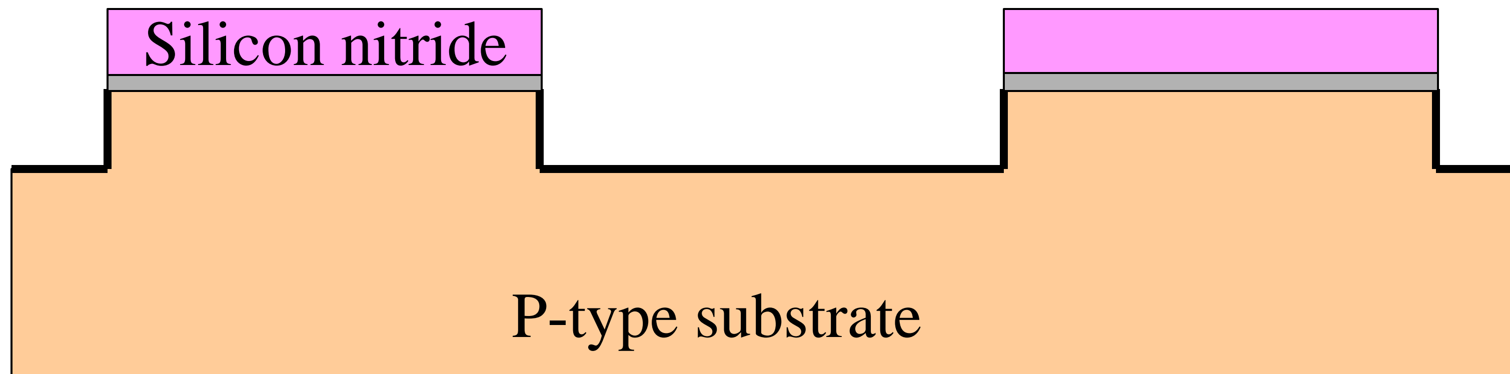
Early STI: Strip Photoresist



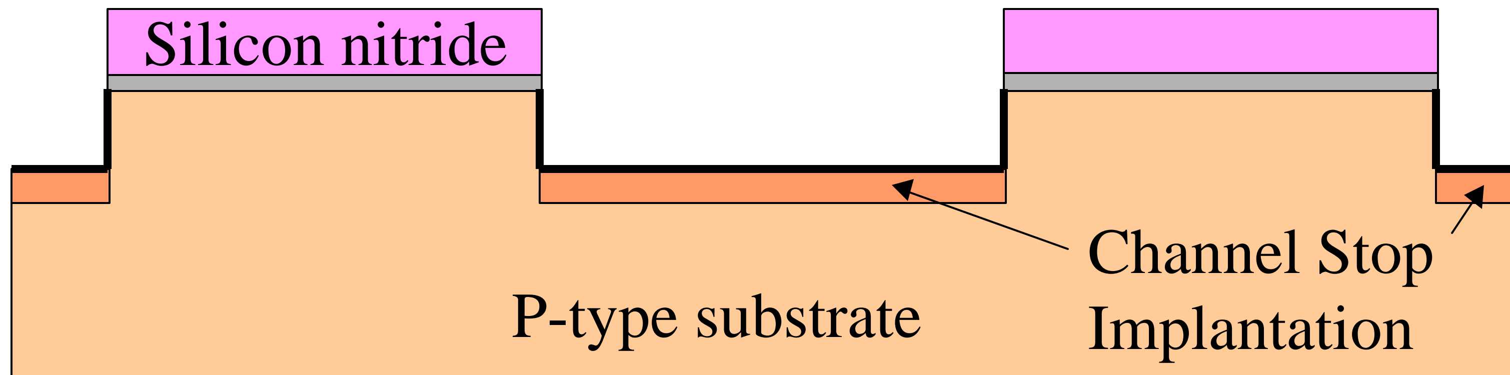
Early STI: Etch Silicon



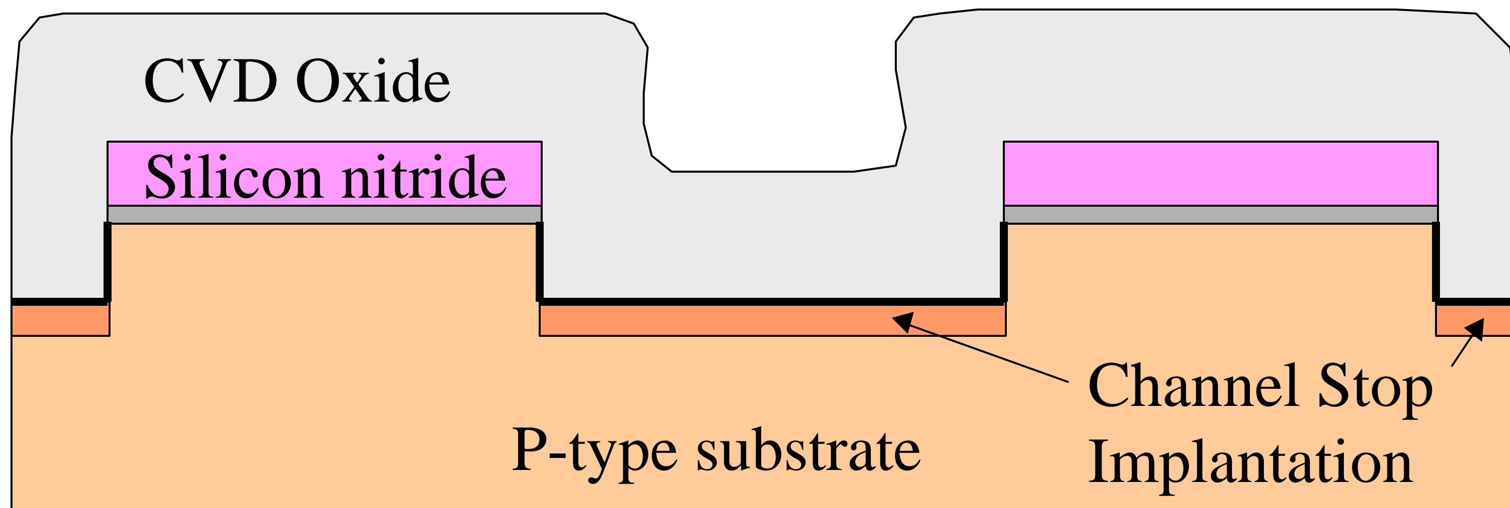
Early STI: Grow Barrier Oxide



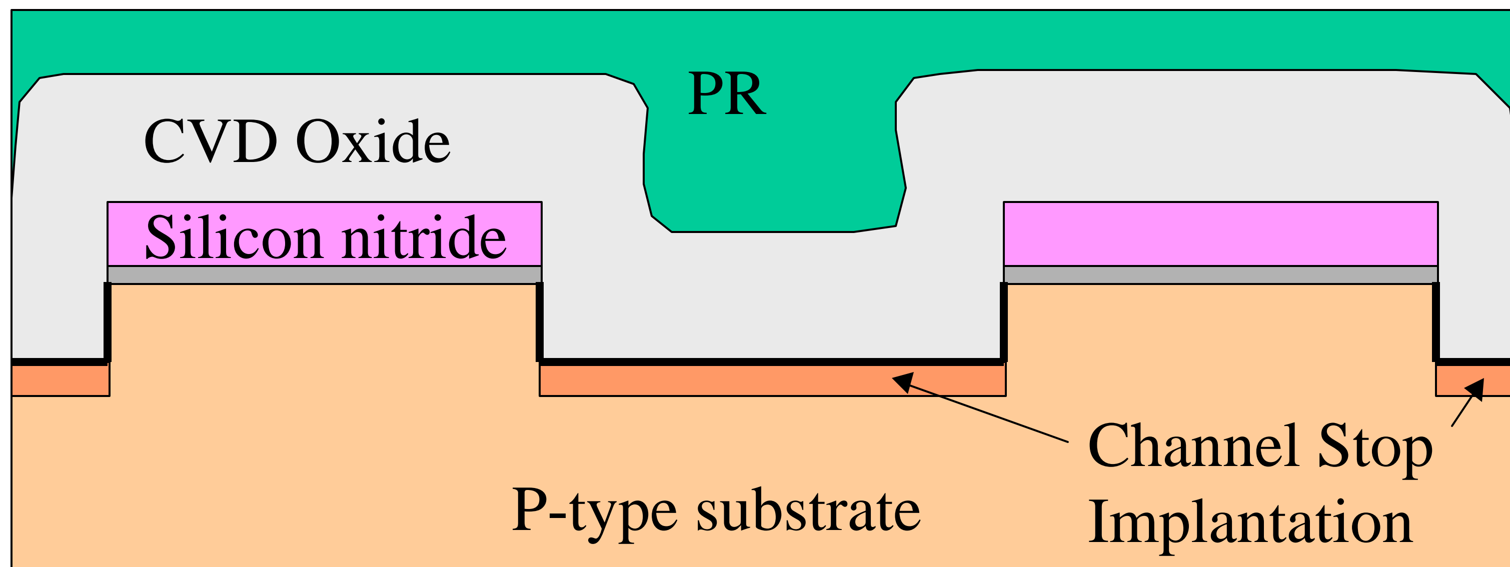
Early STI: Channel Stop Implantation, Boron



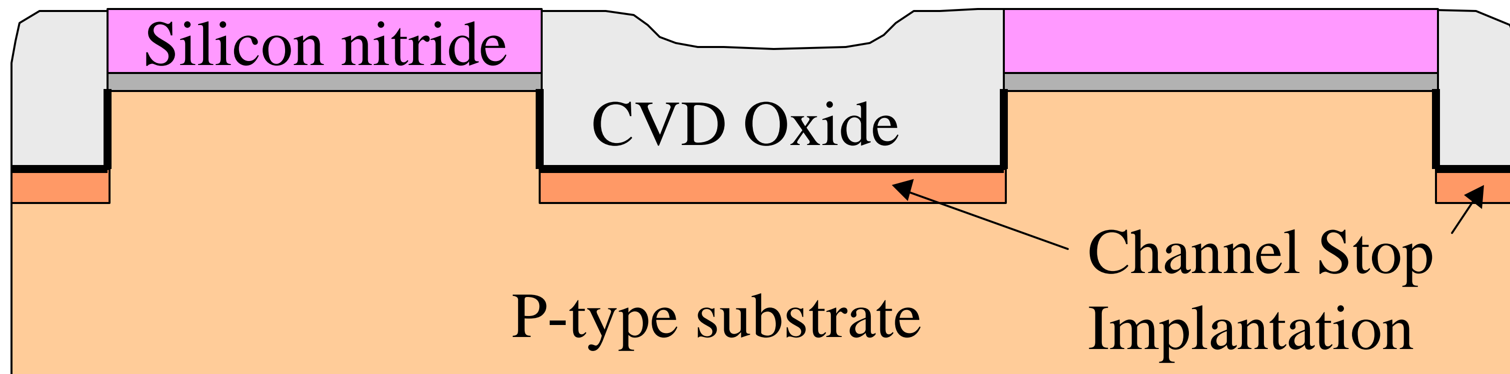
Early STI: CVD Oxide



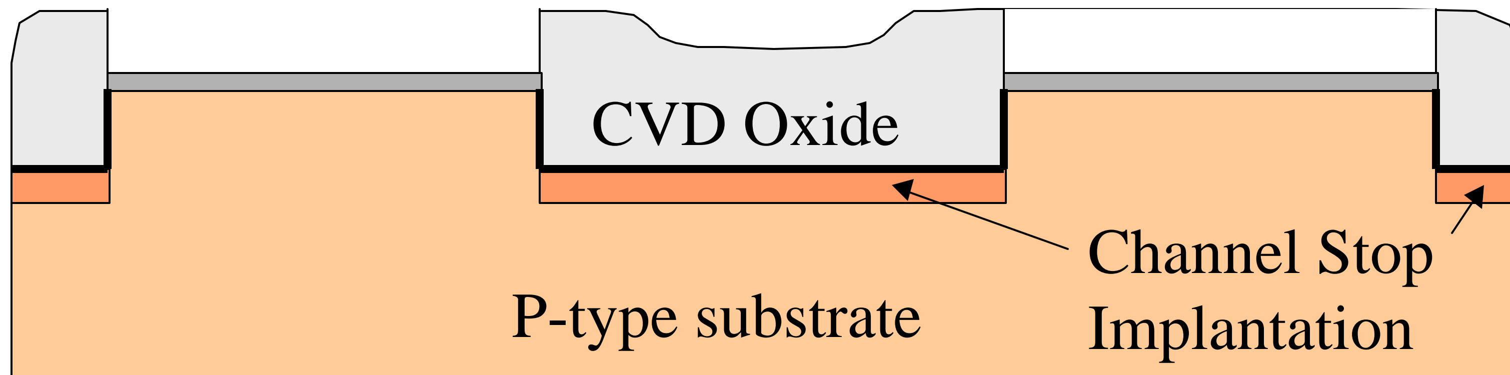
Early STI: Photoresist Coating



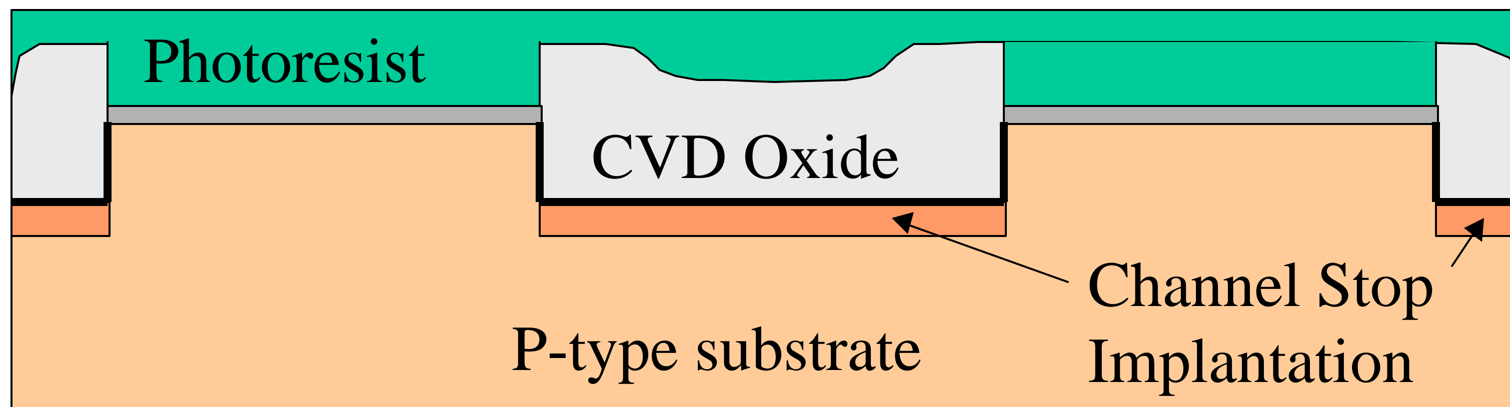
Early STI: Oxide Etch Back, Stop on Nitride



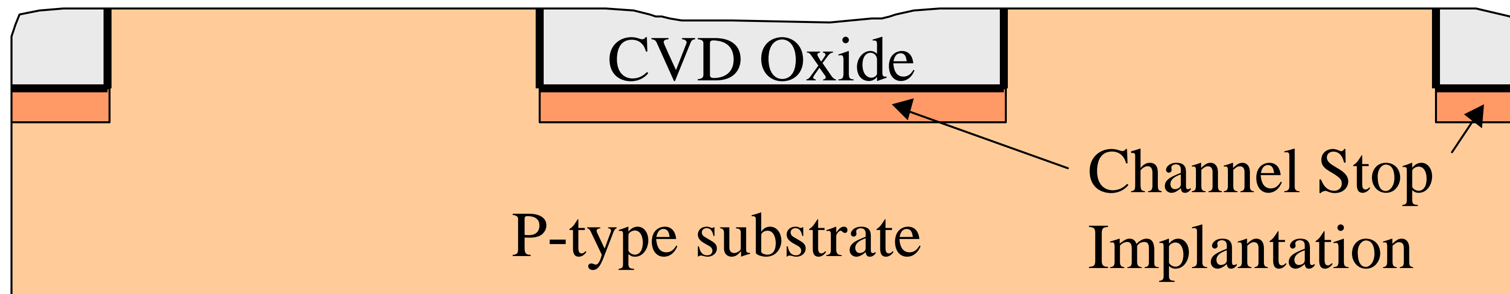
Early STI: Strip Nitride



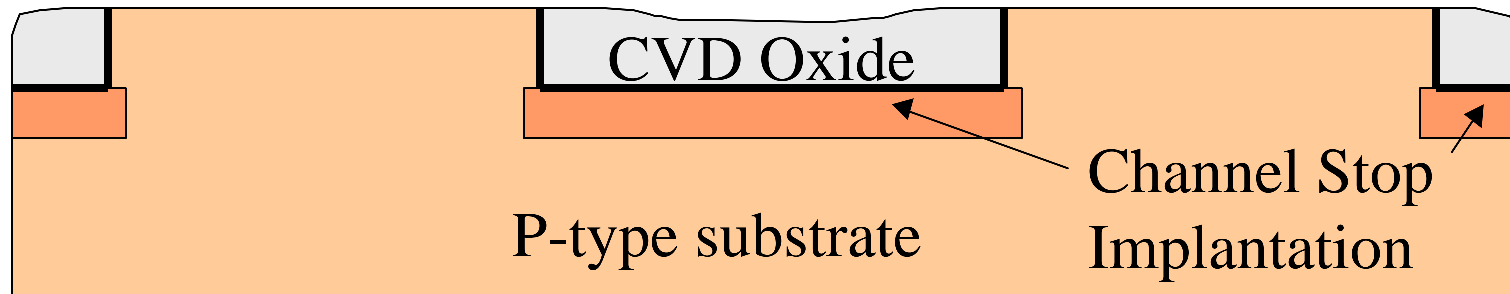
Early STI: Photoresist Coating



Early STI: Oxide Etch Back



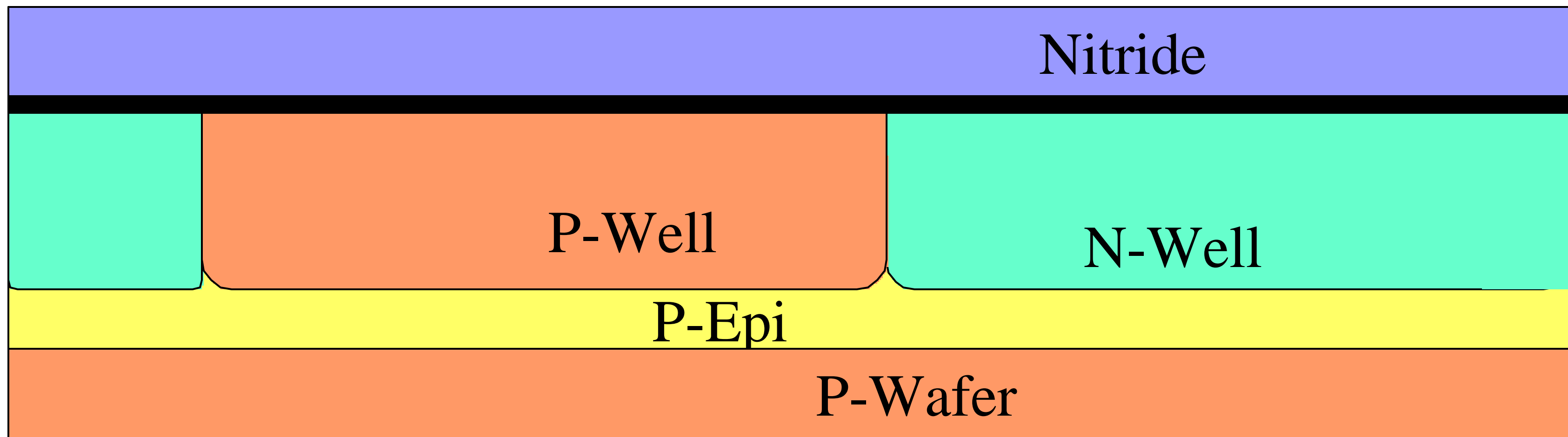
Early STI: Oxide Annealing



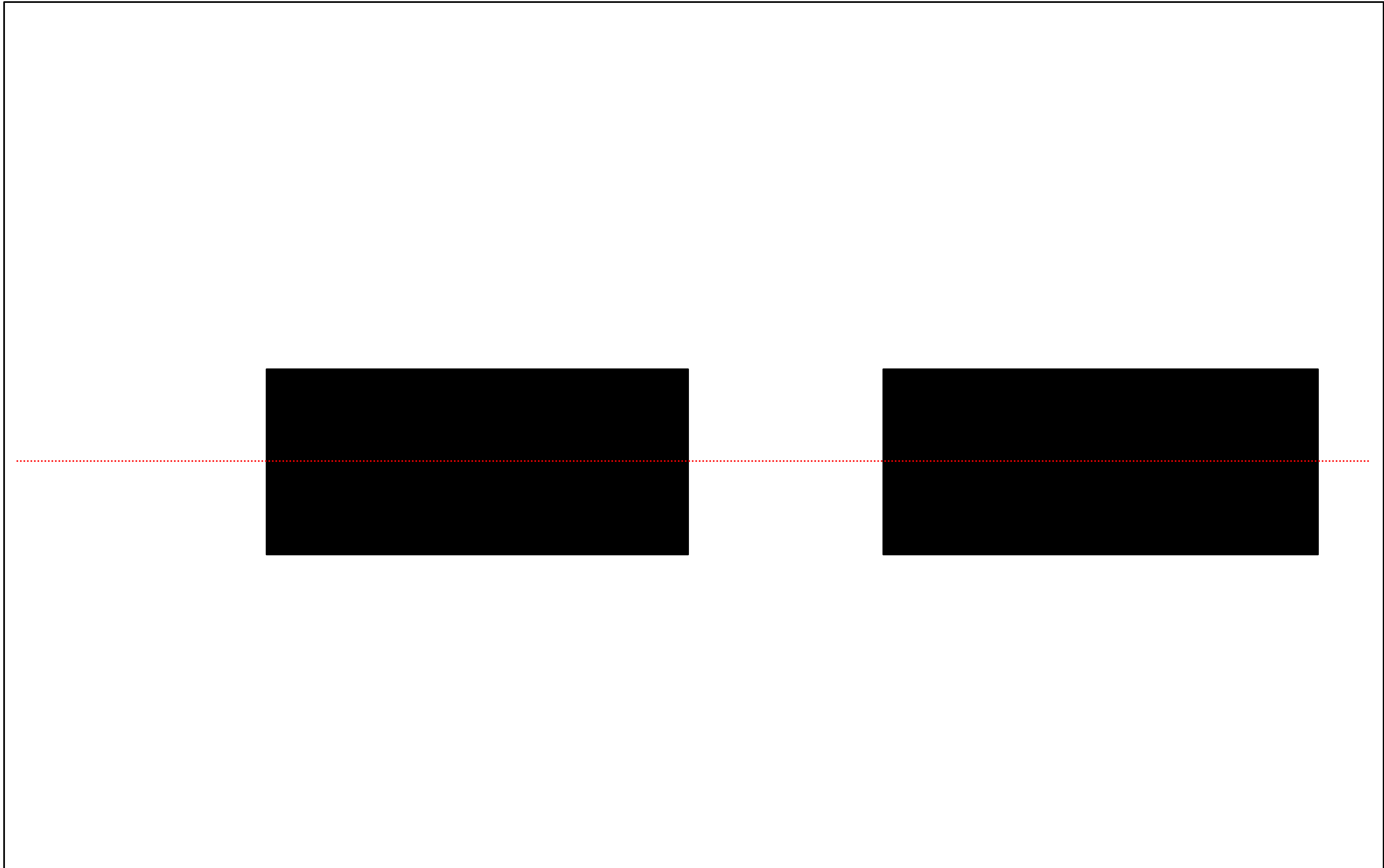
Advanced STI

- No need for channel stop ion implantation to raise the field threshold voltage.
- Trench fill can also be achieved with O_3-TEOS process
  - Need anneal at > 1000 °C to densify the film
- HDP oxide does not require thermal anneal

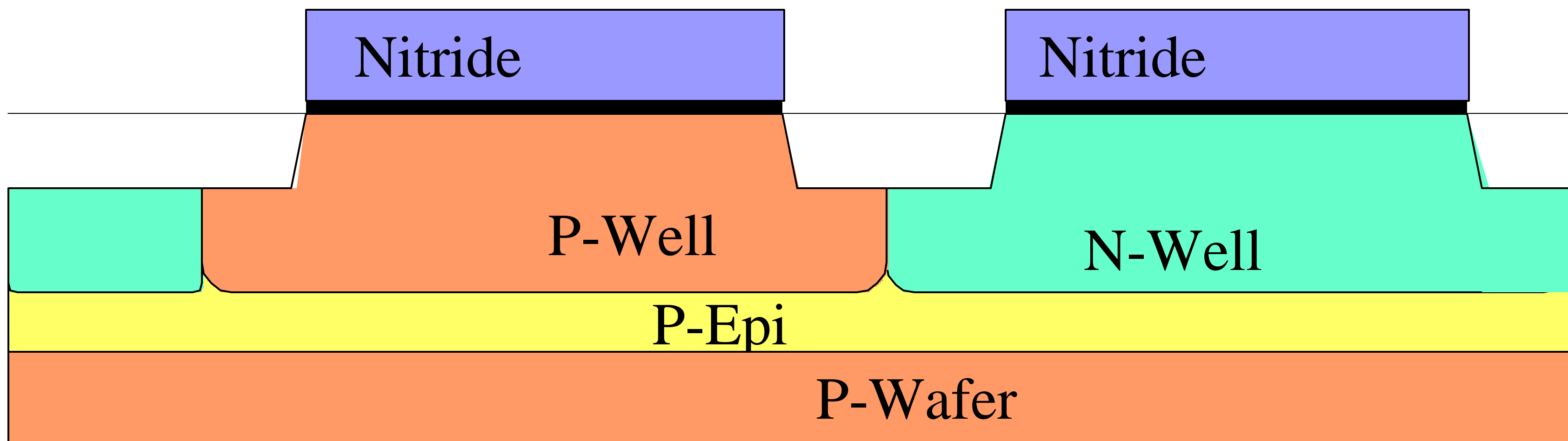
Advanced STI: Pad Oxidation and LPCVD Nitride



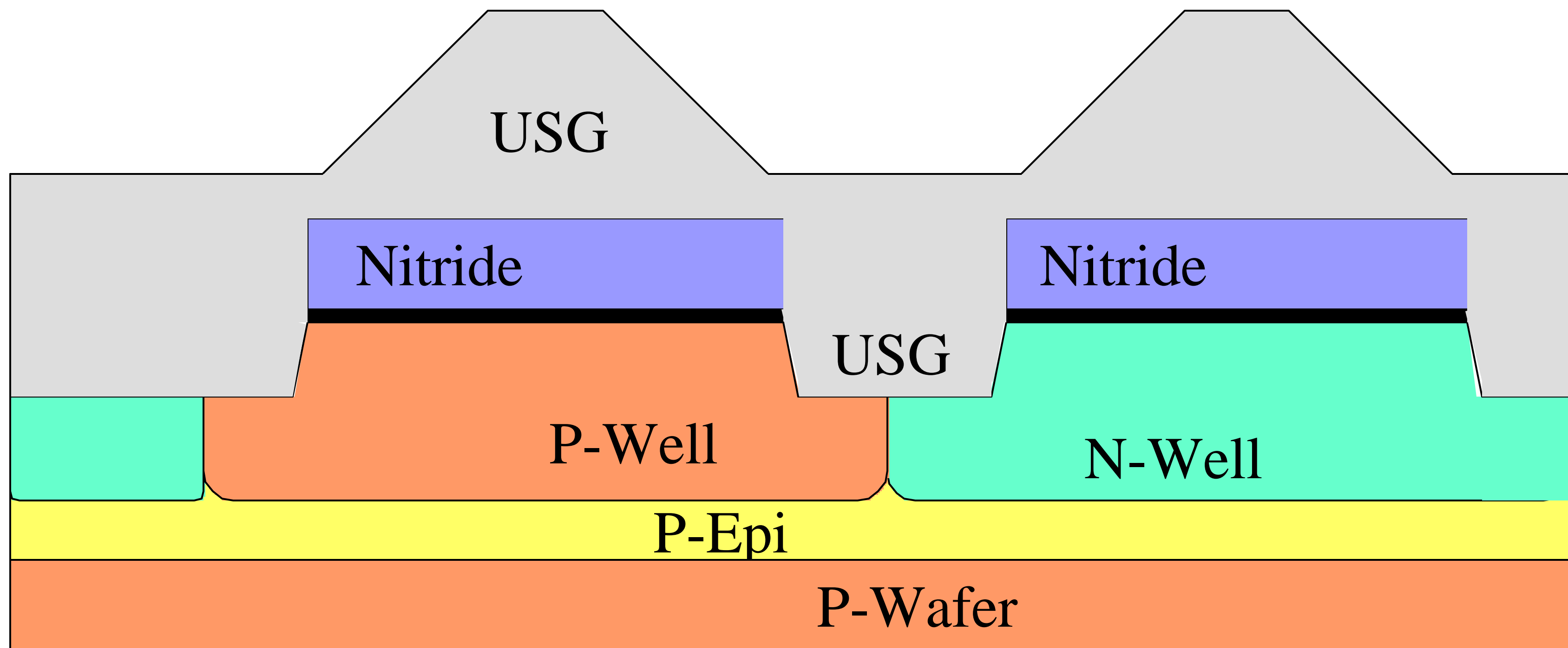
Advanced STI: STI Mask



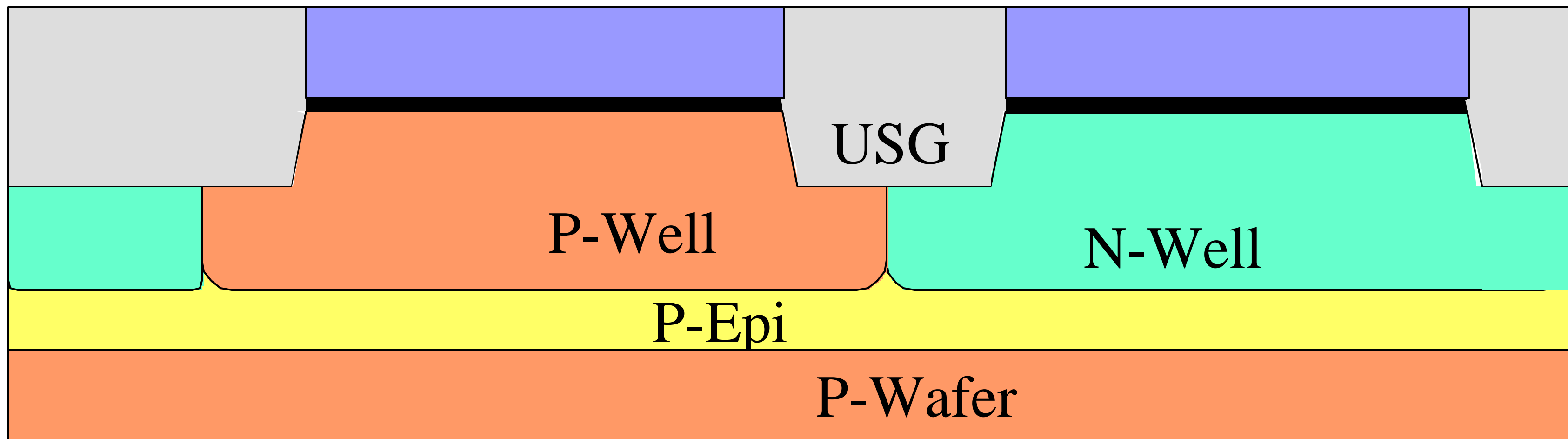
Advanced STI: Etch Nitride, Oxide, and Silicon, Strip Photoresist



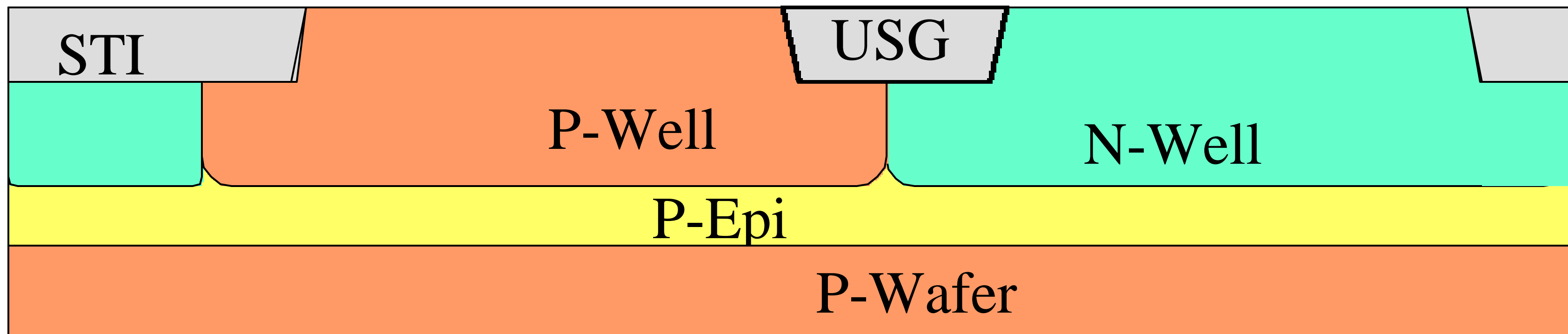
Advanced STI: HDP CVD Oxide



Advanced STI: CMP Oxide, Stop on Nitride



Advanced STI: Nitride Strip



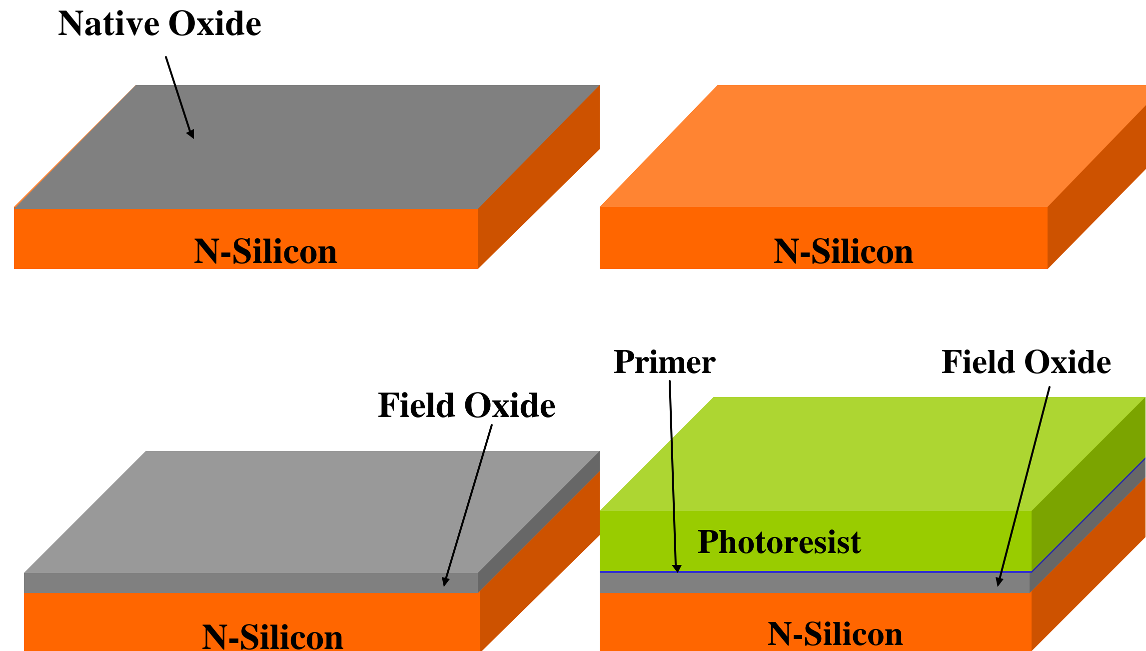
Transistor Making

- Metal gate
- Self-aligned gate
- Lightly doped drain (LDD)
- Threshold adjustment
- Anti punch-through
- Metal and high-κ gate MOS

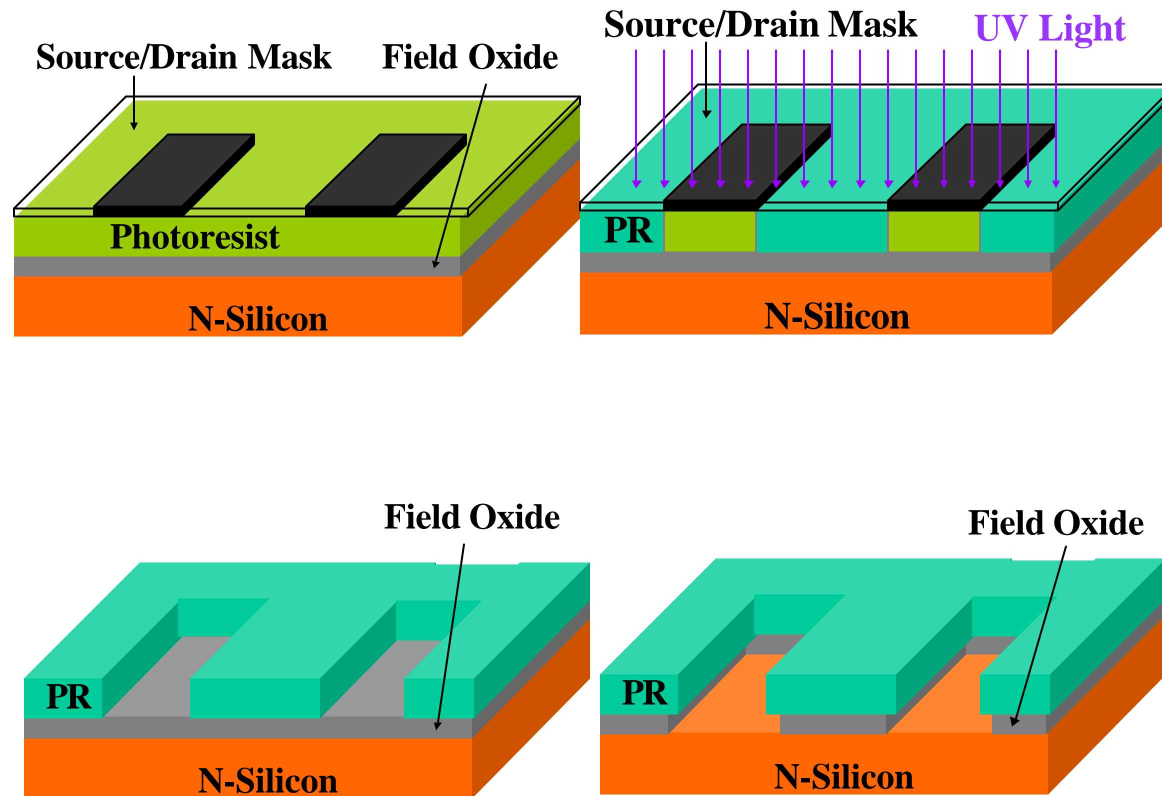
Transistor Making: Metal Gate

- Form source/drain first
  - Diffusion doping with silicon dioxide mask
- Align gates with source/drain, then gate area was etched and gate oxide is grown
- The third mask define the contact holes
- The fourth mask form metal gates and interconnections.
- Last mask defined the bonding pad

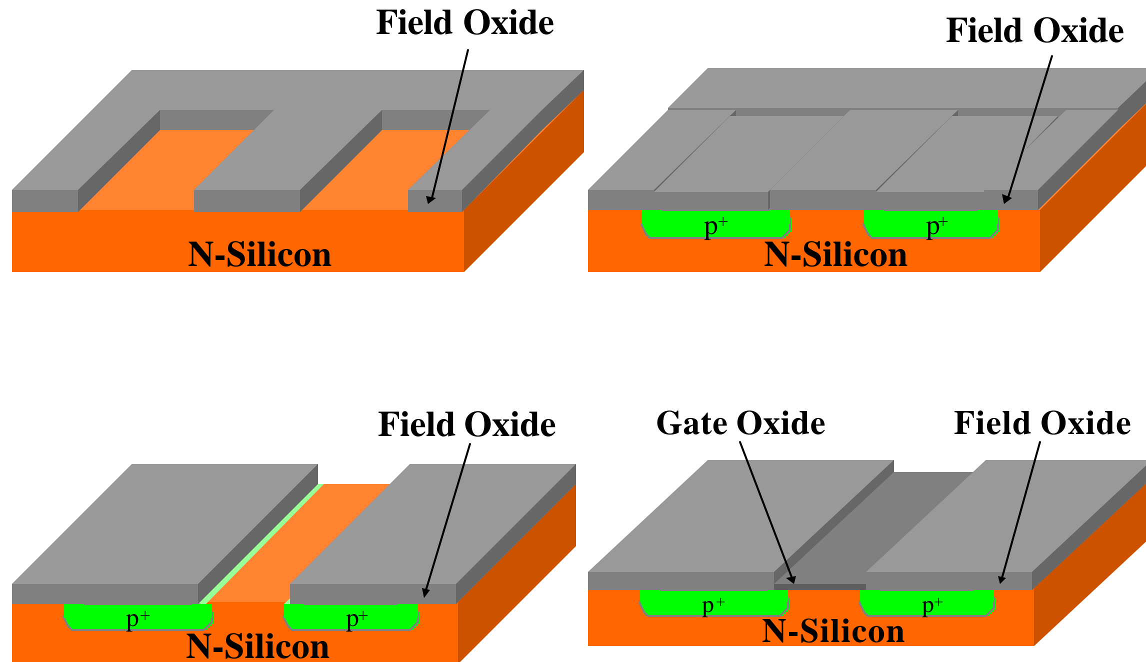
Wafer Clean, Field Oxidation, and Photoresist Coating



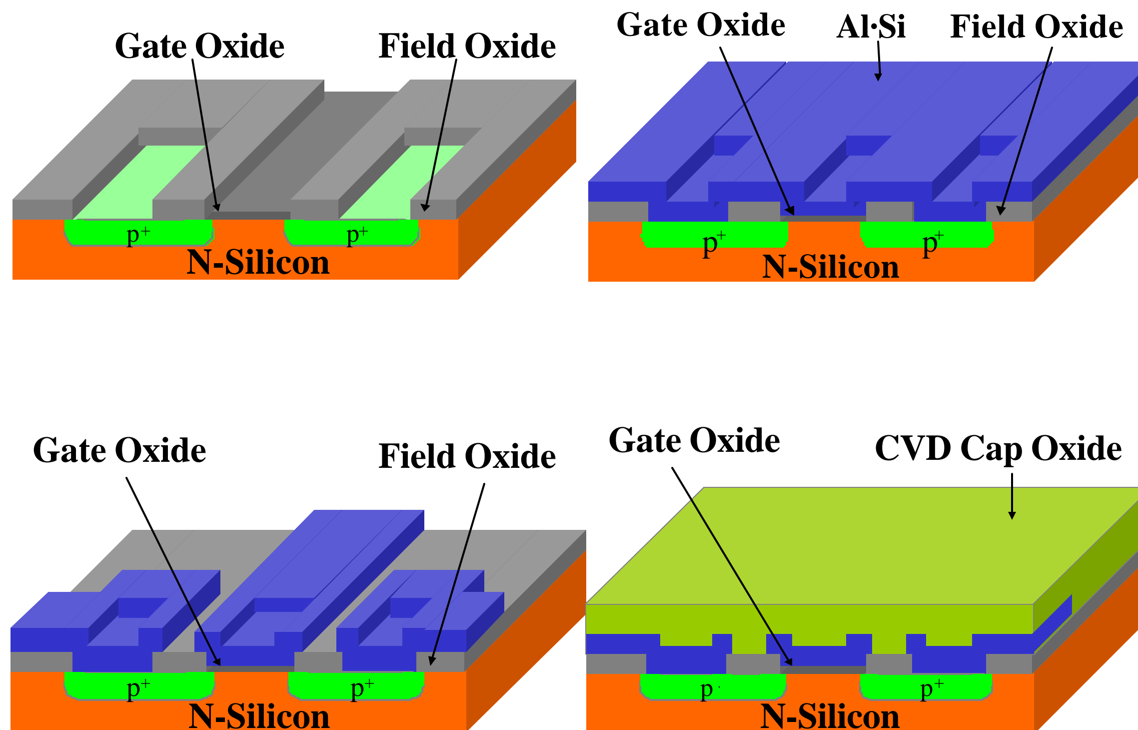
Photolithography and Oxide Etch



Source/drain Doping and Gate Oxidation



Contact, Metallization, and Passivation



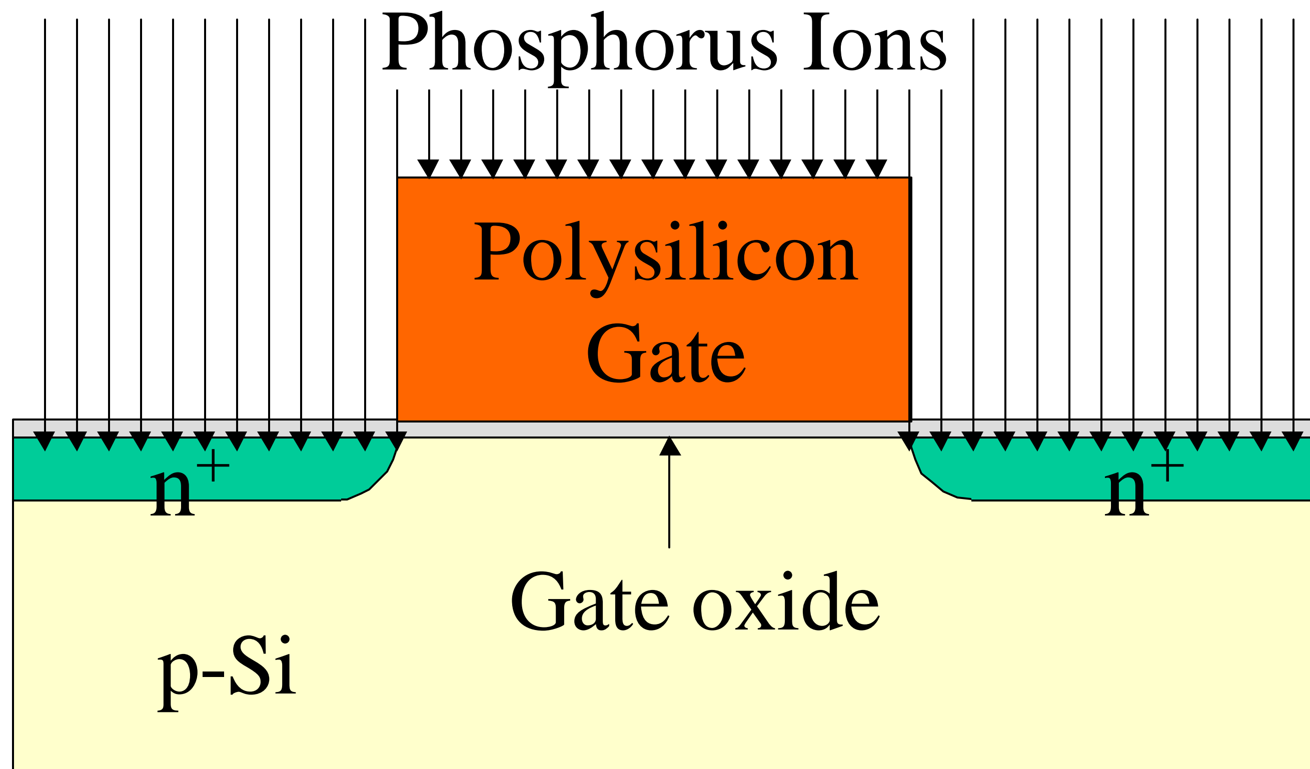
Self-aligned Gate

- Introduction of ion implantation
- NMOS instead of PMOS
- Polysilicon replaced aluminum for gate
  - Al alloy can’t sustain the high temperature post-implantation anneal

Self-aligned Gate

- Activation area for transistors making
- Gate oxidation and polysilicon deposition
- Gate mask defines the gate and local interconnection.
- Transistors are made after ion implantation and thermal annealing
- Advanced MOSFET are made in this way

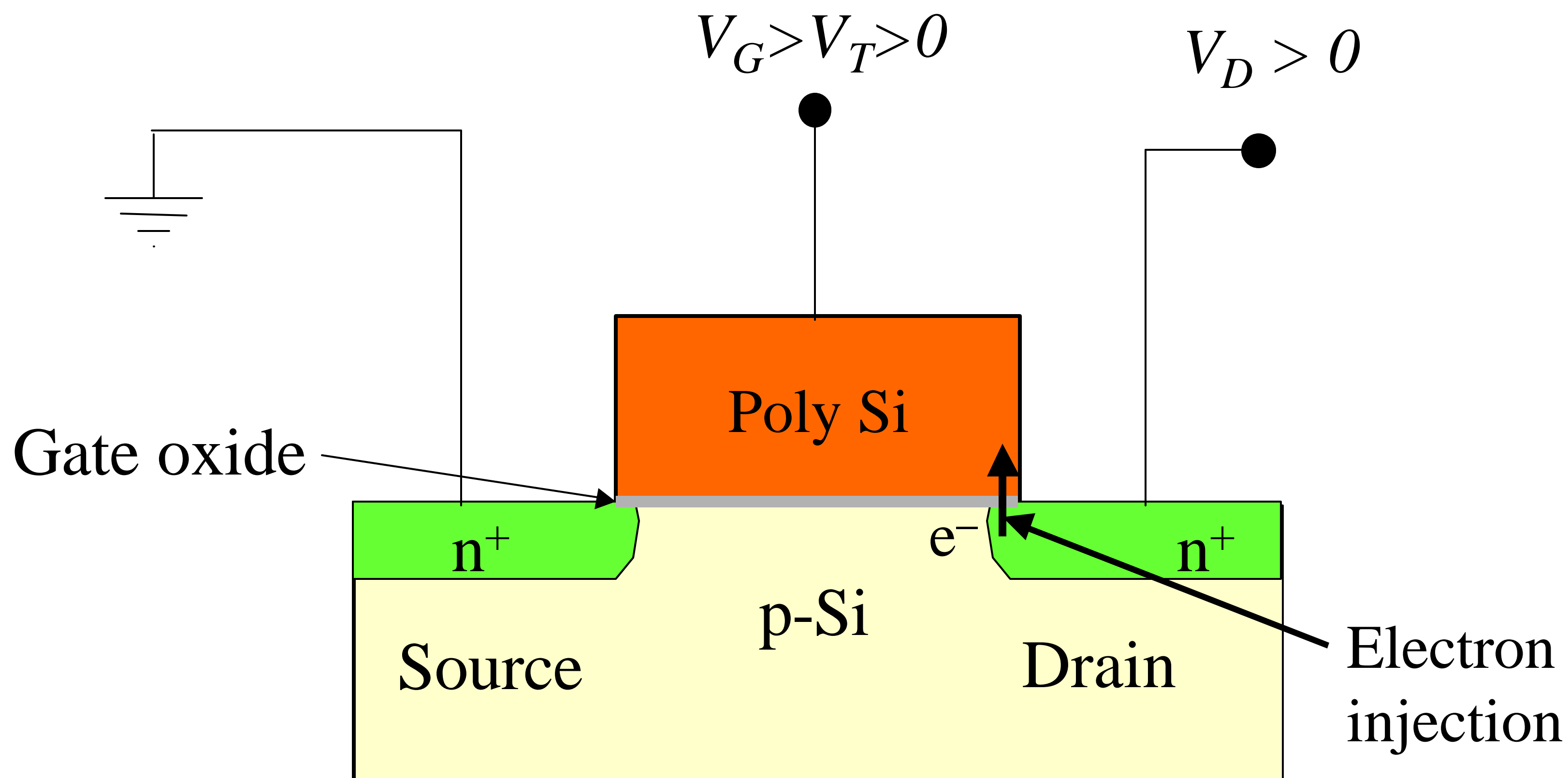
Transistor Making: Self-aligned Gate



Hot Electron Effect

- Gate width is < 2 microns,
- Vertical electric field accelerates electrons tunneling through the thin gate oxide layer
- Hot electron effect
  - gate leakage affect transistor performance
  - trapping of electrons in the gate oxide cause reliability problems for the IC chips
- LDD is used to prevent hot electron effect

Hot Electron Effect



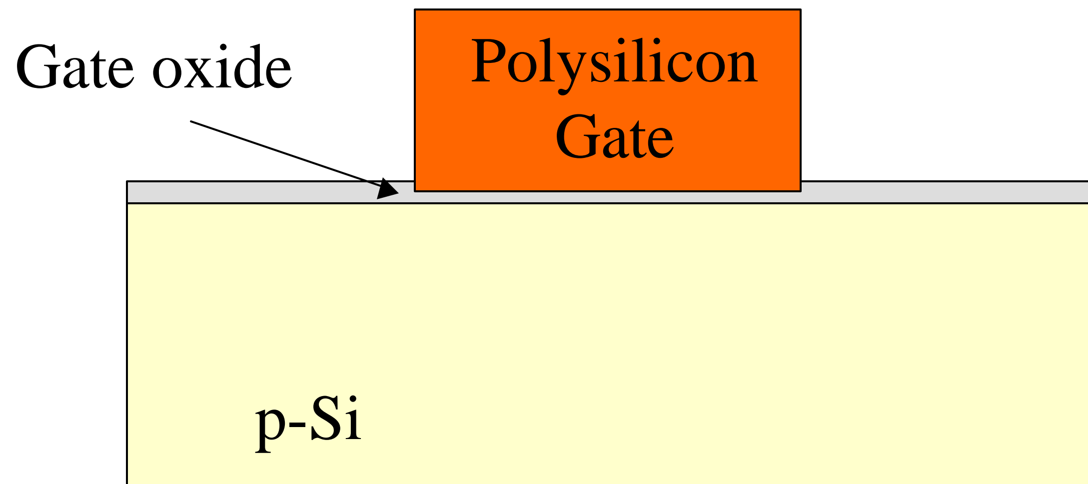
LDD Formation

- Low energy, low current ion implantation
  - very low dopant concentration and shallow junction just extended underneath the gate
- Sidewall spacers can be formed by depositing and etching back dielectric layers
- High current, low energy ion implantation forms the heavily doped source/drain
  - Source/drain are kept apart from the gate

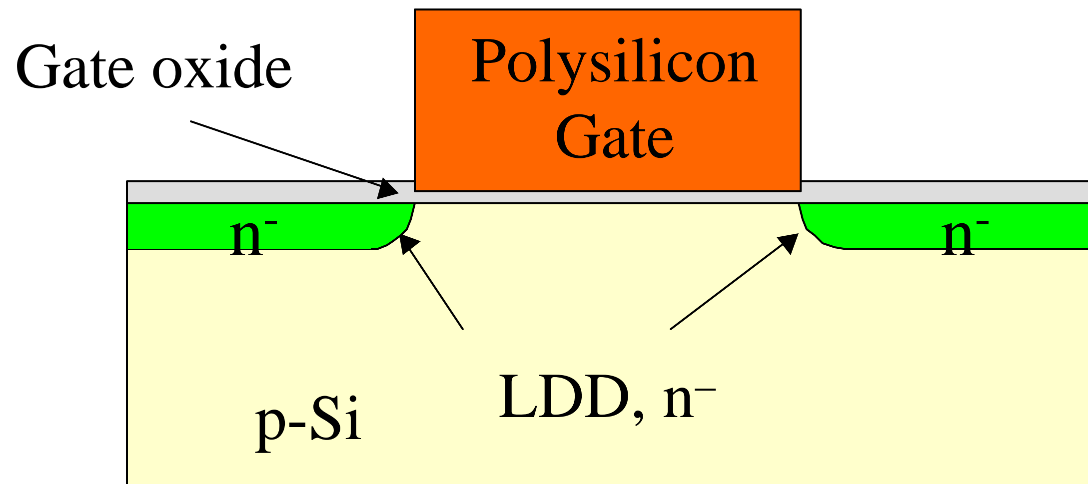
LDD Formation

- Reduce the vertical electric field of the source/drain bias
- Reduce the available electrons for tunneling
- Suppress the hot electron effect

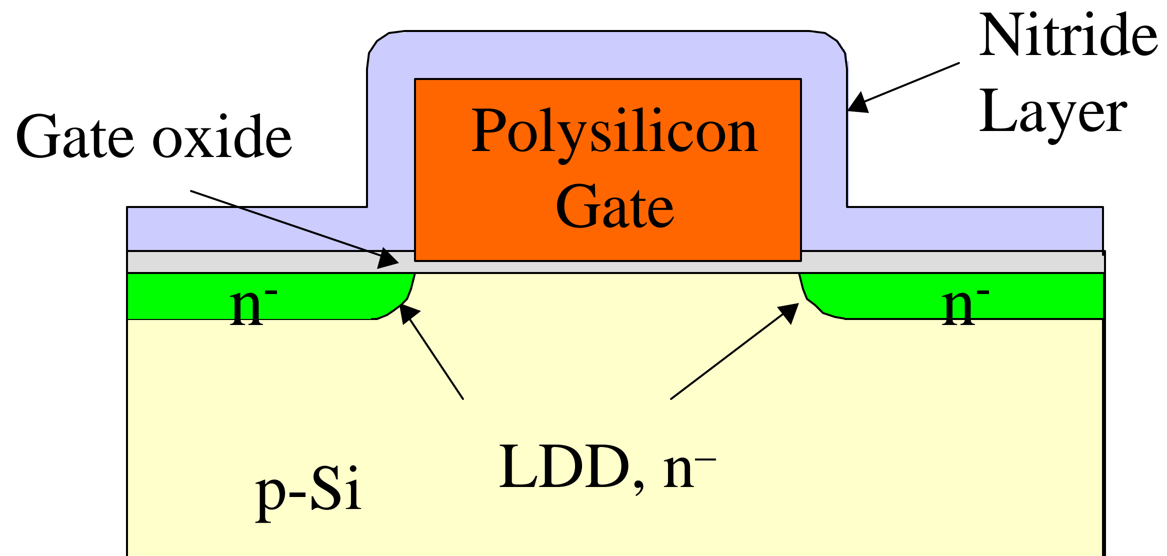
Poly Etch, PR Strip and Poly Anneal



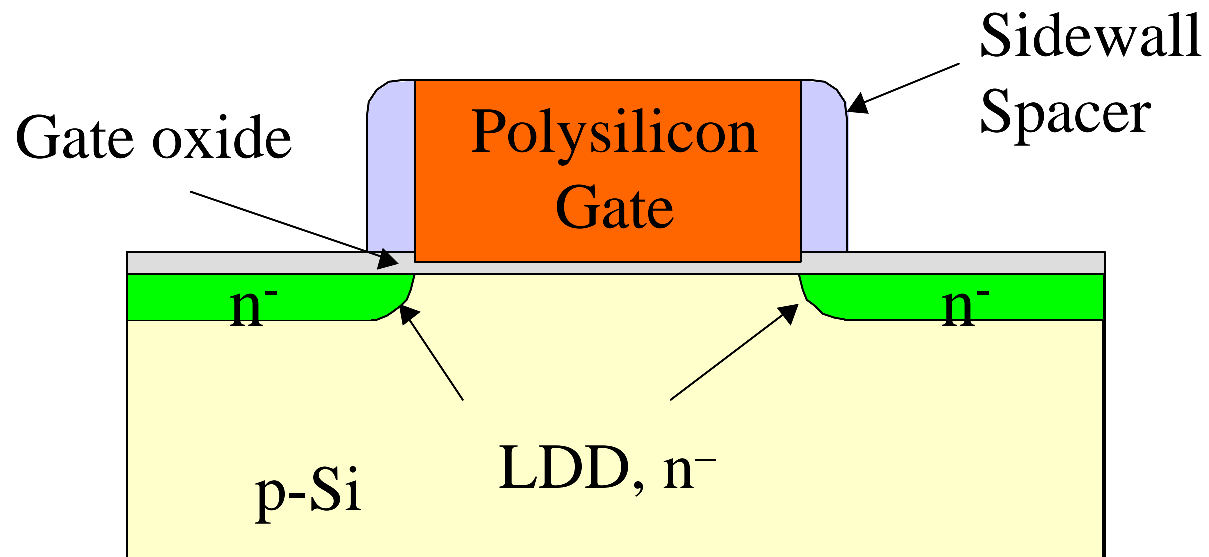
LDD implantation



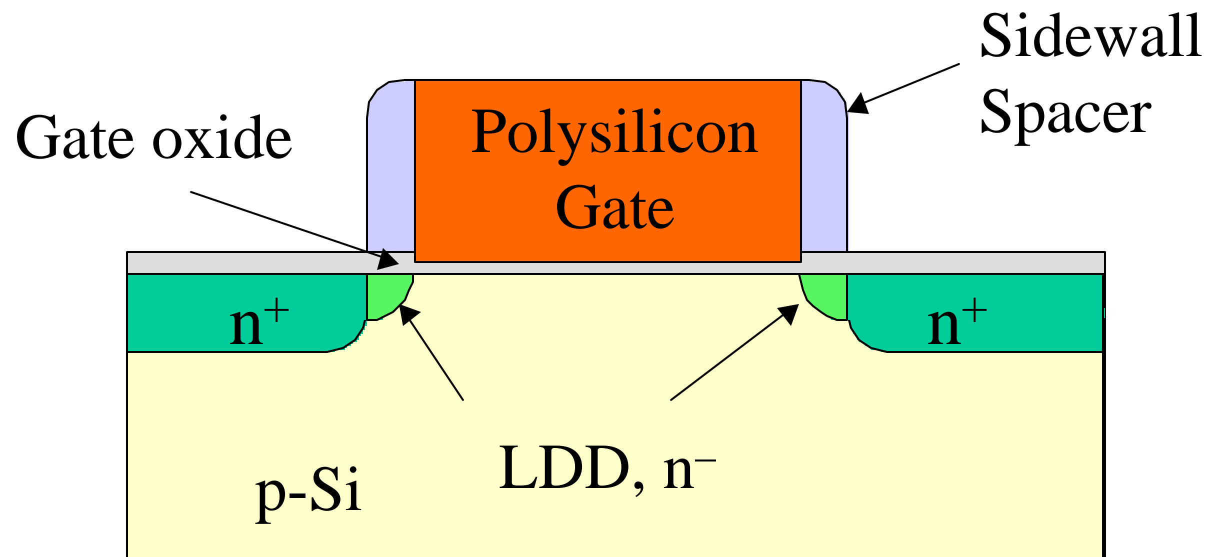
Nitride Deposition



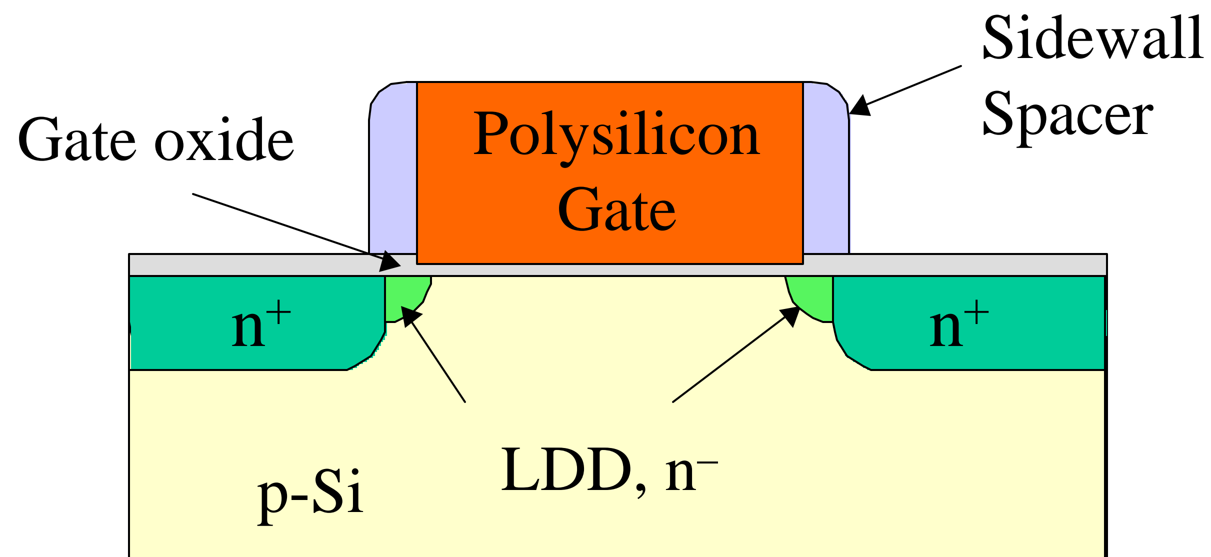
Nitride Etch Back



Source Drain Implantation



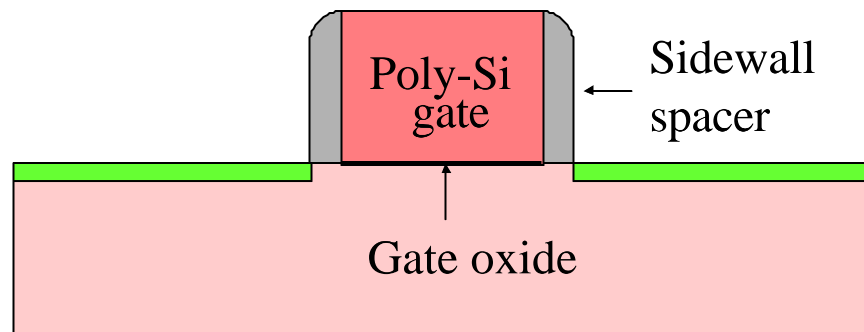
Implantation Anneal

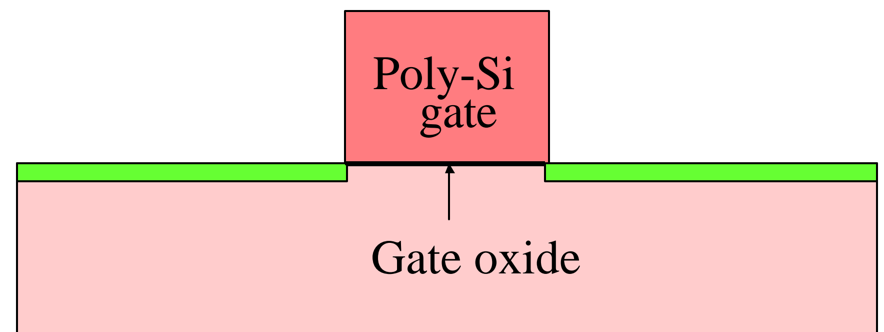


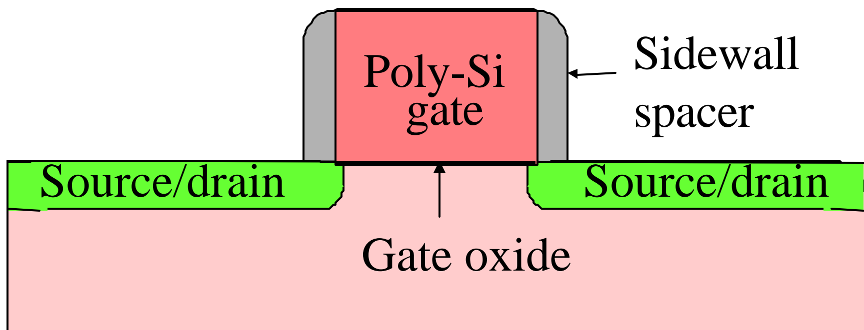
Dopant Diffusion Buffer

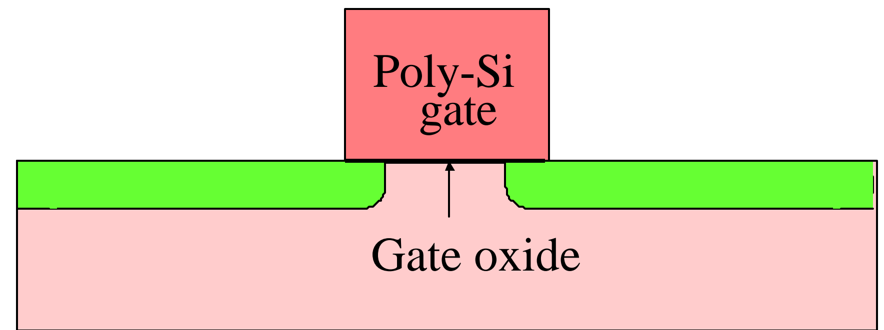
- Sub-0.18 μm, and <1.5 V, hot electron effect may not be so important anymore
- The LDD implantation process probably is no longer needed.
- Sidewall spacers are still needed to provide a diffusion buffer for the dopant in the source/drain junction.

Dopant Diffusion Buffer









(a) After anneal, source/drain are just right

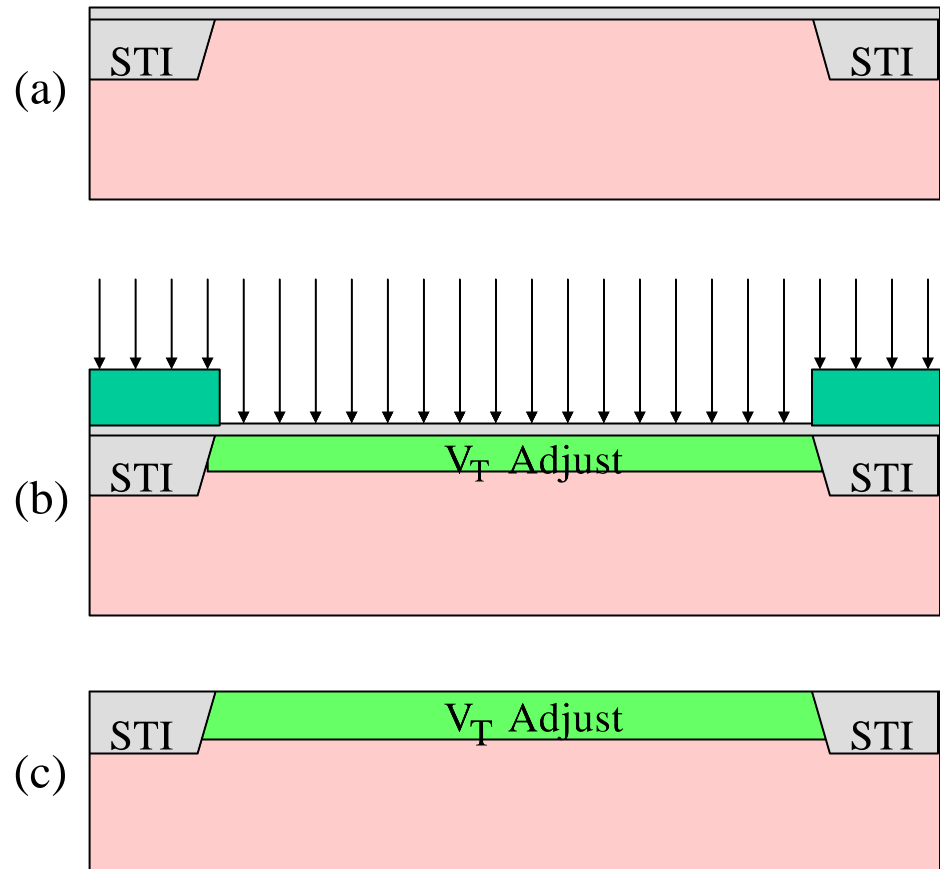
(b) After anneal, source/drain are too close

V_T Adjustment Implantation

- Controls threshold voltage of MOSFET
  - Ensure supply voltage can turn-on or turn-off the MOSFET in IC chip
- Low energy, low current implantation
- Usually before the gate oxide growth
- Two implantations: a p-type and an n-type

V_T Adjust Implantation

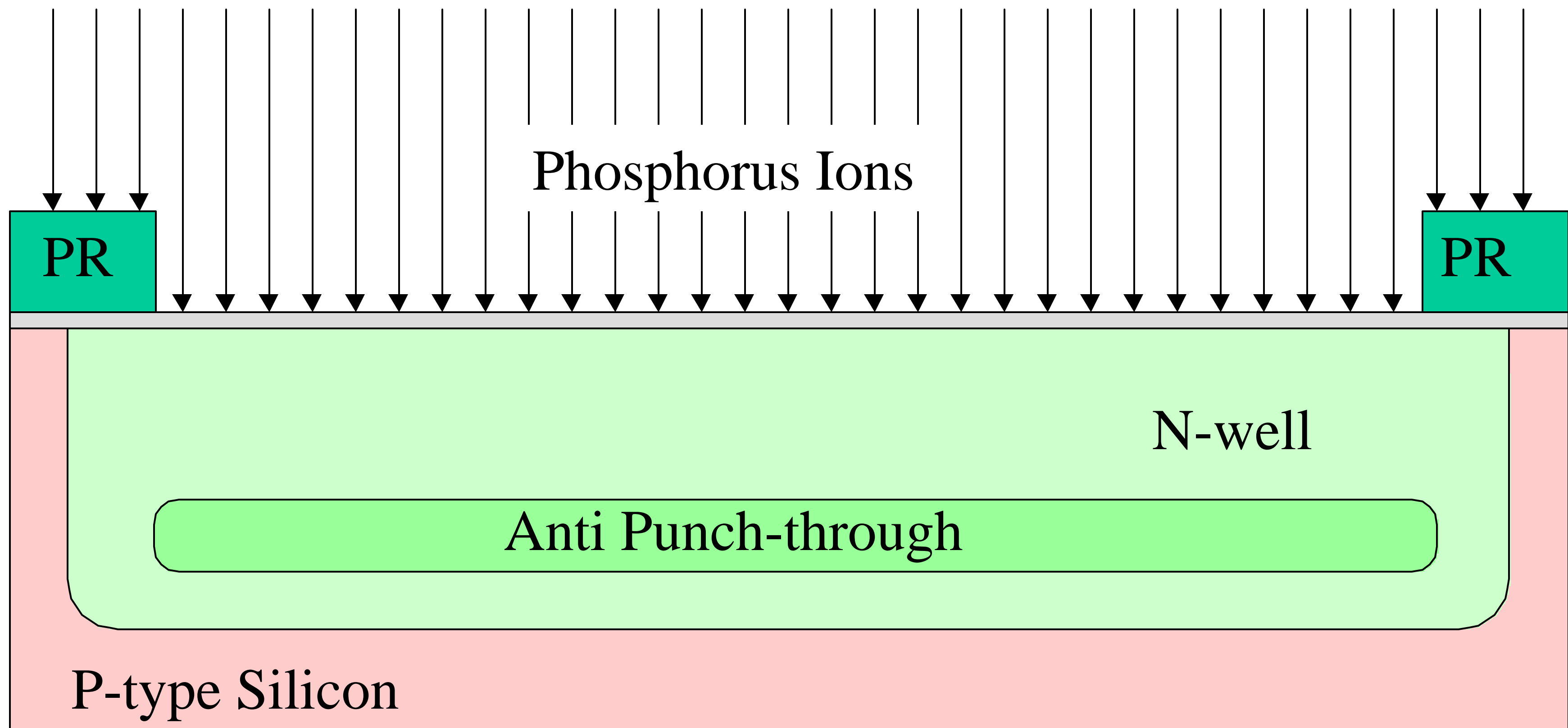
- Wafer clean
- Grow sacrificial oxide (a)
- Activation mask
- Threshold adjustment implantation (b)
- Strip photoresist
- Anneal
- Strip sacrificial oxide (c)



Anti-punch-through Implantation

- Punch-through effect
  - The depletion regions of the source and drain short each other under the influence of both gate-substrate bias and source-drain bias
- Anti punch-through implantation
  - Medium energy, low current
  - Protects transistors against punch-through
  - Normally performed with well implantation

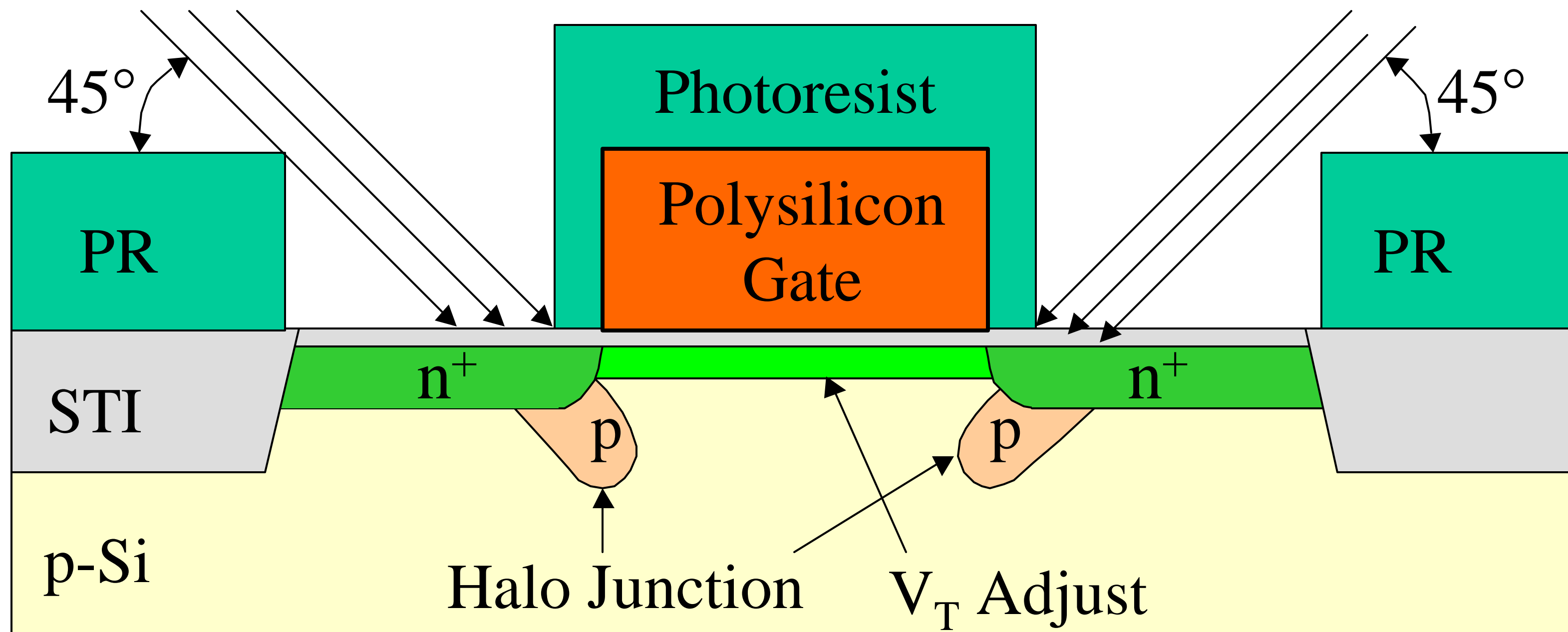
Anti Punch-through Implantation



Halo Implantation

- Another implantation process commonly used to suppress punch through effect
- Low energy and low current
- Large incident angle, 45°

Halo Implantation



High-κ Gate Dielectric

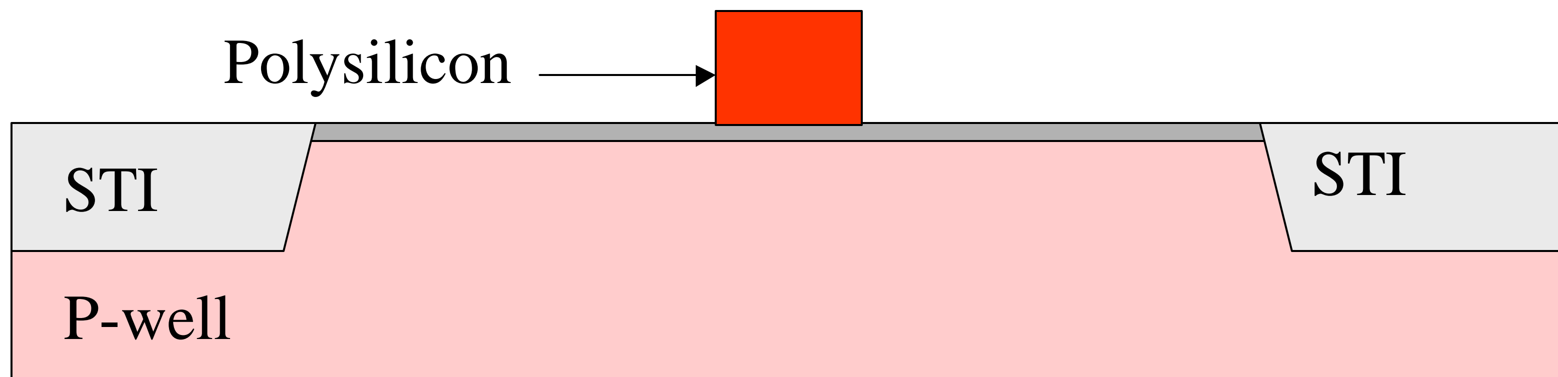
- Device sizes shrinking, t_{ox} is too thin for MOSFET to operate reliably even at 1 V
- Need high-κ dielectric to replace SiO_2 as gate dielectric material for < 0.1 μm device
  - High-κ, thicker gate dielectric, better prevention of tunneling and breakdown
  - Large enough gate capacitance to hold enough charges to turn-on the MOSFET

Metal Gate

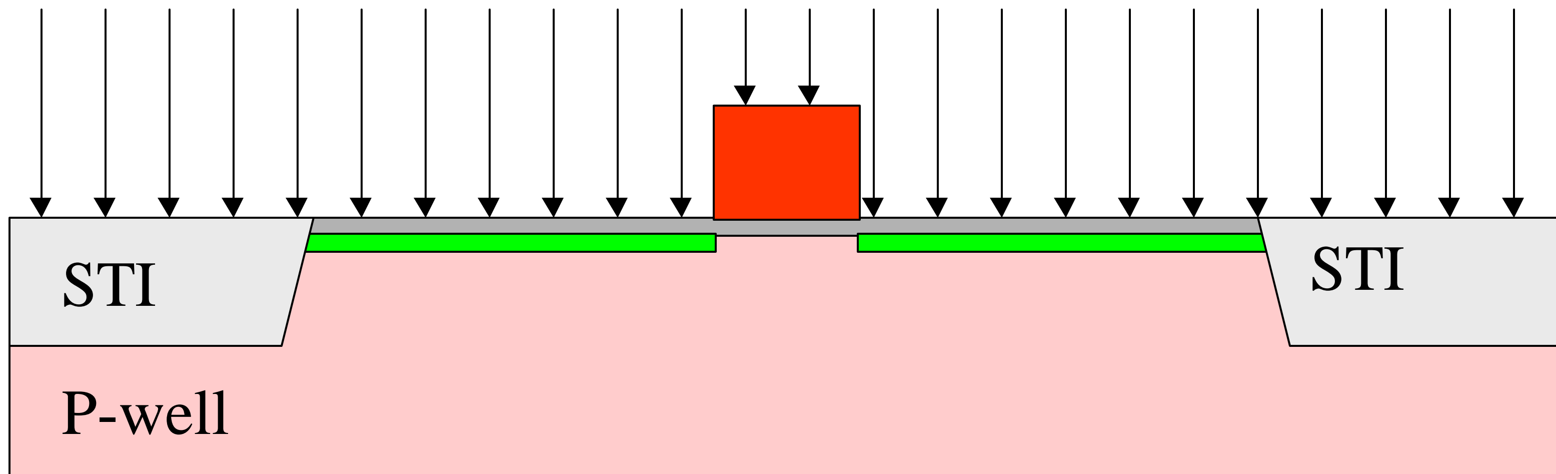
- Lower resistivity
- Help to improve device speed

- A possible future transistor making process
- Metal and high-κ dielectric gate

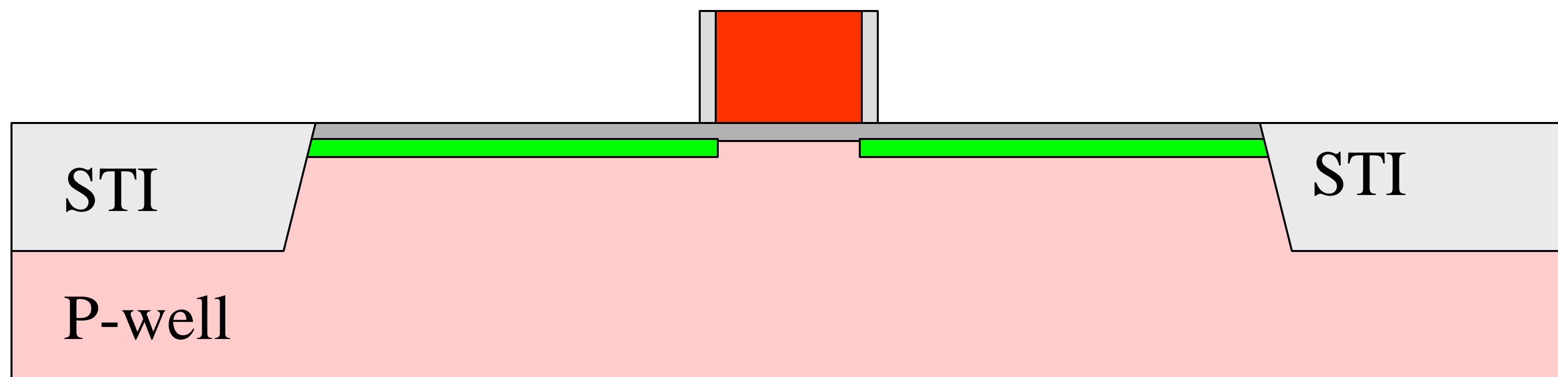
Strip Photoresist



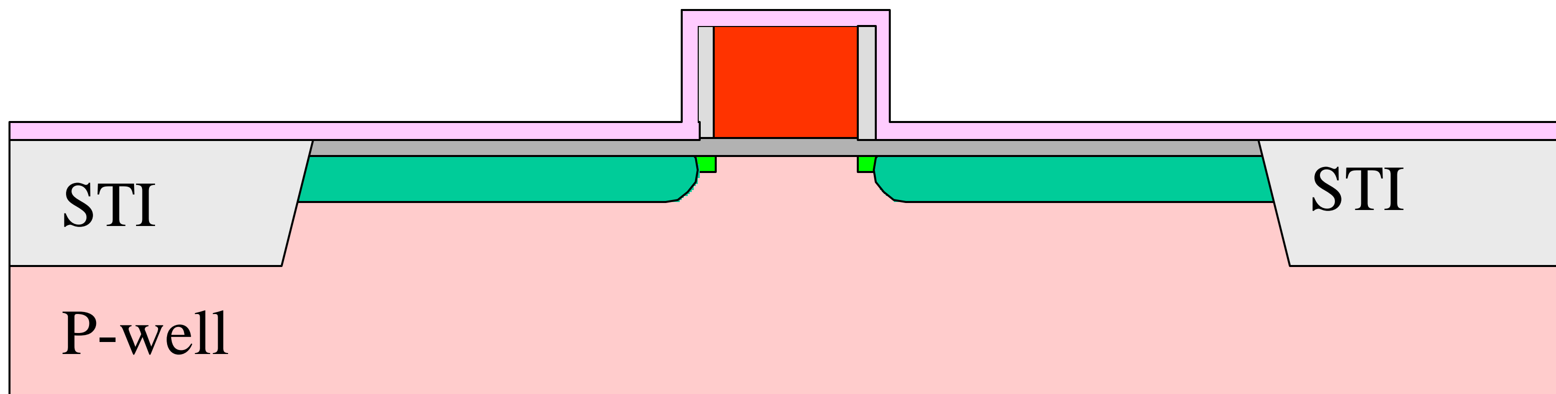
Extension Ion Implantation



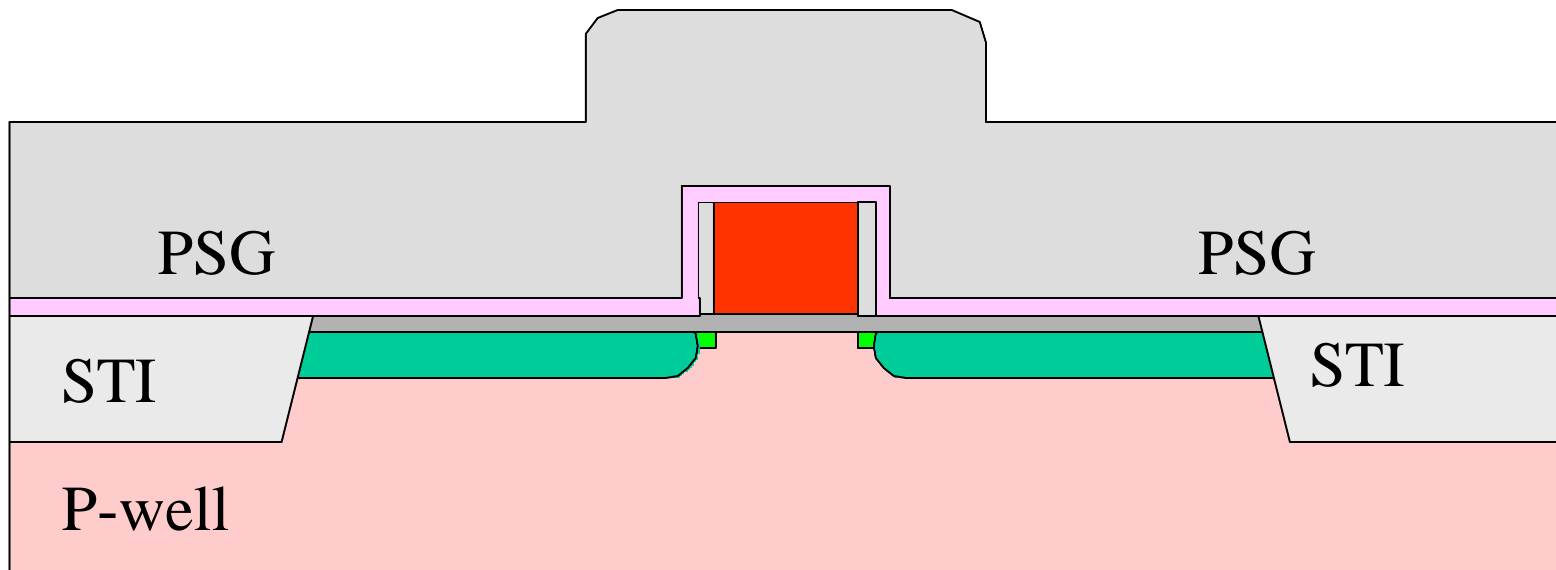
Oxide/Nitride Etch Back,



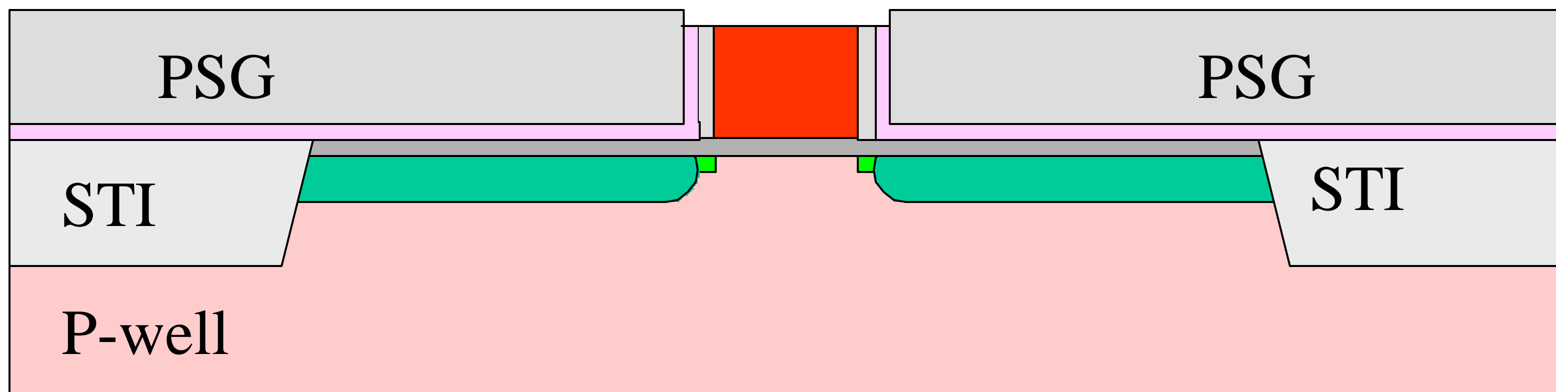
RPCVD Nitride



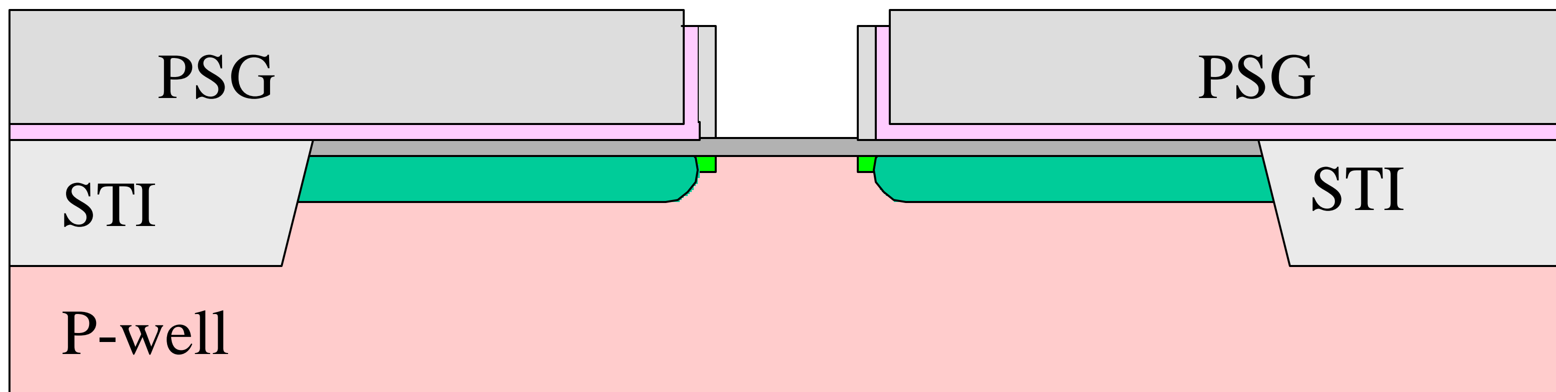
CVD PSG



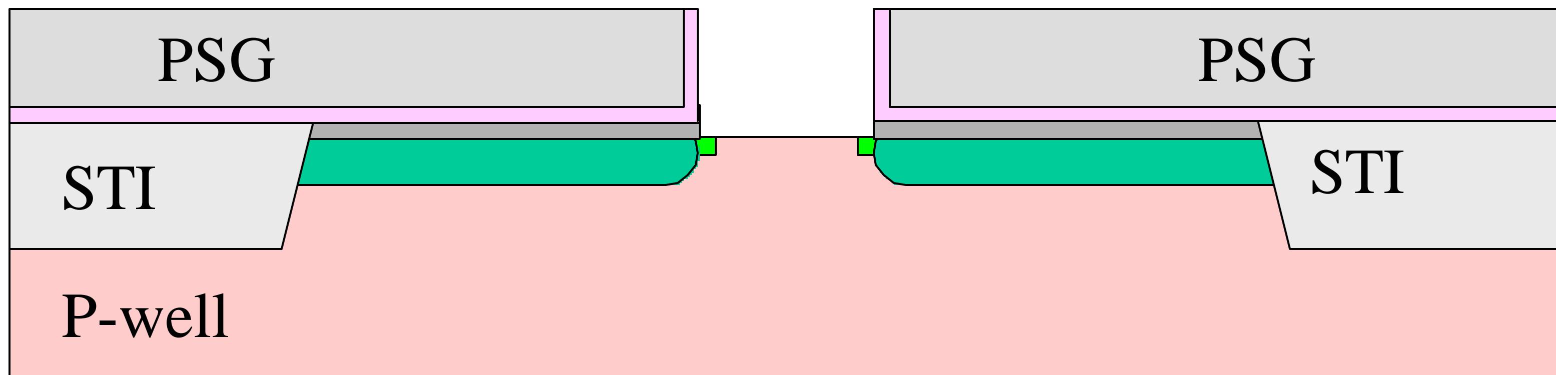
Strip Nitride



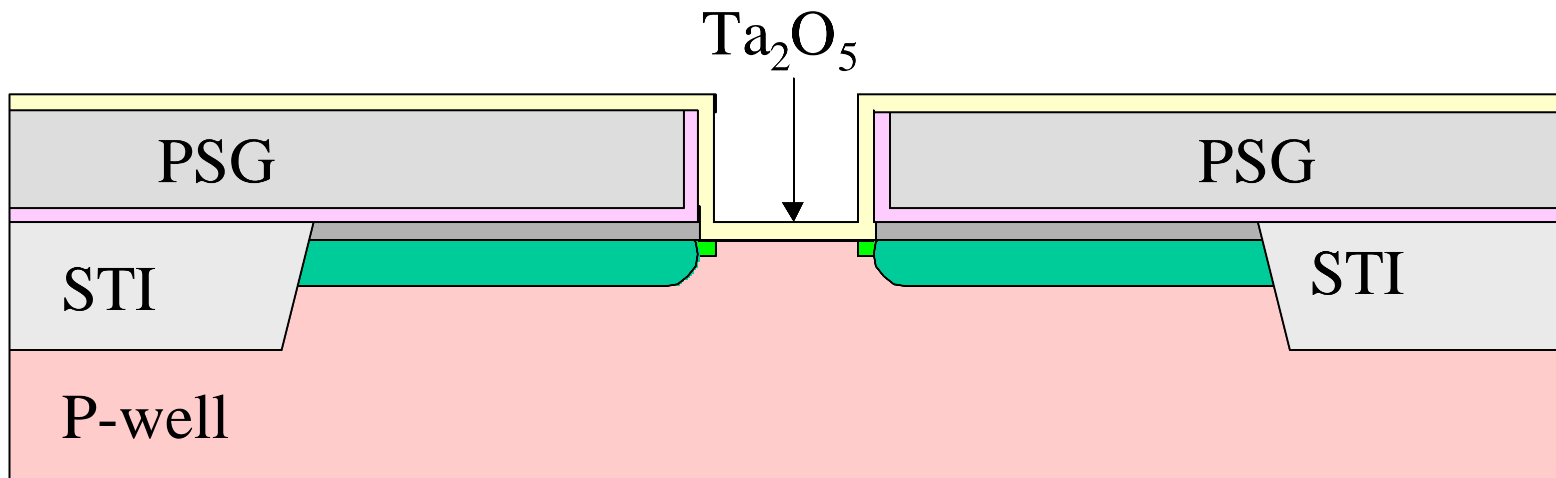
Strip Polysilicon



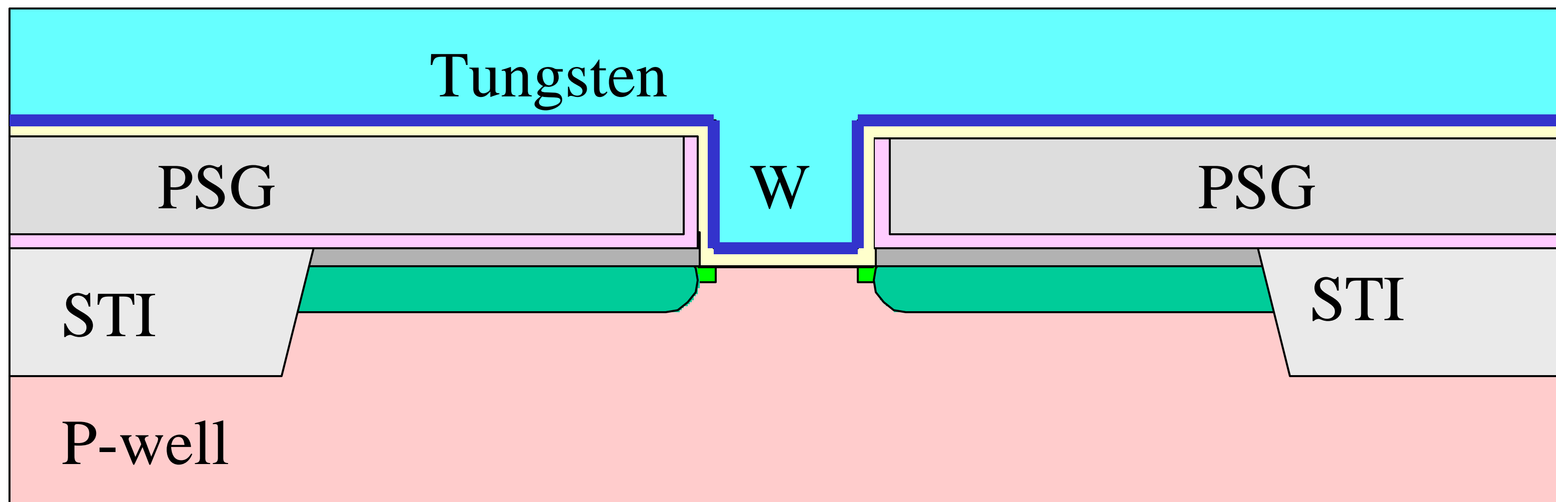
Strip Oxide



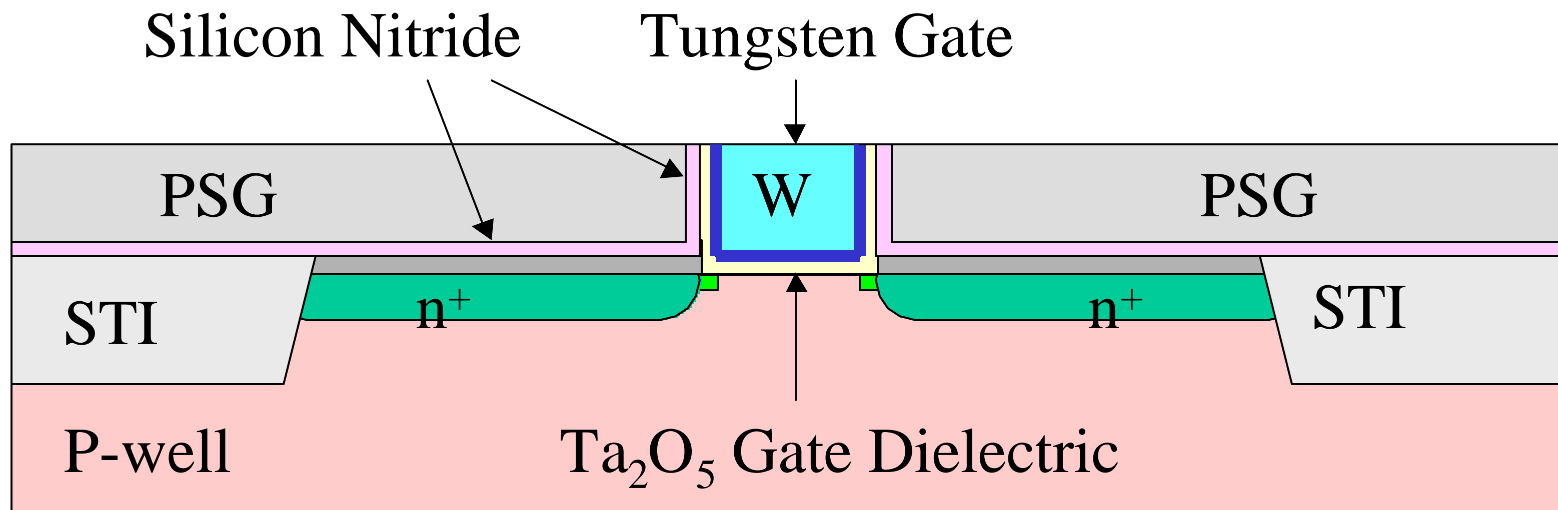
Deposit (Ta_2O_5) and RTA



CVD Tungsten



CMP Tantalum Pentaoxide



Metal and High-κ Gate MOSFET Dummy Gate Process

- For < 0.1 μm IC device
- PSG CMP, polysilicon and oxide stripping, and high-κ dielectric deposition.
- Ta_2O_5, κ ~ 25, TiO_2 κ up to 80, and HfO_2
- CVD plus RTA process
- It may never be used due to complexity
- Advantage: can used Ta_2O_5 hard hard to etch.

Metal and High-κ Gate MOSFET Traditional Process

- Traditional MOSFET making process in R&D
  - Dielectric deposition and annealing
  - Metal deposition
  - Photolithography
  - Metal etch
  - Ion implantation
  - Rapid thermal annealing.
- Too early to predict which method will win

Interconnection

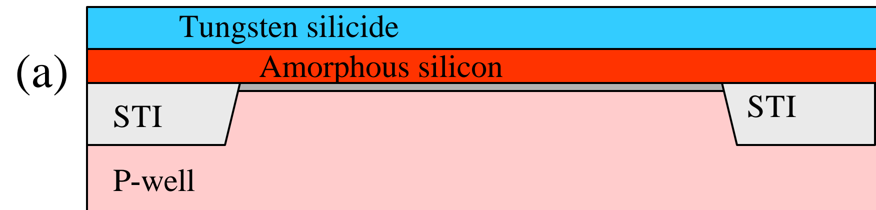
- Making transistor: front-end
- Interconnection: back-end
  - Multi metal layers with dielectric in between
  - Local interconnection: silicide
  - PMD: doped oxide, PSG or BPSG
  - W and Al alloy metallization
  - IMD: USG and FSG
  - Transition to copper and low-κ interconnection

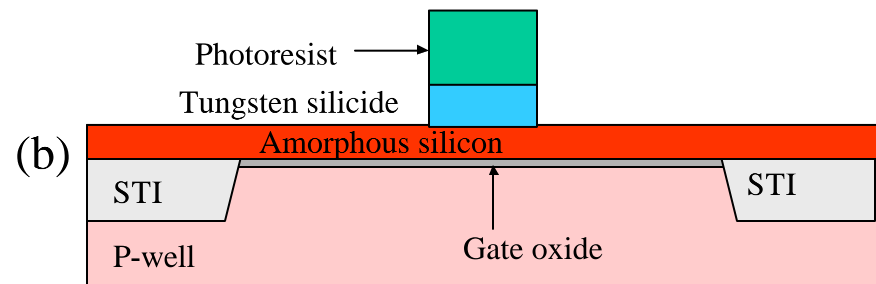
Local Interconnection

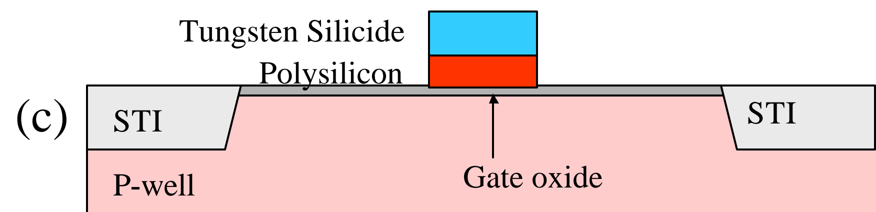
- Connection between neighboring transistors
- Usually polysilicon or polycide stack
- WSi_2, $TiSi_2$, and $CoSi_2$ are commonly used
  - WSi_x: CVD process with WF_6 and SiH_4
- $TiSi_2$: PVD Ti on Si then thermal anneal

Tungsten Silicide Process

- Wafer clean
- Grow gate oxide
- Deposited amorphous silicon
- Deposited tungsten silicide (a)
- Gate and local interconnection mask
- Etch tungsten silicide (fluorine chemistry) (b)
- Etch amorphous silicon (chlorine chemistry)
- Strip photoresist
- Polysilicon and silicide annealing (c)



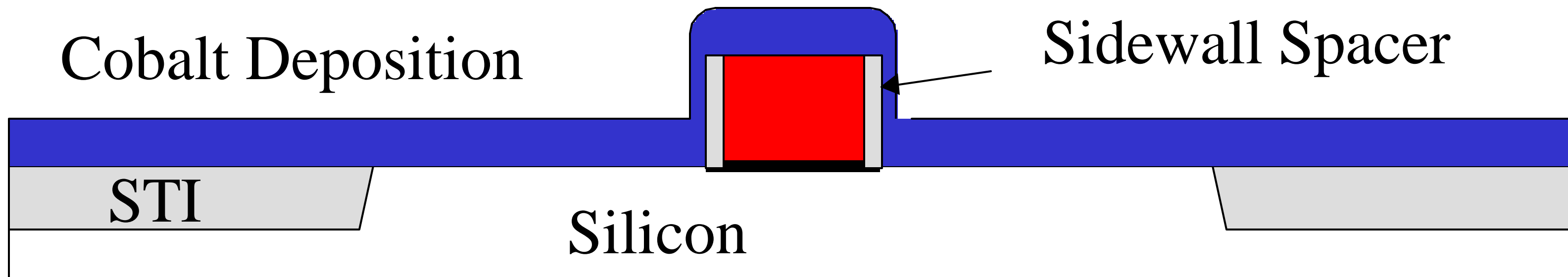


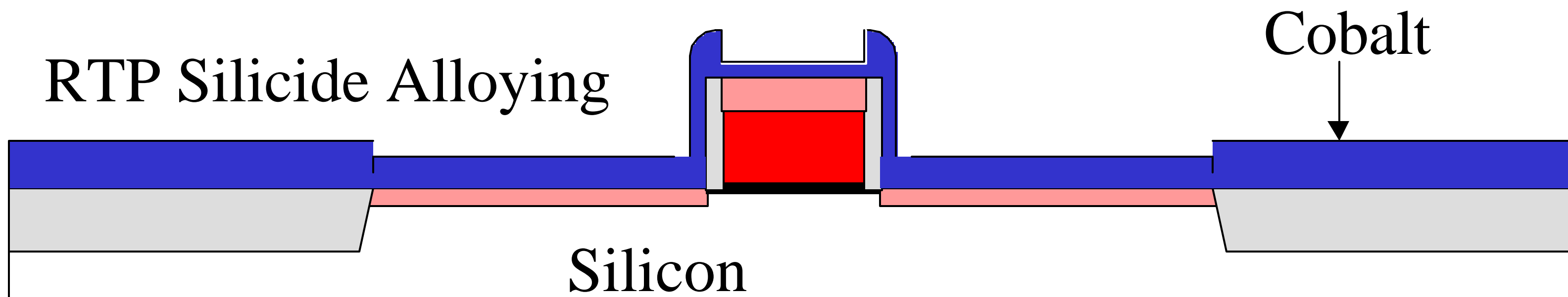


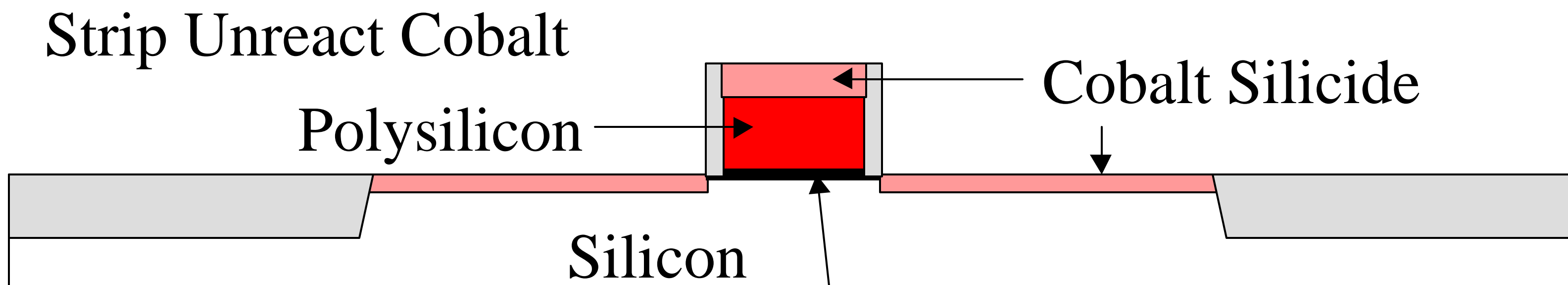
Self-aligned Silicide (Salicide)

- $TiSi_2$ and $CoSi_2$
- Lower resistivity than WSi_2
- $TiSi_2$ when gate size > 0.2 μm
- $CoSi_2$ when gate size < 0.2 μm
- Metal (Ti or Co) PVD
- Thermal anneal to form silicide
- Strip unreacted metal

Cobalt Self-aligned Silicide Process





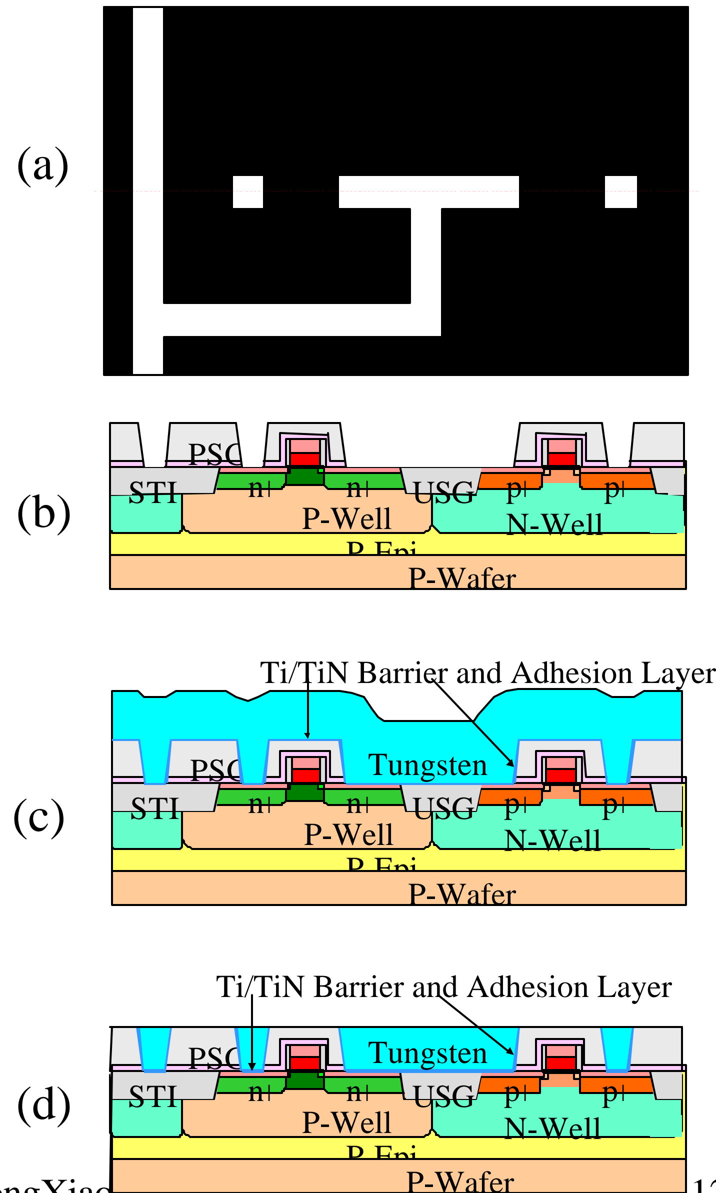


Tungsten Local Interconnection

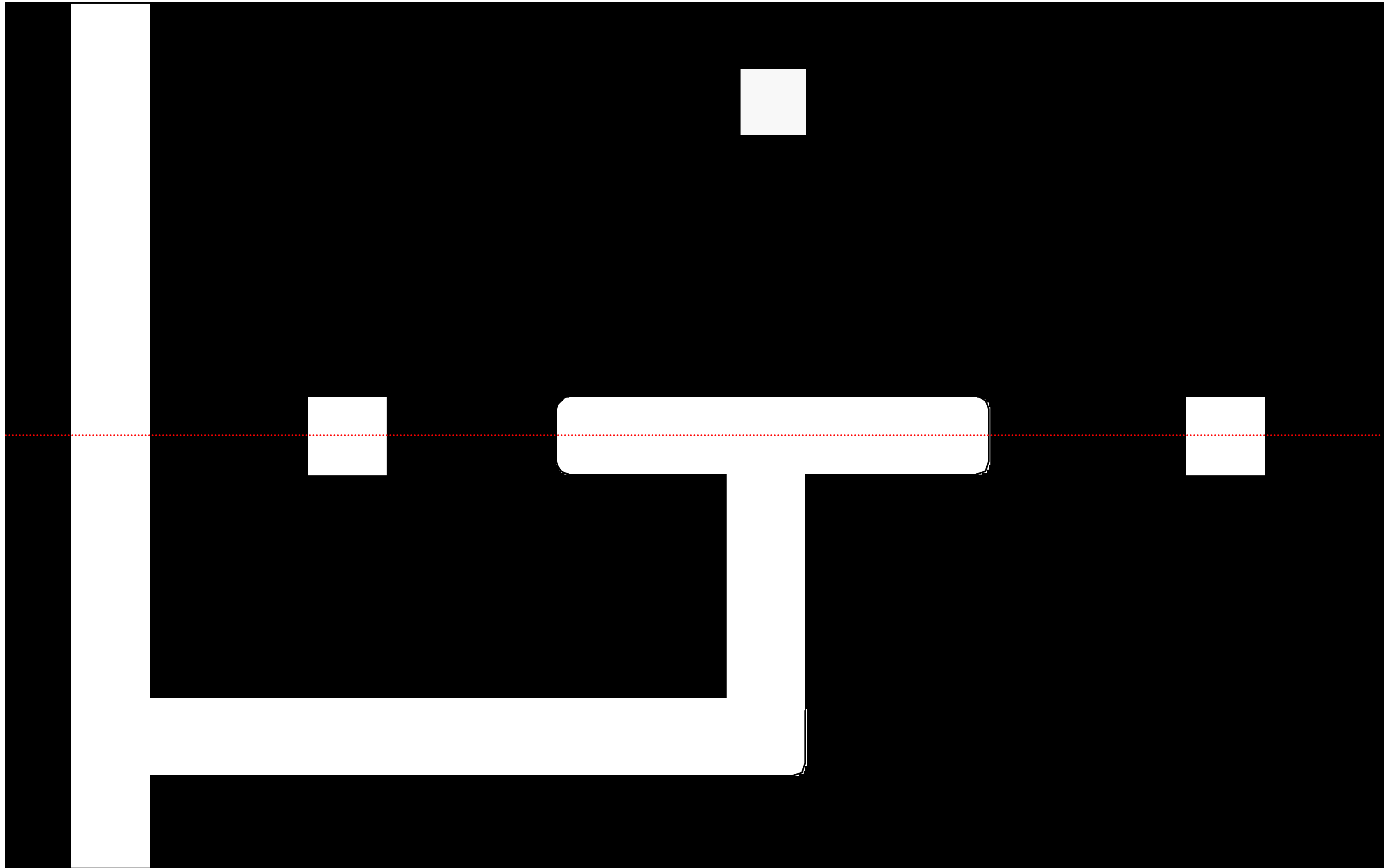
- Lower resistance, higher speed, less power
- Damascene: similar to W plug formation
  - Etched trenches are in silicate glass layer
  - Deposit Ti and TiN barrier/adhesion layers
  - CVD W fill trenches
  - CMP to remove bulk W from wafer surface
  - W left in trenches to form local interconnection

Tungsten Local Interconnection

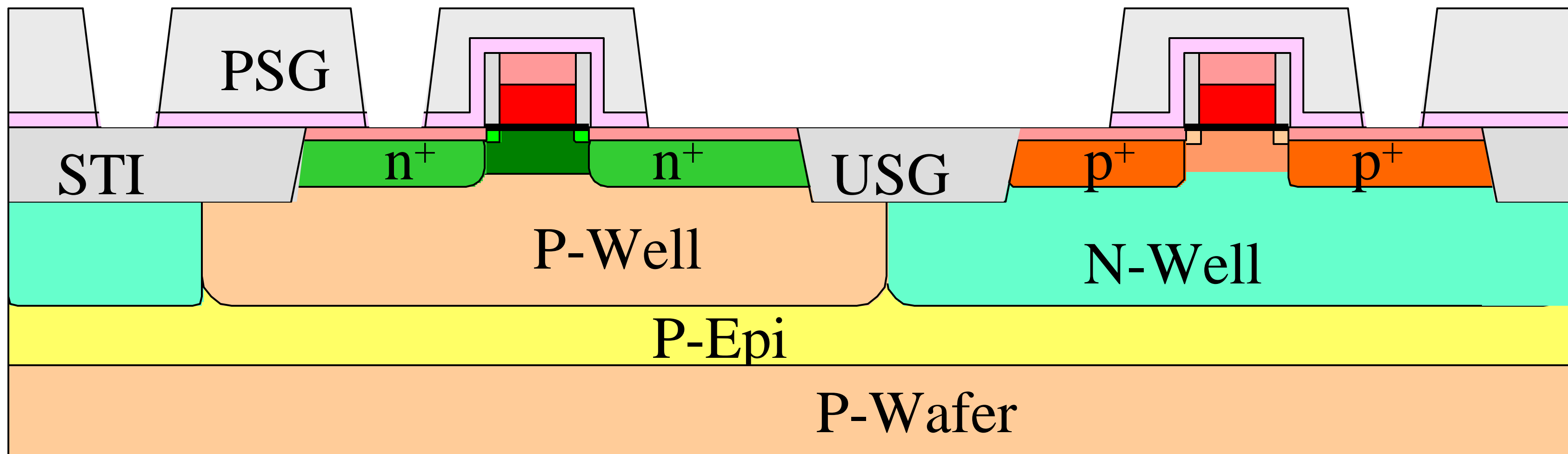
- CMP PSG
- Wafer clean
- Local interconnection mask (a)
- Etch PSG
- Strip photoresist
- Wafer clean (b)
- Argon sputtering clean
- Sputtering Ti
- Sputtering TiN
- CVD TiN
- TiN treatment
- CVD Tungsten (c)
- CMP Tungsten
- CMP titanium and titanium nitride (d)
- Wafer clean



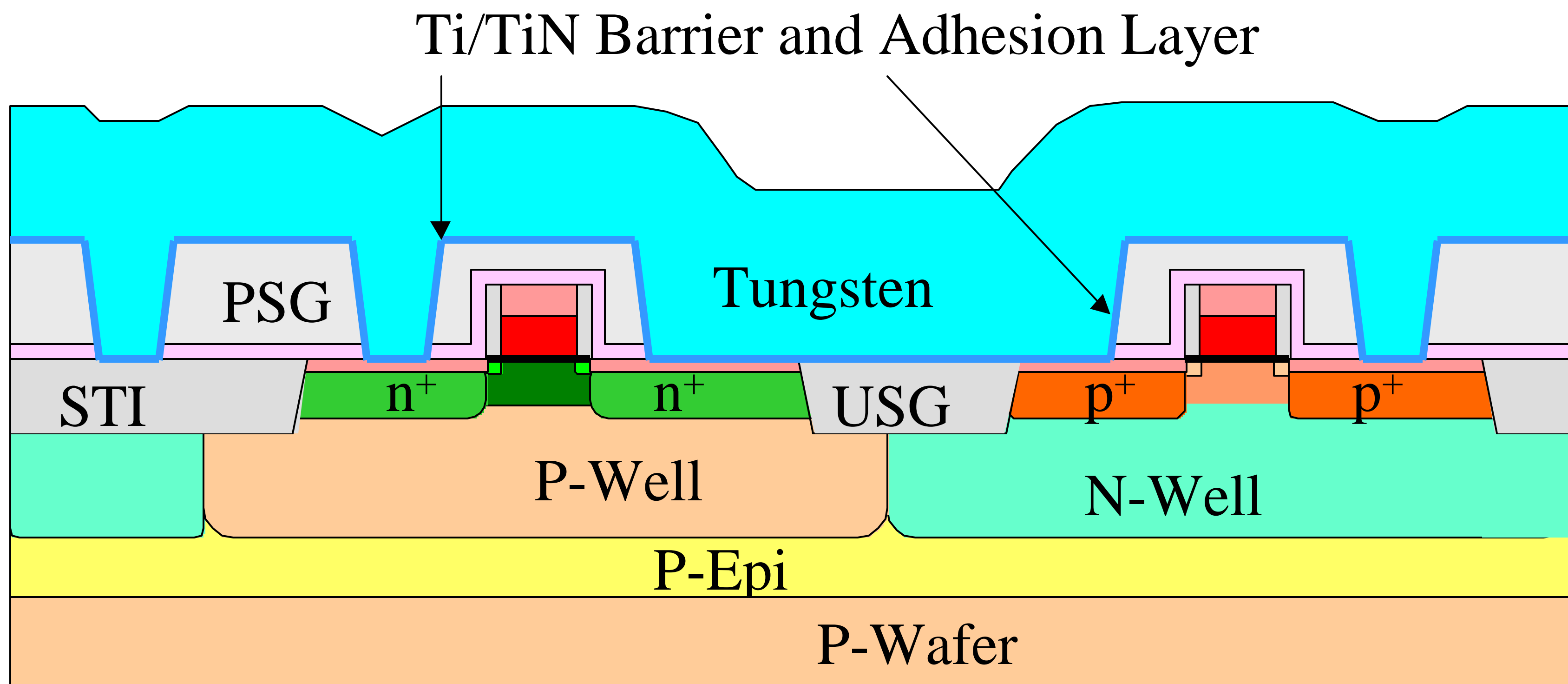
Mask 10: Local Interconnection



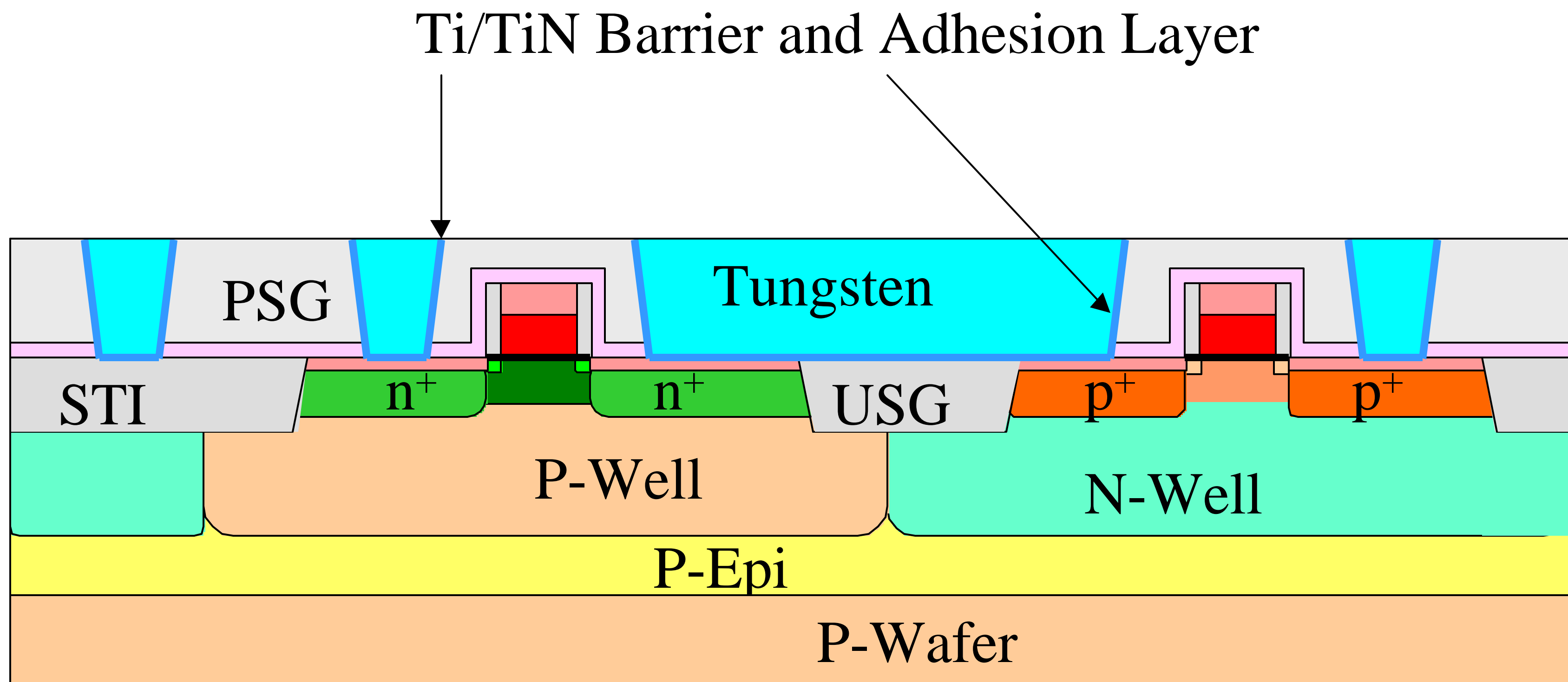
Strip Photoresist/Clean



PVD Ti/TiN and CVD TiN/W



CMP W/TiN/Ti, Clean



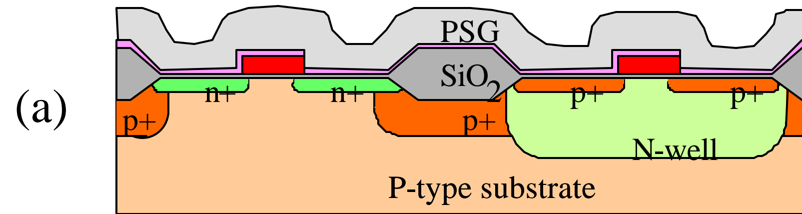
Early Global Interconnection

- Oxide CVD
- Photolithography, oxide etch, and PR strip
- Metal PVD
- Photolithography, metal etch, and PR strip
  - Oxide etch forms contact or via holes
  - metal etch forms interconnection lines

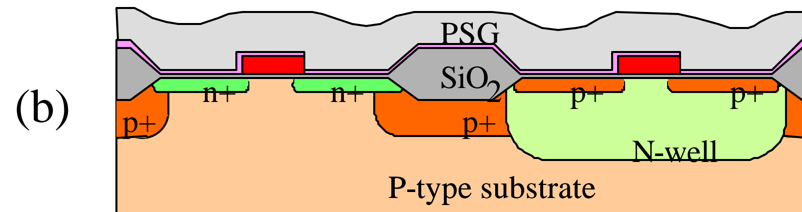
Early Aluminum Interconnection

- CVD PSG (a)
- PSG reflow (b)
- Wafer clean
- Contact hole mask
- Etch PSG
- Strip photoresist (c)
- Wafer clean
- Deposit Al alloy (d)
- Metal interconnection mask
- Etch metal
- Strip photoresist (e)
- Metal anneal

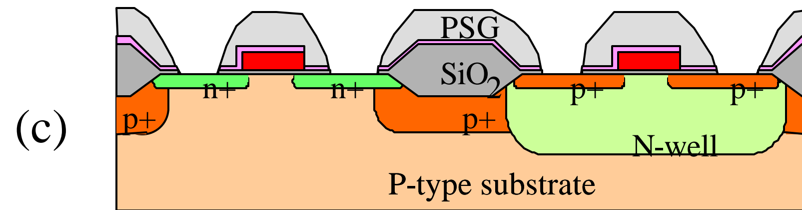
(a)



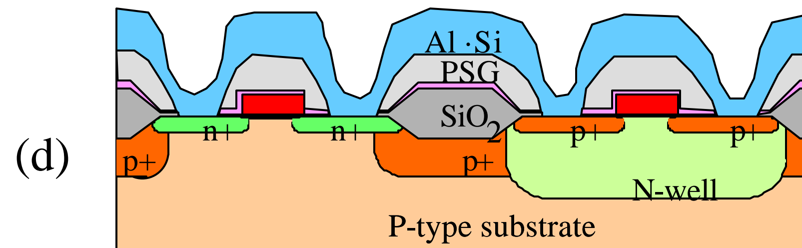
(b)



(c)



(d)



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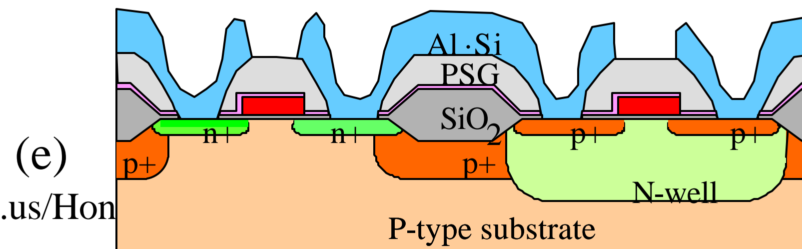


Multi-level Interconnection

- Earlier interconnection has rough surface
- problems in photolithography and metal PVD
- Tungsten to fill narrow contact and via holes

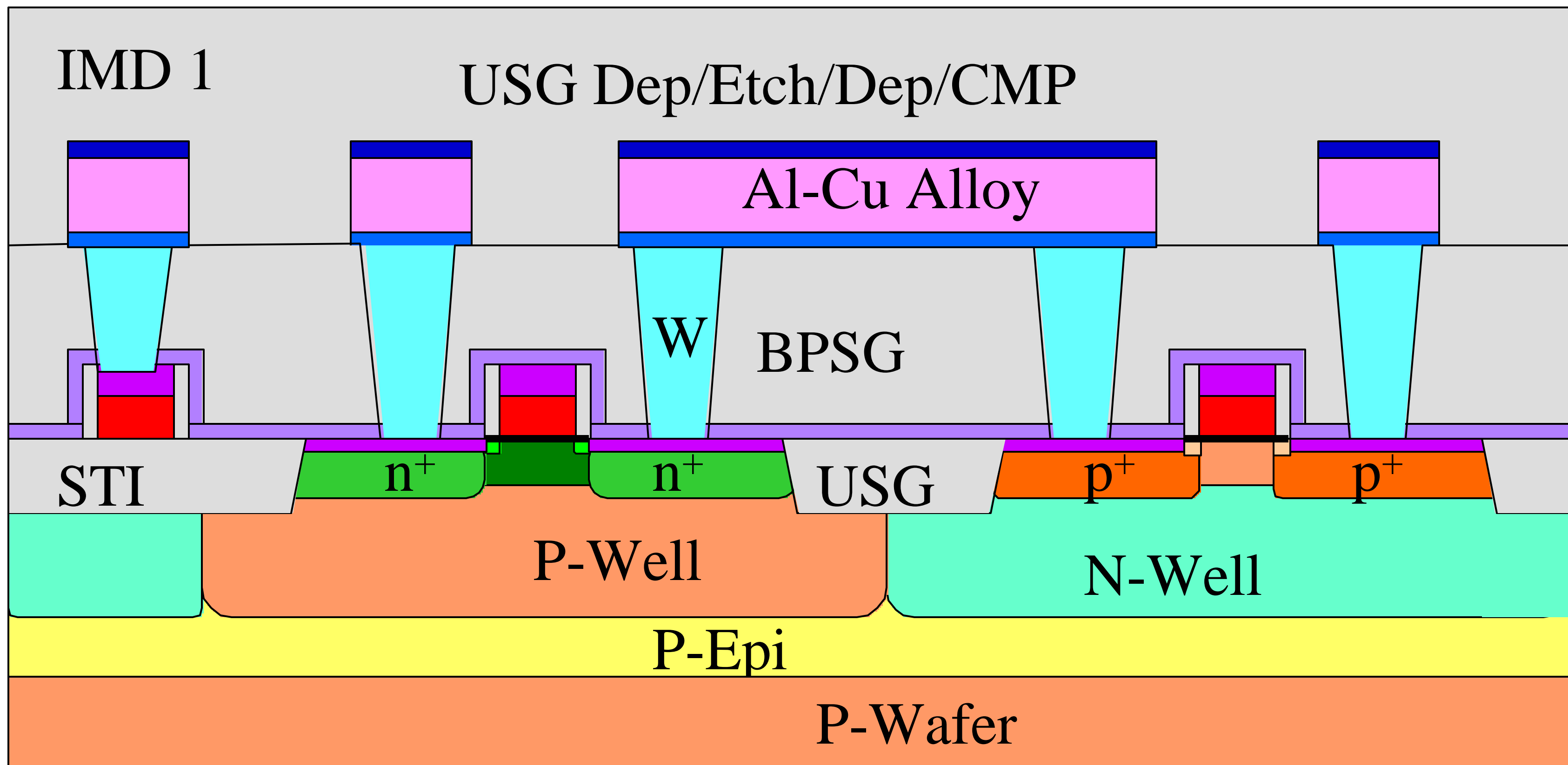
Multi-level Interconnection

- The basics interconnection process steps:
  - Dielectric CVD and planarization
  - Photolithography, oxide etch, and PR strip
  - W CVD, bulk W removal
  - Metal stack PVD,
  - Photolithography, oxide etch, and PR strip
- PSG or BPSG for PMD and USG for IMD

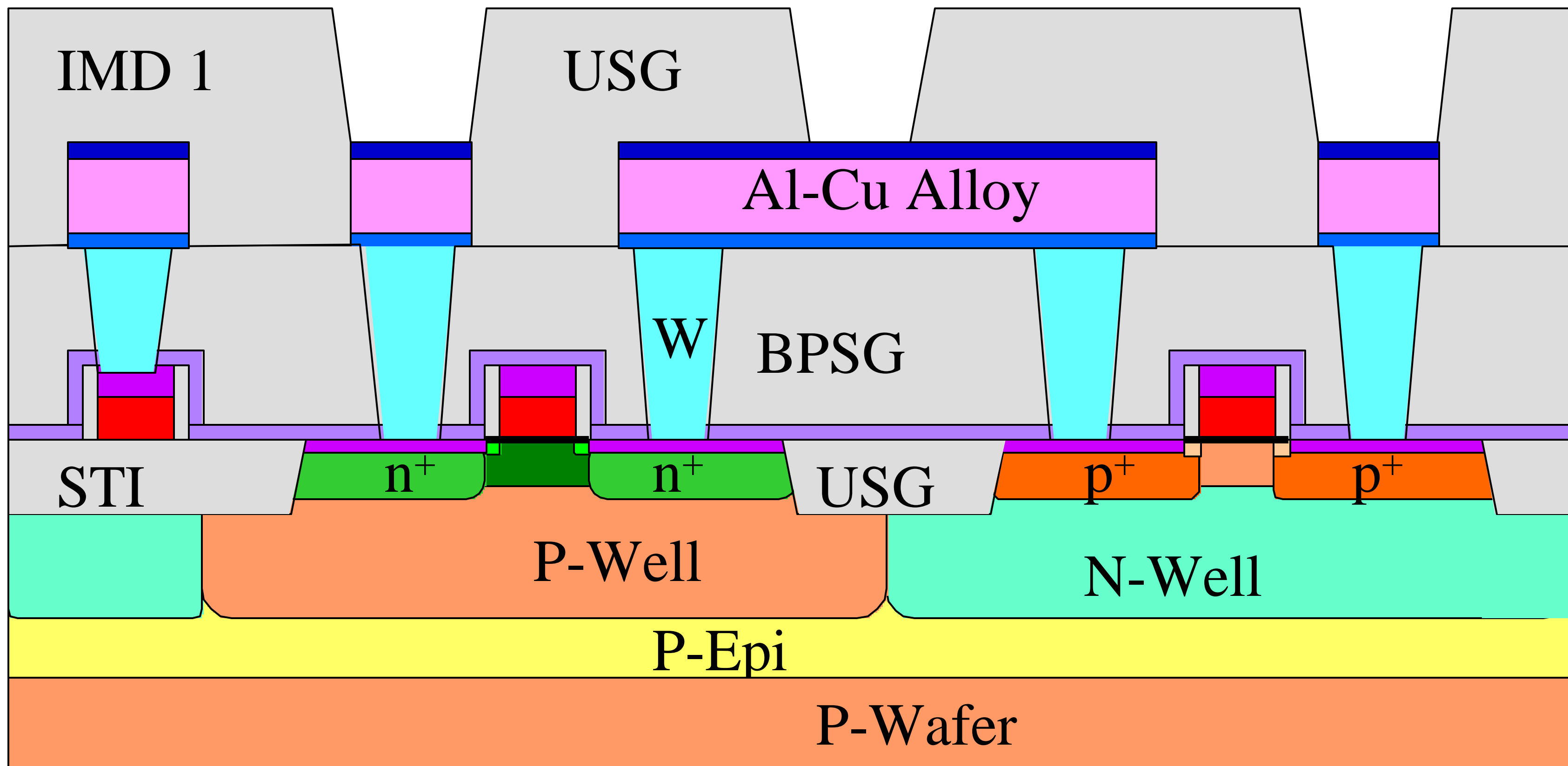
Multi-level Interconnection

- Dielectric CMP for planarization
- W CMP to removal bulk tungsten
- Metal stack: Ti welding layer, Al·Cu alloy, and TiN ARC
- Metal etch defines metal interconnection lines

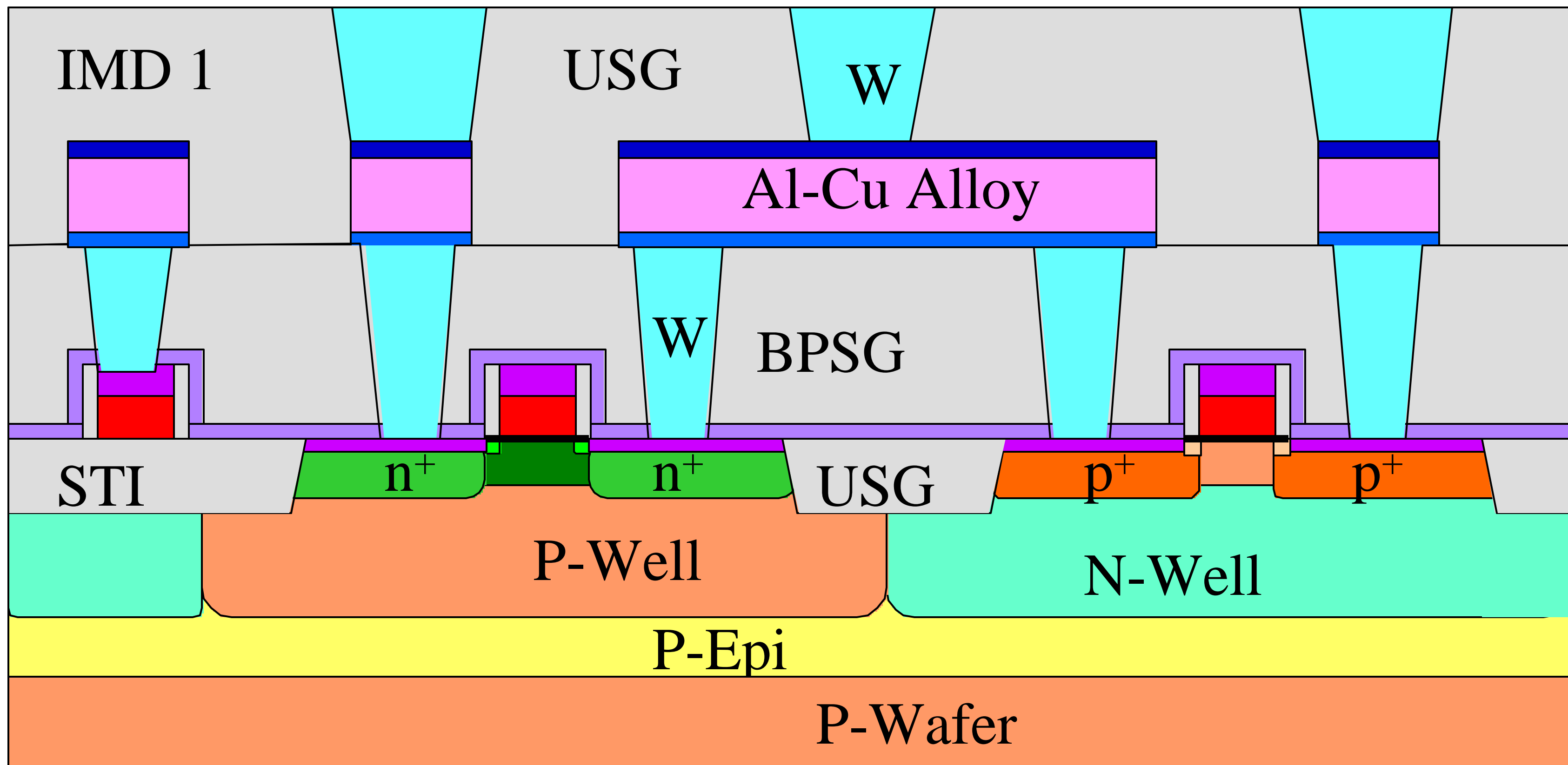
PE-TEOS USG Dep/Etch/Dep/CMP



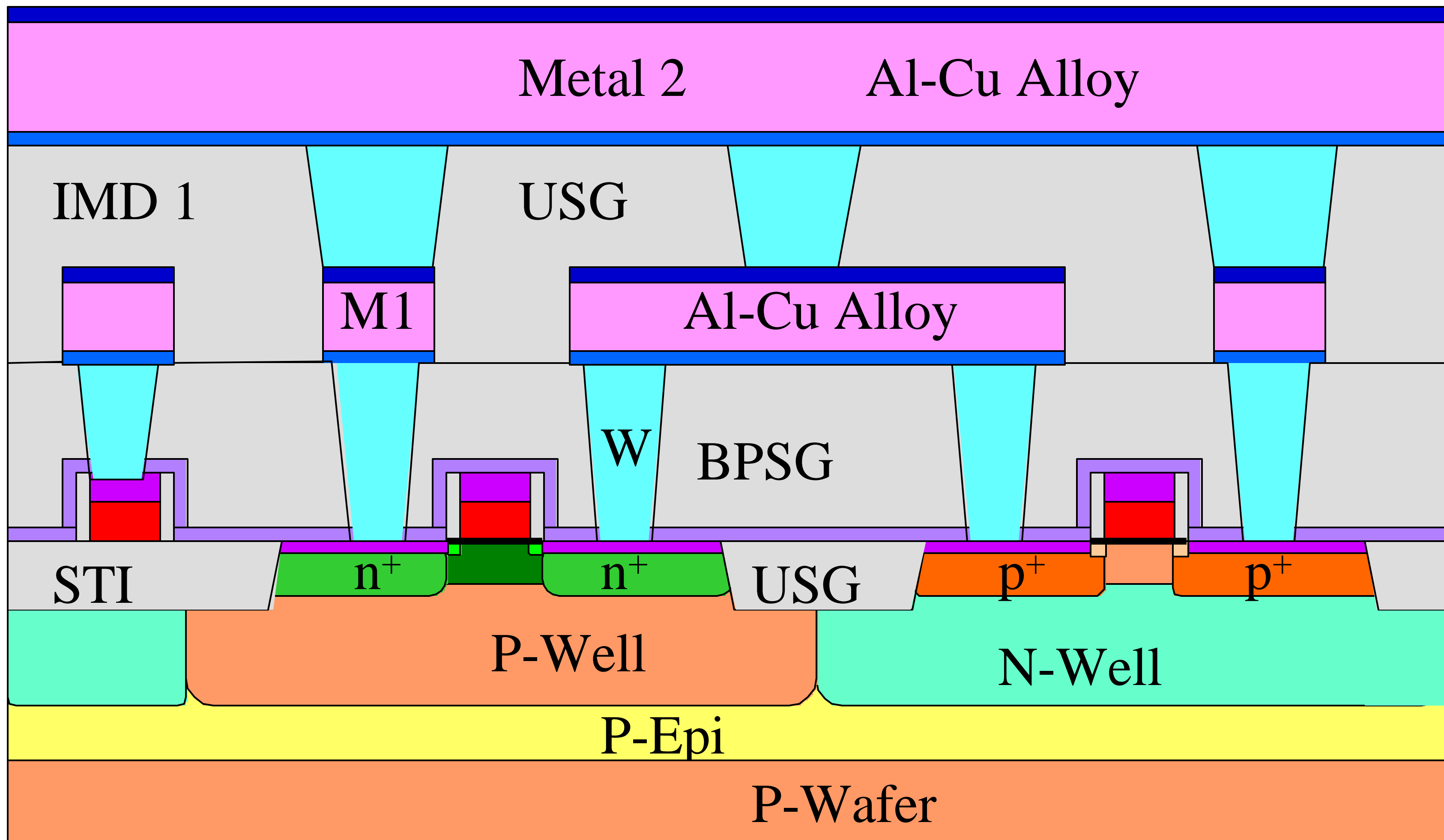
Via Etch, Etch USG



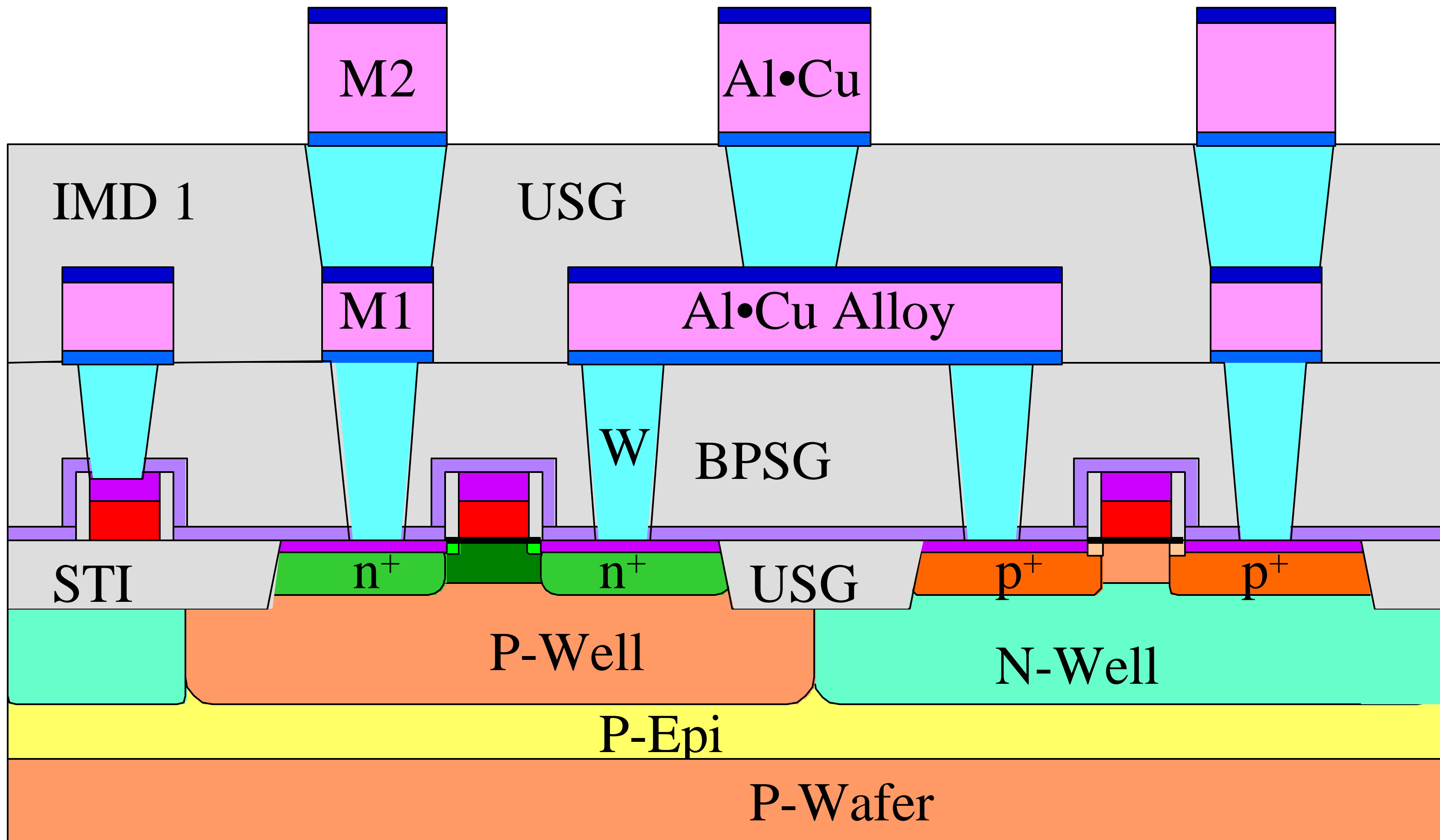
Tungsten CVD and CMP



Via Etch, Etch USG



Etch Metal 2



Copper Interconnection

- Lower resistivity and higher resistance toelectromigration than aluminum alloy
- Faster and reliable interconnection
- Hard to dry etch delayed copper application
- CMP developed and matured in the 1990s
- Used in bulk W removal for plug formation
- Copper process is similar to W plug process

Copper Interconnection

- Trenches are etched on dielectric surface
- Copper is deposited into the trenches
- CMP removes bulk copper layer on surface
- Copper lines embedded in dielectric layer
- No need for metal etch

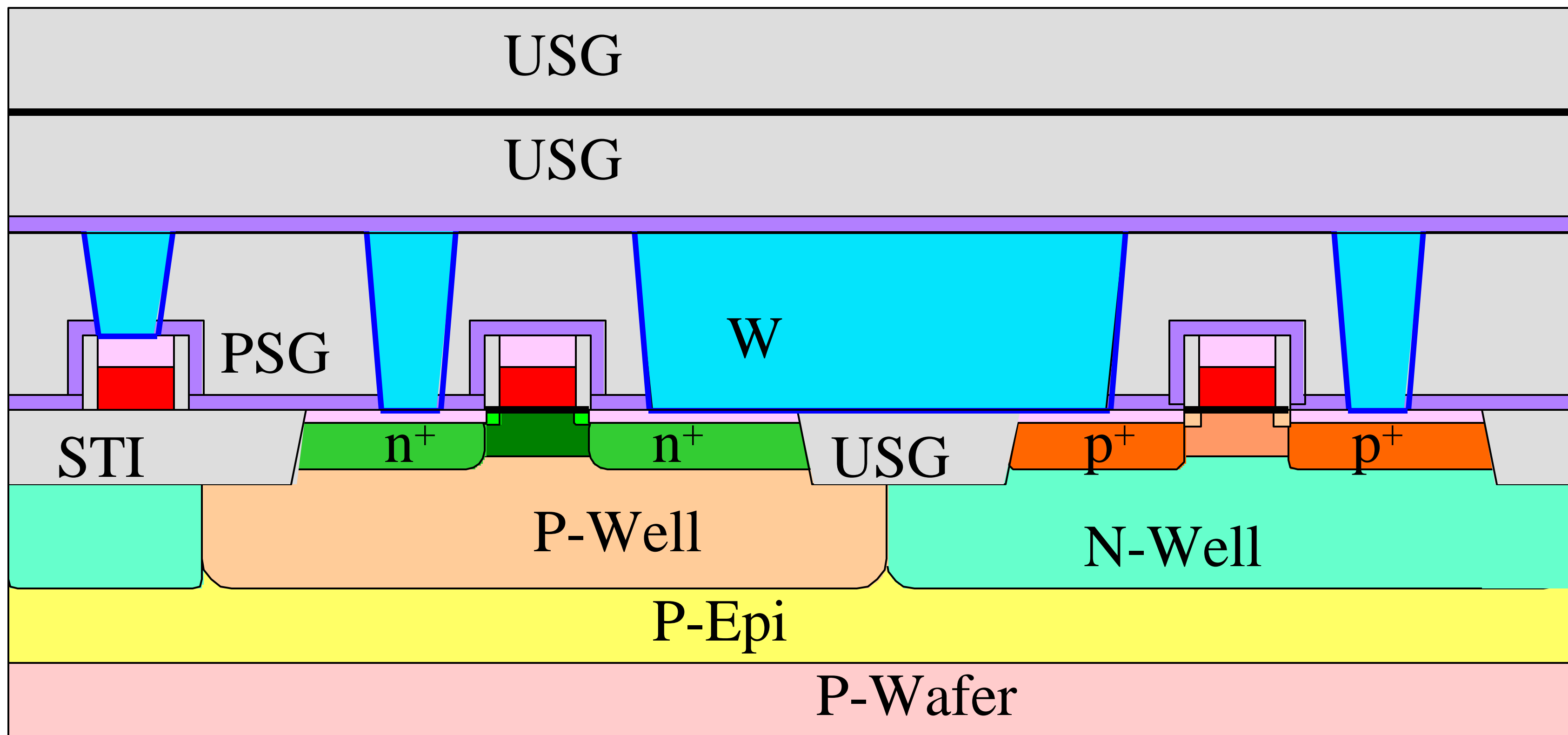
Copper Interconnection

- Dual damascene process
- Most commonly used method for the copper metallization
  - Photolithography, etch via, and PR strip
  - Photolithography, etch trench, and PR strip
  - Metal depositions and anneal
  - Metal CMP

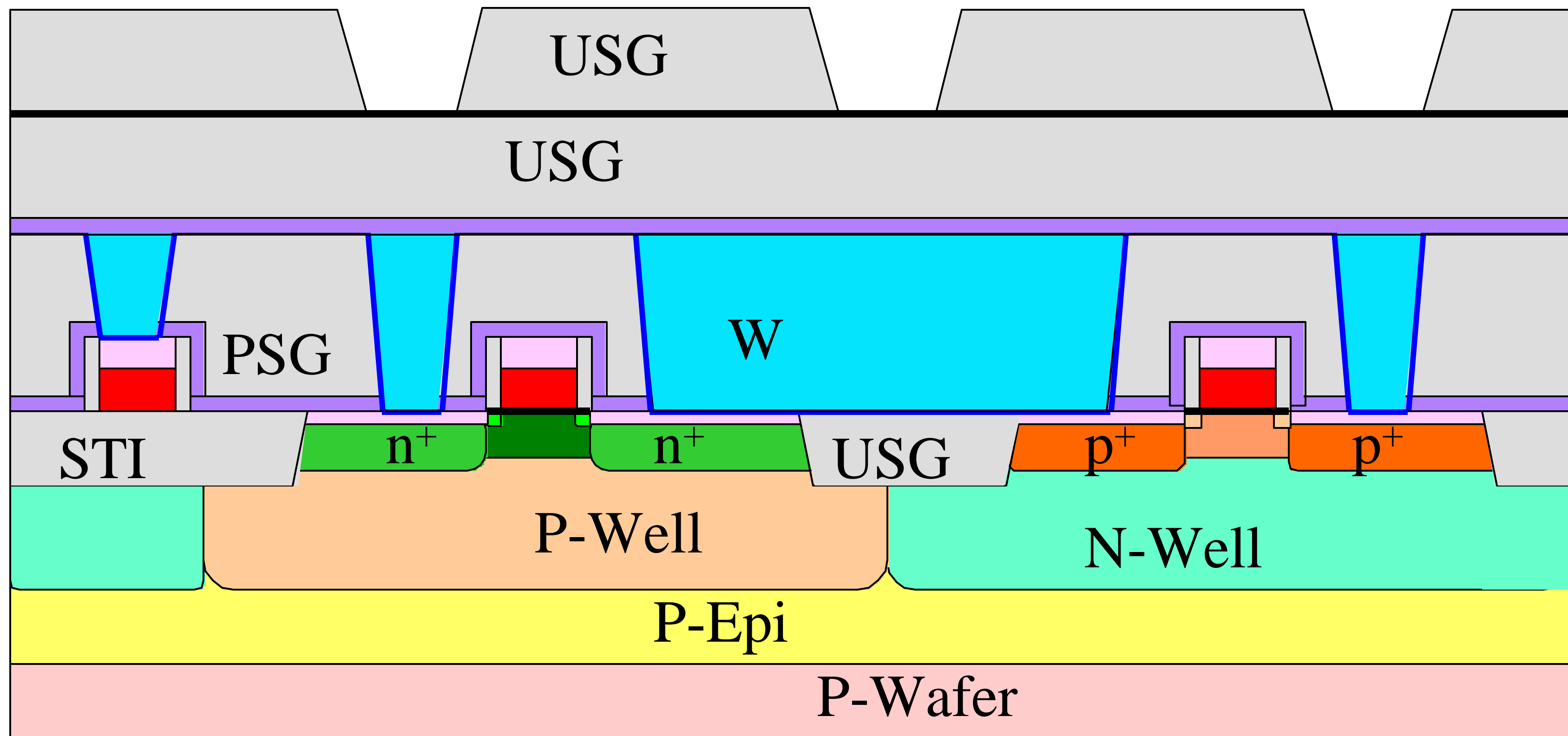
Basic Differences

- Traditional process: one dielectric etch and one metal etch
- Dual damascene copper process: two dielectric etches, no metal etch
- The main challenges of the dual damascene copper process are dielectric etch, metal deposition and metal CMP

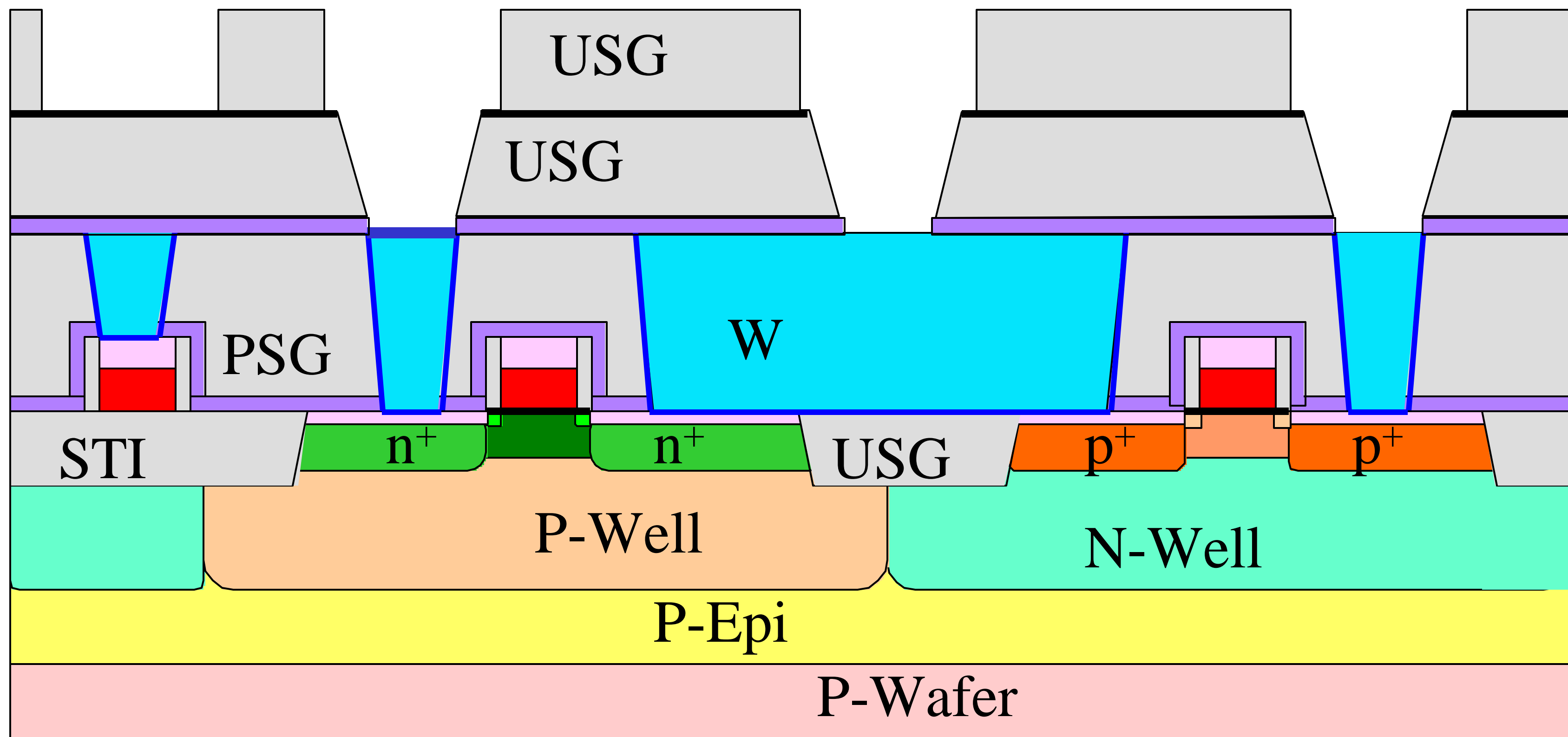
PECVD Nitride/USG/nitride/USG



Via Mask, Etch Via, and Strip PR



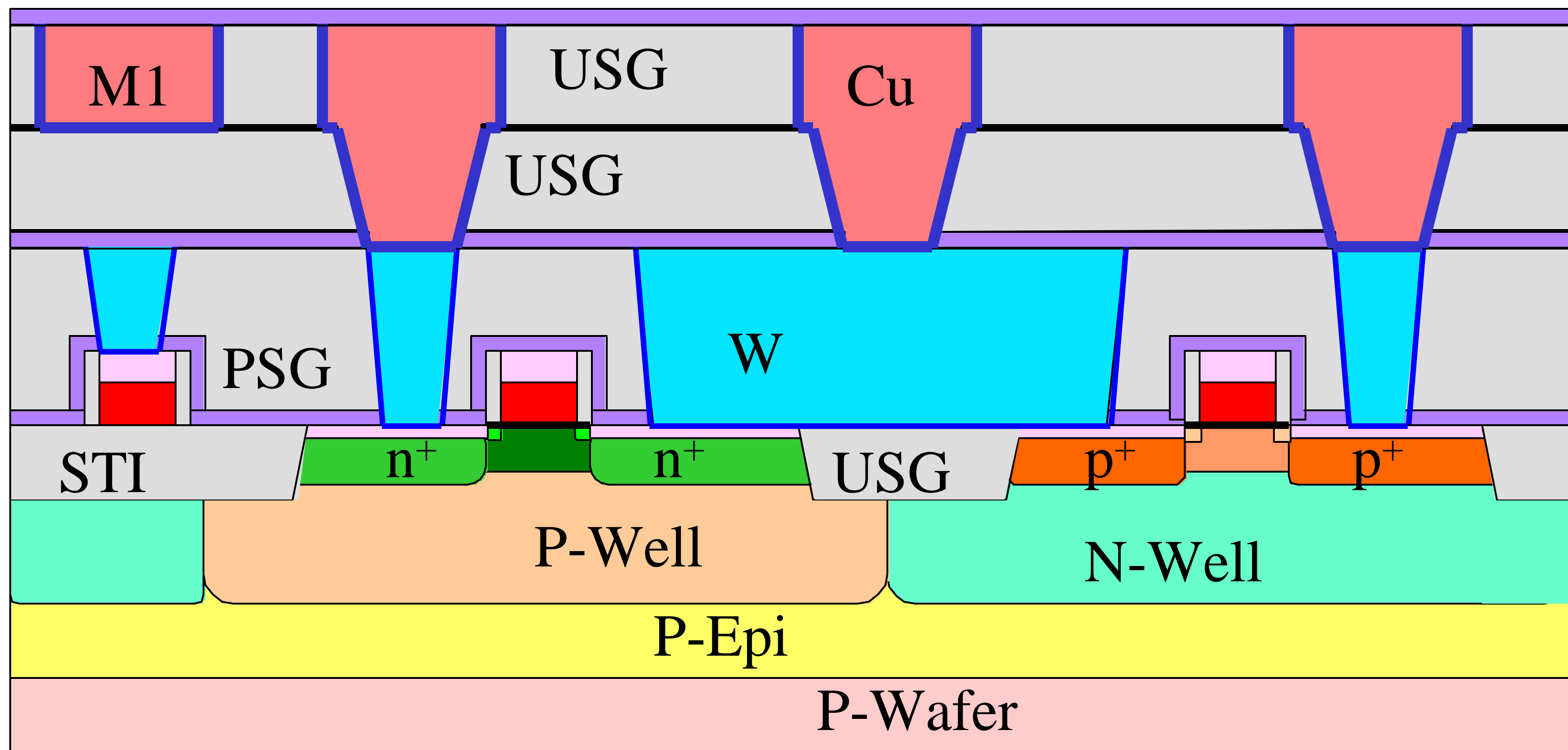
Trench Mask, Etch Trench, Strip PR



PVD Ta and Cu, ECP Bulk Cu, Anneal

Copper
USG
USG
PSG
W
STI
n^+
n^+
USG
p^+
p^+
P-Well
N-Well
P-Epi
P-Wafer

CMP Cu and Ta, PECVD Nitride



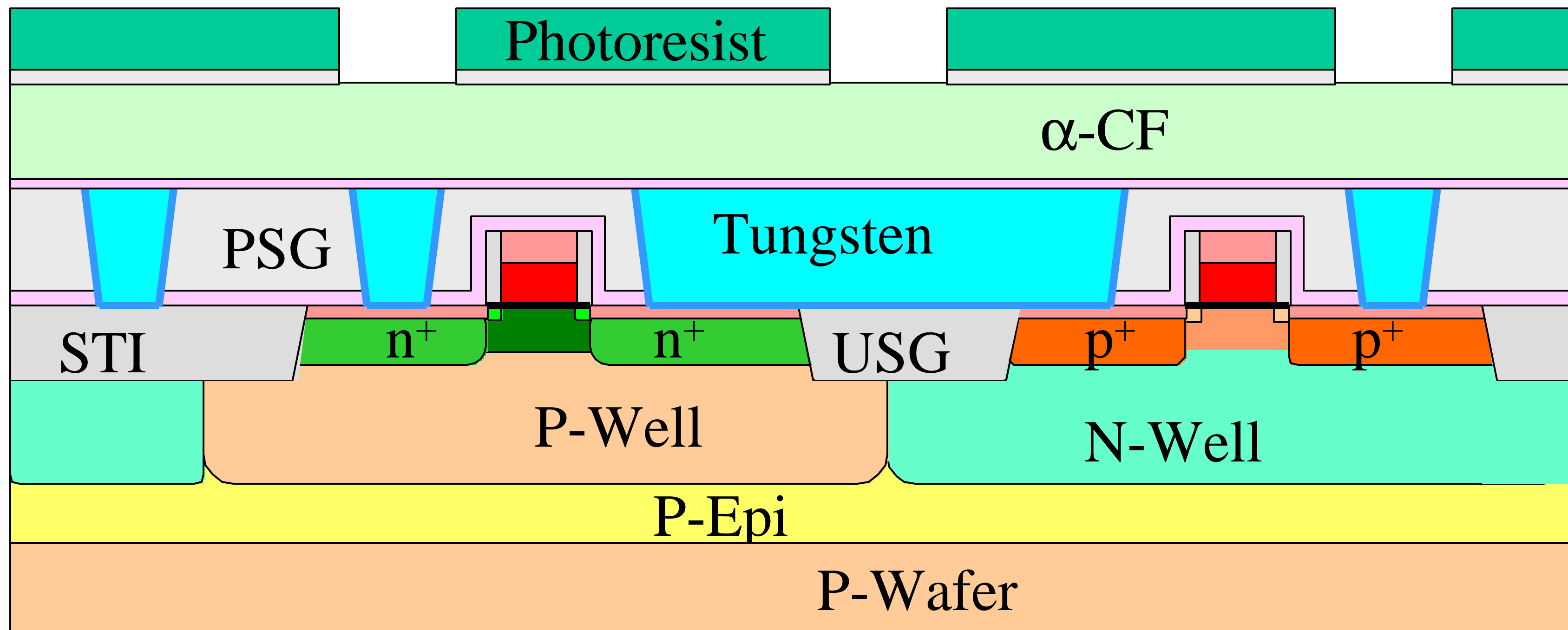
Copper Metallization

- Nitride seal layer prevent copper diffusion and oxidation
- Etch stop nitride separate via and trench etch
- Tantalum used as copper barrier layer
- PVD copper seed layer
- ECP bulk copper

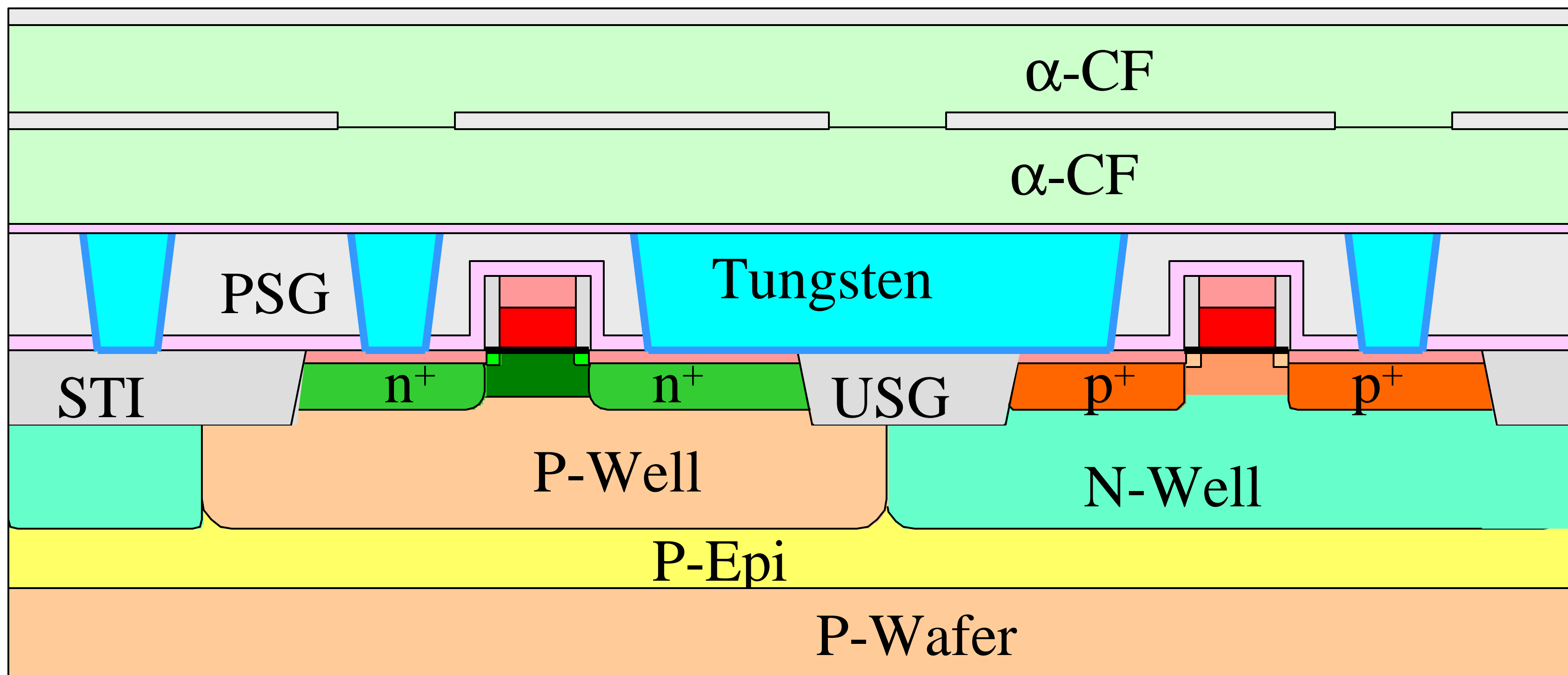
Copper and Low-κ

- Further increase IC chip speed
- low-κ dielectric still in R&D
- α-CF, κ = 2.5 to 2.7
- Can't be etched with fluorine chemistry
- It needs oxygen chemistry to etch
- New challenges for the process integration

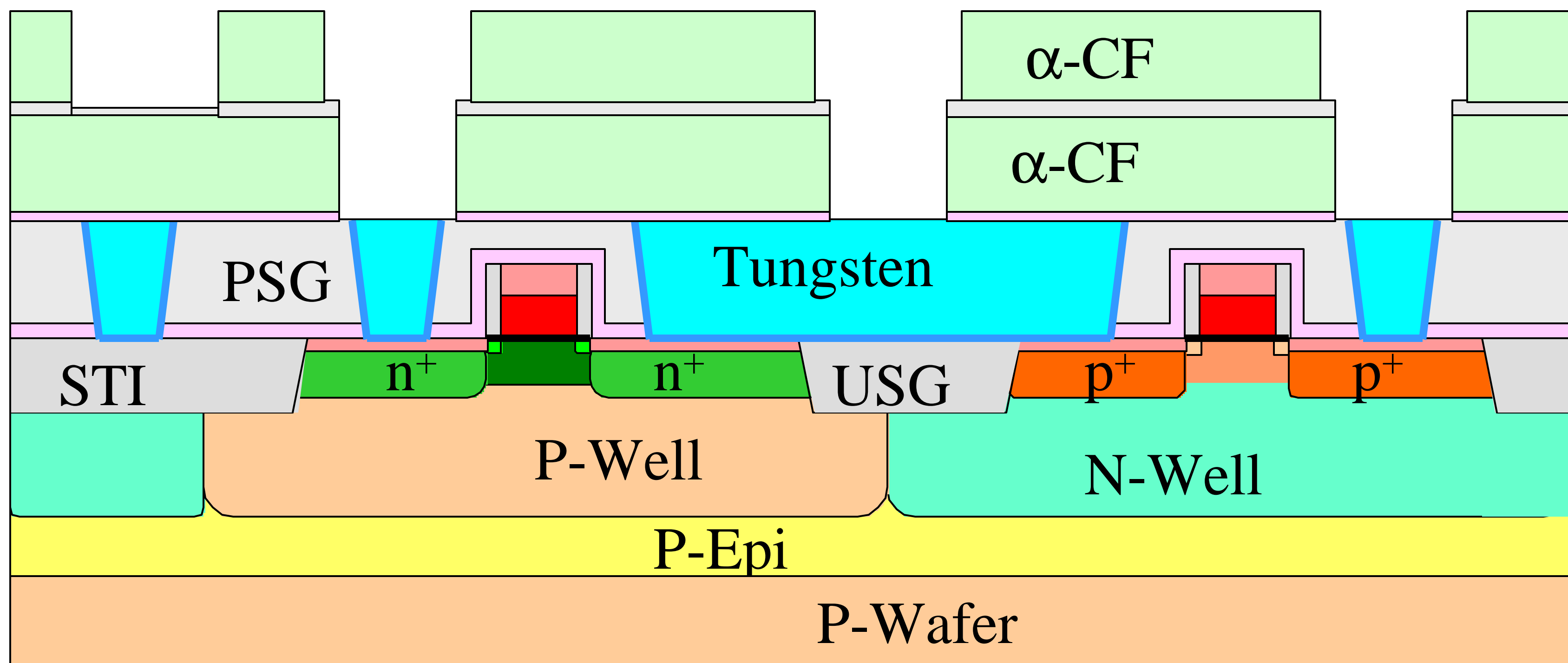
PECVD α-CF, USG, Via Mask, and Etch USG Hard Mask



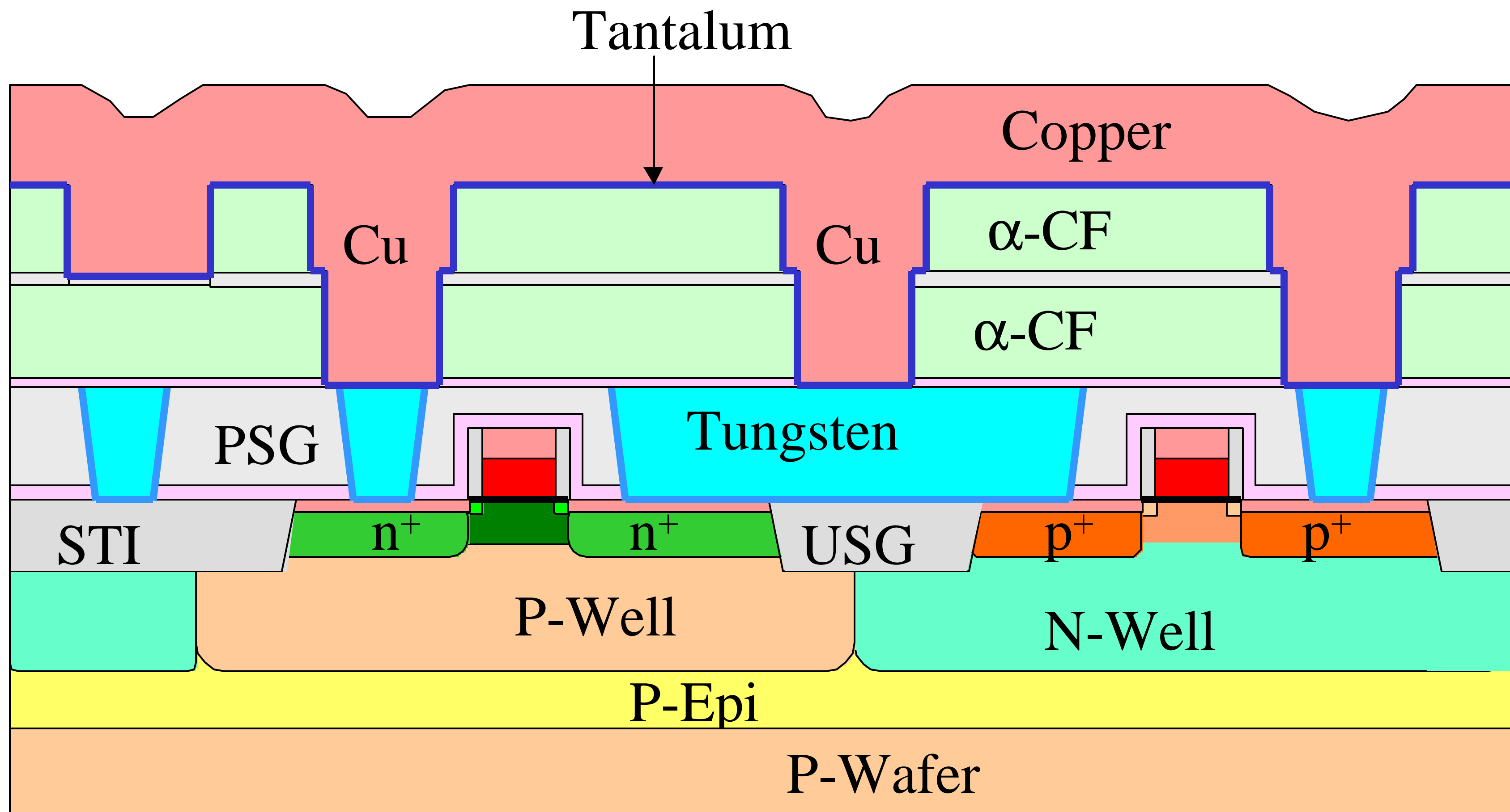
PECVD α-CF and USG



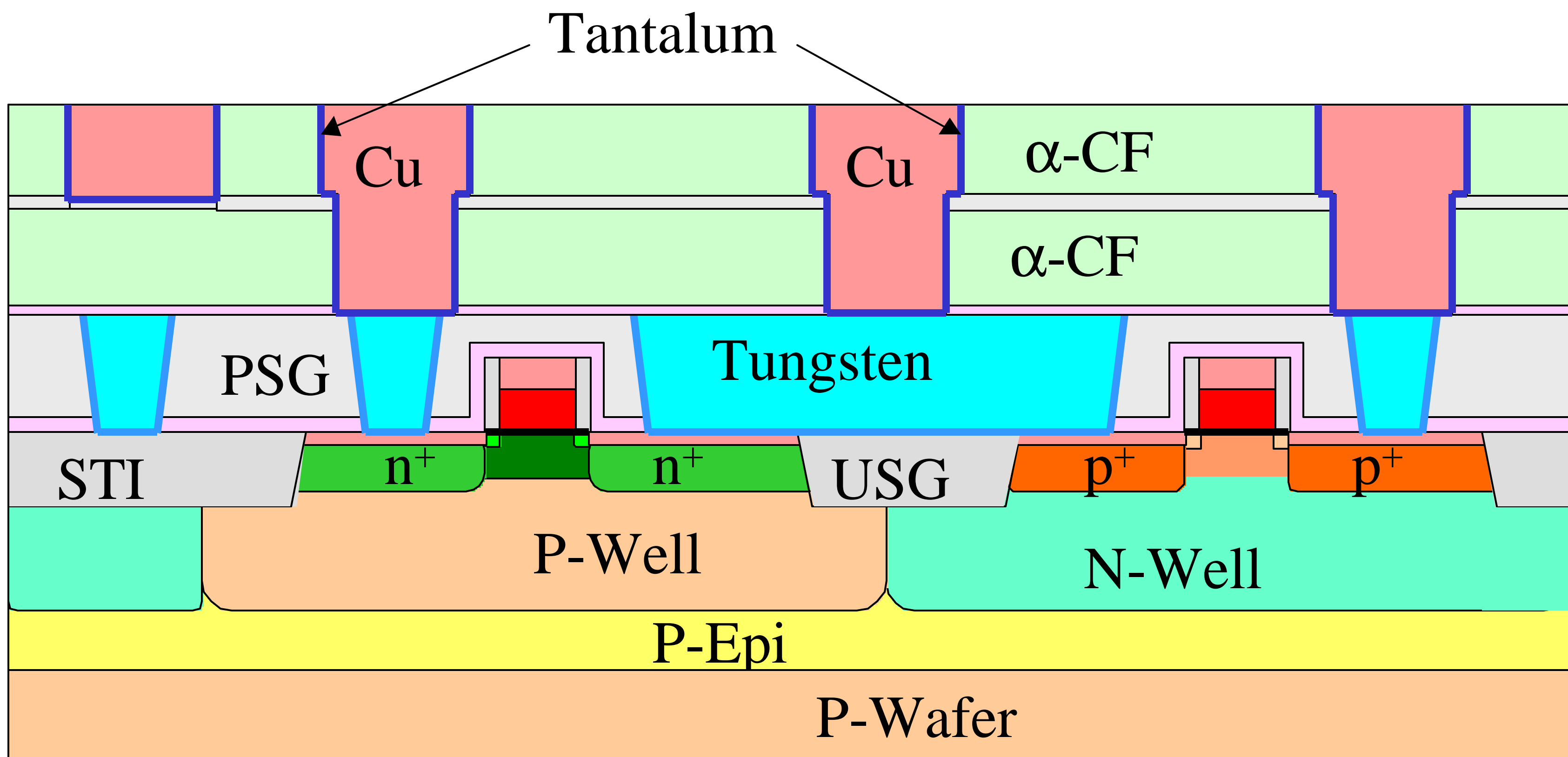
Etch α-CF and Seal Nitride



PVD Ta, Cu Seed, and ECP Cu



CMP Copper and Tantalum



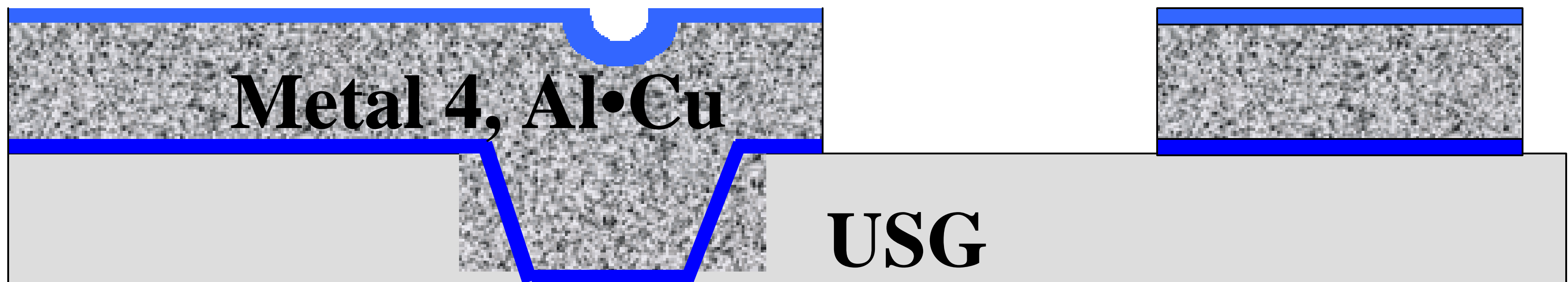
Copper and Low-κ

- Oxygen plasma is used to etch α-CF
- PR can't last long in oxygen plasma
- SiO_2 hard mask is needed
- Oxygen can't etch oxide and nitride
- Trench and via can be etched at the same time
  - High selectivity of α-CF to oxide and nitride
- PR is removed when oxygen plasma etch α-CF

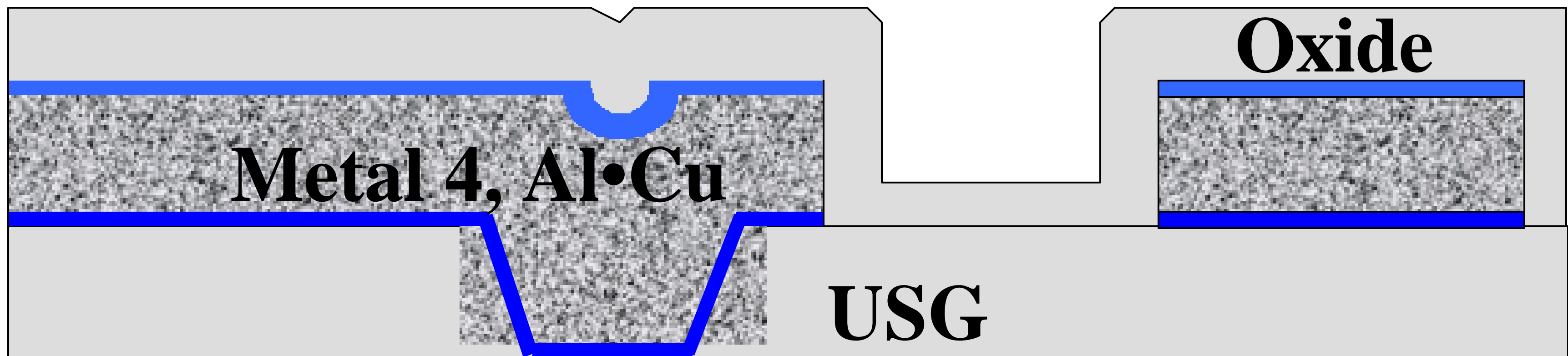
Passivation

- Protect IC chip from moisture and other contaminants such as sodium
- Silicon nitride is the most commonly used
- Usually oxide layer is used as a stress buffer
- SiH_4 based PECVD for both oxide and nitride
- Bonding pad mask or connecting bump mask
- Fluorine based nitride/oxide etch
- Strip PR to finish wafer processing

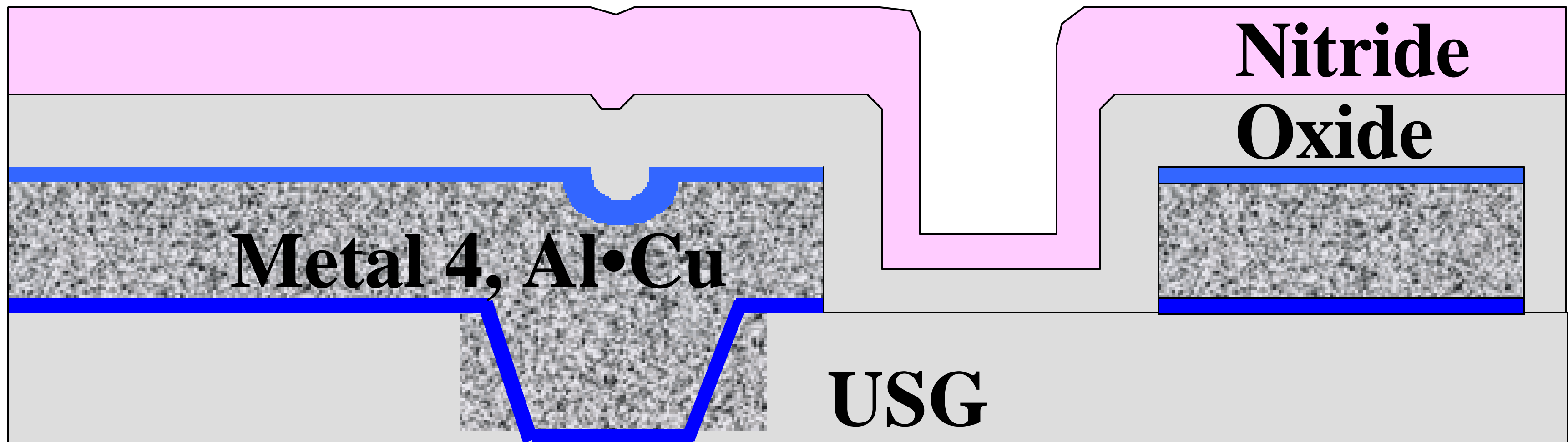
Metal Anneal



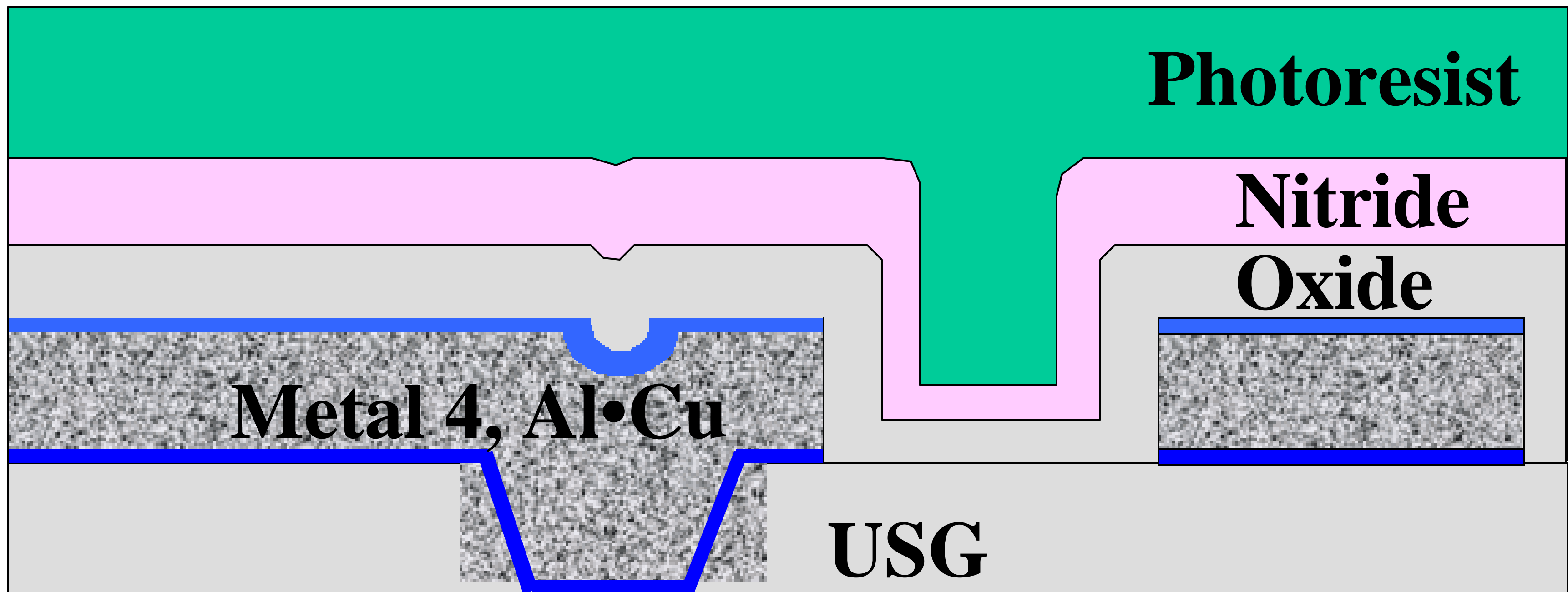
PECVD Oxide



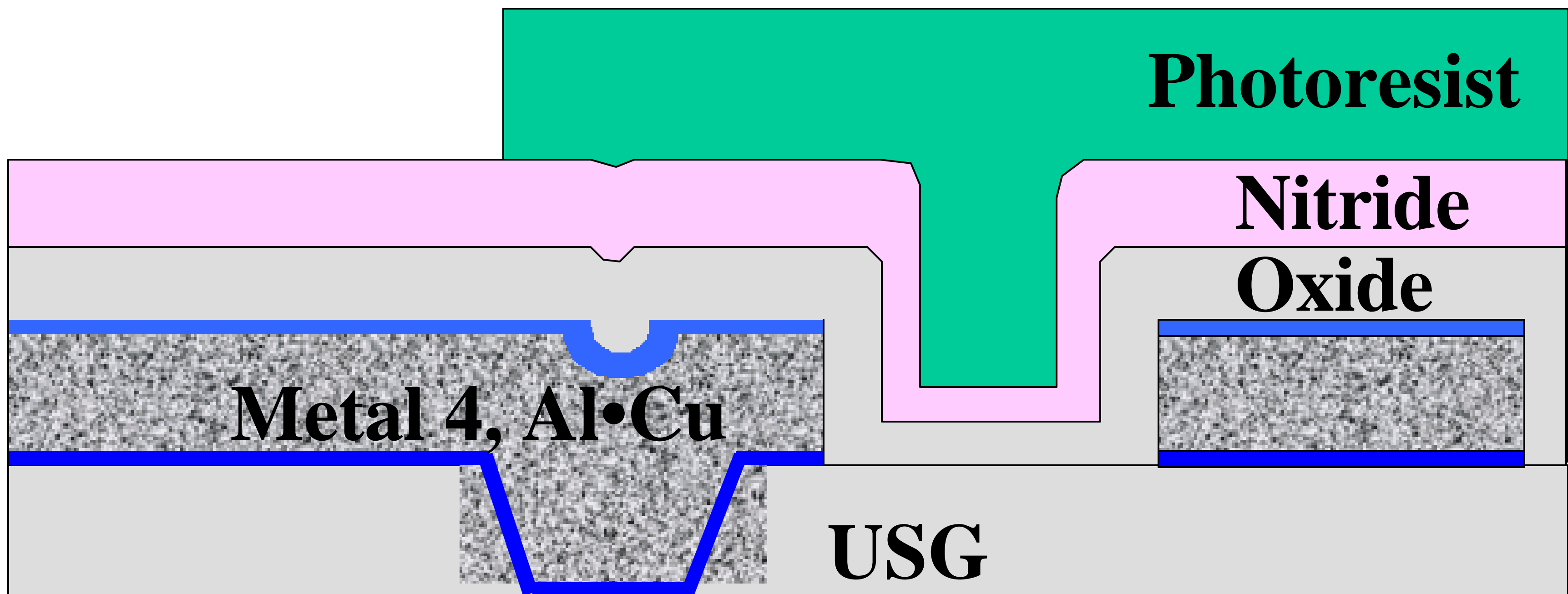
PECVD Nitride



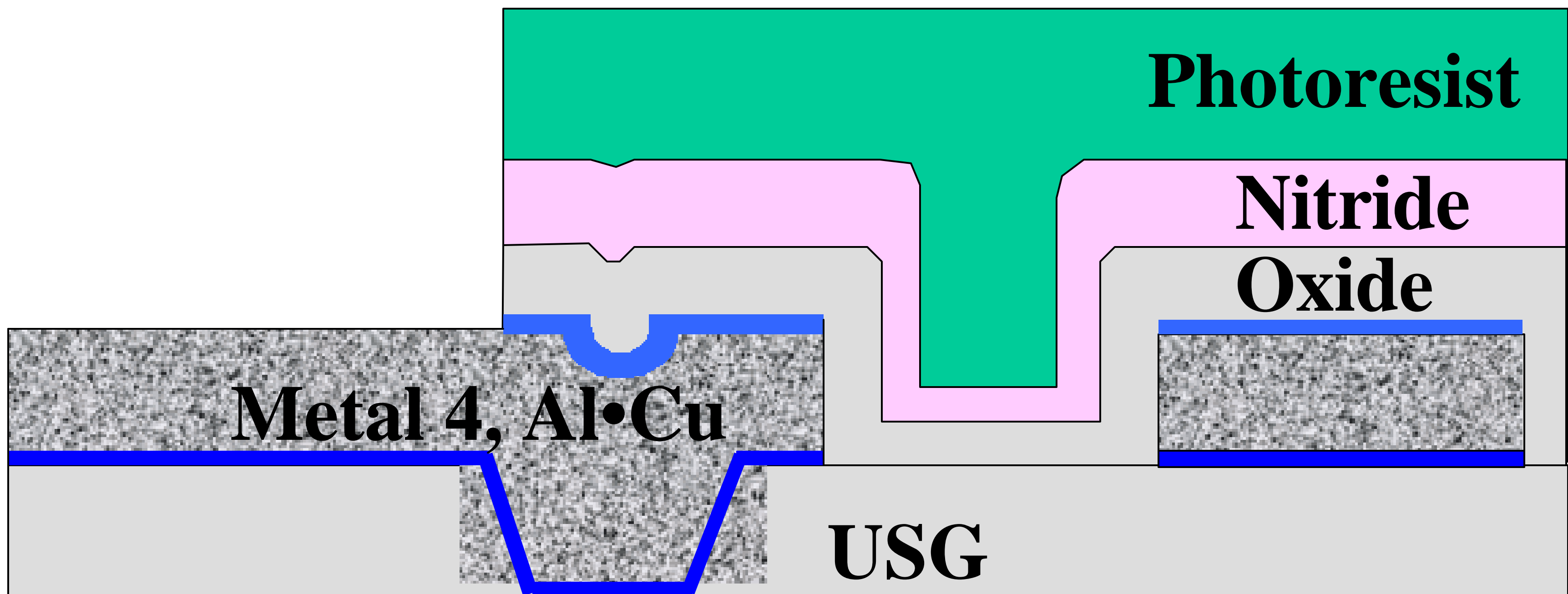
Photoresist Coating



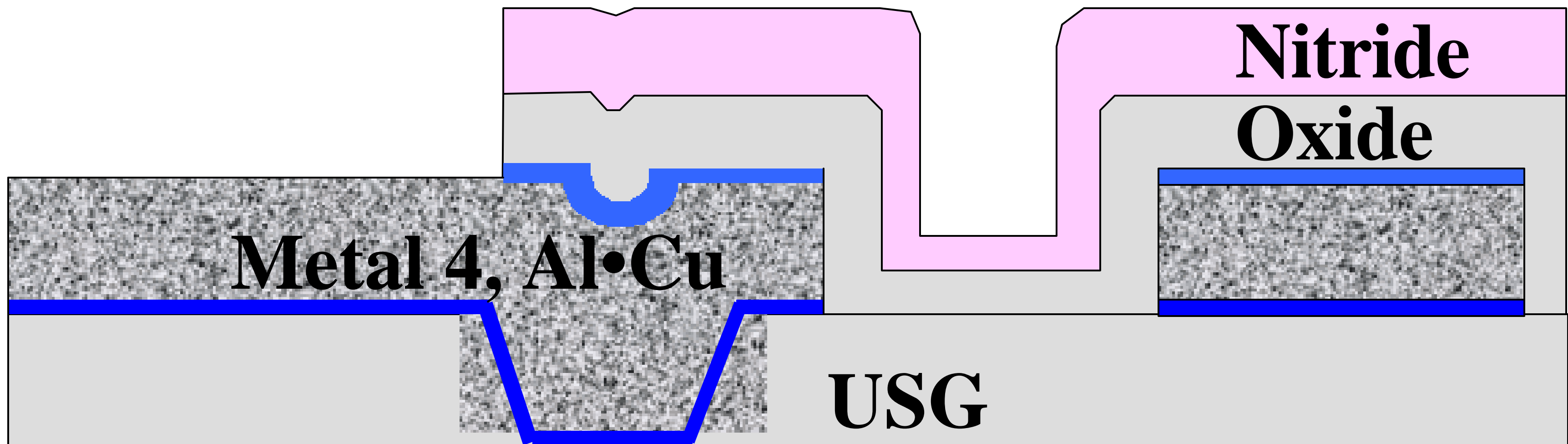
Bonding Pad Mask Exposure and Development



Etch Nitride and Oxide



Strip Photoresist



Summary

- Well formation process
- Isolations: field oxide, LOCOS, and STI
- Sidewall spacer for LDD and salicide
- Al, poly-Si and silicide for gate and local interconnections
- W, Ti and Al alloy are commonly used in traditional interconnection process.

Summary

- Basic process steps for copper metallization are dielectric deposition, dielectric etches, metal deposition, and metal polishing
- Silicon nitride is the most commonly used passivation materials in IC processing

Chapter 14
CMOS Processes

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Objectives

- List the major process technology changes from the 1980 to the 1990s
- Explain the differences between copper metallization and traditional metallization

From 1960s to 1970s

- 1960s
  - PMOS
  - Diffusion
  - Metal gate
- 1970s
  - NMOS
  - Ion implantation
  - Polysilicon gate

1980's Technology

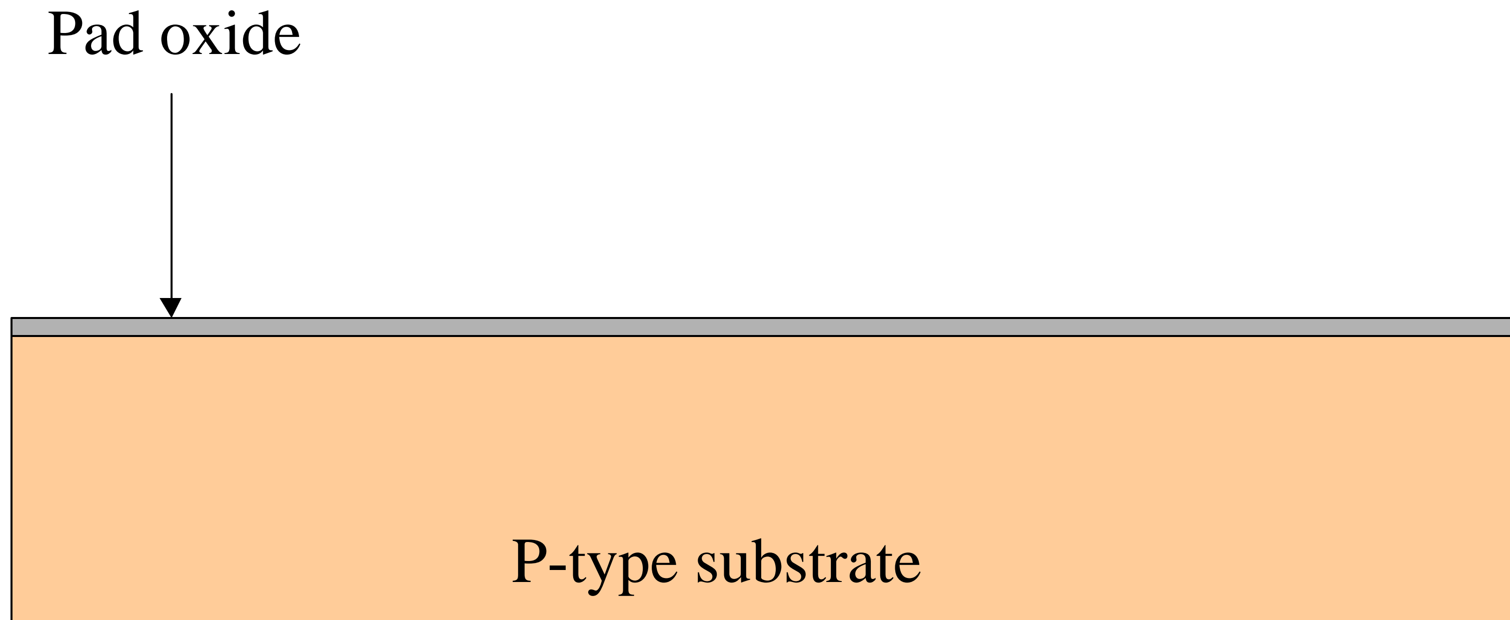
- LCD replacing LED as indicators for electronic watches and calculators
- CMOS IC replacing NMOS IC for lower power consumption
- Minimum feature size: from 3 μm to 0.8 μm
- Wafer size: 100 mm (4 in) to 150 mm (6 in)

1980's CMOS Technology

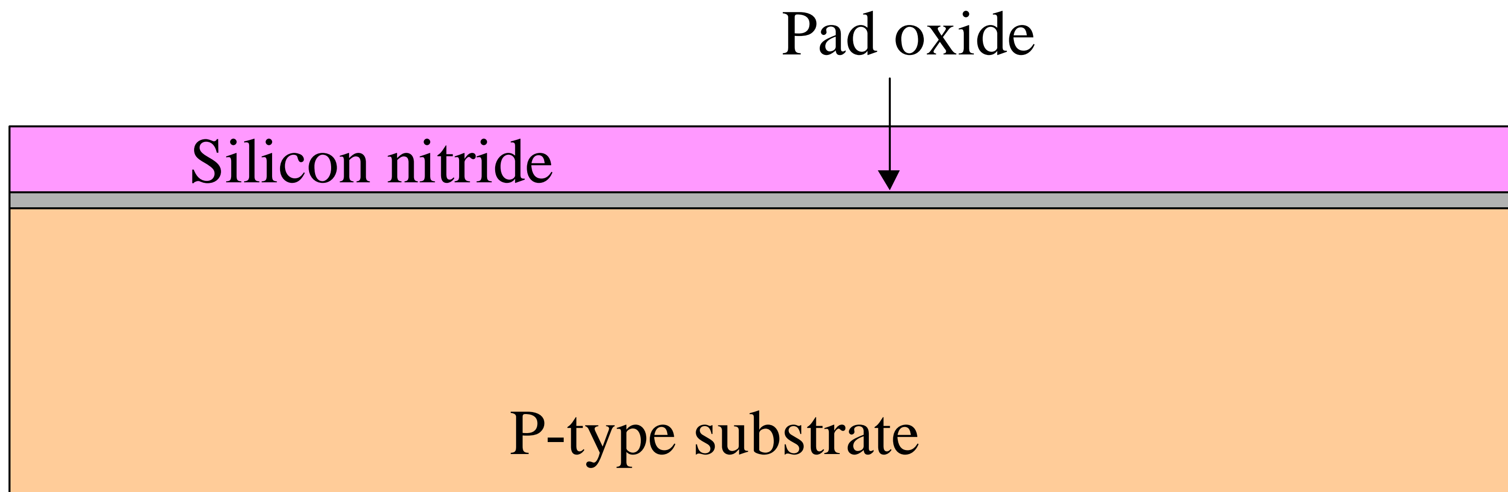
- LOCOS
- PSG and reflow
- Evaporator for metal deposition
- Positive photoresist
- Projection printer
- Plasma etch and wet etch

1980's Technology, Wafer Clean

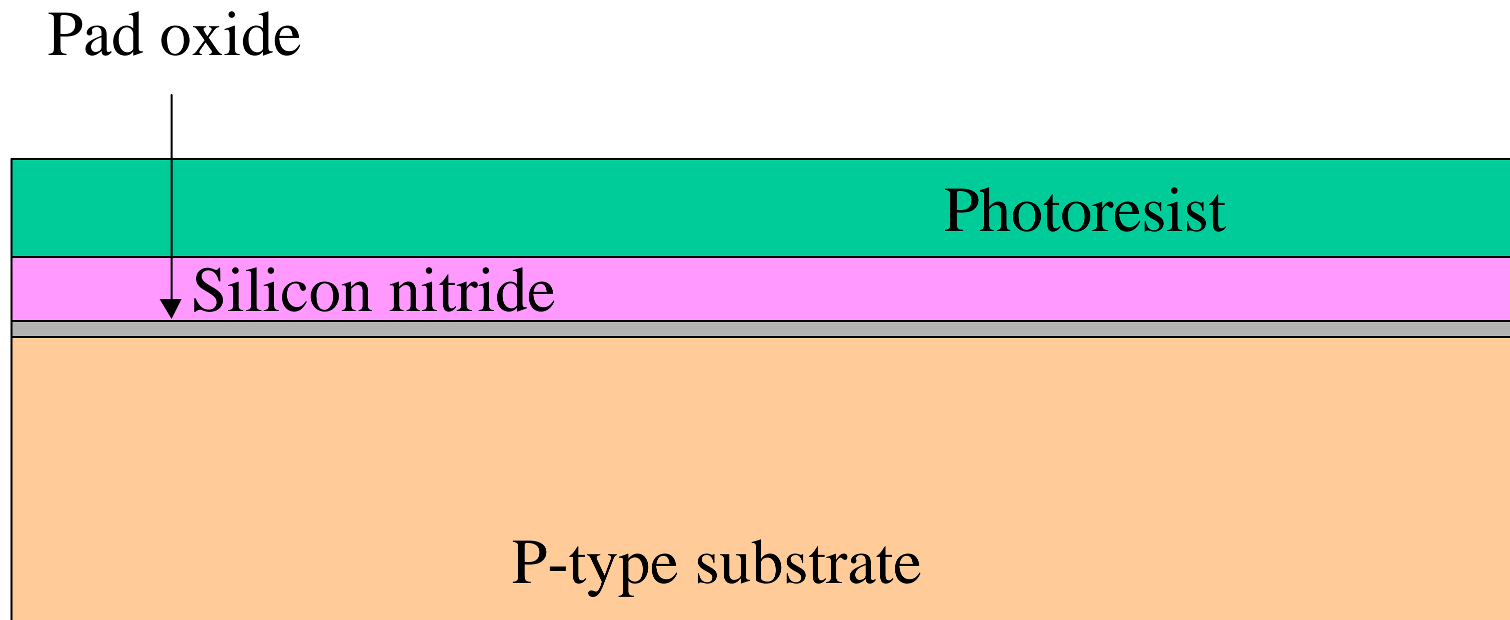
Pad Oxidation



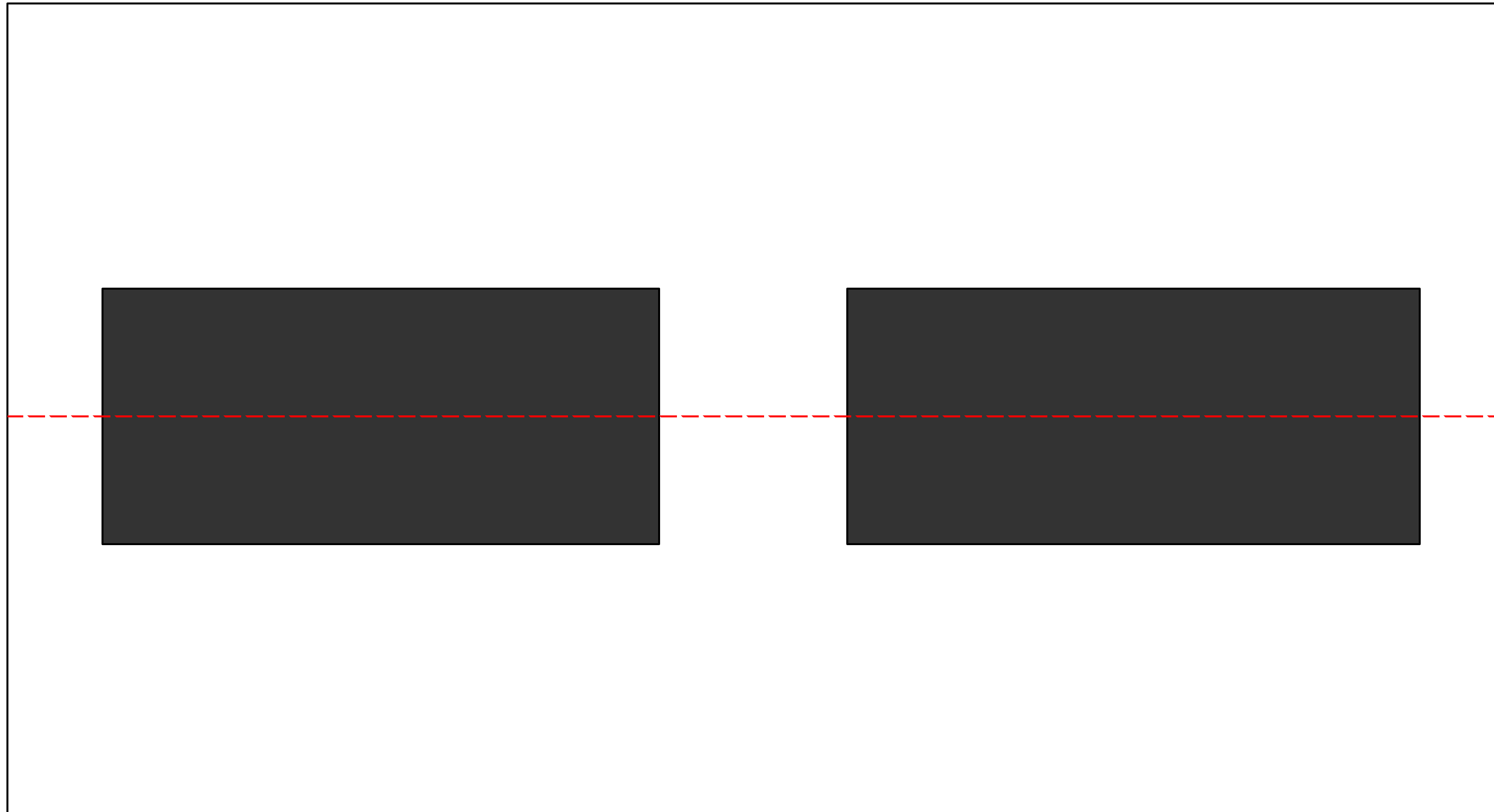
LPCVD Nitride



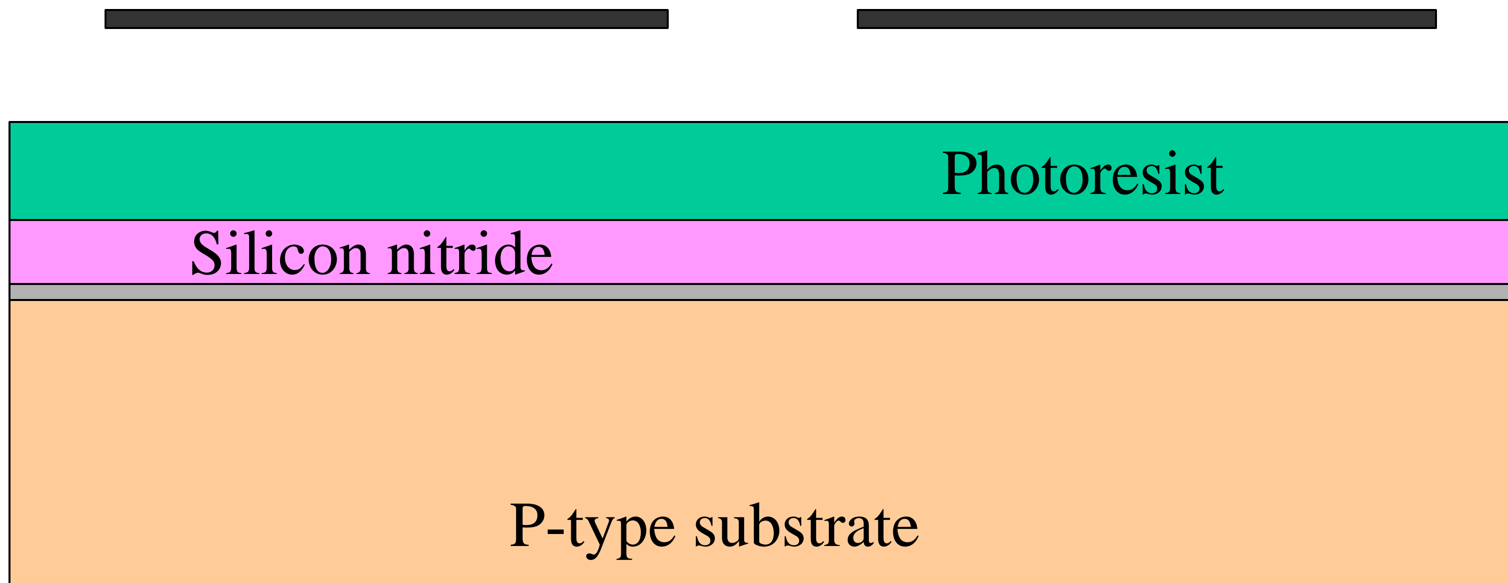
Photoresist Coating



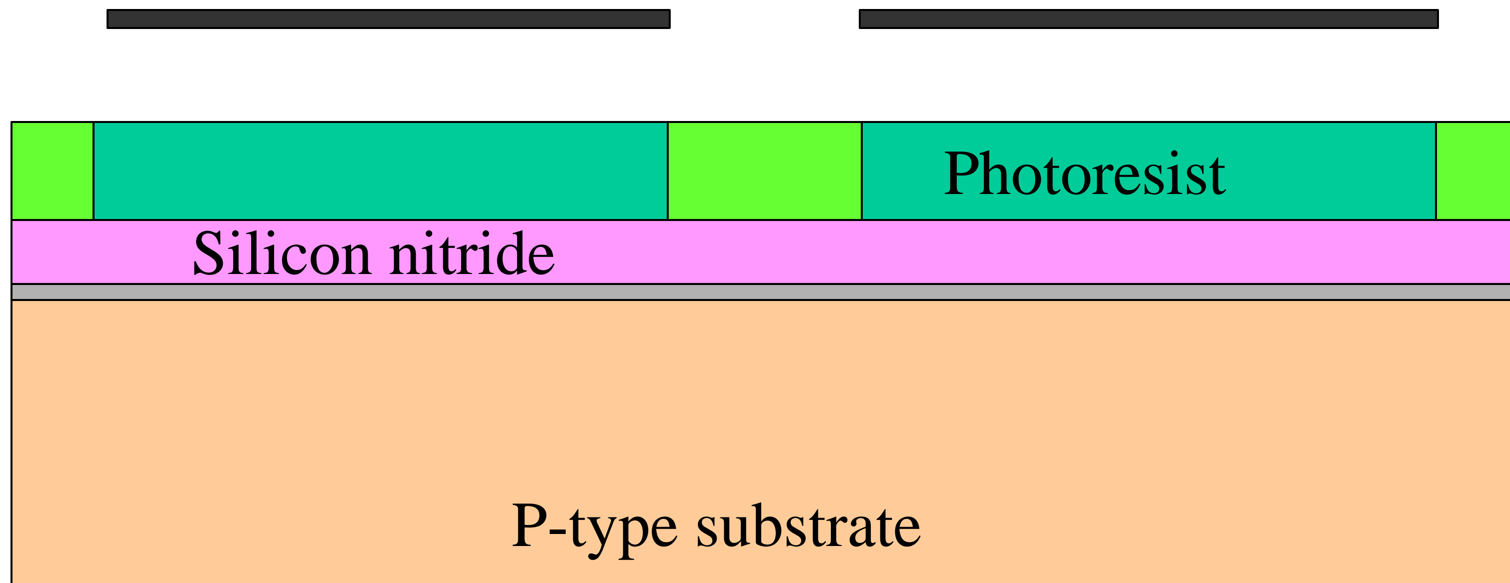
Mask 1, LOCOS



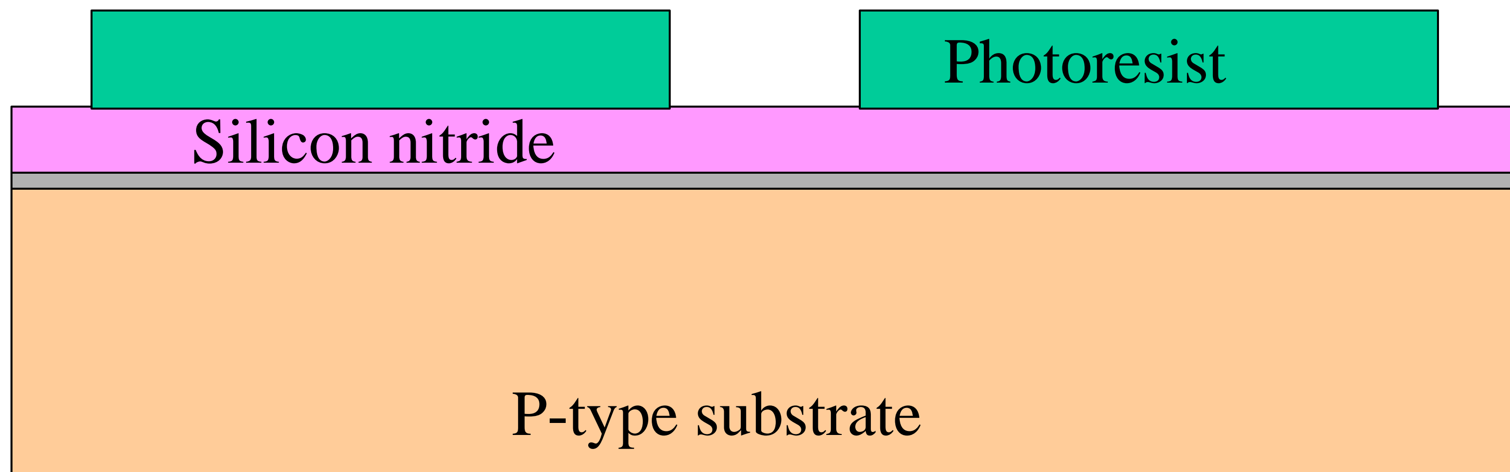
Mask 1, LOCOS



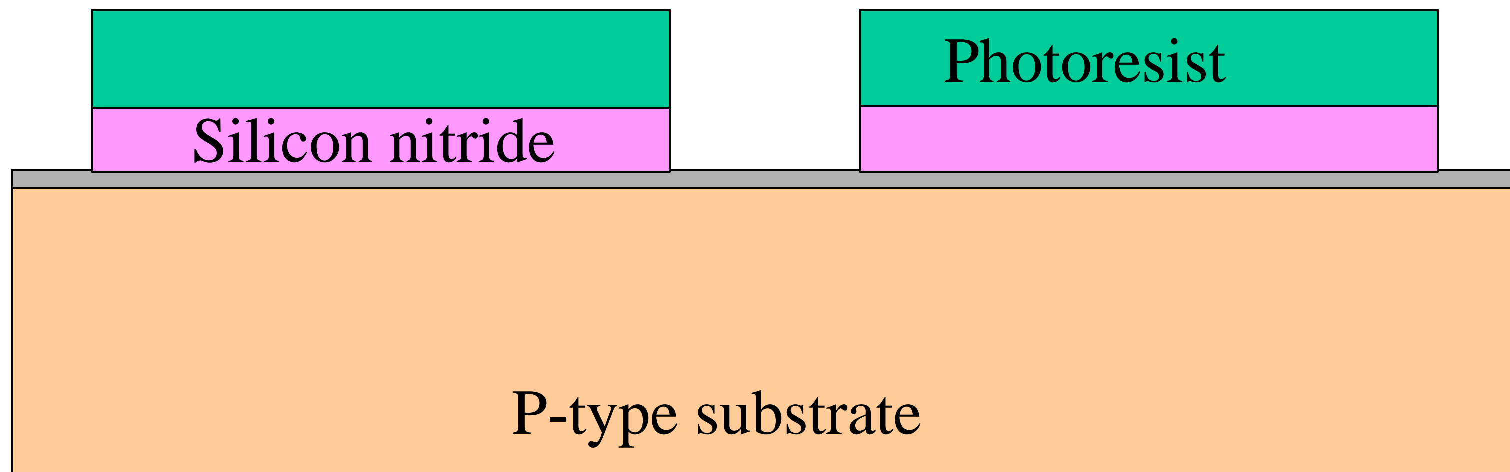
Alignment and Exposure



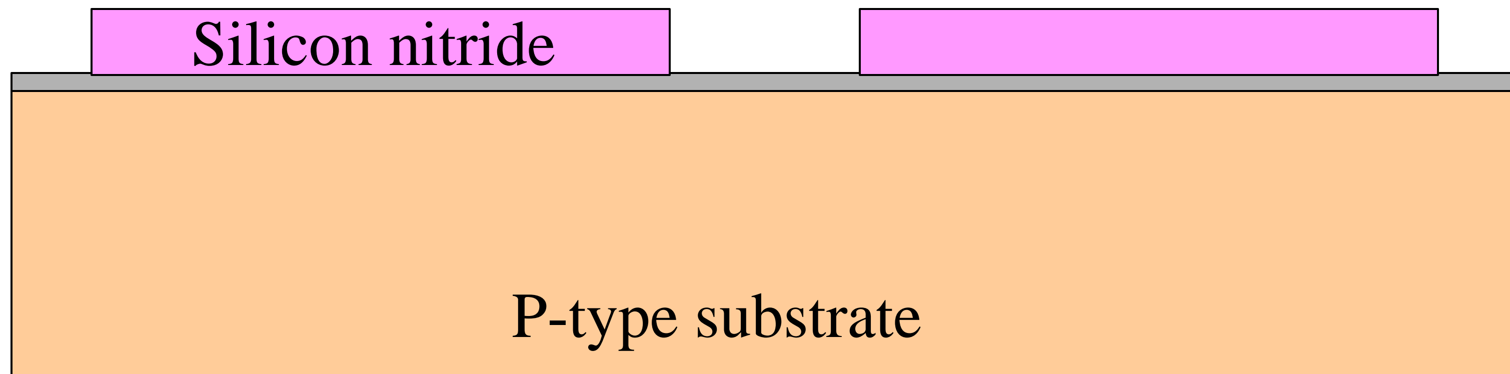
Development



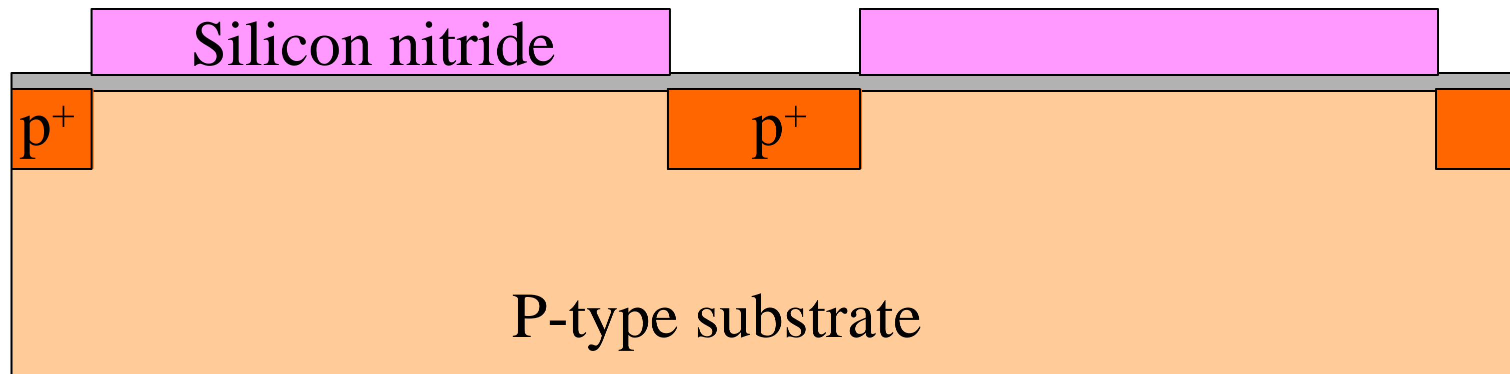
Etch Nitride



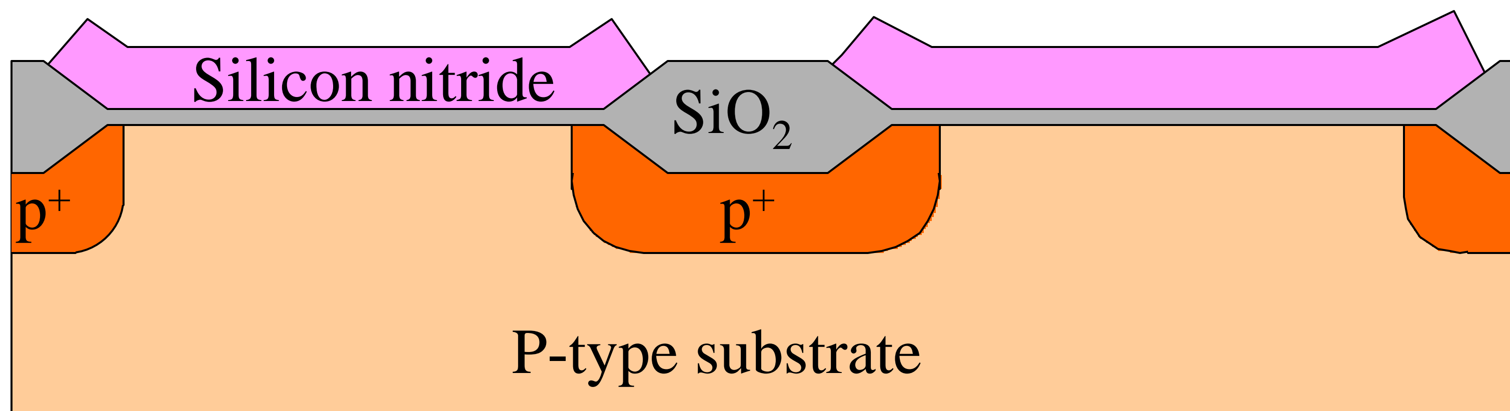
Strip Photoresist



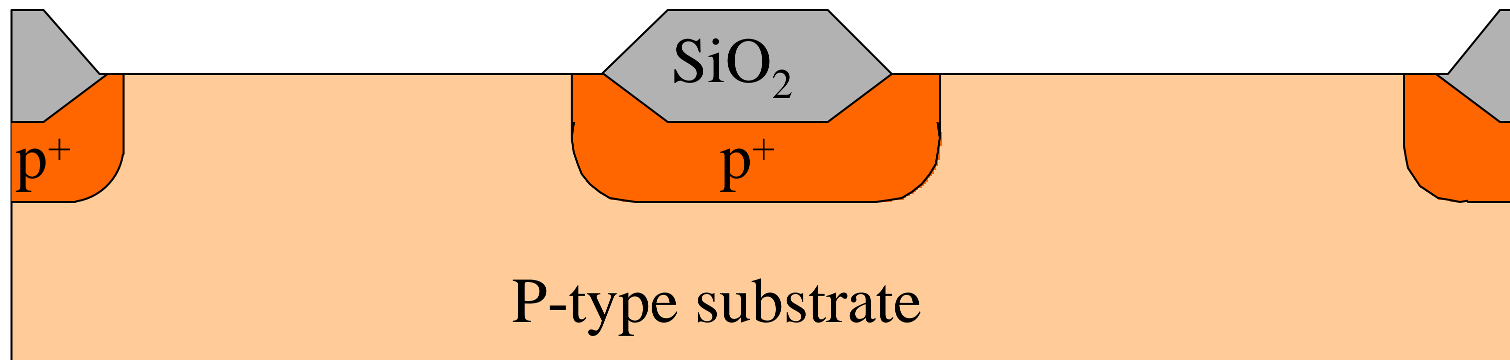
Isolation Implantation



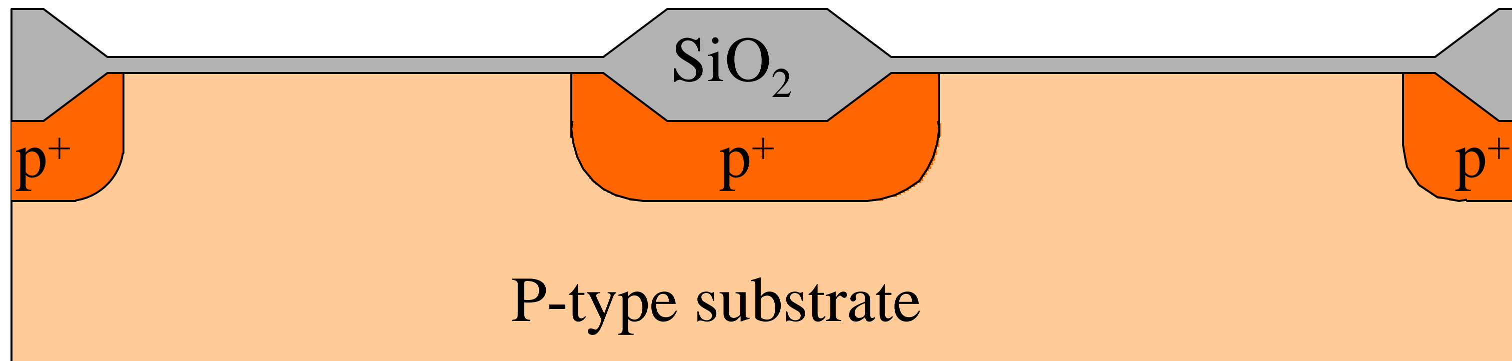
LOCOS Oxidation



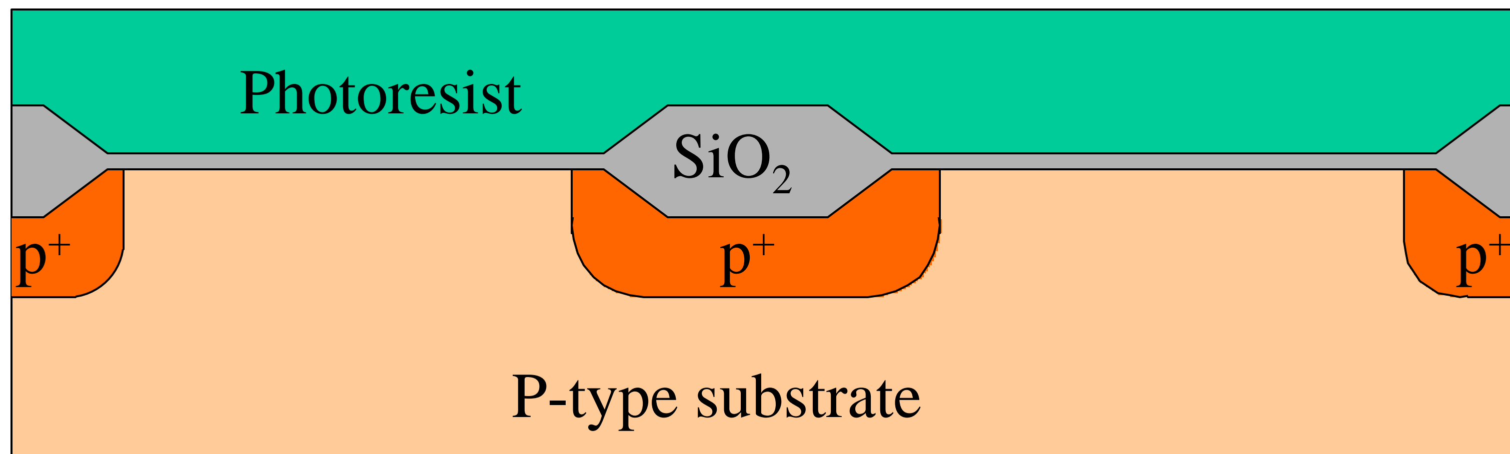
Strip Nitride and Pad Oxide, Clean



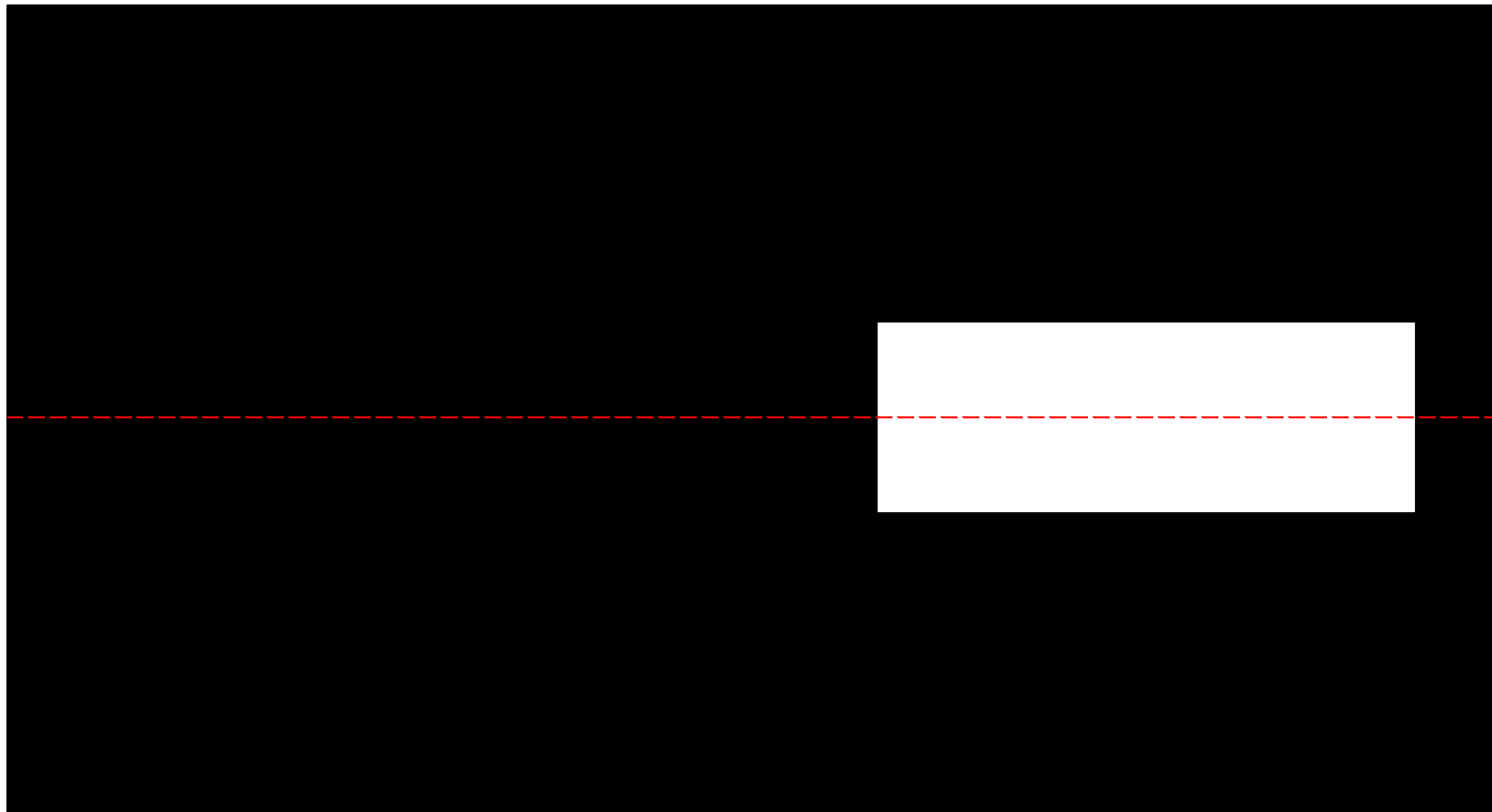
Screen Oxidation



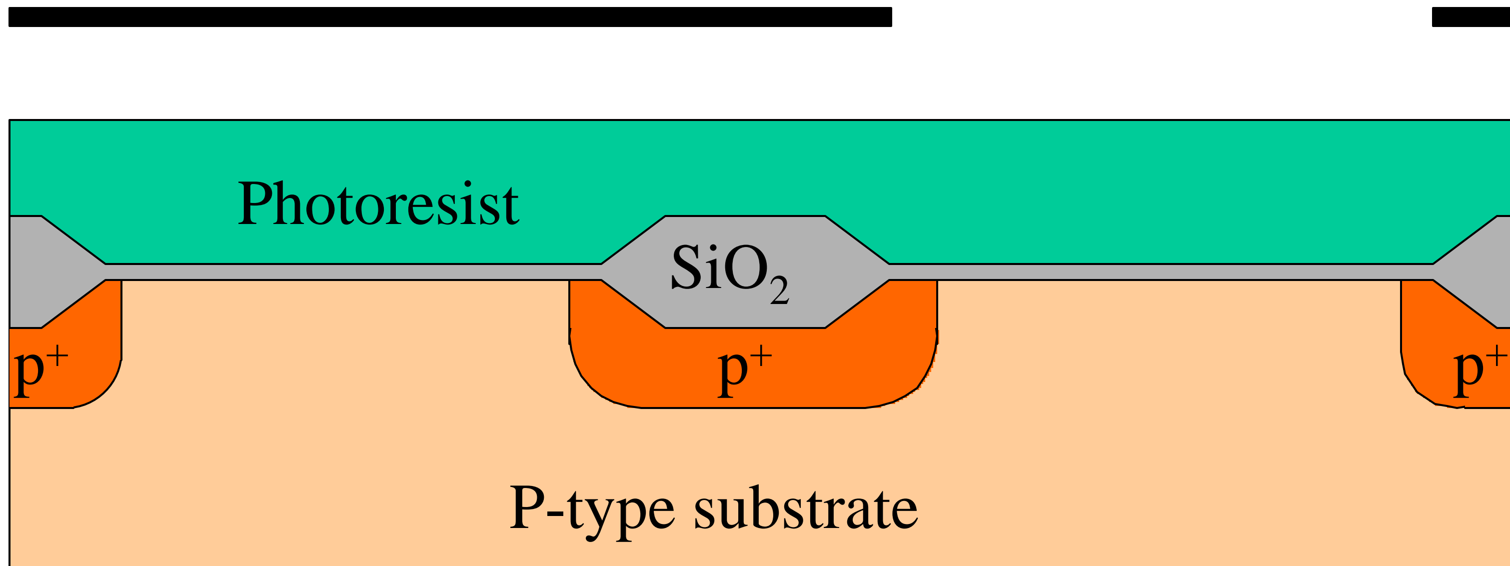
Photoresist Coating



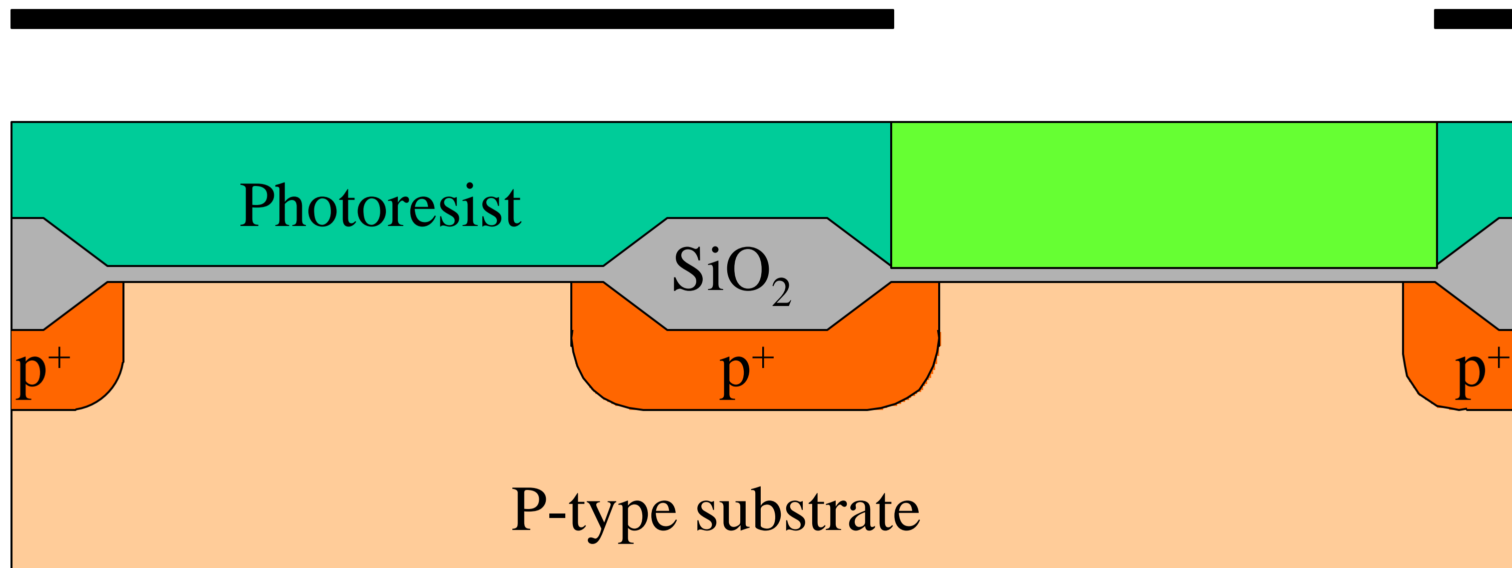
Mask 2, N-well



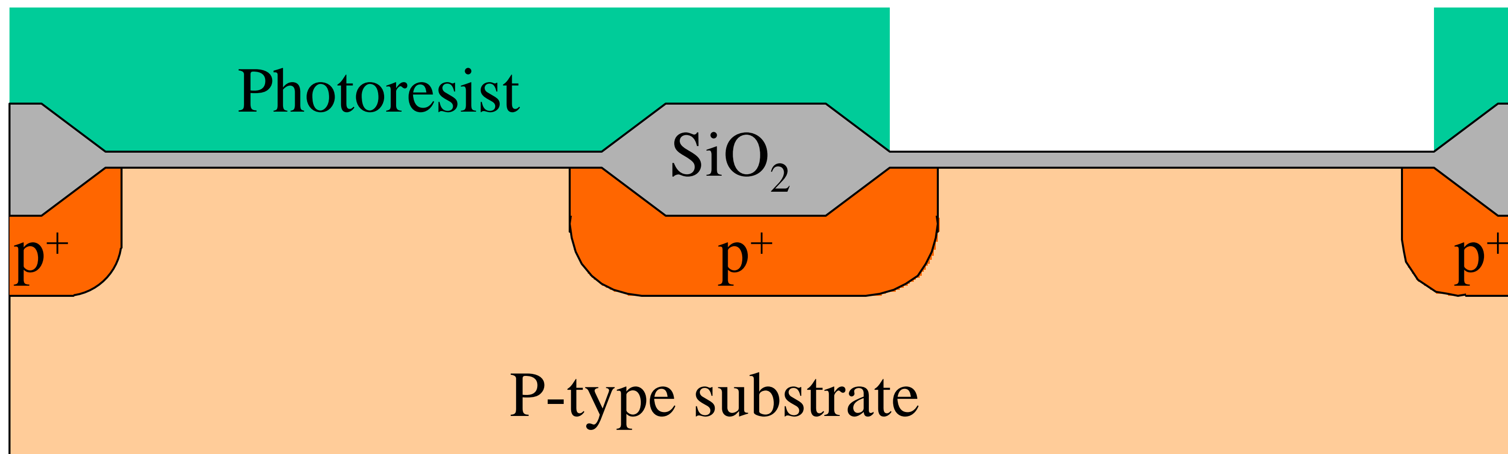
Mask 2, N-well



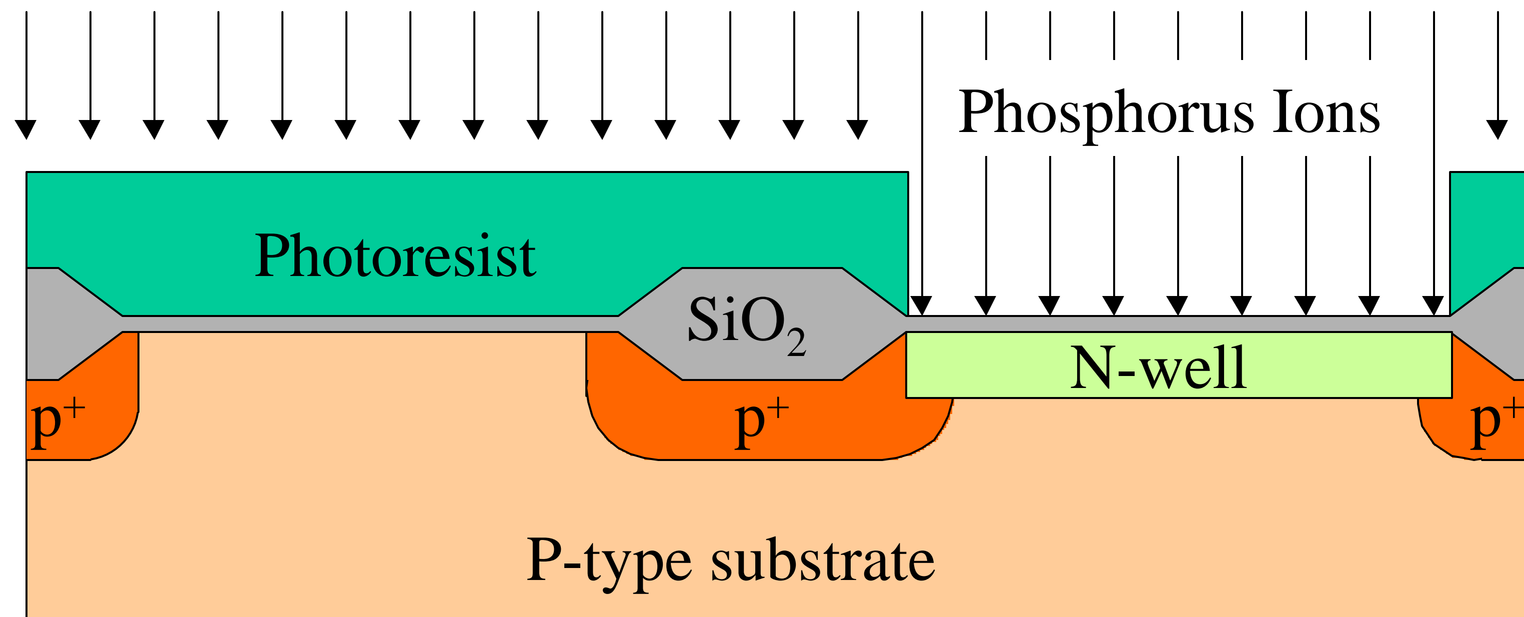
Exposure



Development



N-well Implantation



Strip Photoresist

SiO$_2$

N-well

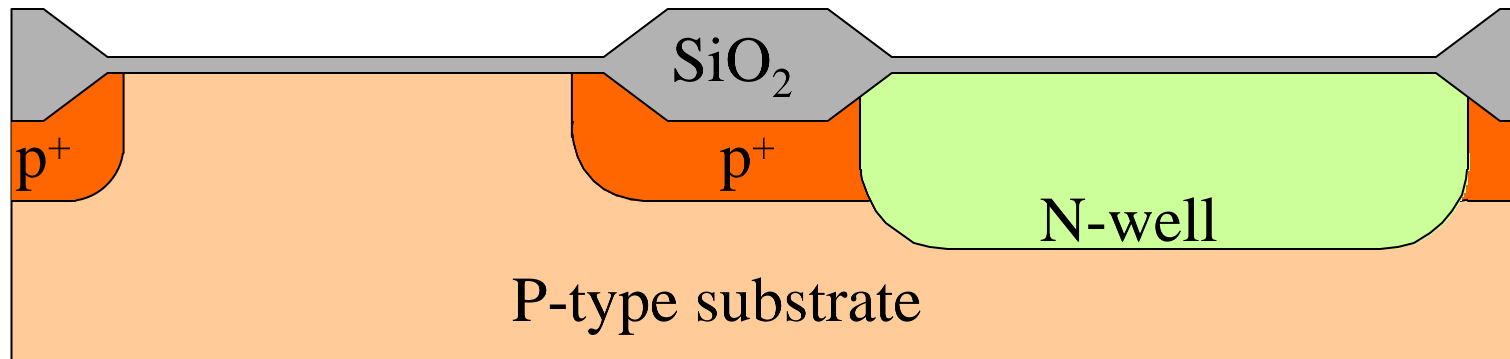
p$^+$

p$^+$

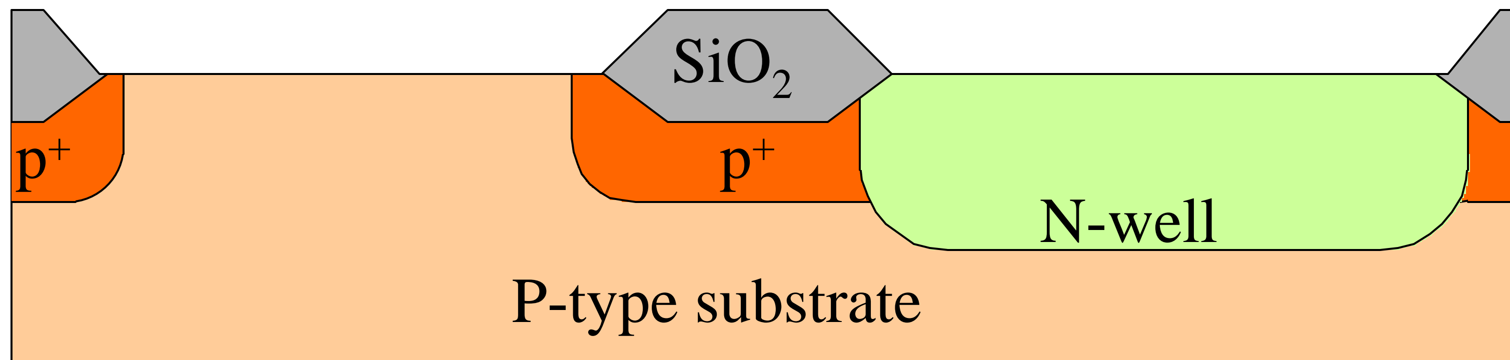
p$^+$

P-type substrate

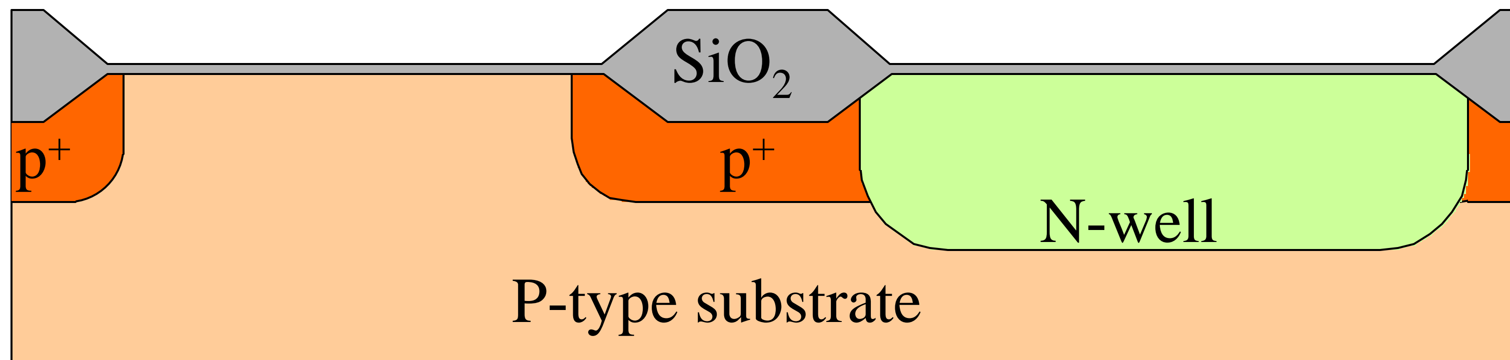
N-well Drive-in



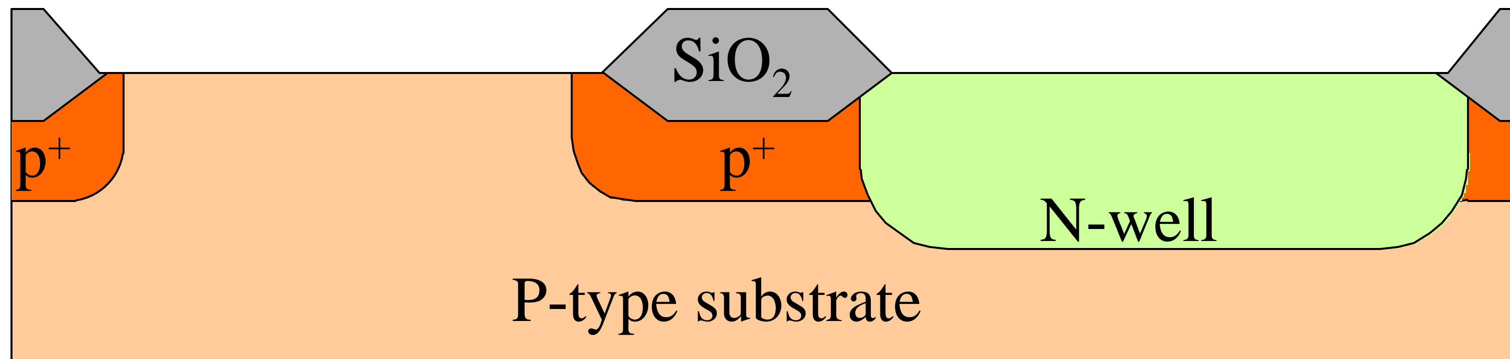
Strip Screen Oxide



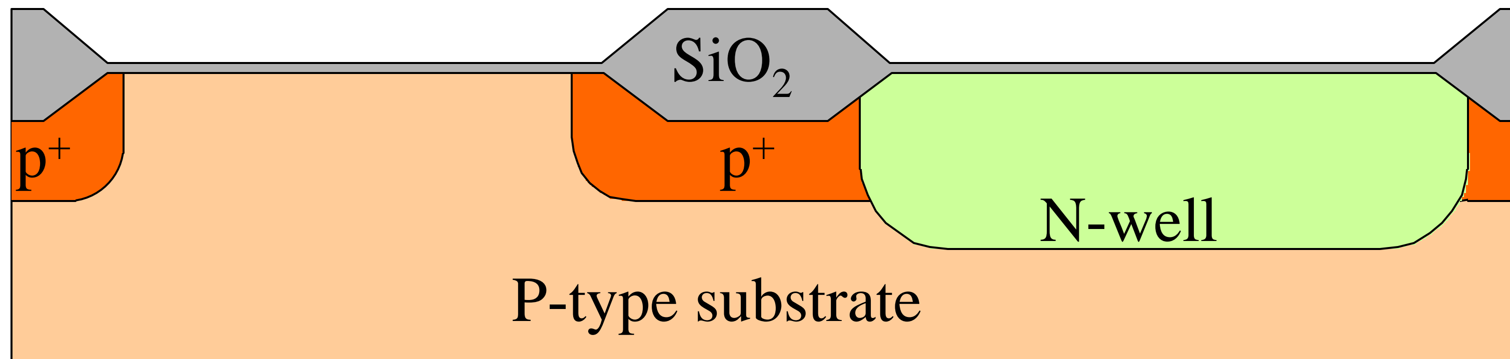
Grow Sacrificial Oxide



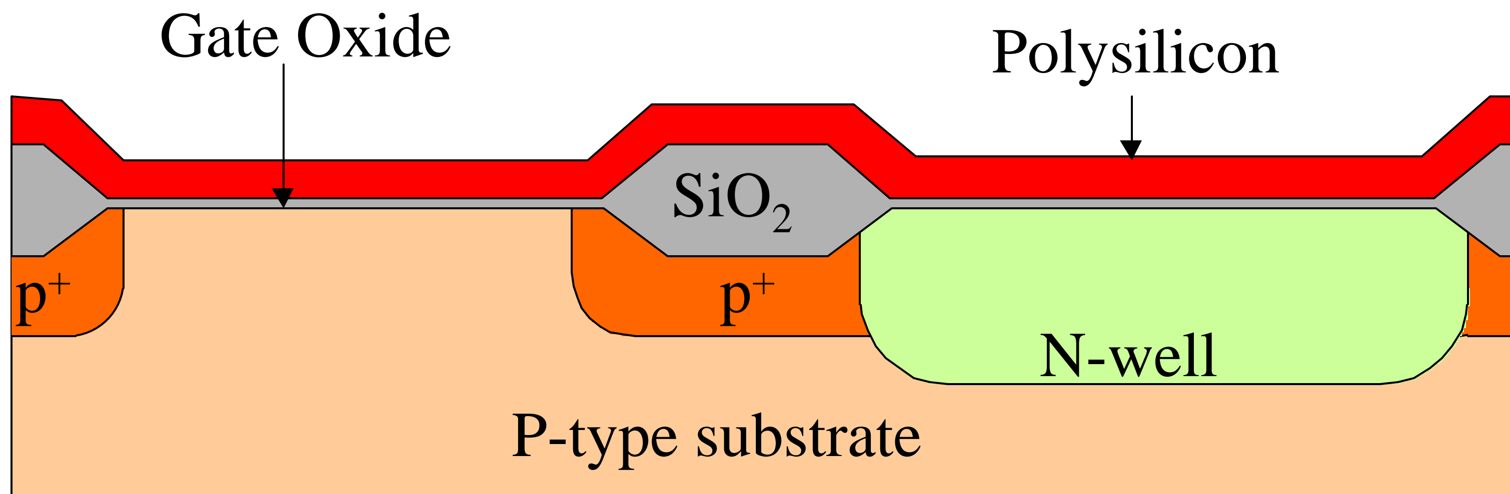
Strip Sacrificial Oxide



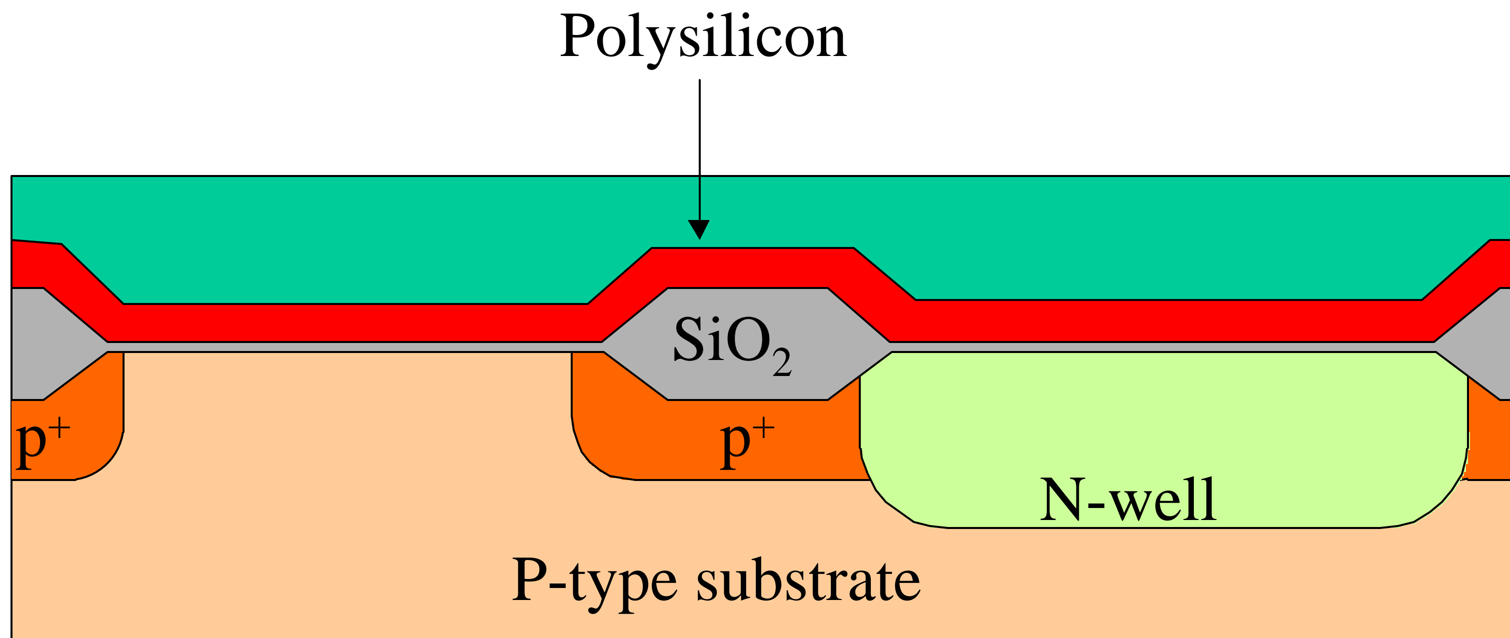
Grow Gate Oxide



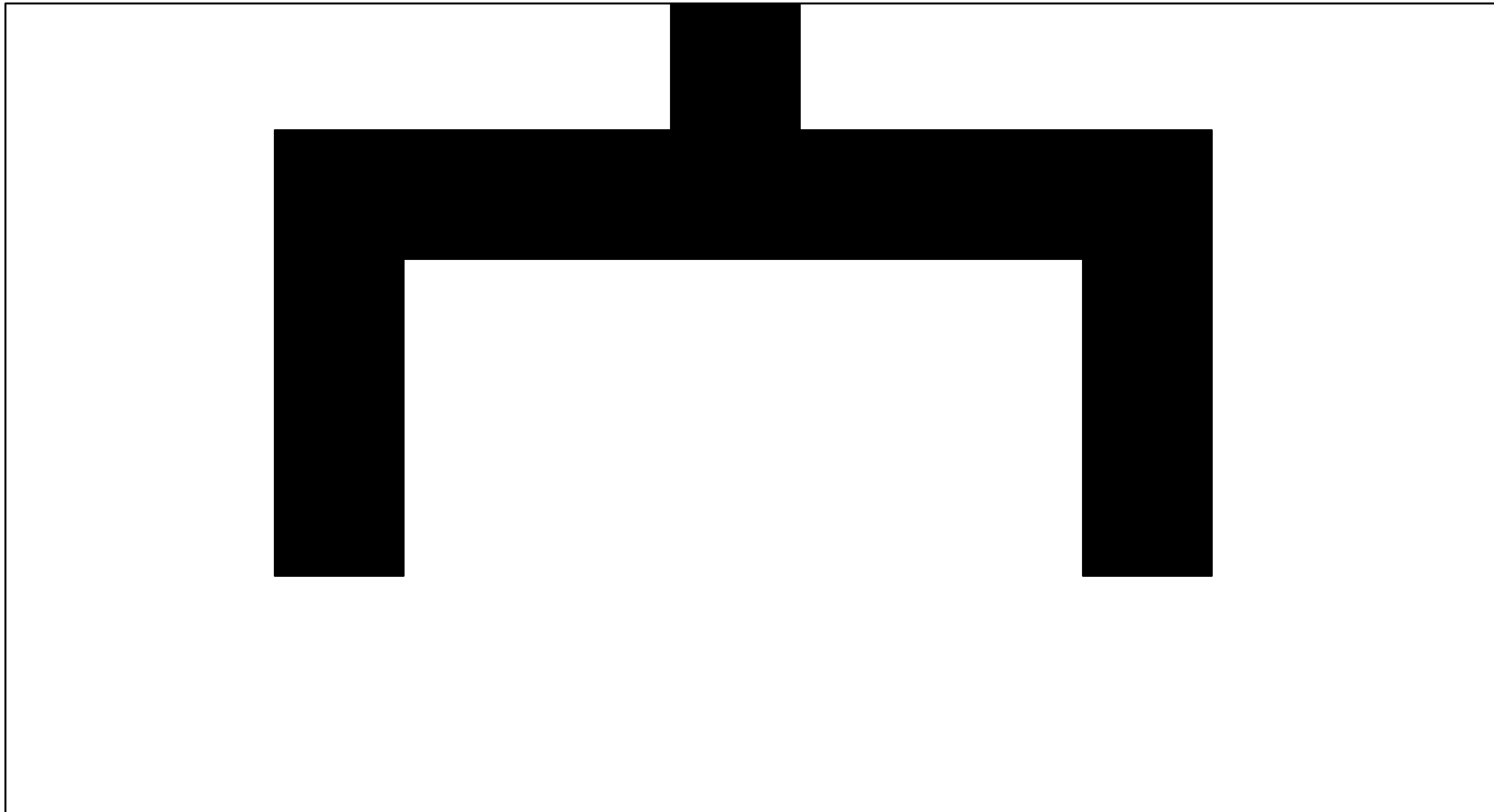
Deposit Polysilicon



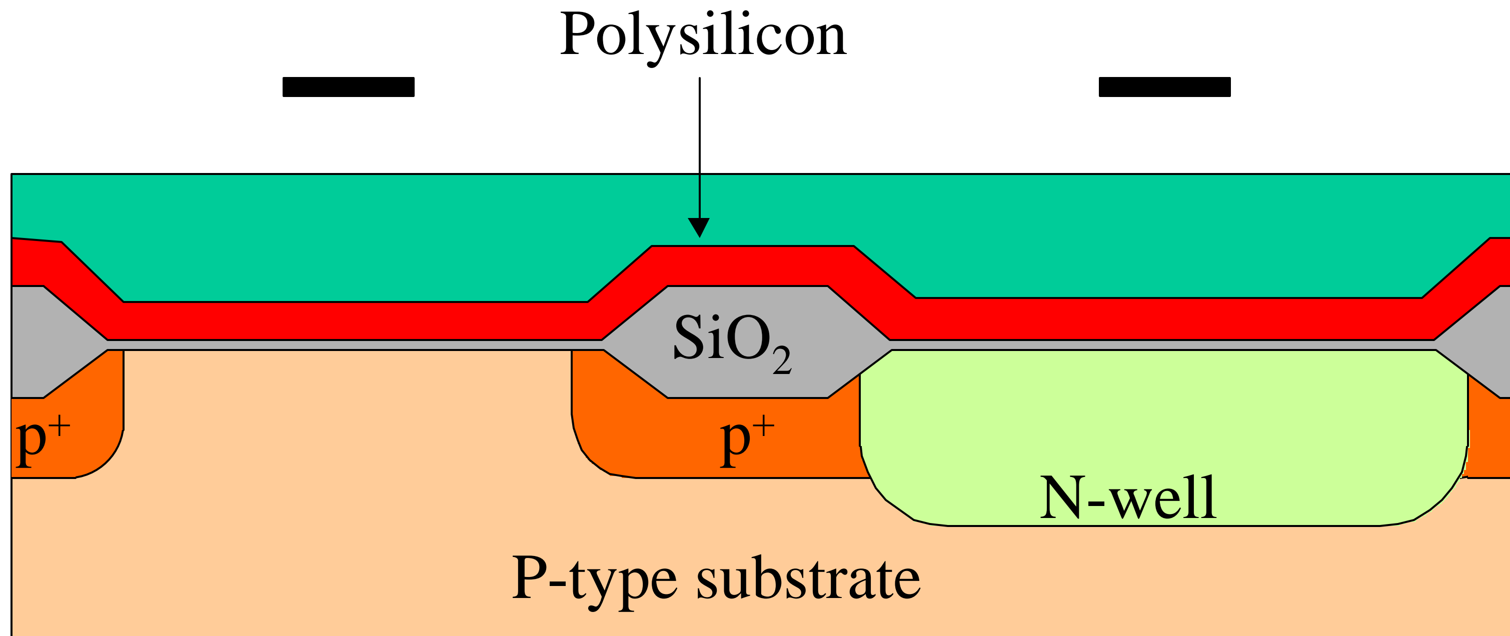
Photoresist Coating



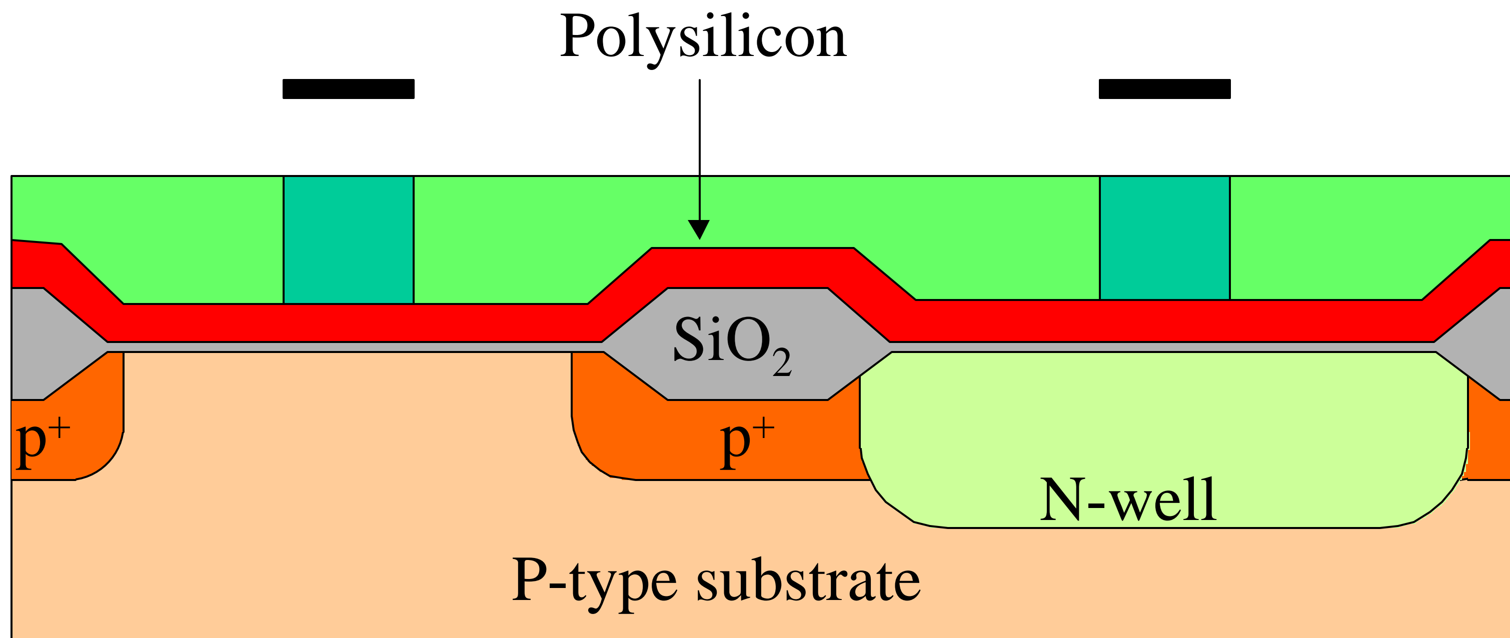
Mask 3, Gate and Local Interconnection



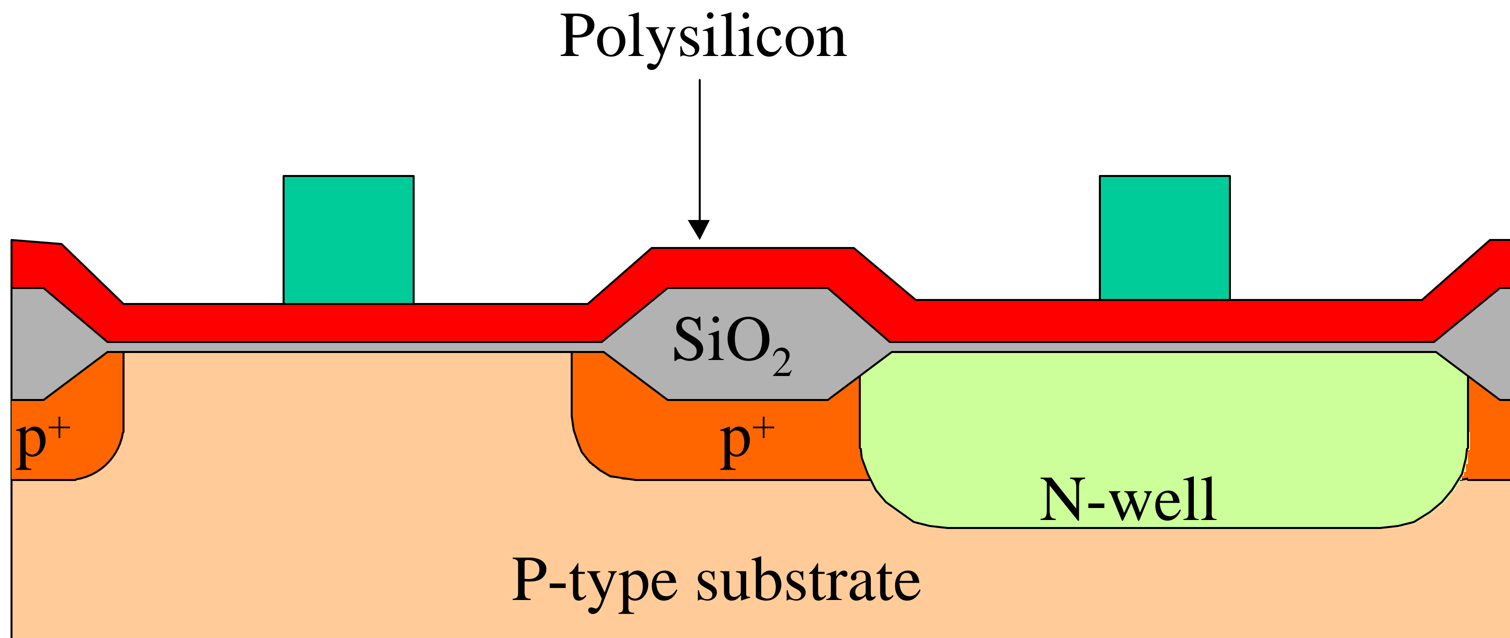
Mask 3, Gate and Local Interconnection



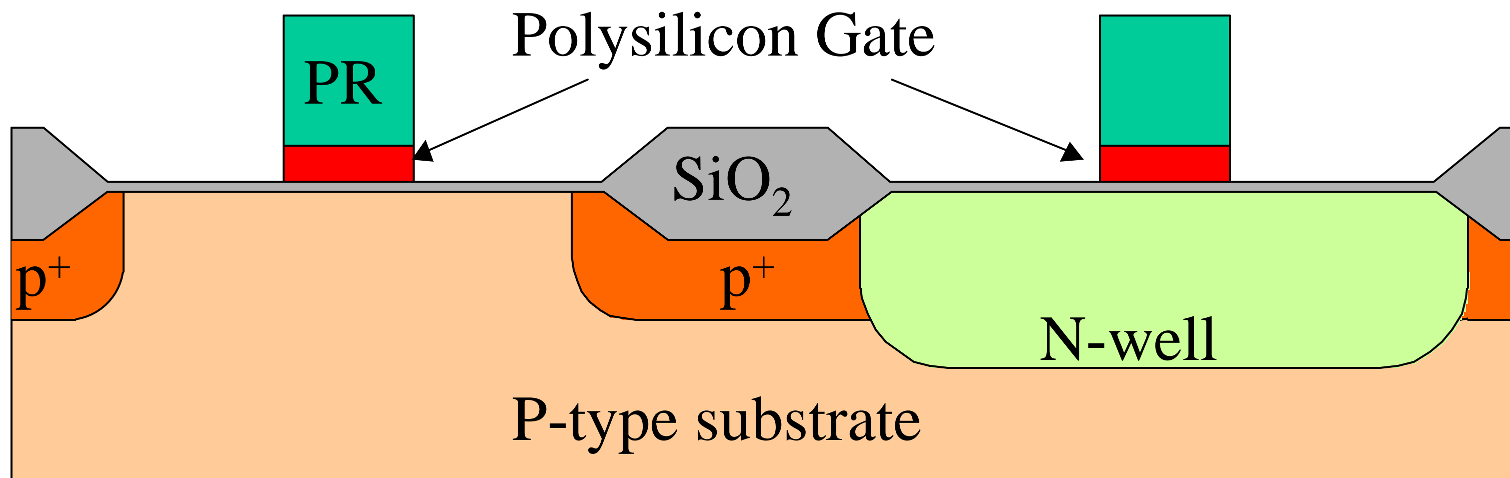
Exposure



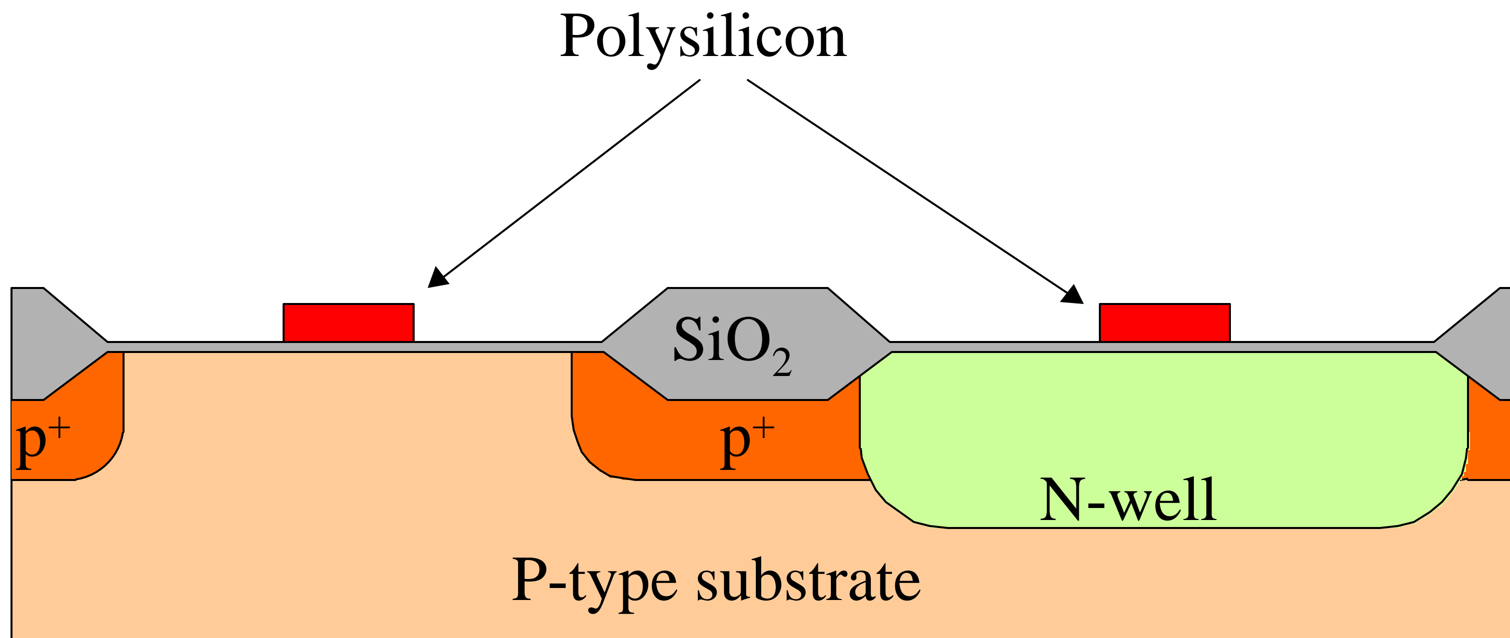
Development



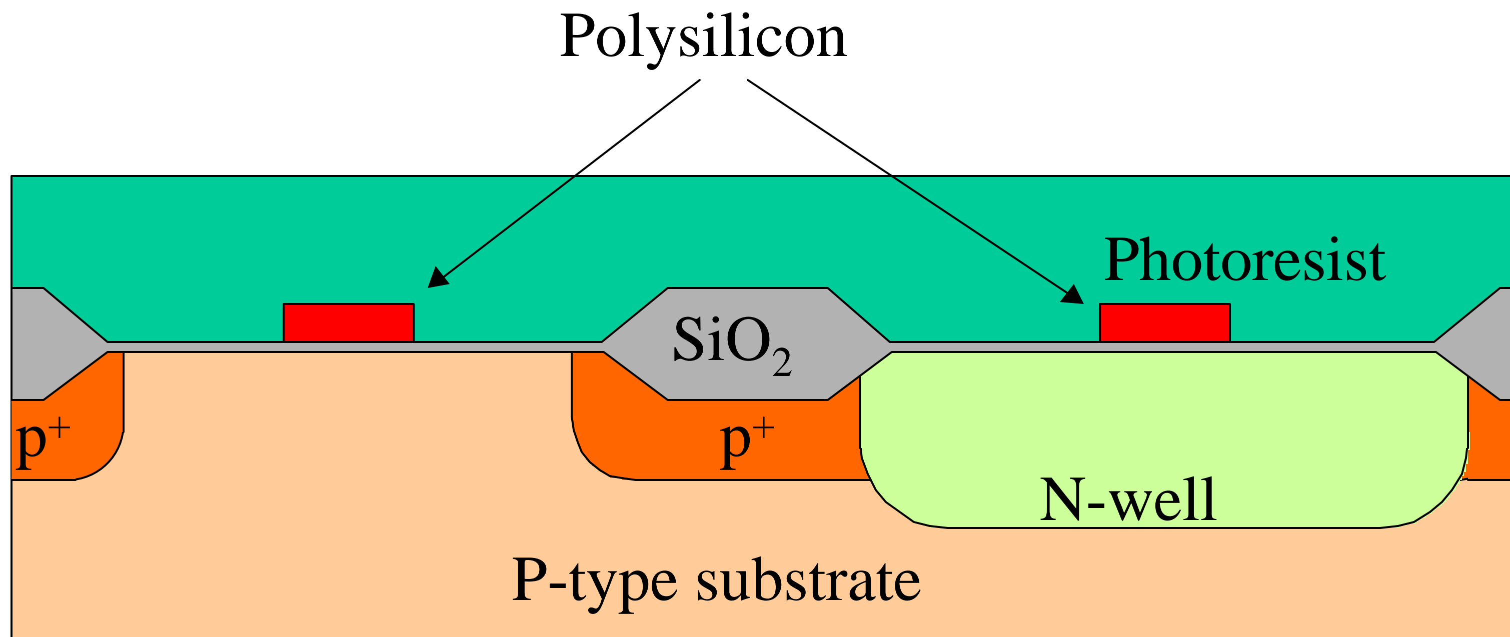
Etch Polysilicon



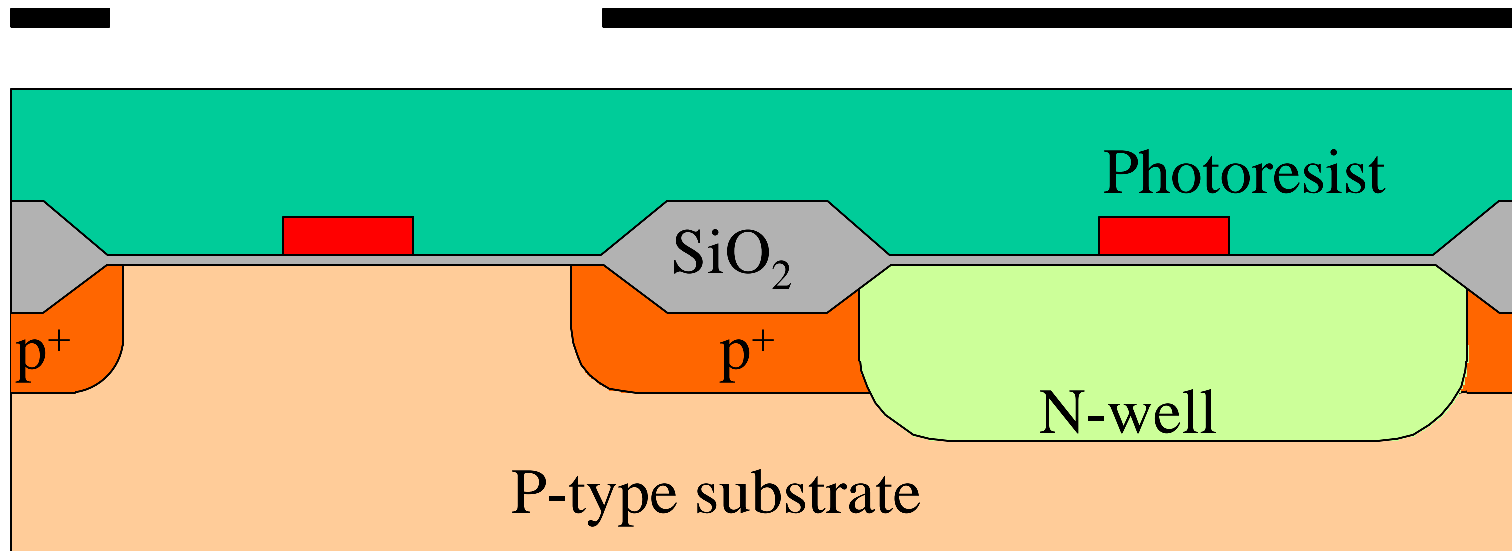
Strip Photoresist



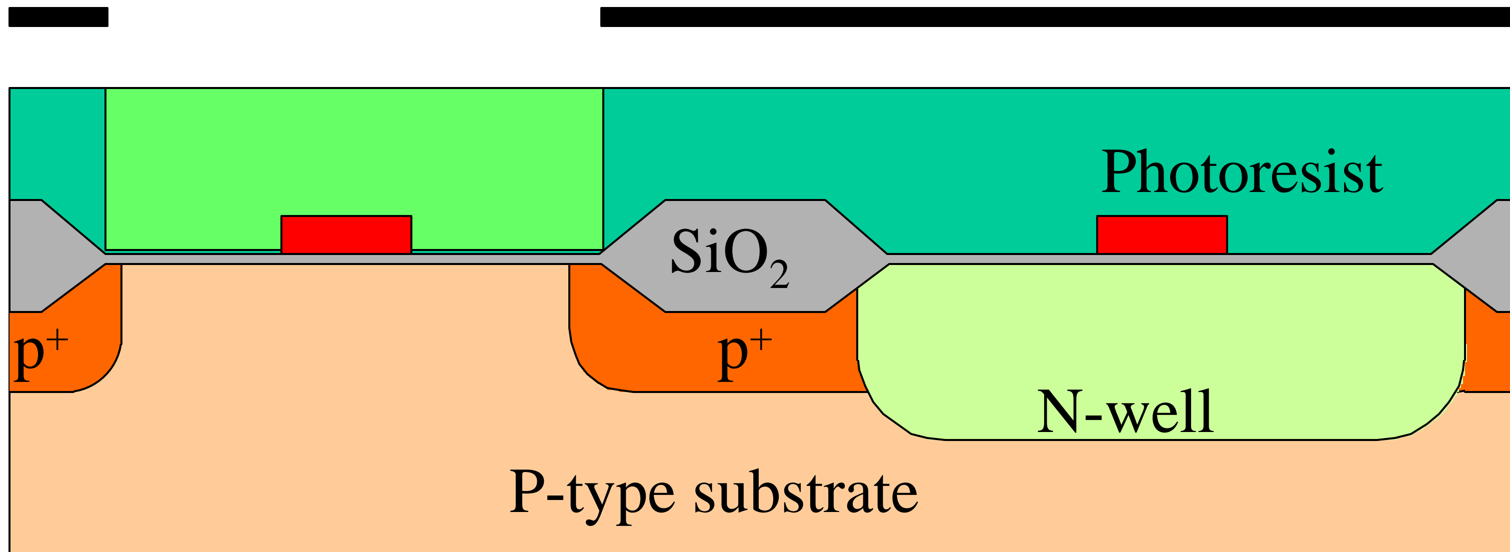
Photoresist Coating



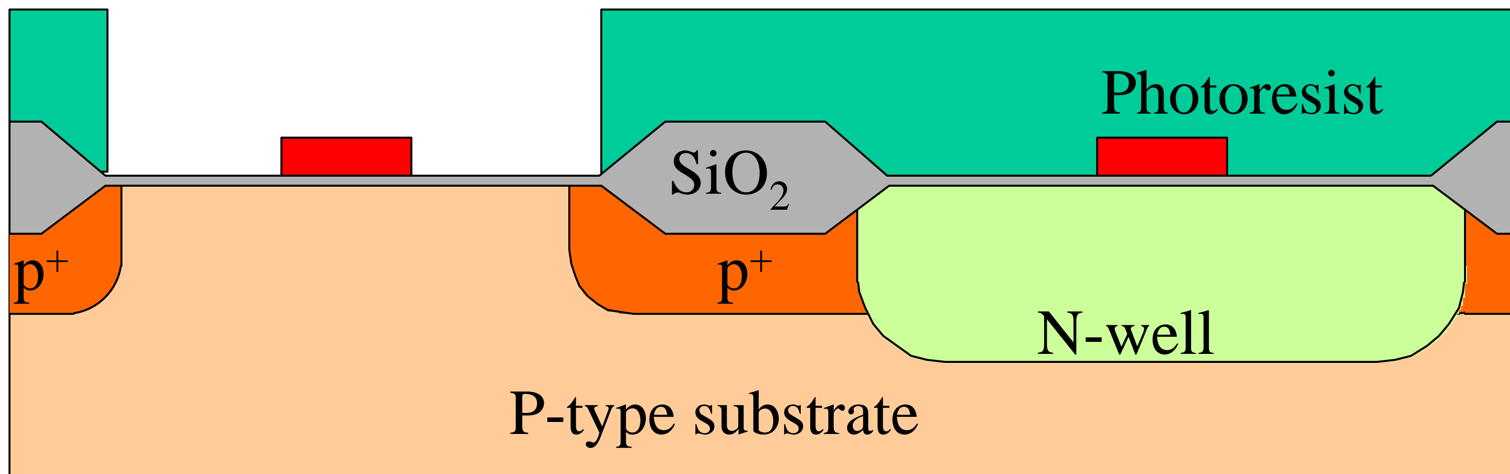
Mask 4, n-Source/Drain



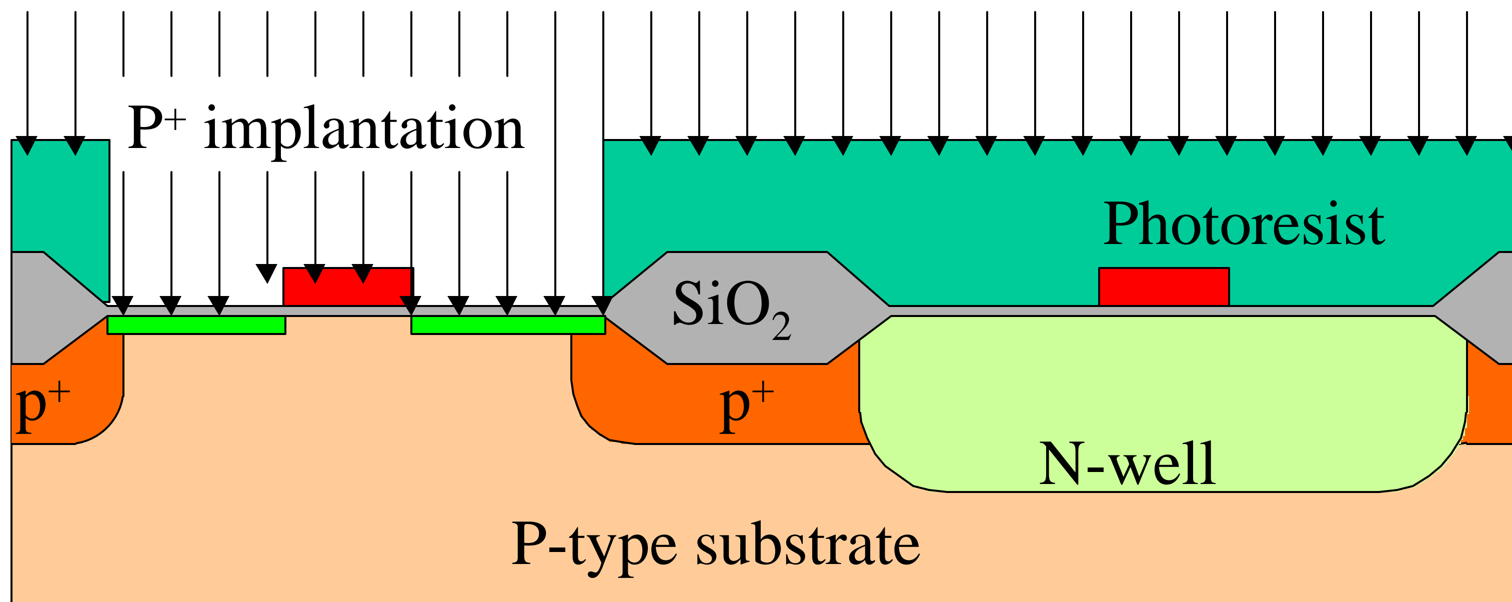
Exposure



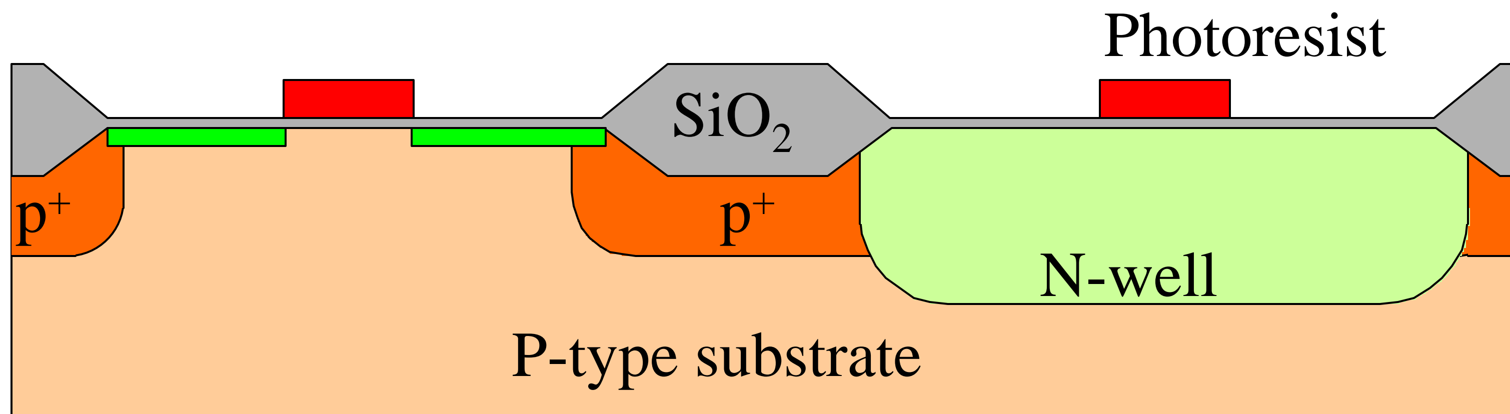
Development



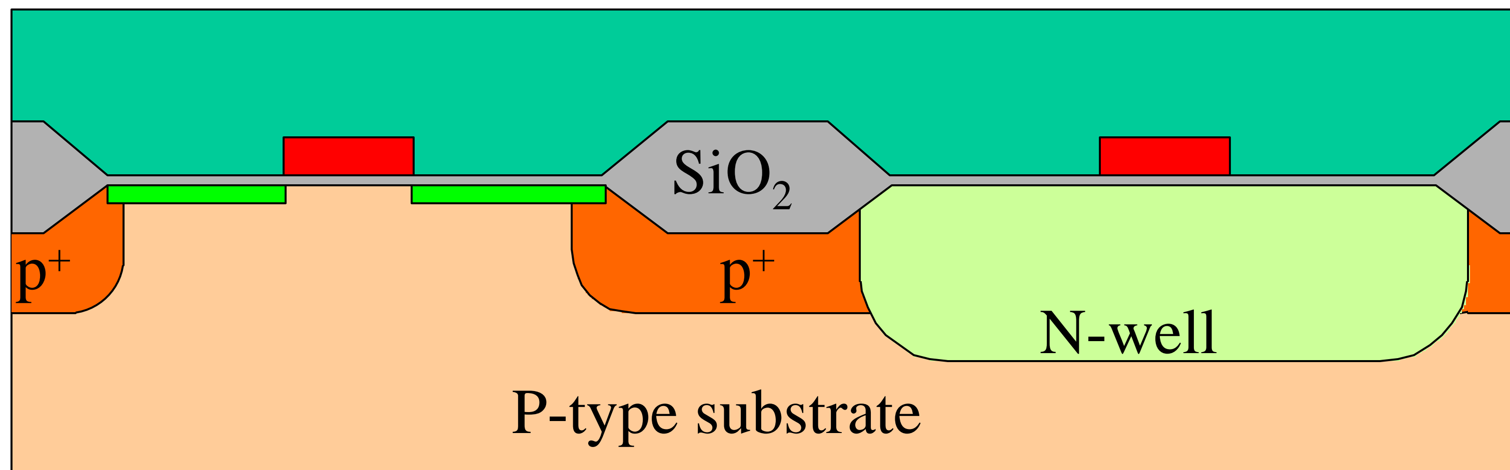
N-Source/Drain Ion Implantation



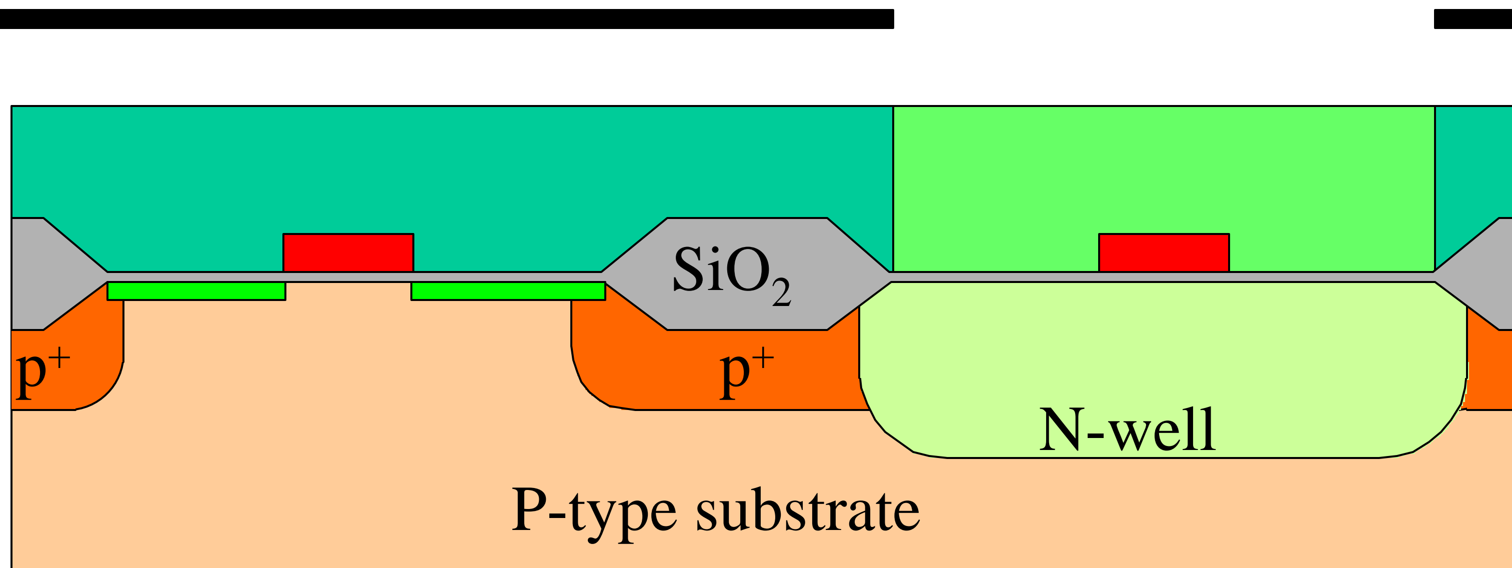
Strip Photoresist



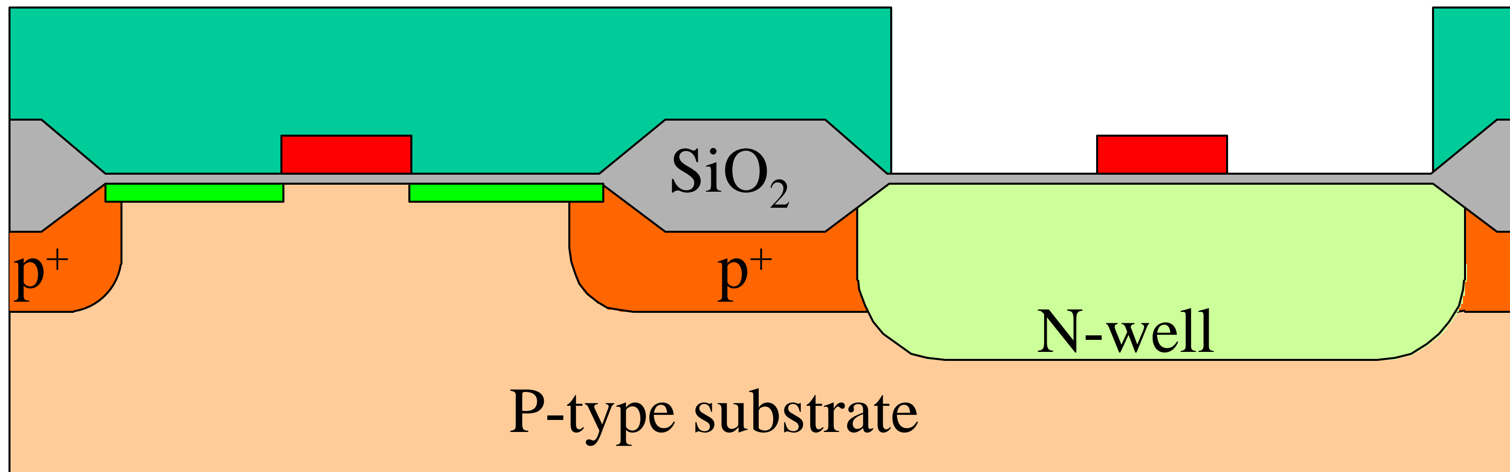
Photoresist Coating



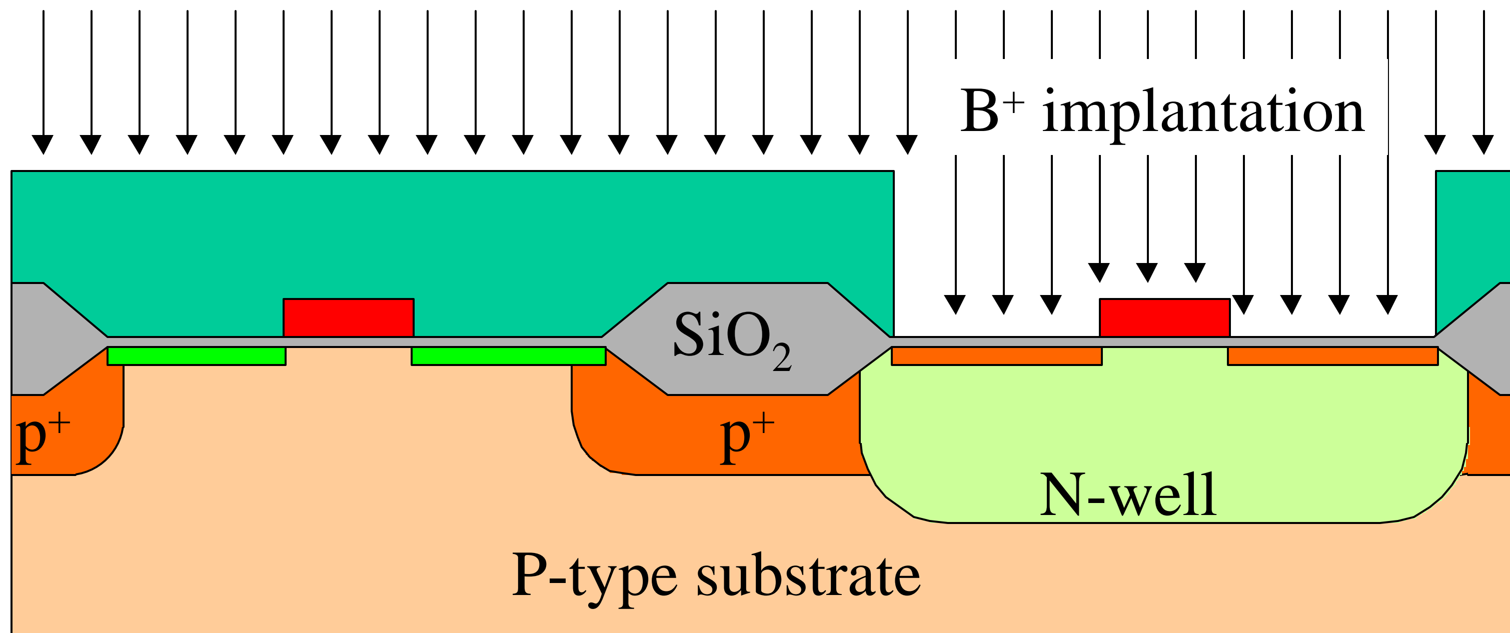
Mask 5, P-Source/Drain Exposure



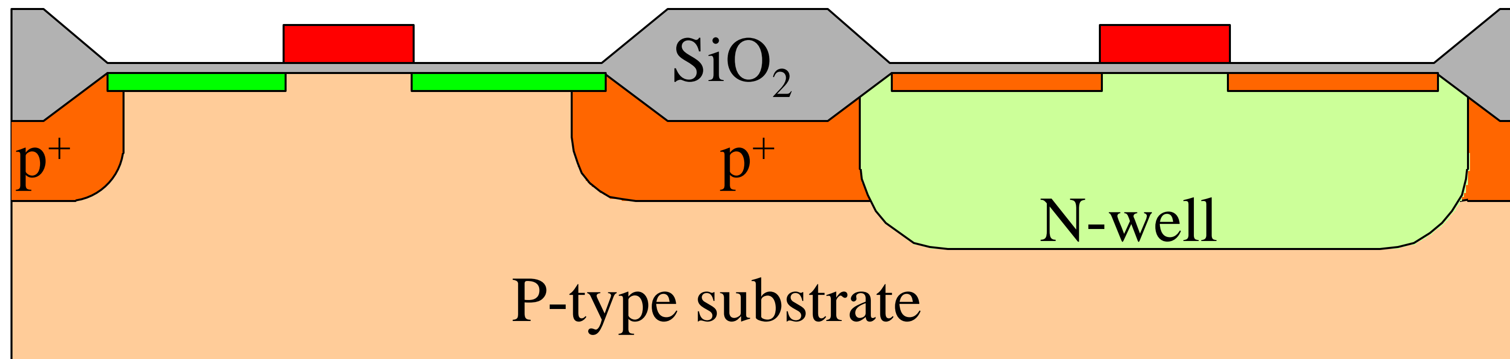
Development



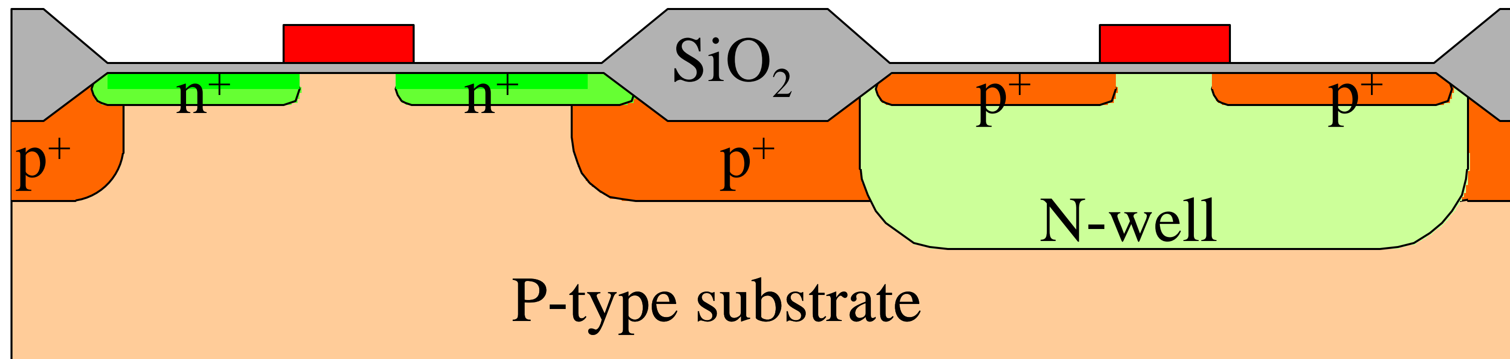
P-Source/Drain Implantation



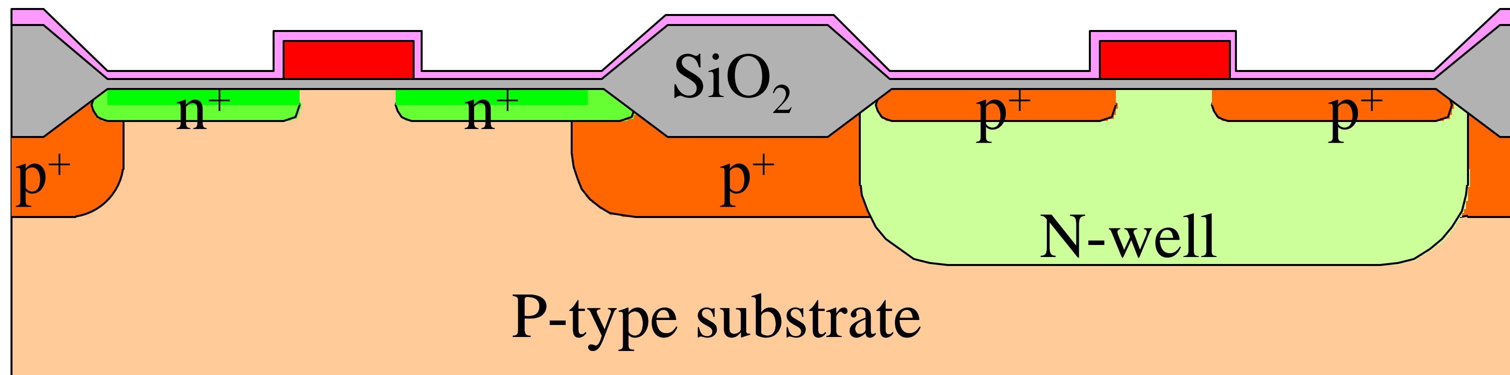
Strip Photoresist



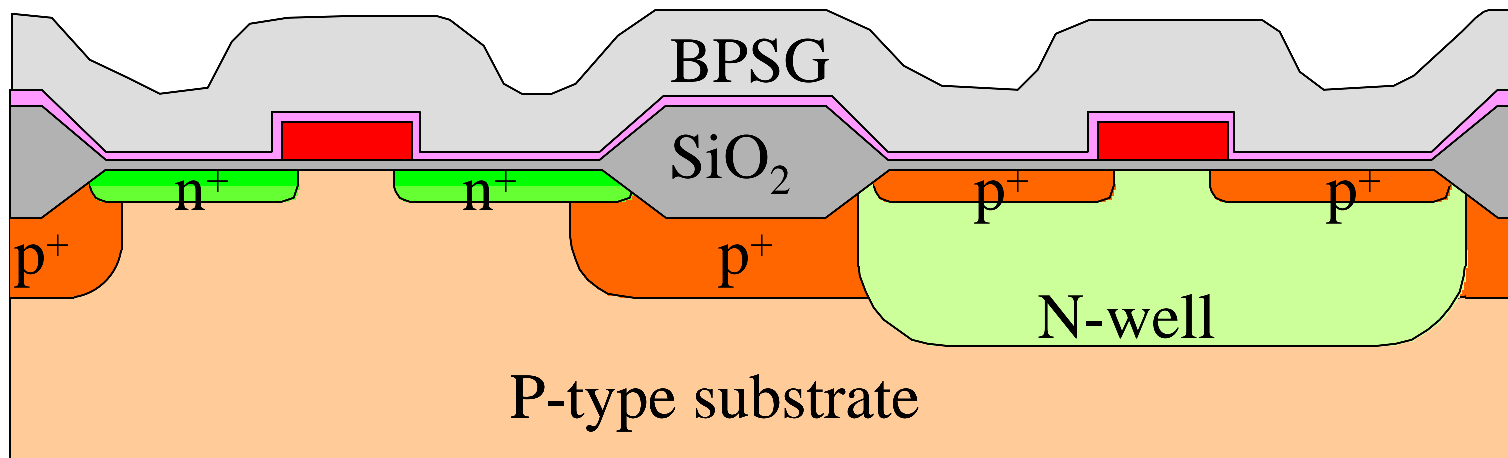
Anneal



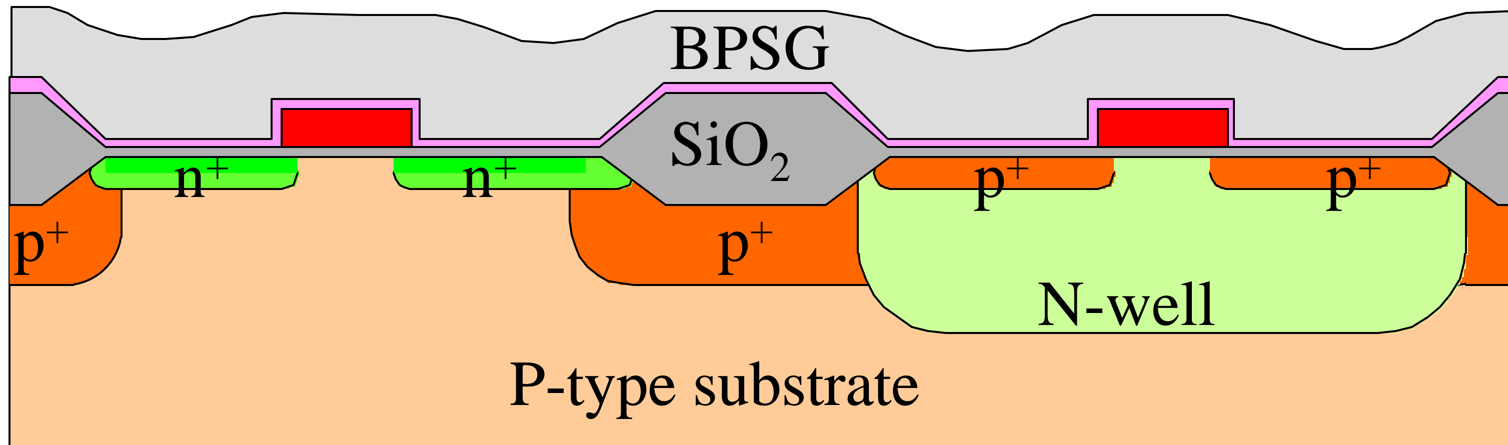
LPCVD Barrier Nitride



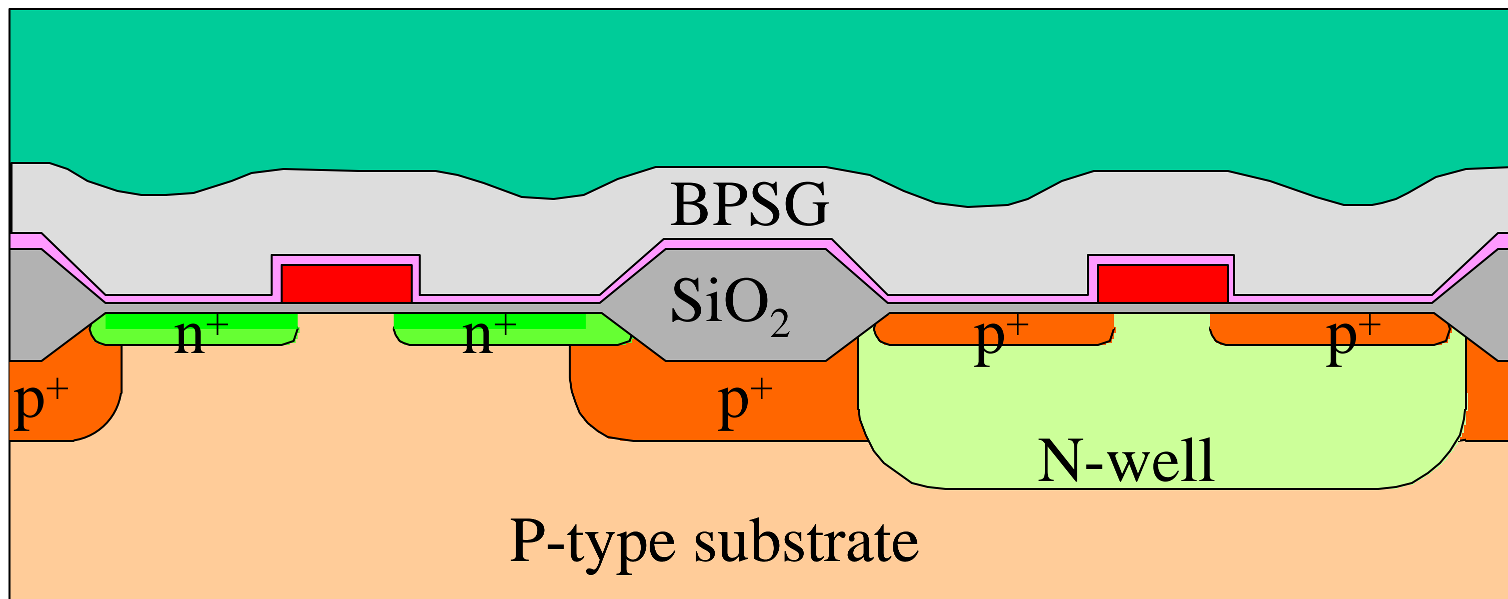
CVD BPSG



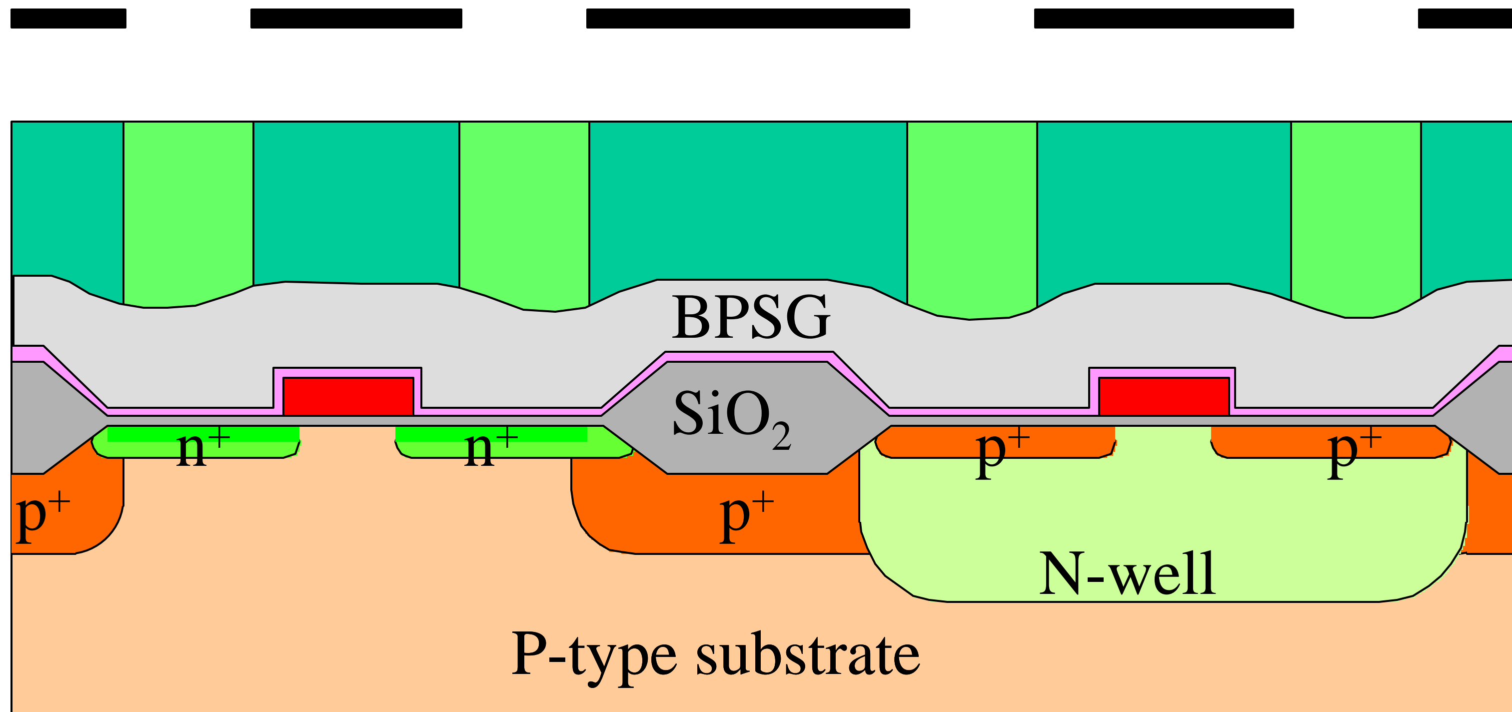
BPSG Reflow



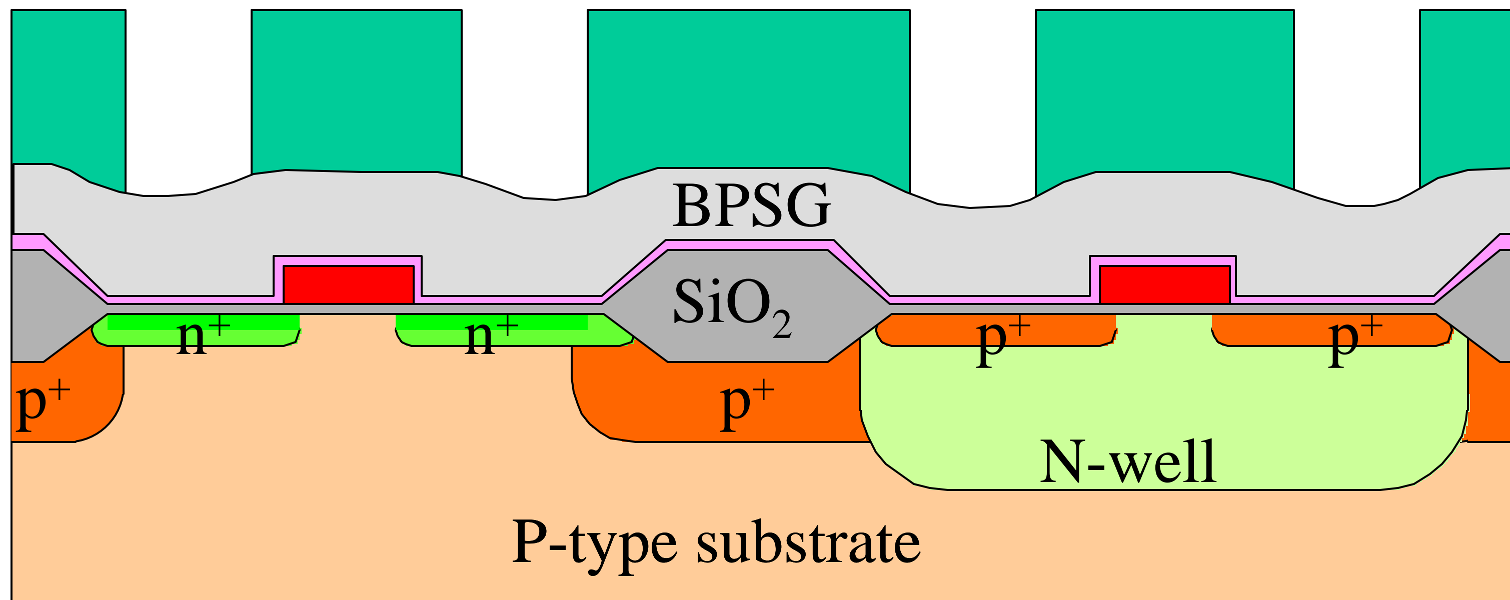
Photoresist Coating



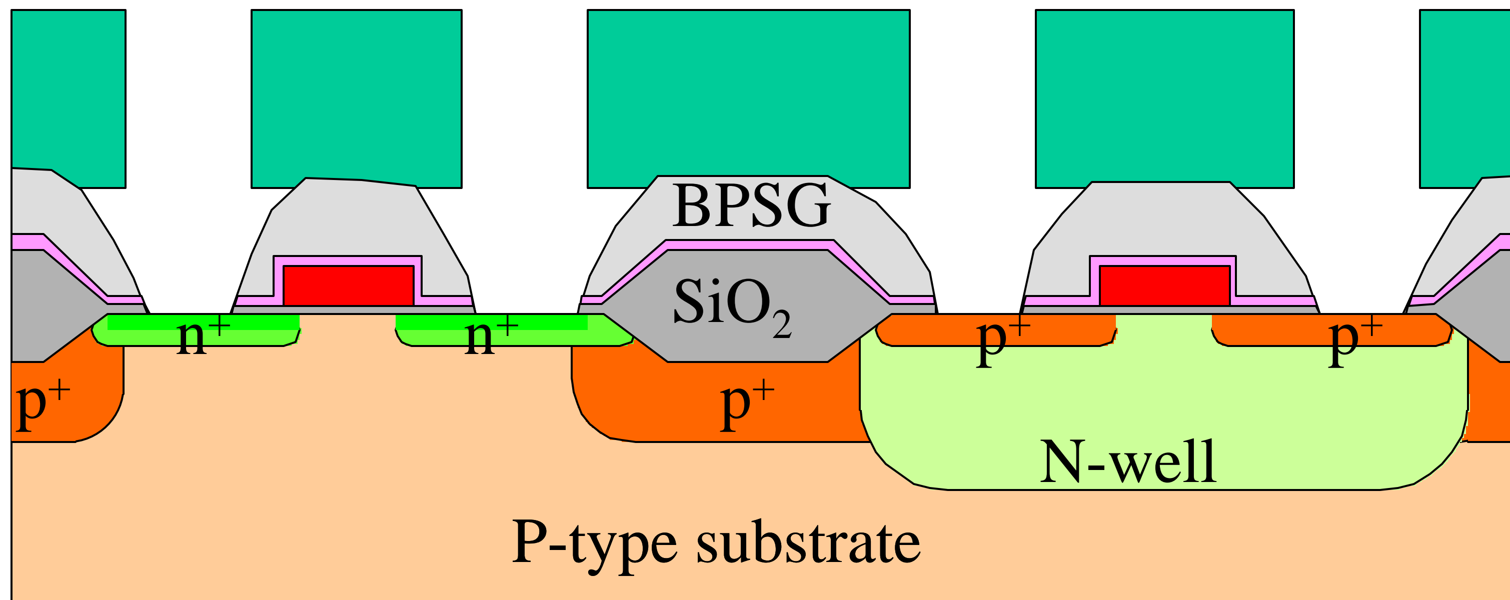
Mask 6, Contact Exposure



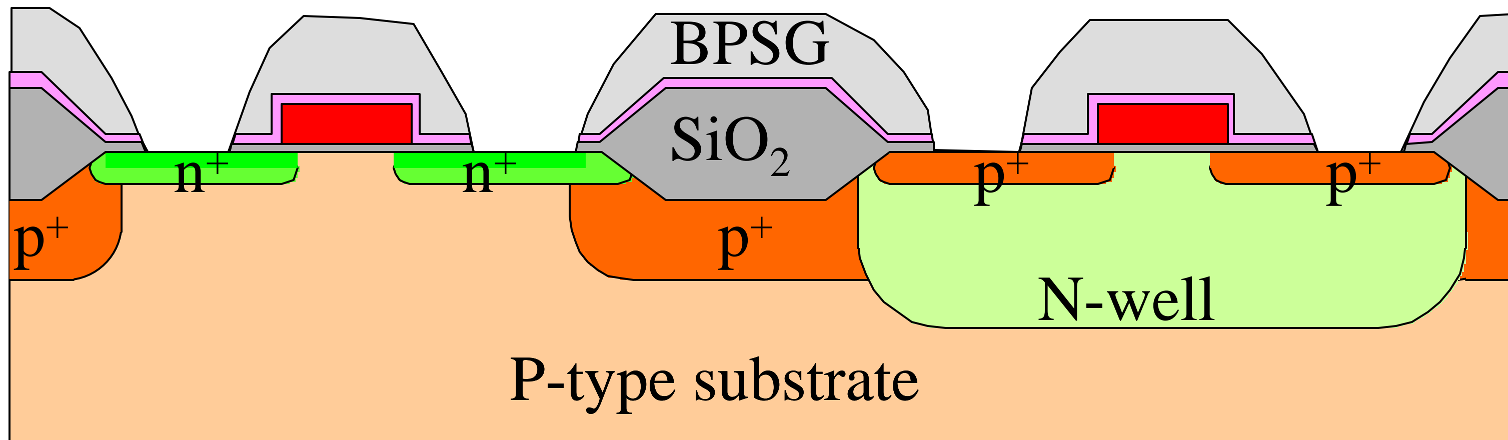
Development



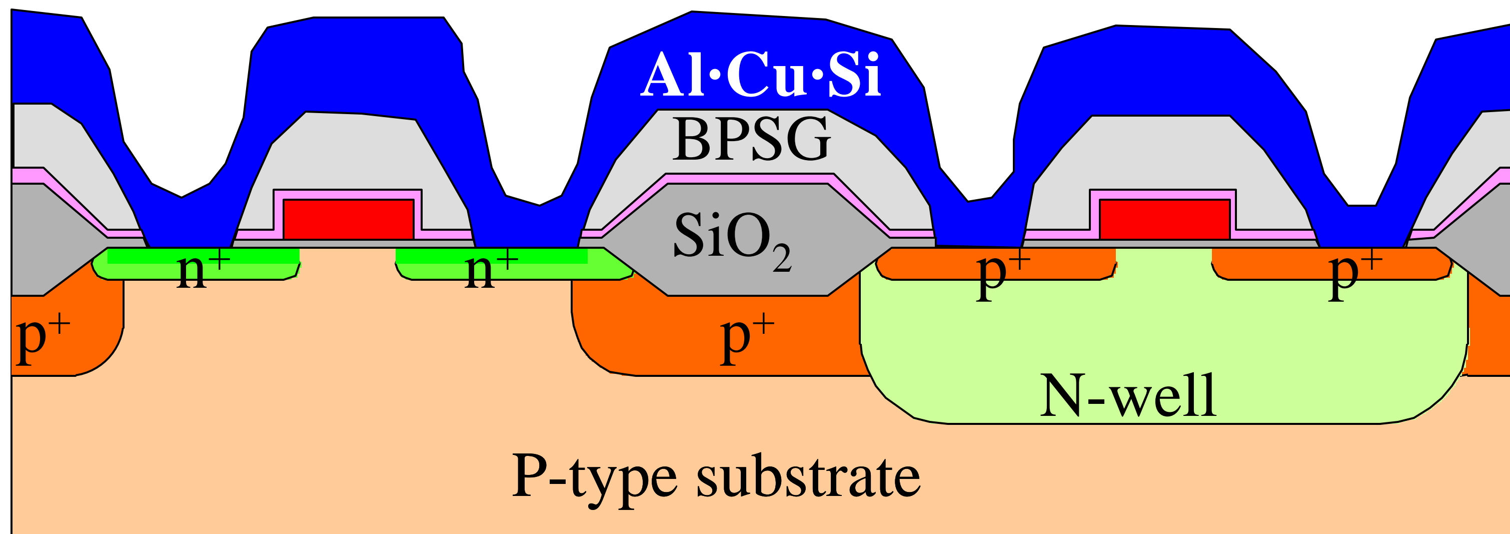
Contact Etch



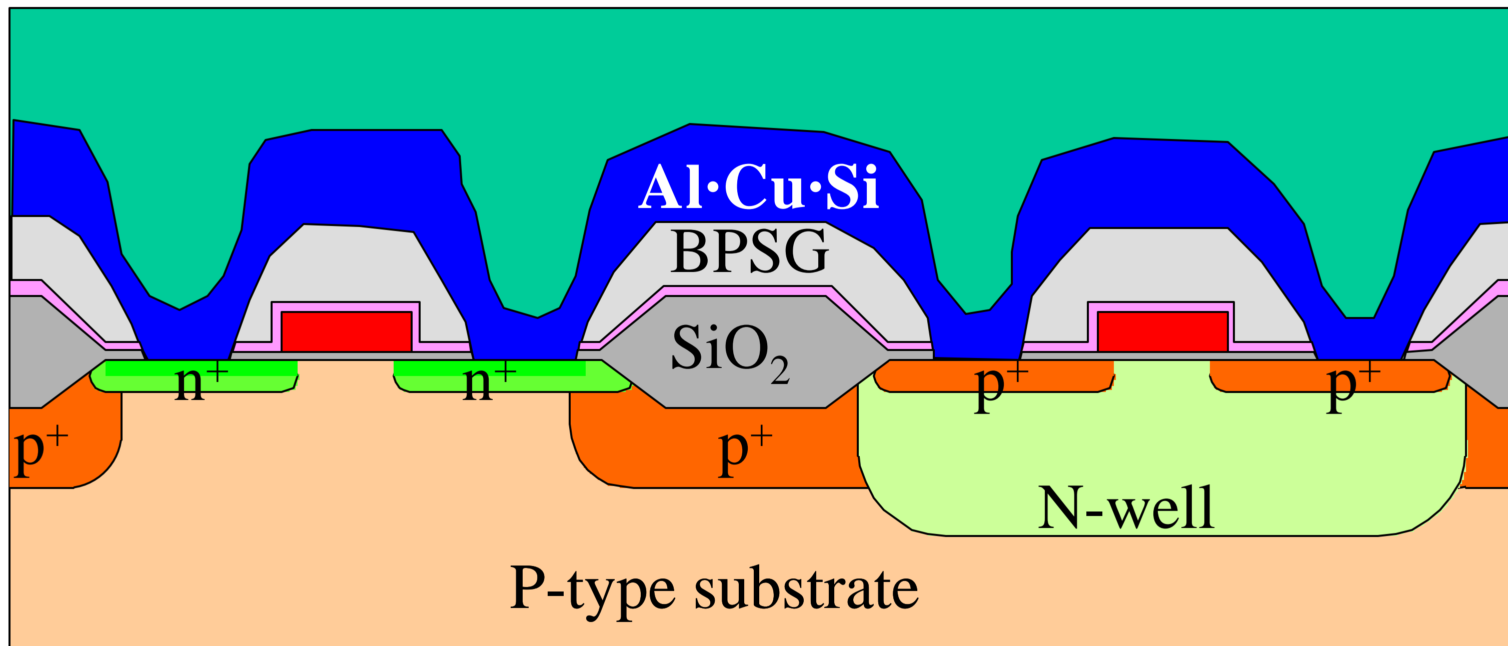
Strip Photoresist



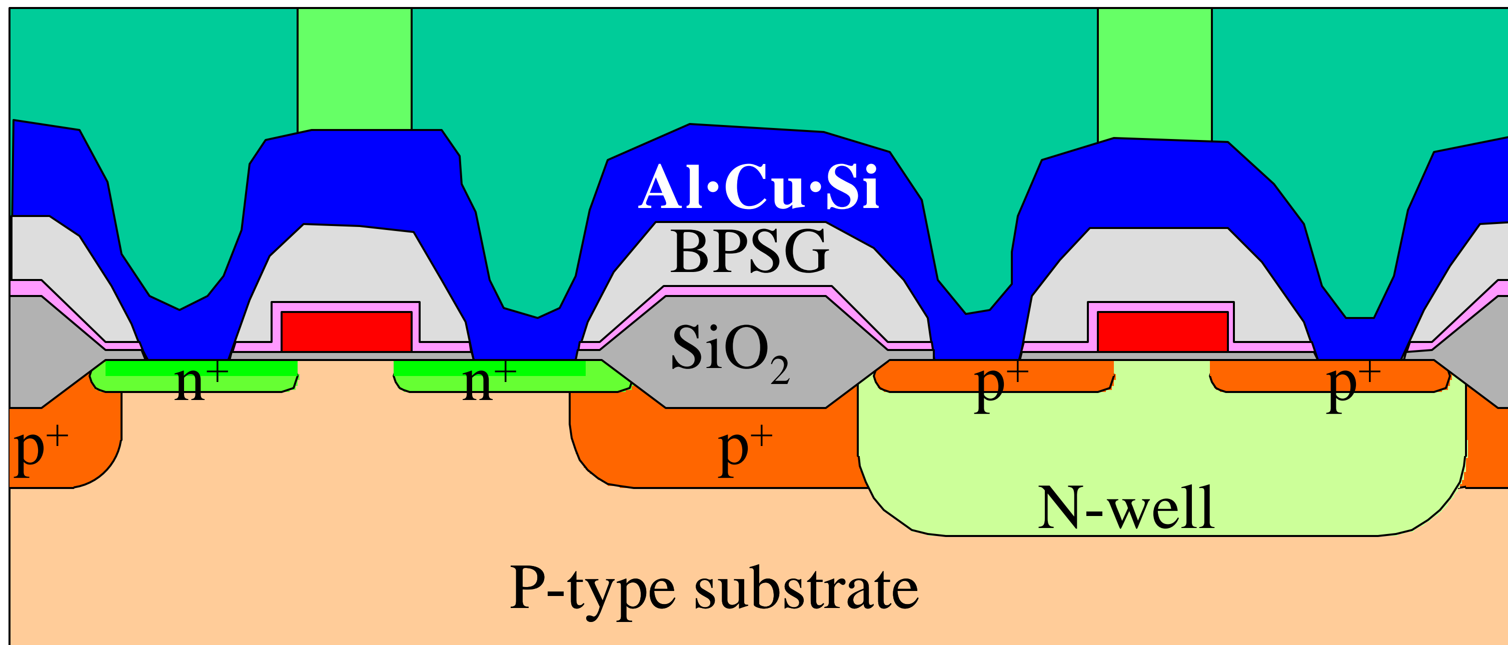
Metal Deposition



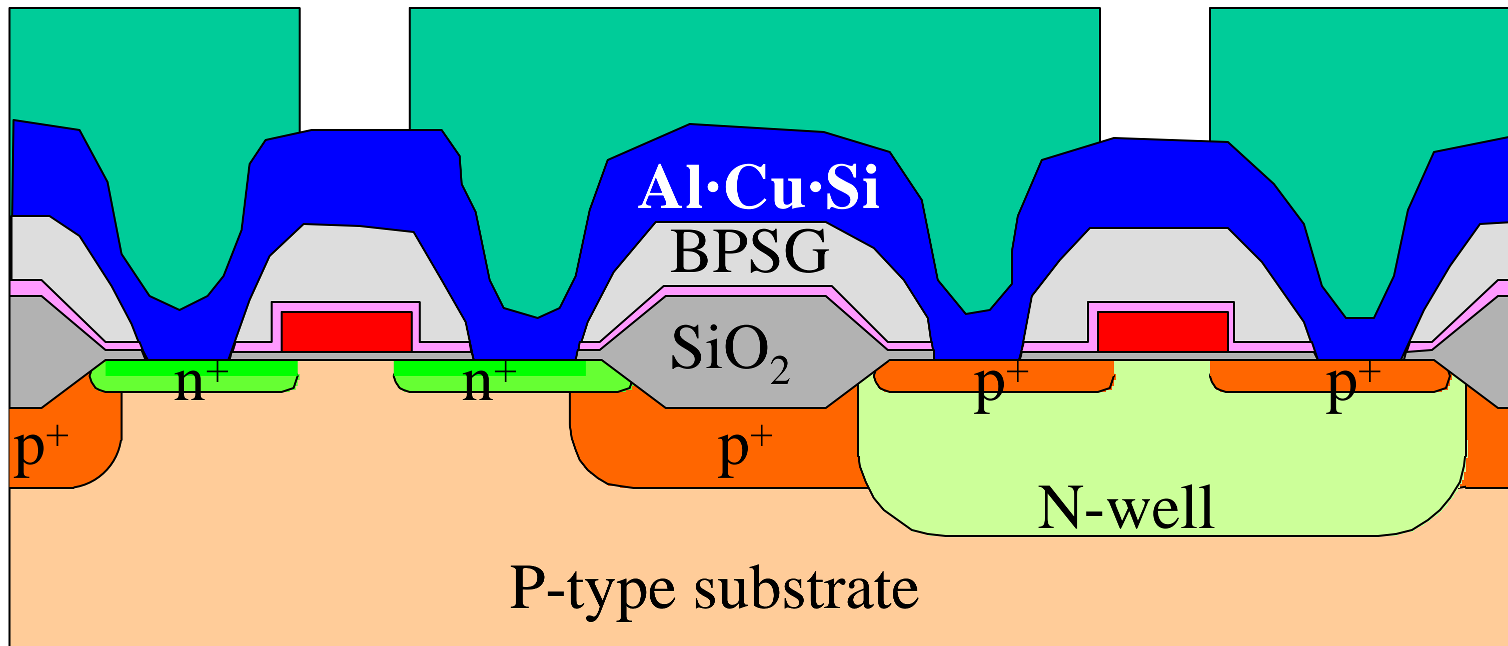
Photoresist Coating



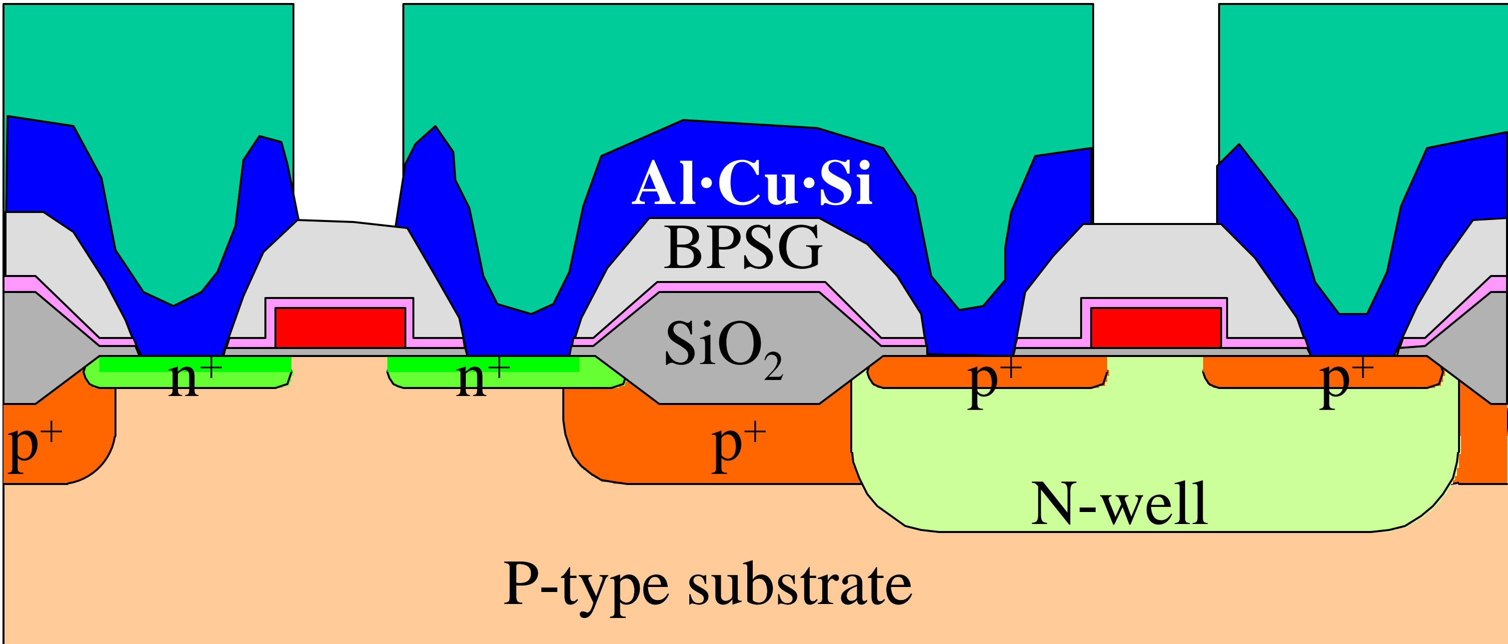
Mask 7, Metal Interconnection Exposure



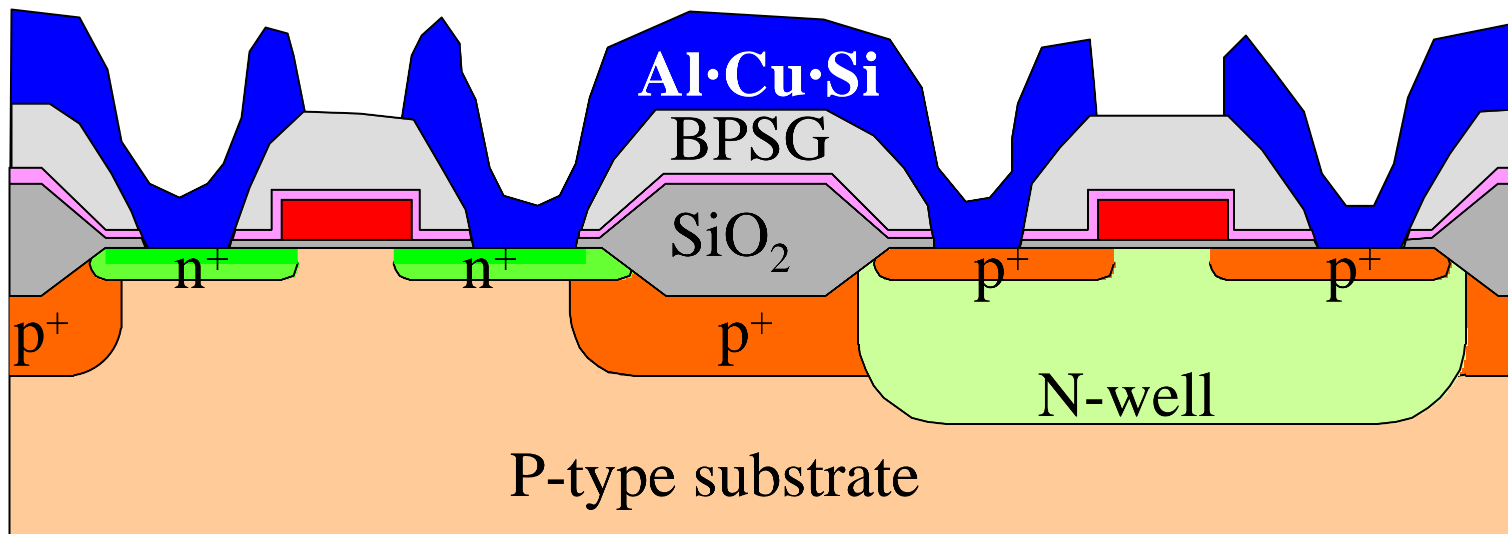
Development



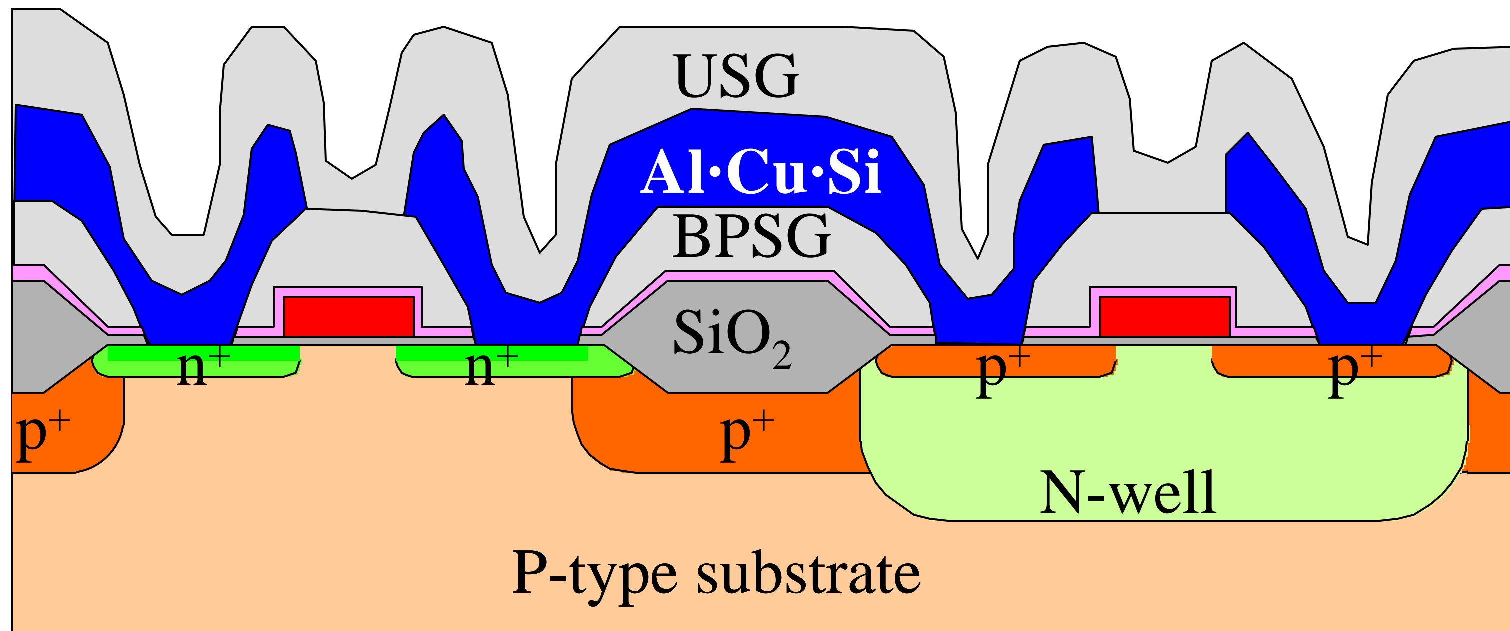
Etch Metal



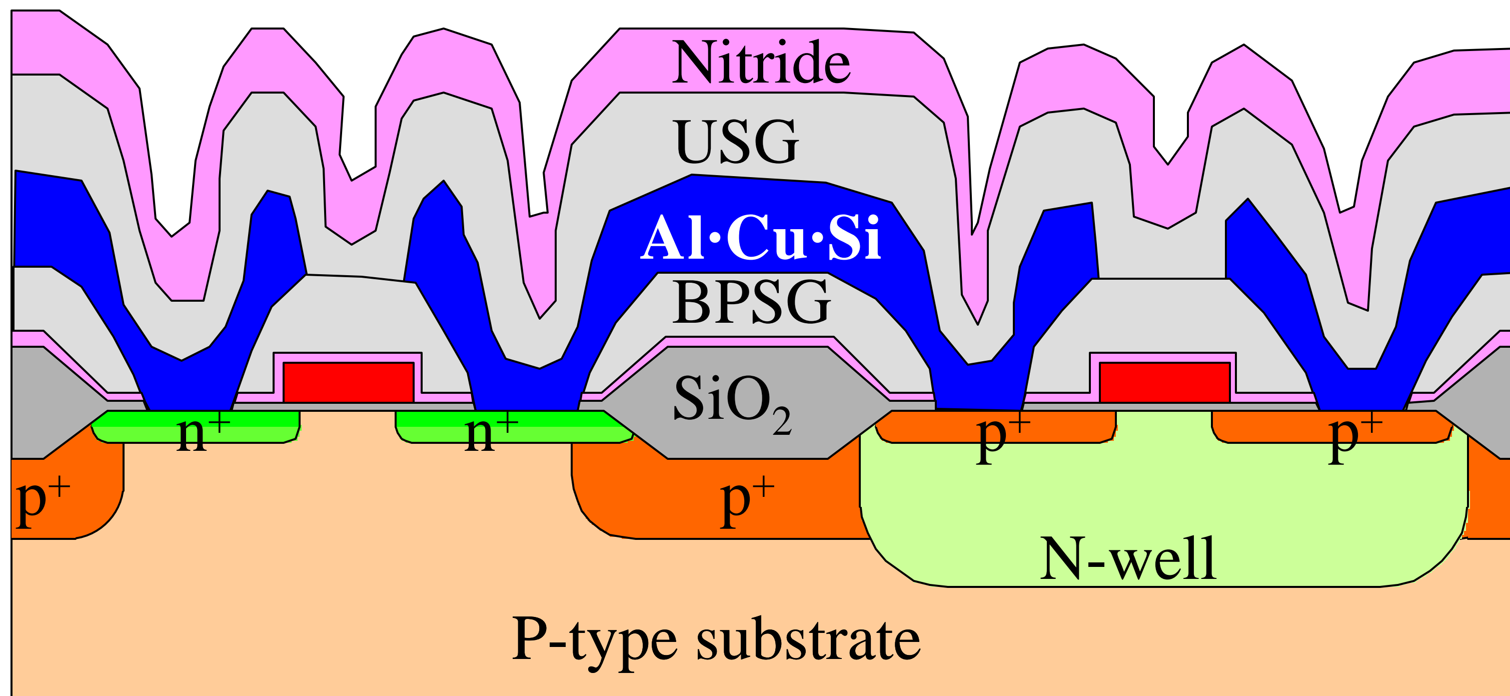
Strip Photoresist



CVD USG



CVD Nitride



1990's Technology

- Driving force: digital logic electronics
  - PC, telecommunication, and internet.
- Feature size: from 0.8 μm to 0.18 μm
- Wafer size: from 150 mm to 300 mm

1990's CMOS Technology

- Epitaxy silicon
- Shallow trench isolation
- The sidewall spacer for LDD and salicide
- Polycide gates and local interconnections reduce resistance and improve device speed
  - Tungsten silicide and titanium silicide.

1990's CMOS Technology

- Photolithography
  - G-line, I-line (365 nm), and DUV 248 nm
  - Positive photoresist
  - Steppers replaced projection printer
  - Track-stepper integrated systems
- Plasma etches for patterned etch
- Wet etches for blanket film stripping

1990's CMOS Technology

- Vertical furnaces
  - smaller footprints, better contamination control.
- RTP systems
  - post-implantation annealing
  - silicide formation,
  - faster, better process and thermal budget control.
- DC magnetron sputtering replaced evaporation

1990's CMOS Technology

- Multi-layer metal interconnection
- W CVD and CMP (or etch back) to form plugs
- Ti and TiN barrier/adhesion layer for W
- Ti welding layer for Al-Cu to reduce contact resistance
- TiN ARC

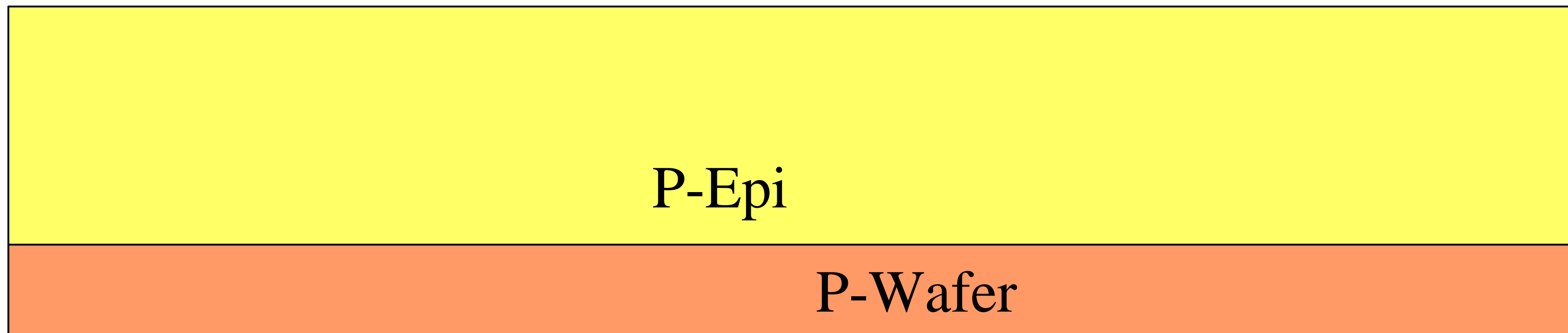
1990's CMOS Technology

- BPSG was popularly used as PMD.
- DCVD: PE-TEOS and O_3-TEOS
  - STI, sidewall spacer, PMD, and IMD
- DCVD: PE-silane
  - PMD barrier nitride, dielectric ARC, and PD nitride
- Tungsten CMP to form plug
- Dielectric CMP for planarization

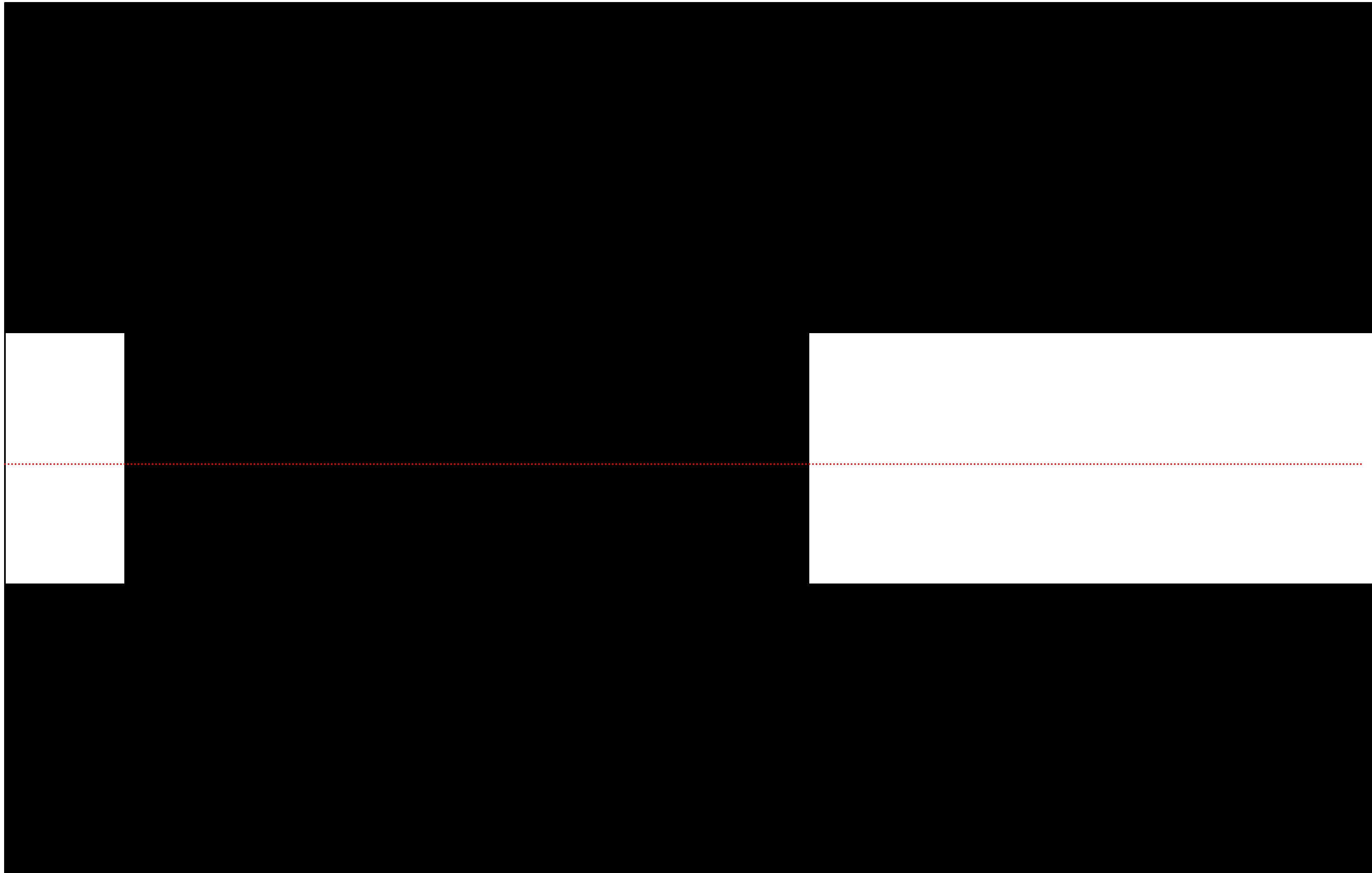
1990's CMOS Technology

- Cluster tools became very popular
- Single wafer processing systems improve wafer-to-wafer uniformity control
- Batch systems is still commonly employed in many non-critical processes for their high throughput.

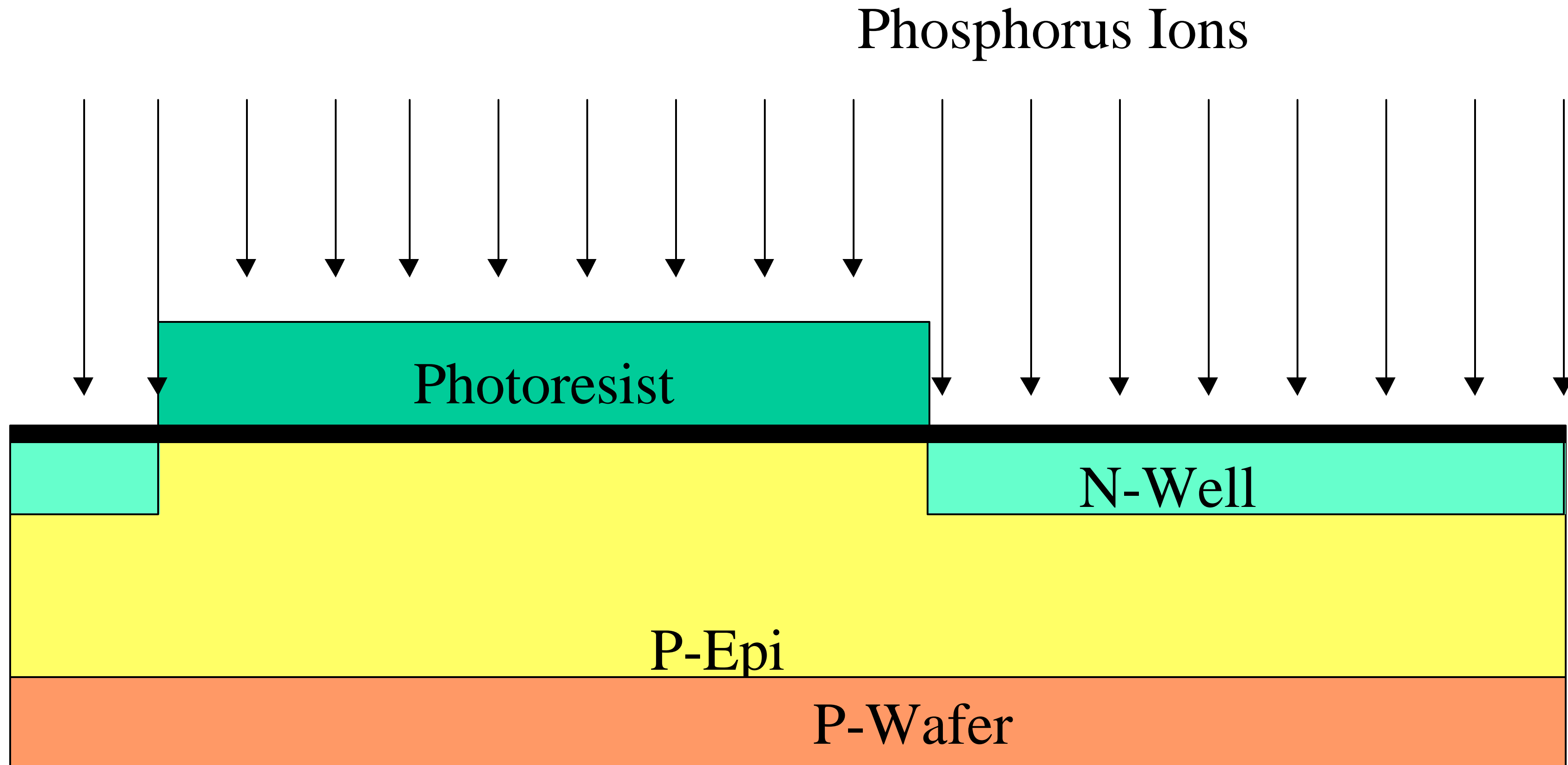
Epitaxy Deposition



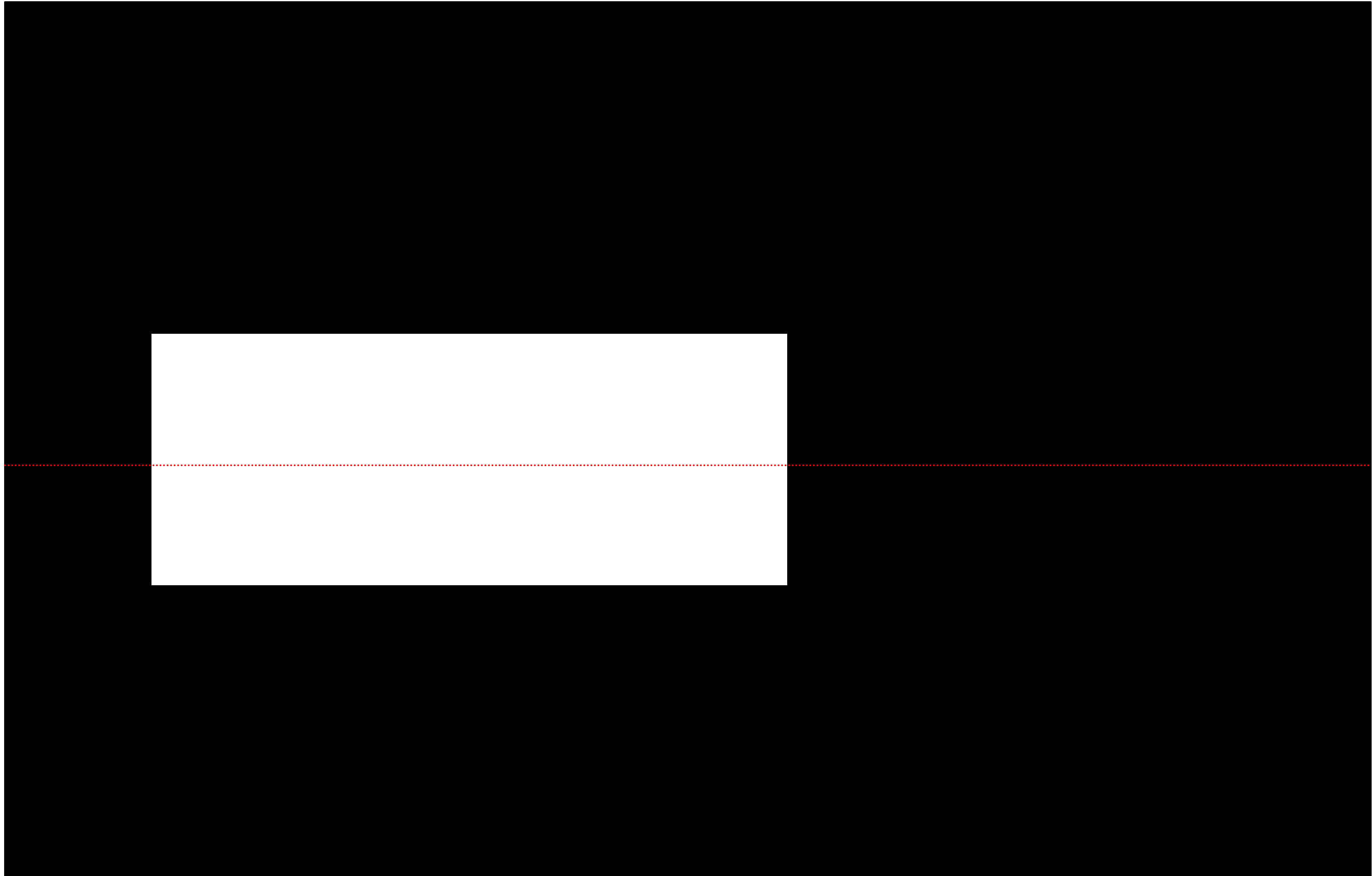
Mask 1: N-well



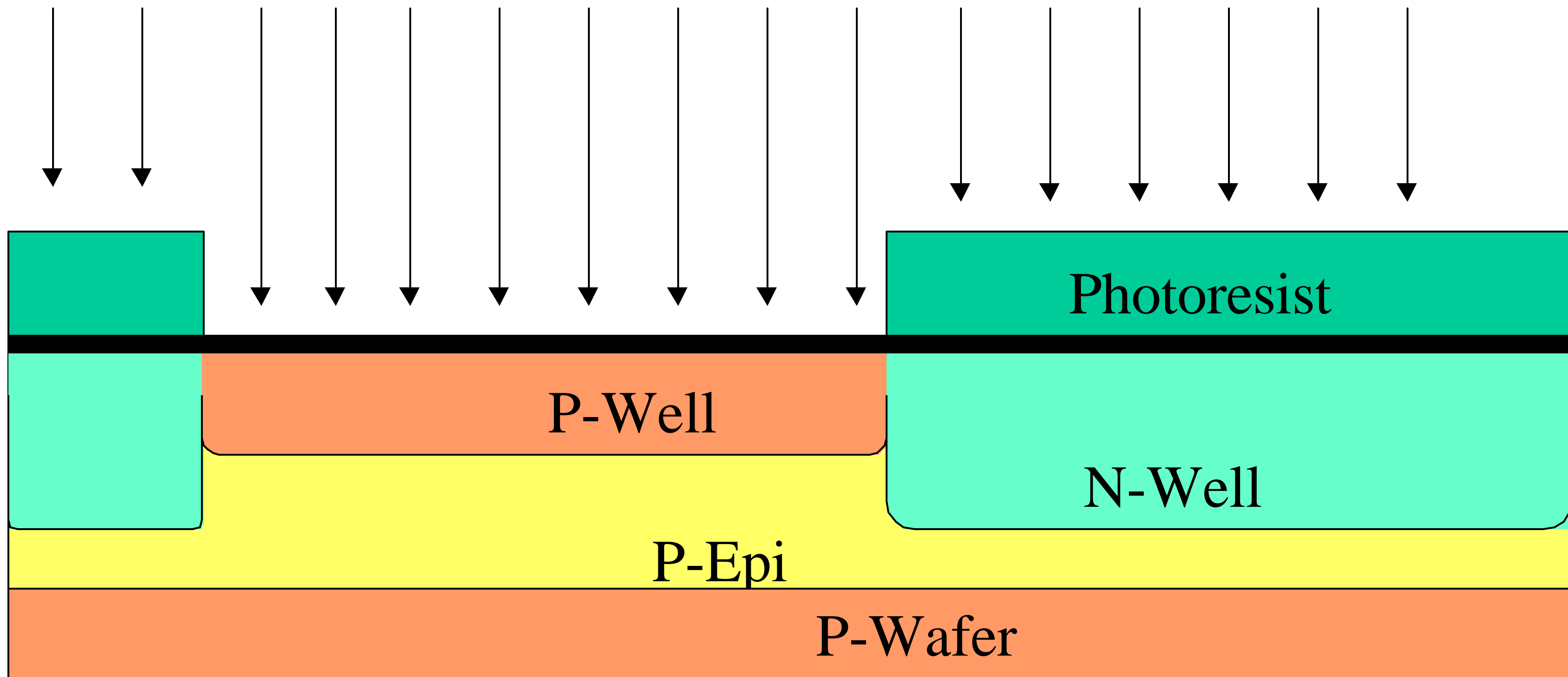
N-well Implantation



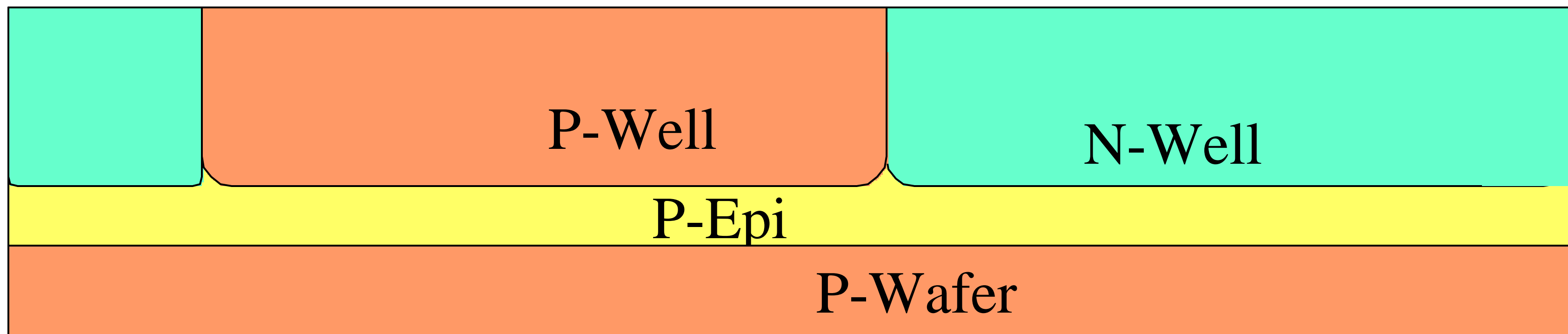
Mask 2: P-well



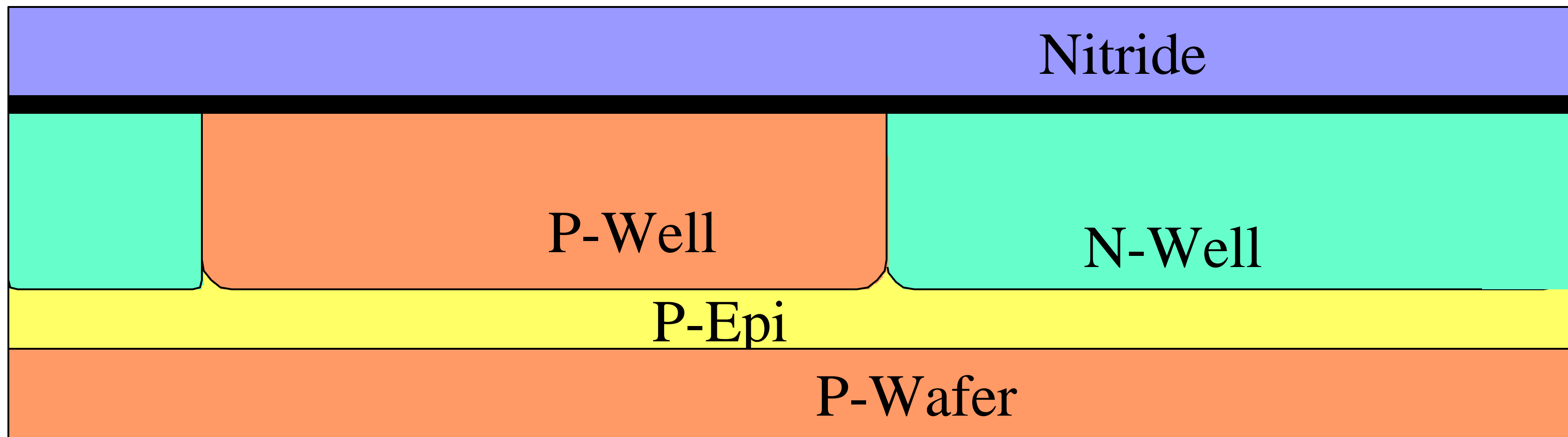
P-well Implantation



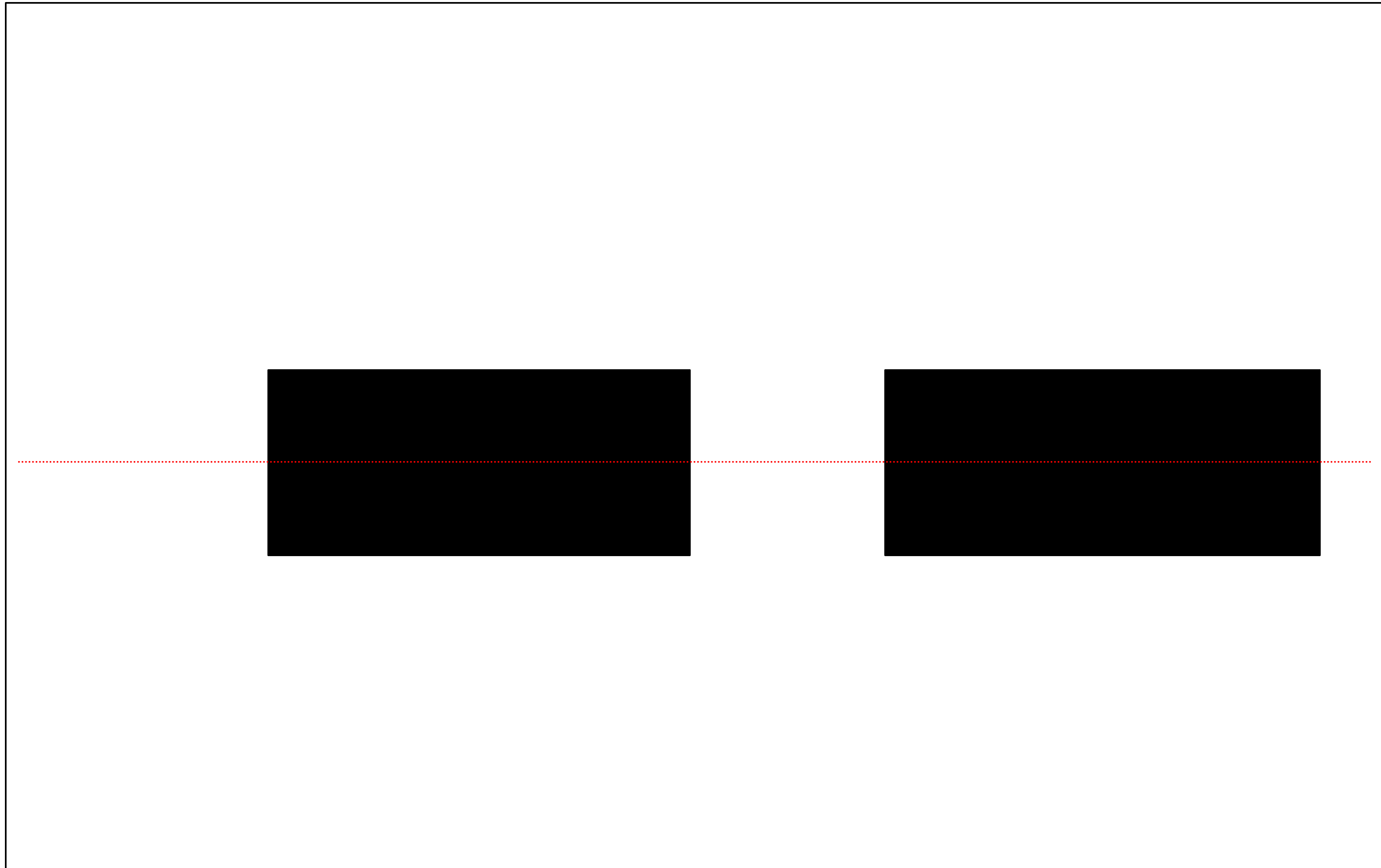
Strip PR, Strip Nitride/Pad Oxide



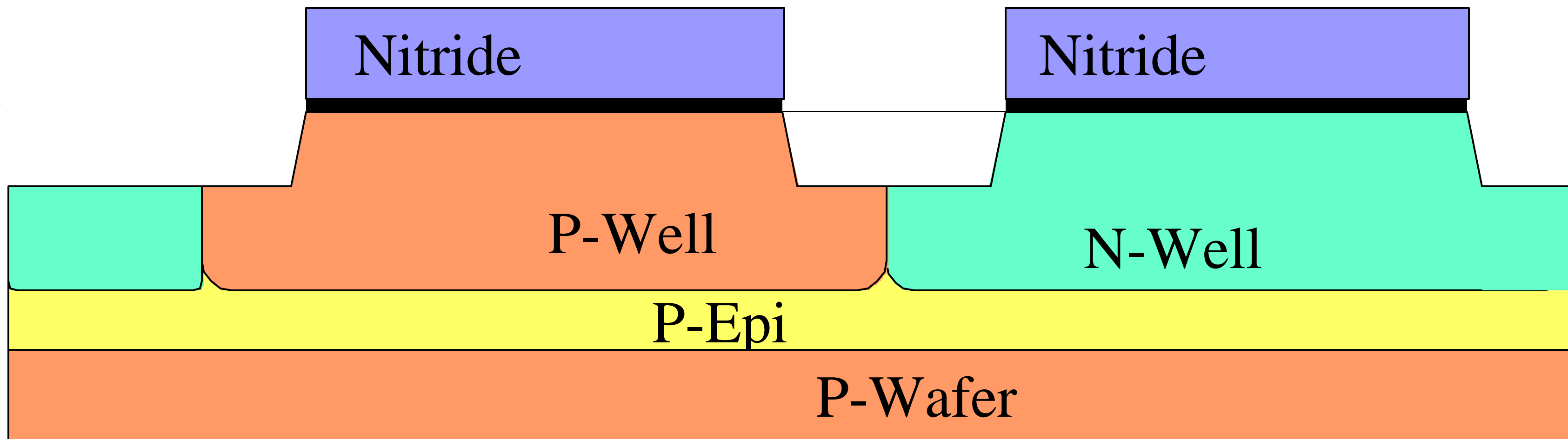
Pad Oxidation, LPCVD Nitride



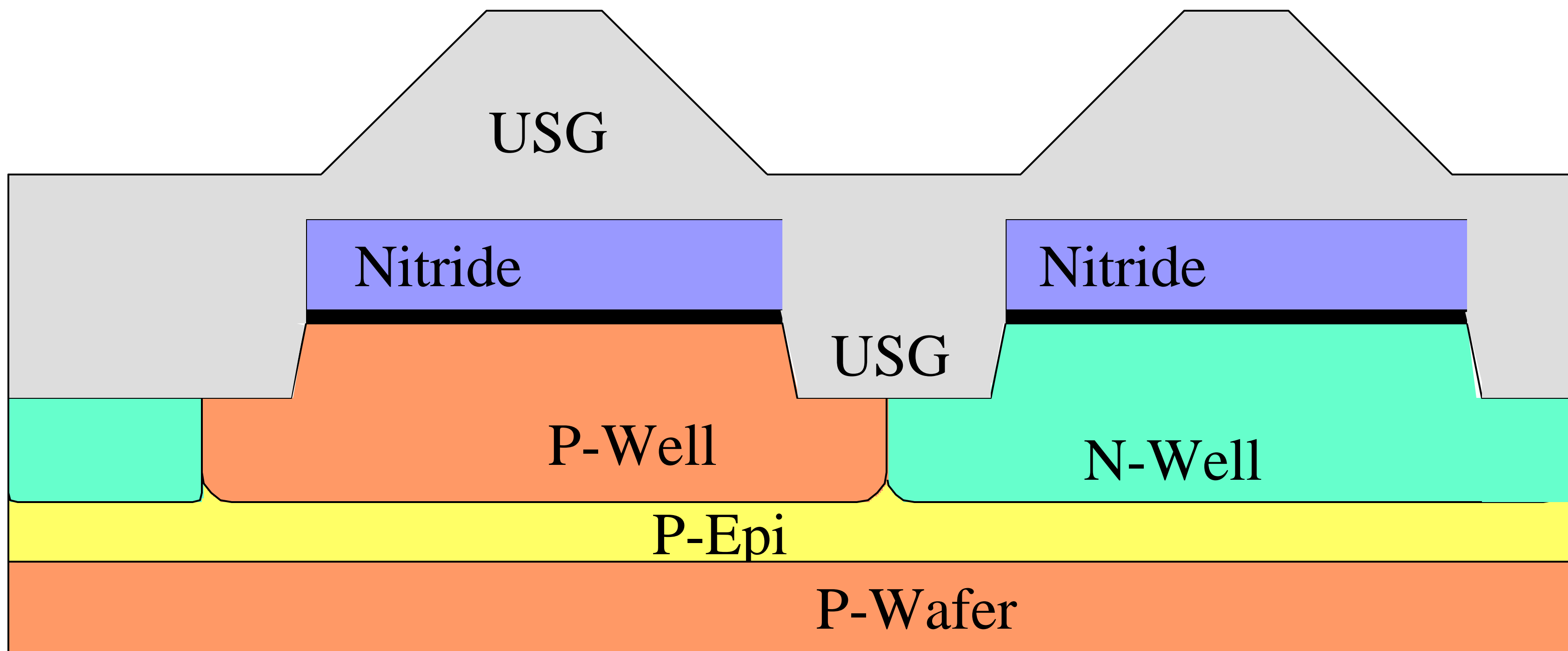
Mask 3: Shallow Trench Isolation



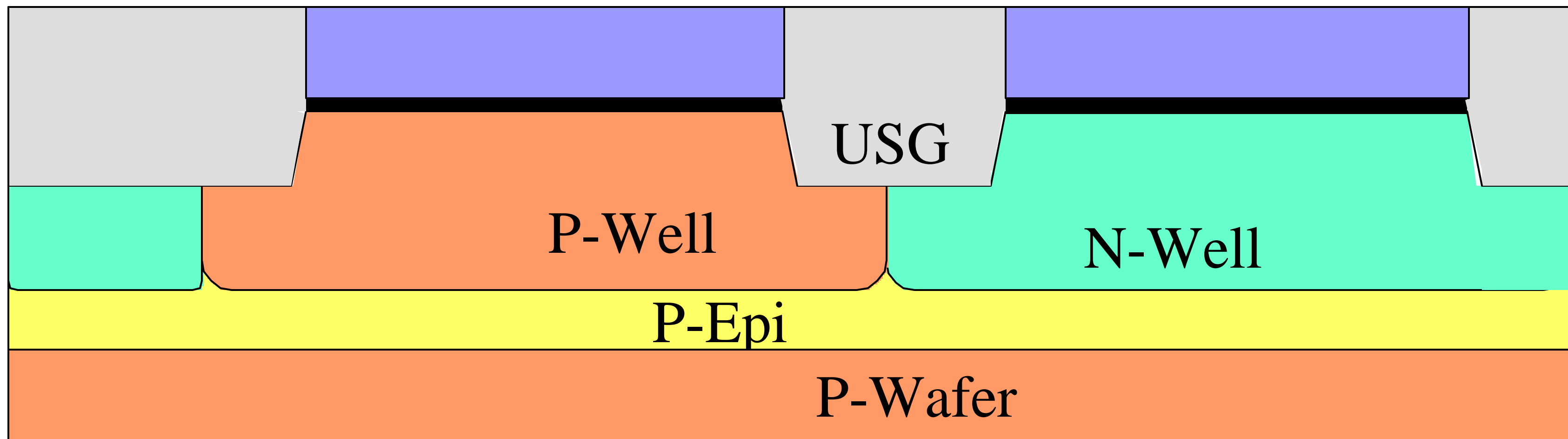
Etch Nitride, Pad Oxide and Silicon



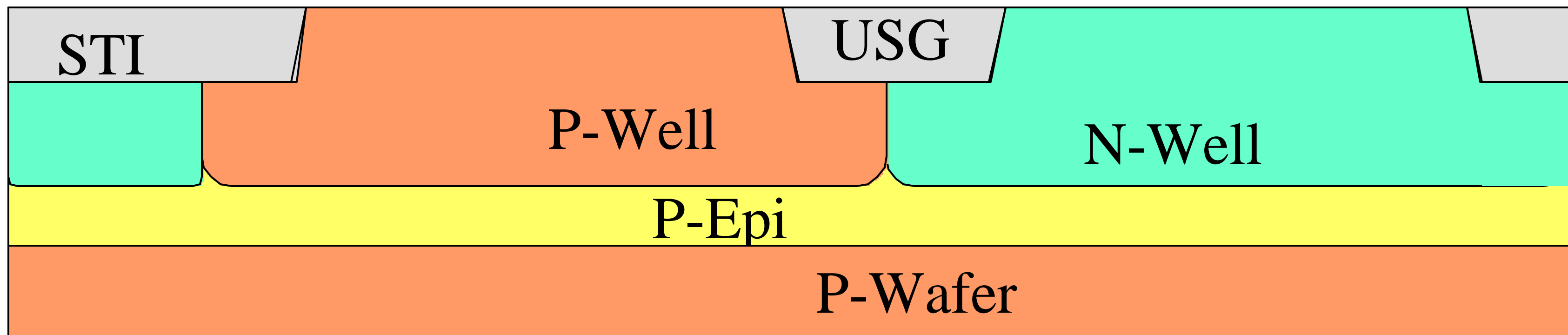
HDP-CVD USG Trench Fill



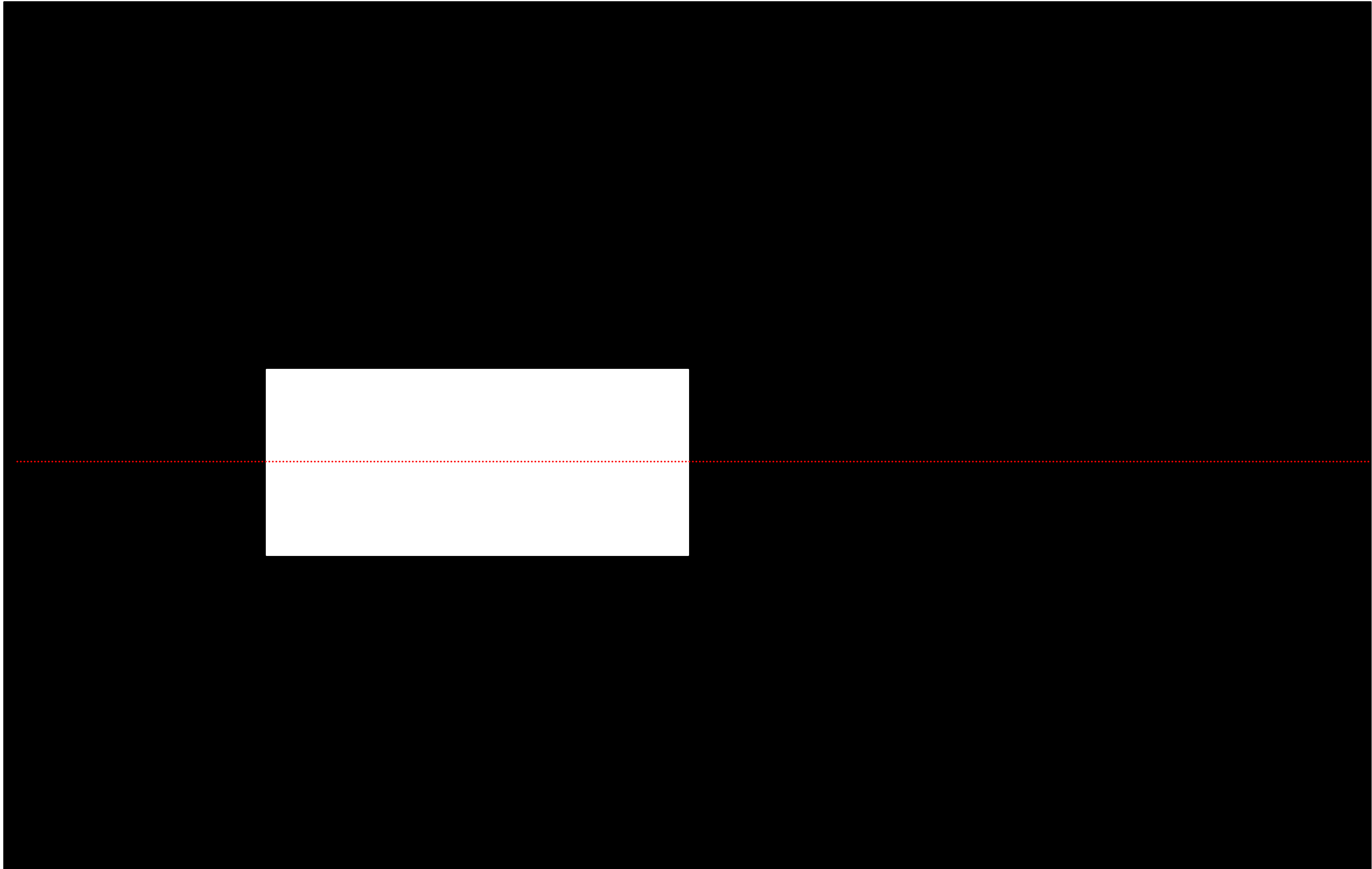
CMP USG, Stop on Nitride

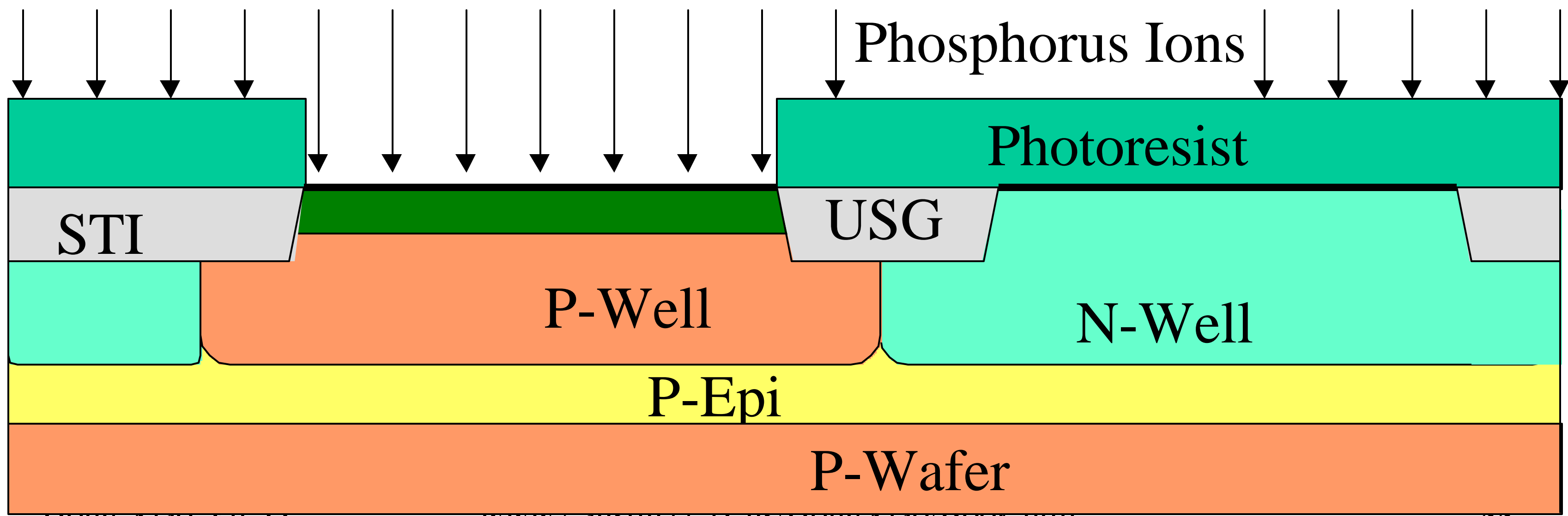


Strip Nitride and Pad Oxide, Clean

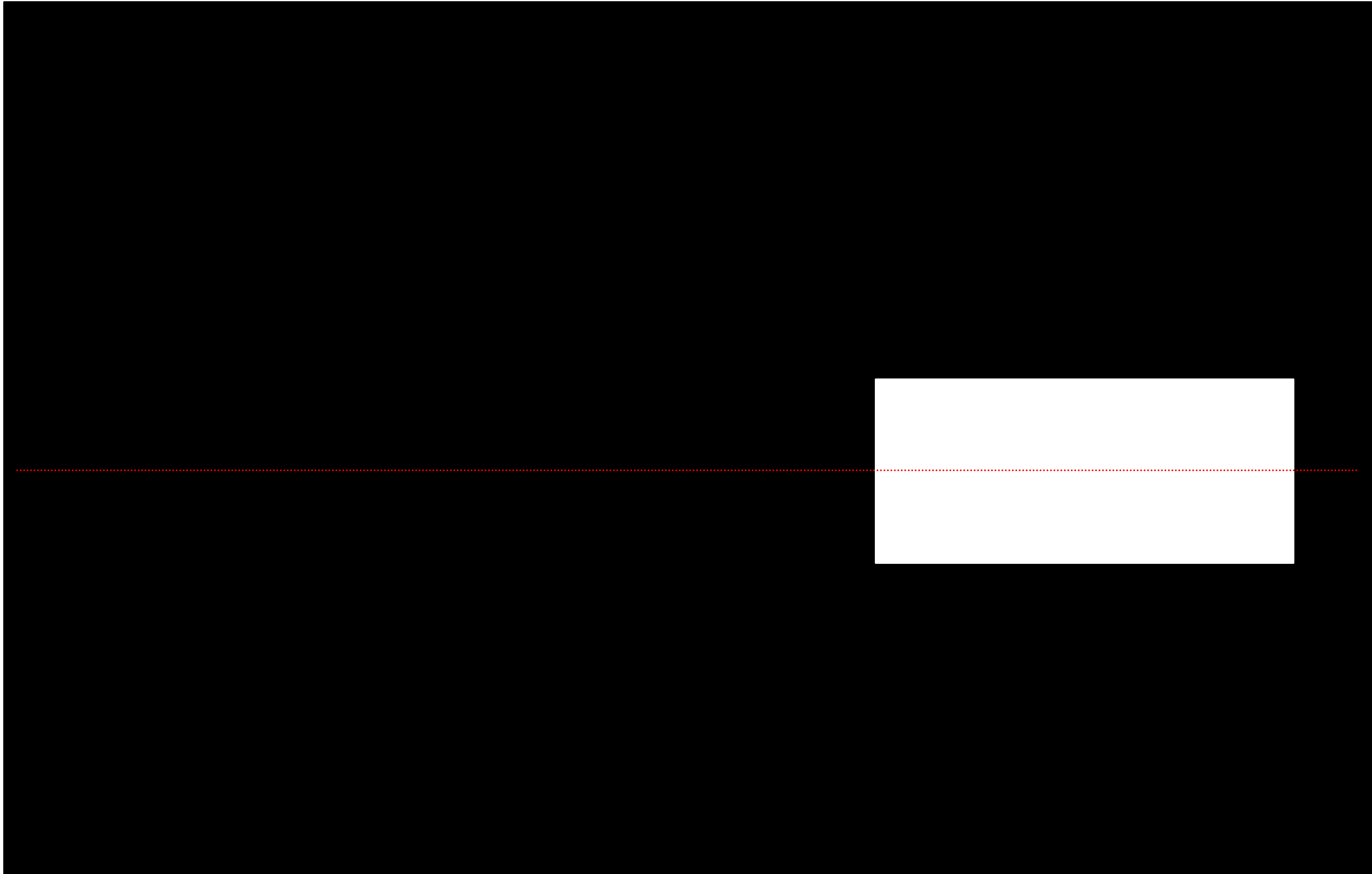


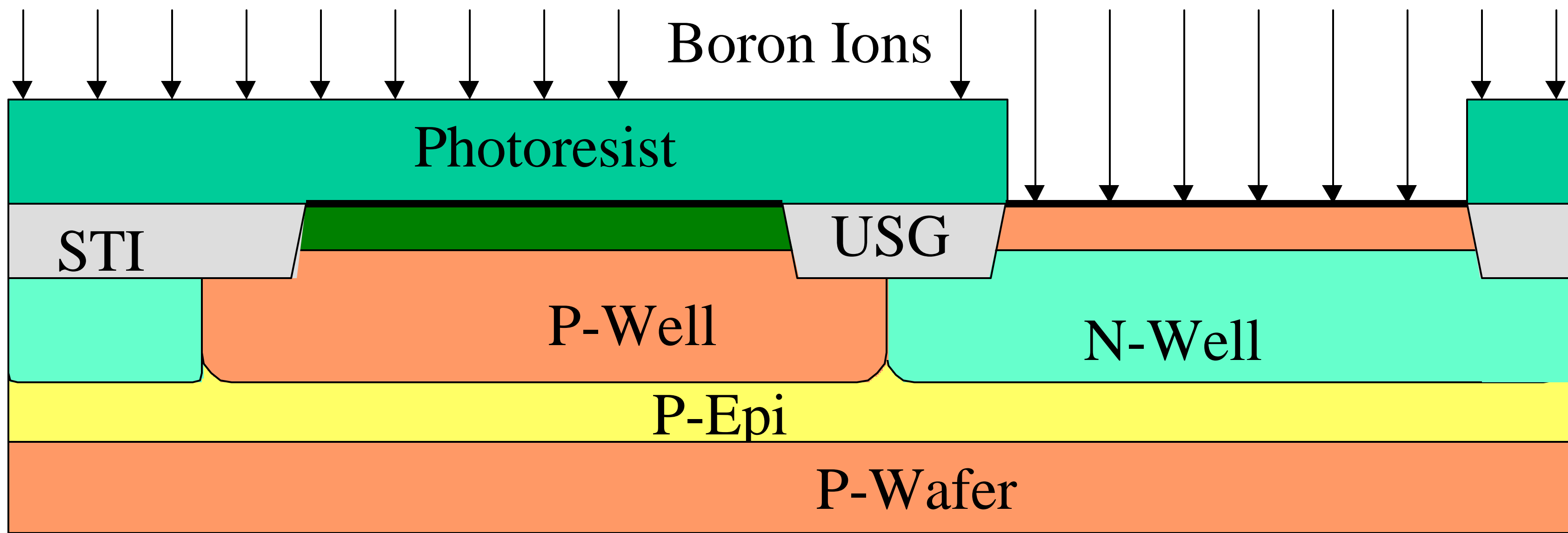
Mask 4: N-channel V_T Adjust



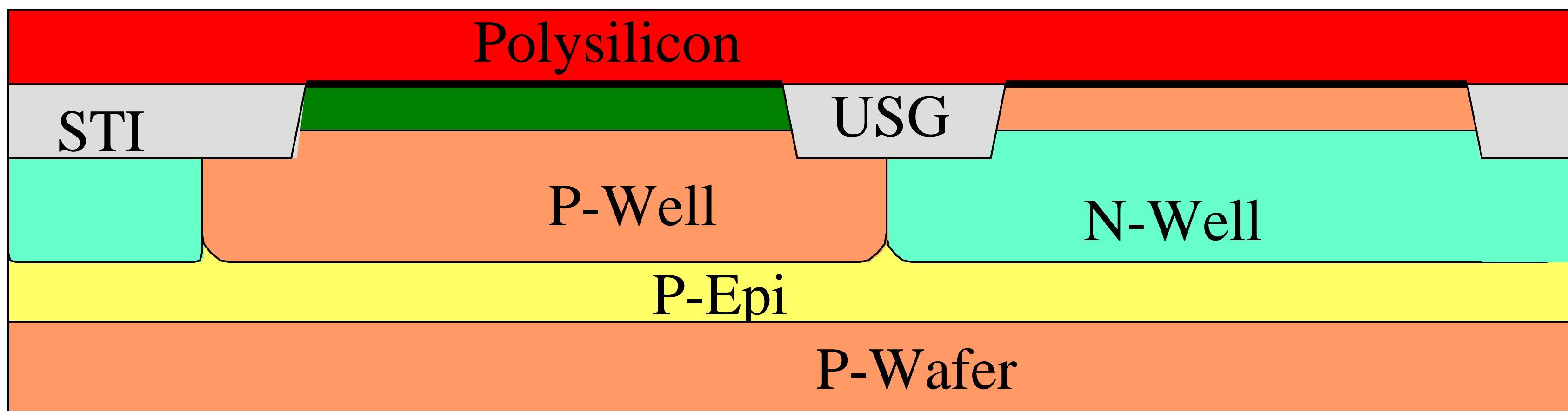

Phosphorus Ions
Photoresist
STI
USG
P-Well
N-Well
P-Epi
P-Wafer

Mask 5: P-channel V_T Adjust

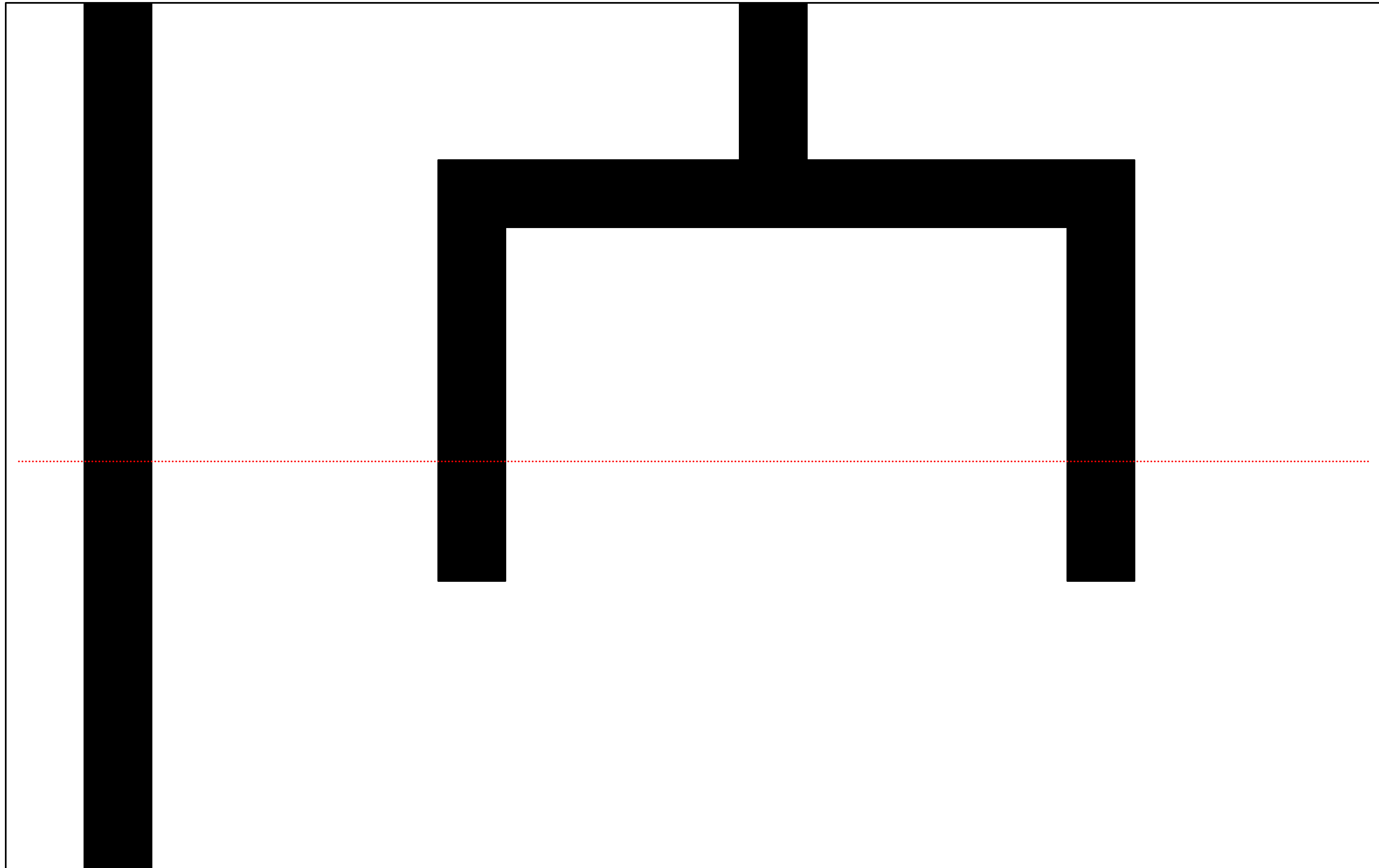



Boron Ions
Photoresist
STI
USG
P-Well
N-Well
P-Epi
P-Wafer

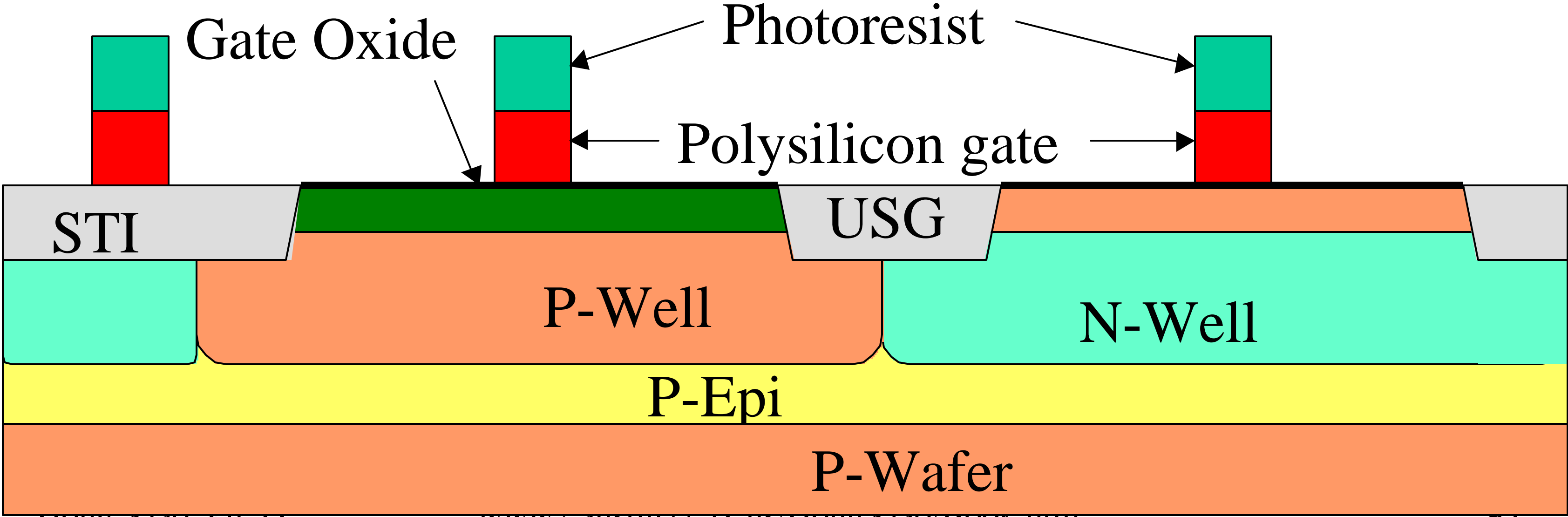
Gate Oxidation, LPCVD Polysilicon



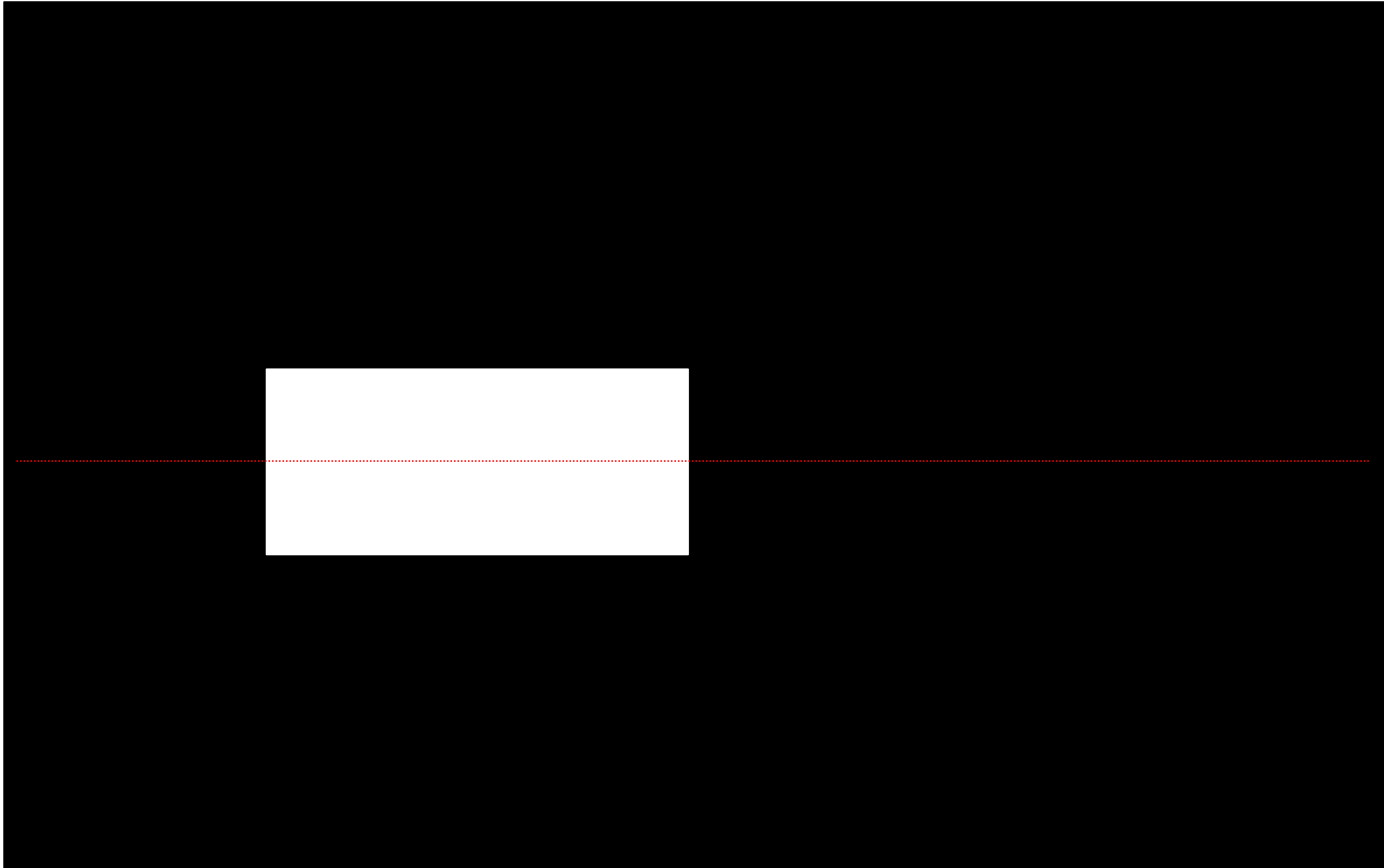
Mask 6: Gate & Local Interconnection



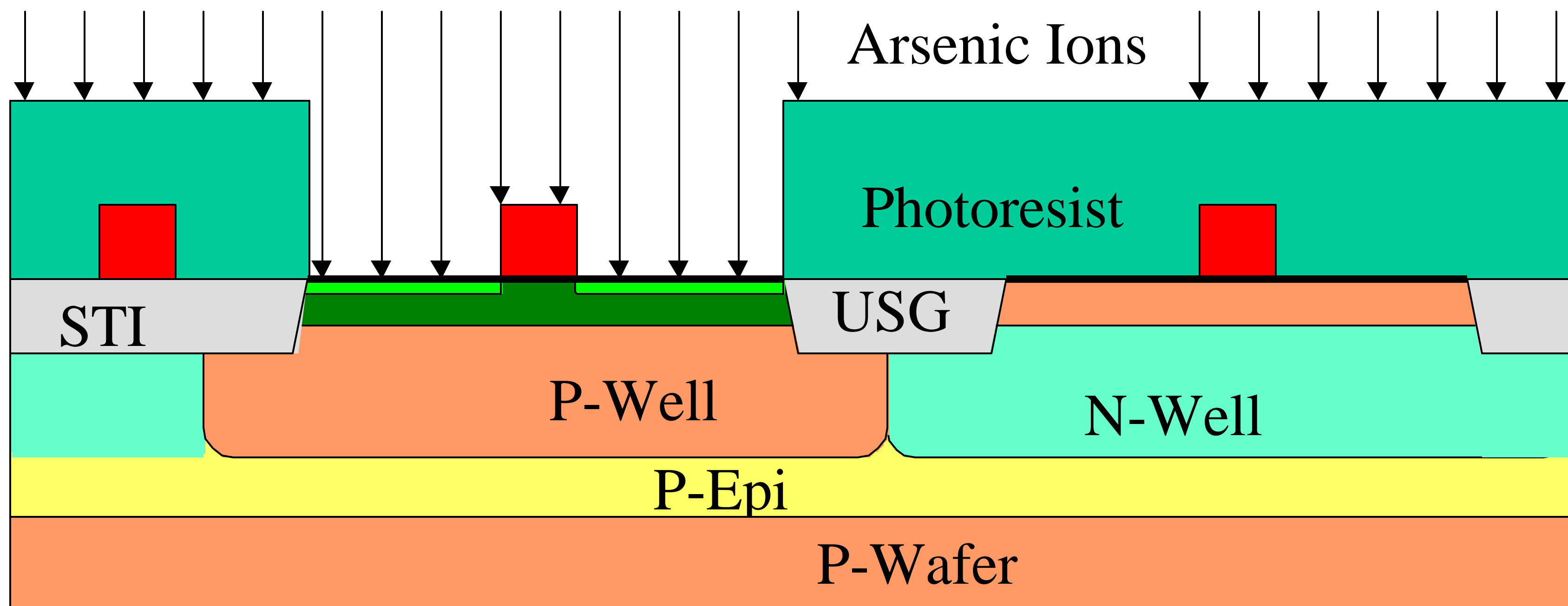
Etch Polysilicon



Mask 7: N-channel LDD

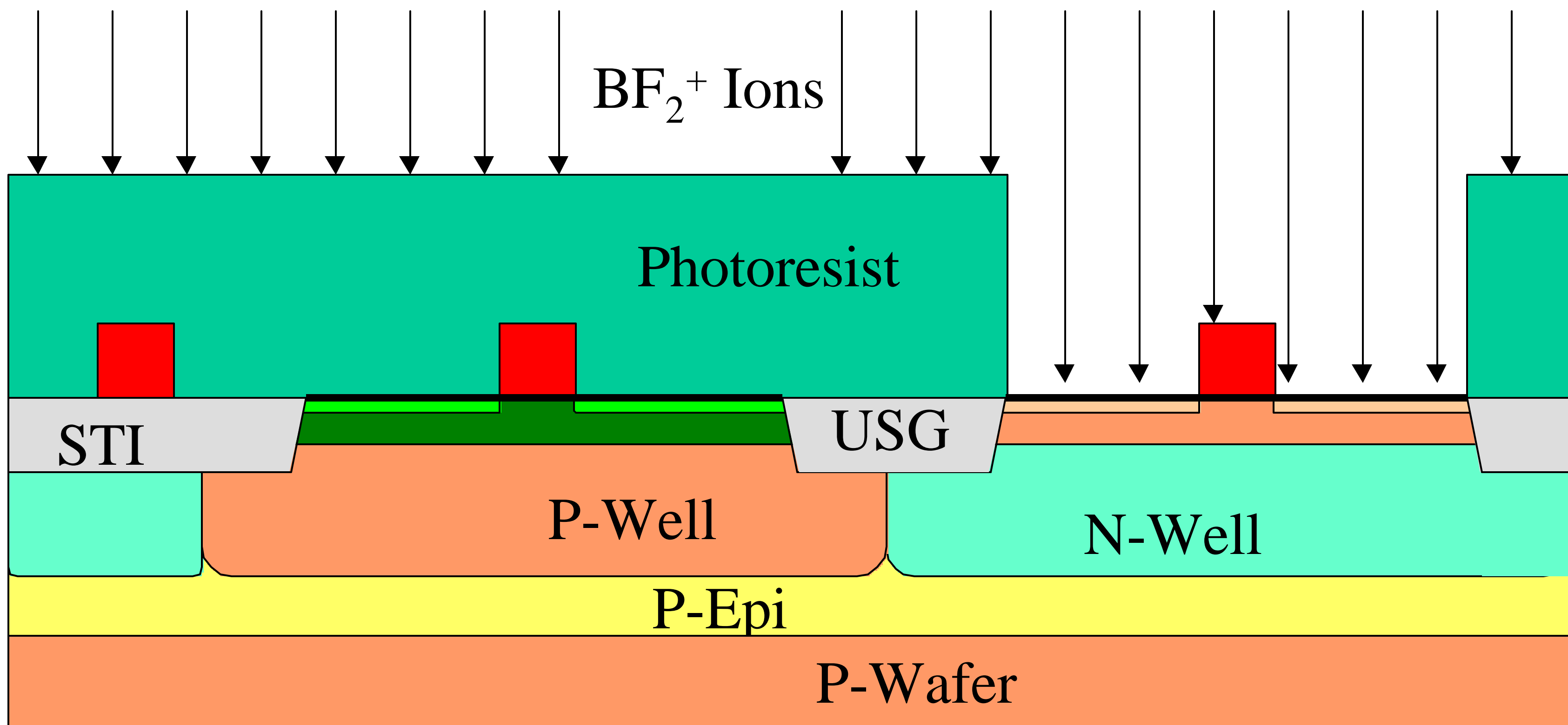


N-channel LDD Implantation, Arsenic

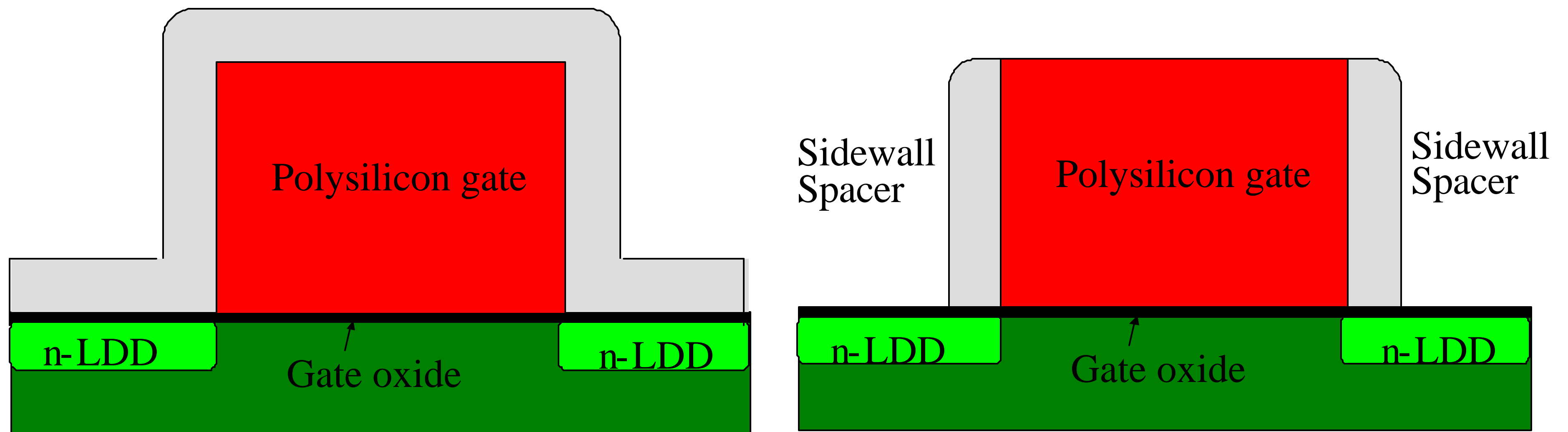


Mask 8: P-channel LDD

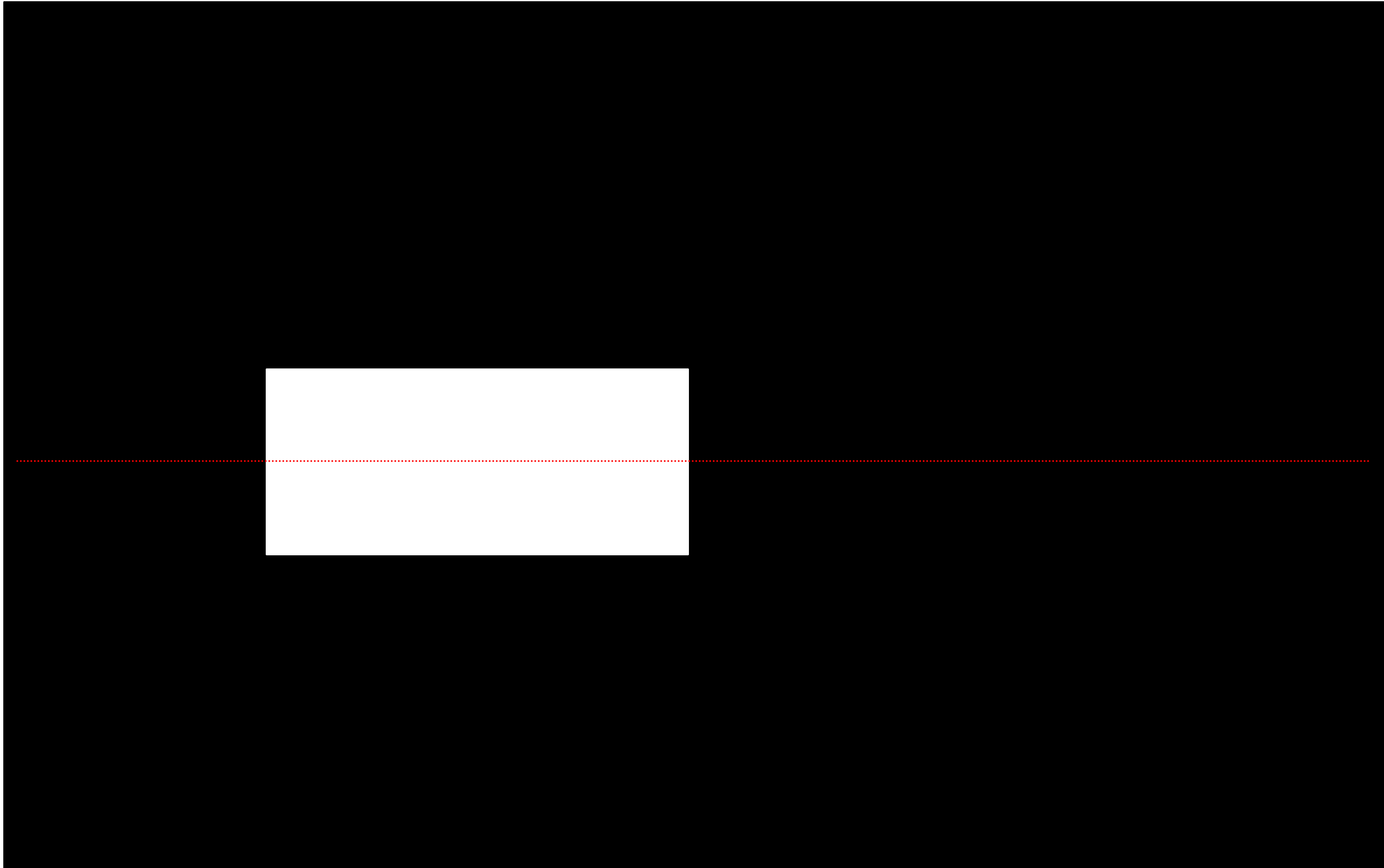
P-channel LDD Implantation, BF_2^+



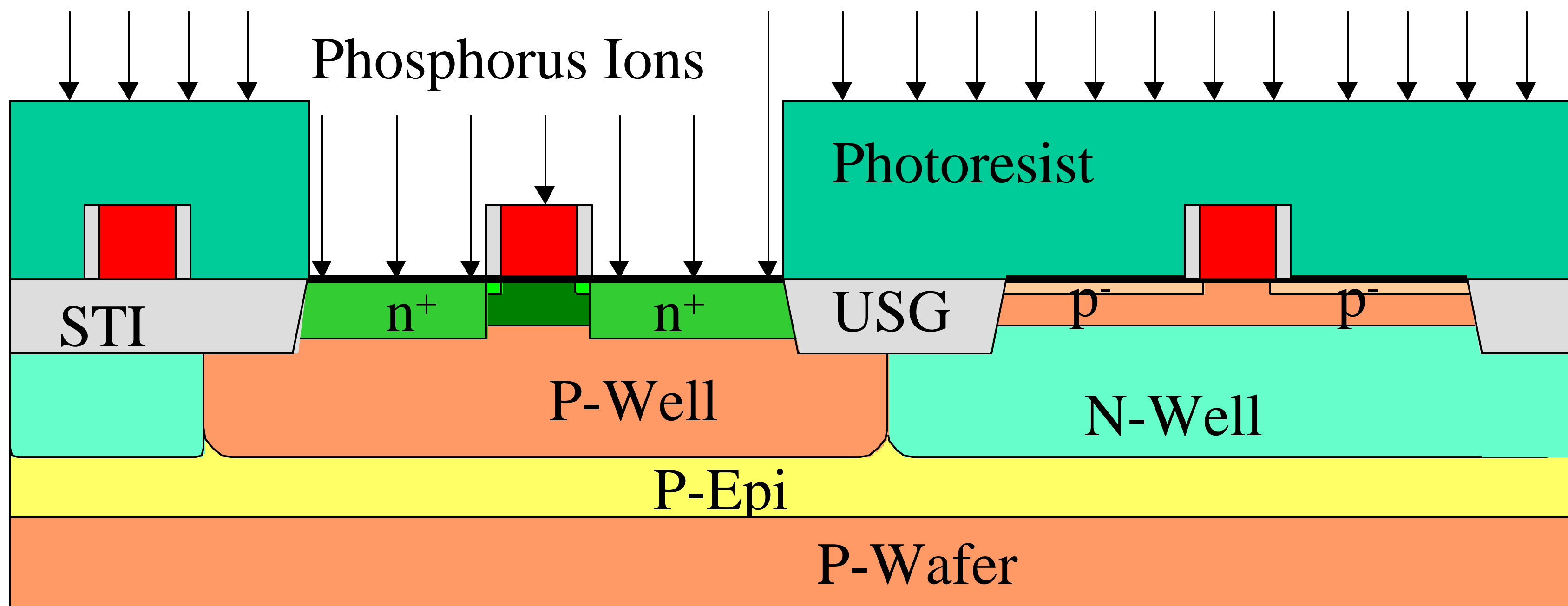
Sidewall Spacer



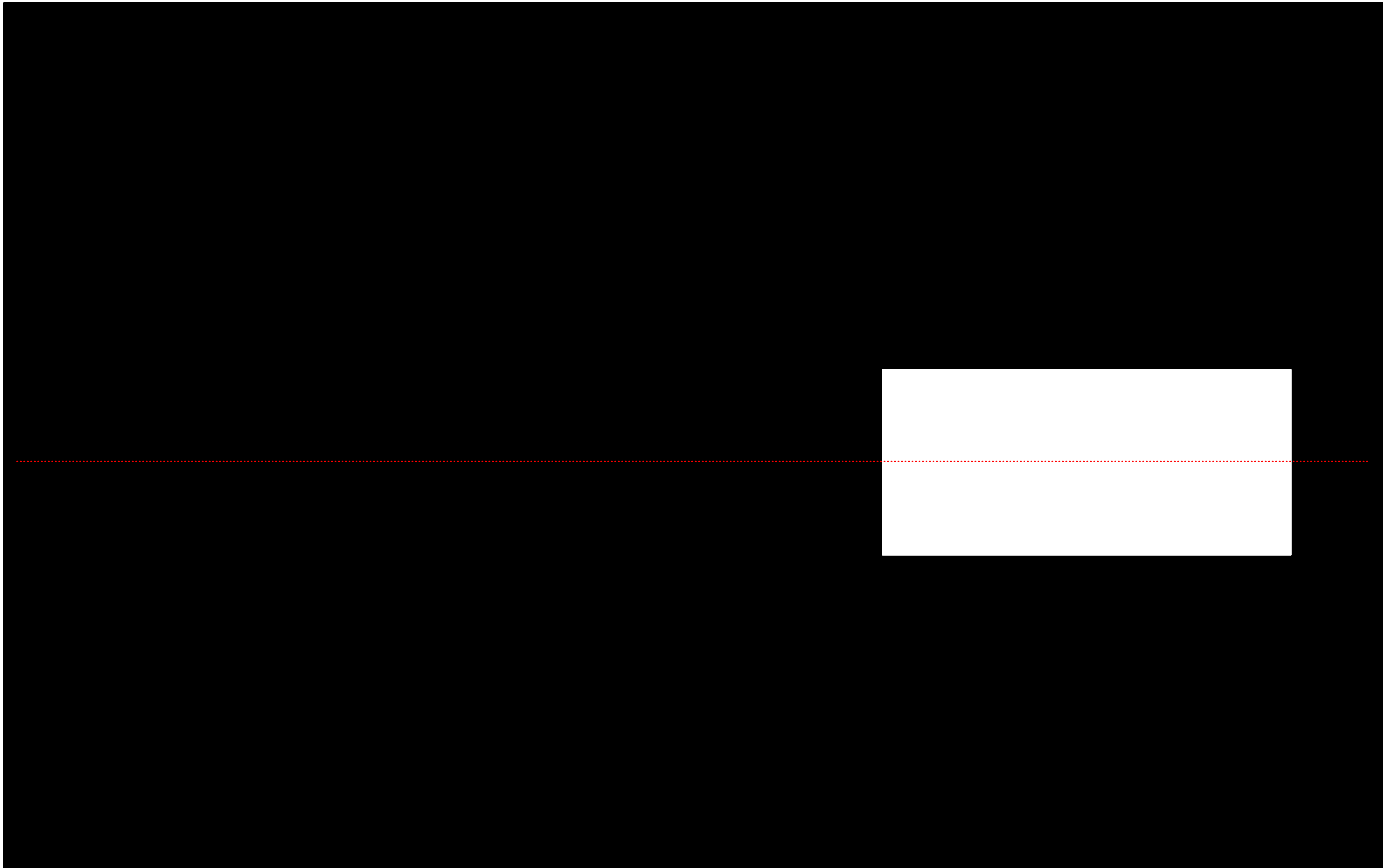
Mask 9: N-channel Source/Drain



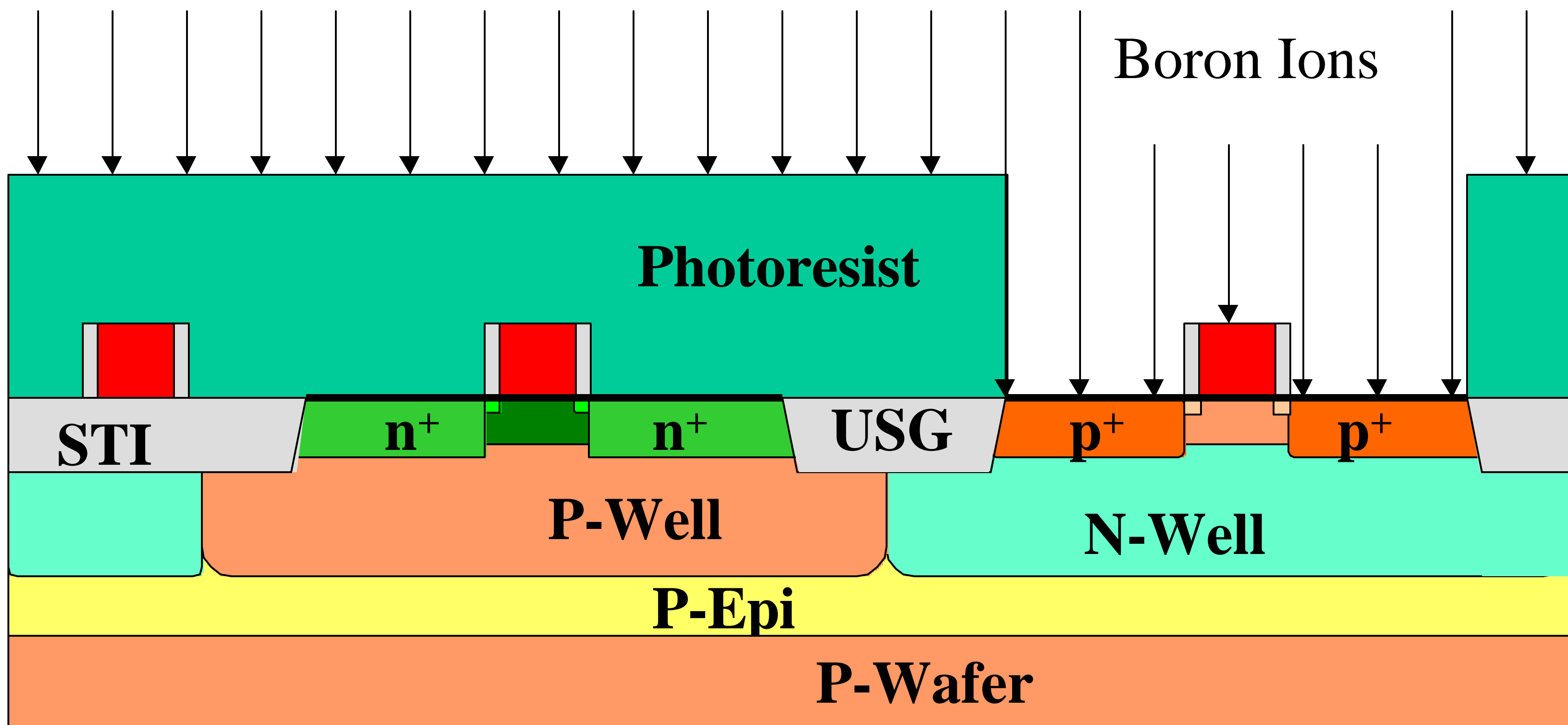
N-channel Source/Drain Implantation



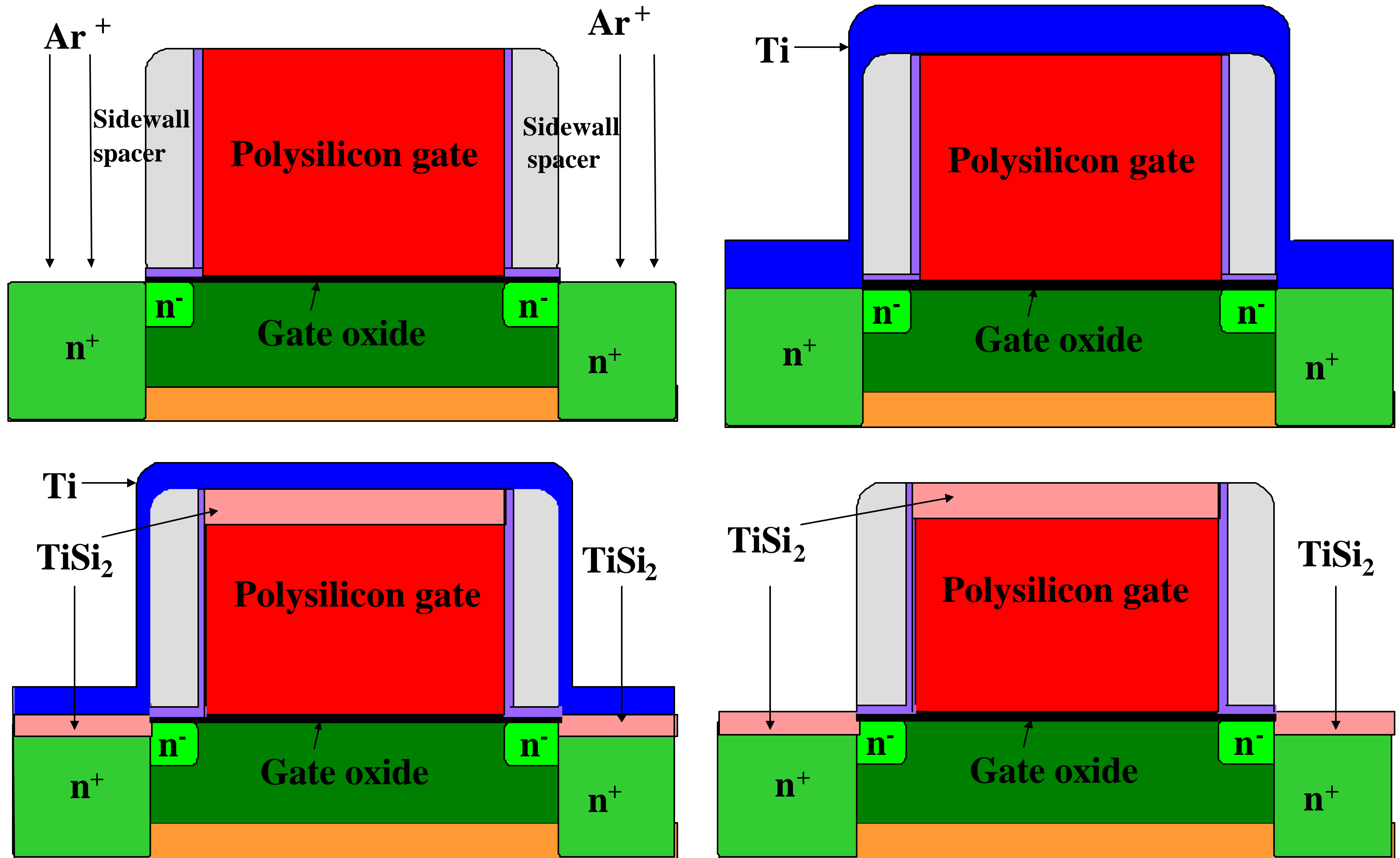
Mask 9: P-channel Source/Drain



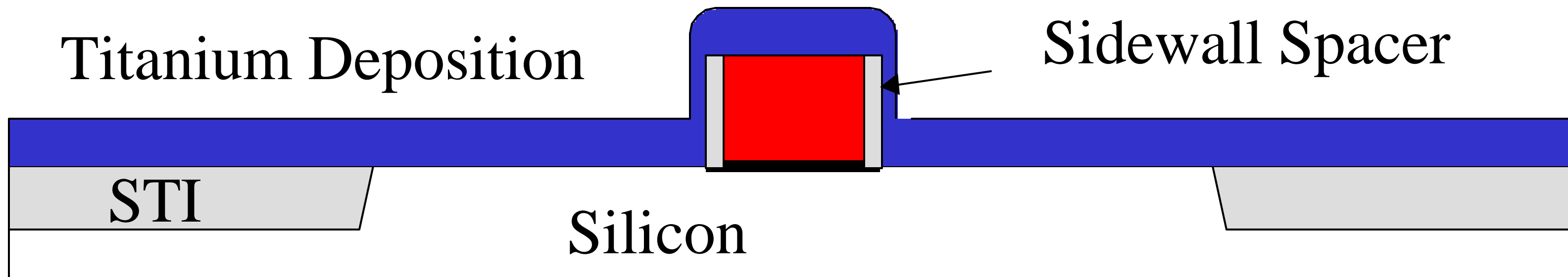
P-channel Source/Drain Implantation

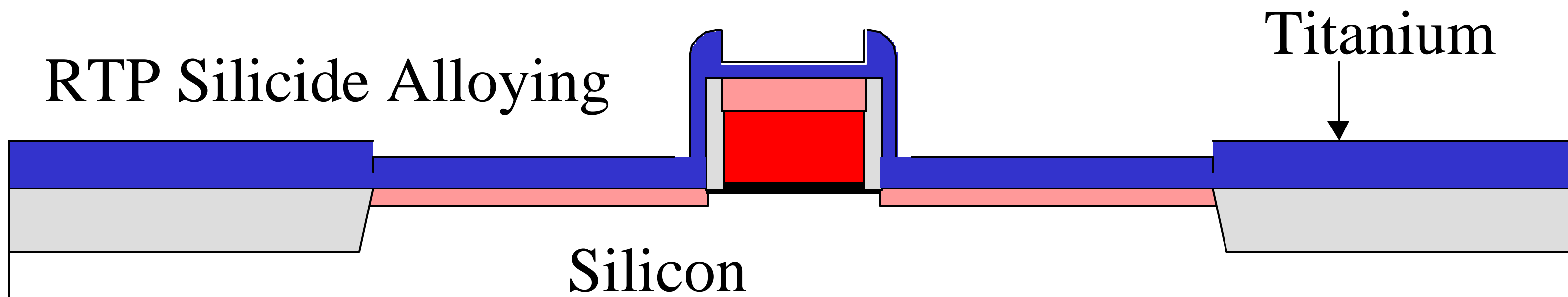


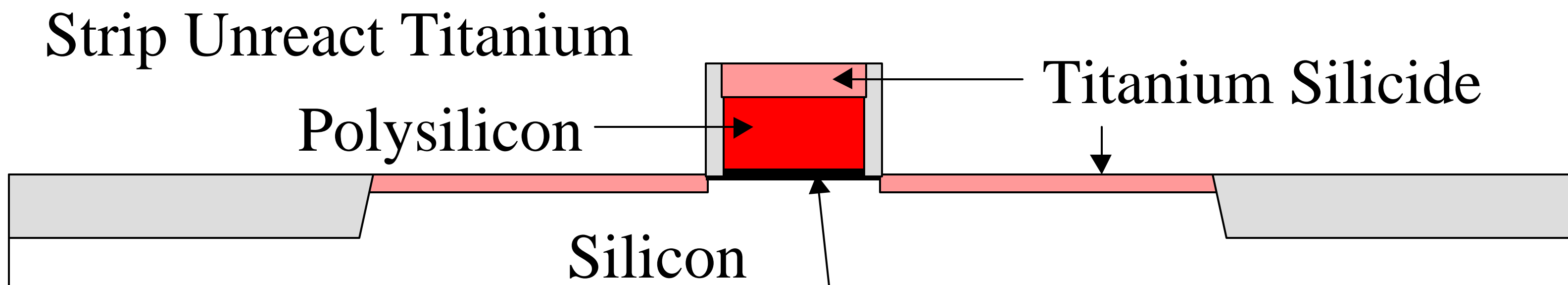
Titanium Salicide Process



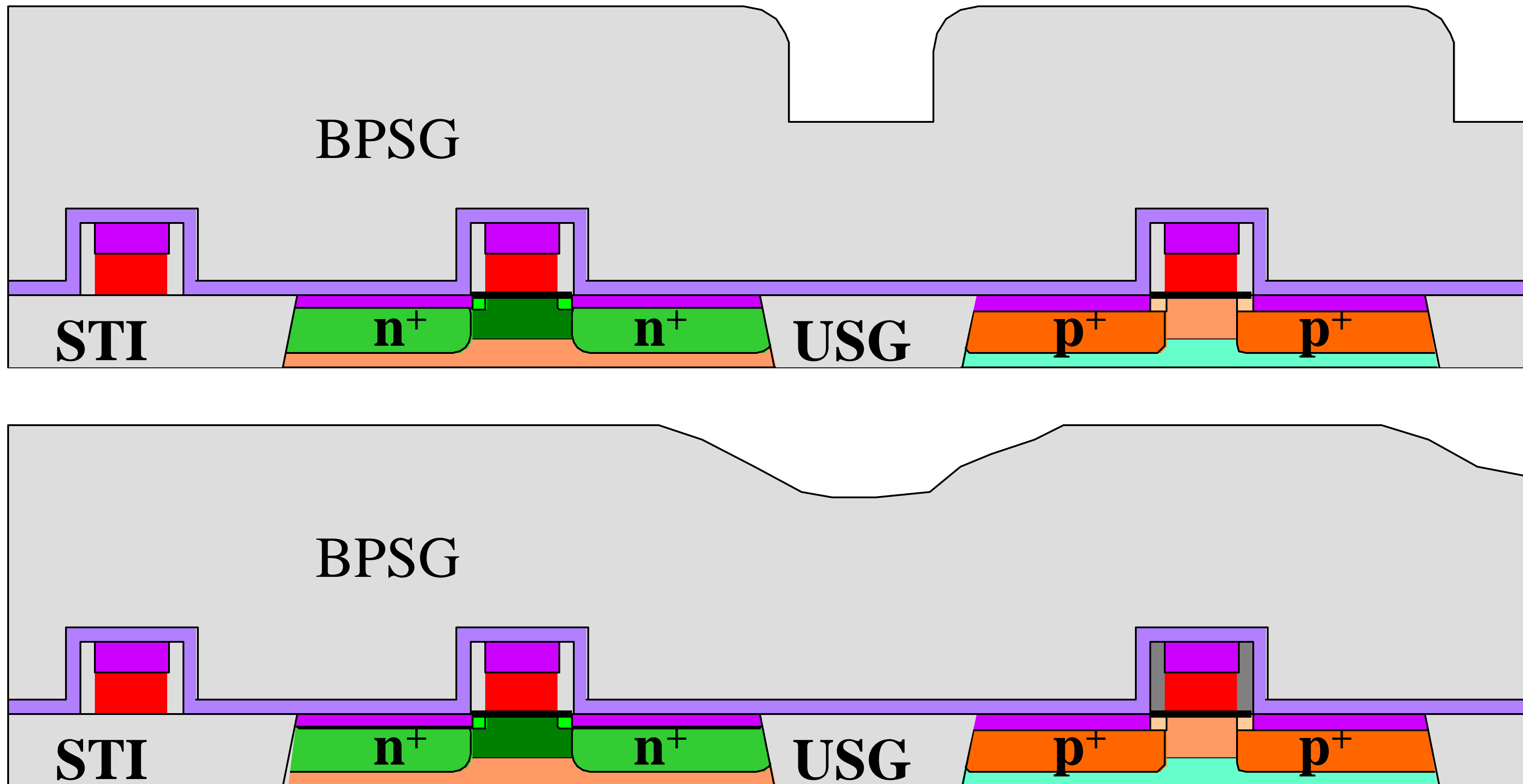
Titanium Self-aligned silicide Process



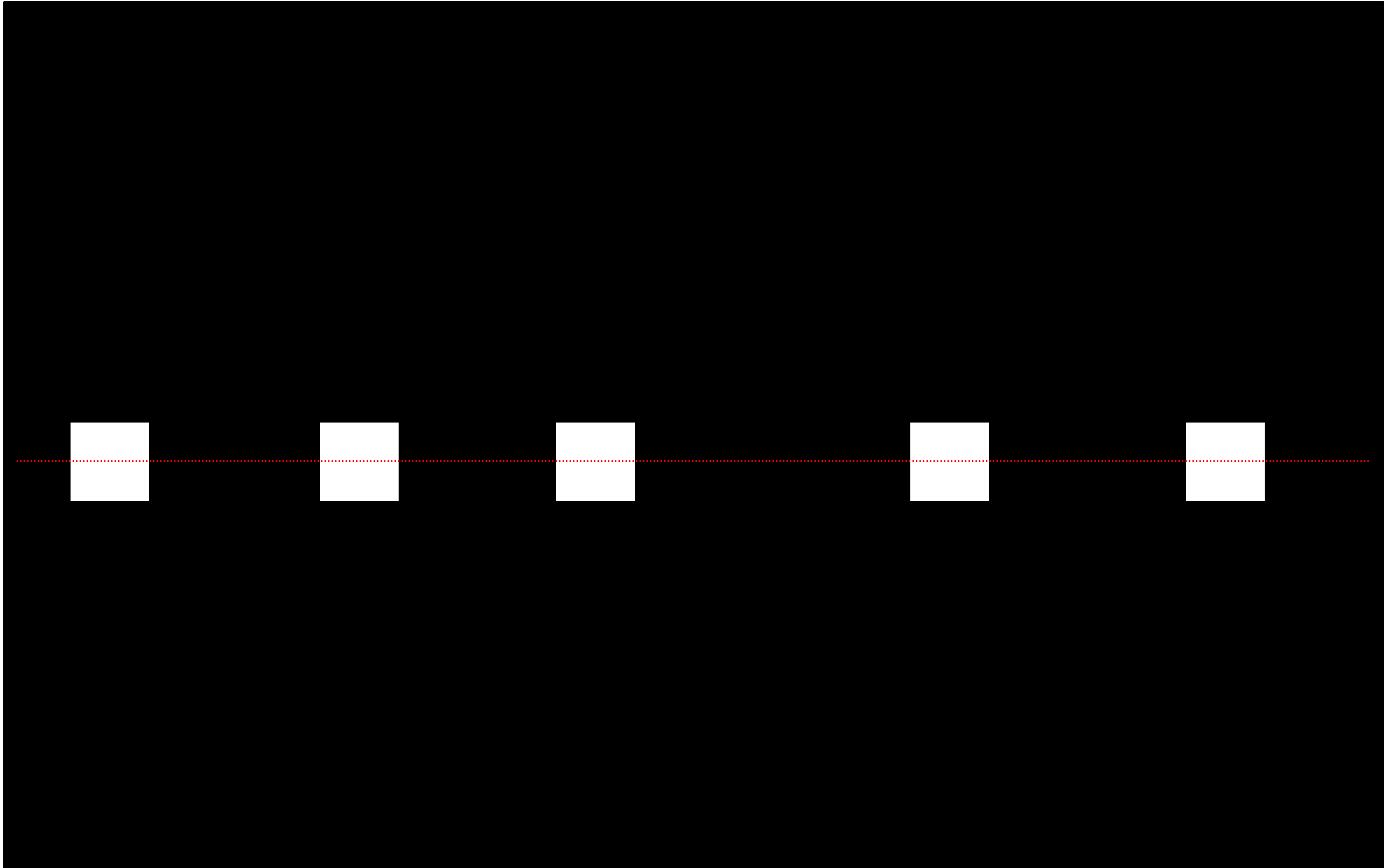




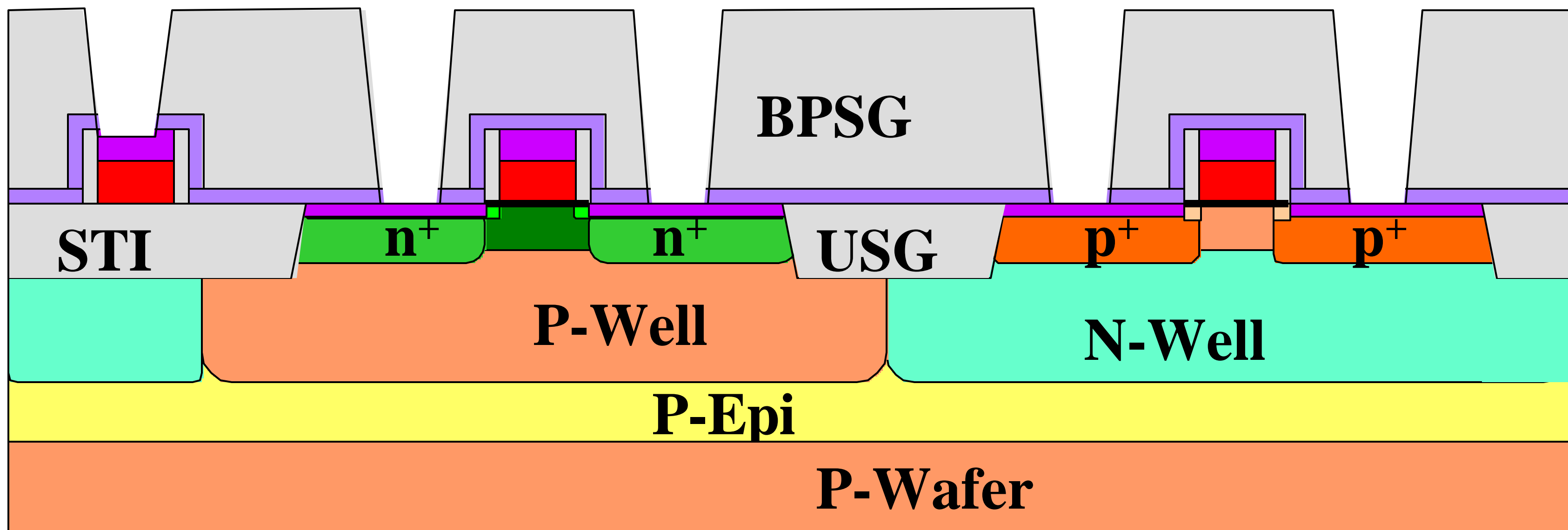
BPSG Deposition and Reflow



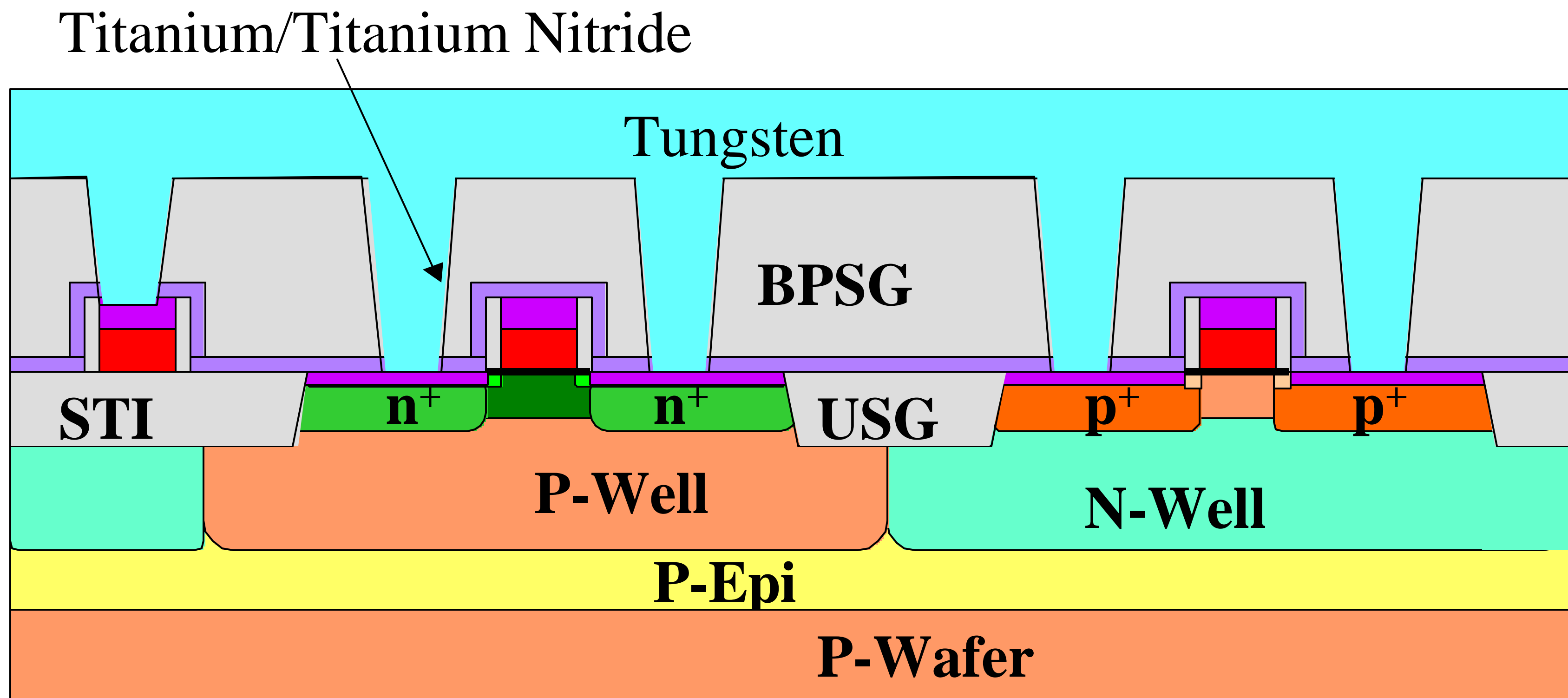
Mask 10: Contact Hole



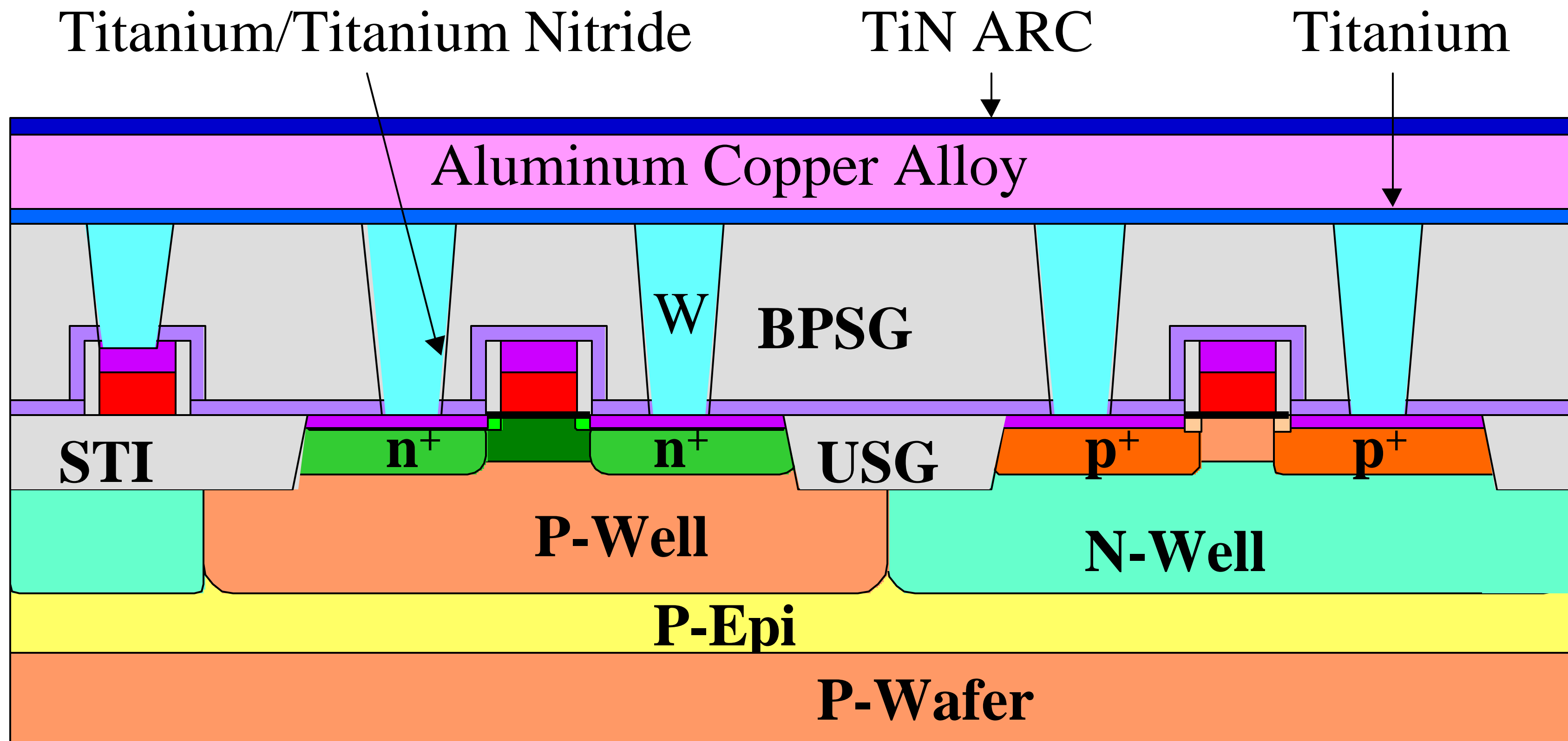
Contact Hole Etch, BPSG Etch



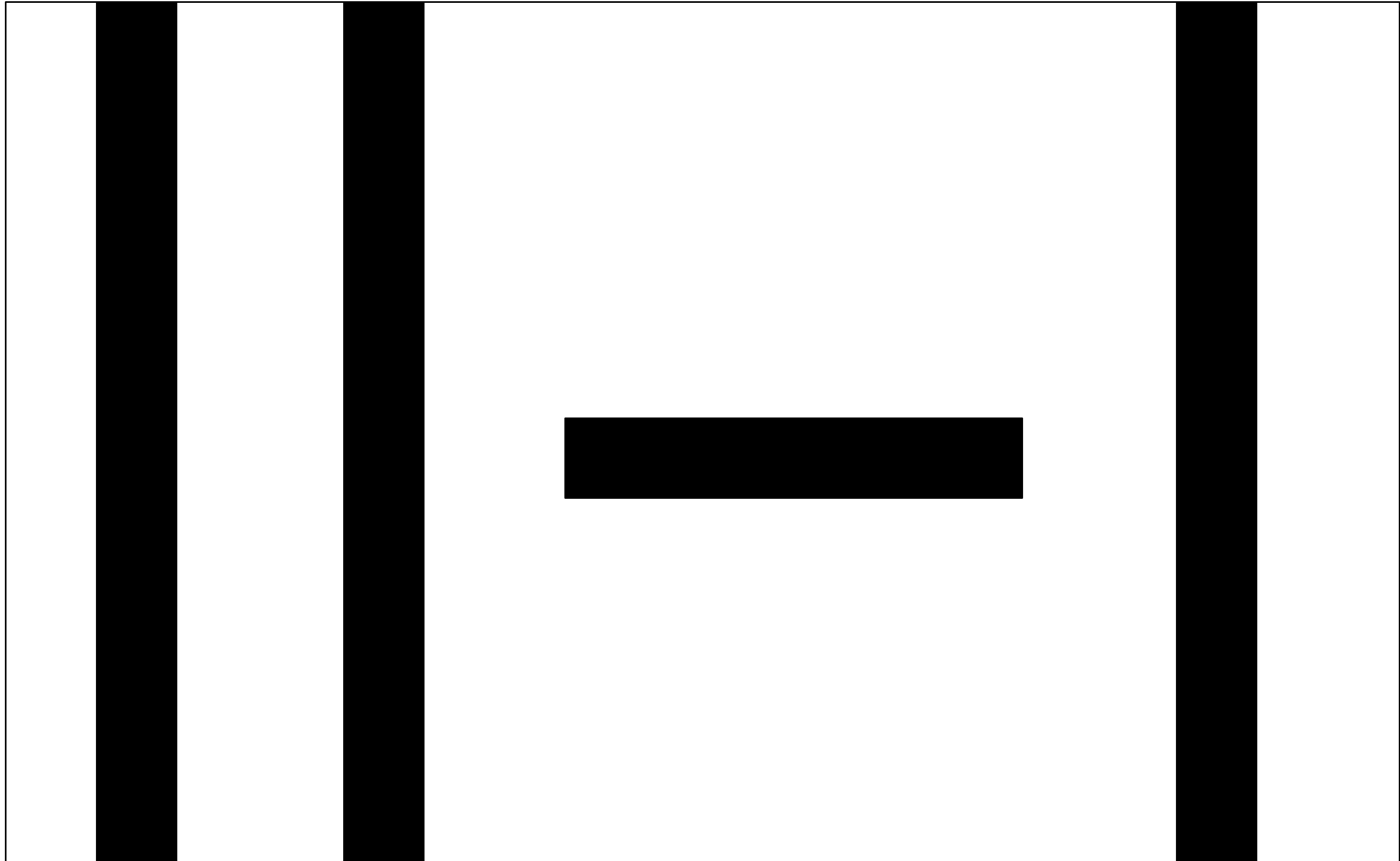
Contact Hole Etch, BPSG Etch



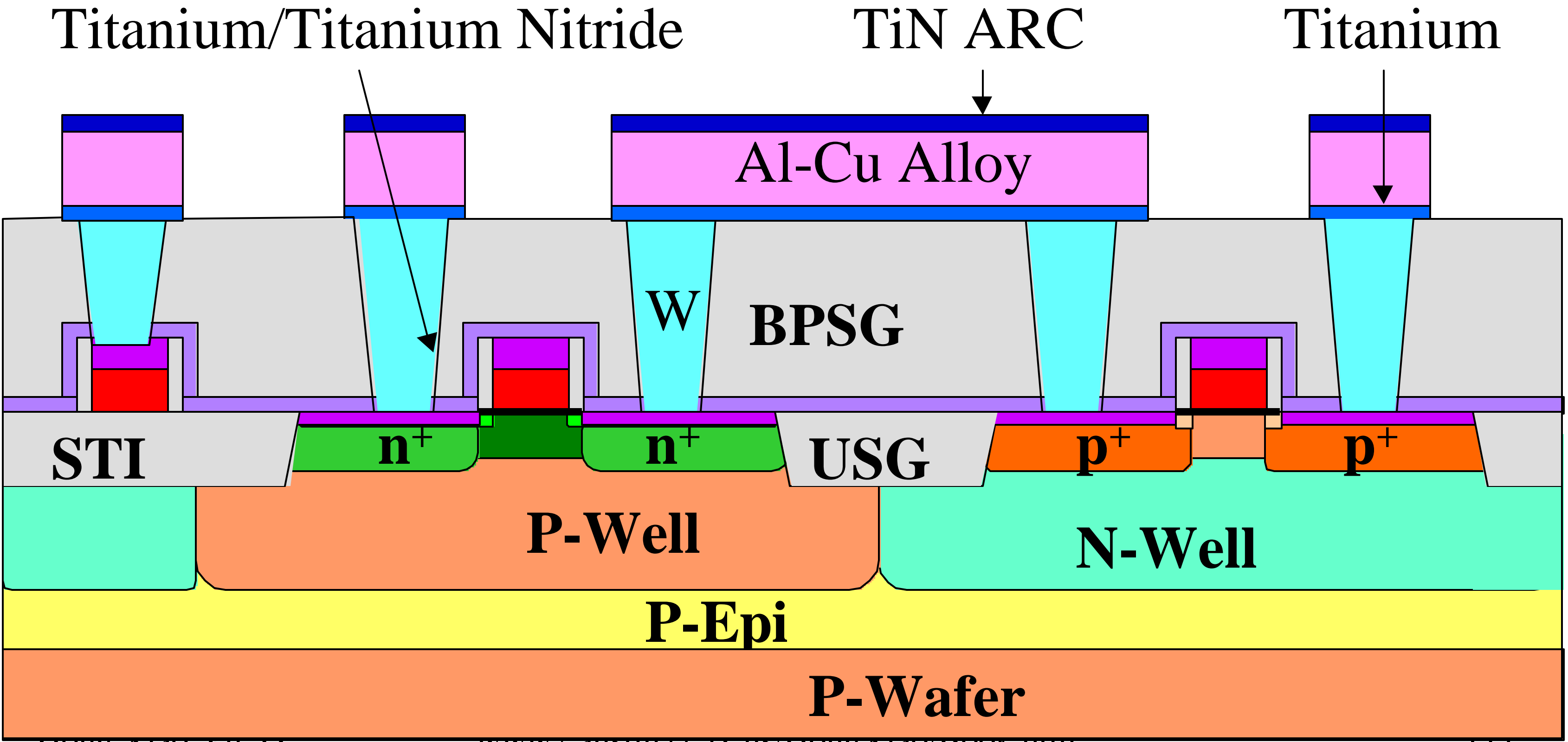
Contact Hole Etch, BPSG Etch



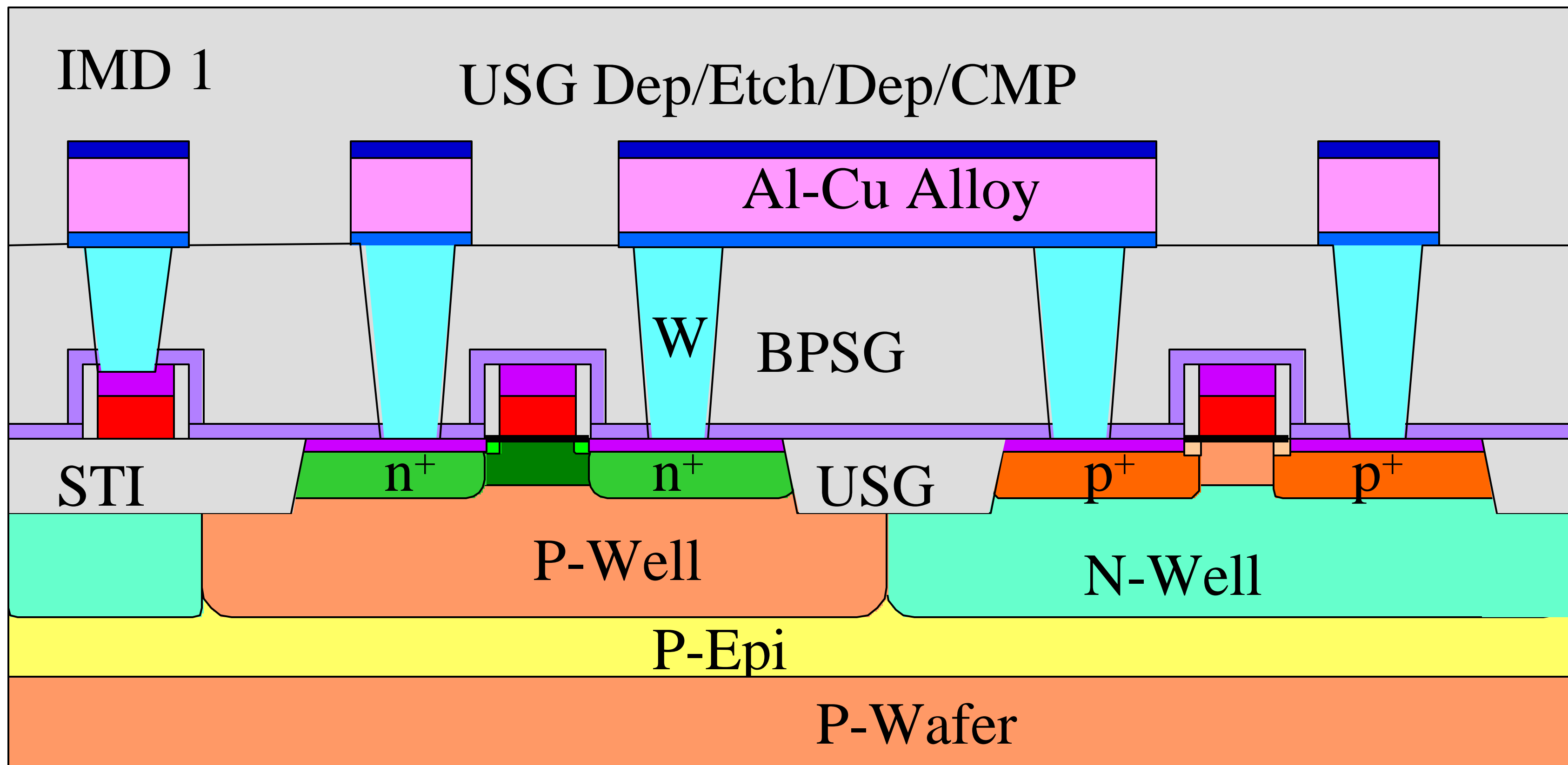
Mask 11: Metal 1 Interconnect



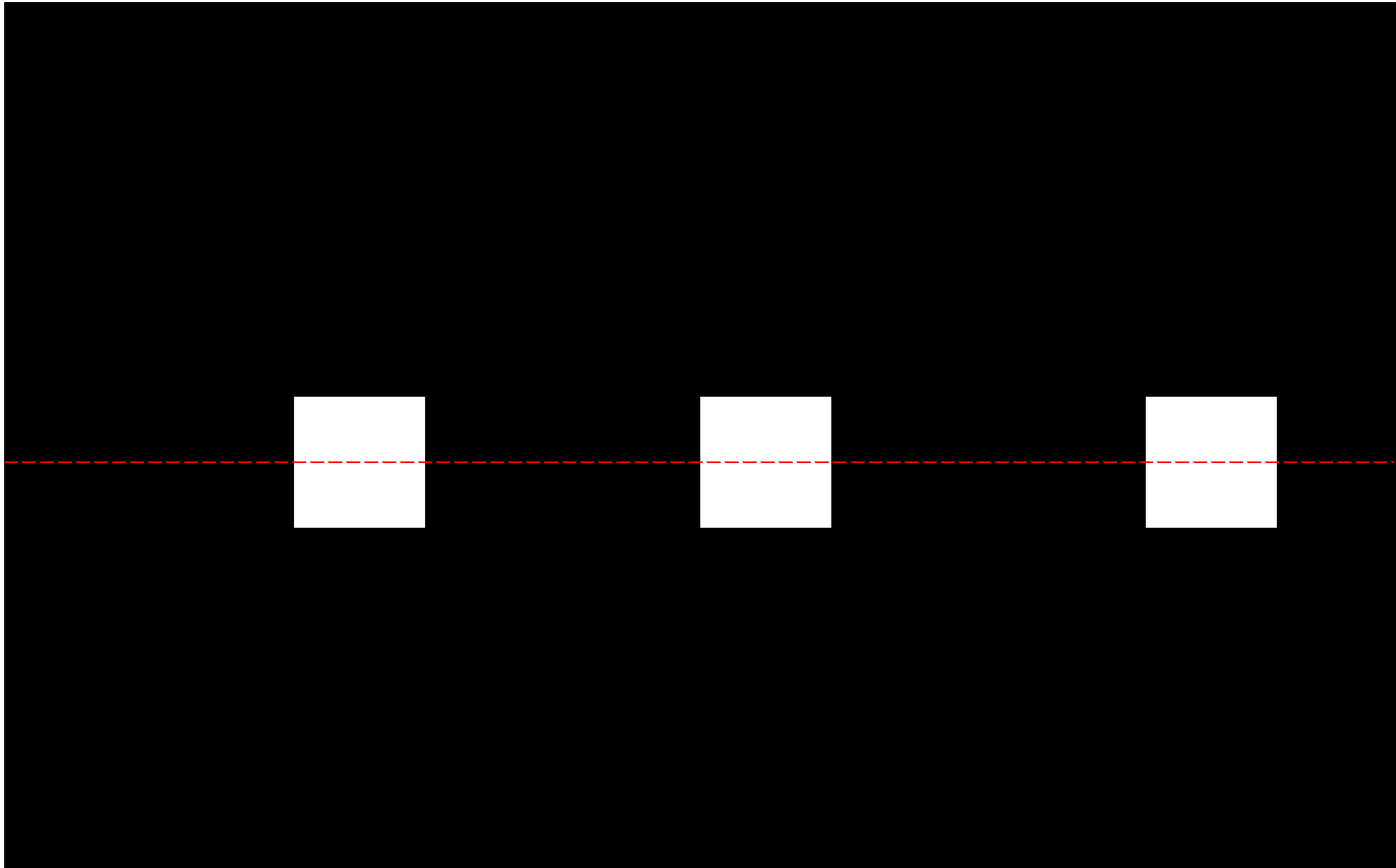
Metal Etch



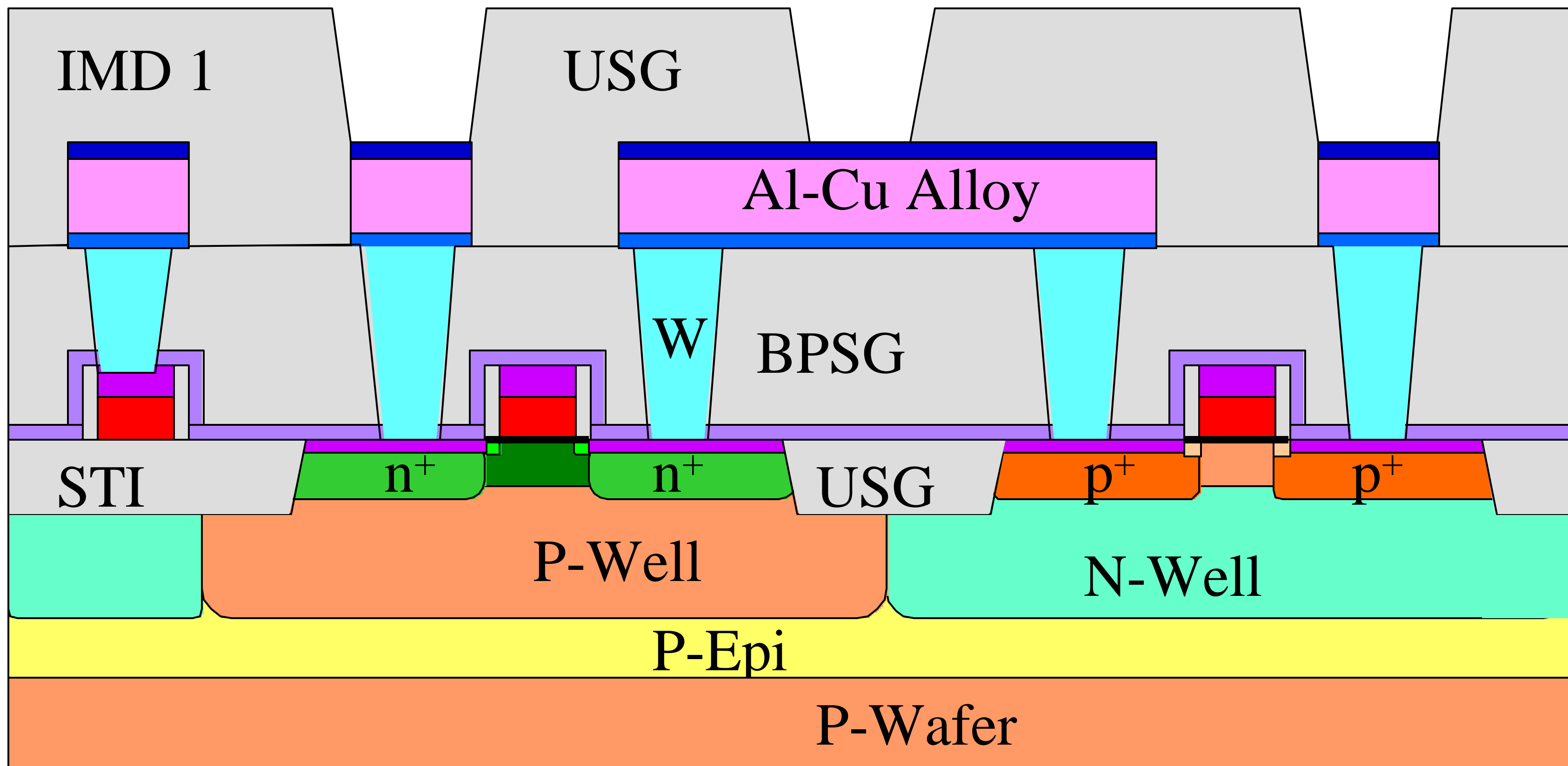
PE-TEOS USG Dep/Etch/Dep/CMP



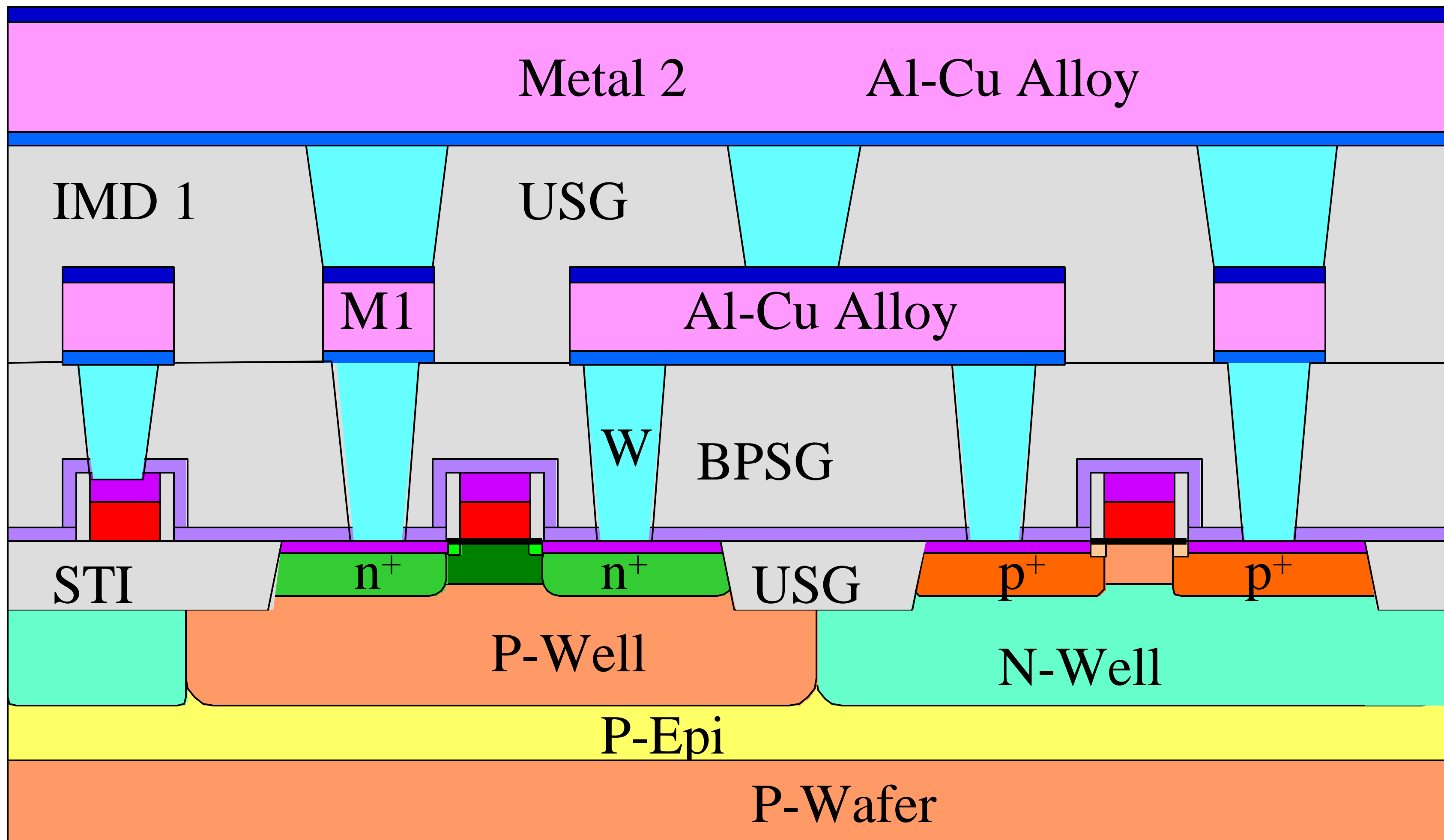
Mask 12: Via 1



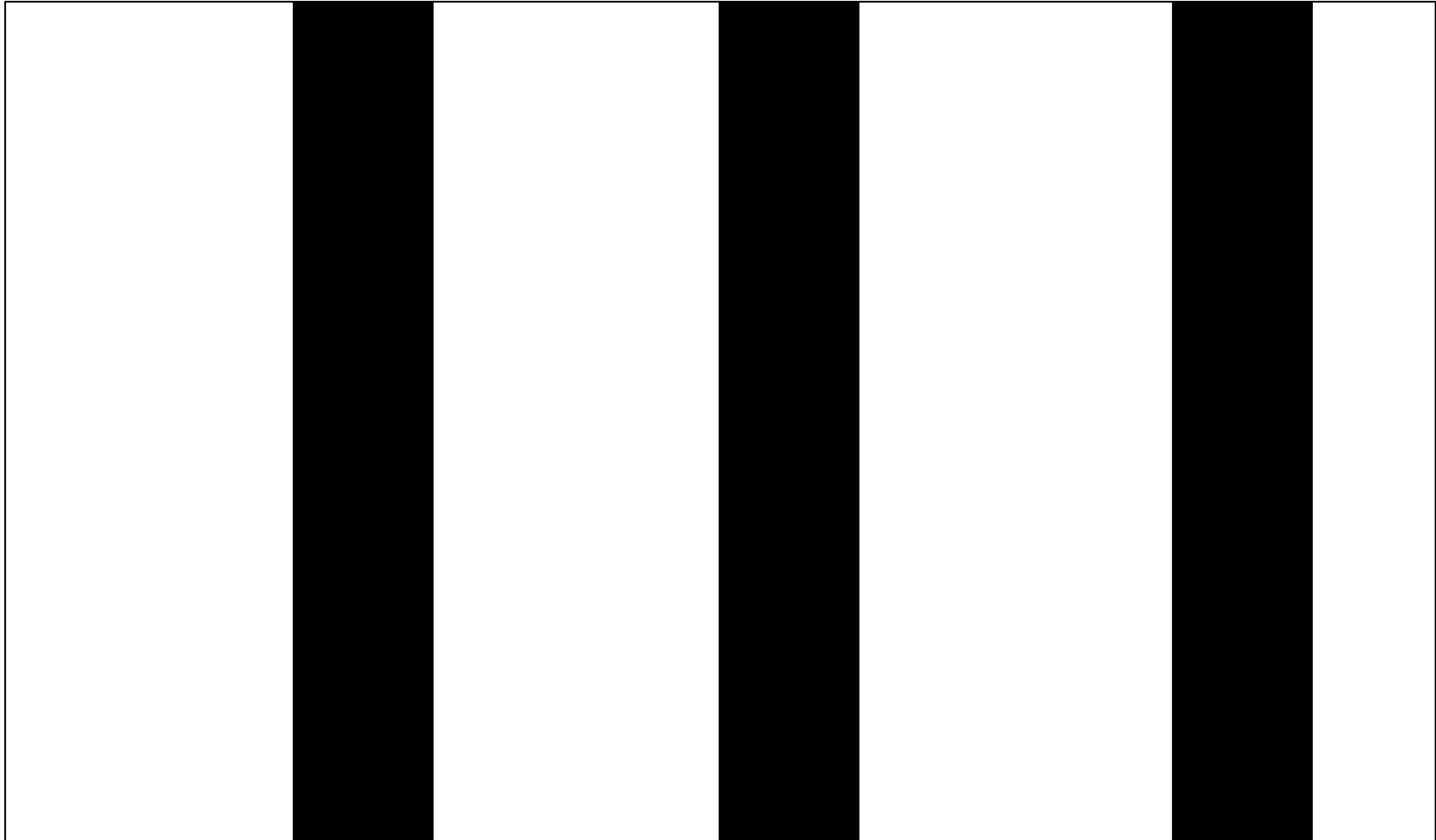
Via Etch, Etch USG



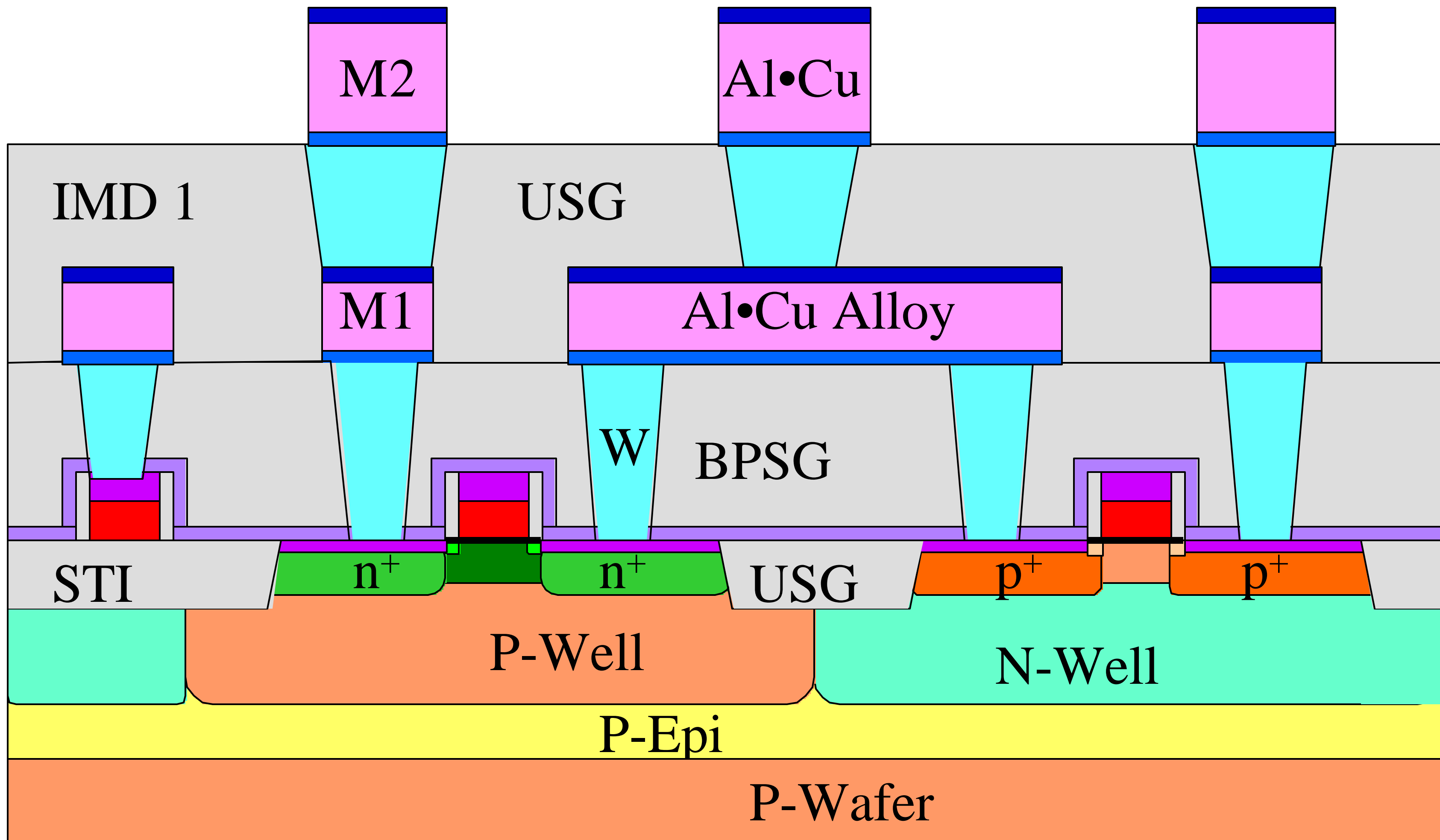
Via Etch, Etch USG



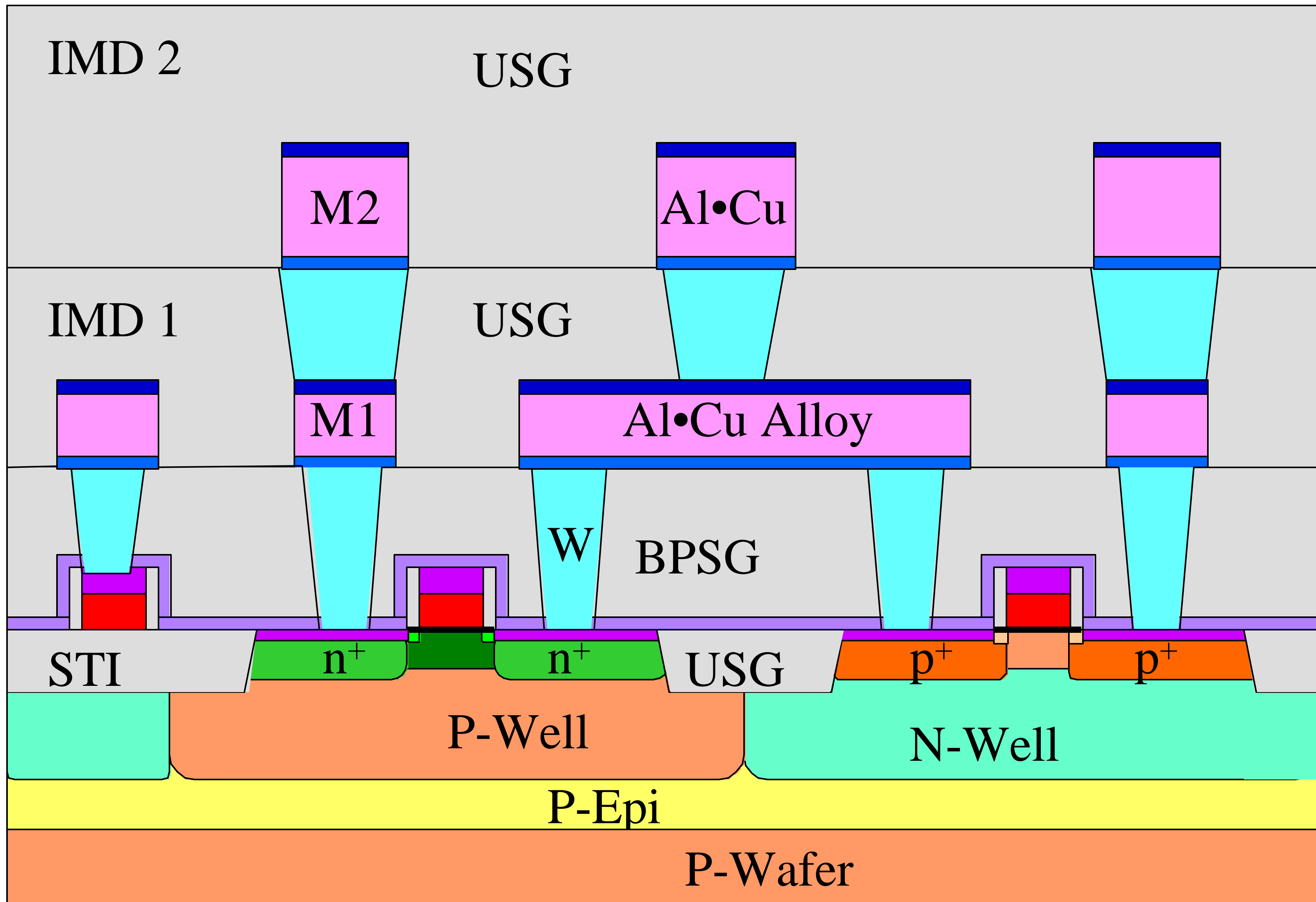
Mask 13: Metal 2 Interconnect



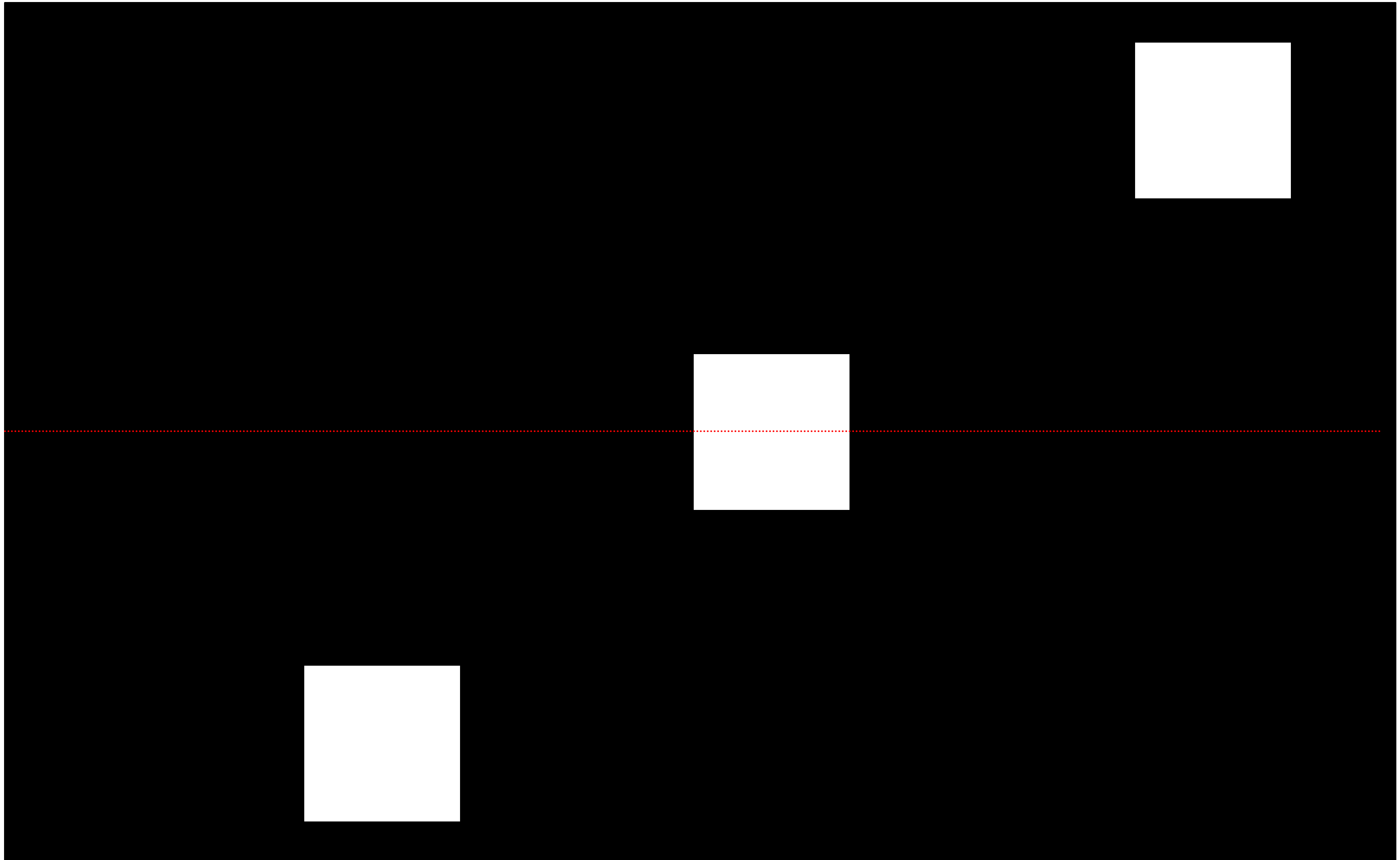
Etch Metal 2



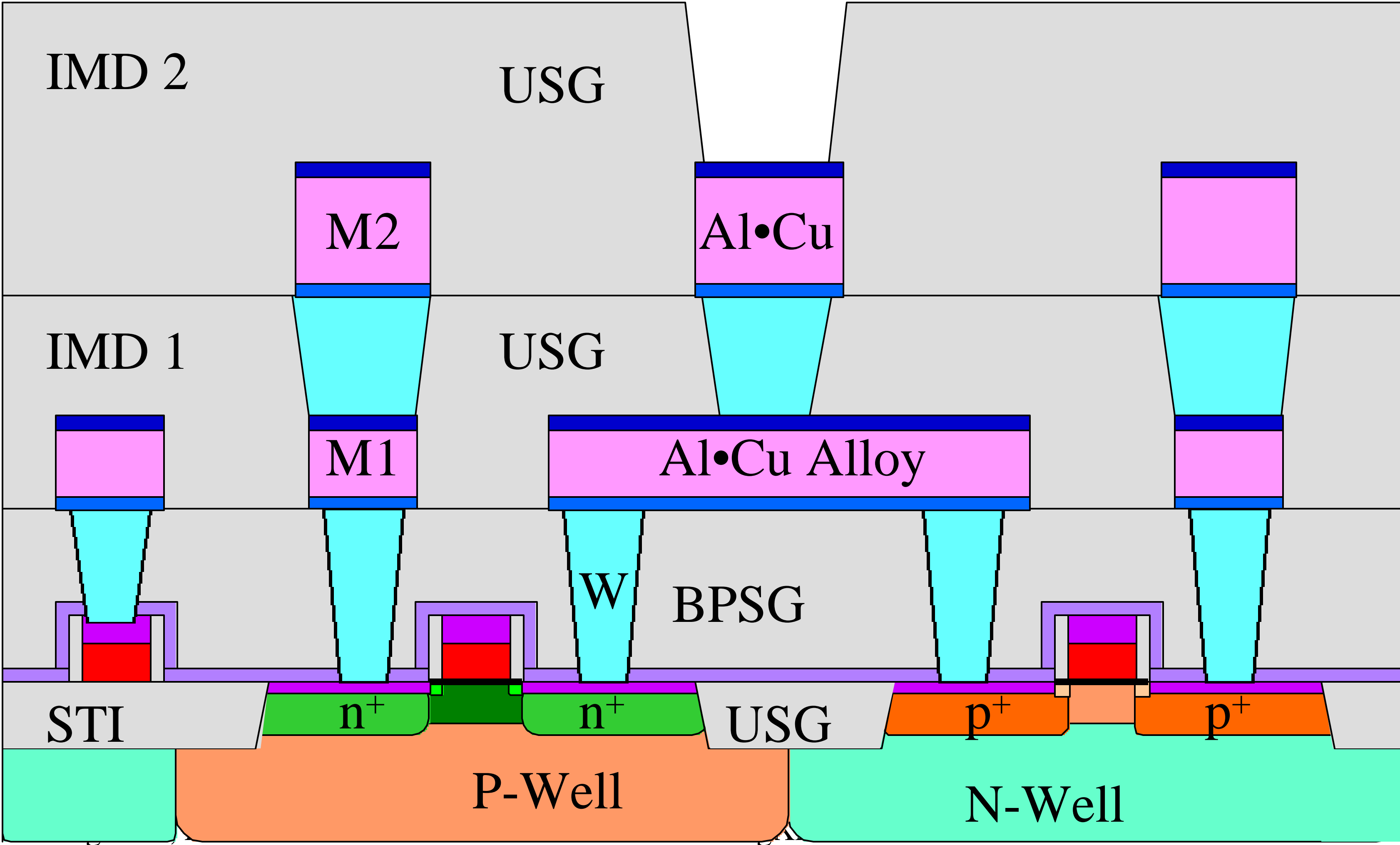
USG Dep/Etch/Dep/CMP



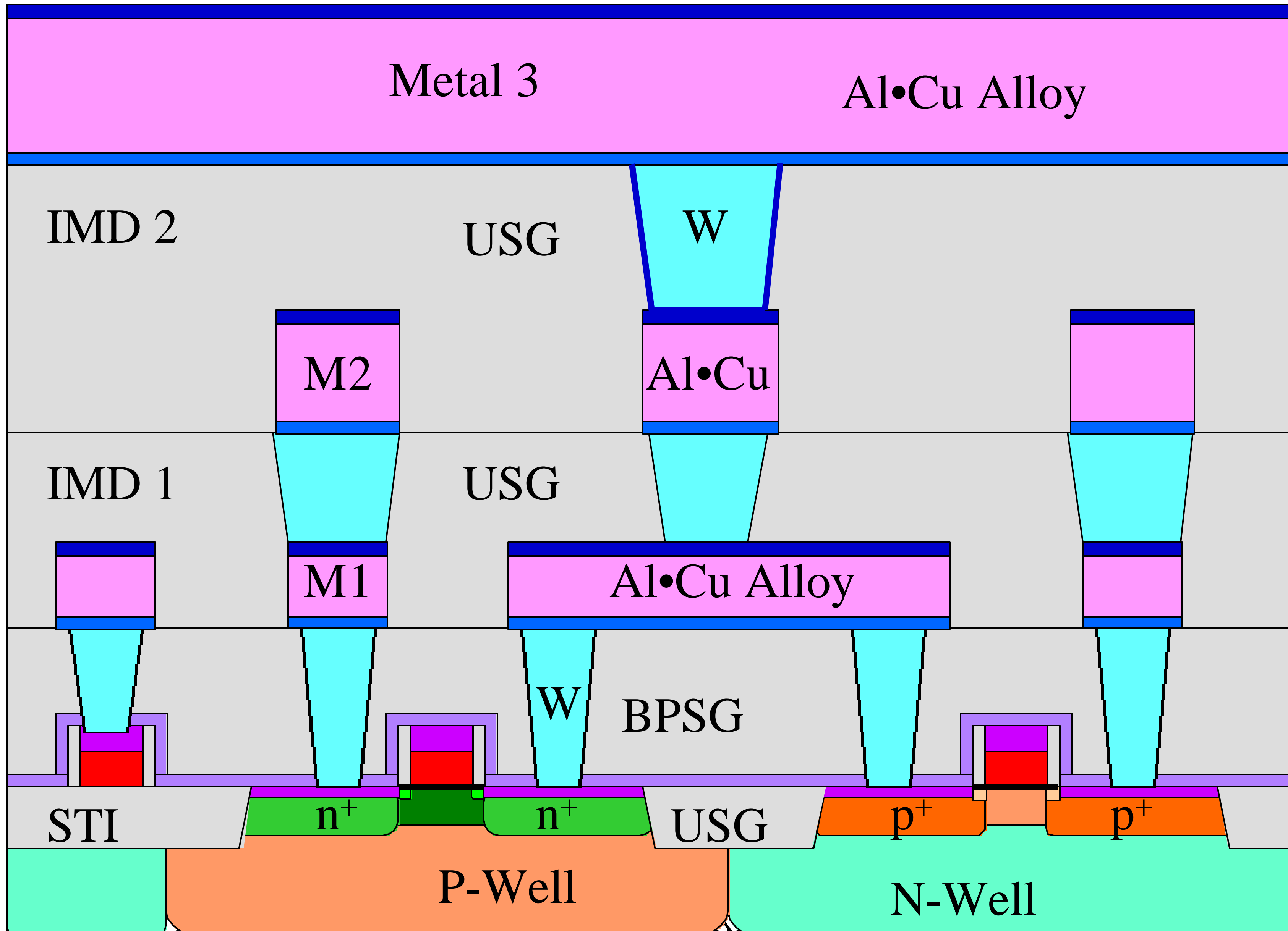
Mask 14: Via 2



Via 2 Etch, Etch USG

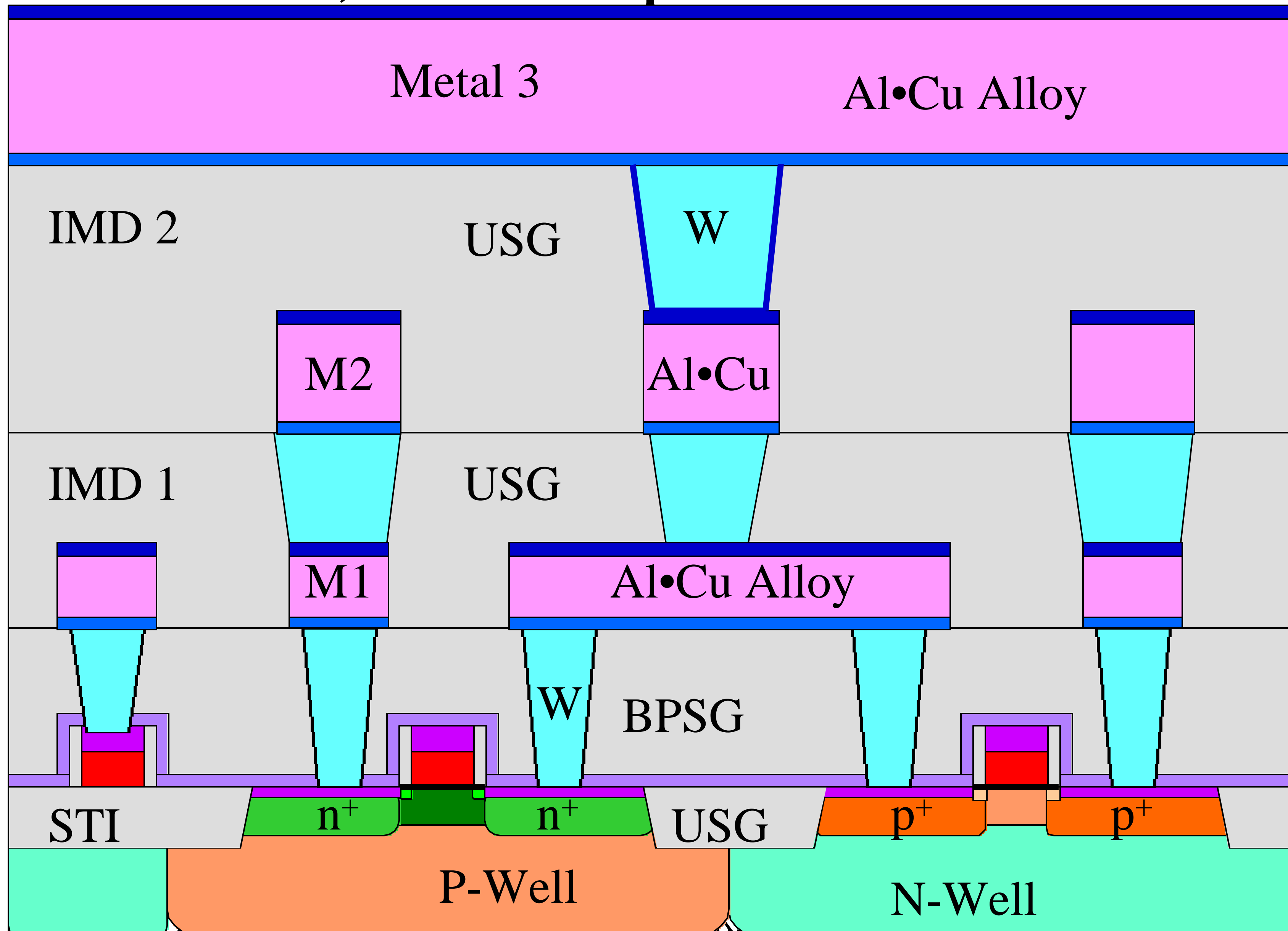


Metallization of Metal 3

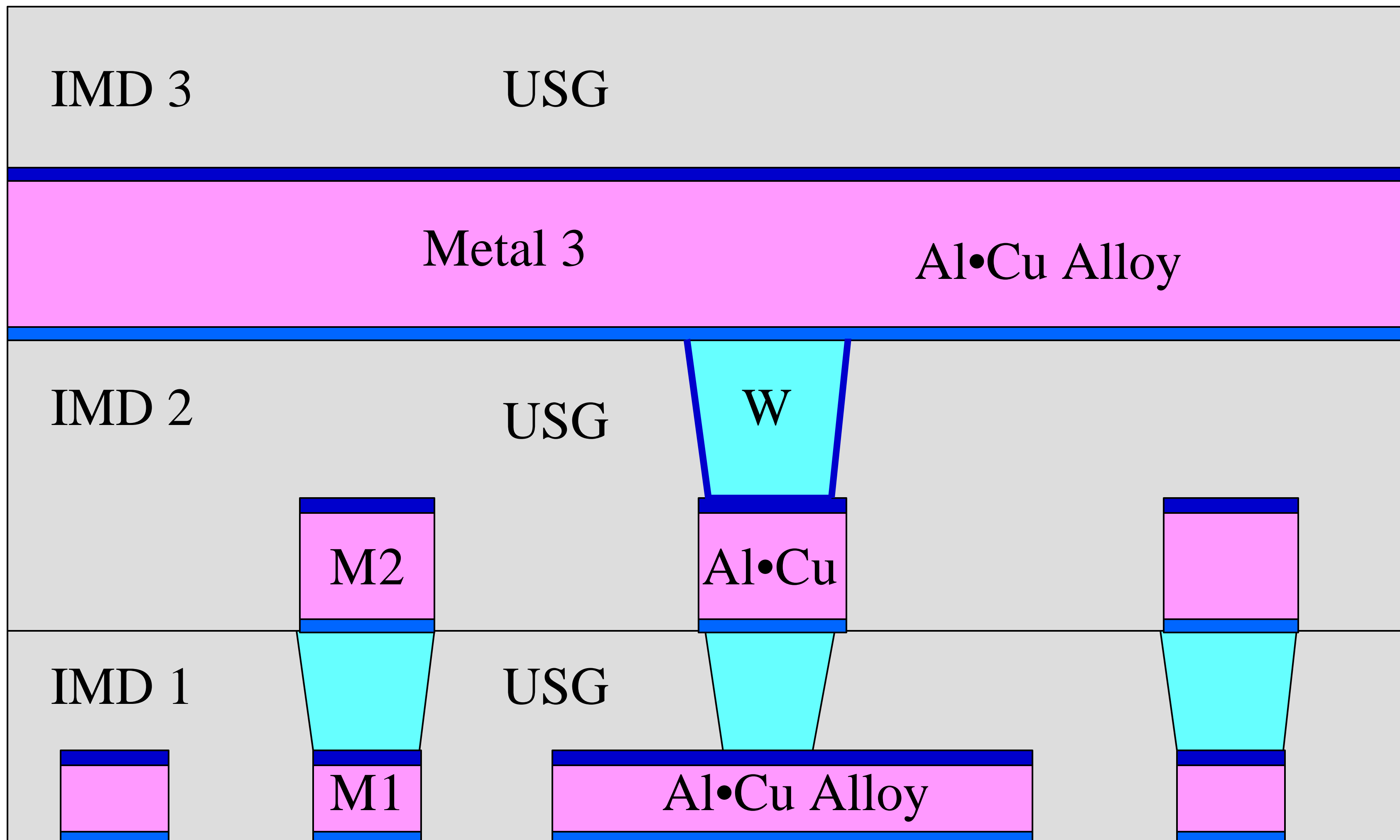


Mask 15: Metal 3 Interconnects

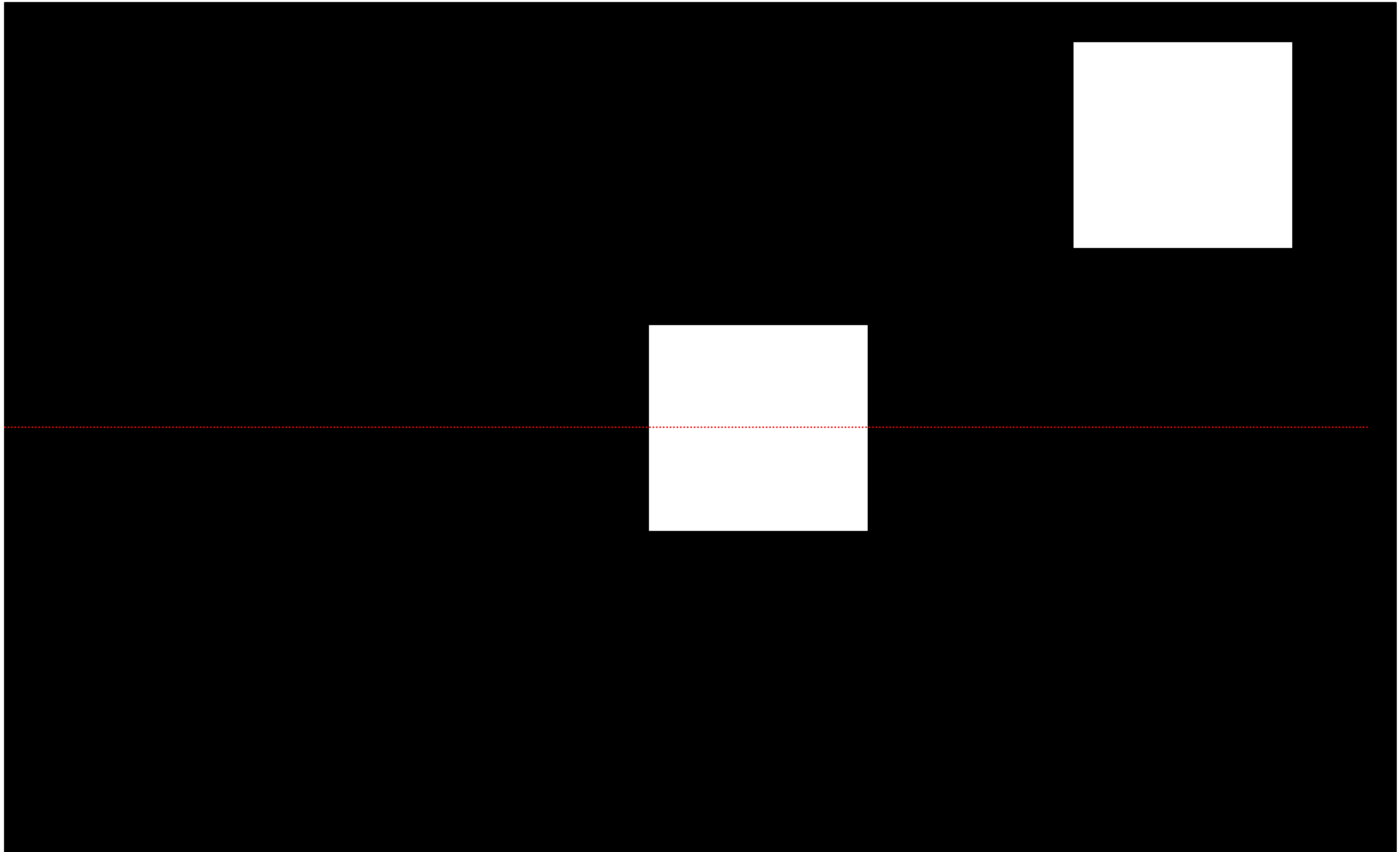
Metal Etch, PR Strip and Metal Anneal



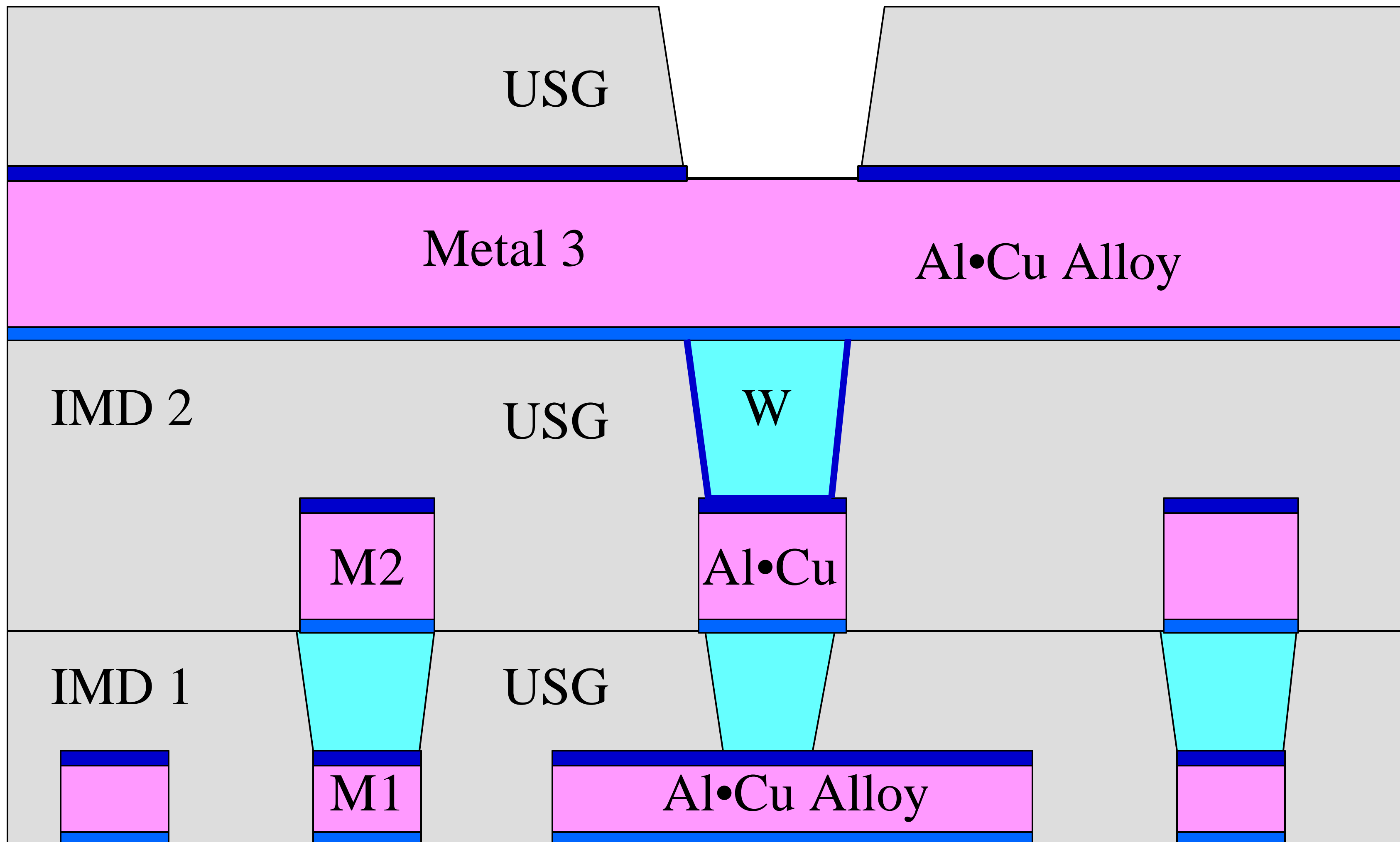
PE-TEOS USG Dep/Etch/Dep/CMP



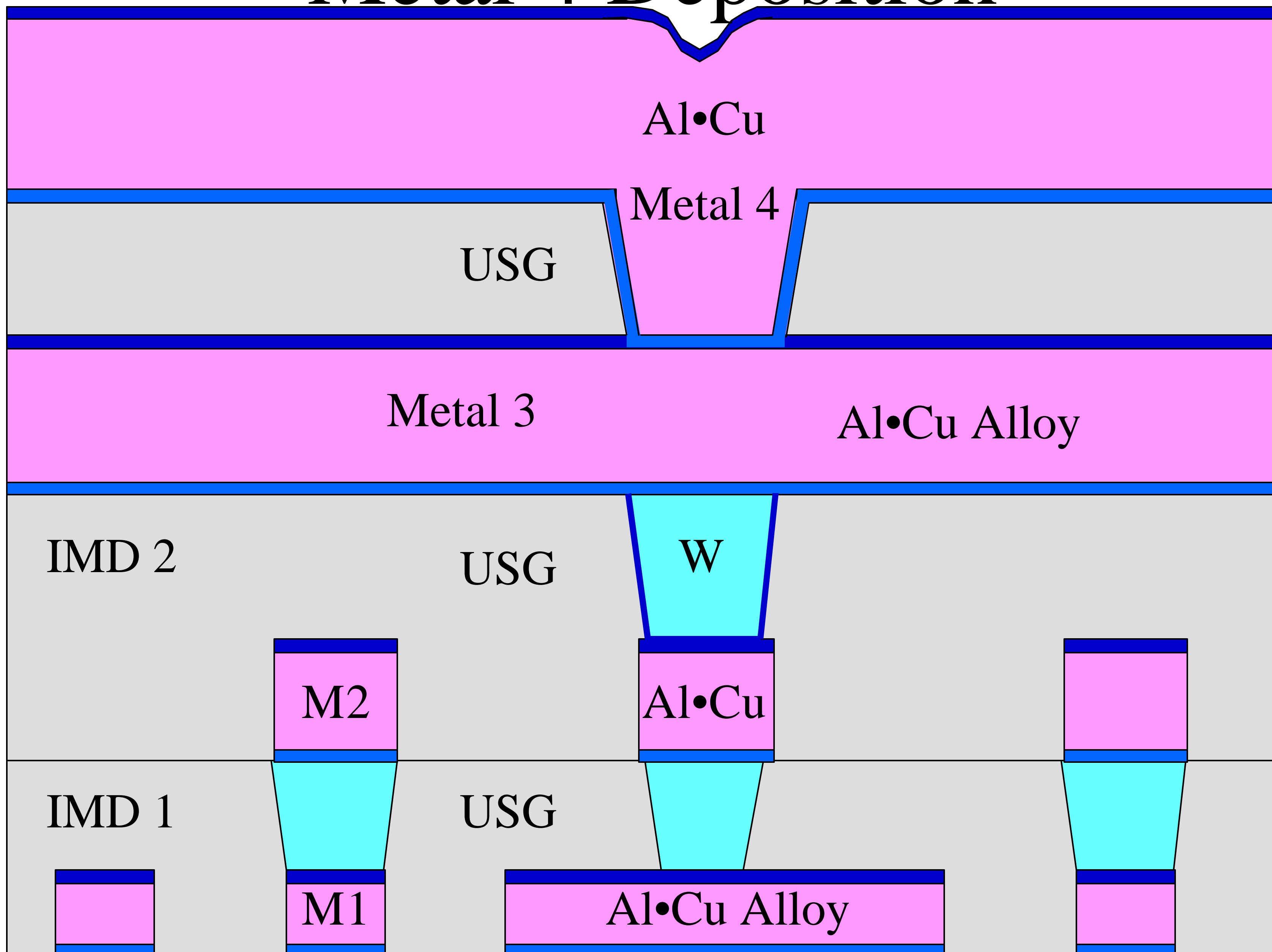
Mask 16: Via 3



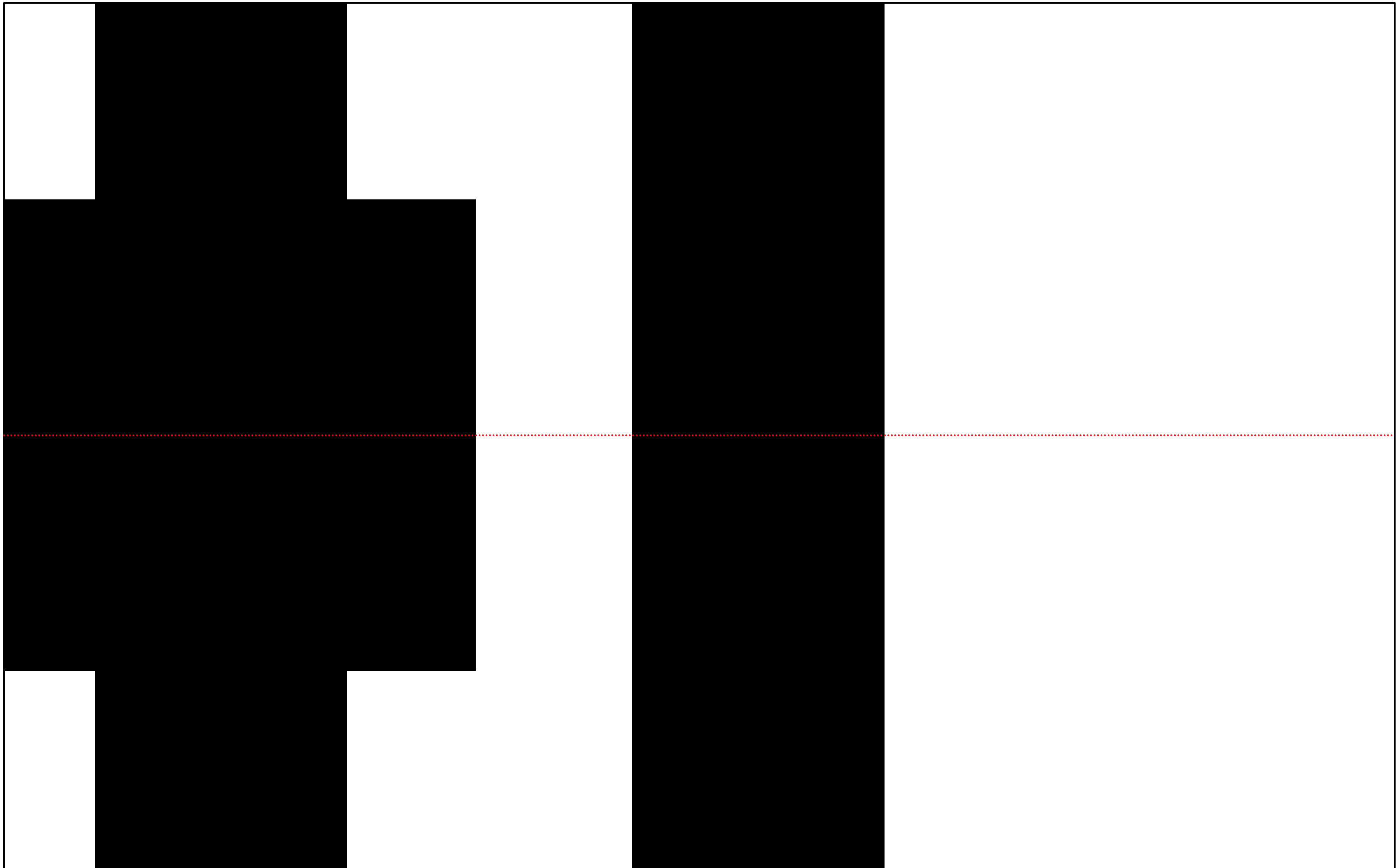
Via 3 Etch and PR Strip



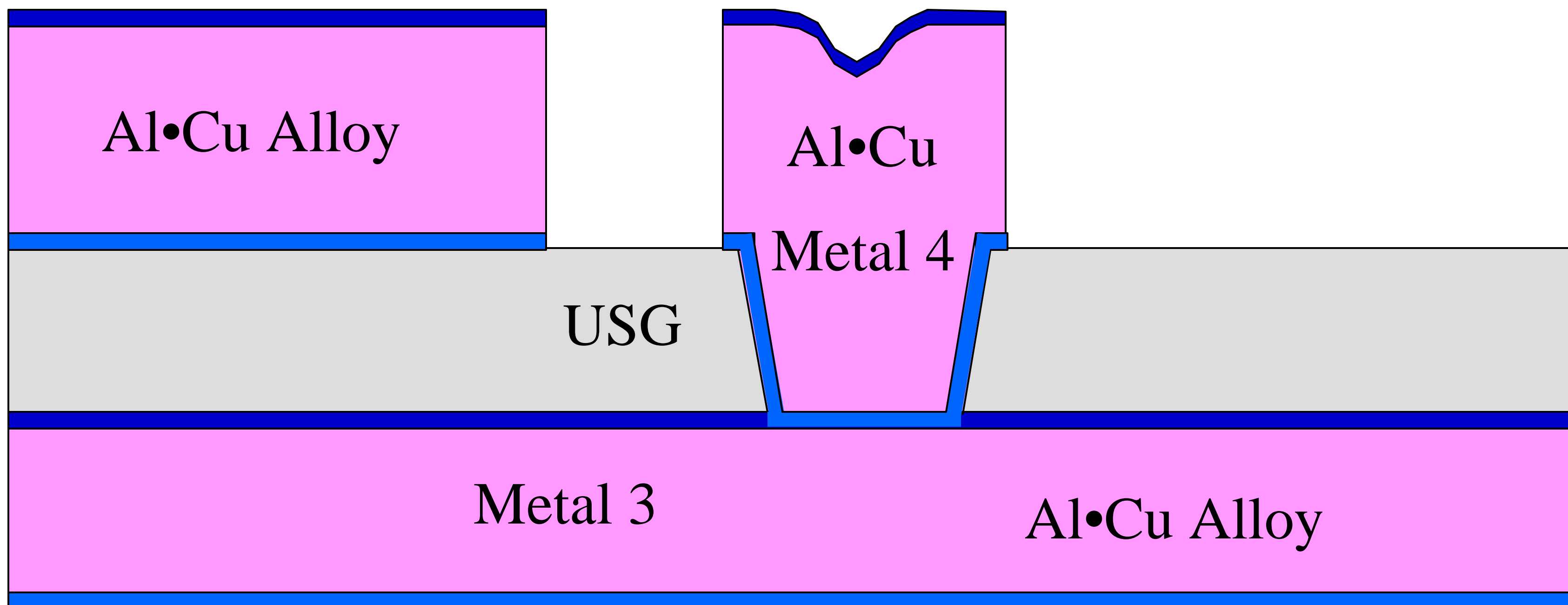
Metal 4 Deposition



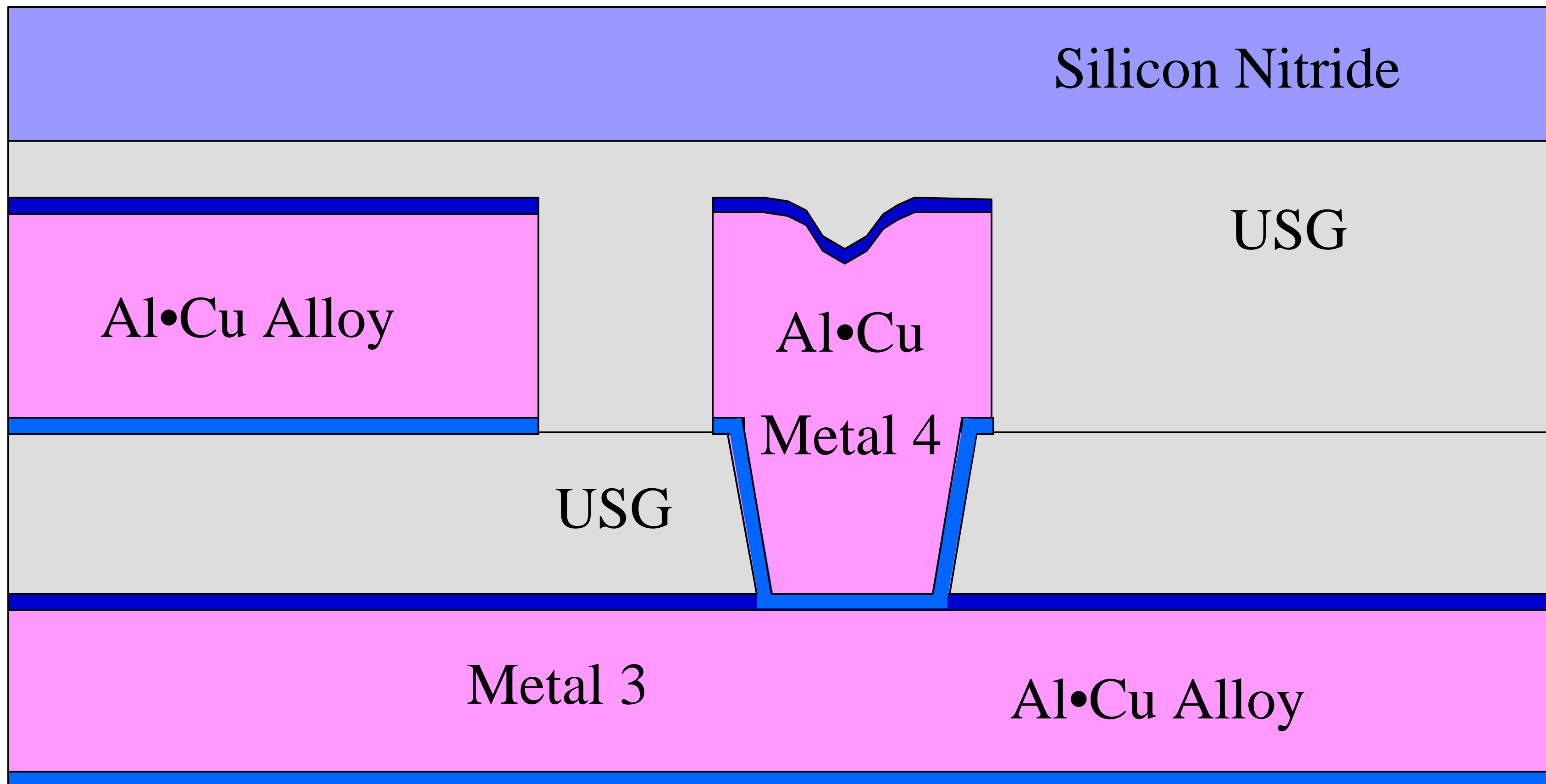
Mask 17: Metal 4 Interconnects



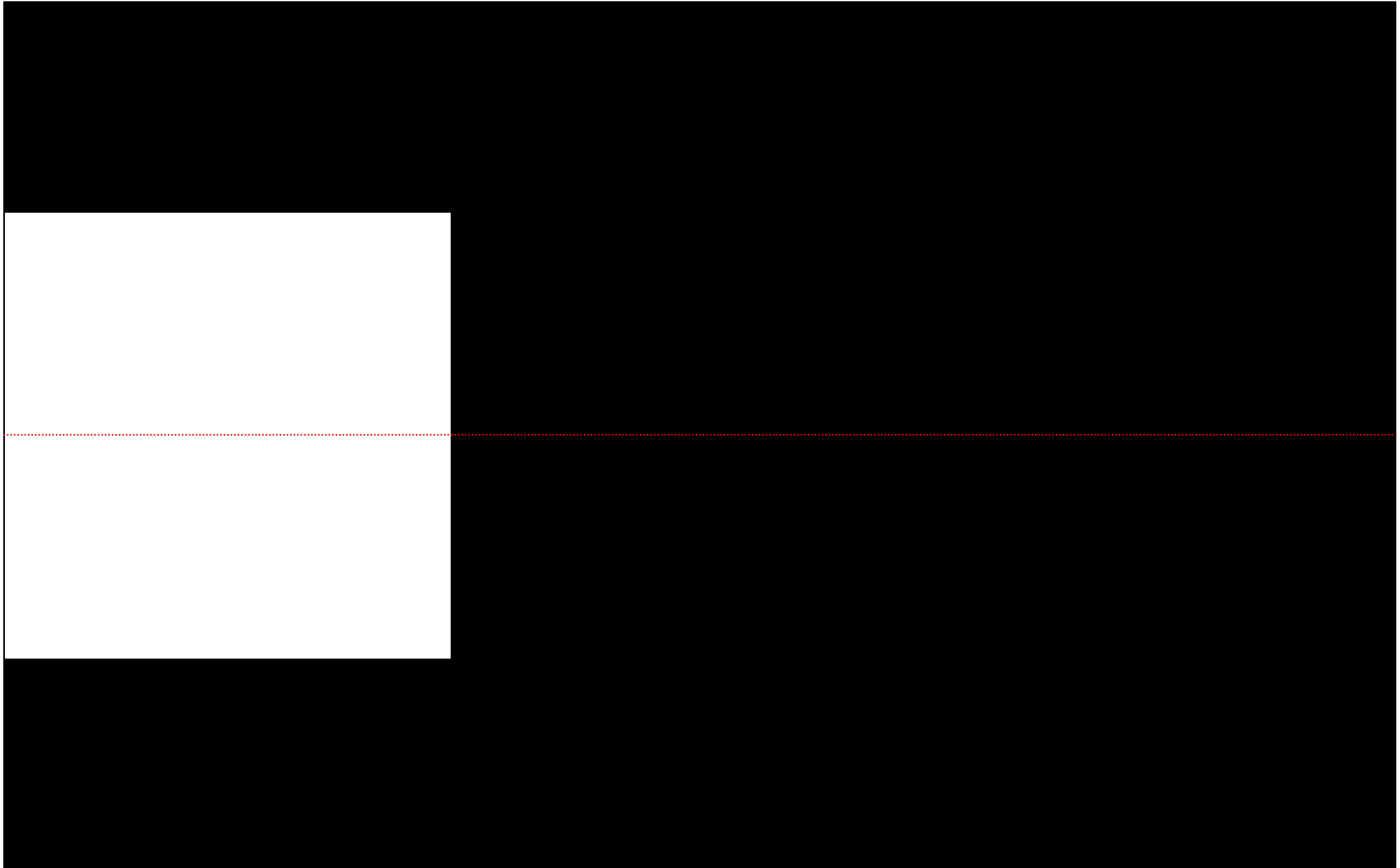
Etch Metal 4



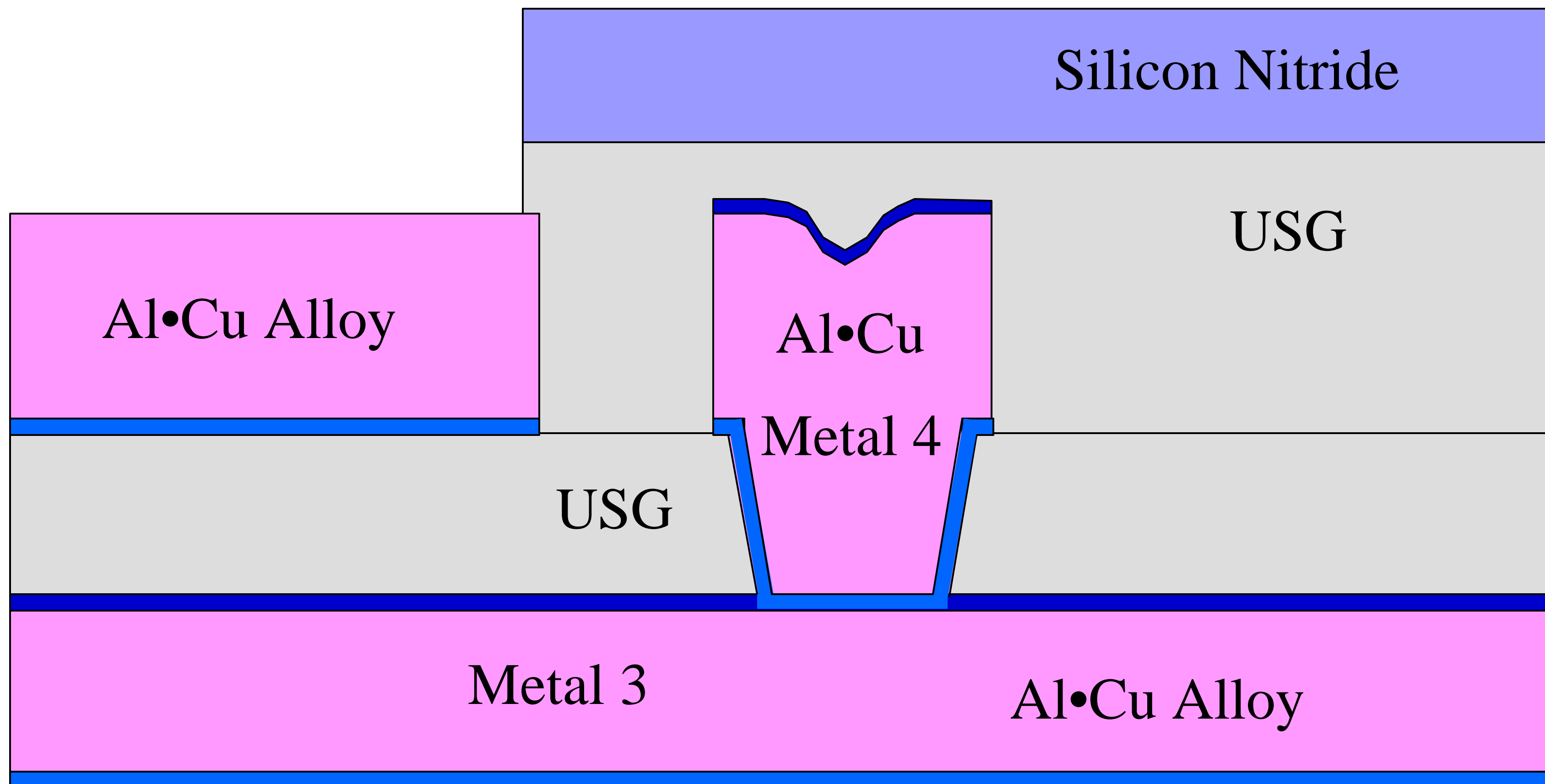
Passivation Dielectric Deposition

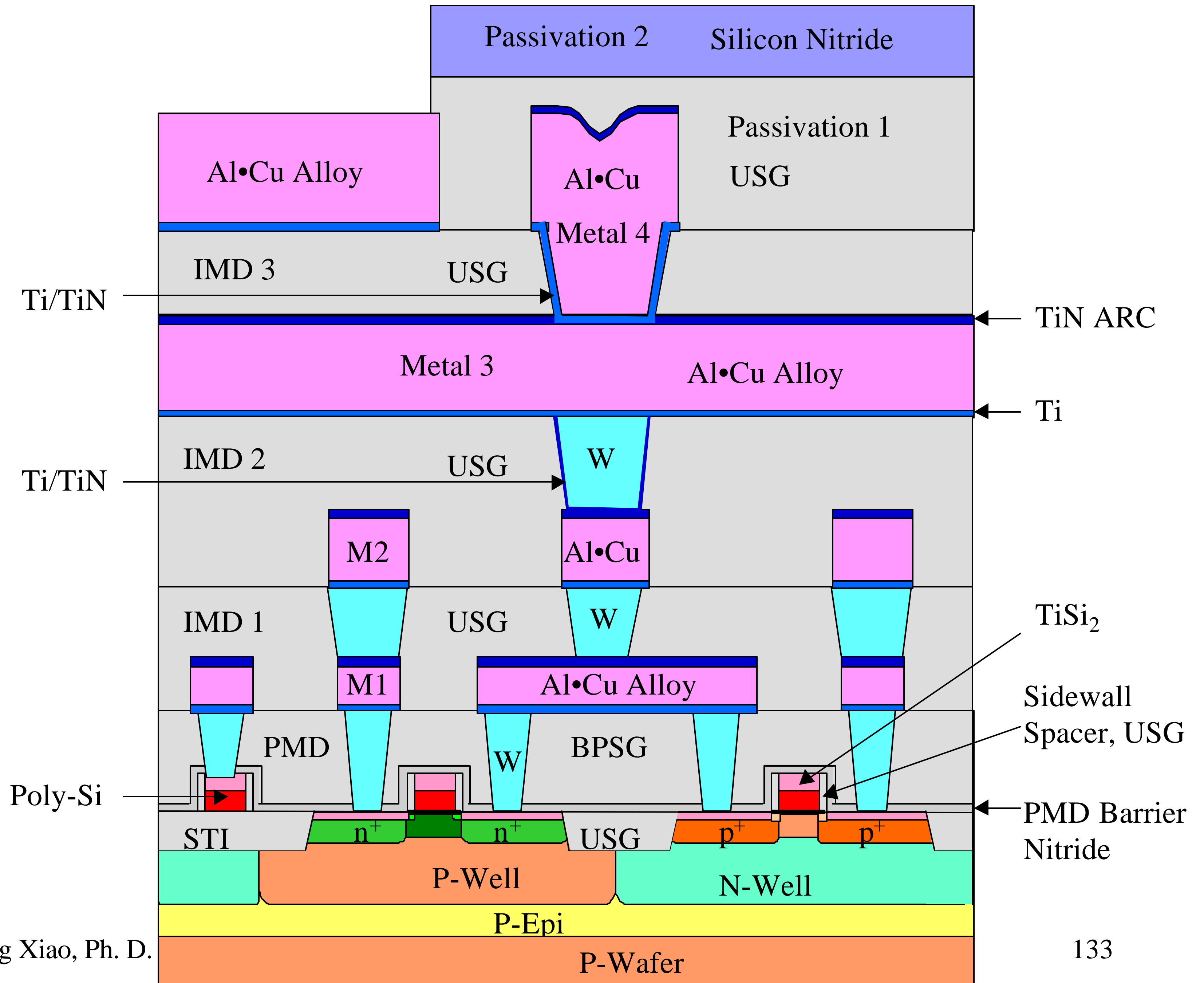


Mask 18: Bonding Pad



Etch Bonding Pad, Strip PR




Passivation 2
Silicon Nitride
Passivation 1
USG
Al•Cu Alloy
Al•Cu
Metal 4
IMD 3
USG
Ti/TiN
TiN ARC
Metal 3
Al•Cu Alloy
Ti
IMD 2
USG
Ti/TiN
W
M2
Al•Cu
IMD 1
USG
W
TiSi$_2$
M1
Al•Cu Alloy
Sidewall
Spacer, USG
PMD
BPSG
W
Poly-Si
PMD Barrier
Nitride
STI
n$^+$
n$^+$
USG
p$^+$
p$^+$
P-Well
N-Well
P-Epi
P-Wafer

State-of-art Technology

- The 2000's Technology
- Feature size 0.13 μm or smaller
- Wafer size 200 mm or 300 mm

State-of-art Technology

- Silicon on isolator (SOI) with STI
  - Completely isolate the transistor on the silicon surface from the bulk silicon substrate
  - Eliminate radiation-induced soft error.
- Increase the packing density of IC chip.
- High radiation resistance
- SOI chips will become the mainstream for the high-performance electronics

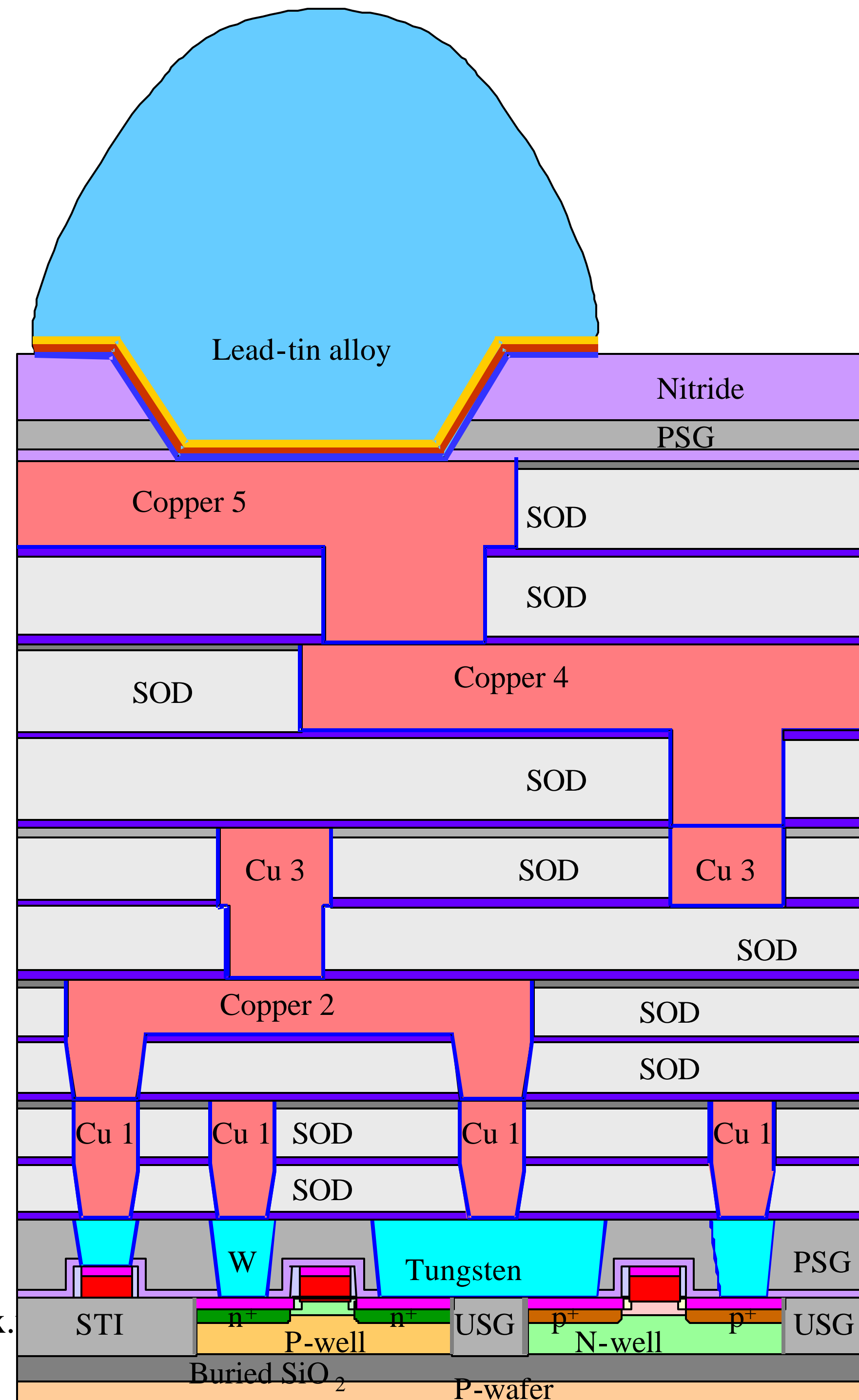
State-of-art Technology

- Copper and low-κ to reduce *RC* delay,
- Lower power consumption, higher IC speed
- Dual damascene process
  - Two dielectric etches, no metal etch
  - Uses metal CMP instead of metal etch
- Main challenges: dielectric etch, metal deposition, and metal polish

State-of-art Technology

- Copper metallization: Cu seed, Ta/TaN barrier, Cu ECP, anneal, and metal CMP
- Low-κ dielectric: still in development
  - CVD and spin-on dielectric (SOD).
  - CVD: familiar technologies, existing process equipment and experience
  - SOD: extendibility to very low dielectric constant (κ<2) with porous silica

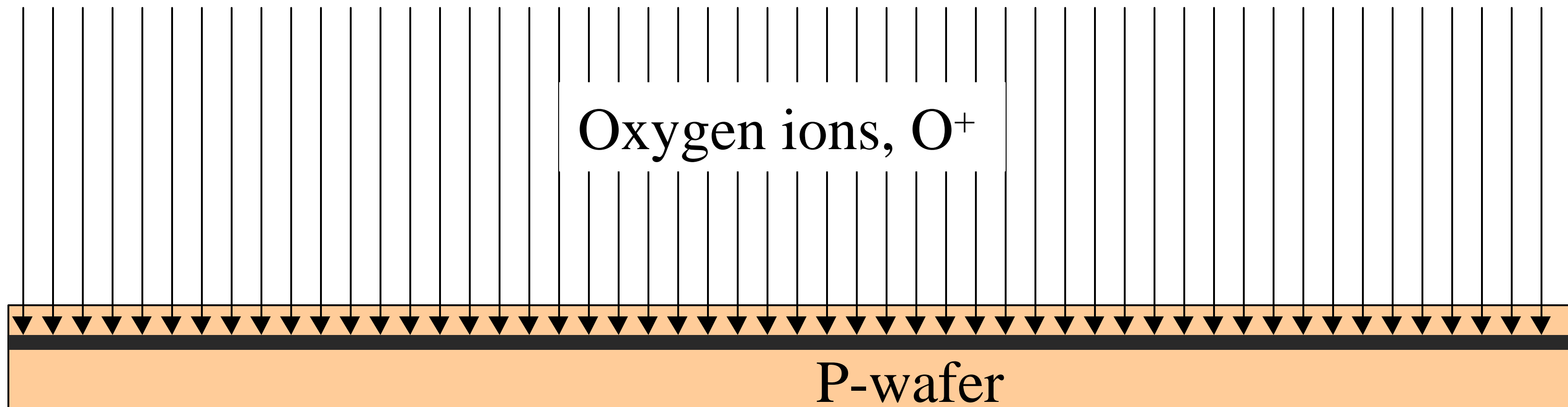
State-of-Art SOI CMOS IC with Copper and Low-κ Interconnection



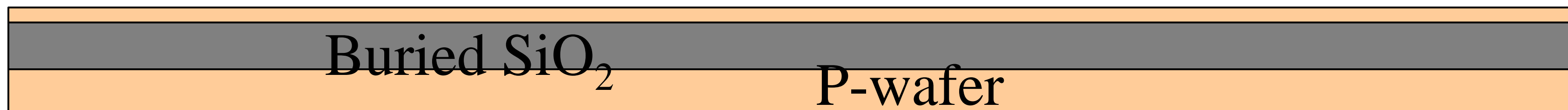
Bare wafer

P-wafer

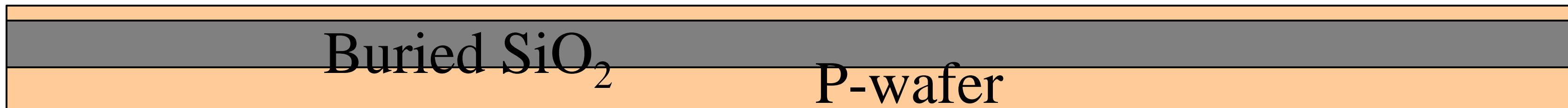
High Current Oxygen Ion Implantation



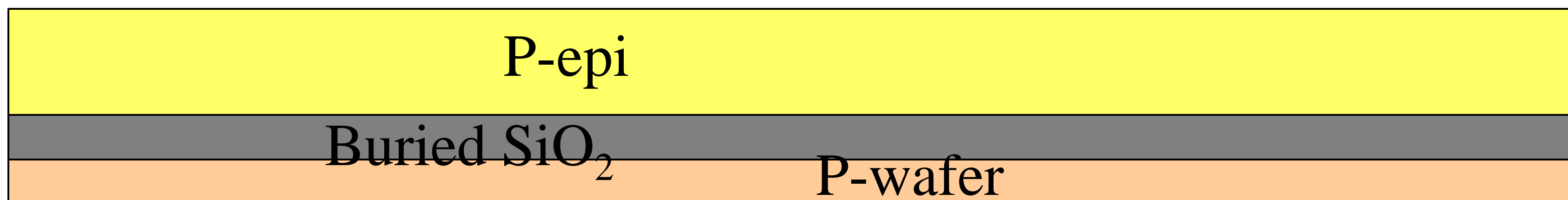
Oxide Anneal



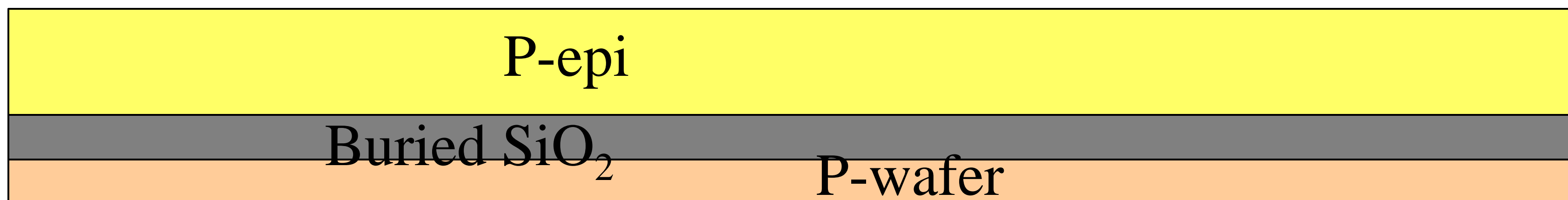
Wafer Clean



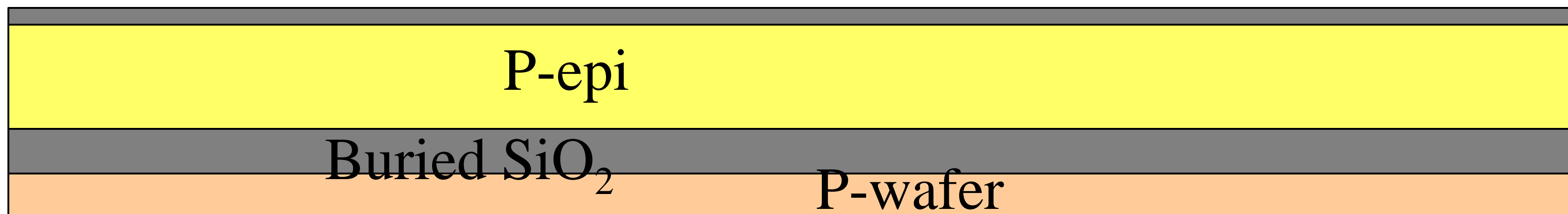
Epitaxial Silicon Deposition



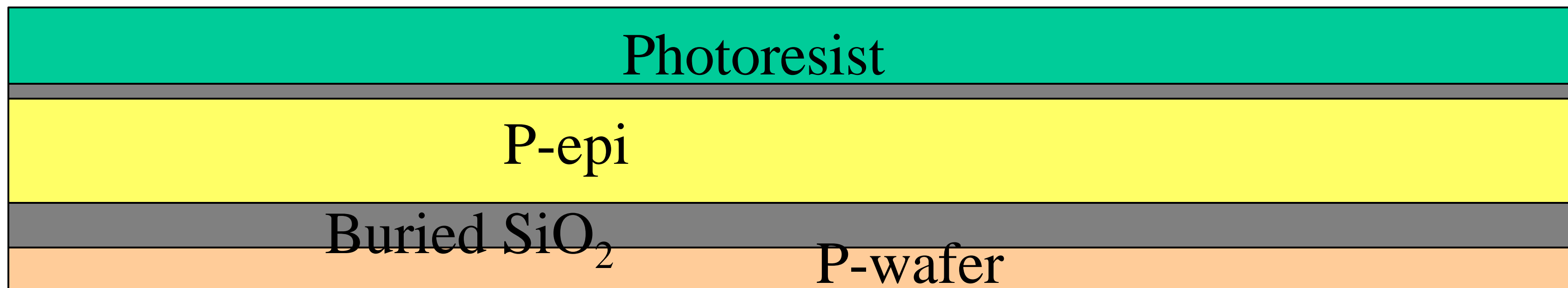
Wafer Clean



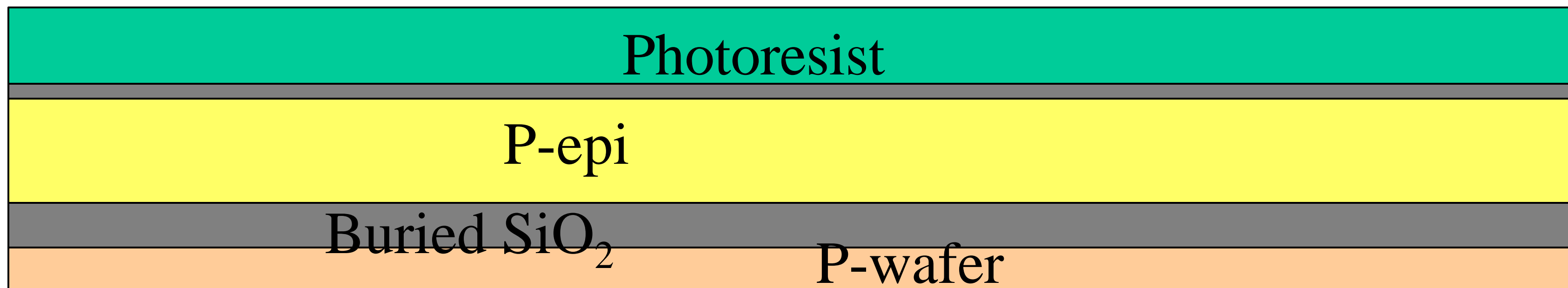
Oxidation, Screen Oxide



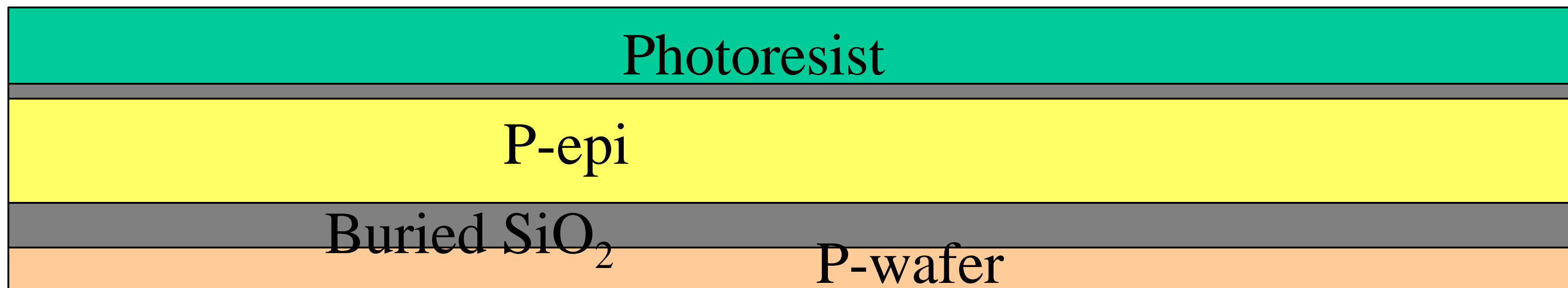
Photoresist Coating and Baking



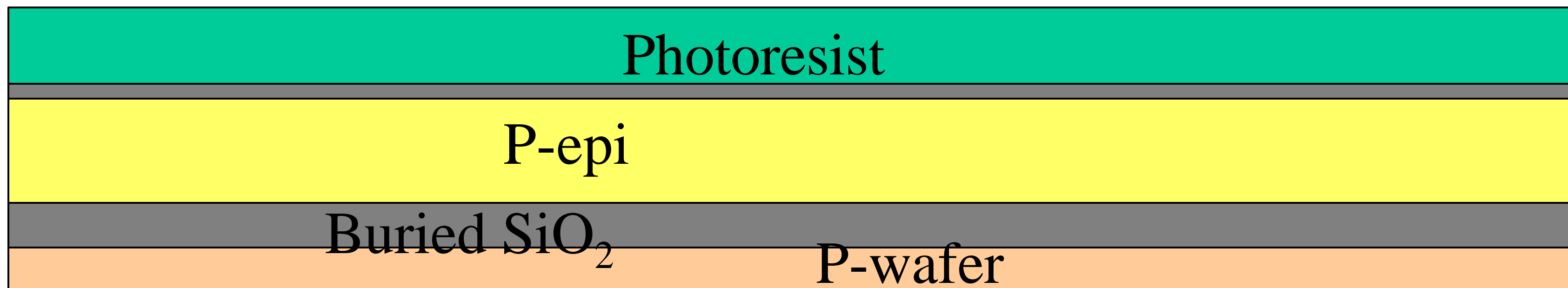
Mask 0, Alignment Mark



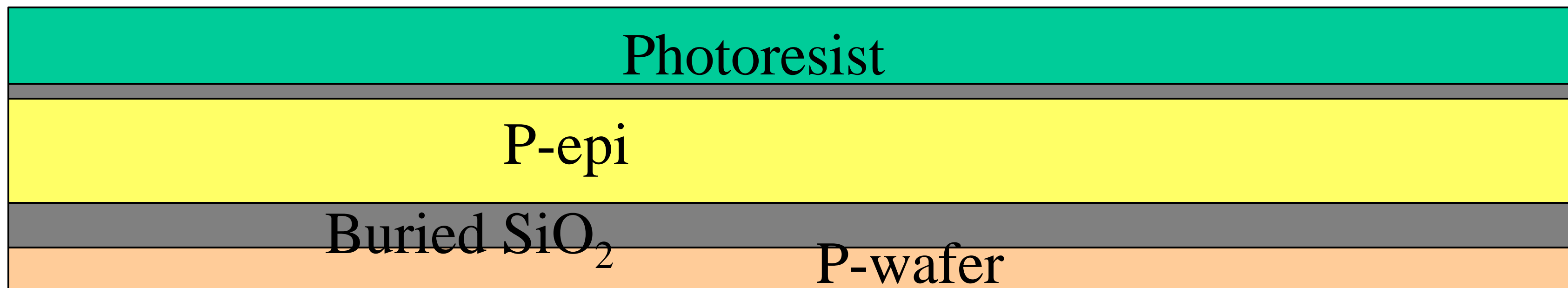
Exposure



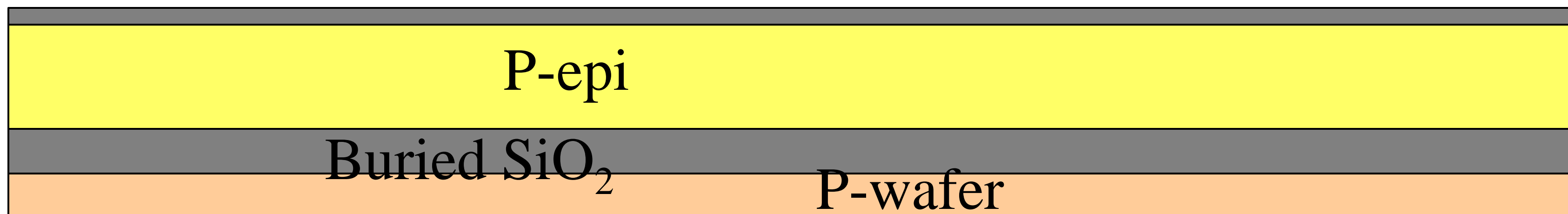
PEB, Development, and Inspection



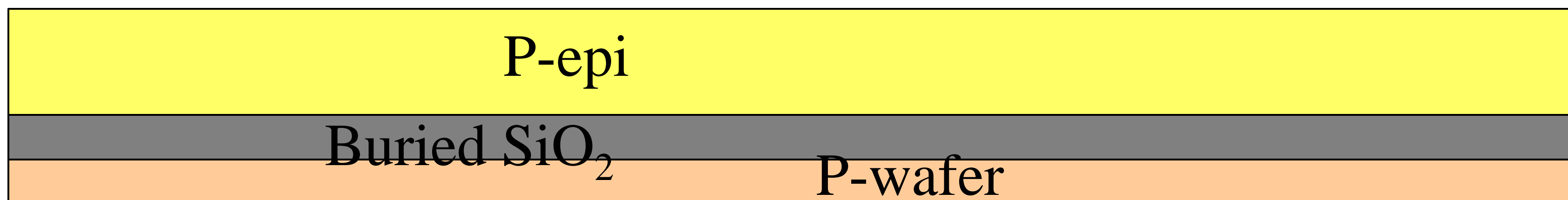
Etch Oxide, Etch silicon



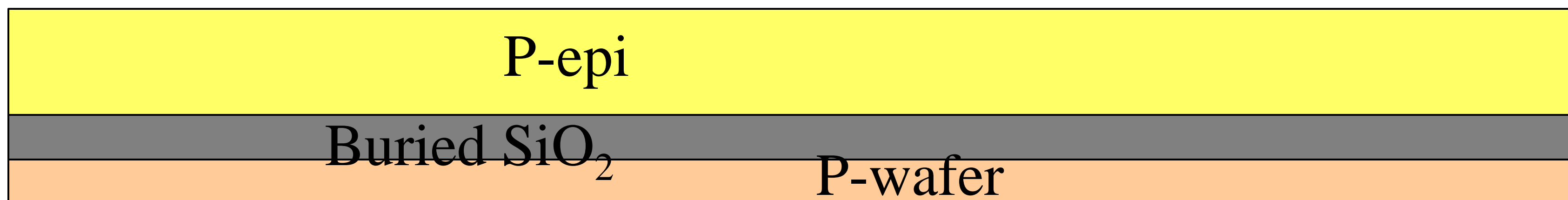
Strip Photoresist



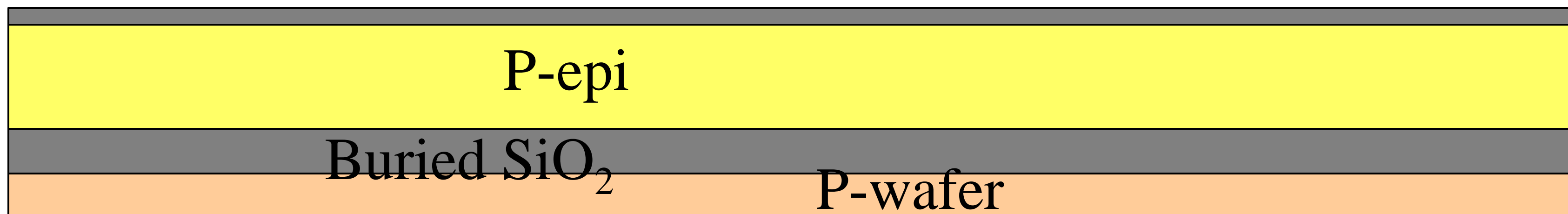
Strip Screen Oxide



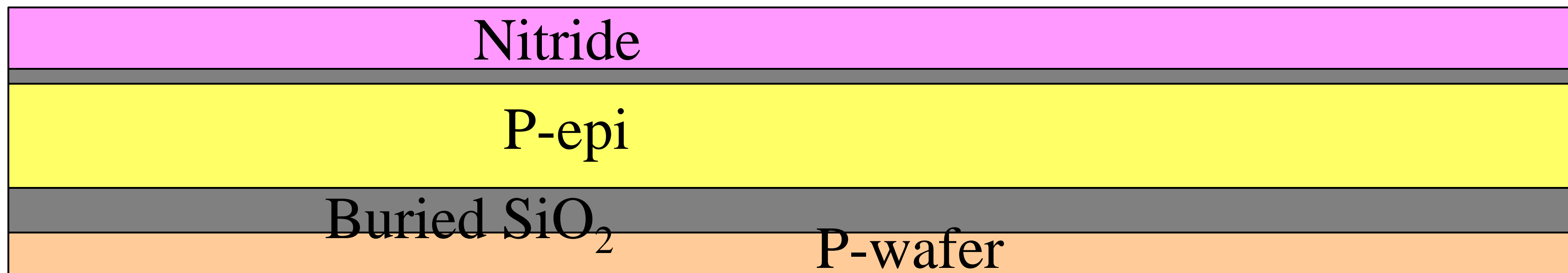
Wafer Clean



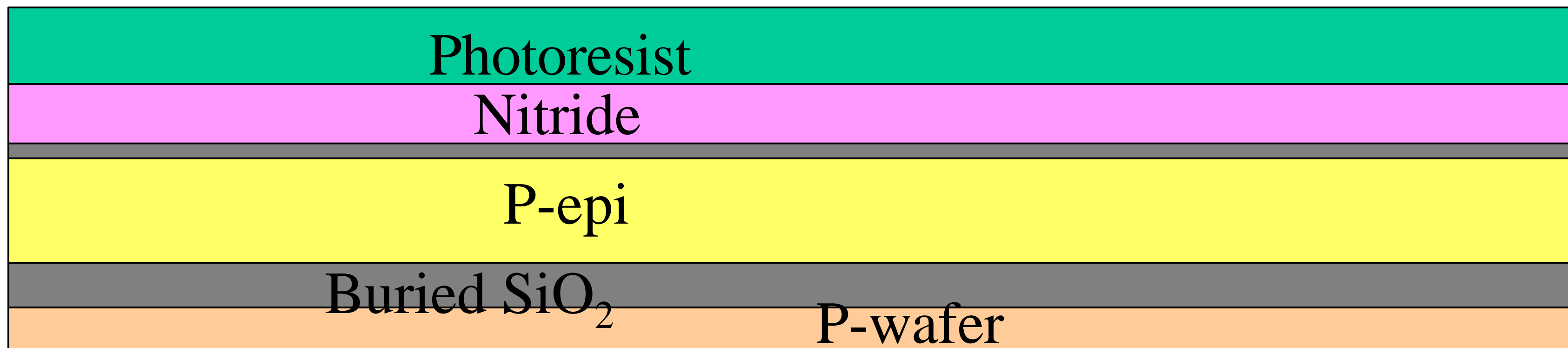
Oxidation, Pad Oxide



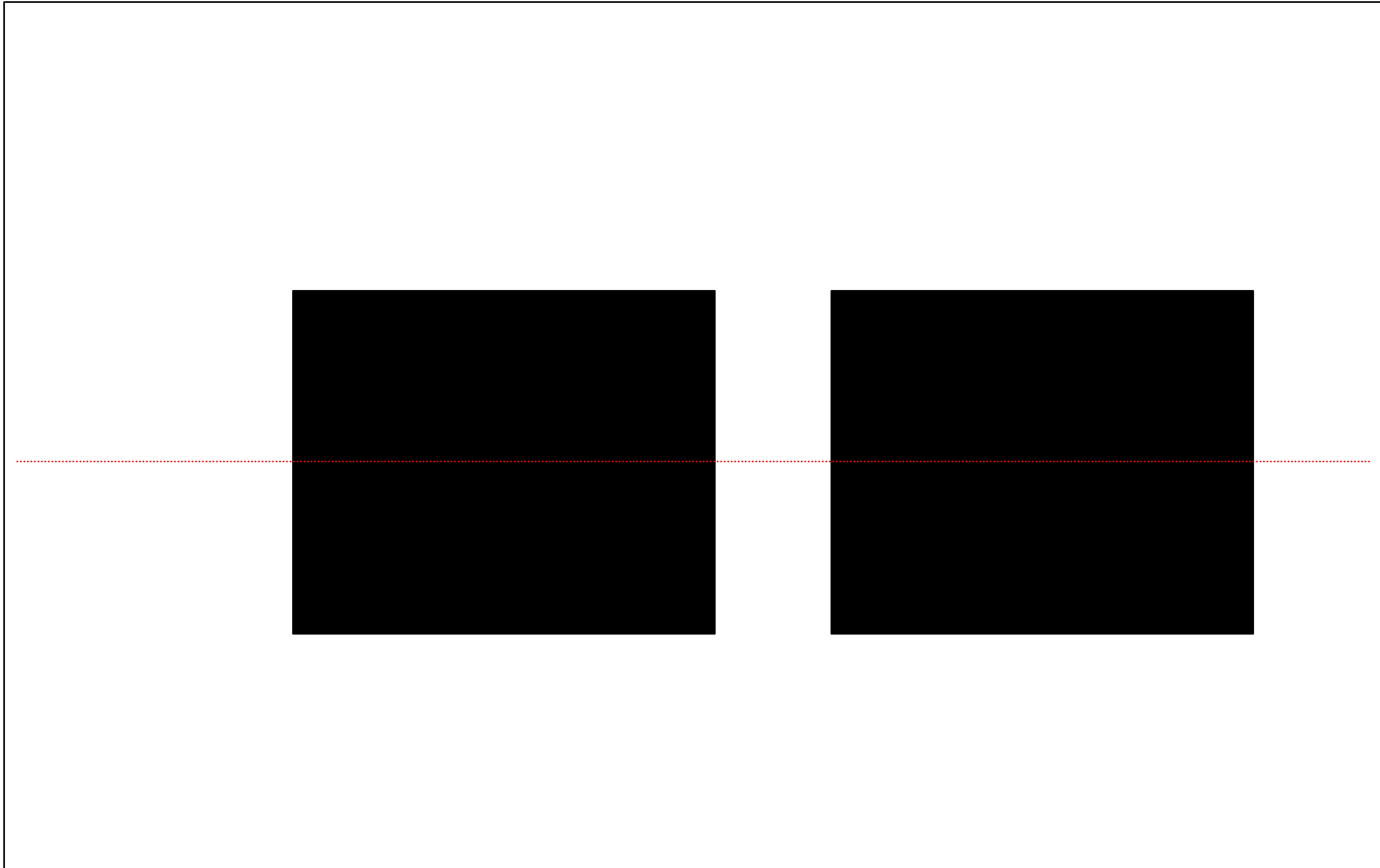
LPCVD Silicon Nitride



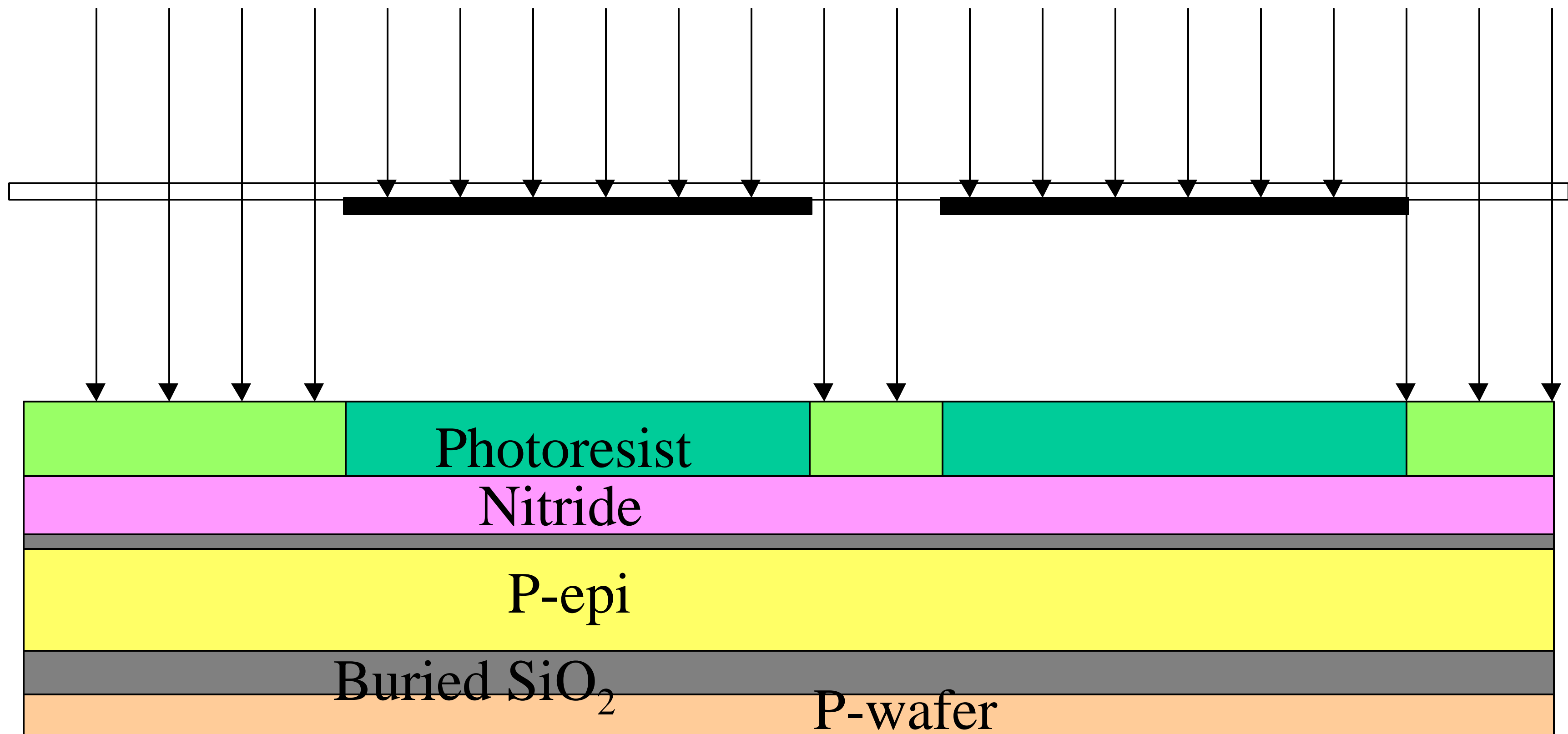
Photoresist Coating and Baking



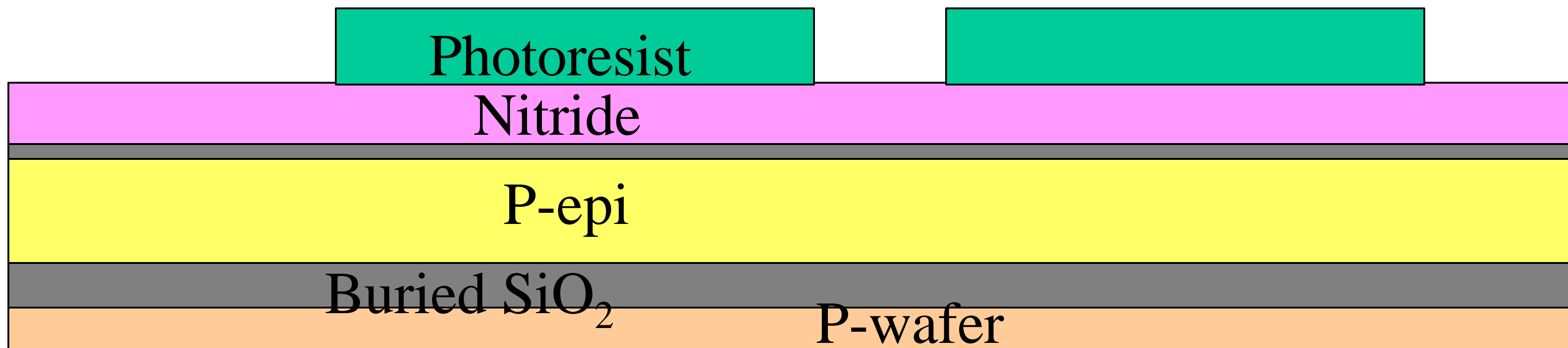
Mask 1: Shallow Trench Isolation



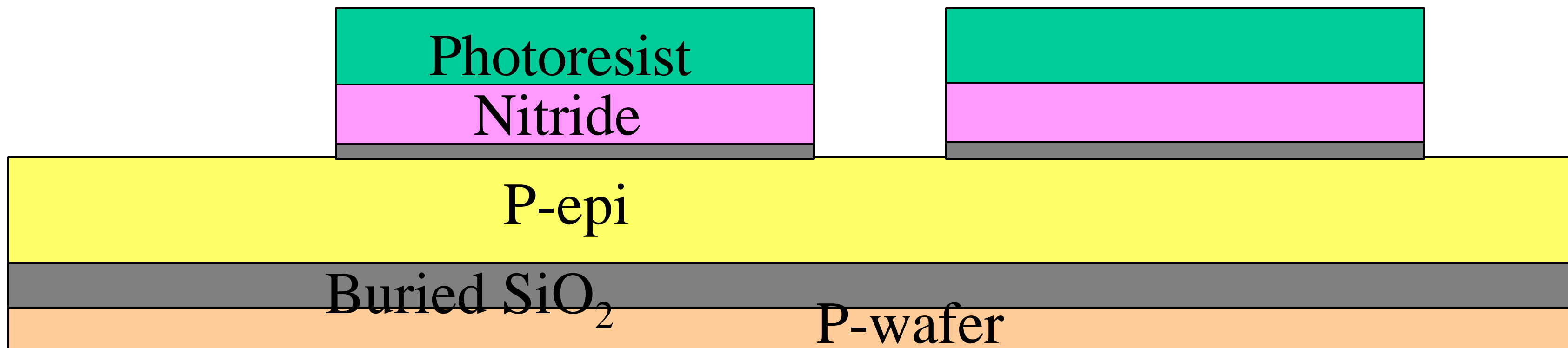
Alignment and Exposure



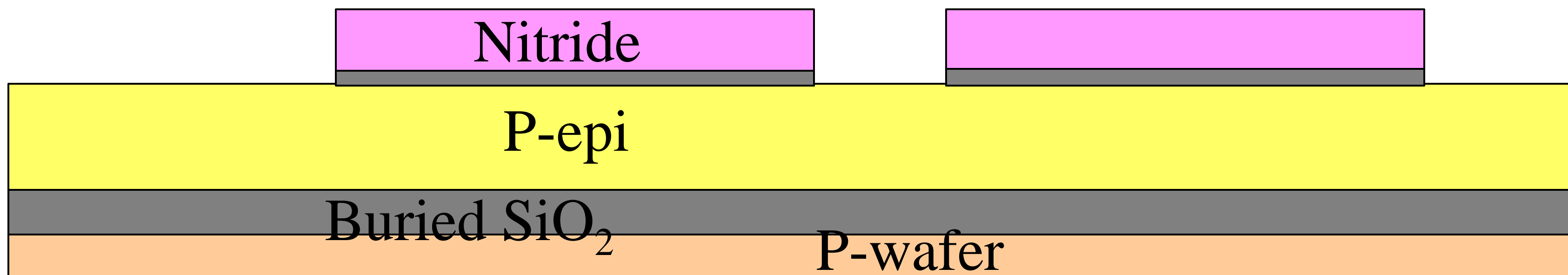
PEB, Development, and Inspection



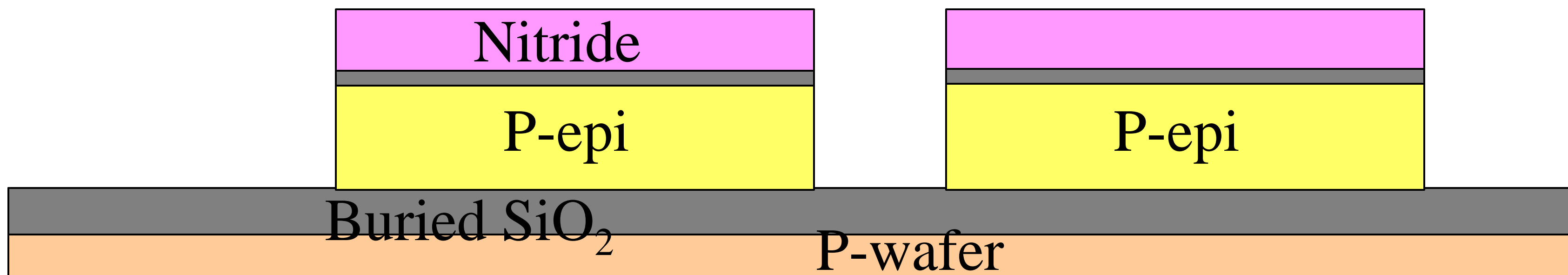
Etch Nitride and Pad Oxide



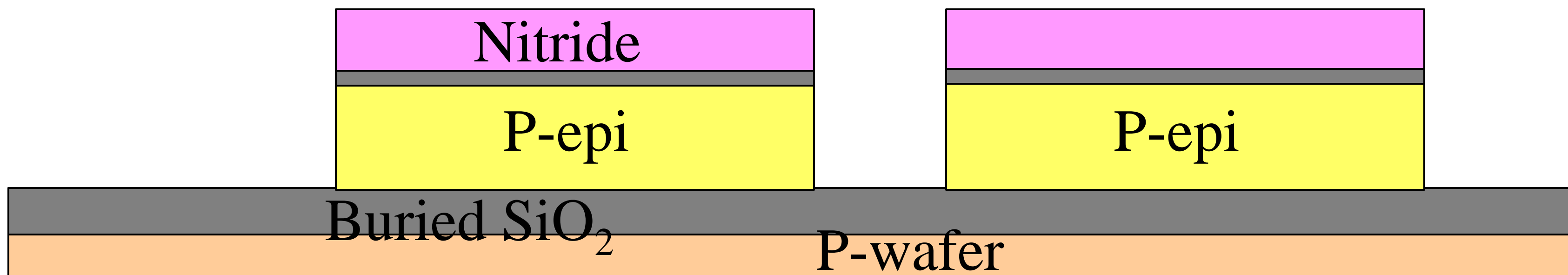
Strip Photoresist



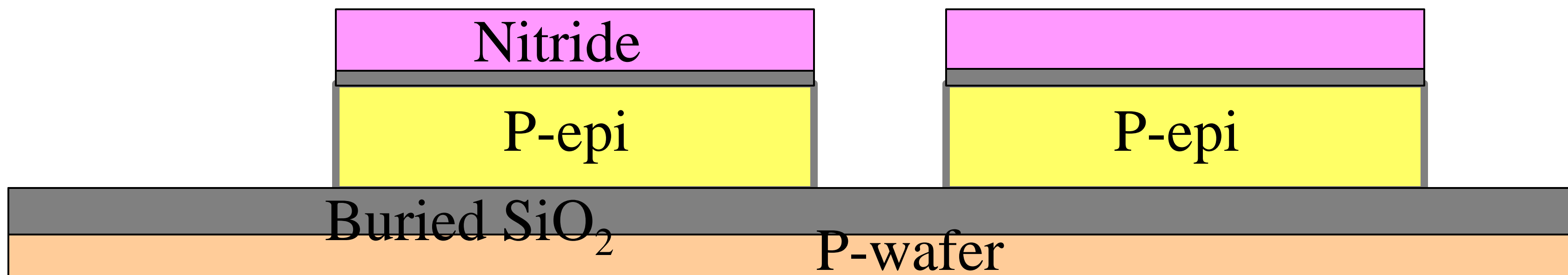
Etch Silicon



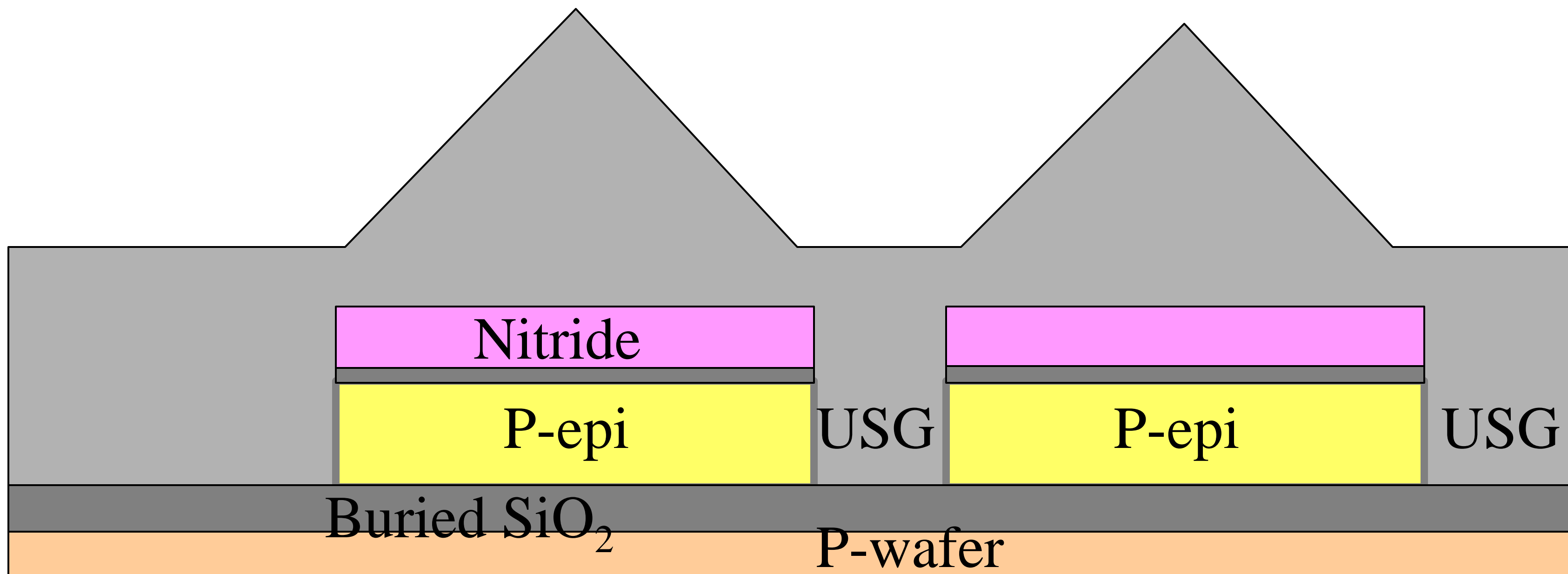
Wafer Clean



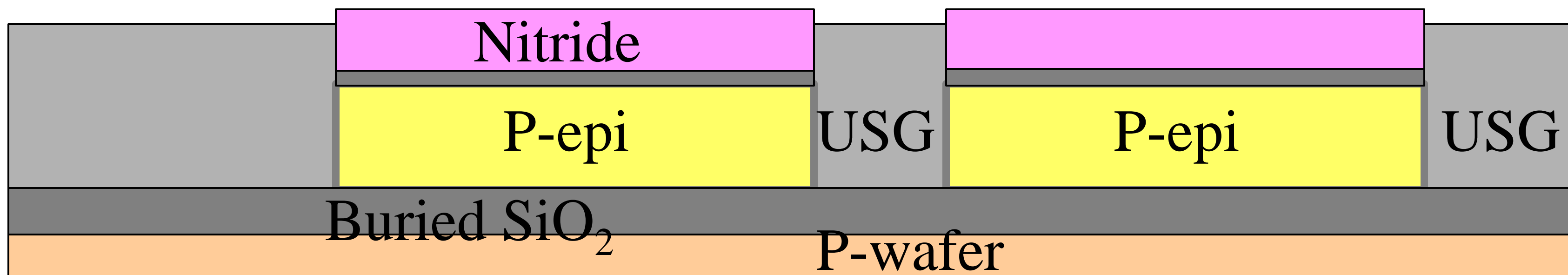
Oxidation, Barrier Oxide



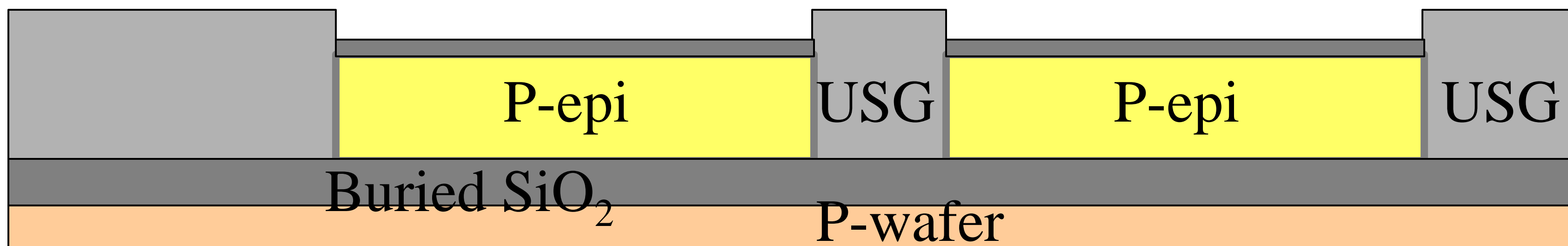
HDP CVD USG



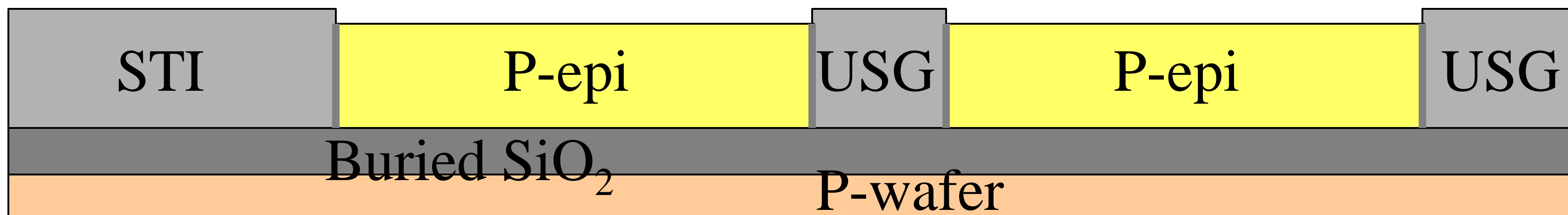
CMP USG



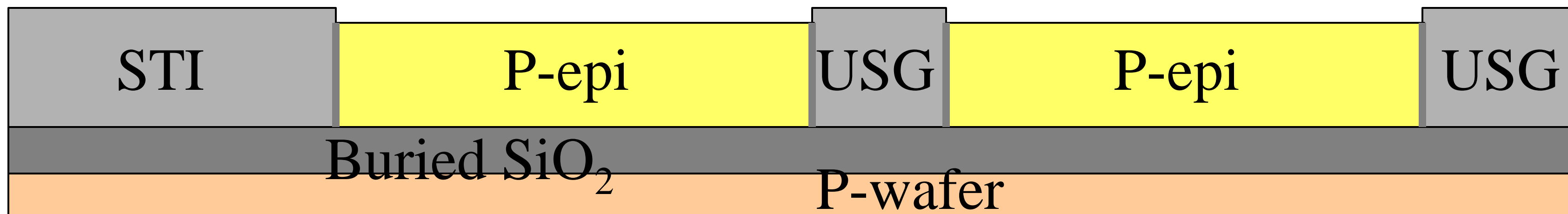
Strip Nitride



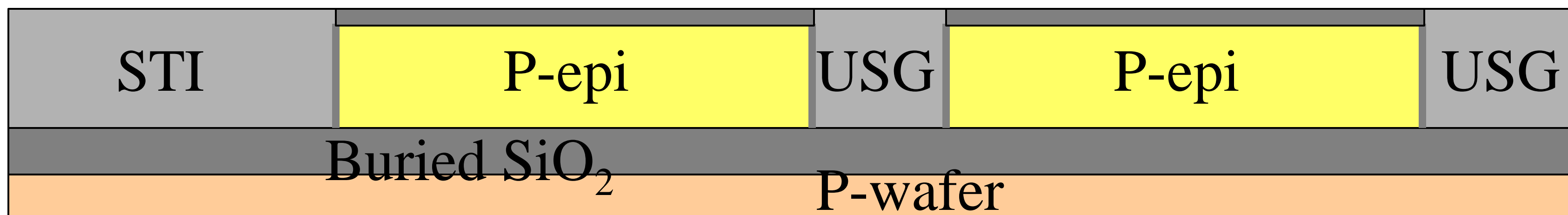
Strip Pad Oxide



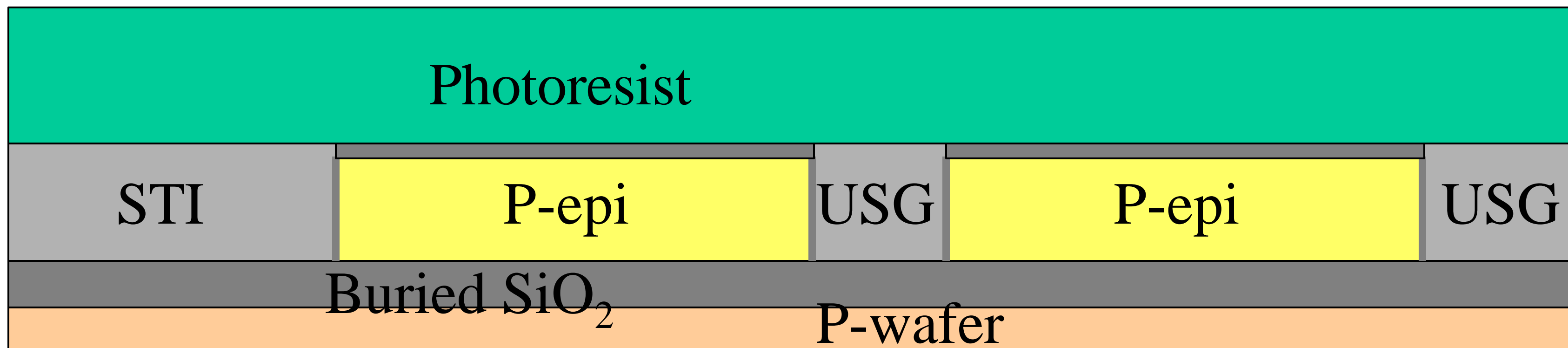
Wafer Clean



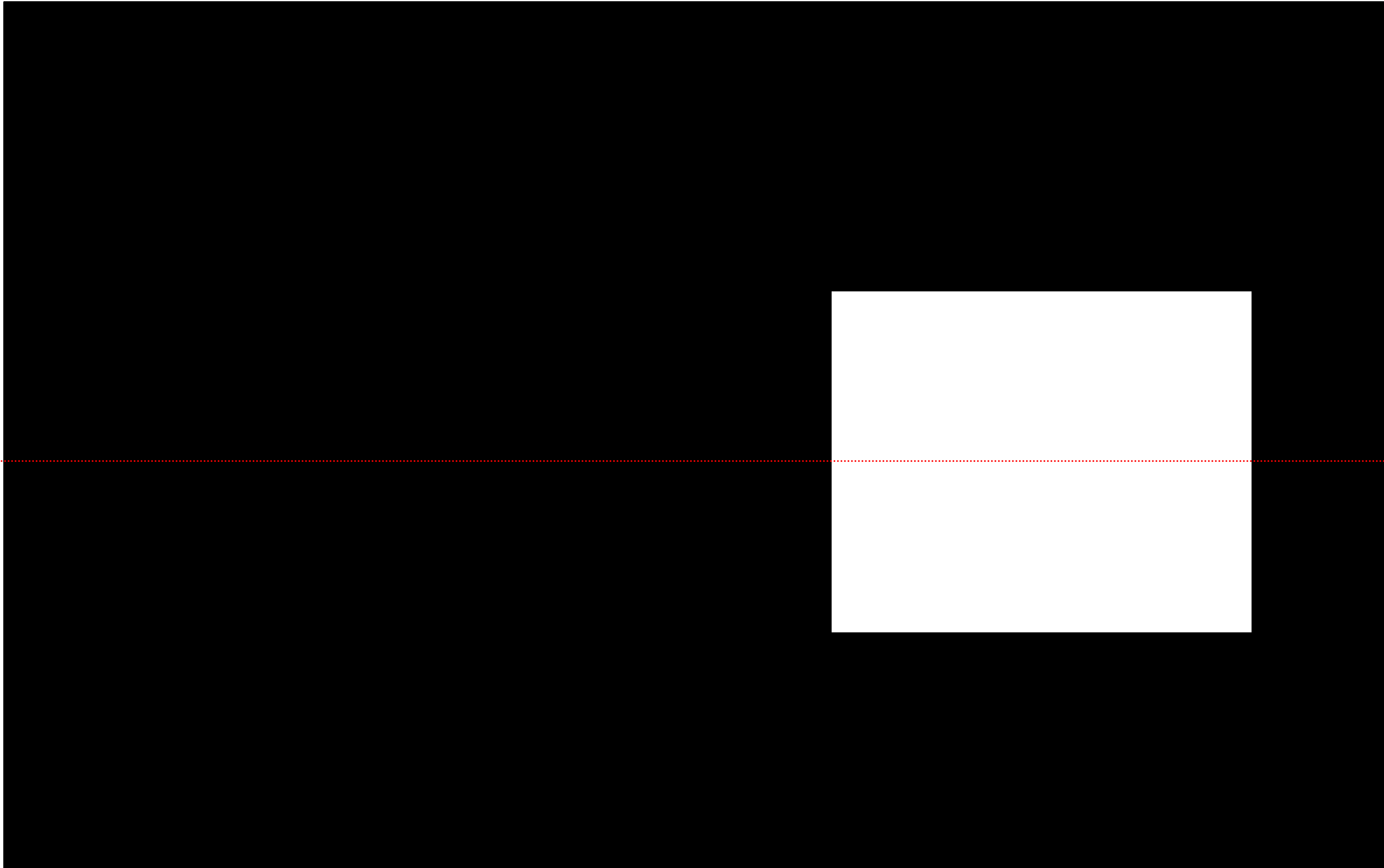
Oxidation, Sacrificial Oxide



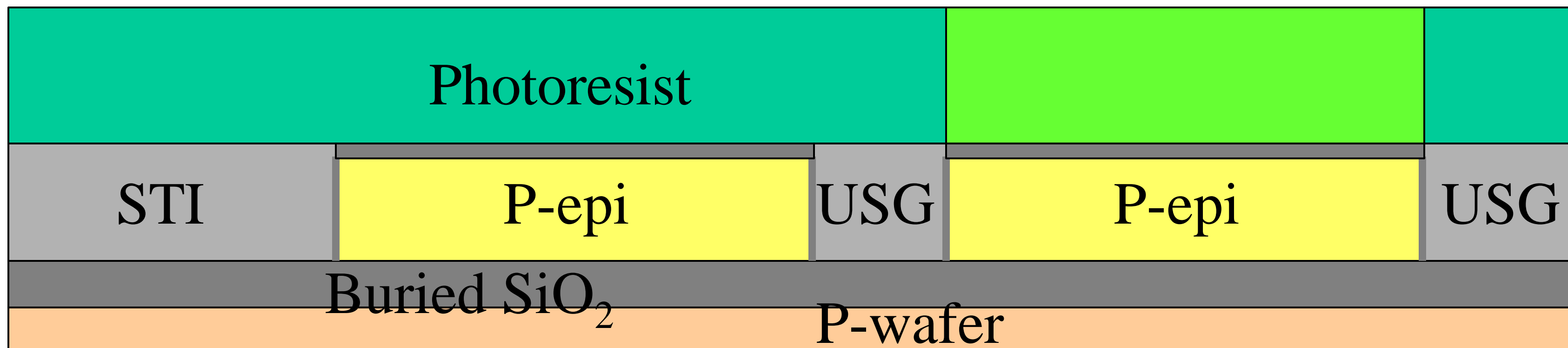
Photoresist Coating and Baking



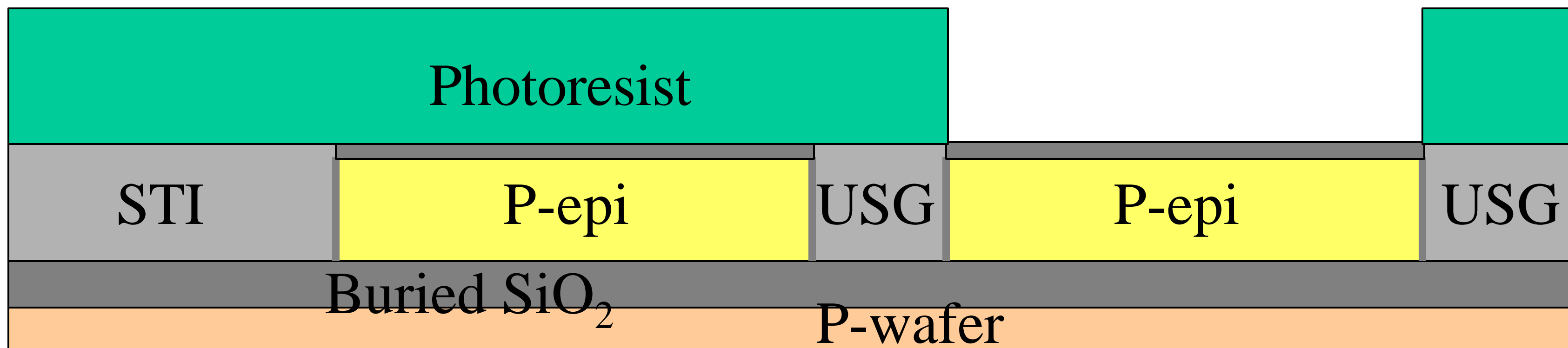
Mask 2: N-well



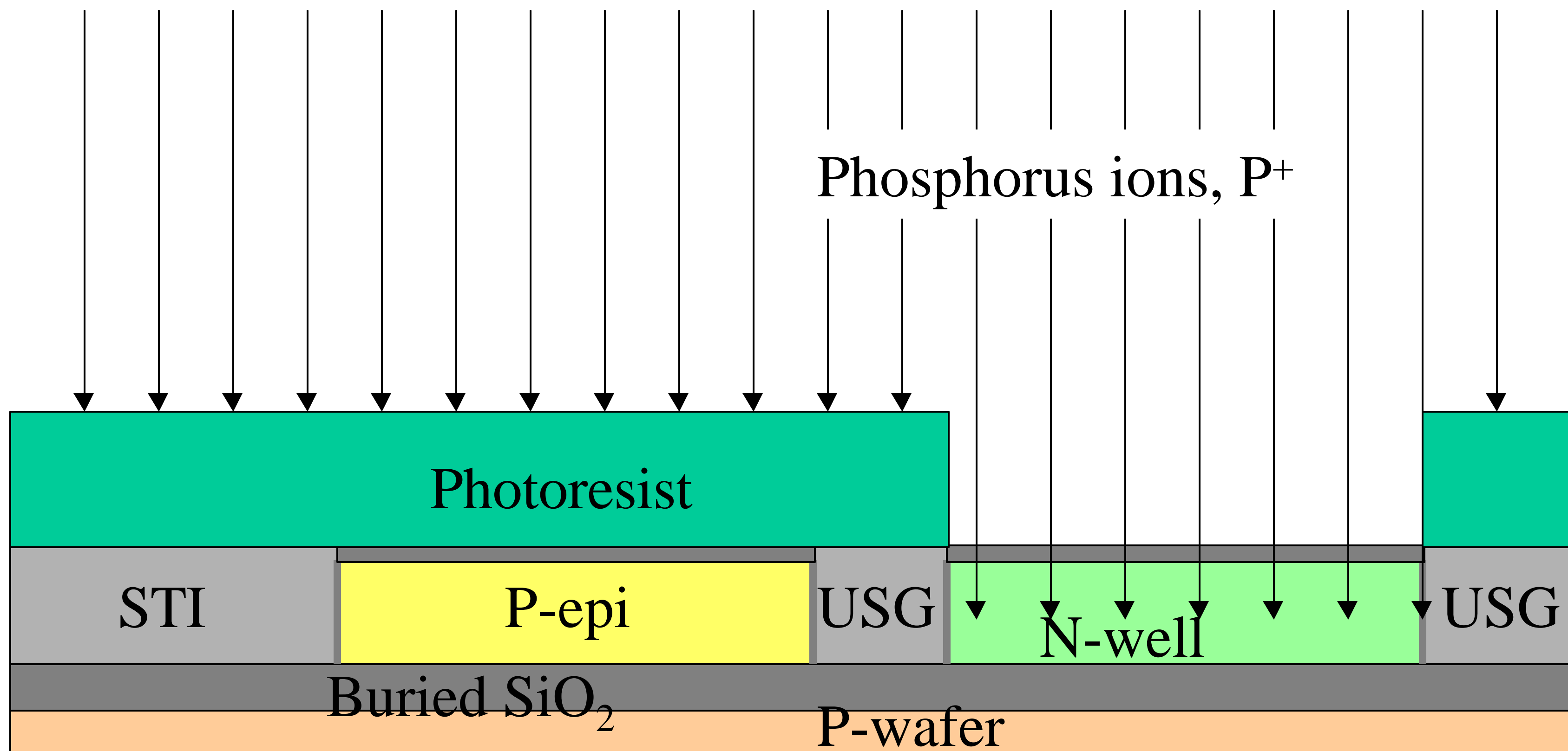
Alignment and Exposure



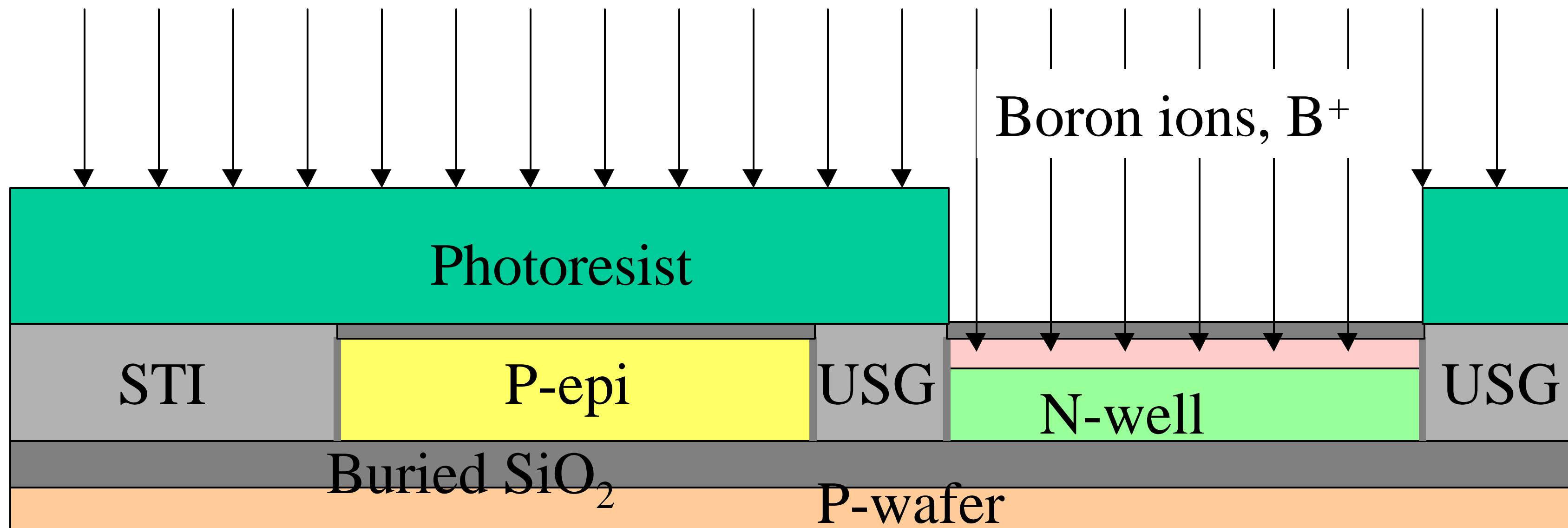
PEB, Development, and Inspection



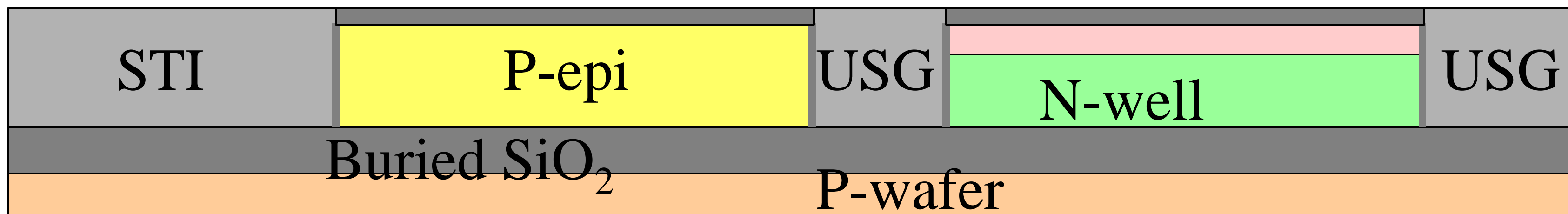
N-well Implantations



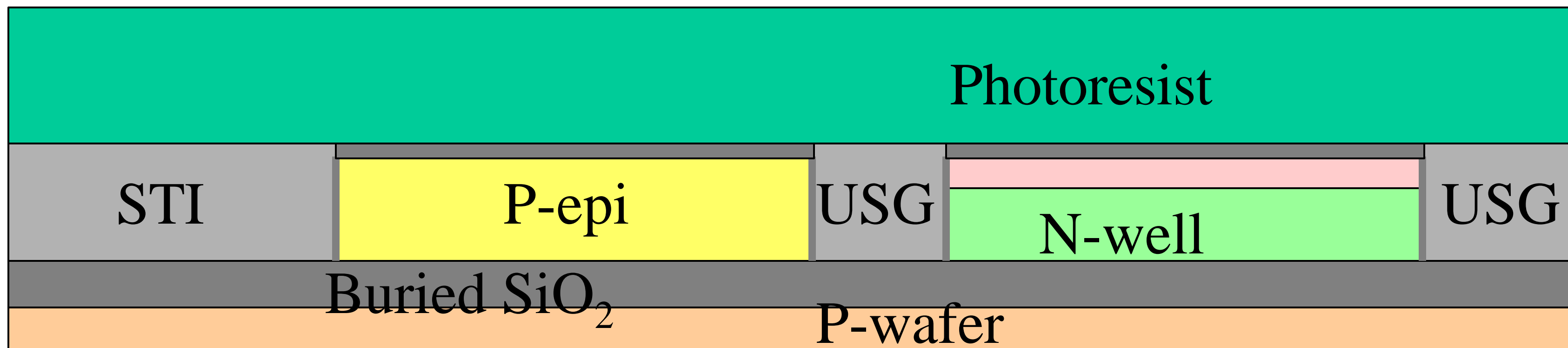
PMOS V_T Adjust Implantation



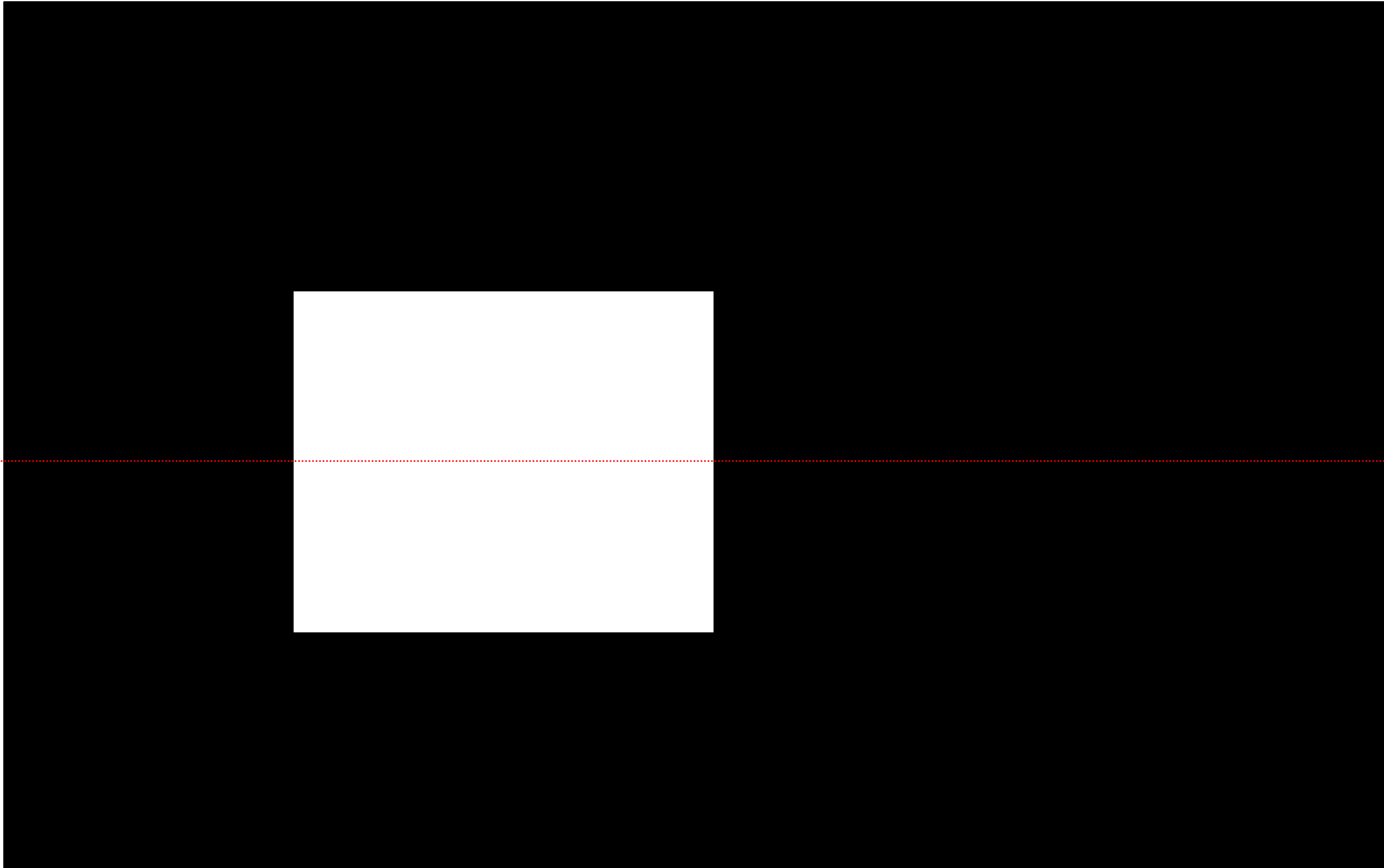
Strip Photoresist



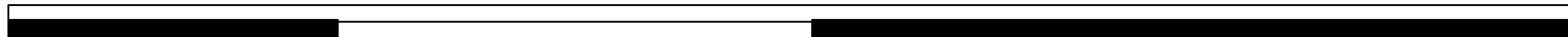
Photoresist Coating and Baking

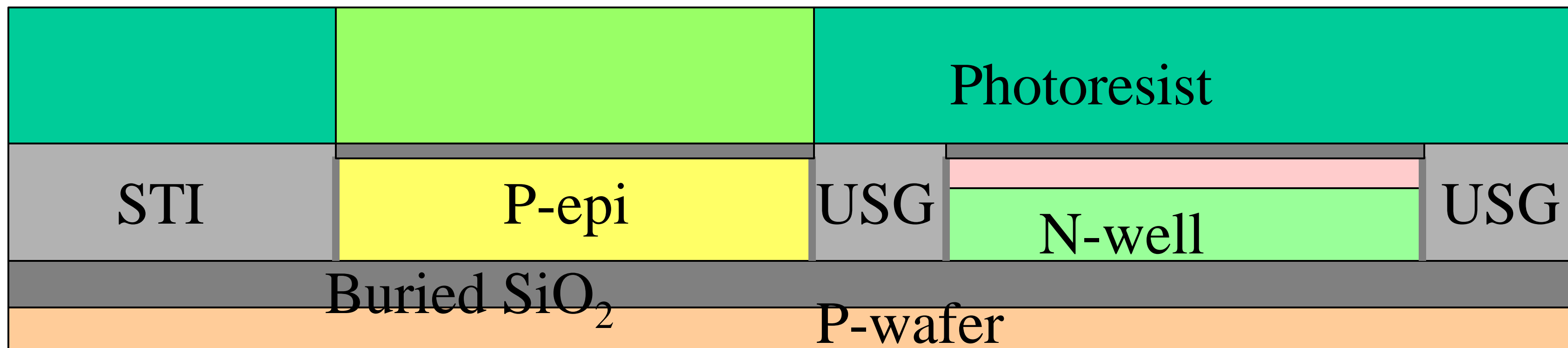


Mask 3: P-well

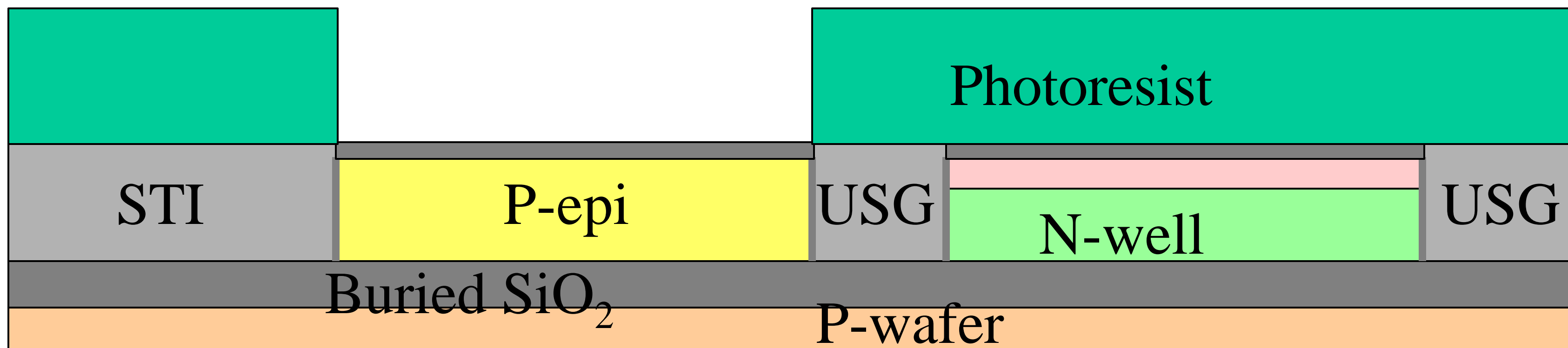


Alignment and Exposure

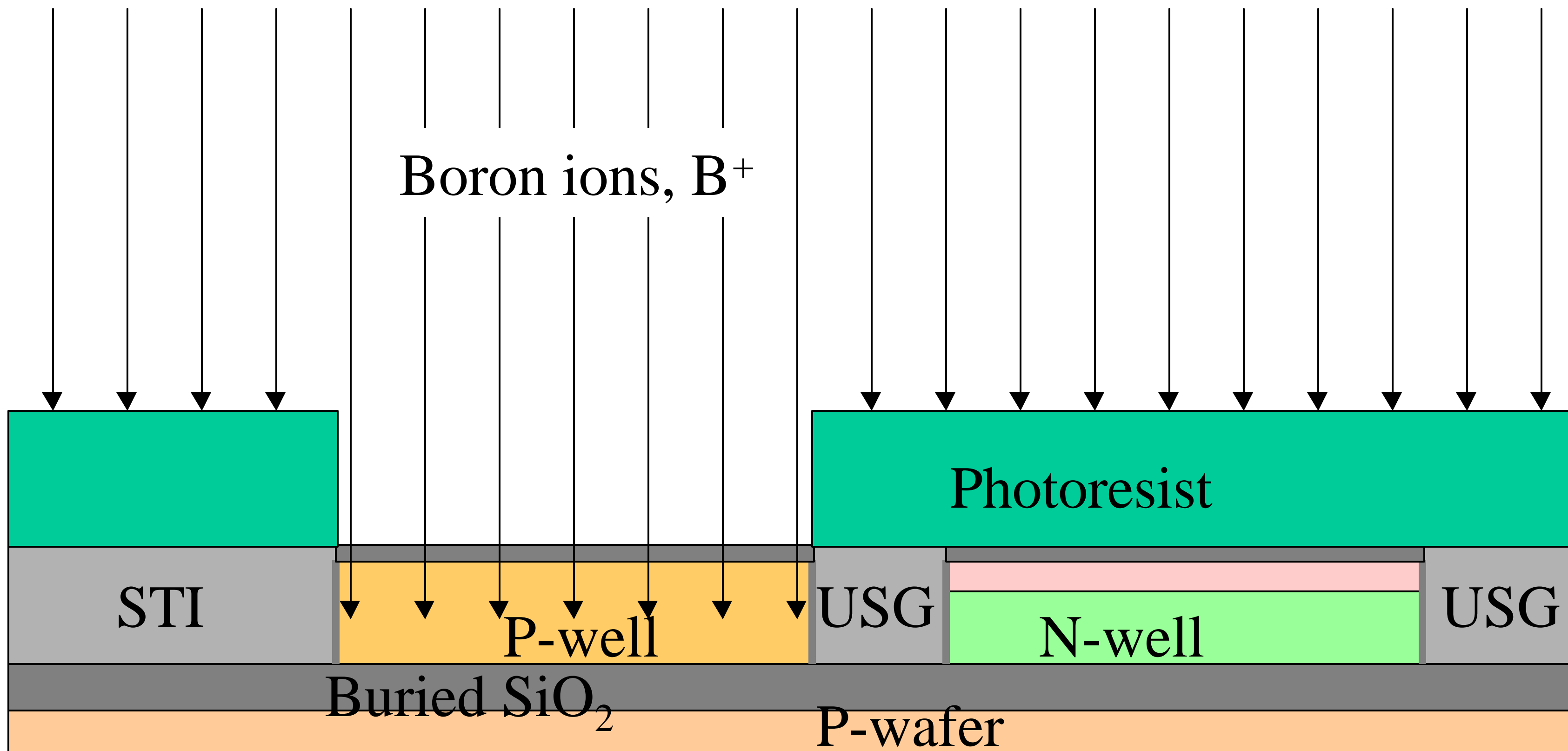




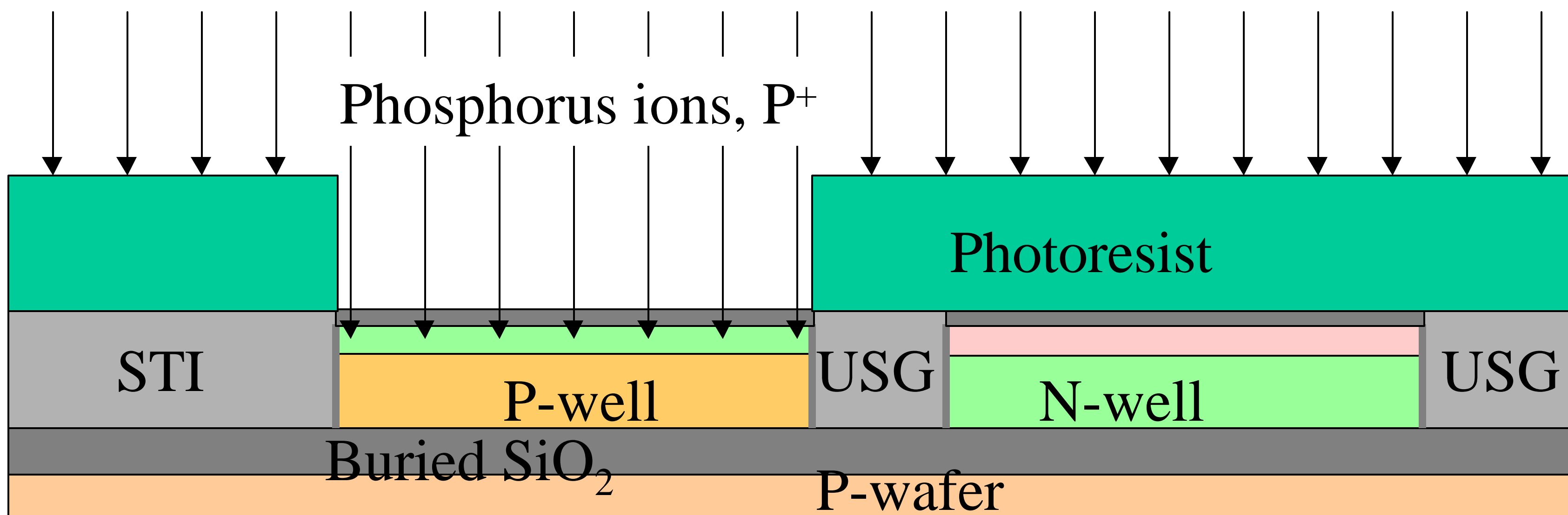
PEB, Development, and Inspection



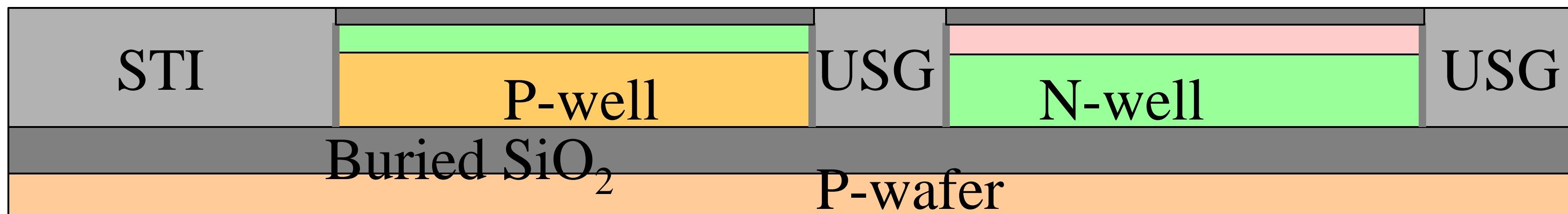
P-well Implantations



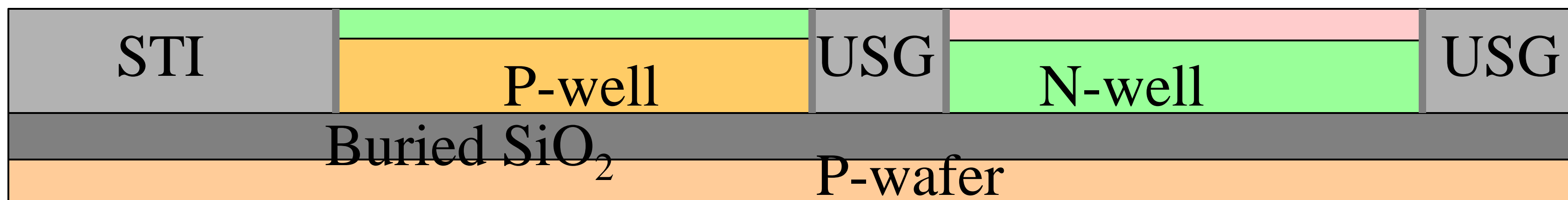
NMOS V_T Adjust Implantation



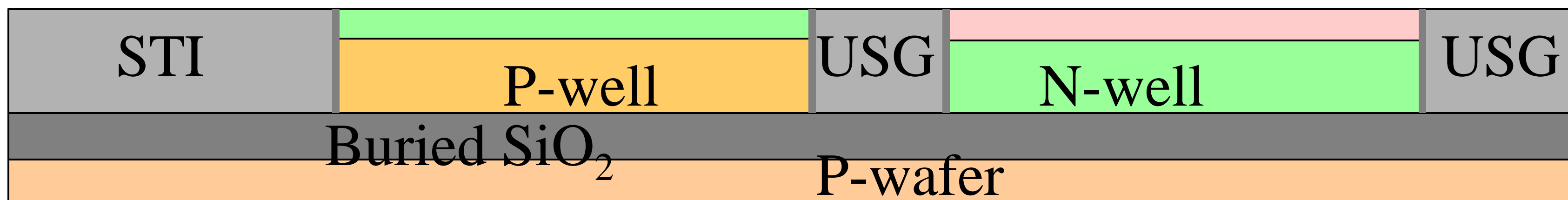
Strip Photoresist



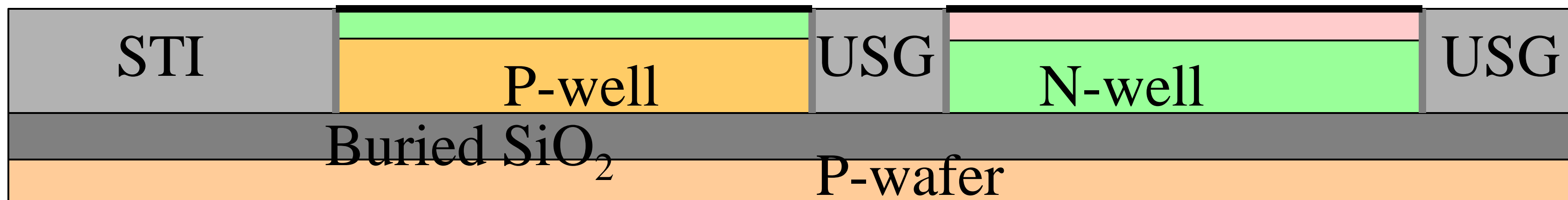
Strip Sacrificial Oxide



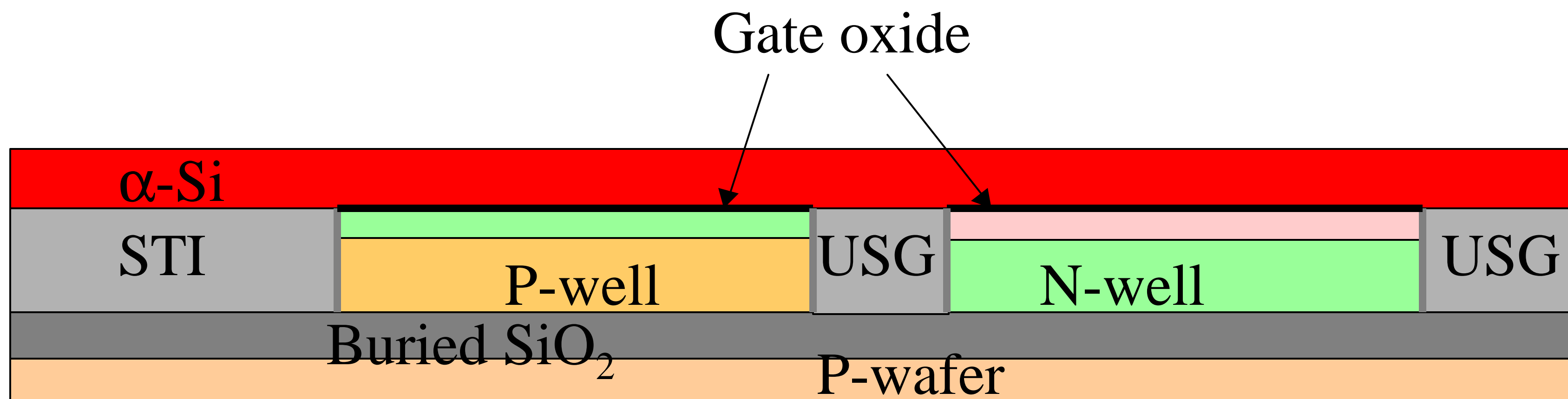
Wafer Clean



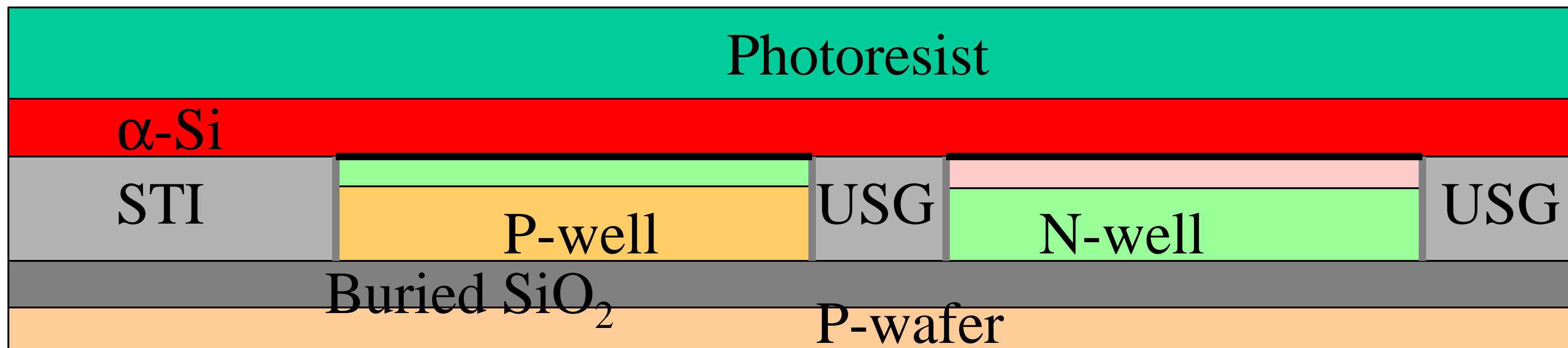
Gate Oxidation



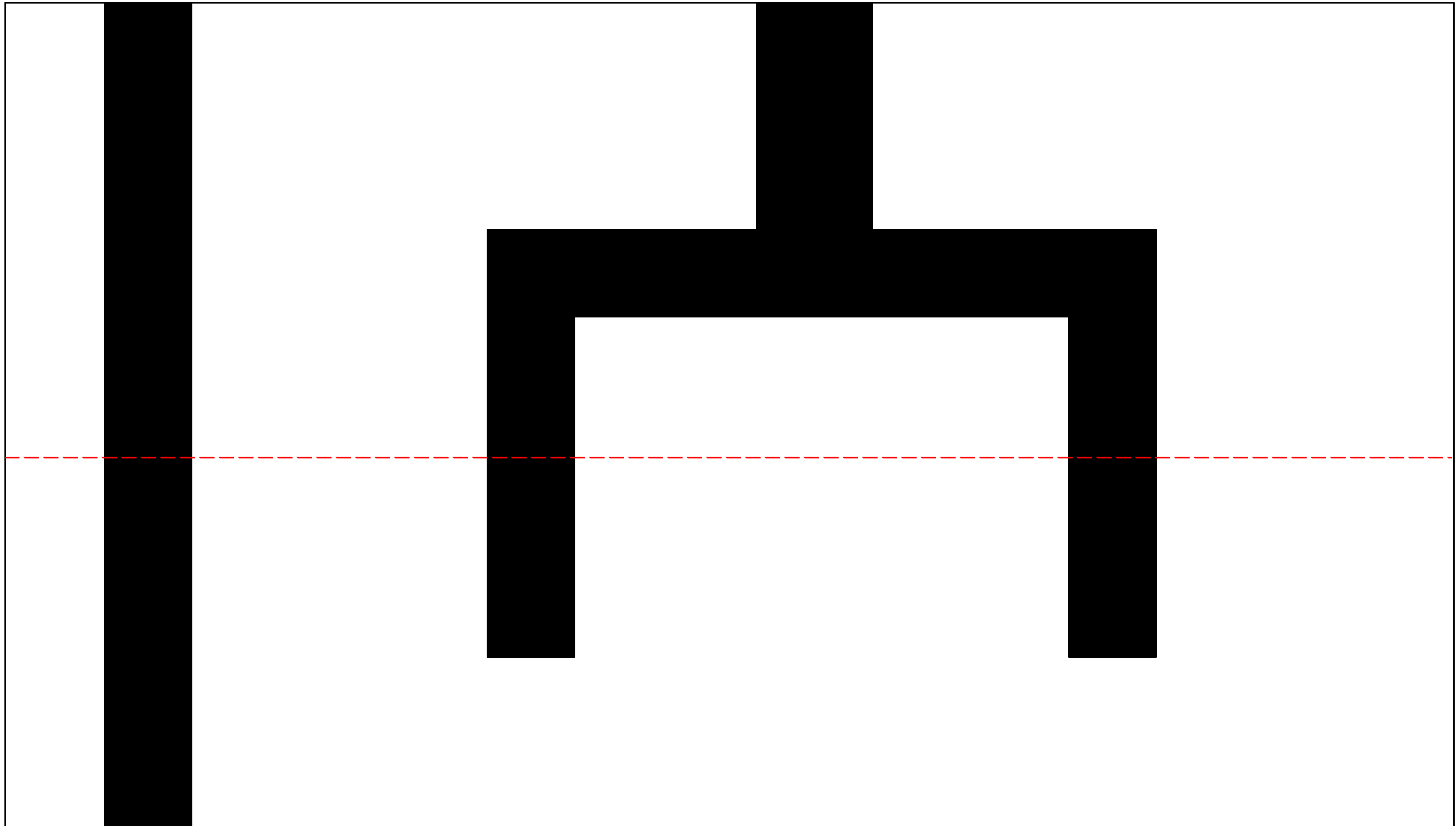
LPCVD Amorphous Silicon



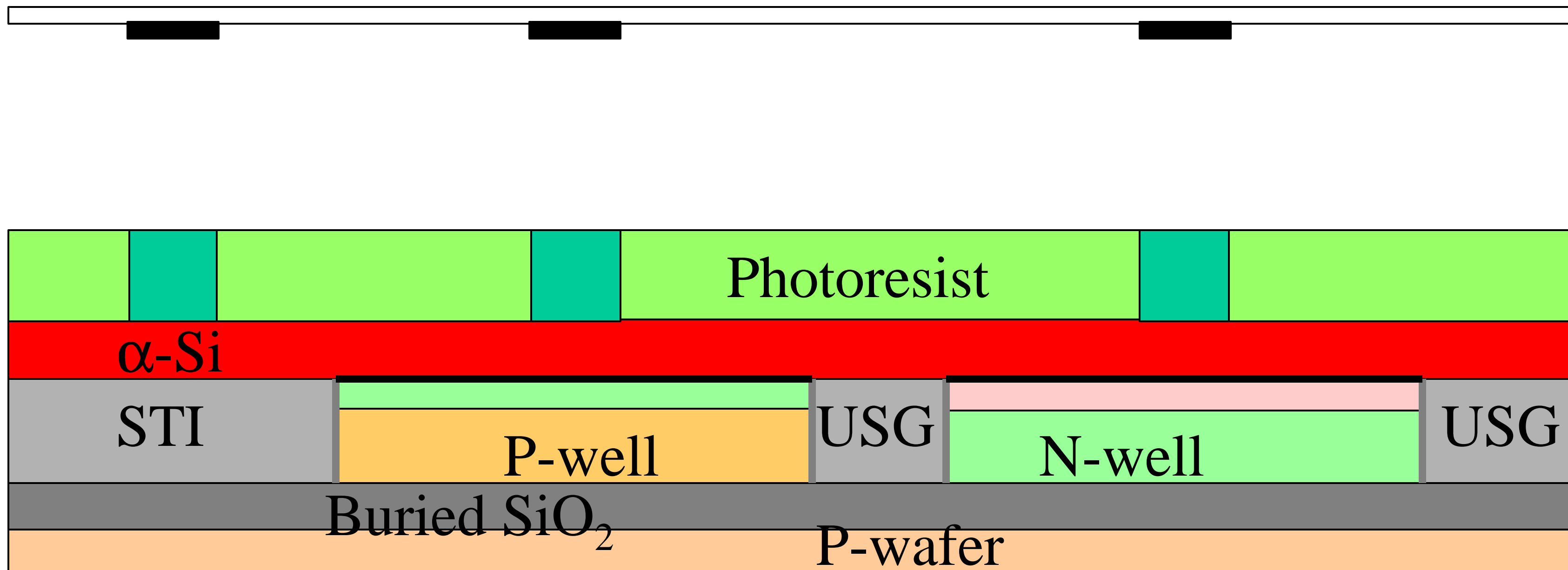
Photoresist Coating and Baking



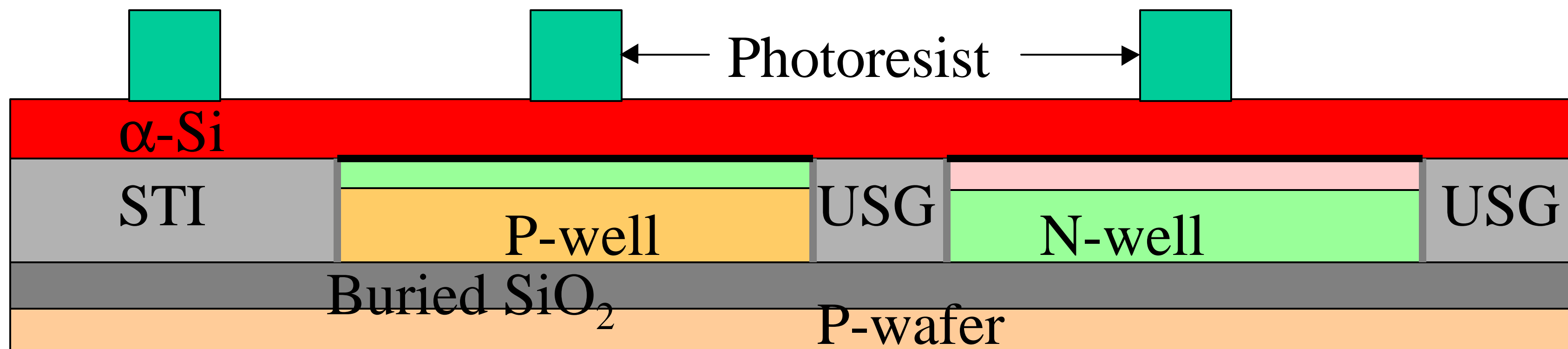
Mask 4, Gate and Local Interconnection



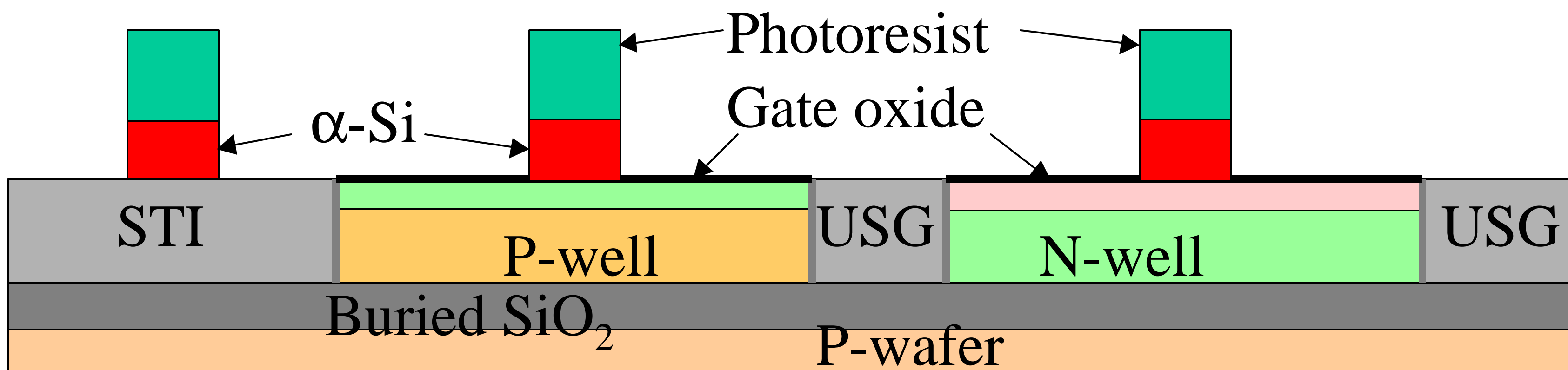
Alignment and Exposure



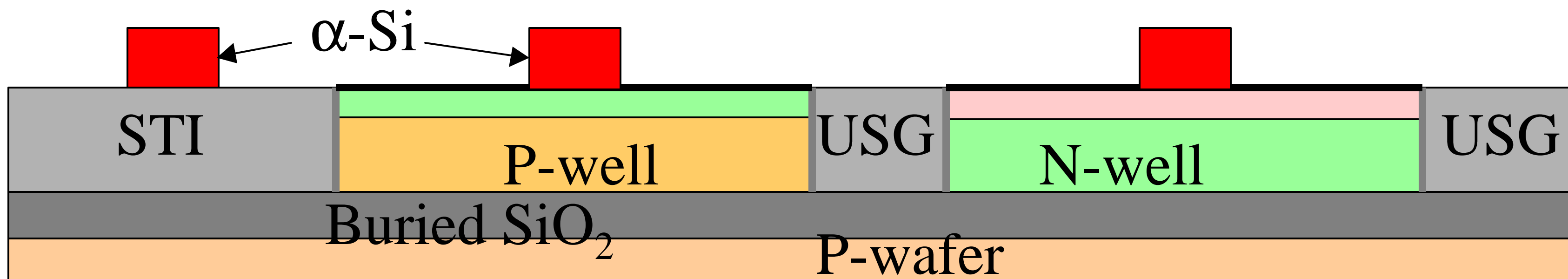
PEB, Development, and Inspection



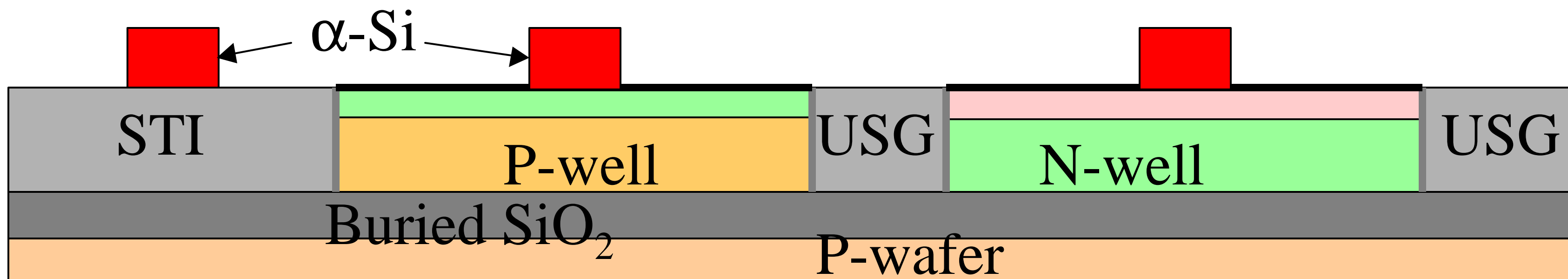
Etch Amorphous Silicon



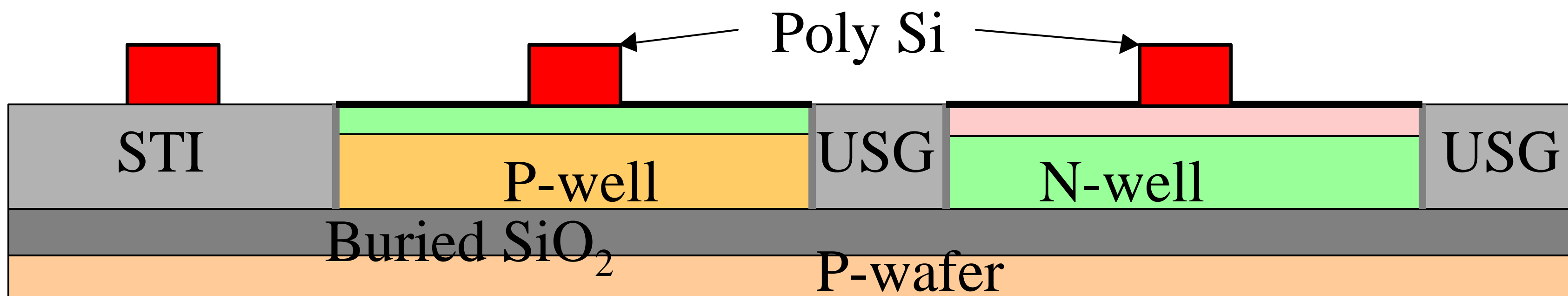
Strip Photoresist



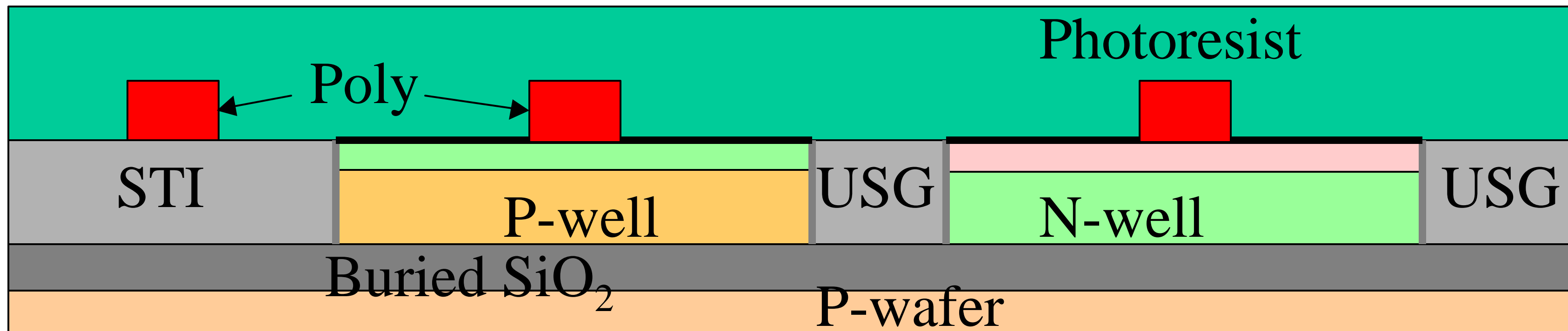
Wafer Clean



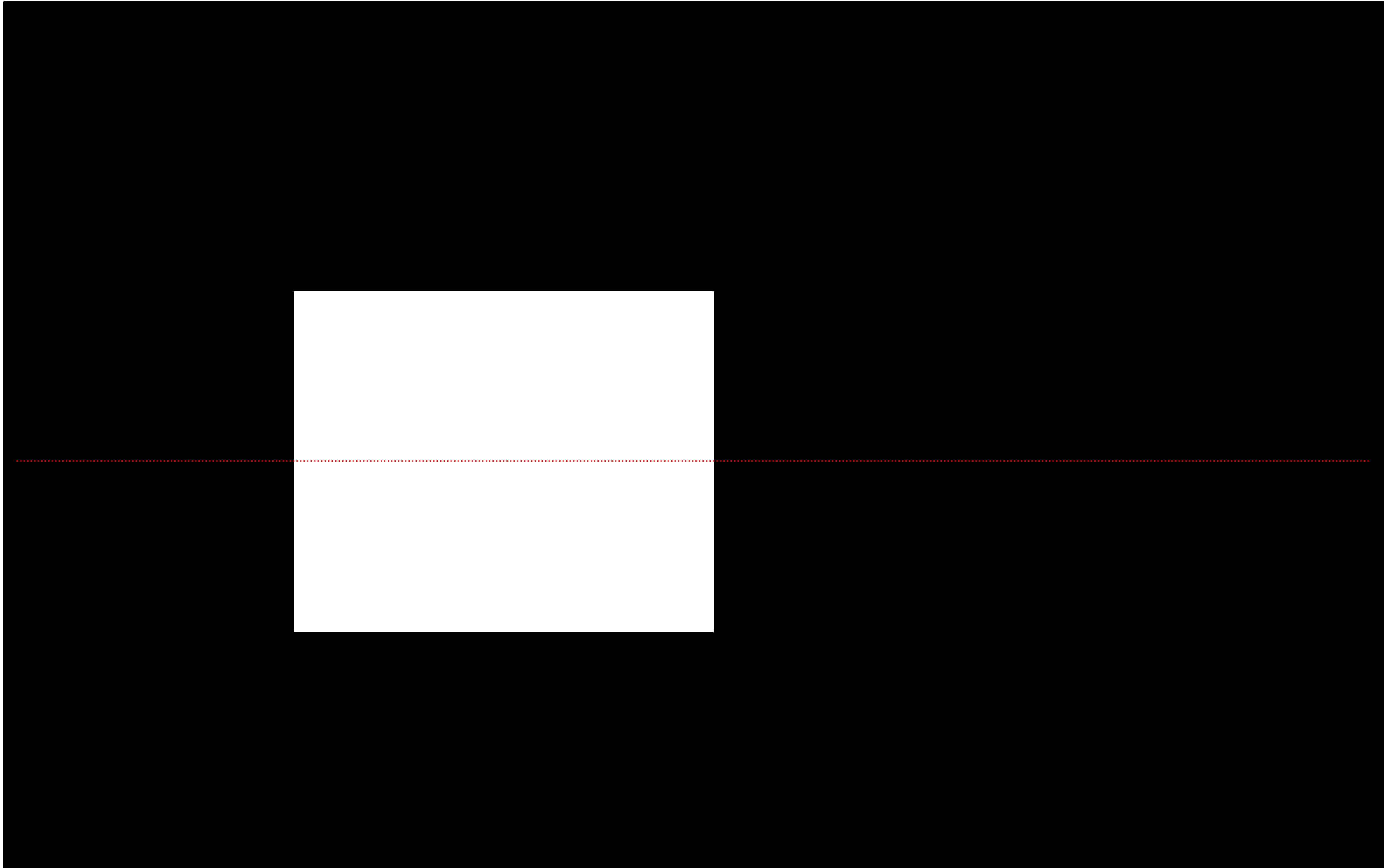
Polysilicon Annealing and Oxidation



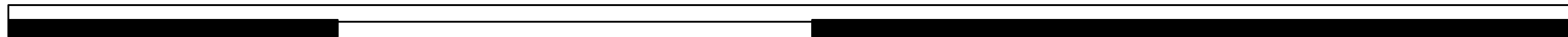
Photoresist Coating and Baking

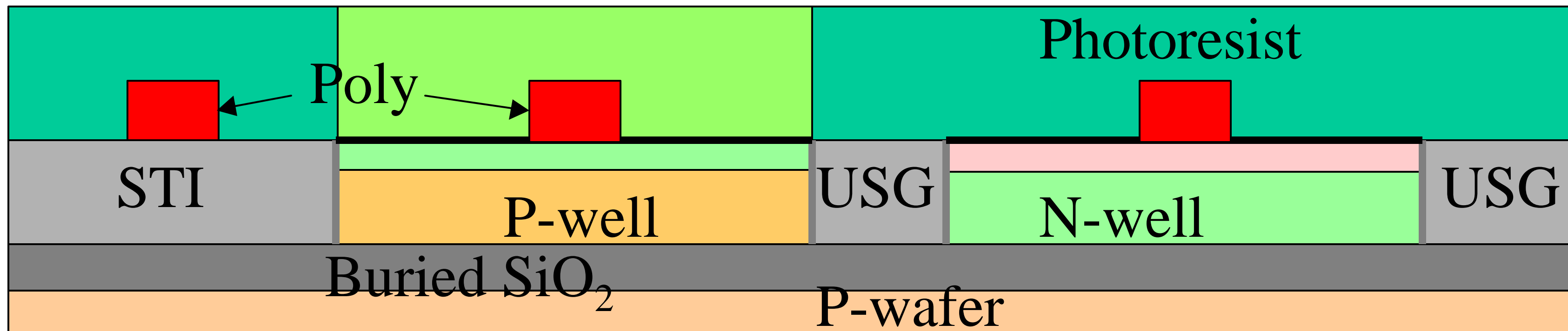


Mask 5, NMOS LDD Implantation

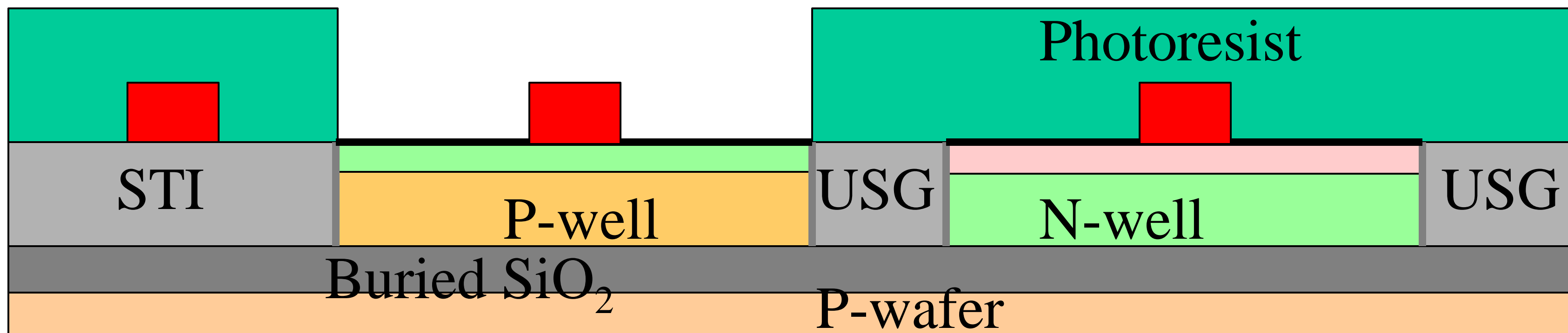


Alignment and Exposure

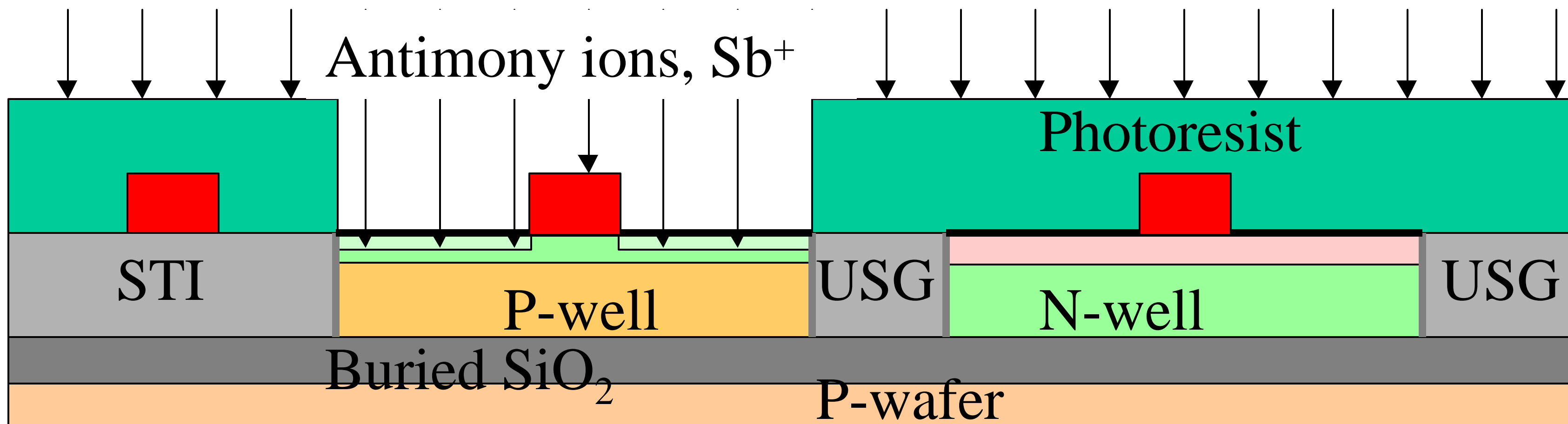




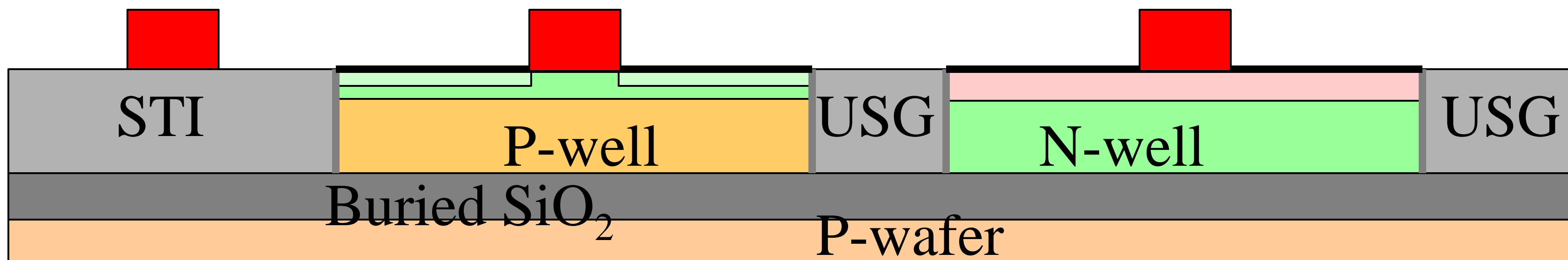
PEB, Development, and Inspection



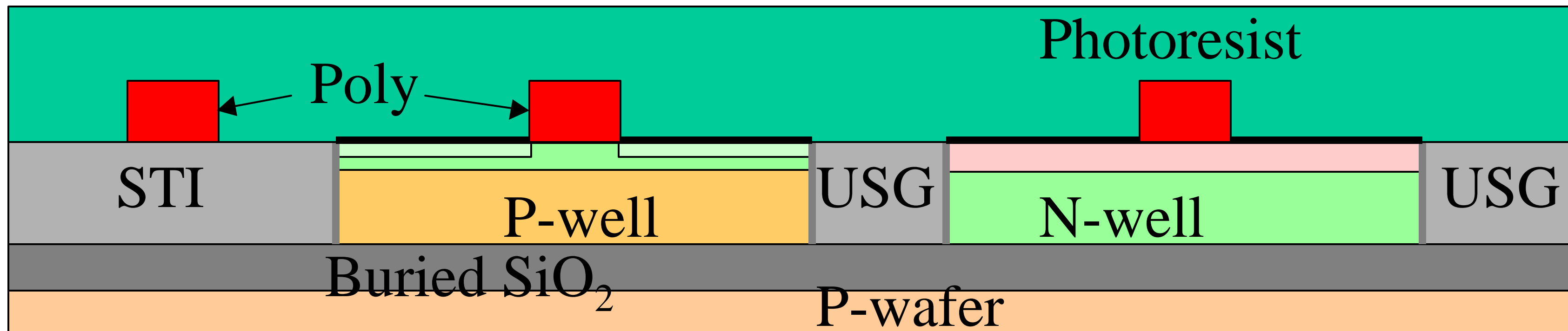
NMOS LDD Implantation



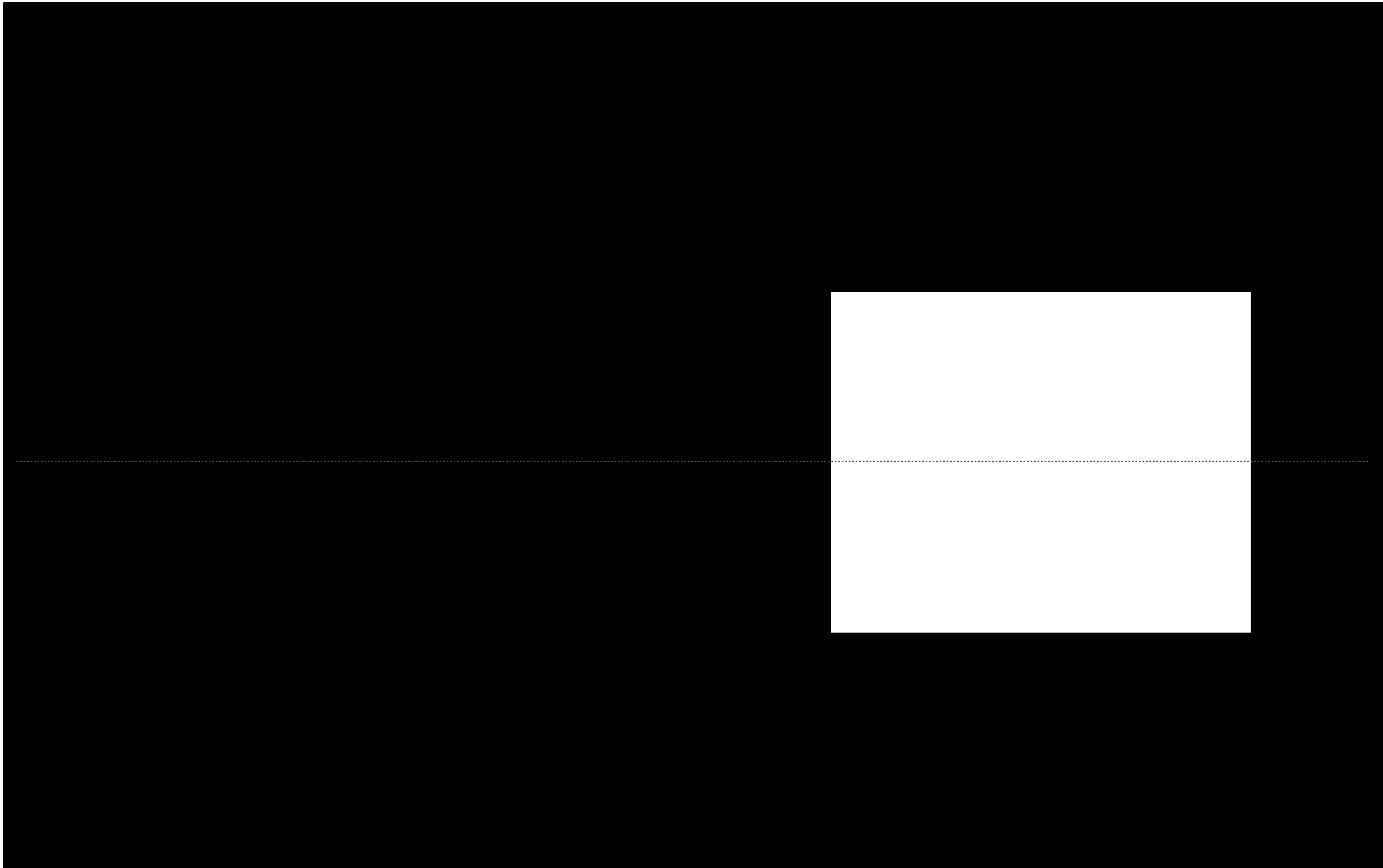
Strip Photoresist



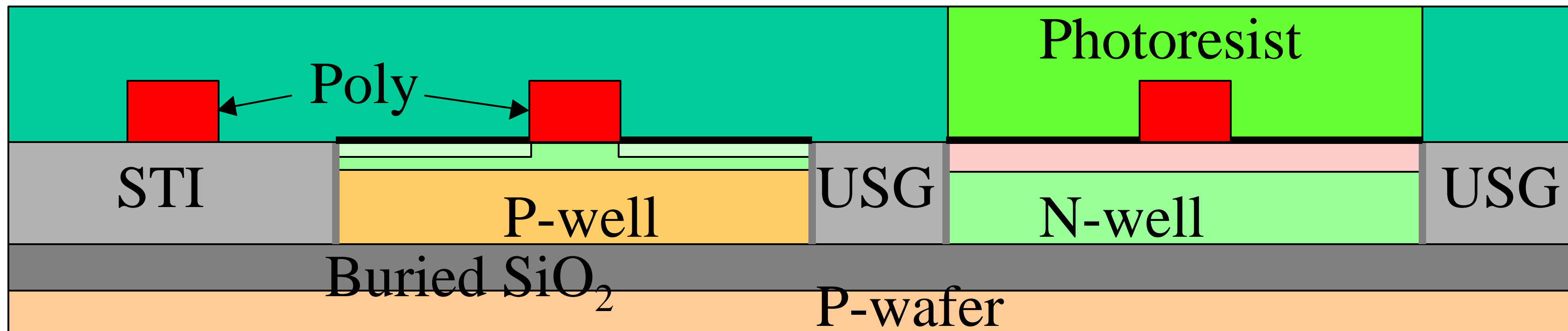
Photoresist Coating and Baking



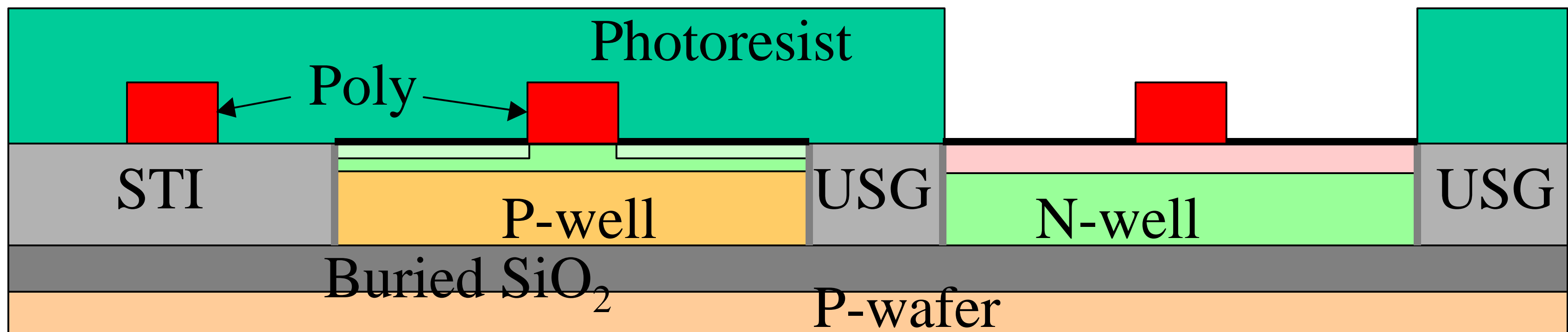
Mask 6: PMOS LDD Implantation



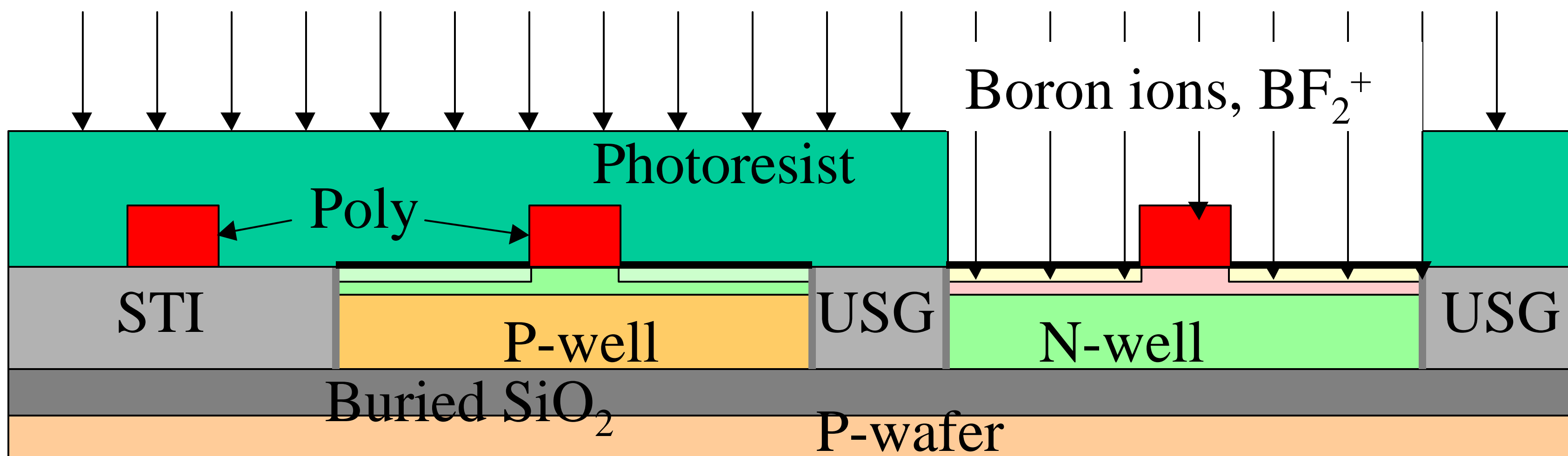
Alignment and Exposure



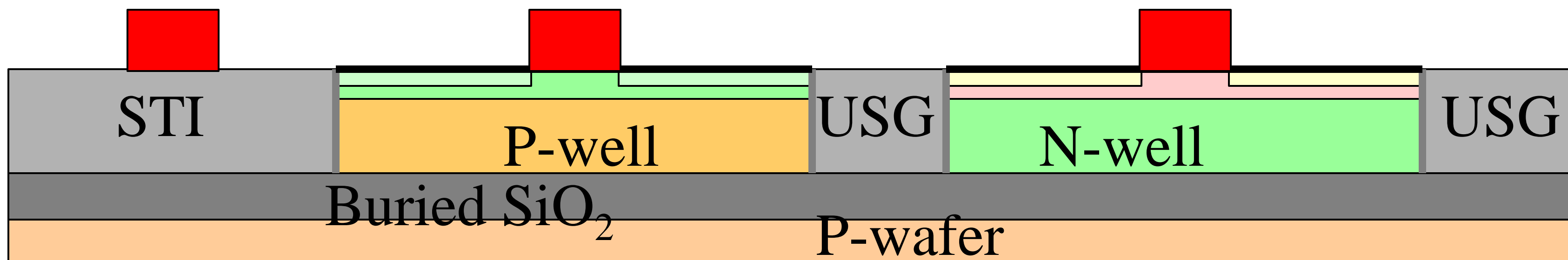
PEB, Development, and Inspection



PMOS LDD Implantation



Strip Photoresist



CVD USG, CVD Nitride

STI

P-well

USG

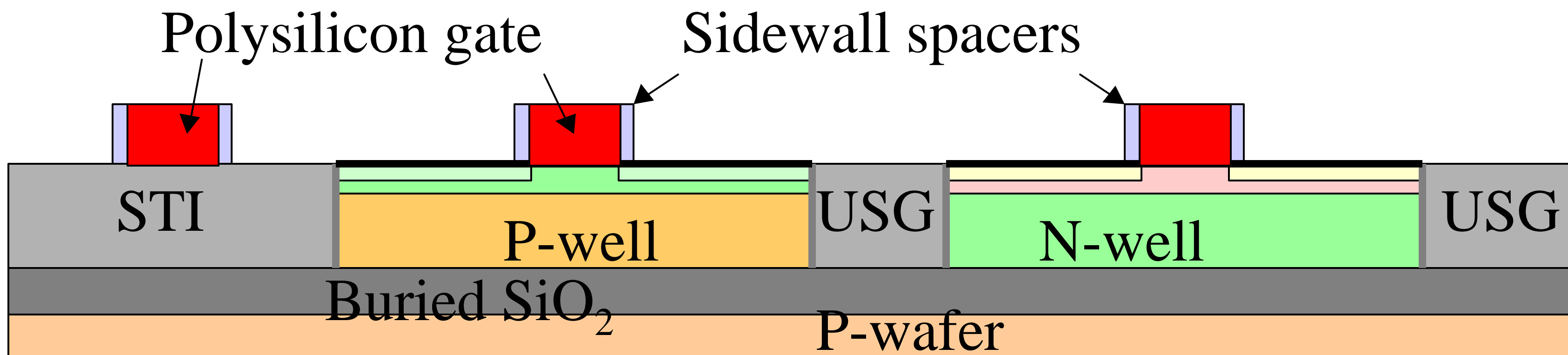
N-well

USG

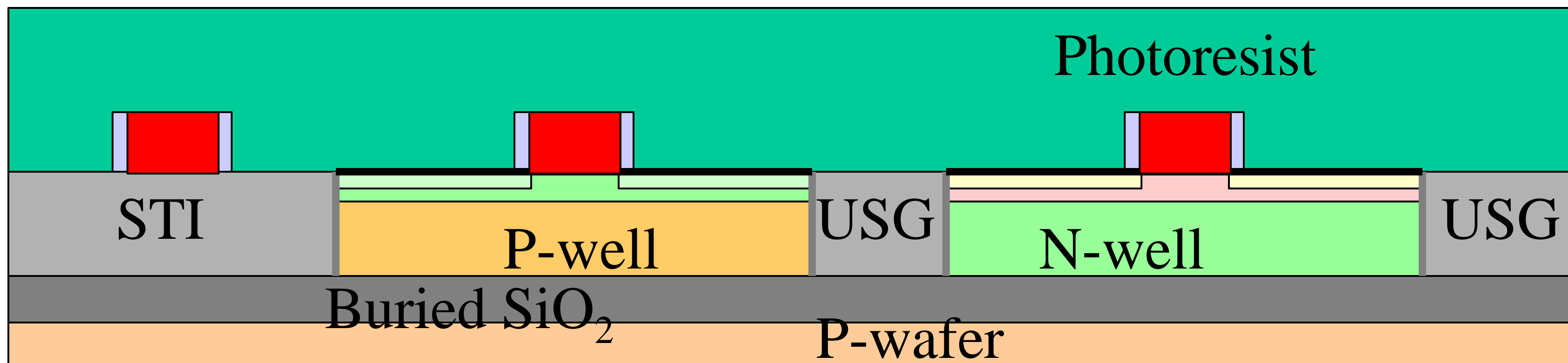
Buried SiO_2

P-wafer

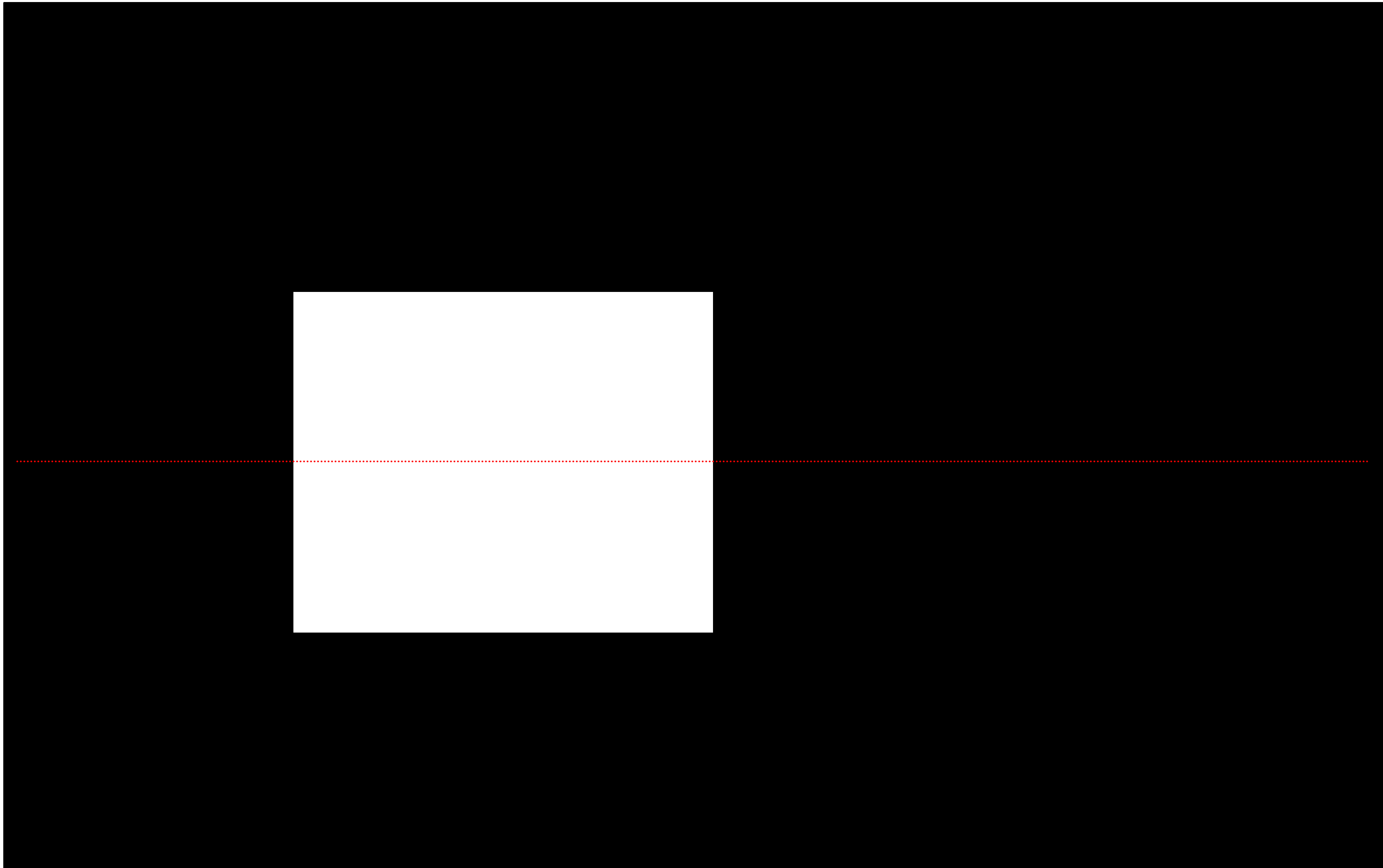
Nitride and USG Etchback



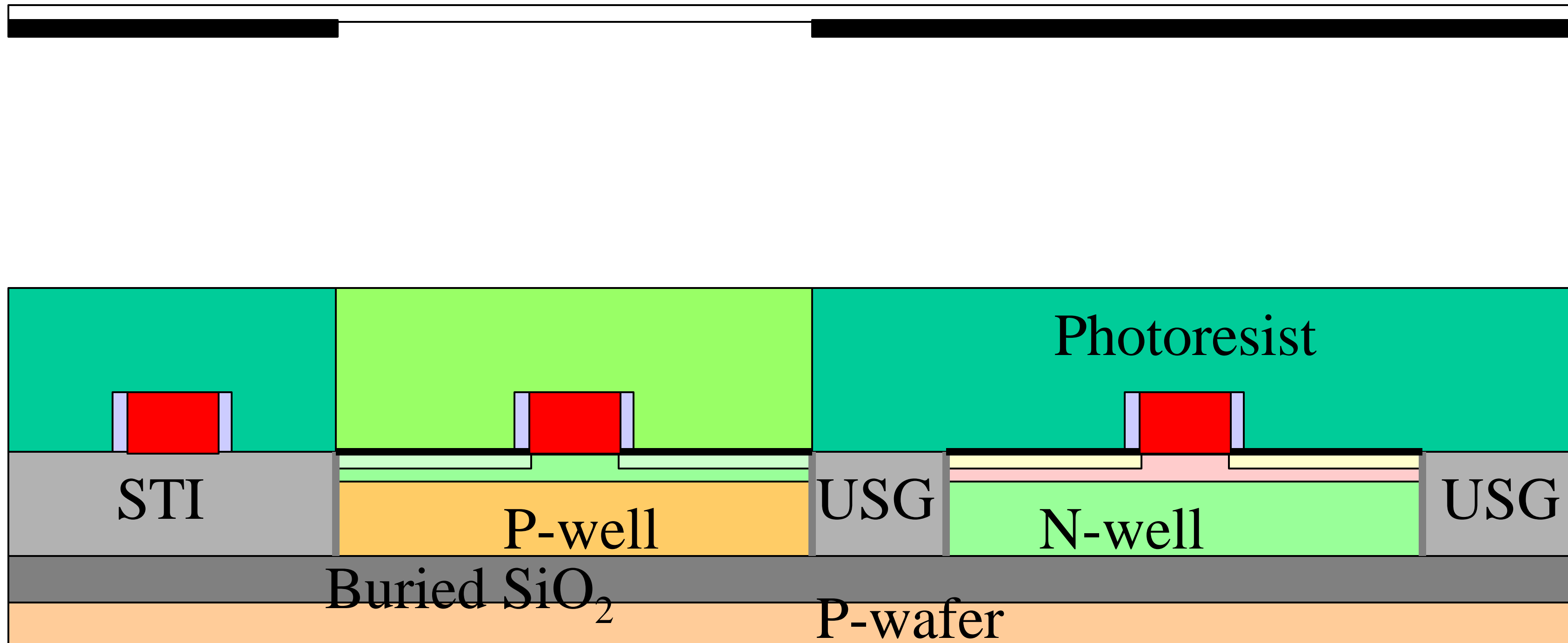
Photoresist Coating and Baking



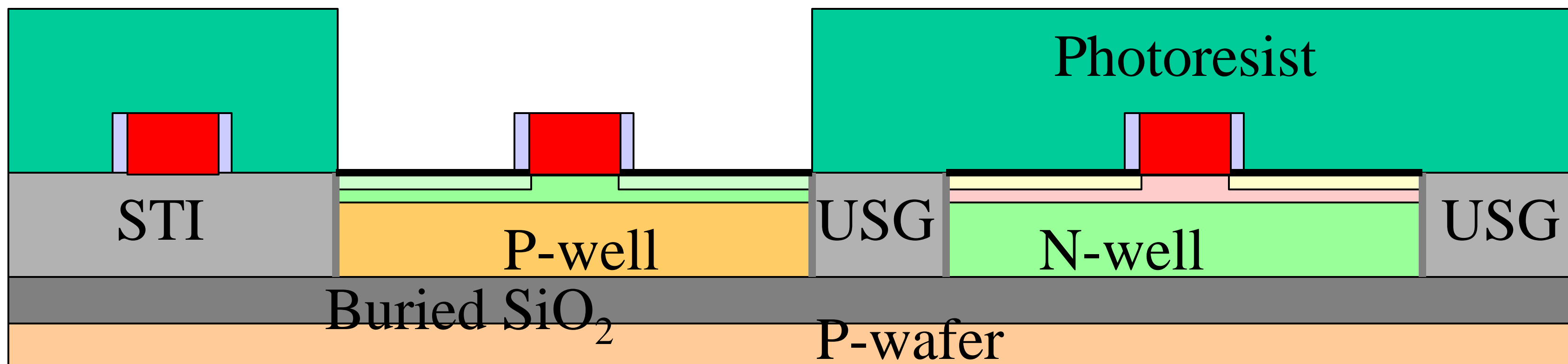
Mask 7, NMOS S/D Implantation



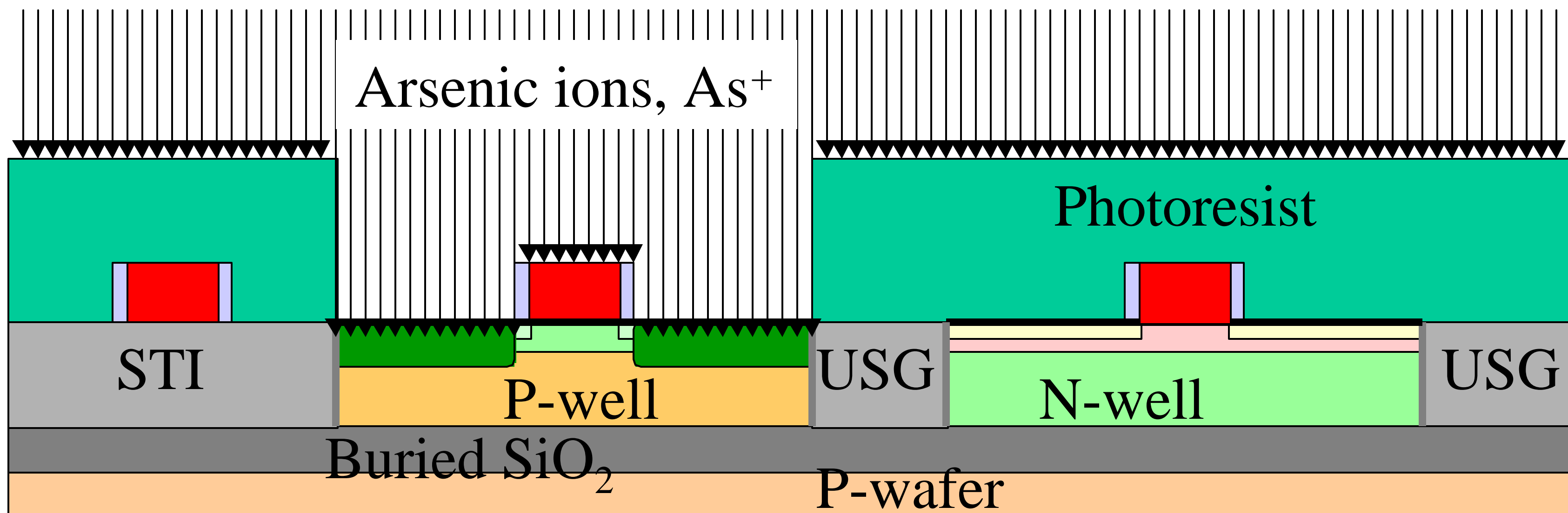
Alignment and Exposure



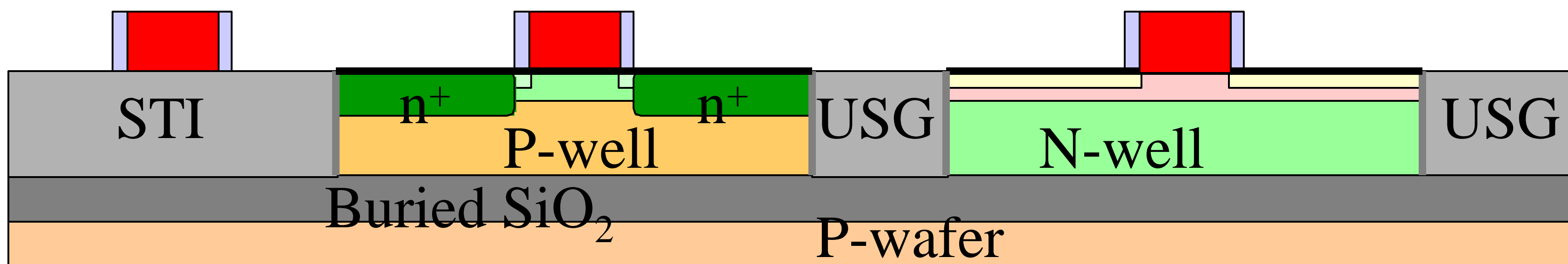
PEB, Development, and Inspection



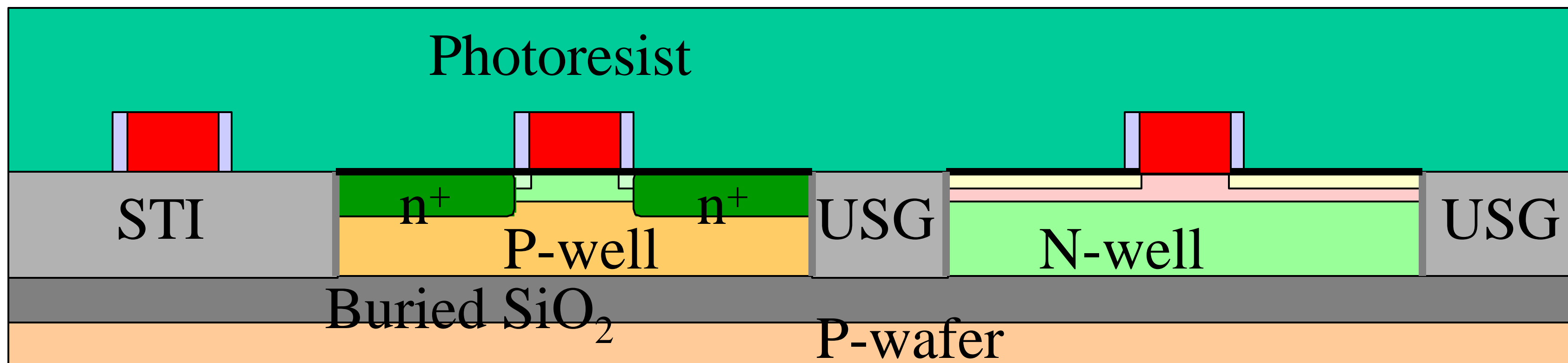
NMOS S/D Implantation



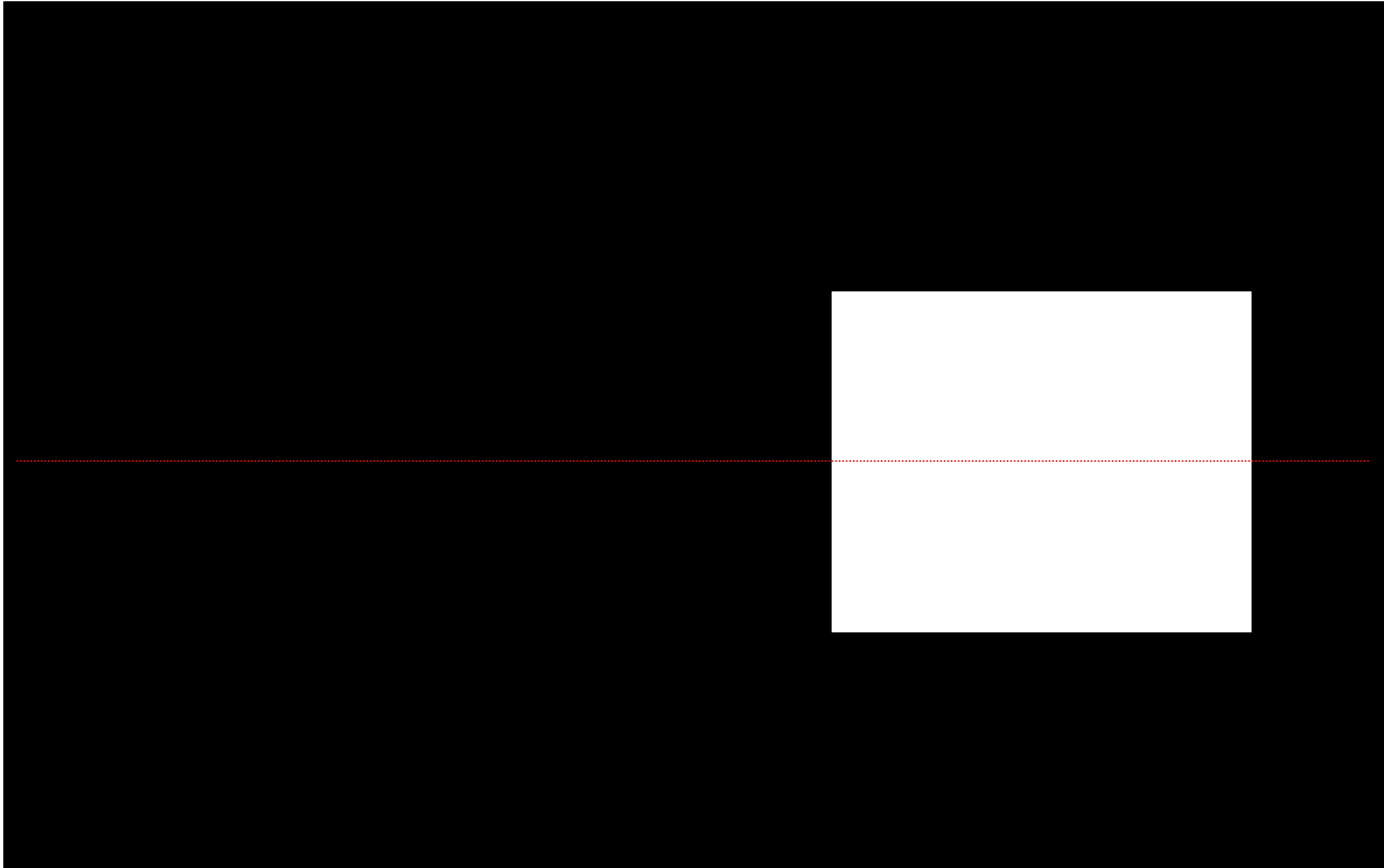
Strip Photoresist



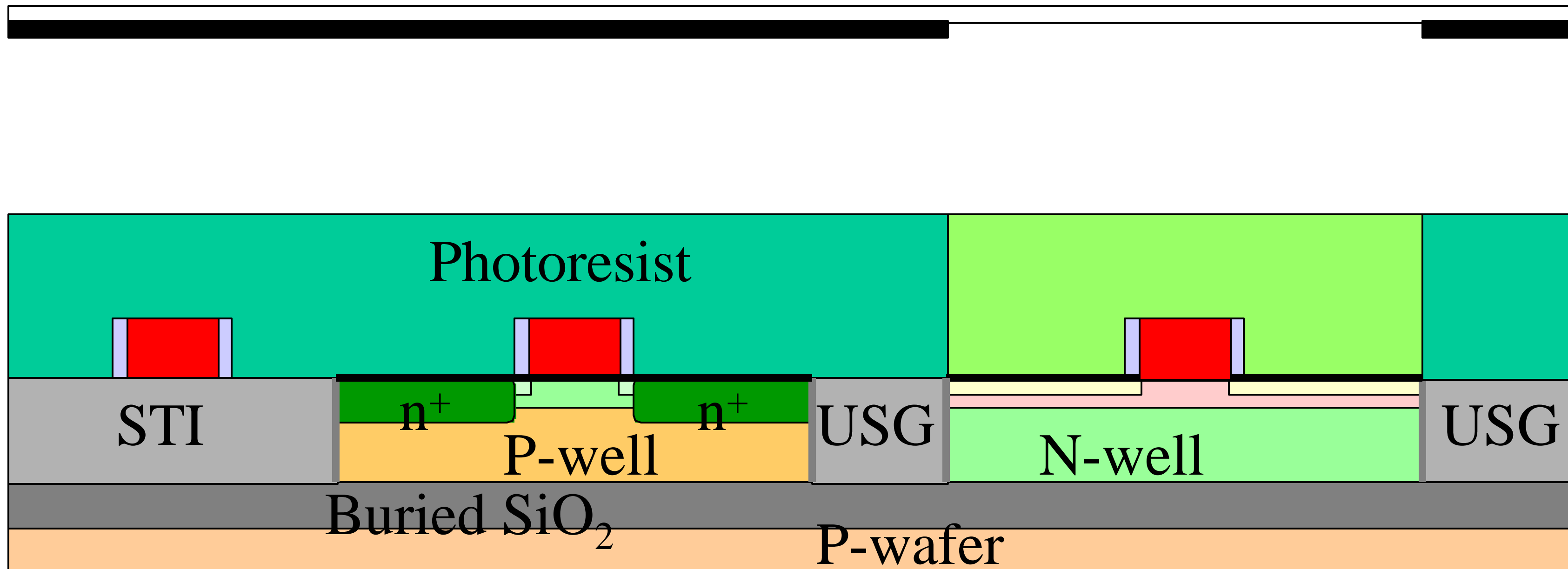
Photoresist Coating and Baking



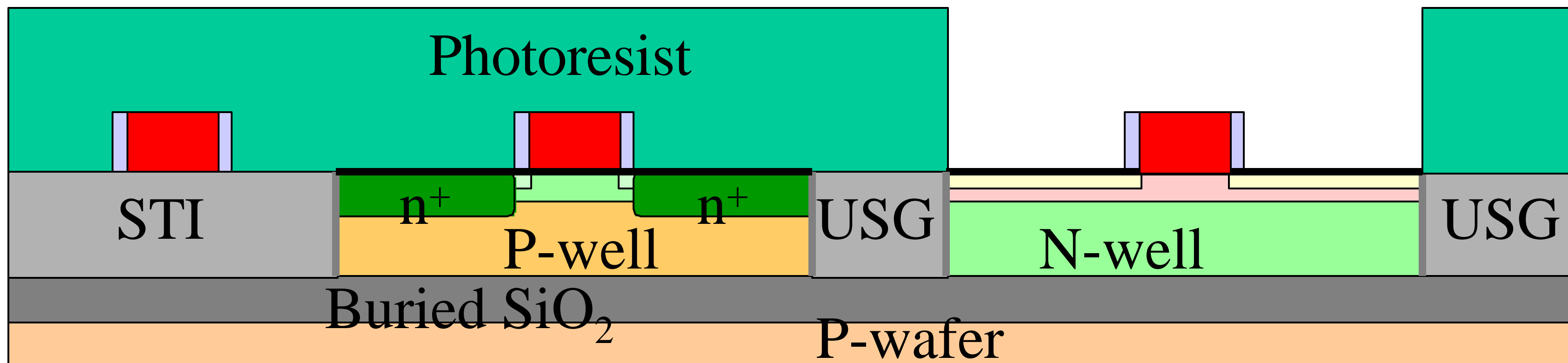
Mask 8, PMOS S/D Implantation



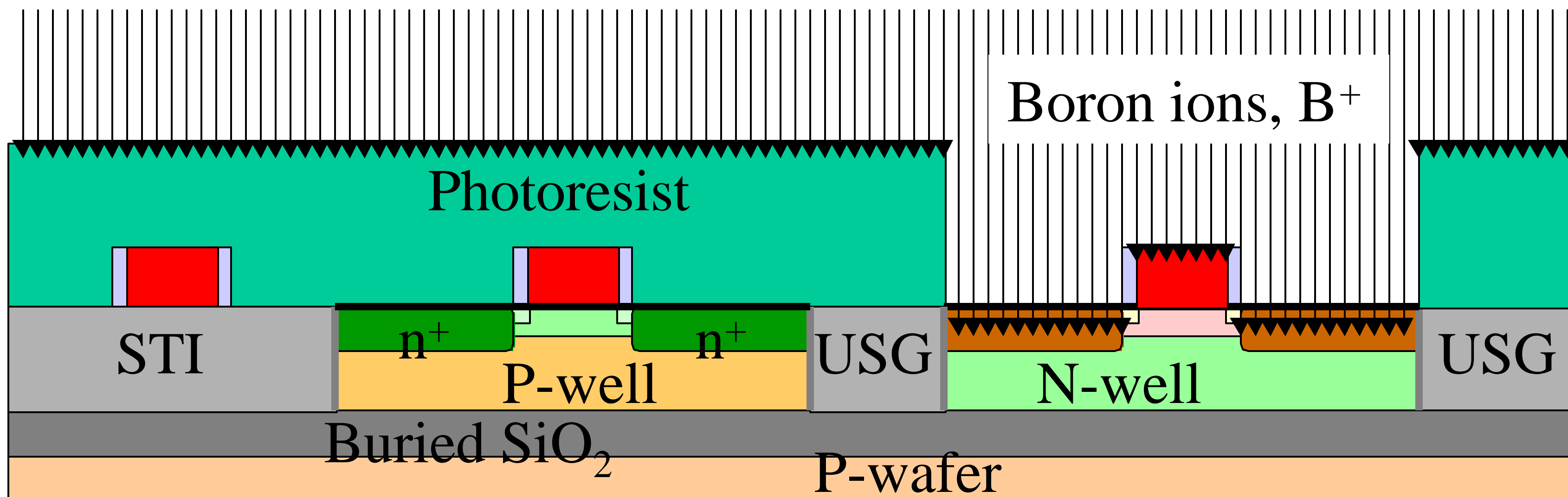
Alignment and Exposure



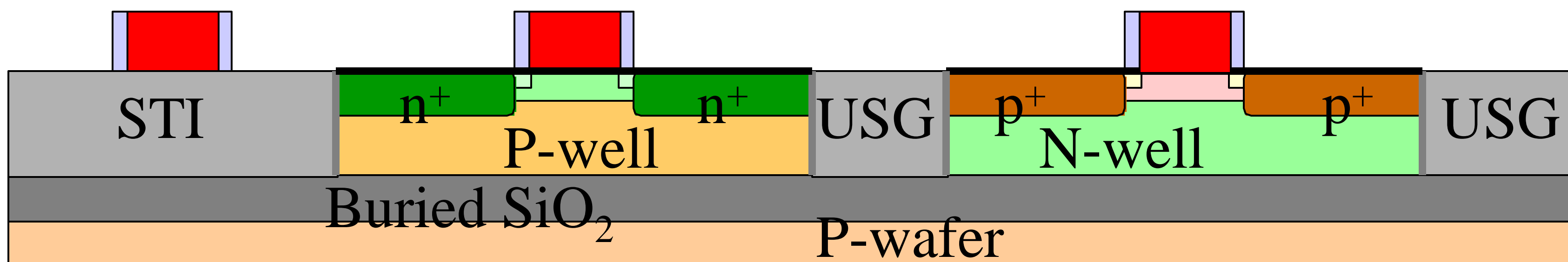
PEB, Development, and Inspection



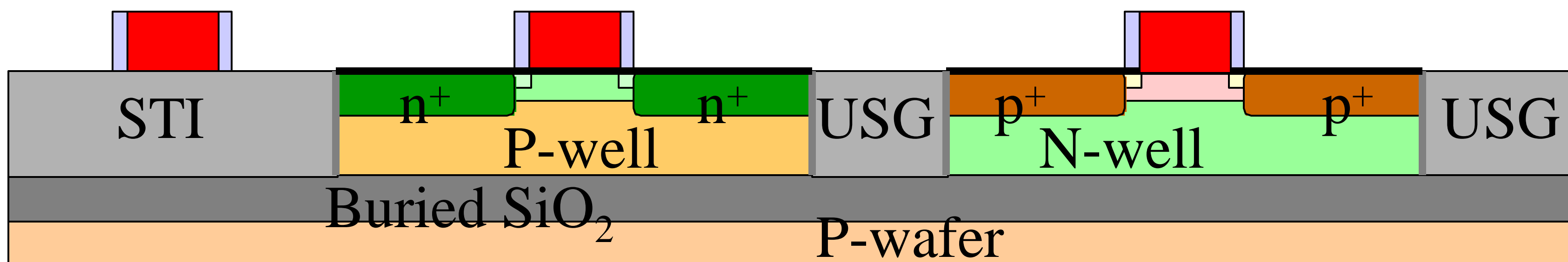
PMOS S/D Implantation



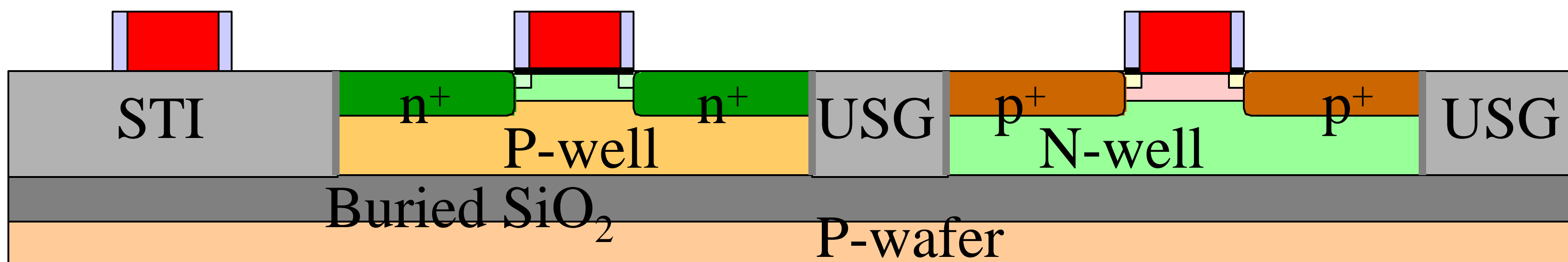
Strip Photoresist



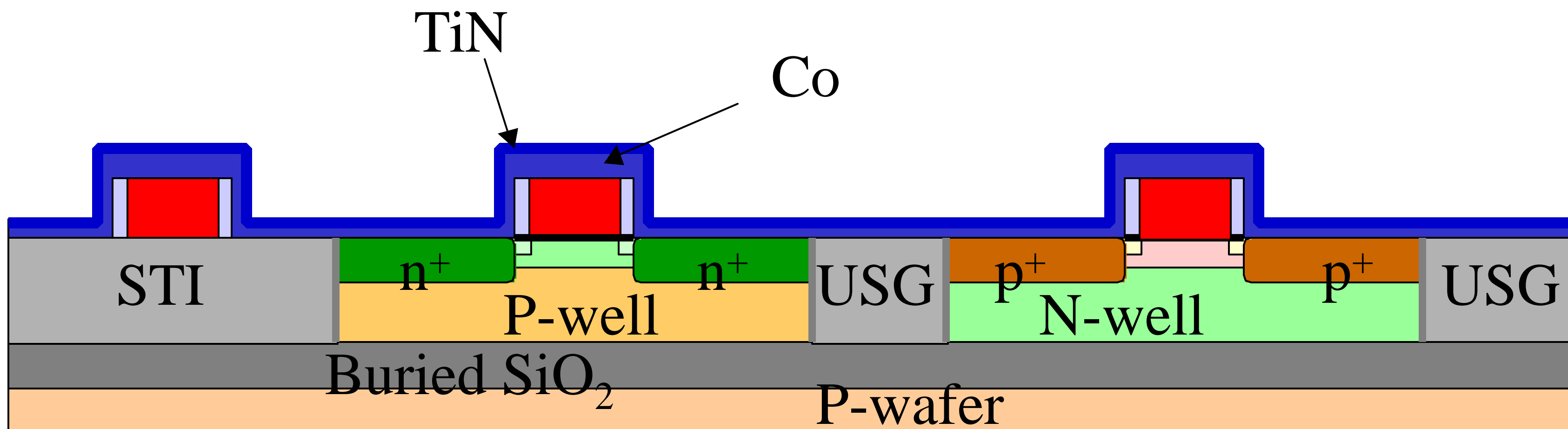
Rapid Thermal Annealing



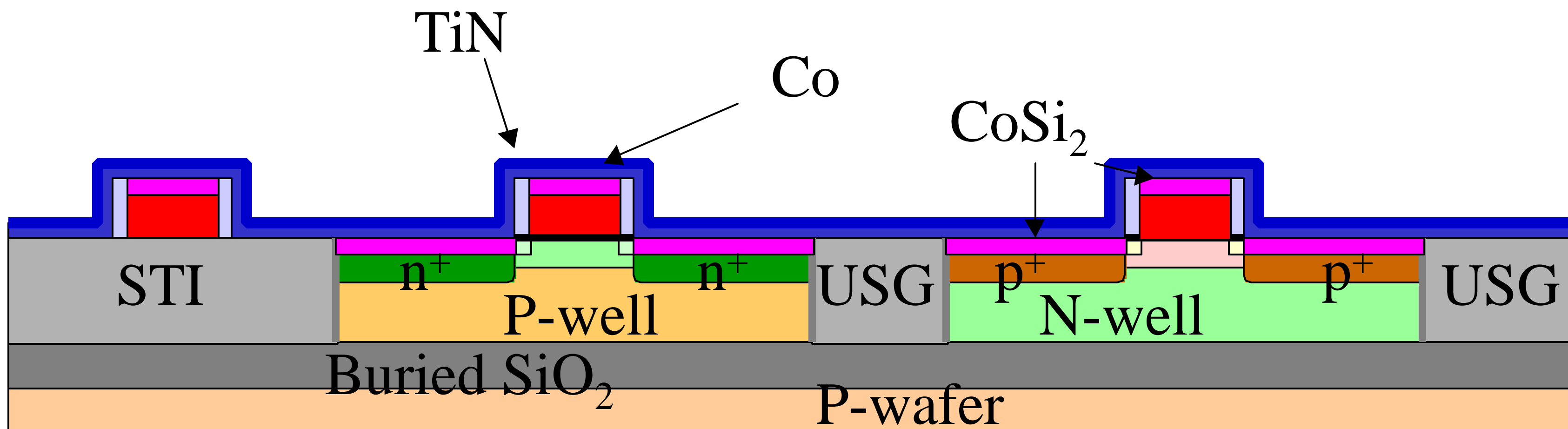
Argon Sputtering Etch



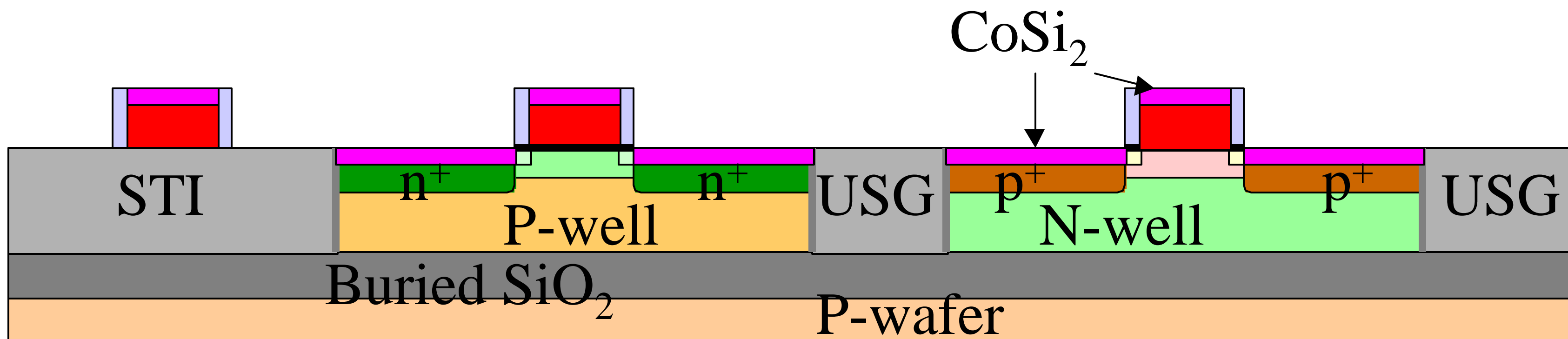
Co and TiN Sputtering Deposition



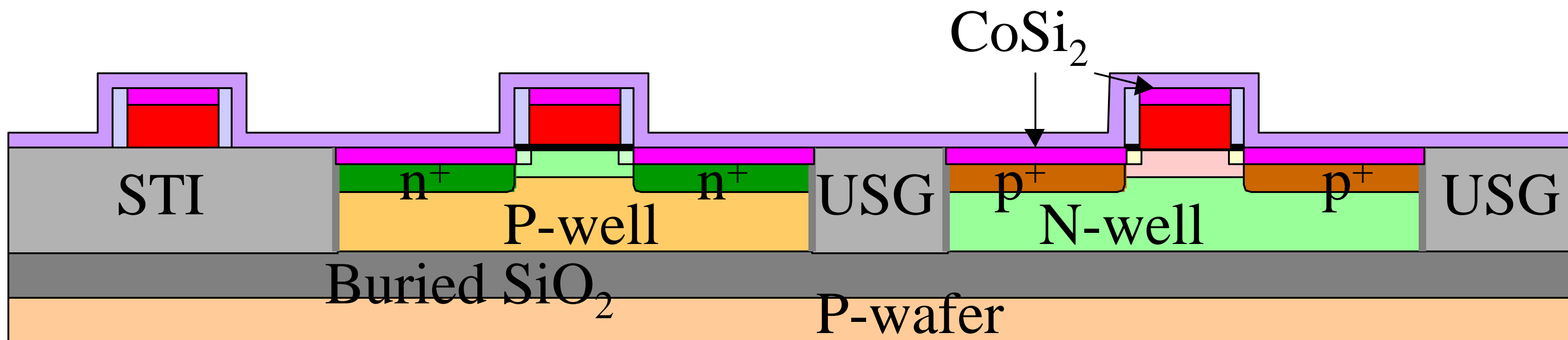
Rapid Thermal Annealing



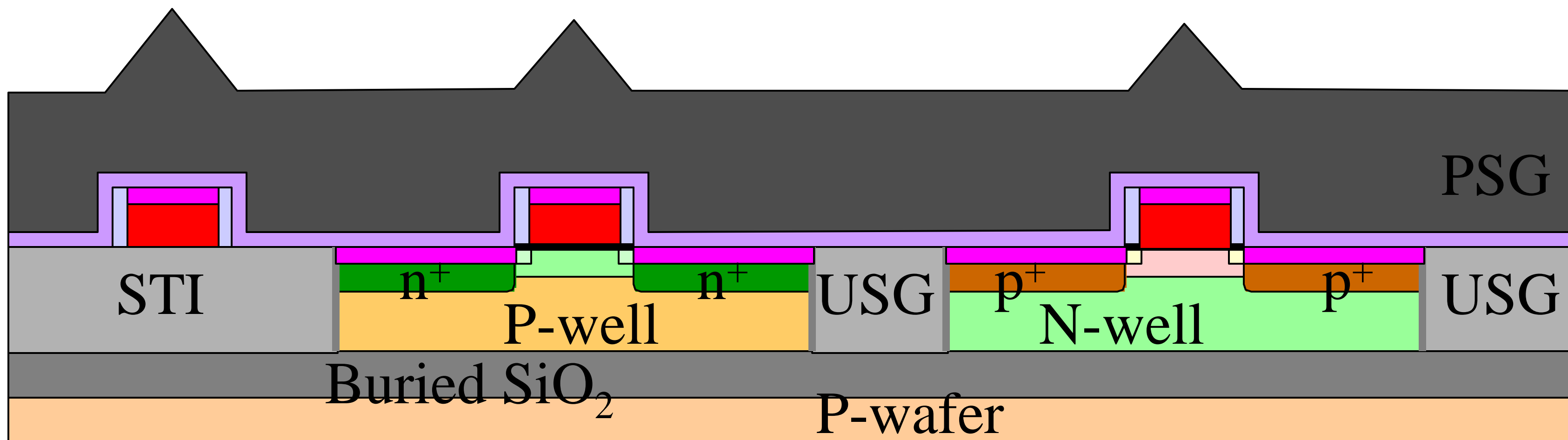
Strip Titanium Nitride and Cobalt



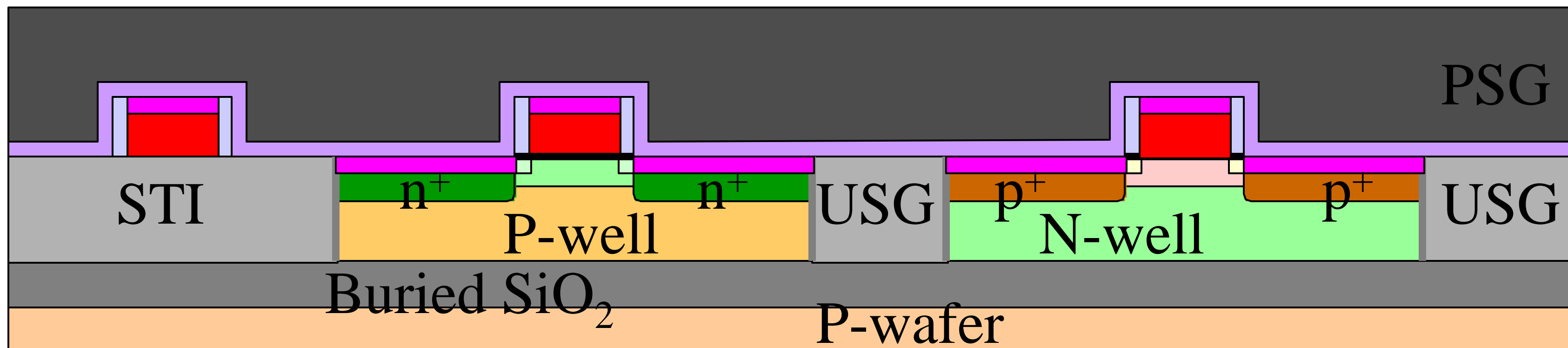
PECVD Nitride



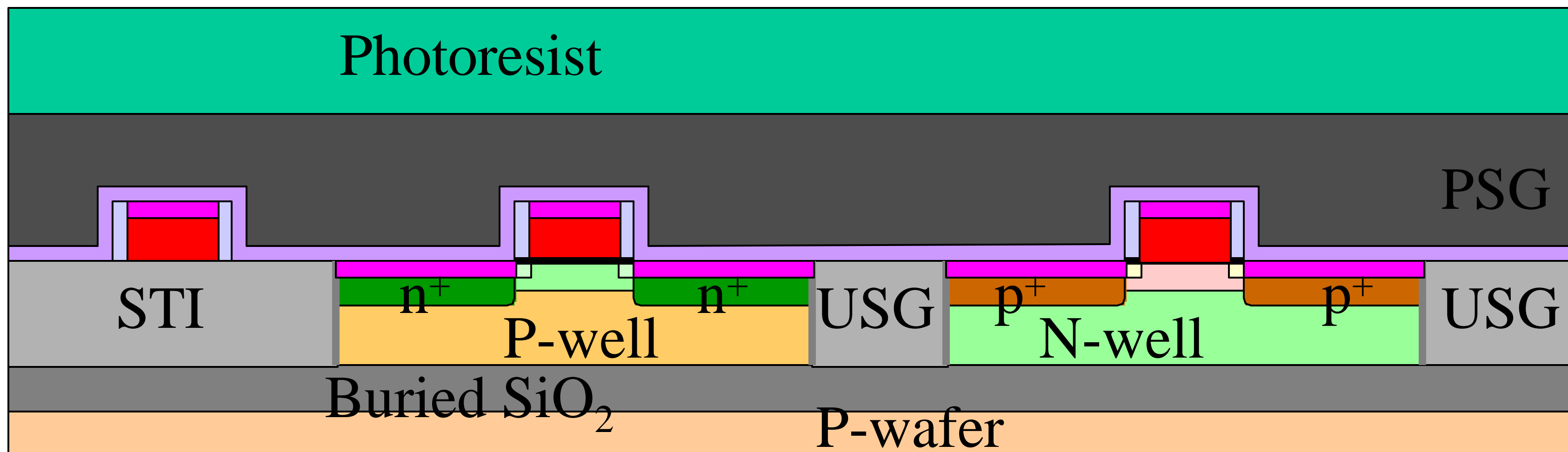
HDP CVD PSG



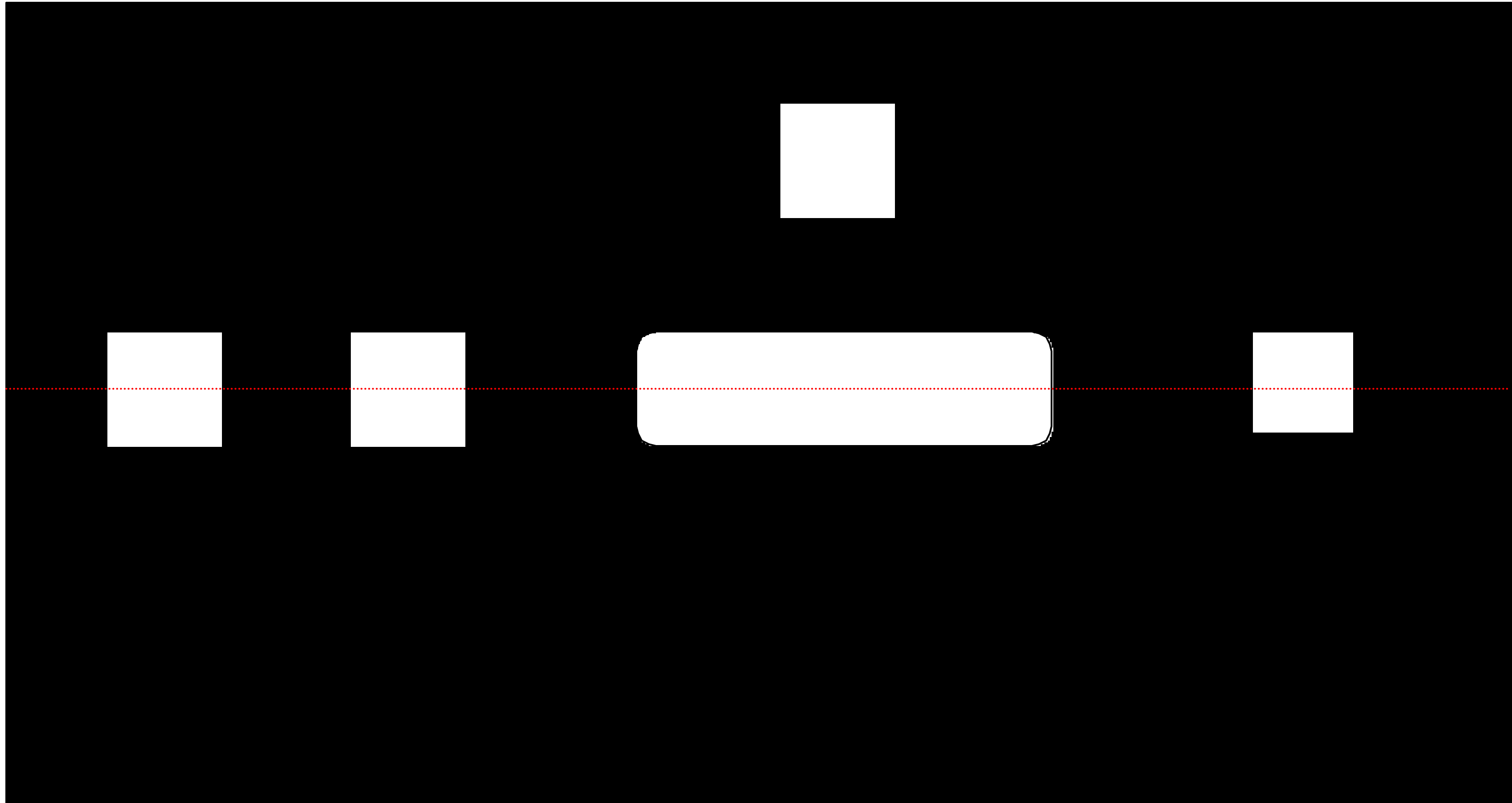
CMP PSG



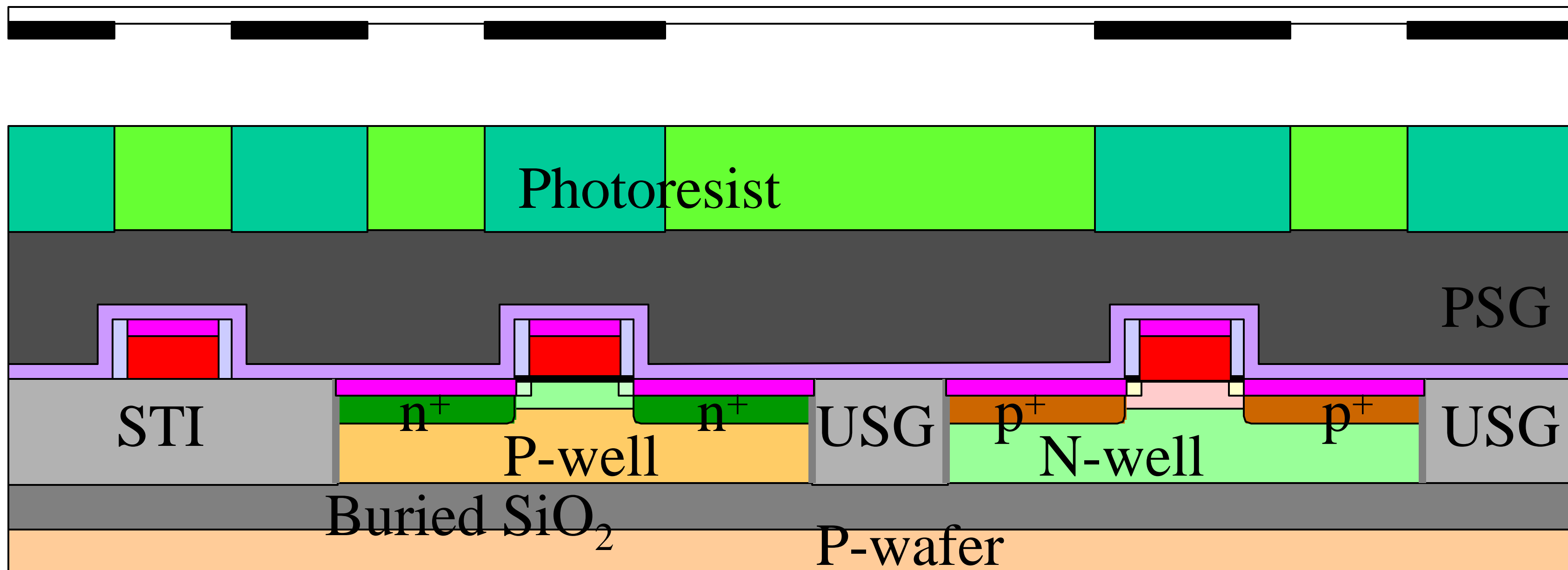
Photoresist Coating and Baking



Mask 9, Contact and Local Interconnection

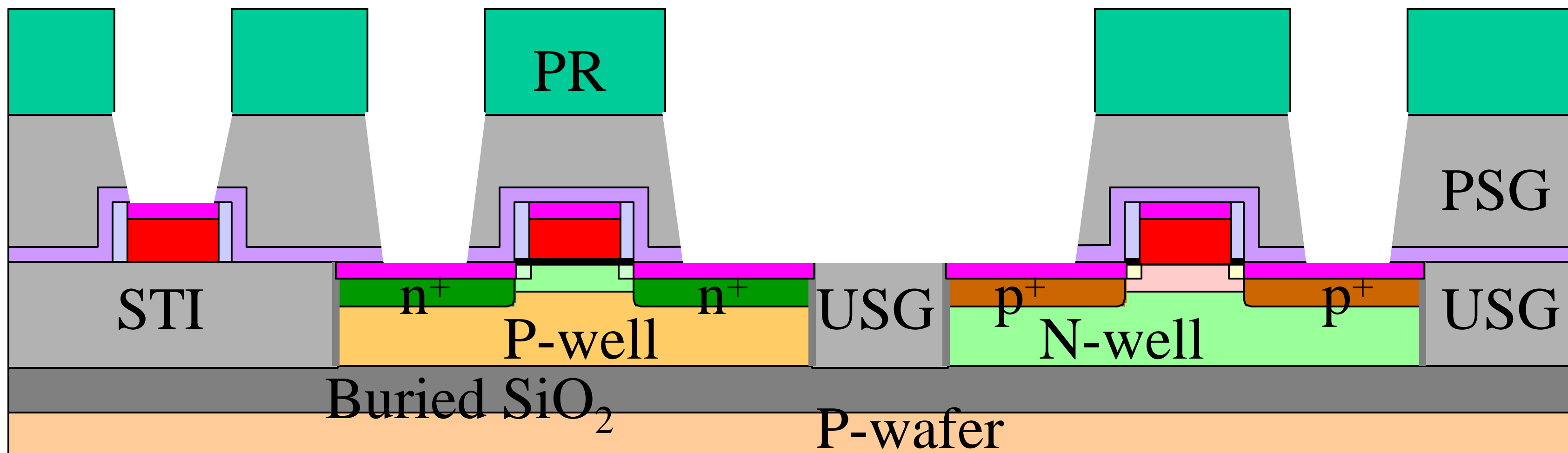


Alignment and Exposure

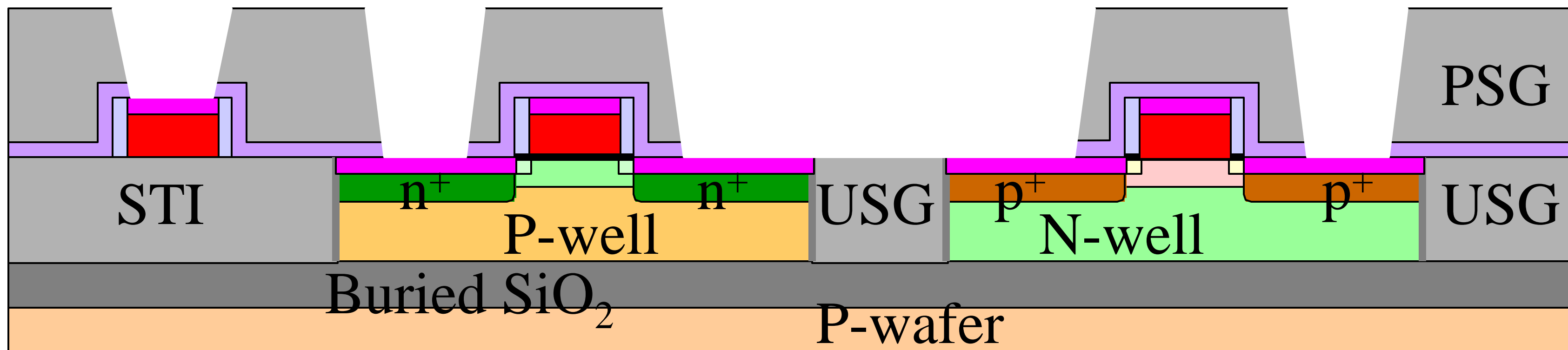


PEB, Development, and Inspection

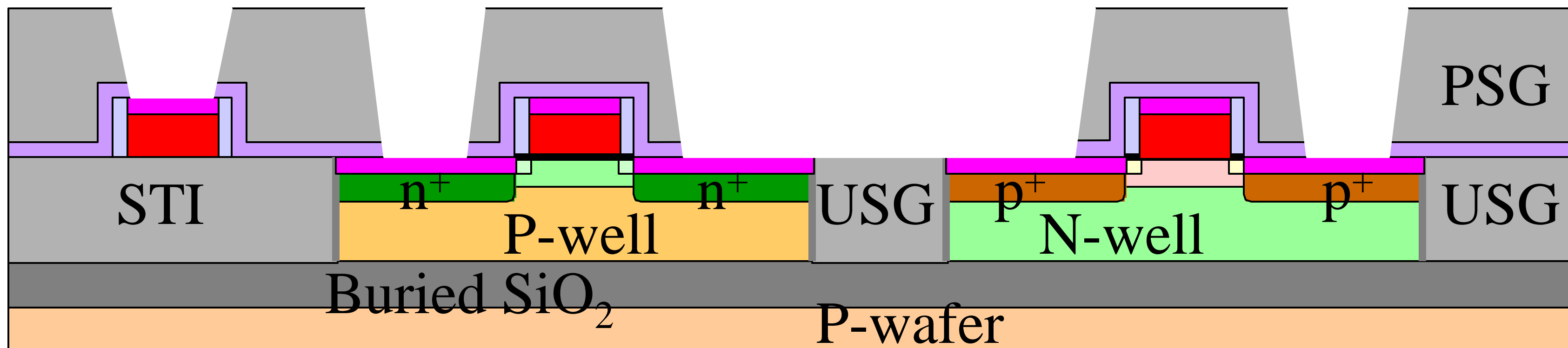
Etch PSG



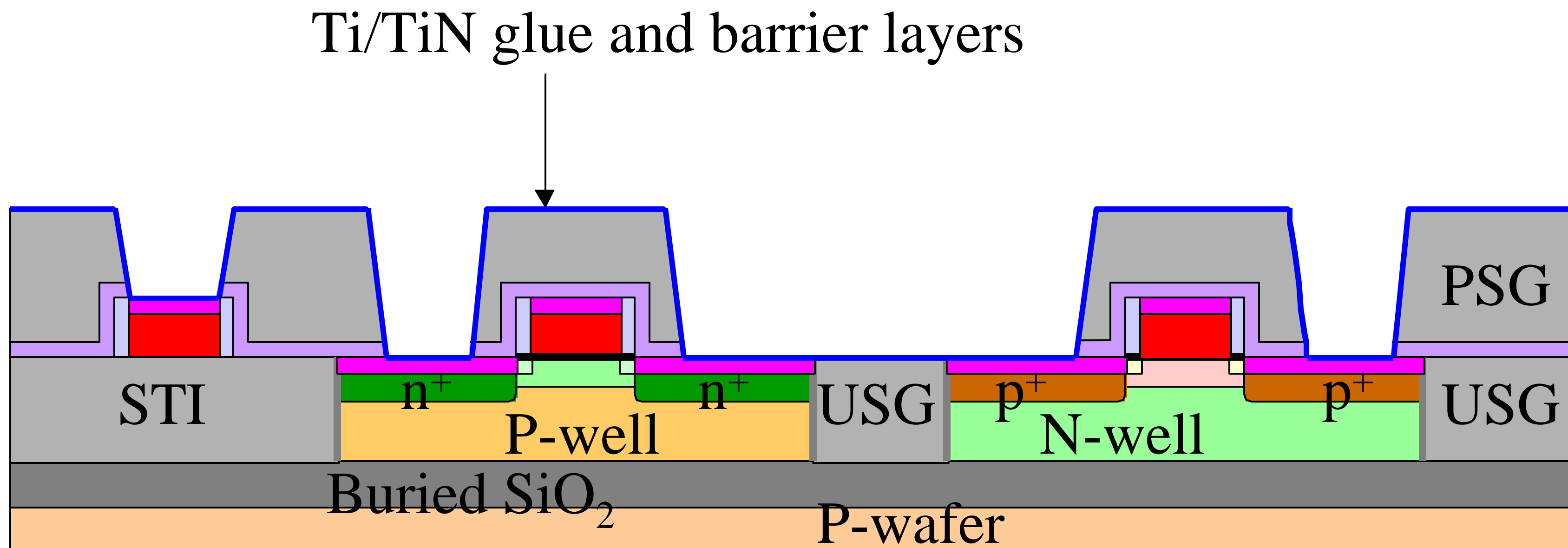
Strip Photoresist



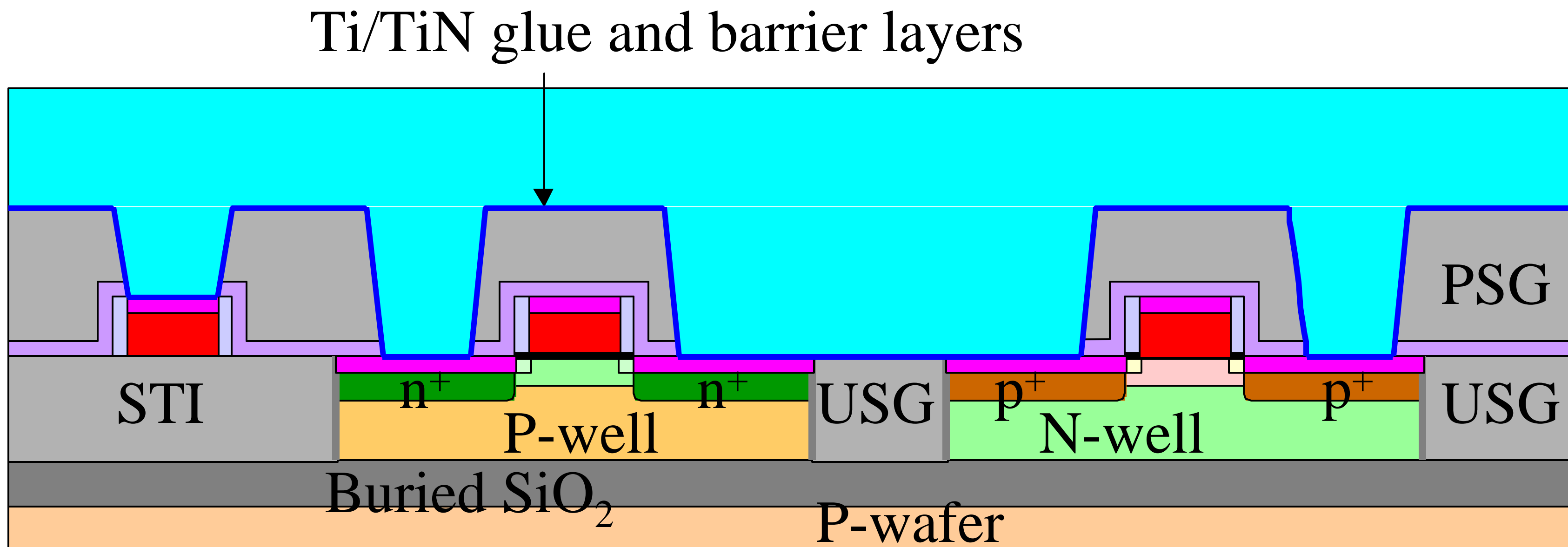
Argon Sputtering Etch



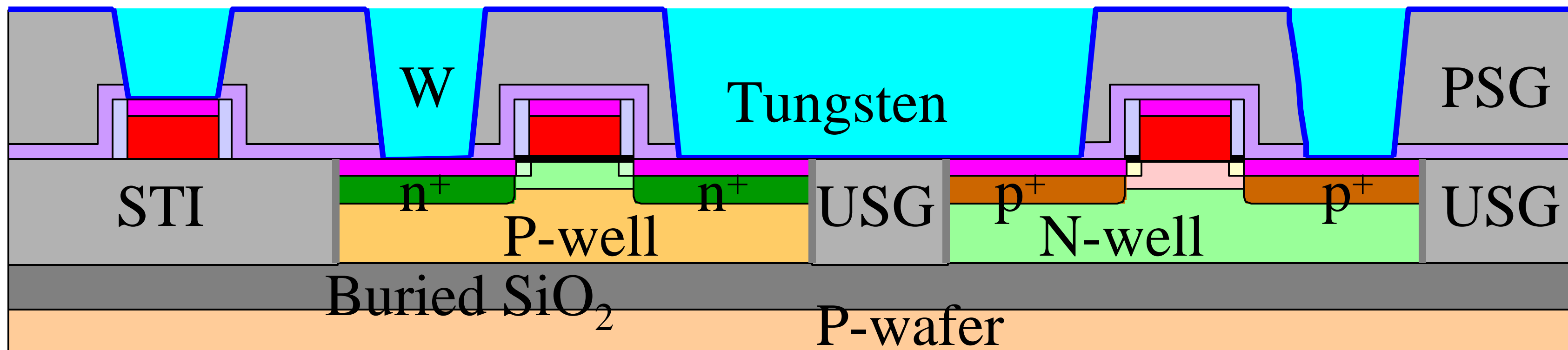
Ti and TiN Sputtering Deposition



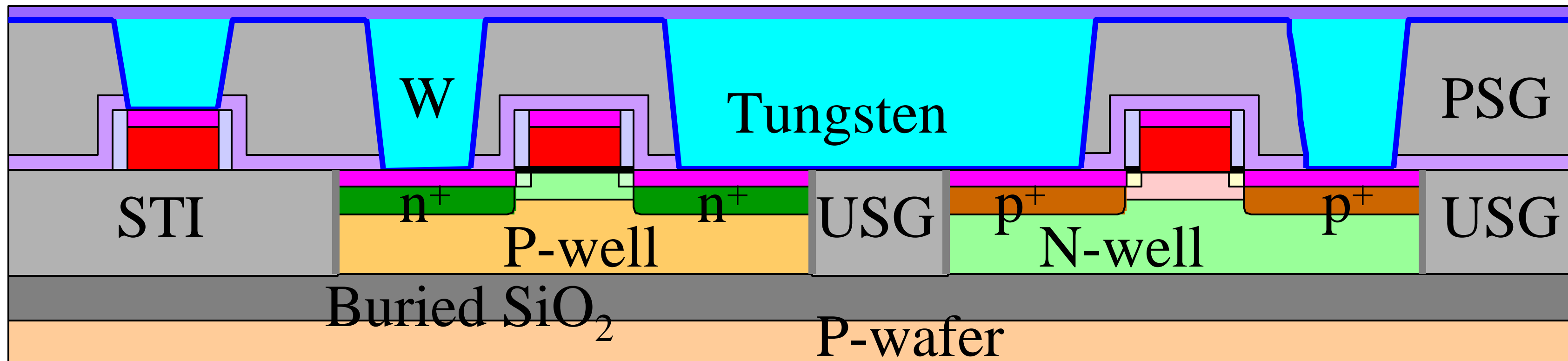
Tungsten CVD



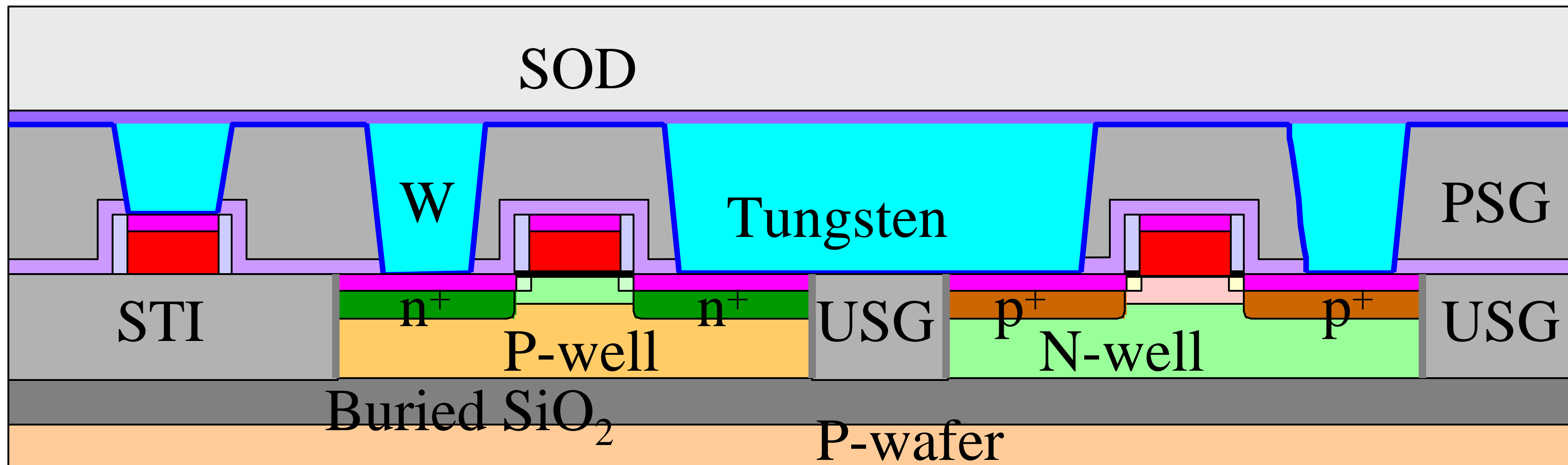
W, TiN, and Ti CMP



PECVD Silicon Carbide Seal Layer



Spin-on Dielectric (SOD) Coating



SOD Cure

SOD

W

Tungsten

PSG

STI

n^+

n^+

USG

p^+

p^+

USG

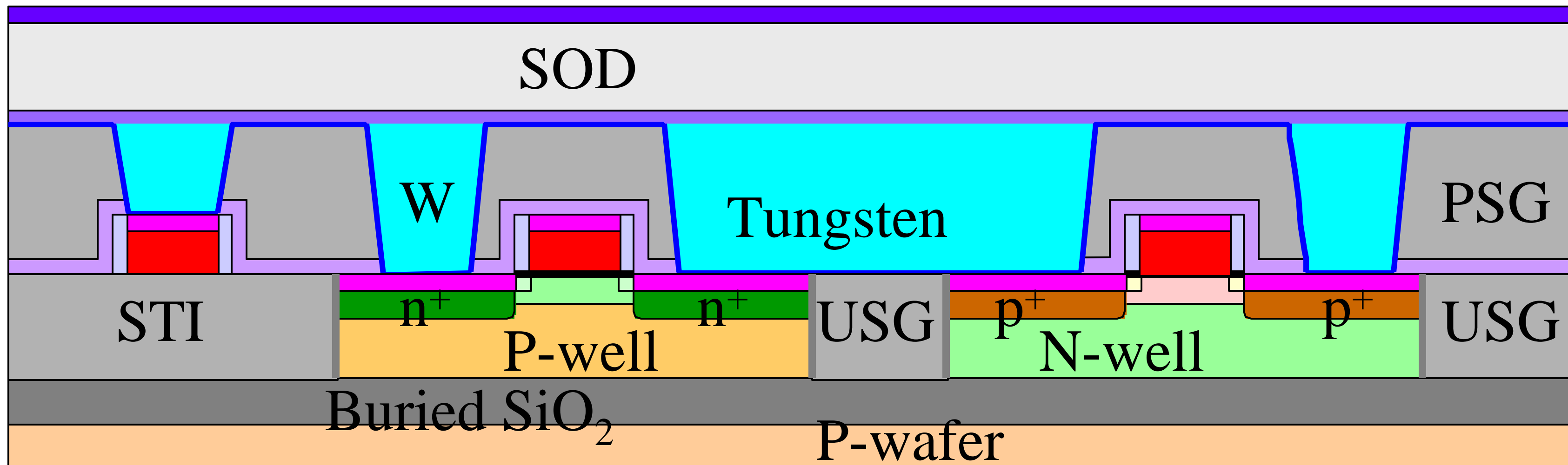
P-well

N-well

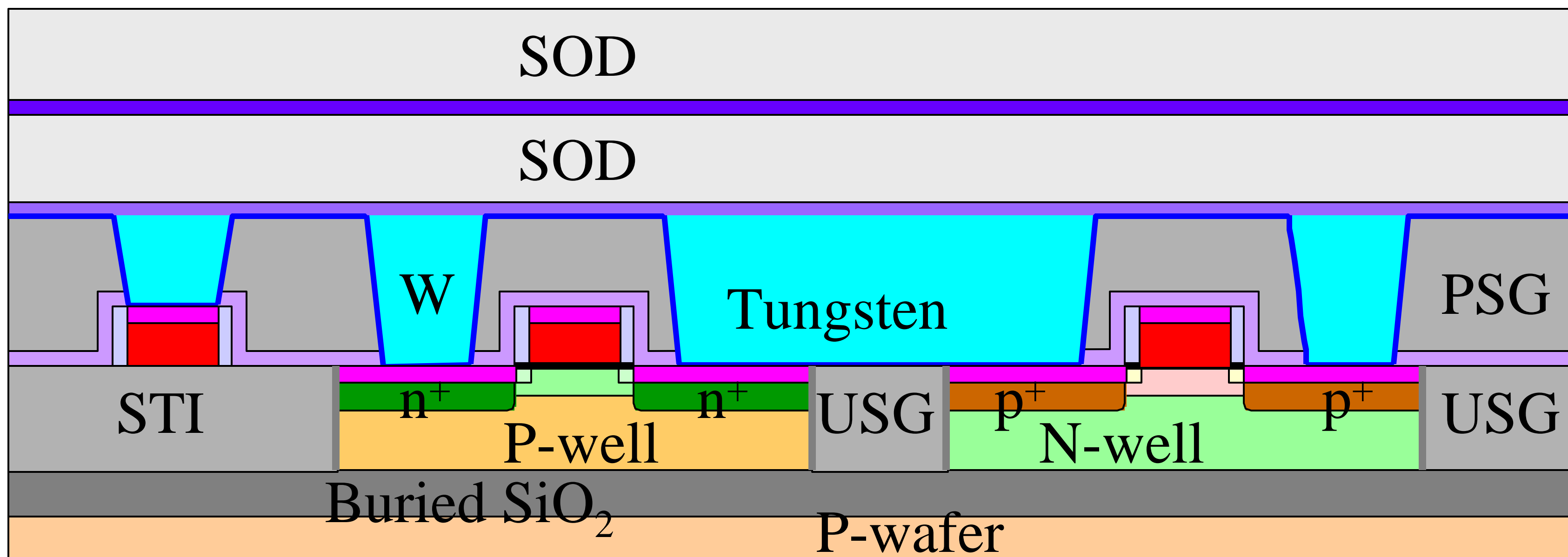
Buried SiO_2

P-wafer

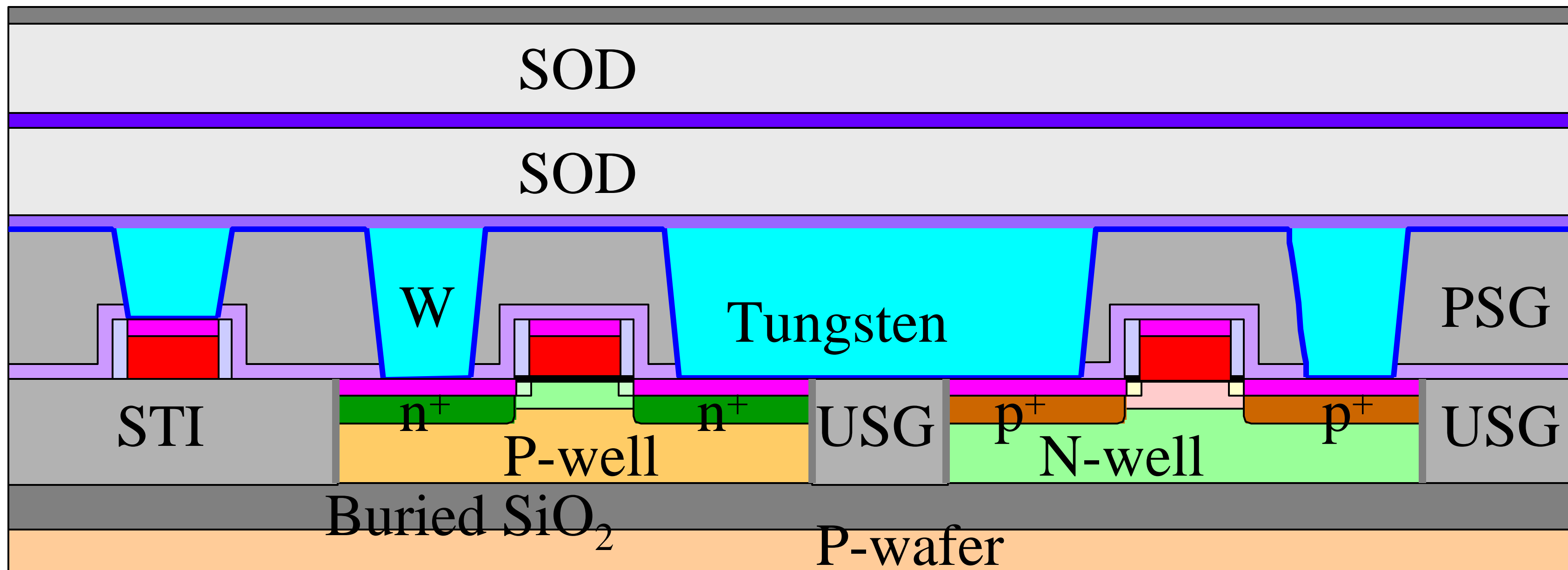
PECVD SiC Etch Stop Layer



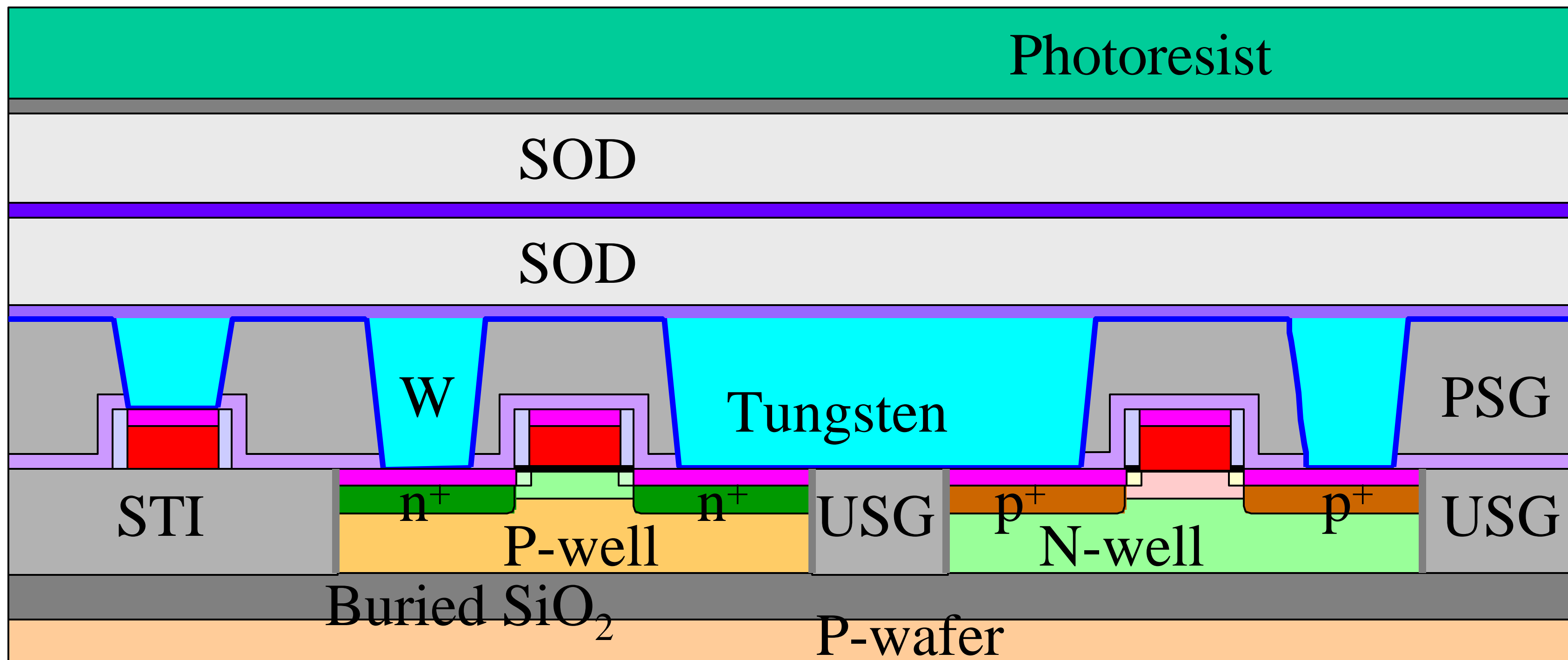
SOD Coating and Curing



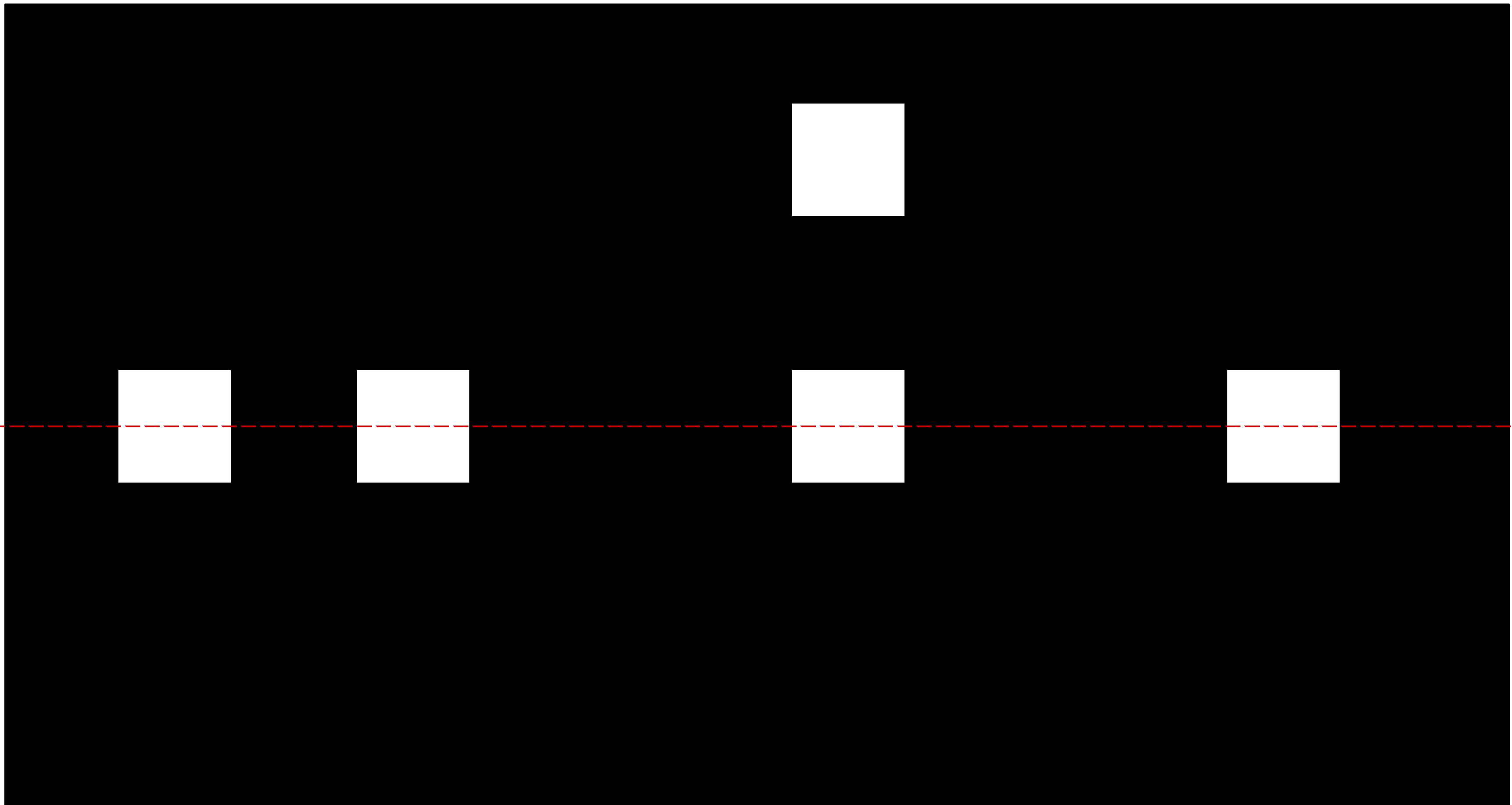
PE-TEOS Cap



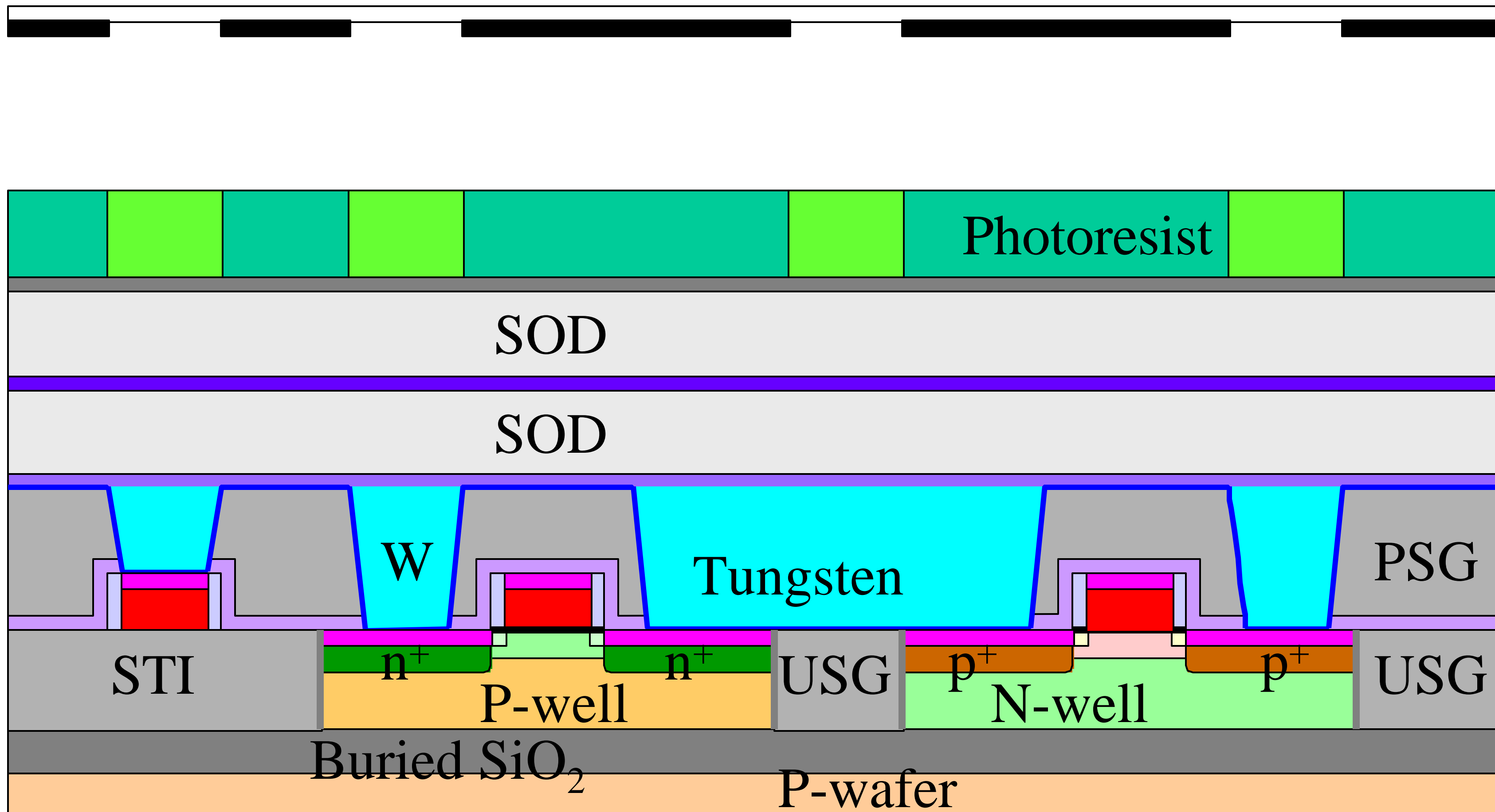
Photoresist Coating and Baking



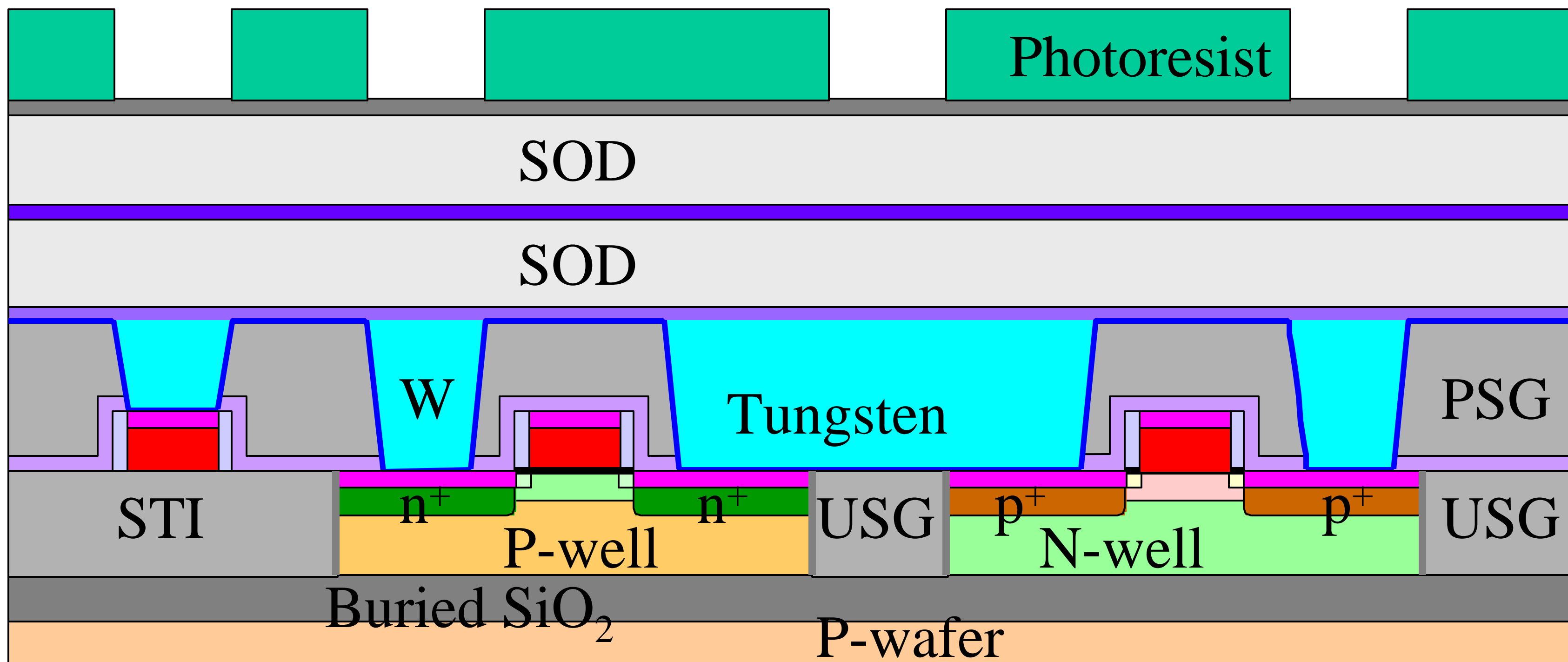
Mask 10, Via 1



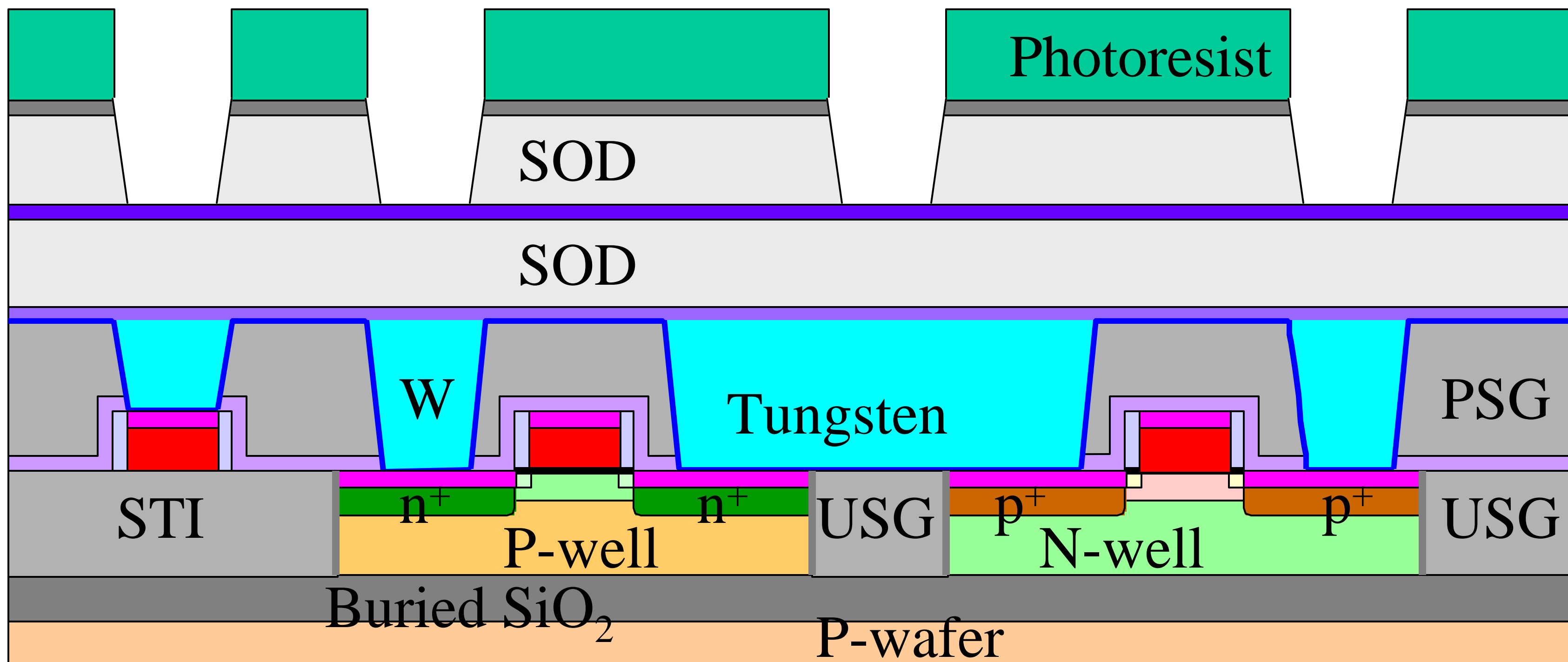
Alignment and Exposure



PEB, Development, and Inspection



Etch PE-TEOS&SOD, Stop on SiC



Strip Photoresist

SOD

SOD

W

Tungsten

PSG

STI

n^+

n^+

P-well

USG

p^+

N-well

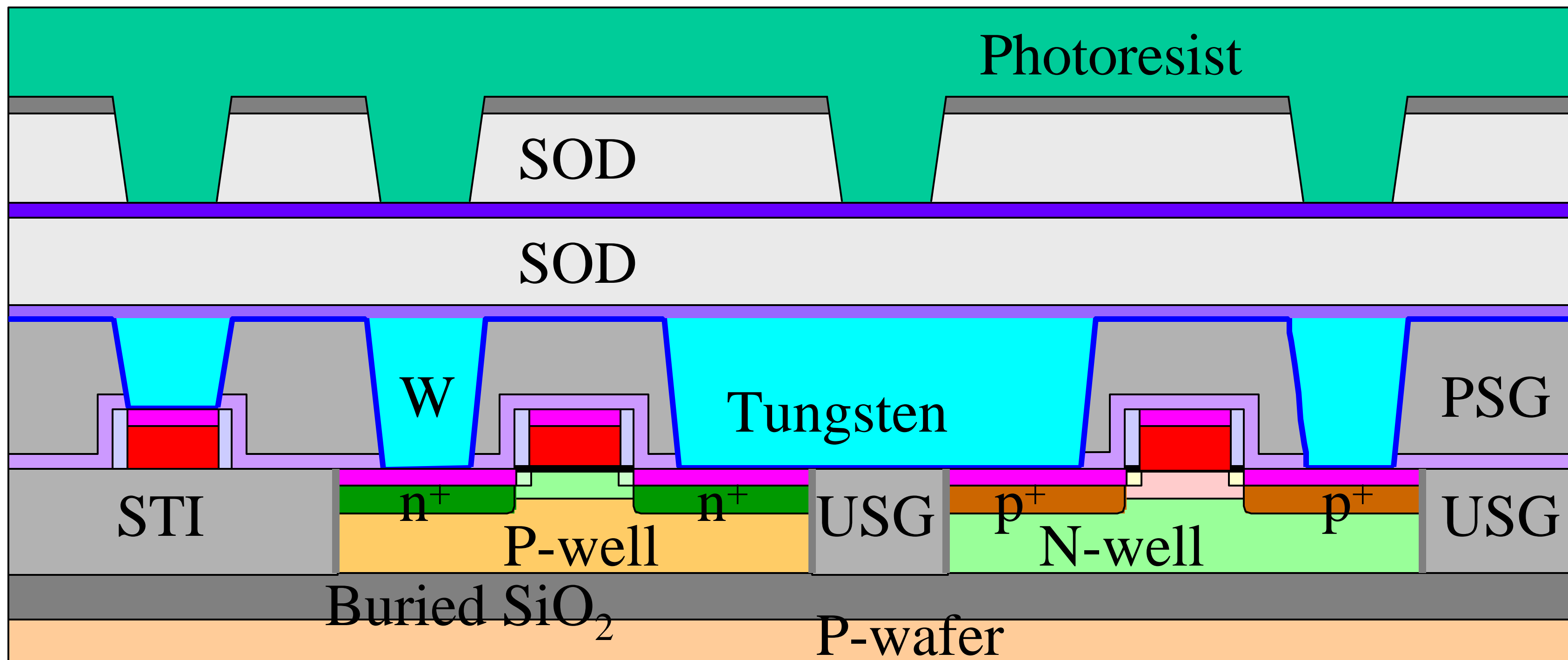
p^+

USG

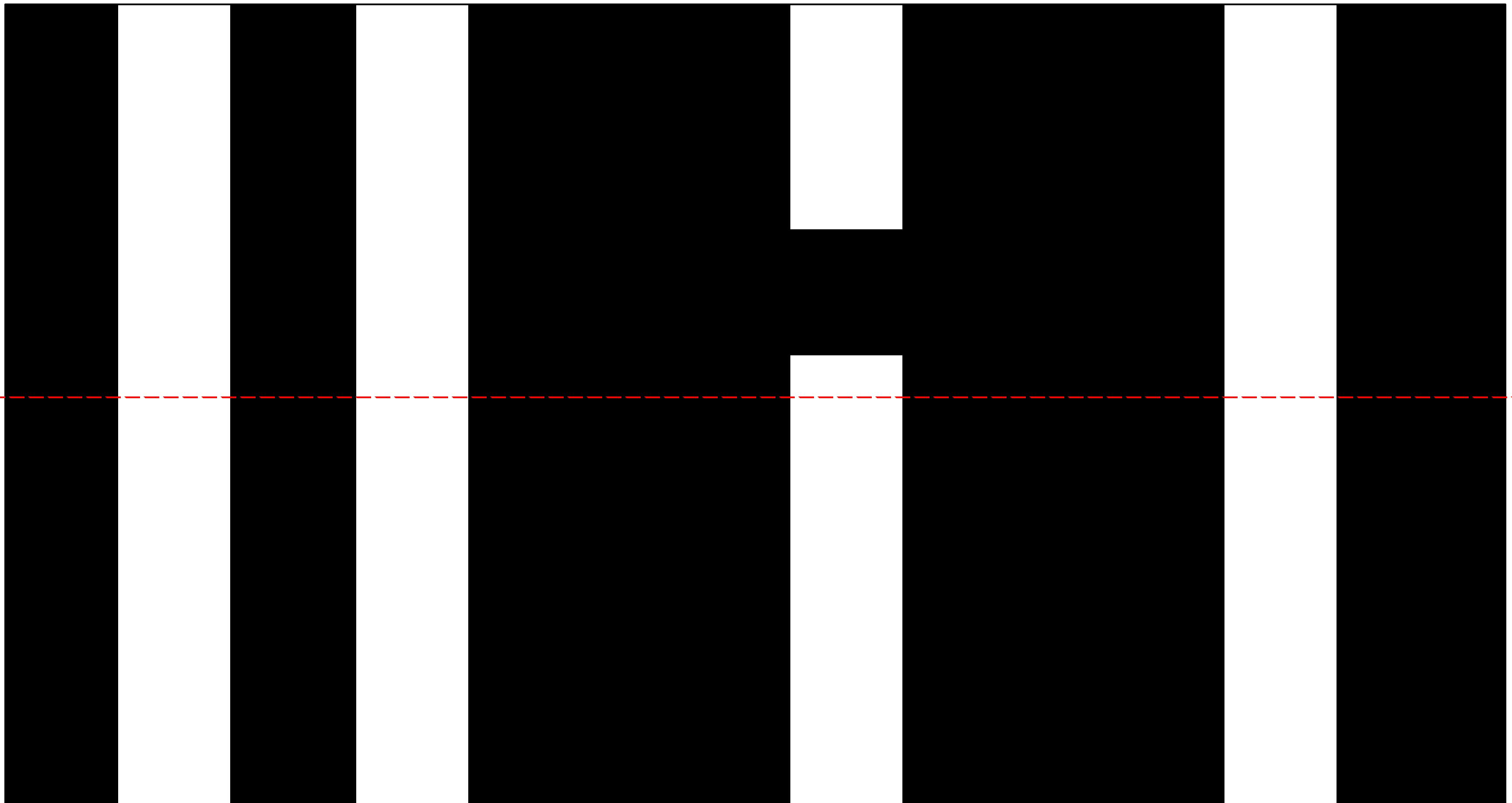
Buried SiO_2

P-wafer

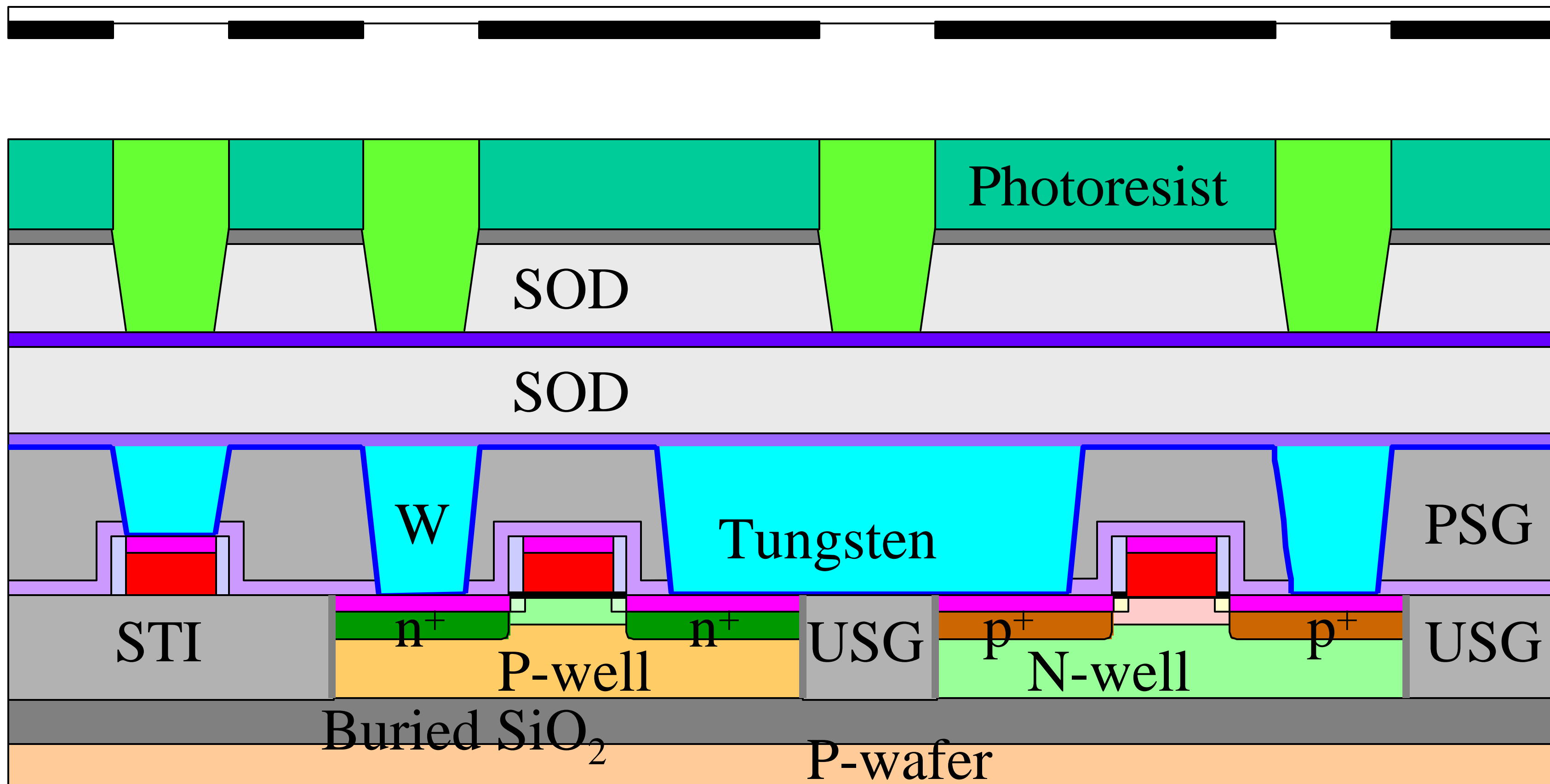
Photoresist Coating and Baking



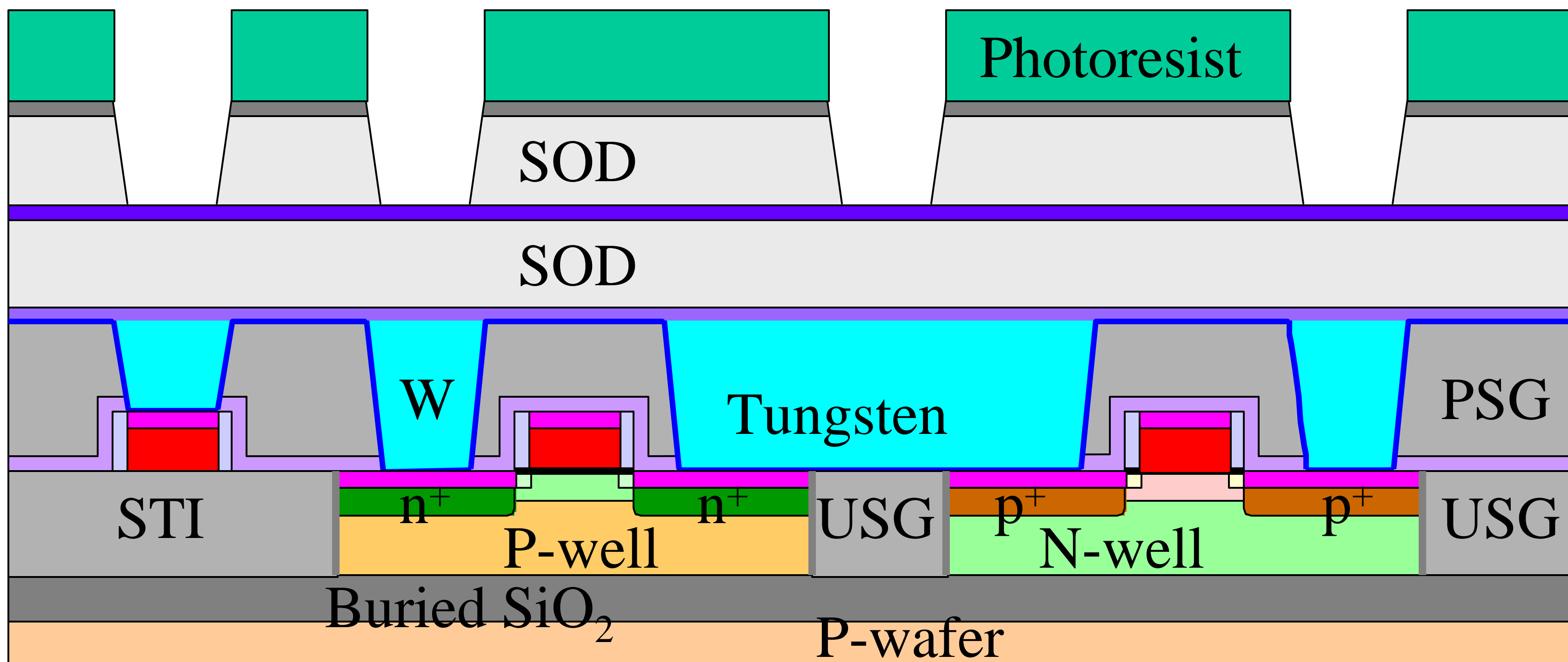
Mask 11, Metal Trench 1



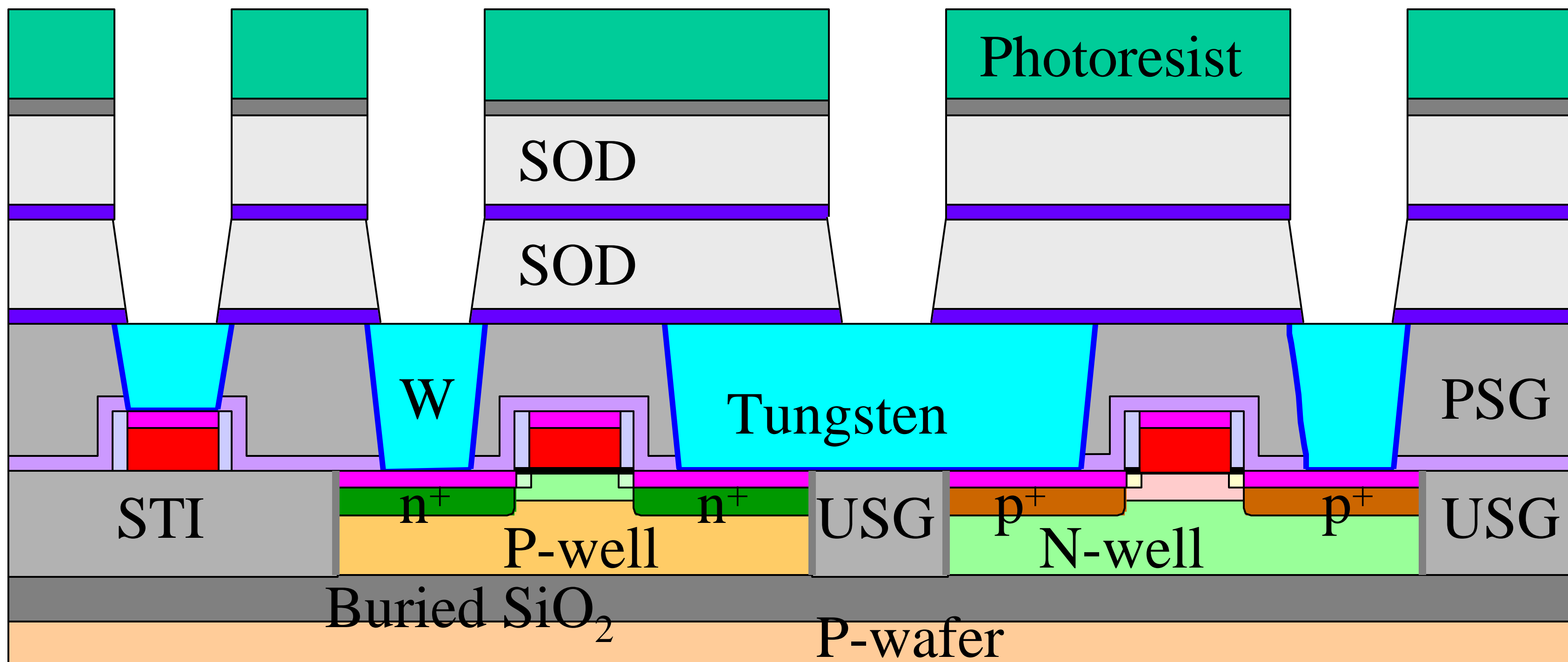
Alignment and Exposure



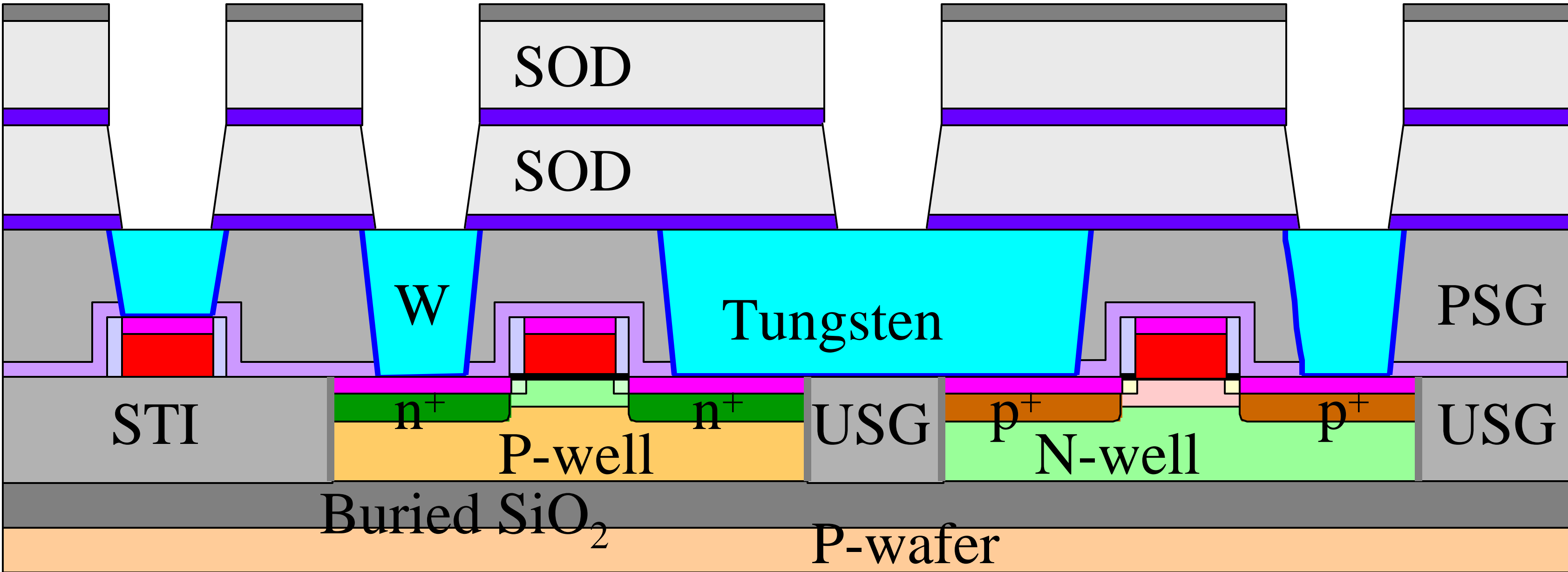
PEB, Development, and Inspection



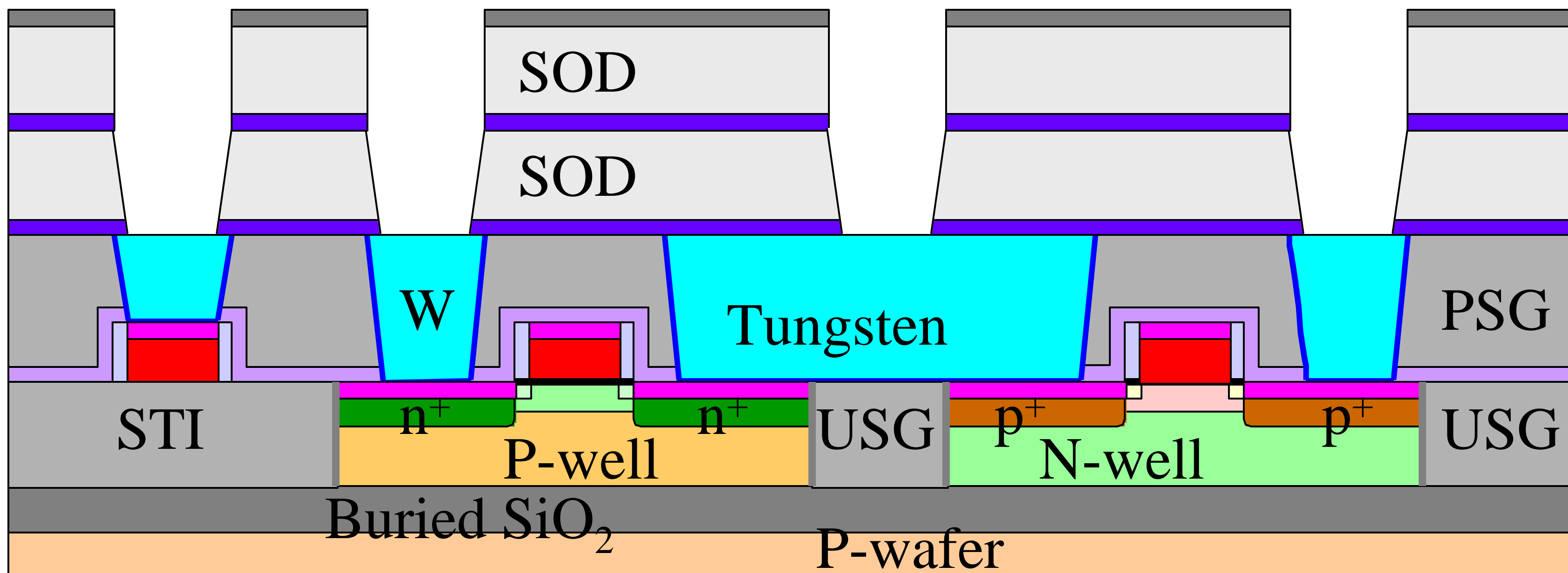
Etch Trench



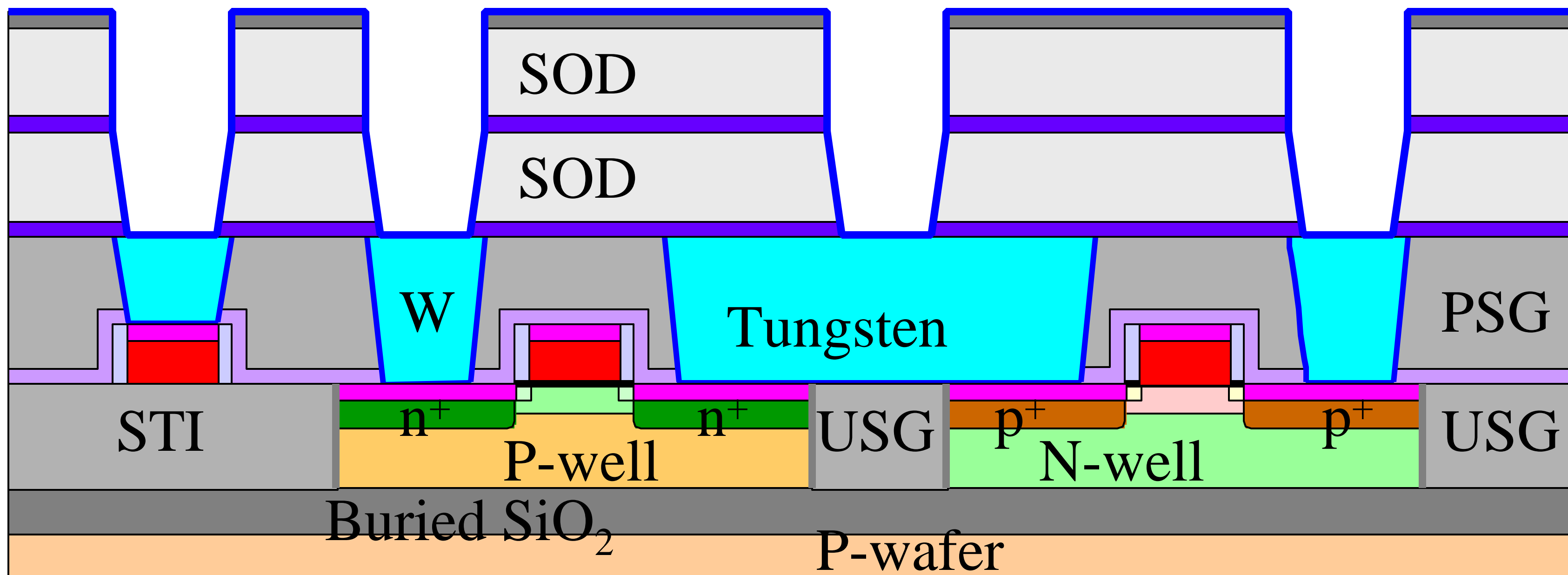
Strip Photoresist



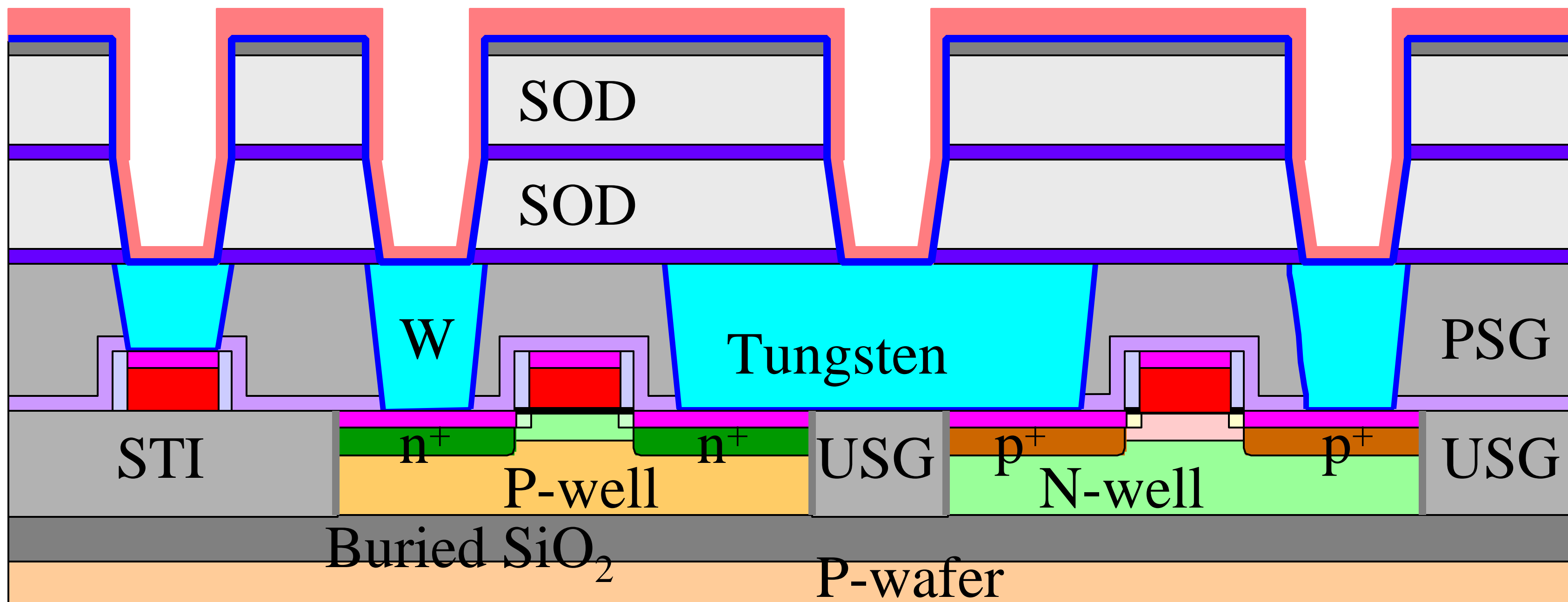
Argon Sputtering Clean



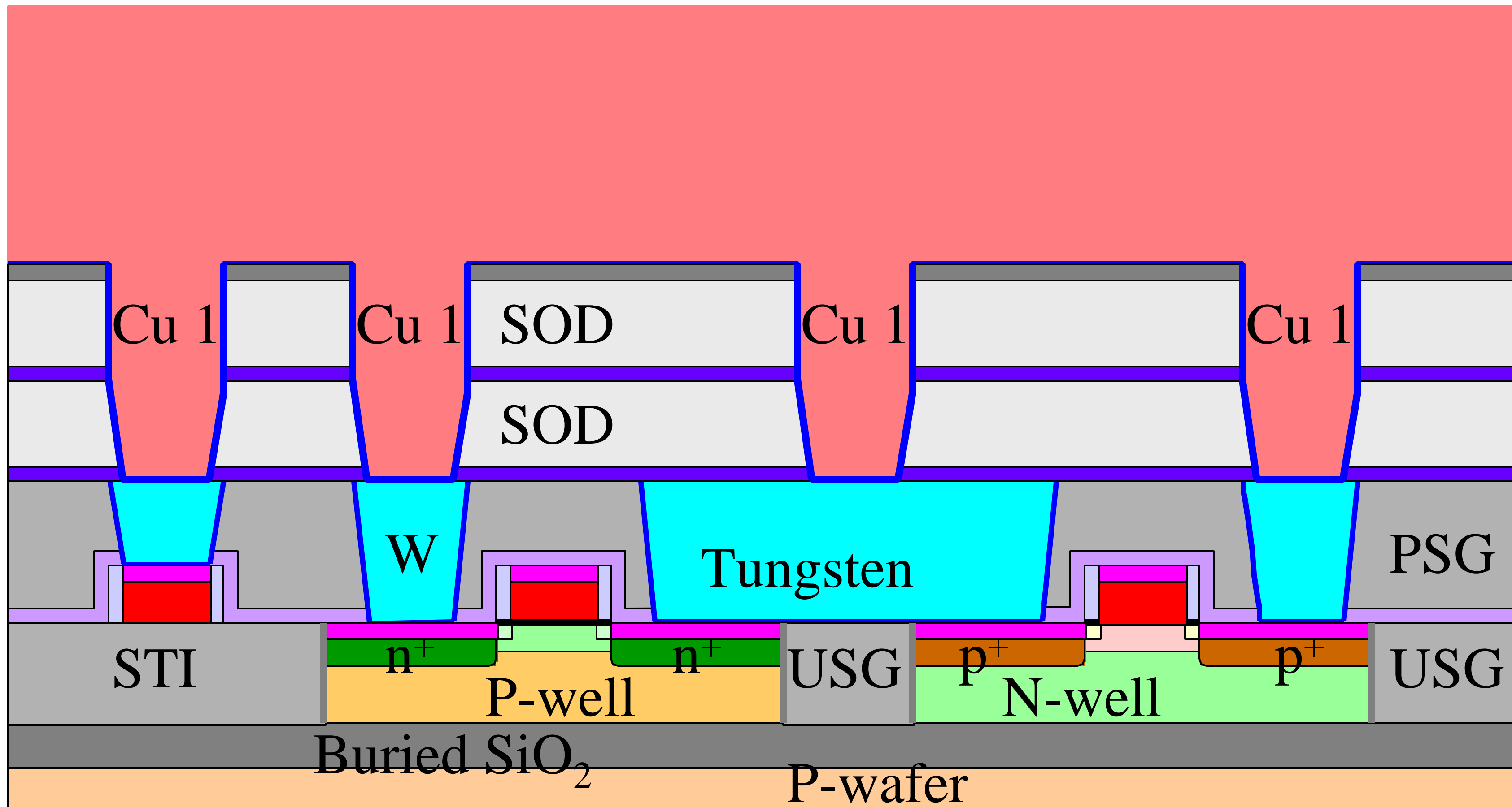
Ta and TaN Barrier Layer PVD



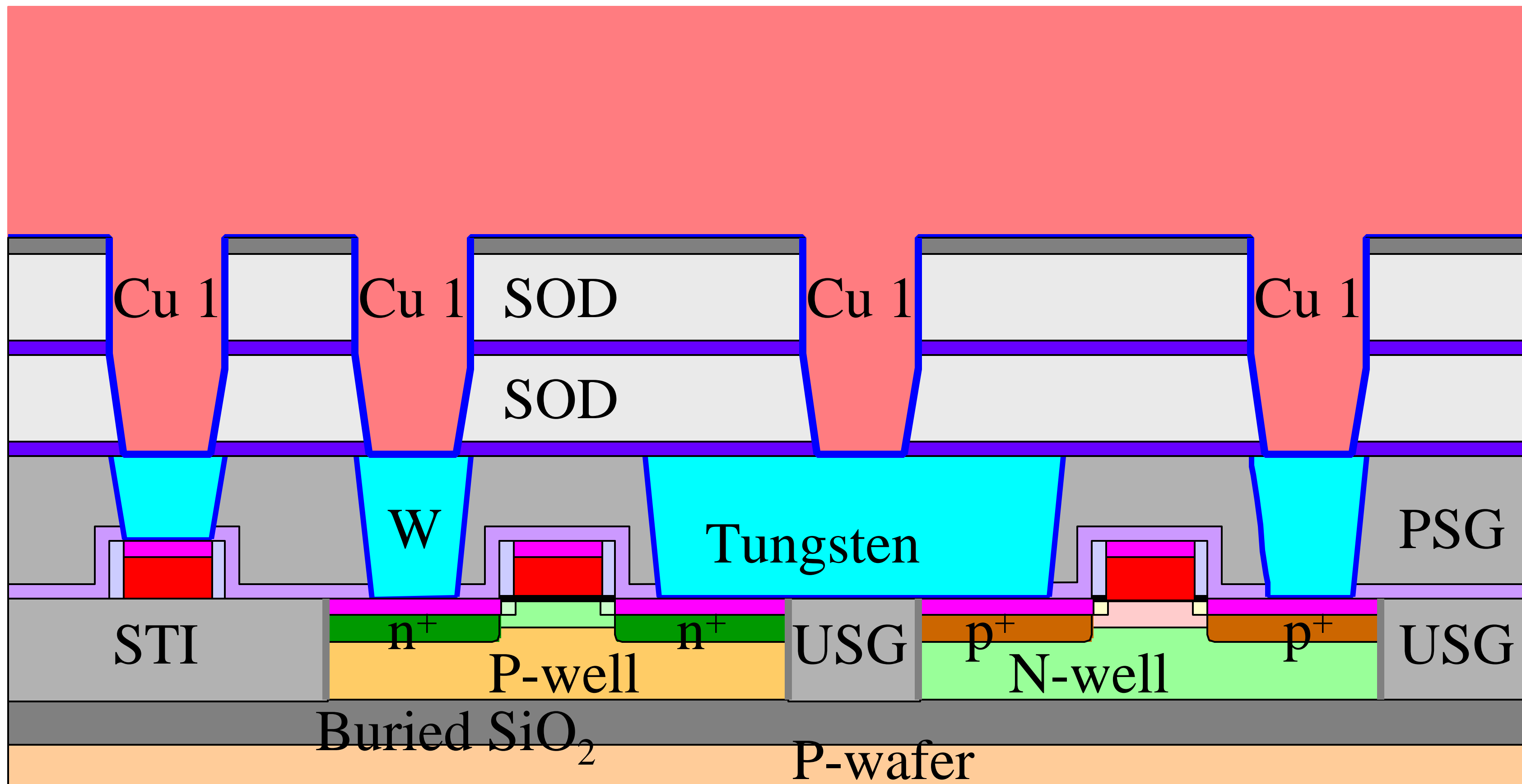
Cu Seed Layer PVD



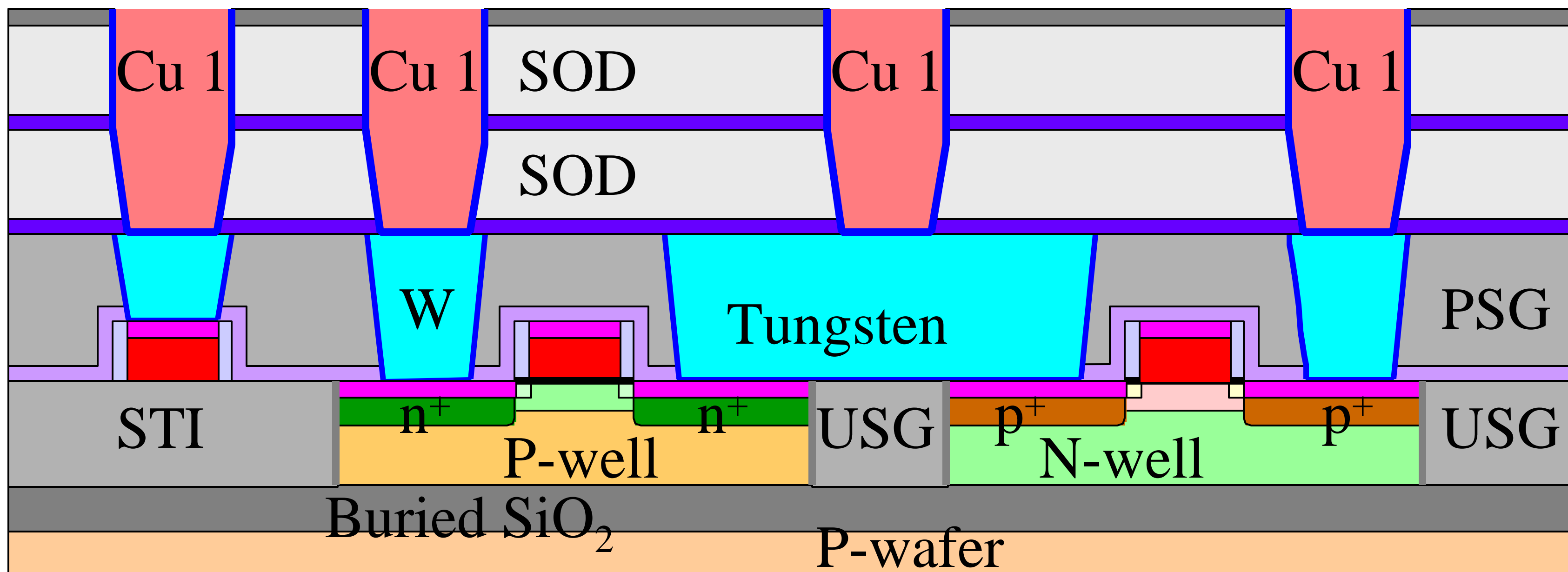
Bulk Copper Electrochemical Plating



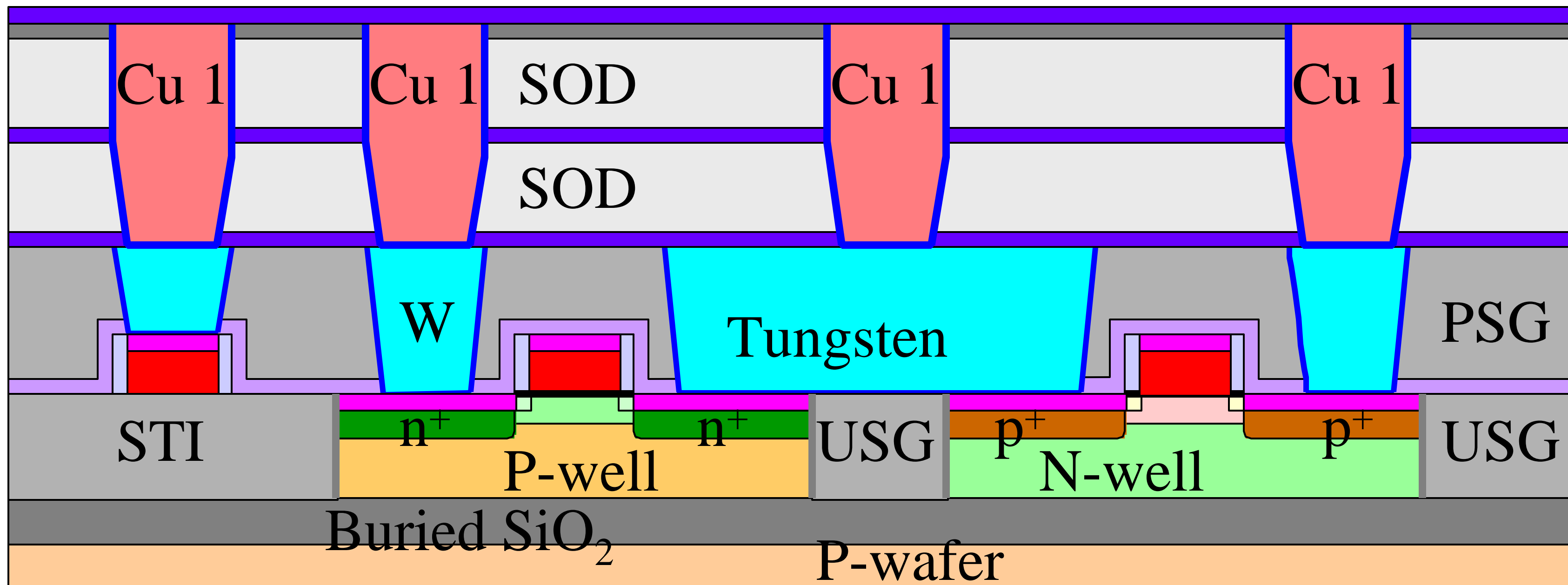
Copper Anneal



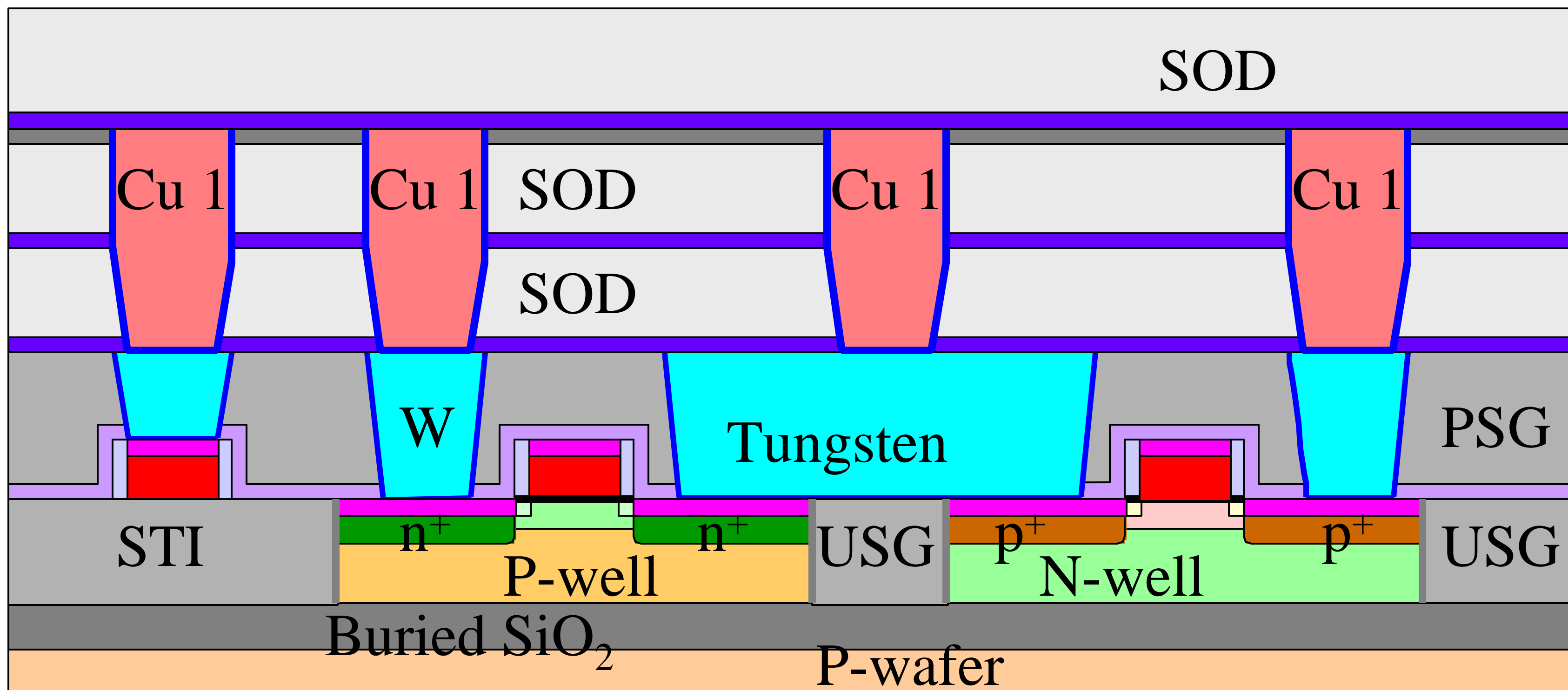
Cu, Ta, and TaN CMP



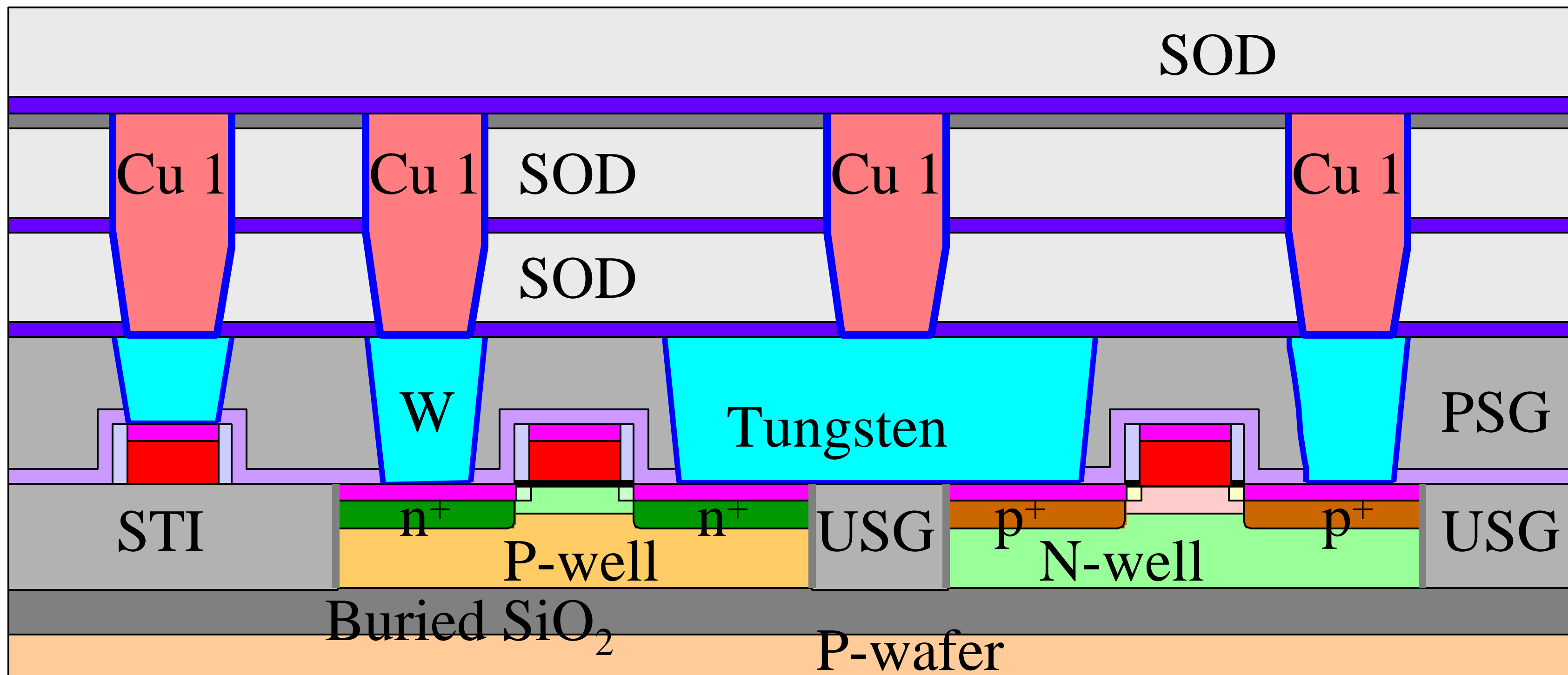
PECVD SiC Seal Layer



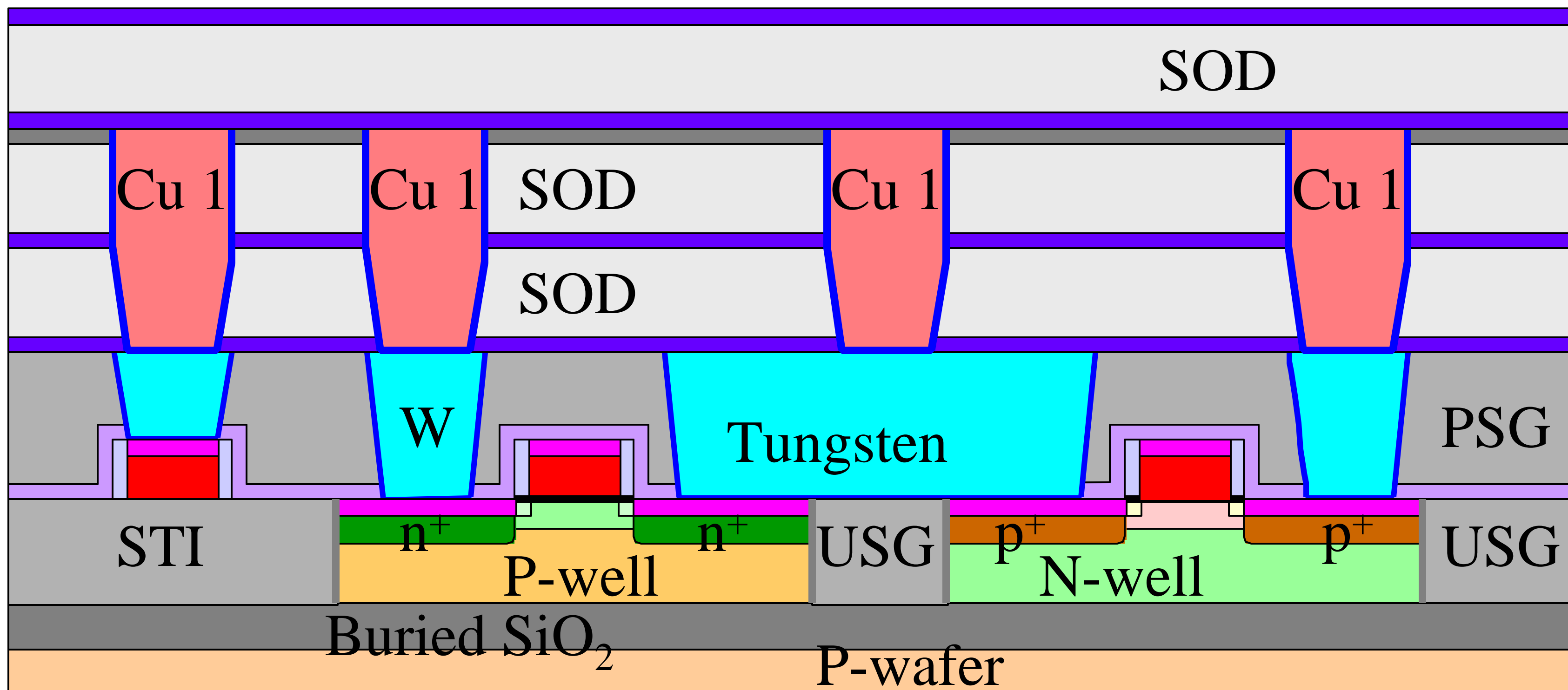
Spin-on Dielectric (SOD) Coating



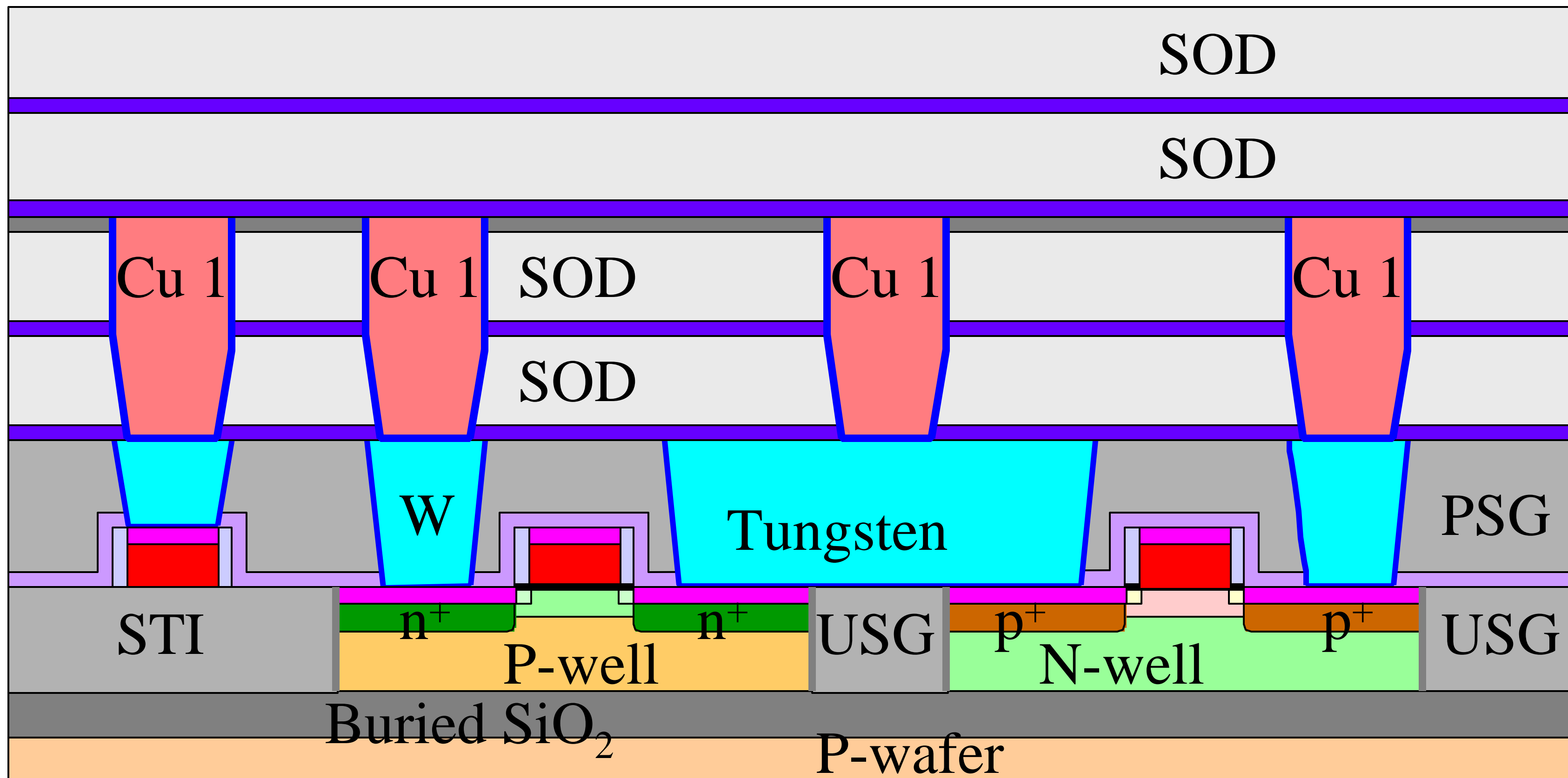
SOD Curing



PECVD SiC Etch Stop Layer



SOD Coating and Curing



PE-TEOS Cap

SOD
SOD
Cu 1 Cu 1 SOD Cu 1 Cu 1
SOD
W Tungsten PSG
STI n^+ n^+ USG p^+ p^+ USG
P-well N-well
Buried SiO_2
P-wafer

Photoresist Coating and Baking

SOD

SOD

Cu 1 Cu 1 SOD Cu 1 Cu 1

SOD

W Tungsten PSG

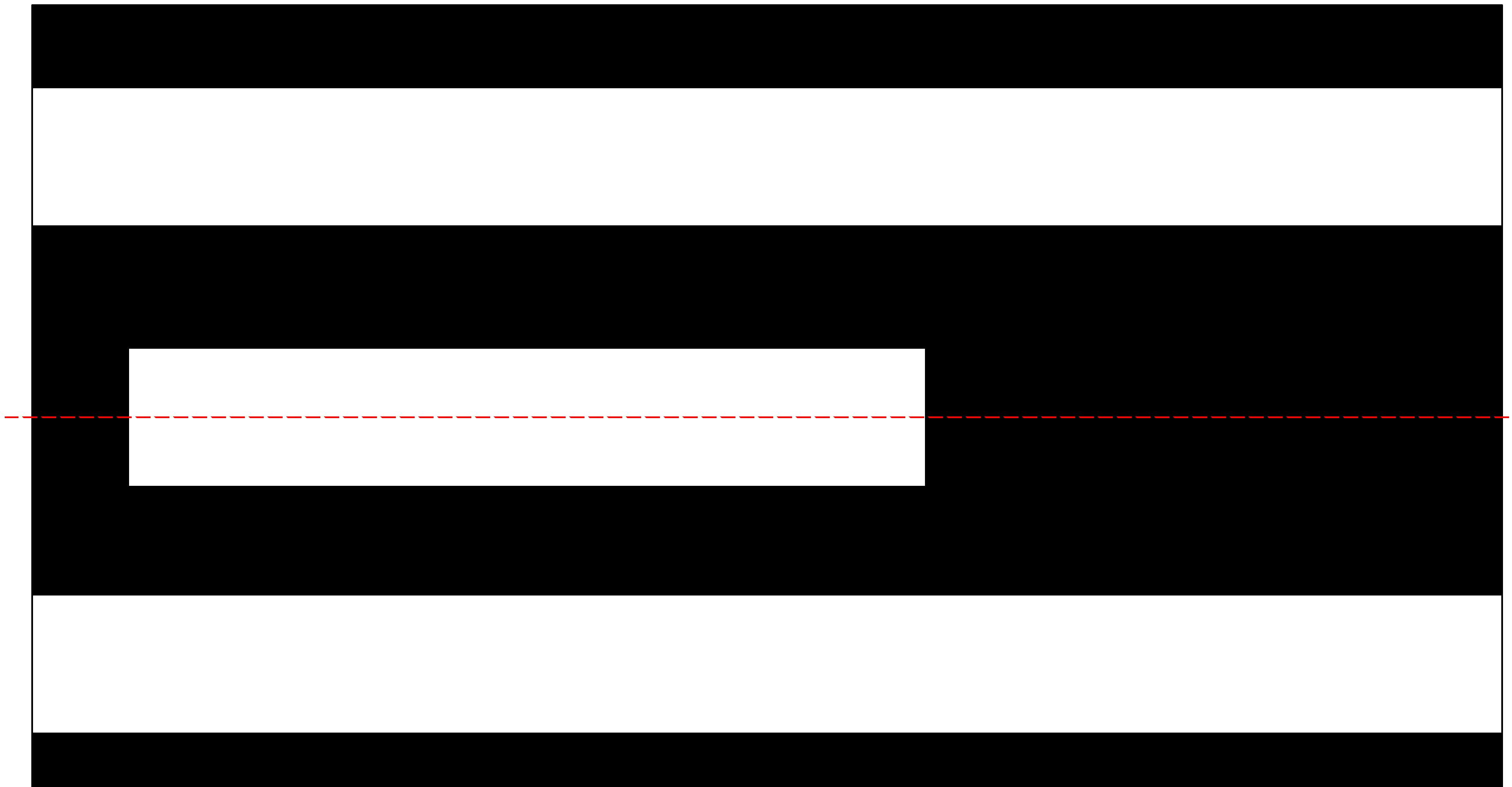
STI n^+ n^+ USG p^+ p^+ USG

P-well N-well

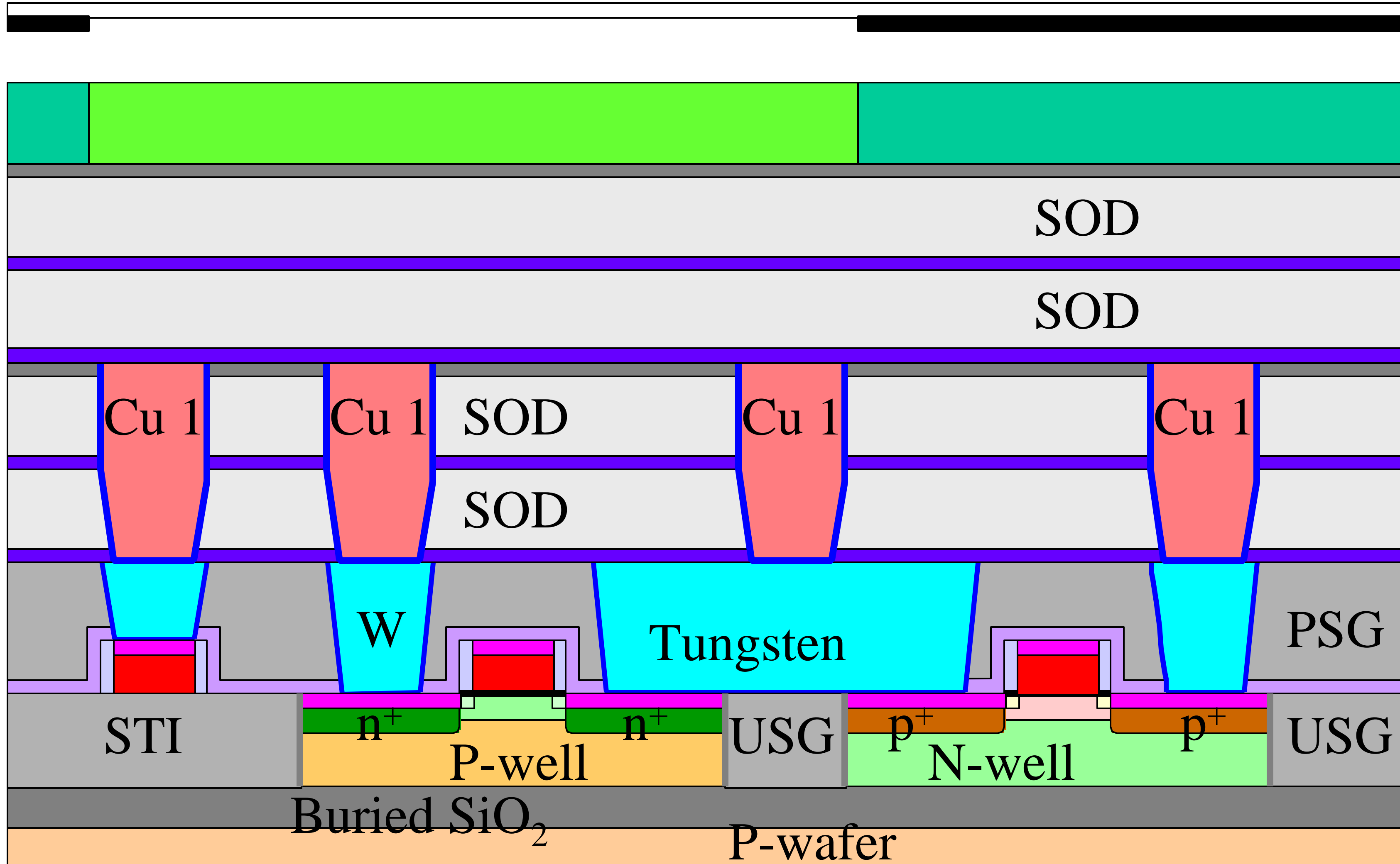
Buried SiO_2

P-wafer

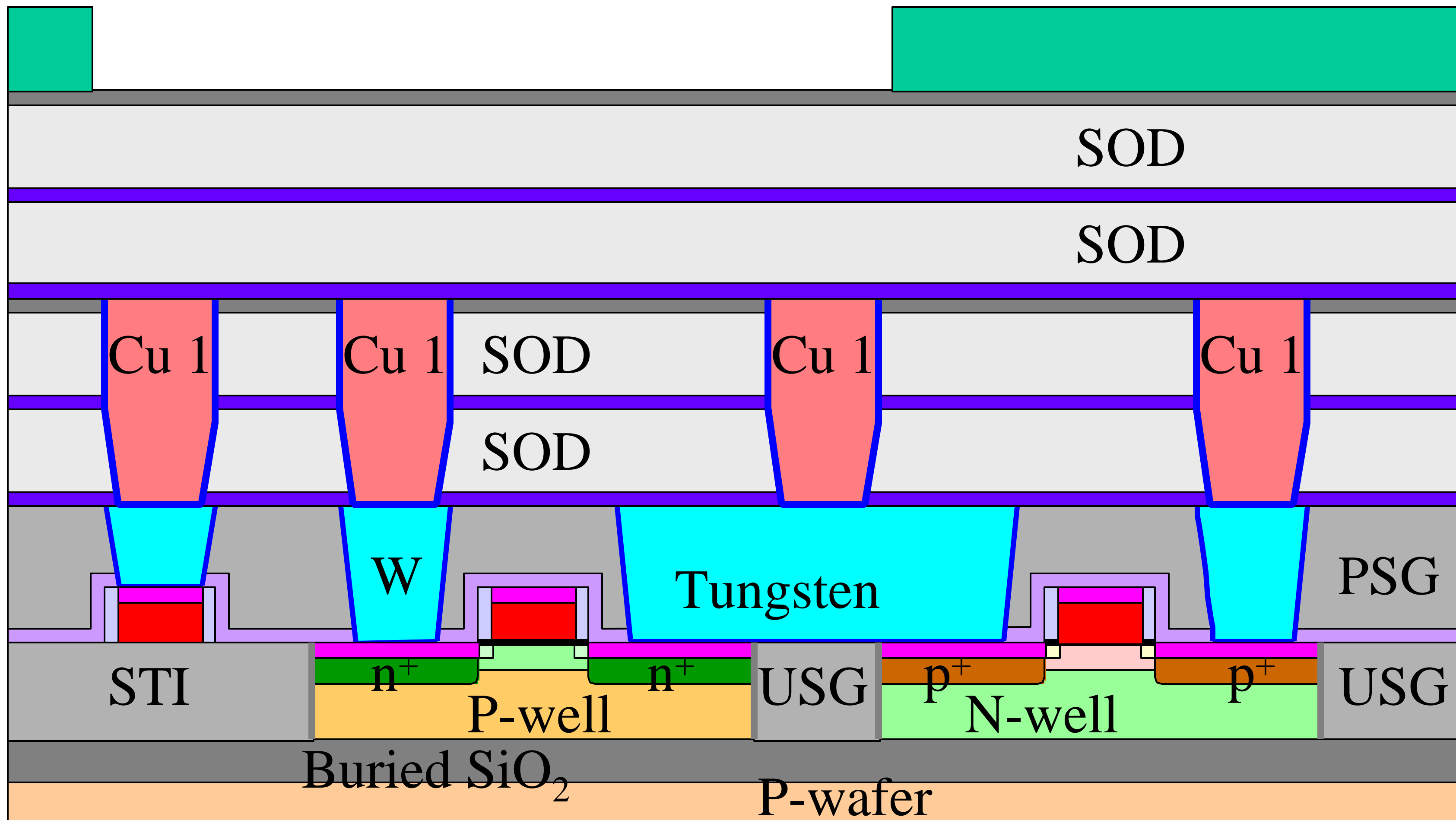
Mask 12, Metal Trench 2



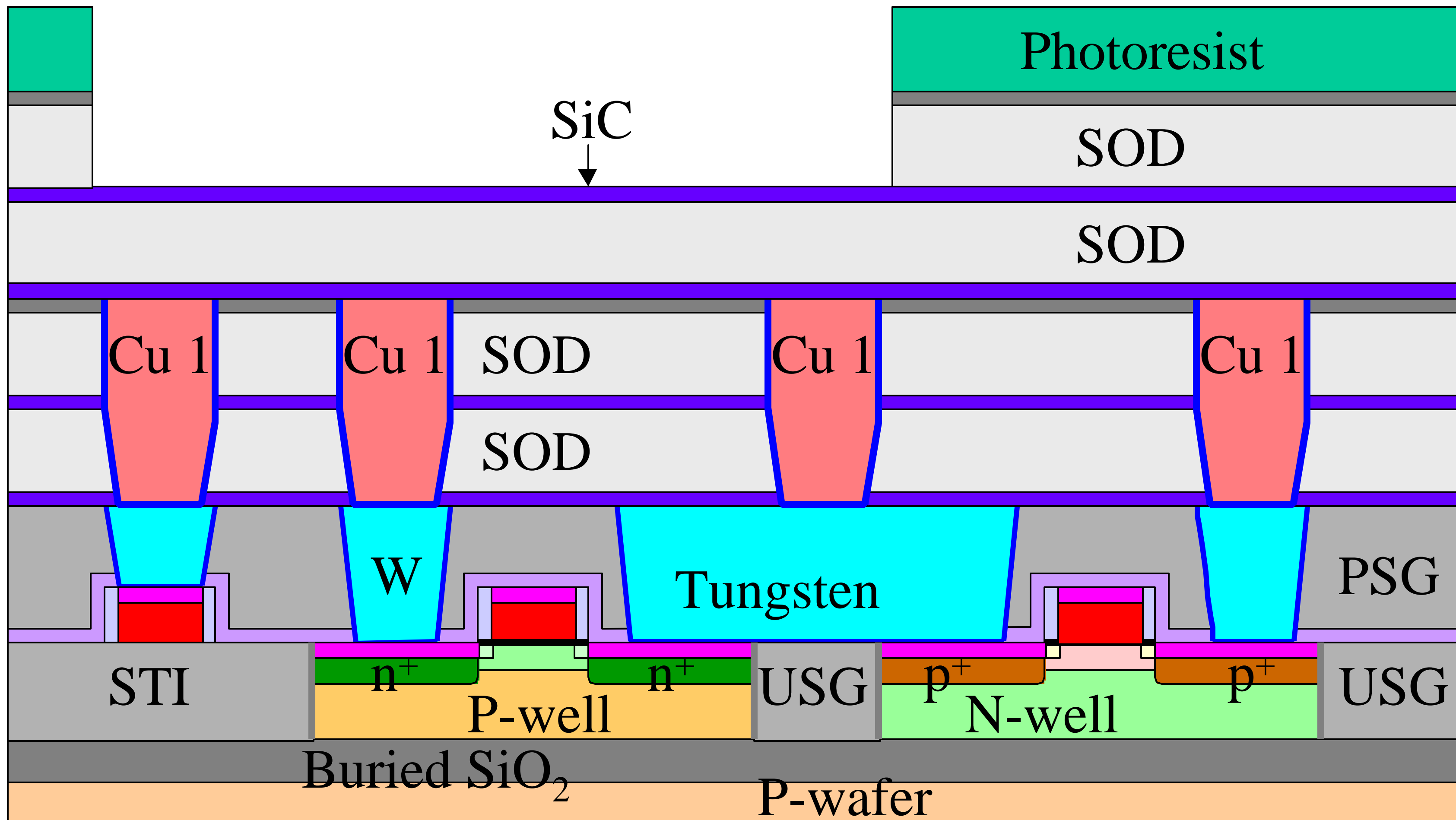
Alignment and Exposure



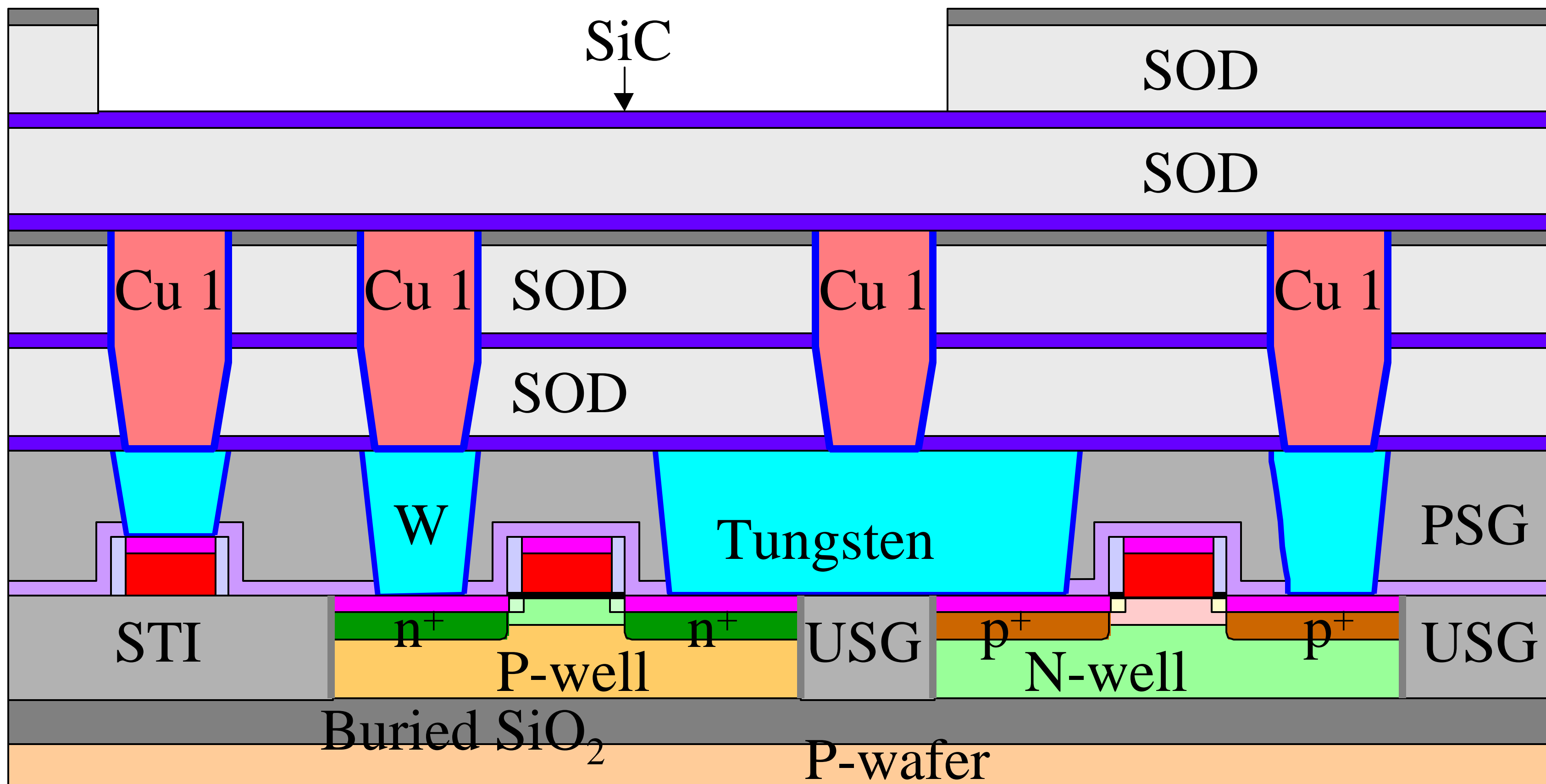
PEB, Development, and Inspection



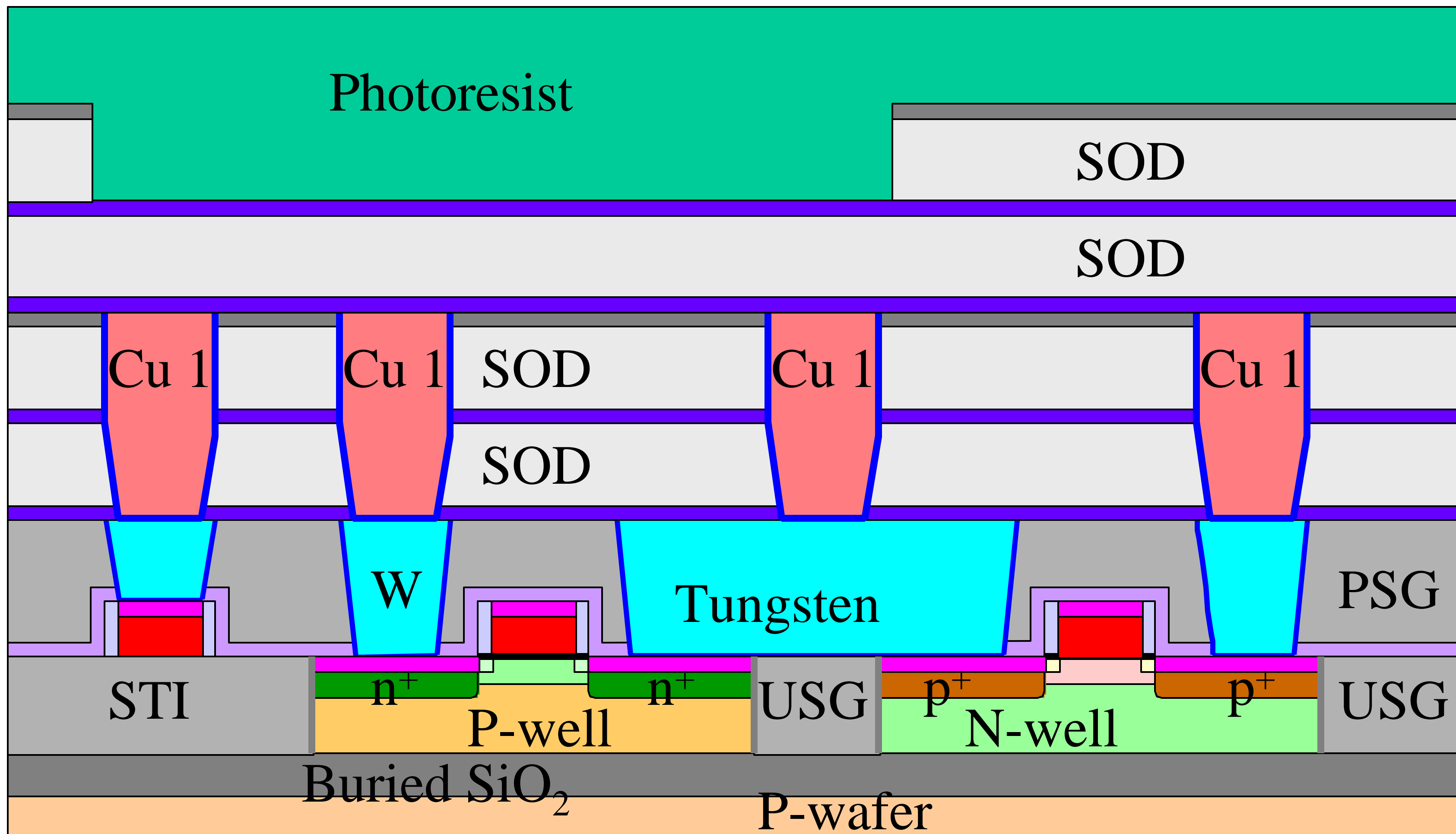
Etch Trench, Stop on SiC Layer



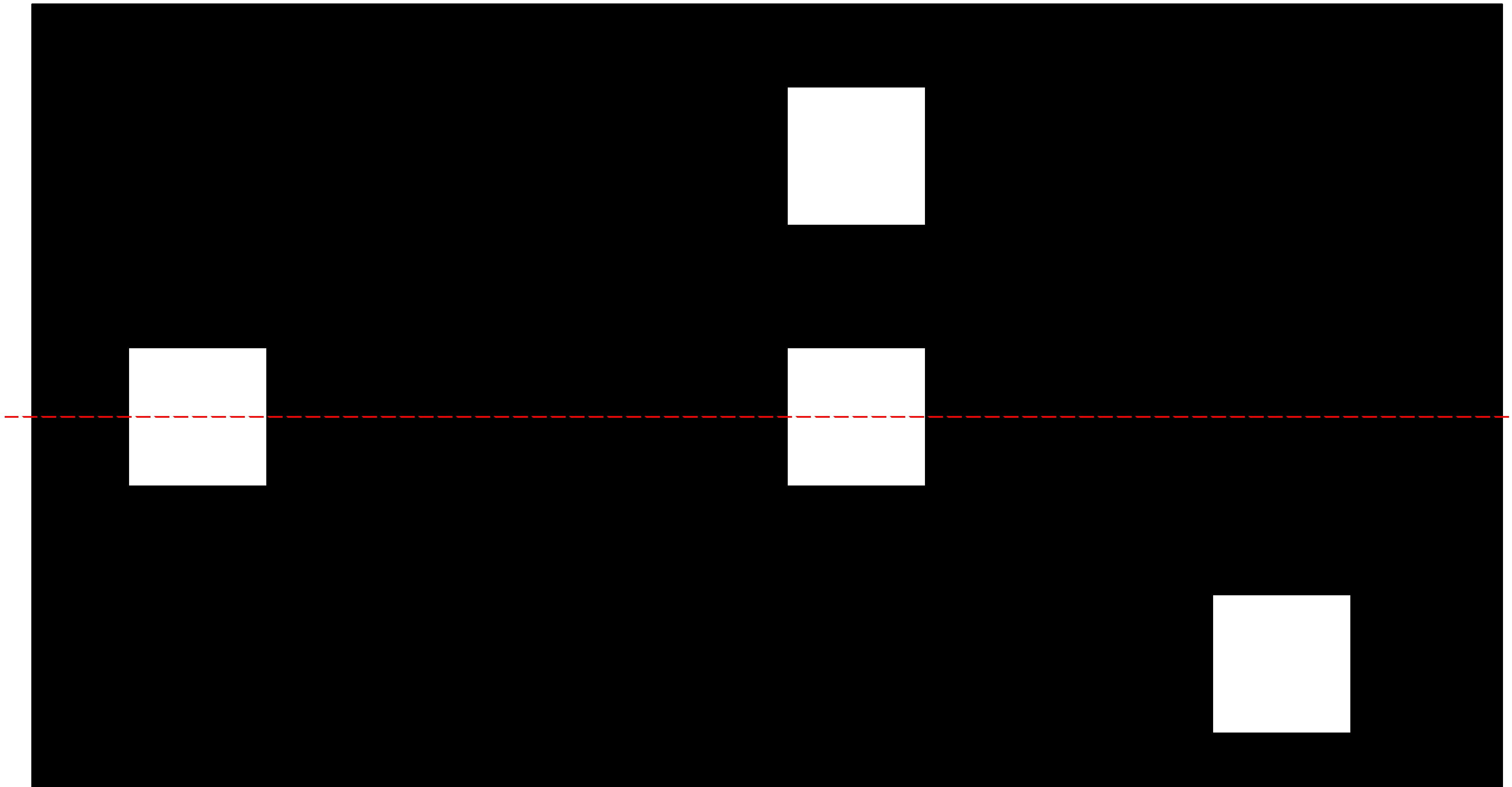
Strip Photoresist



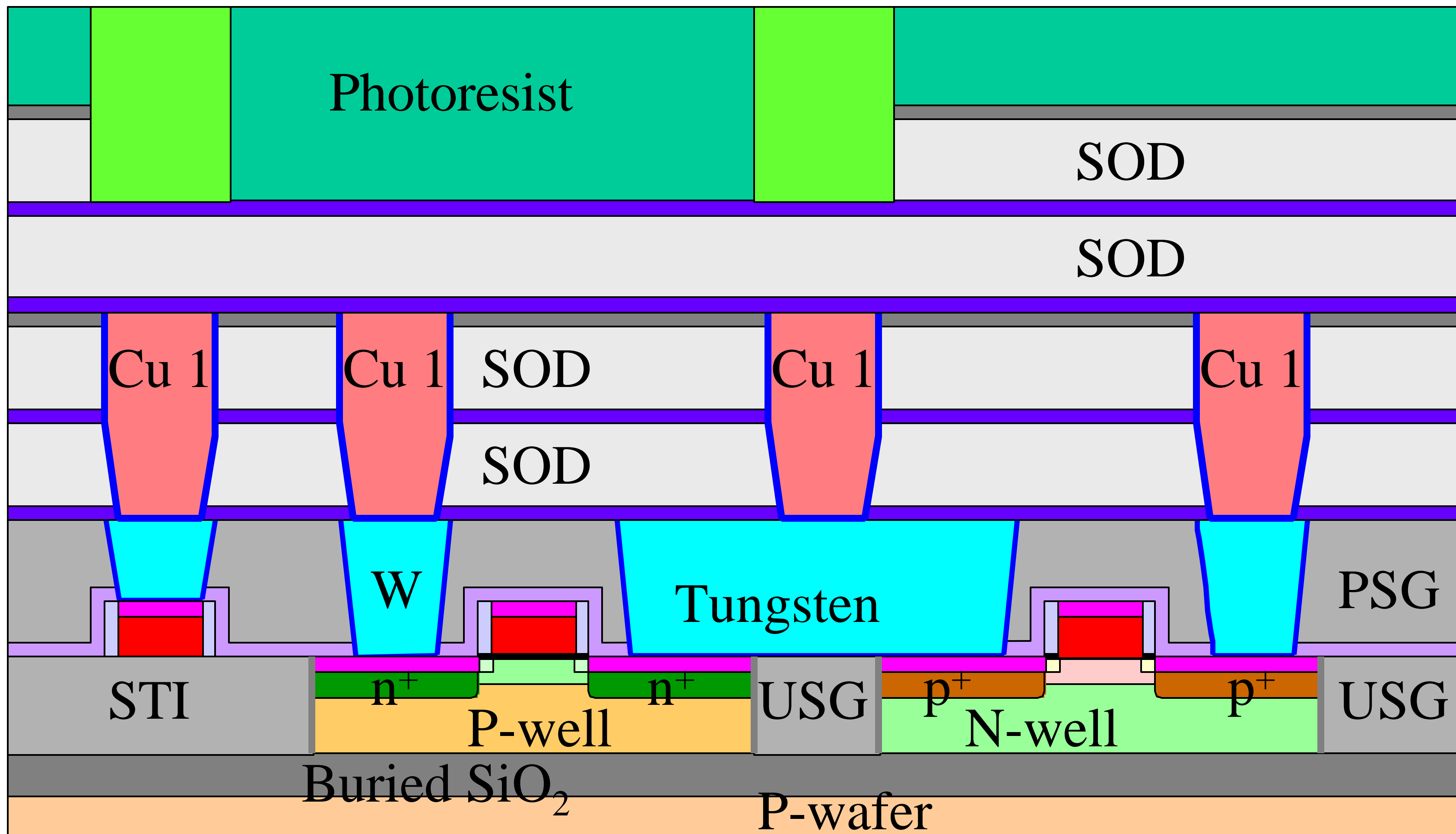
Photoresist Coating and Baking



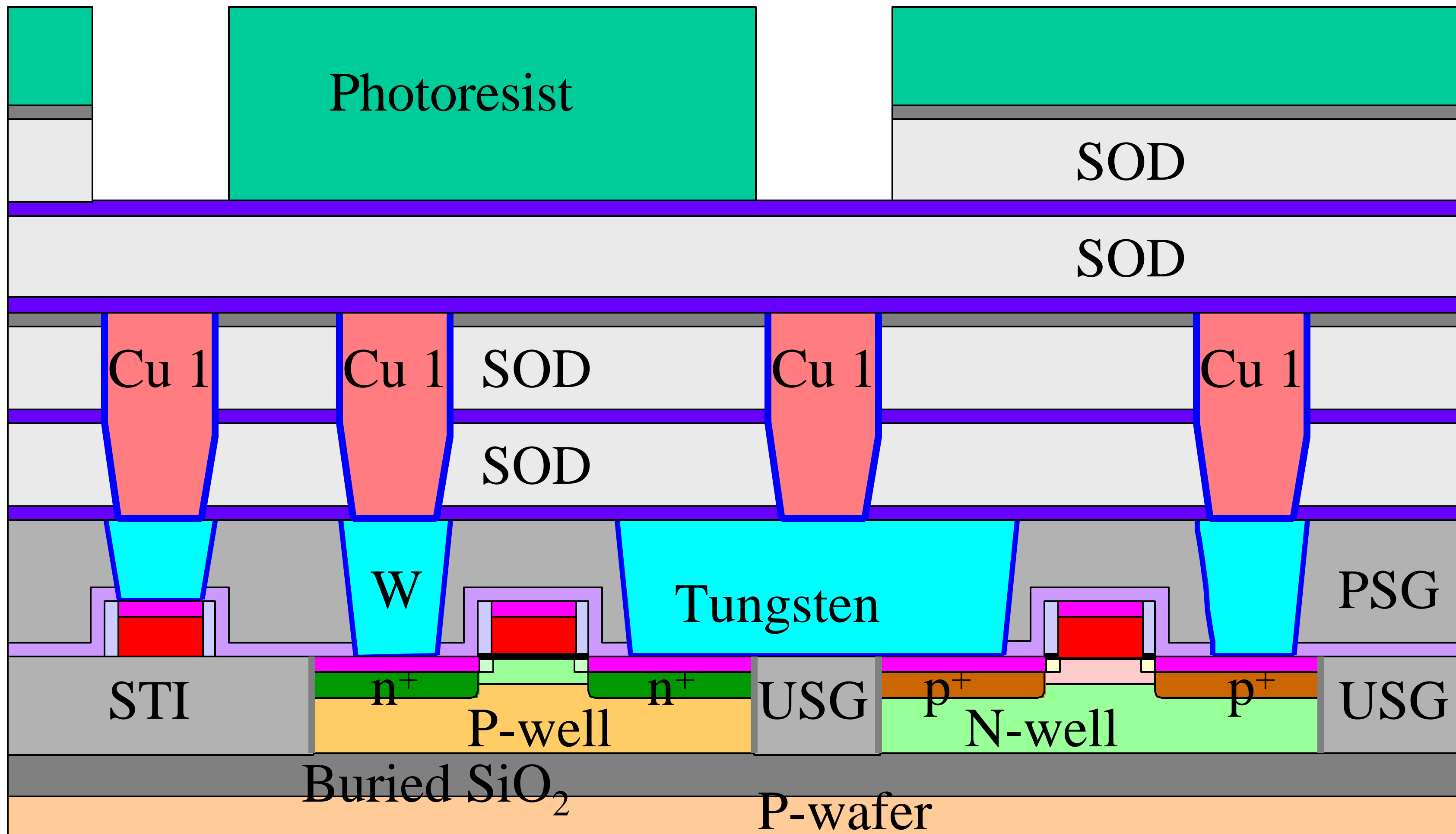
Mask 13, Via 2



Alignment and Exposure



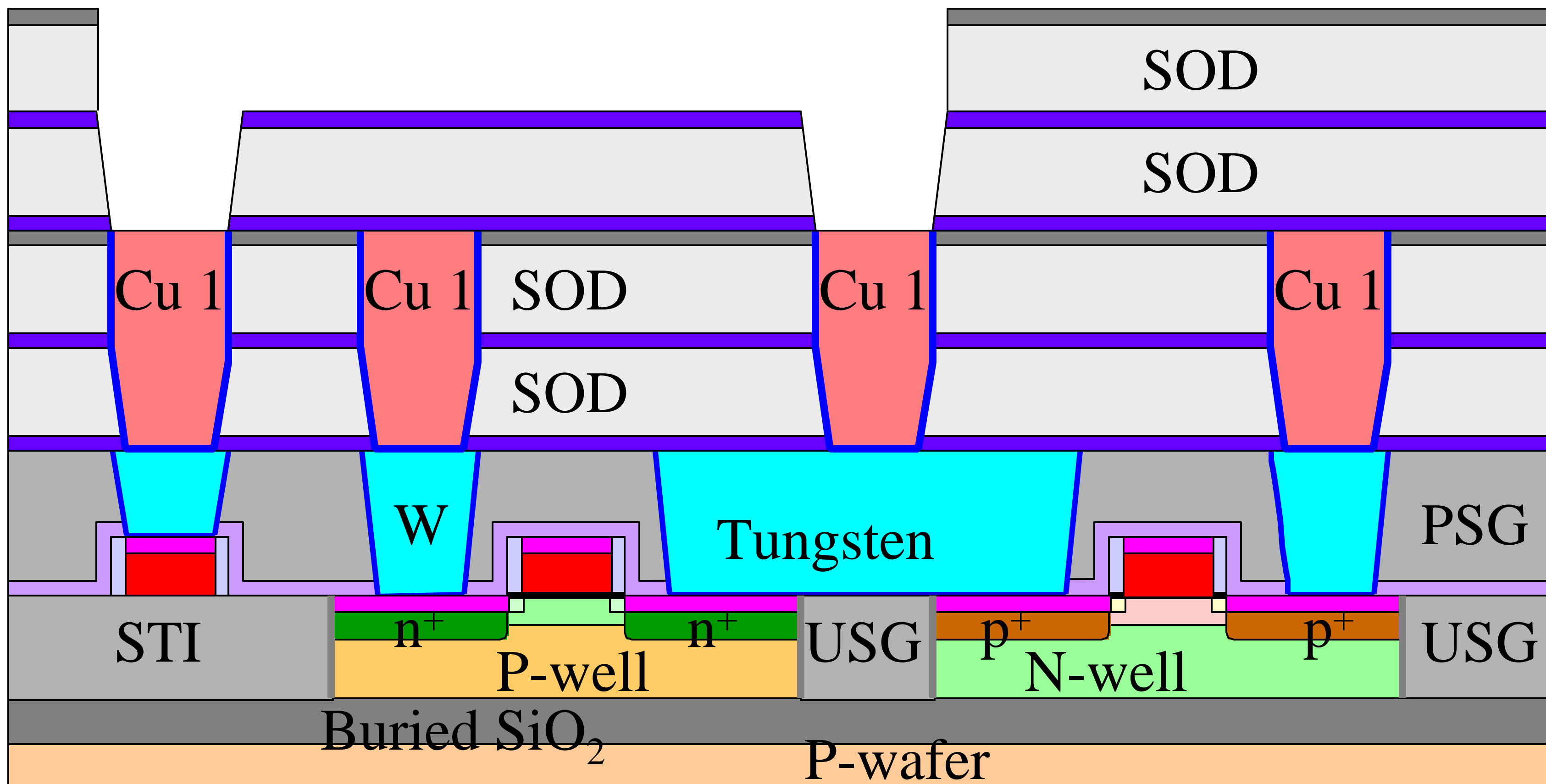
PEB, Development, and Inspection



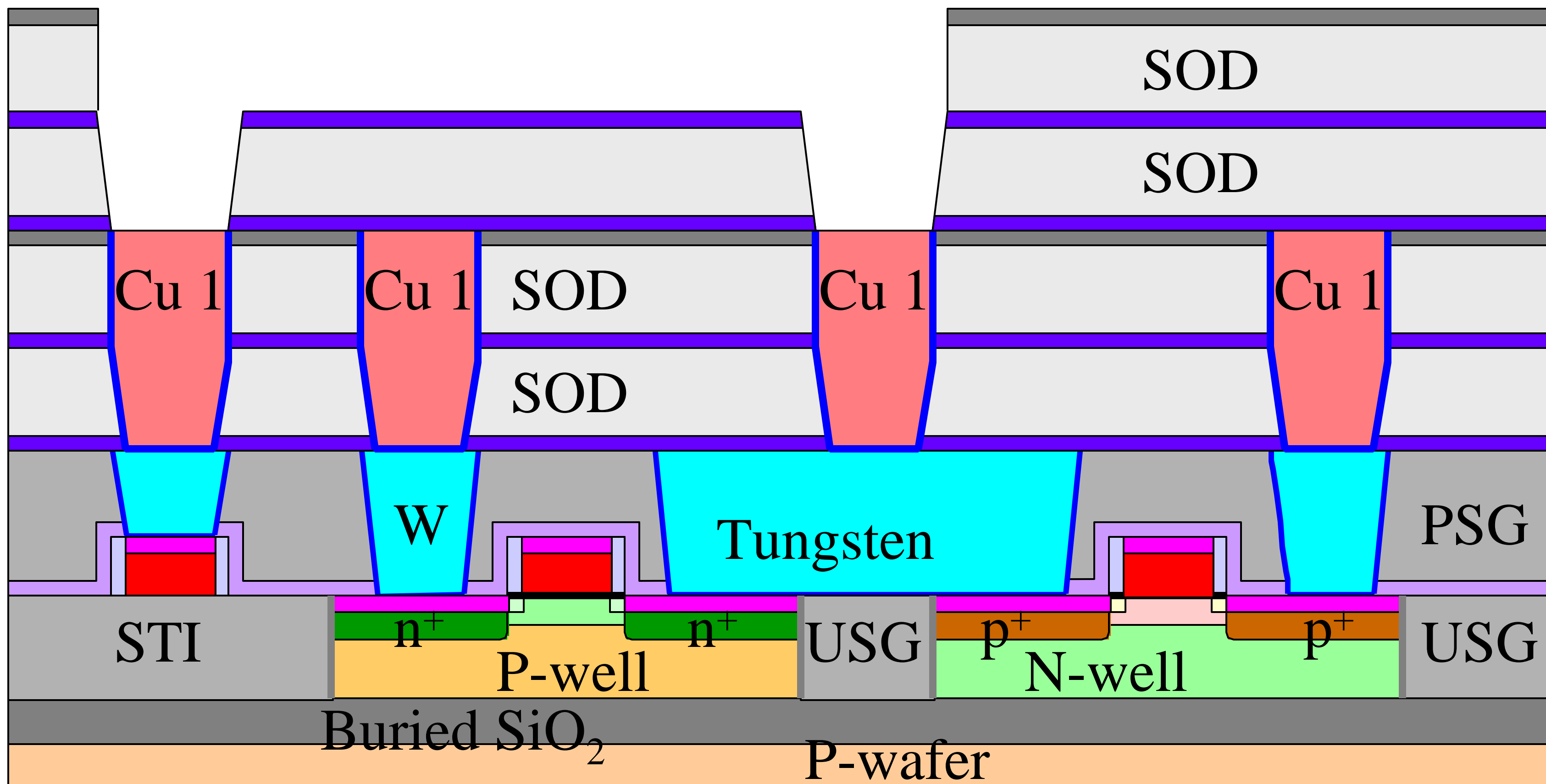
Via2 Etch

Photoresist
SOD
SOD
Cu 1
Cu 1
SOD
Cu 1
Cu 1
SOD
W
Tungsten
PSG
STI
n+
n+
USG
p+
p+
USG
P-well
N-well
Buried SiO_2
P-wafer

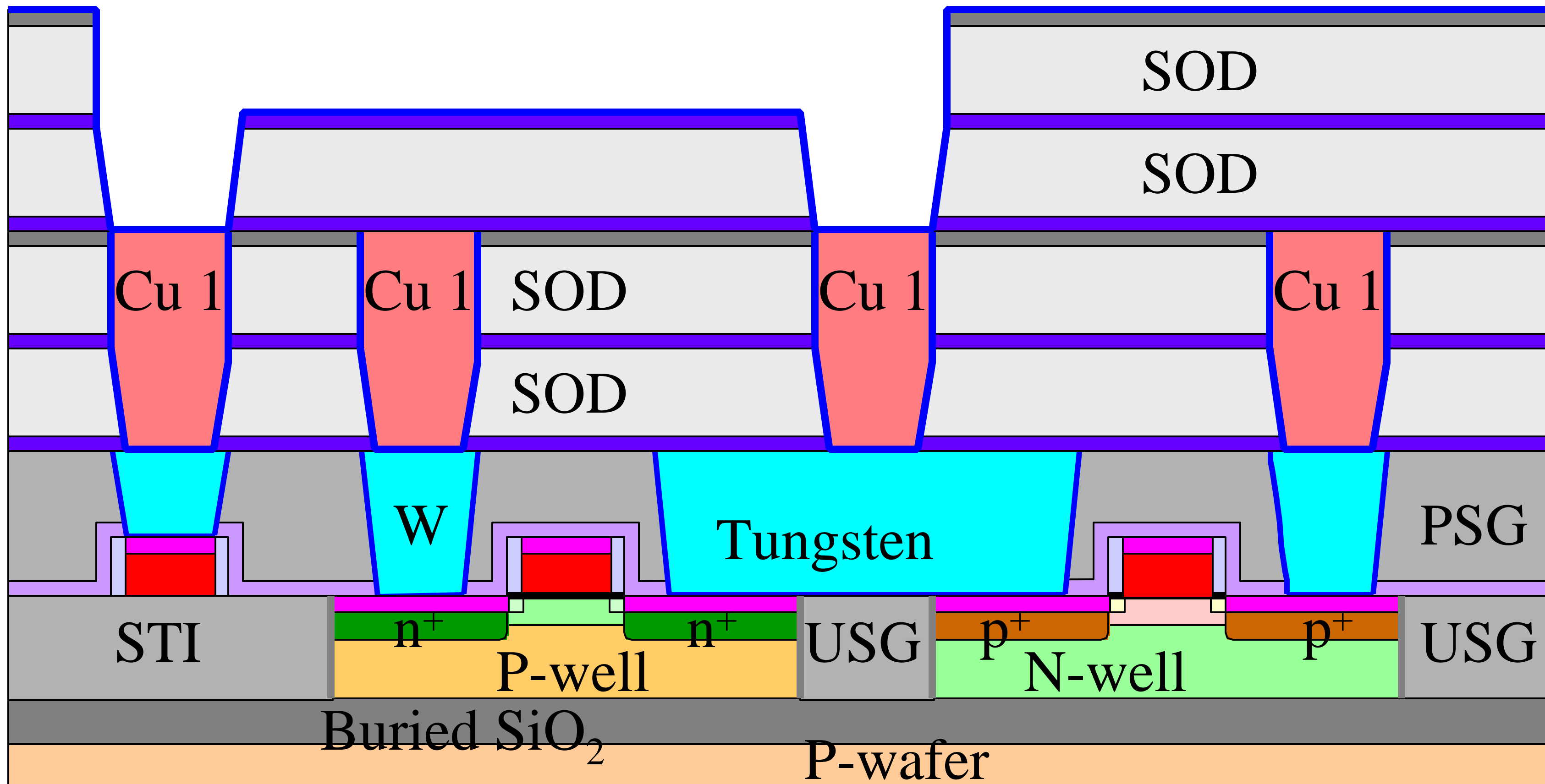
Strip Photoresist



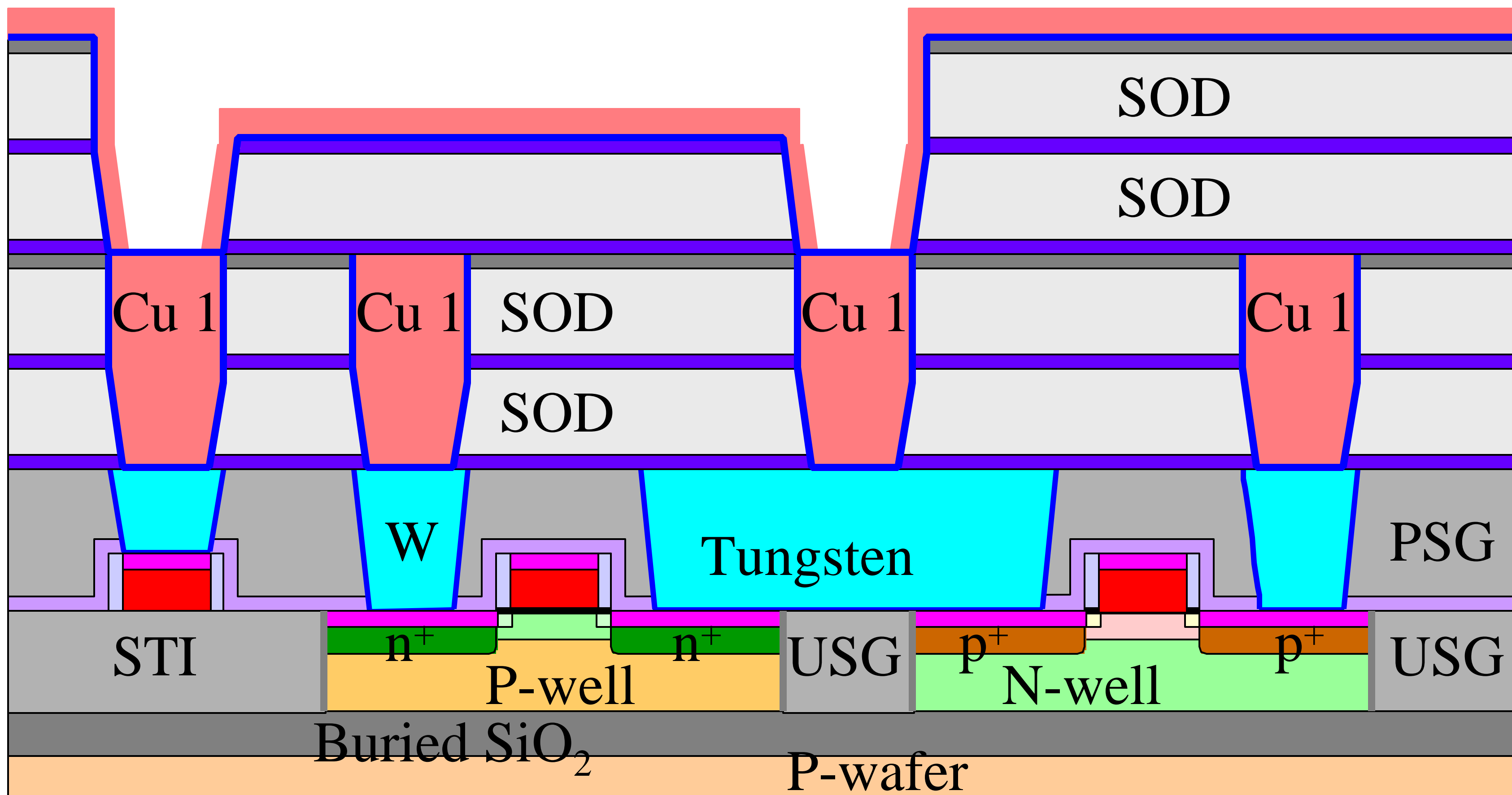
Hydrogen Plasma Clean



Ta and TaN Barrier Layer PVD

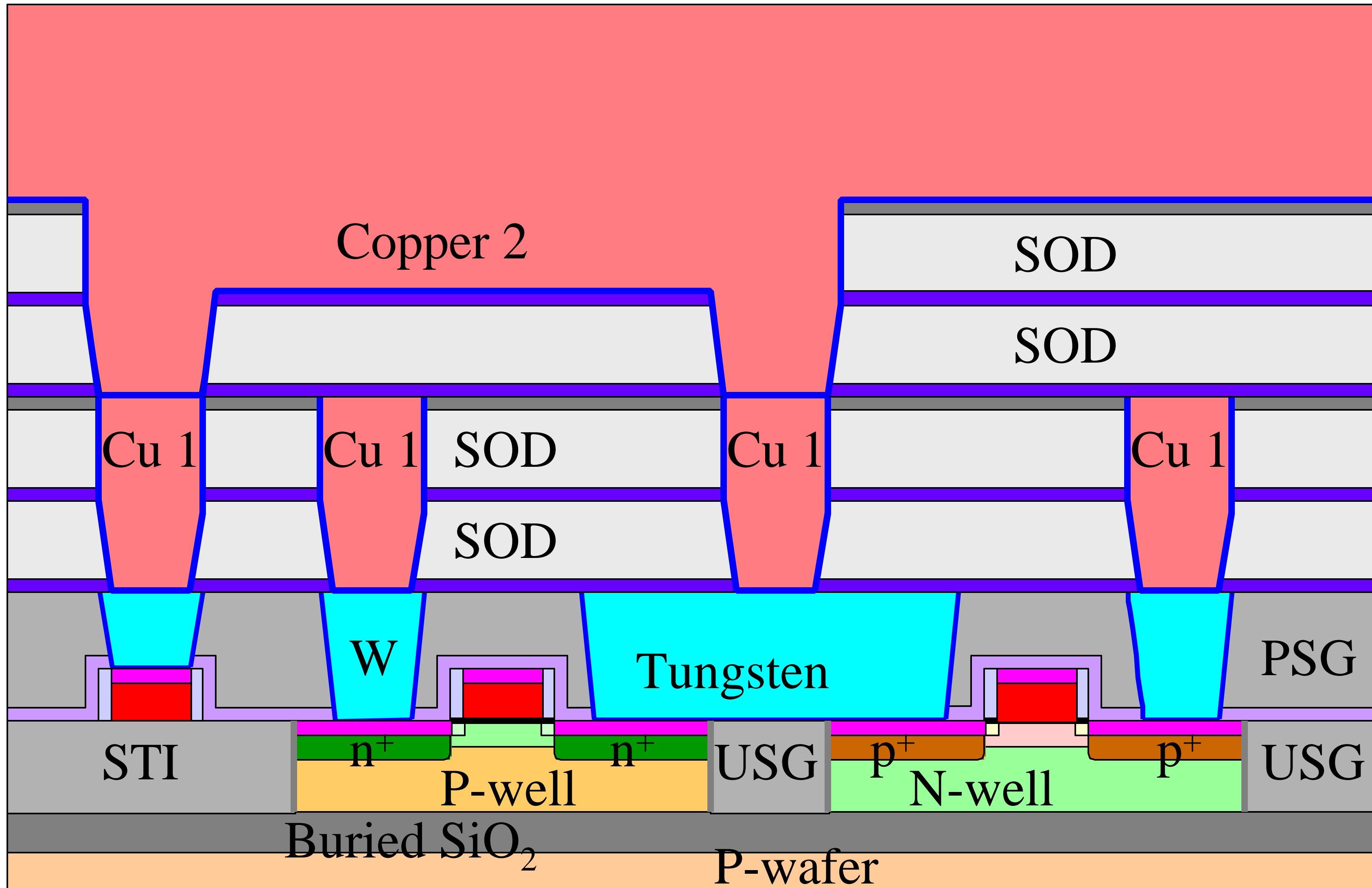


Cu Seed Layer PVD

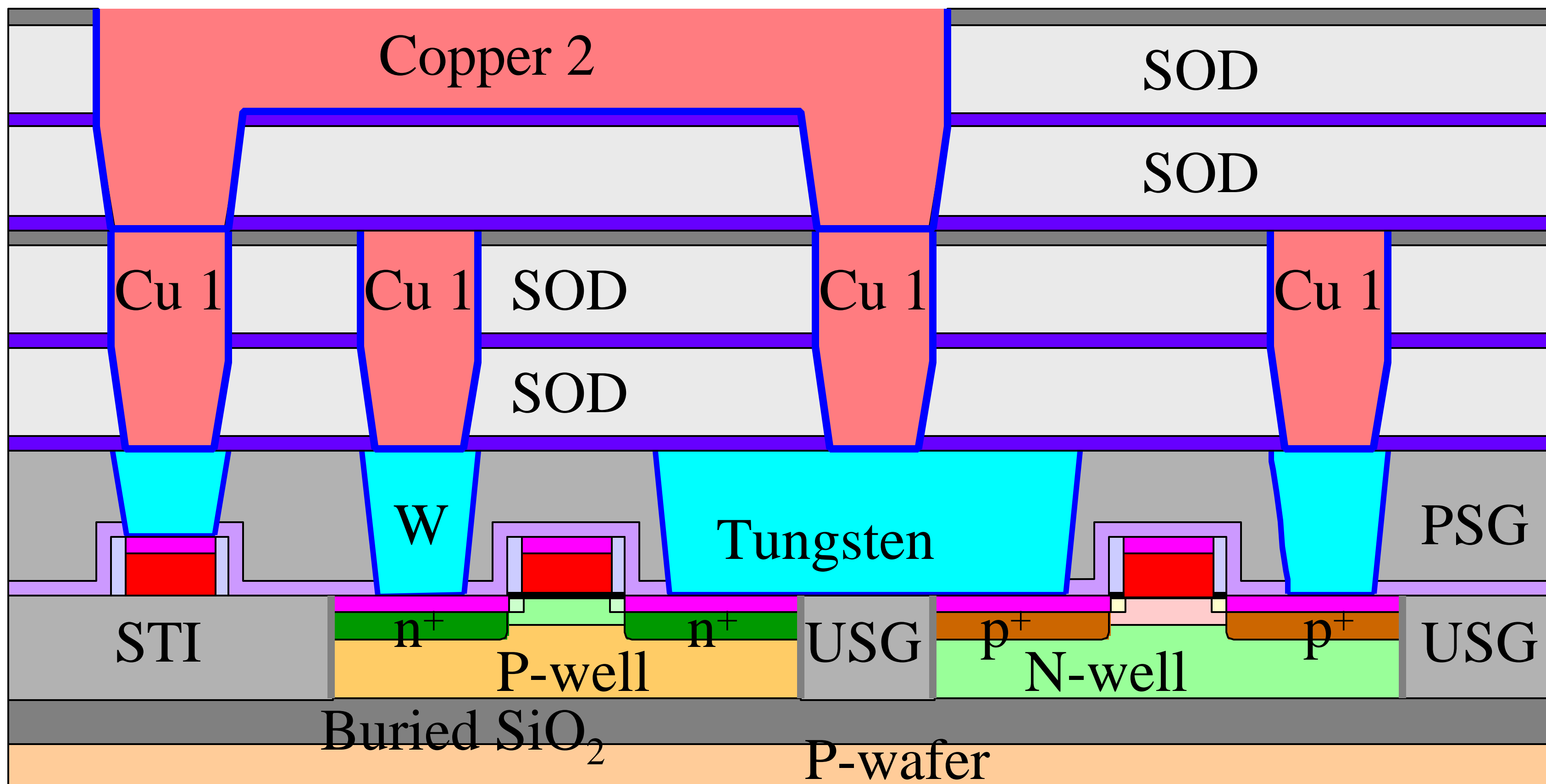


Bulk Cu ECP

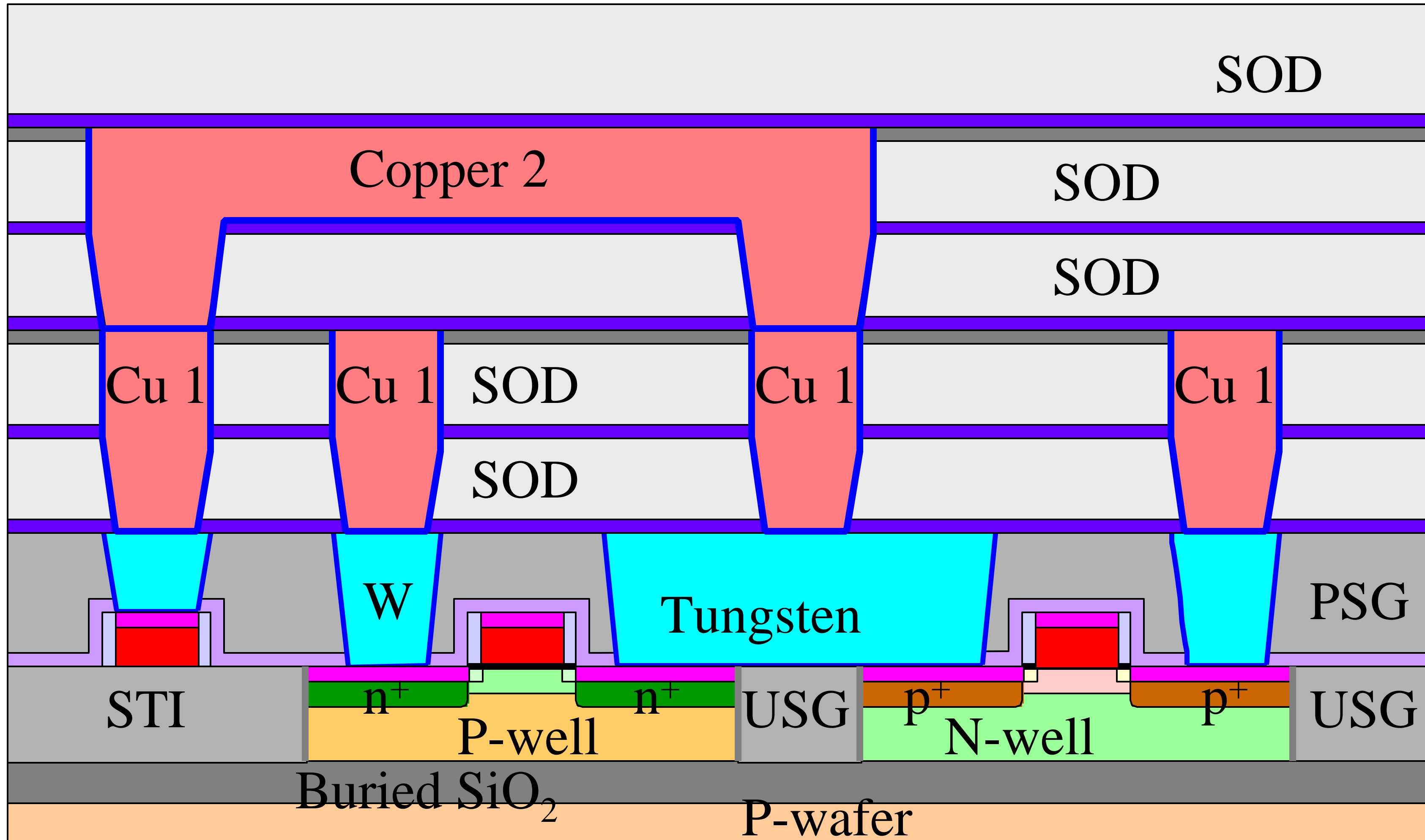
Copper Anneal



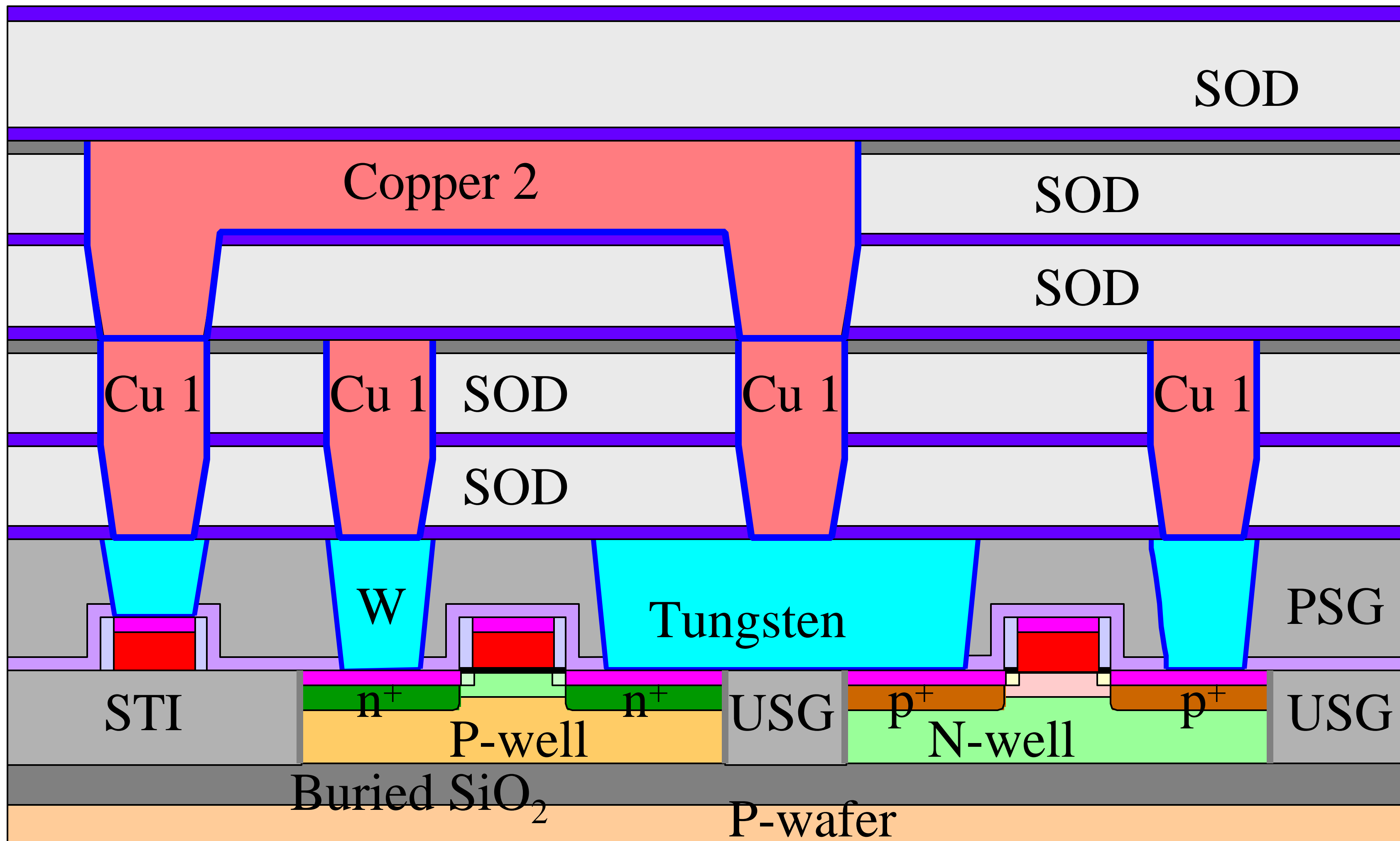
Cu, Ta, and TaN CMP



PECVD SiC, SOD Coating and Curing



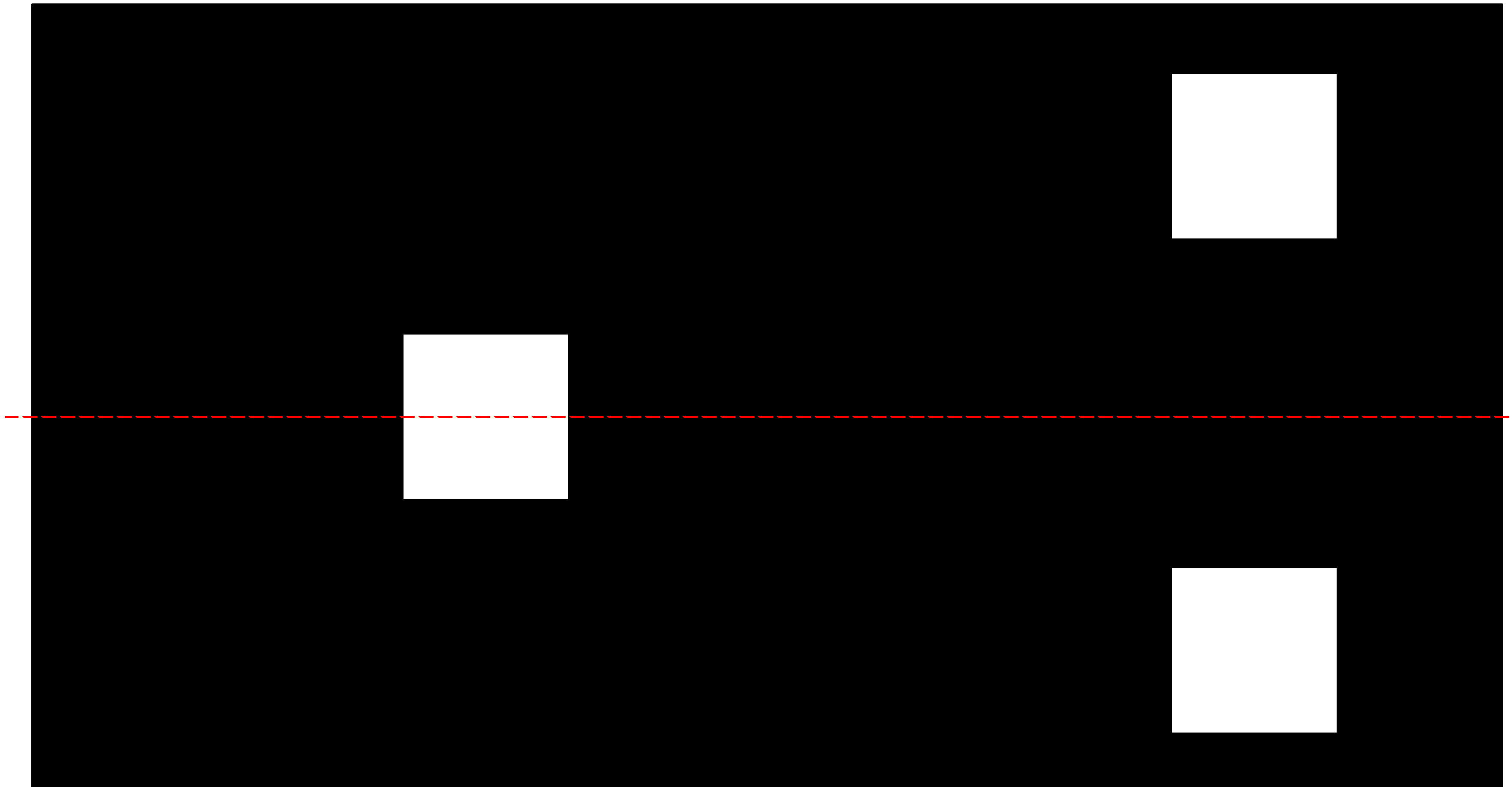
PECVD SiC Etch Stop Layer



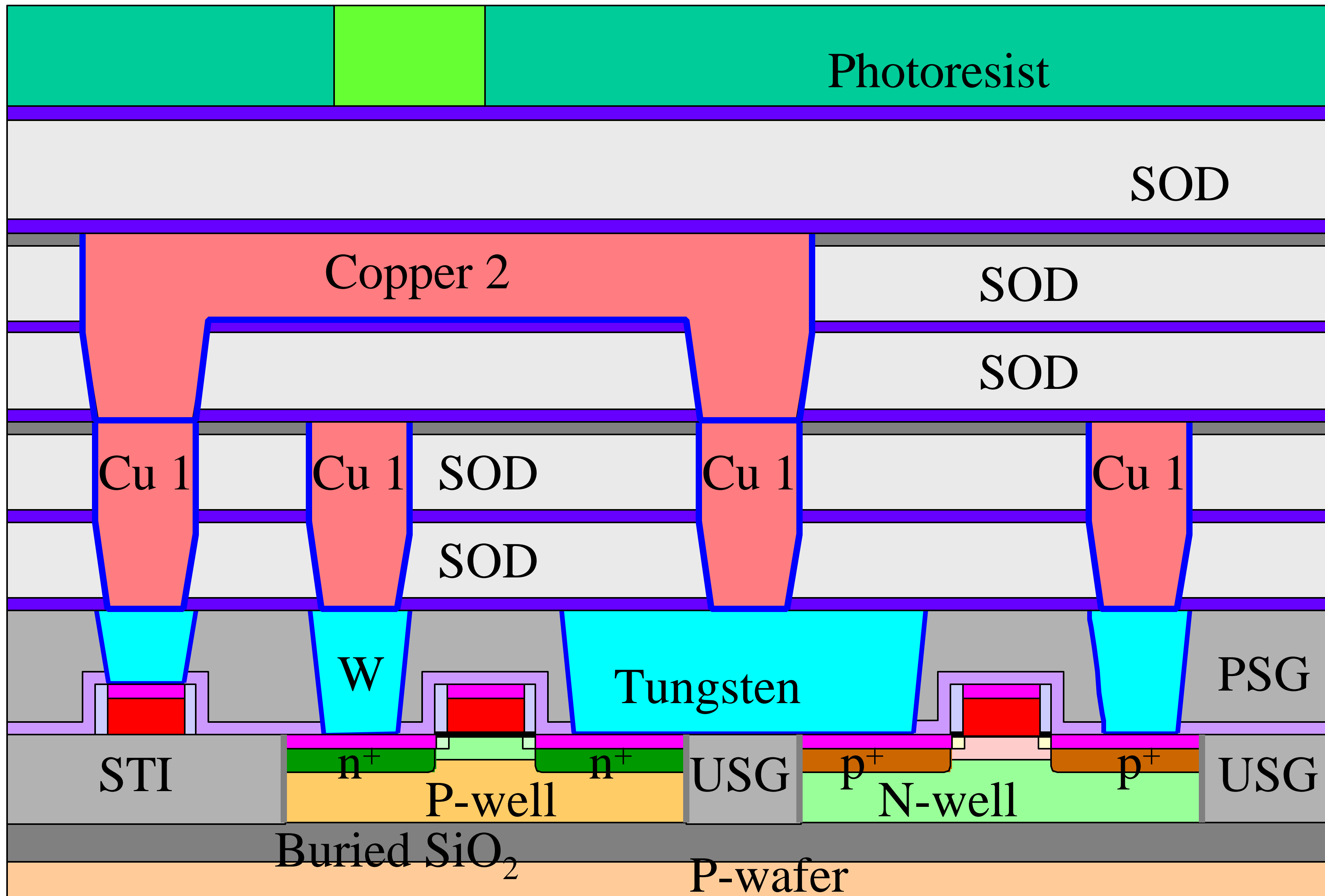
Photoresist Coating and Baking

Photoresist
SOD
Copper 2
SOD
SOD
Cu 1
Cu 1
SOD
Cu 1
Cu 1
SOD
W
Tungsten
PSG
STI
n^+
n^+
USG
p^+
p^+
USG
P-well
N-well
Buried SiO_2
P-wafer

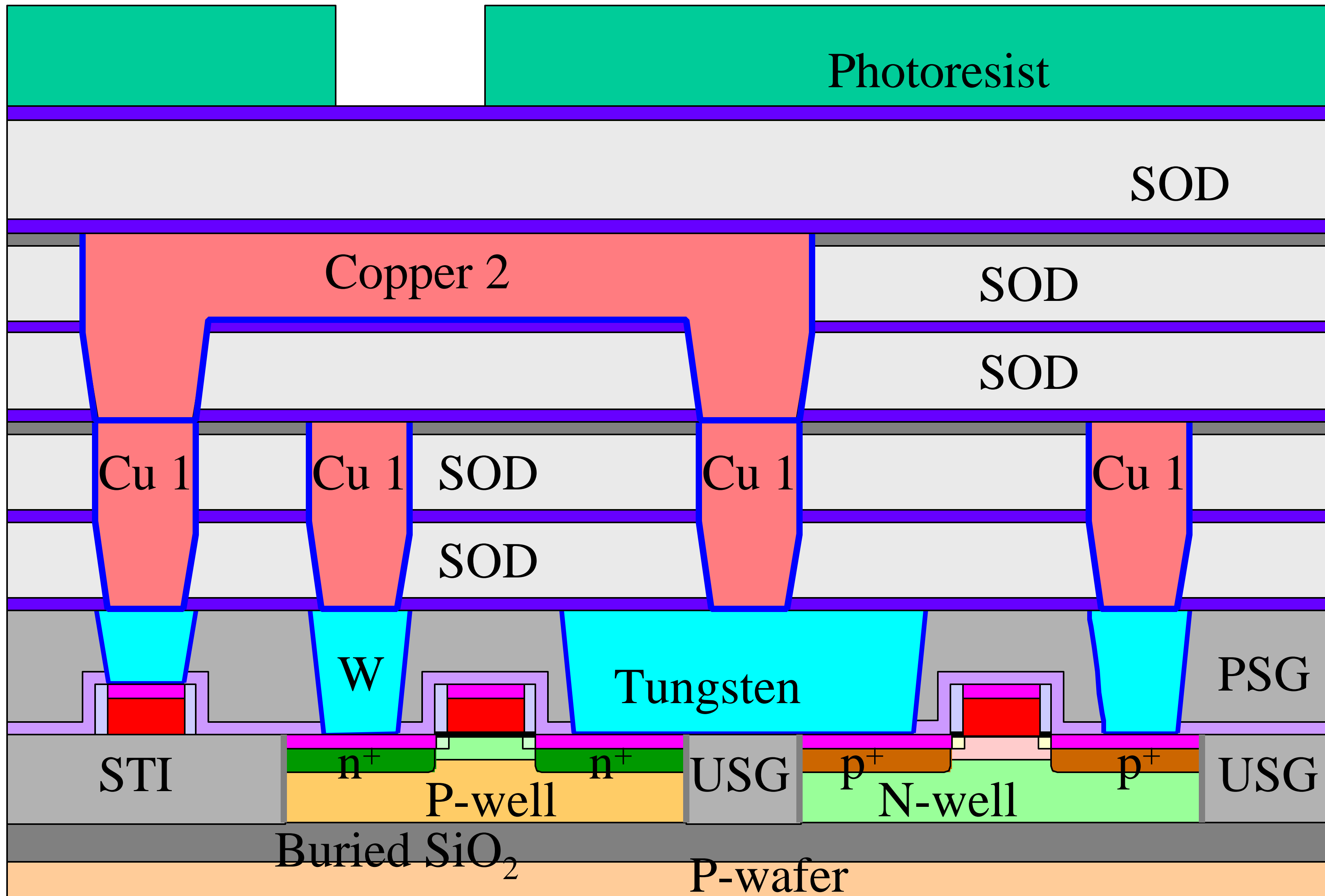
Mask 14, Via 3



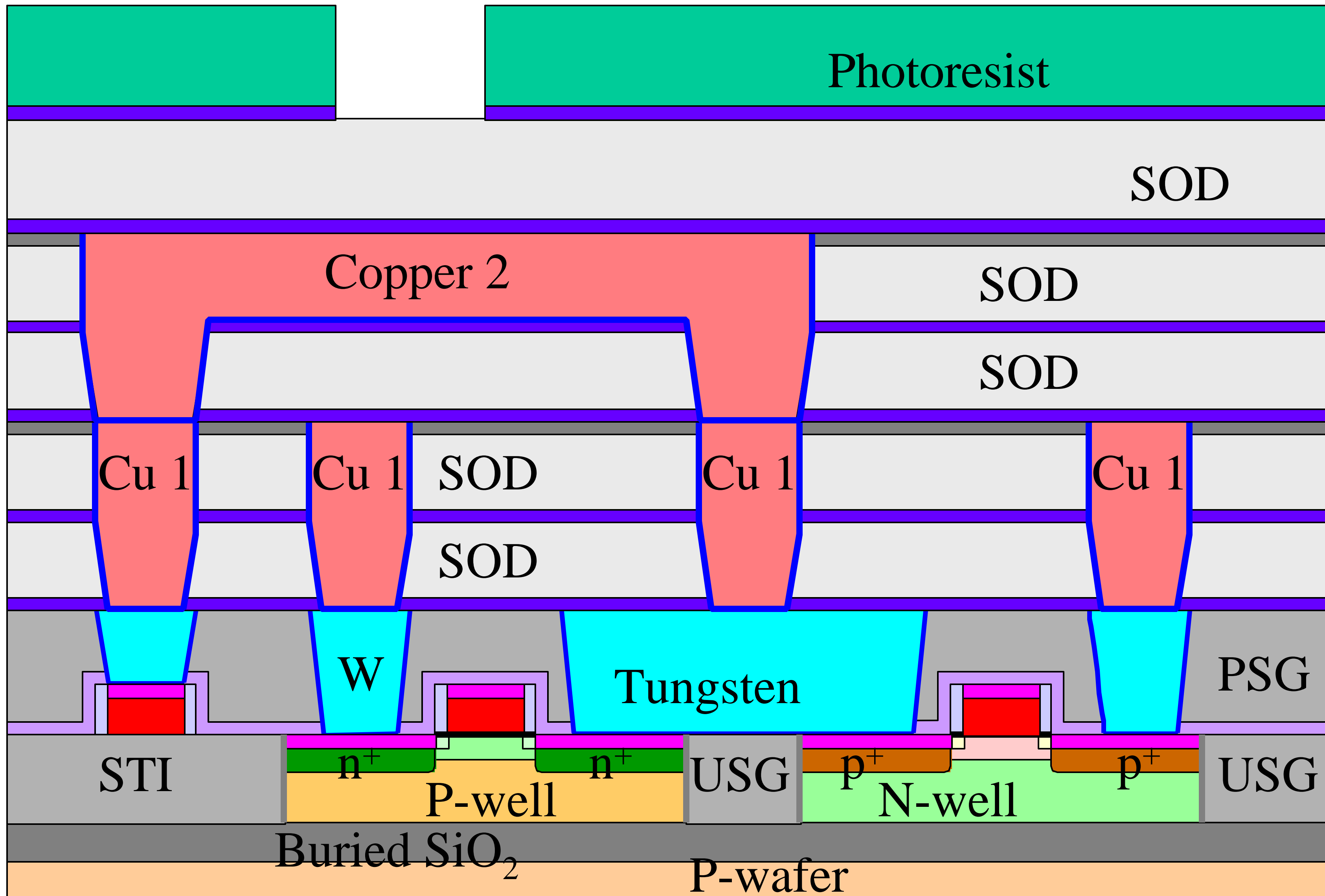
Alignment and Exposure



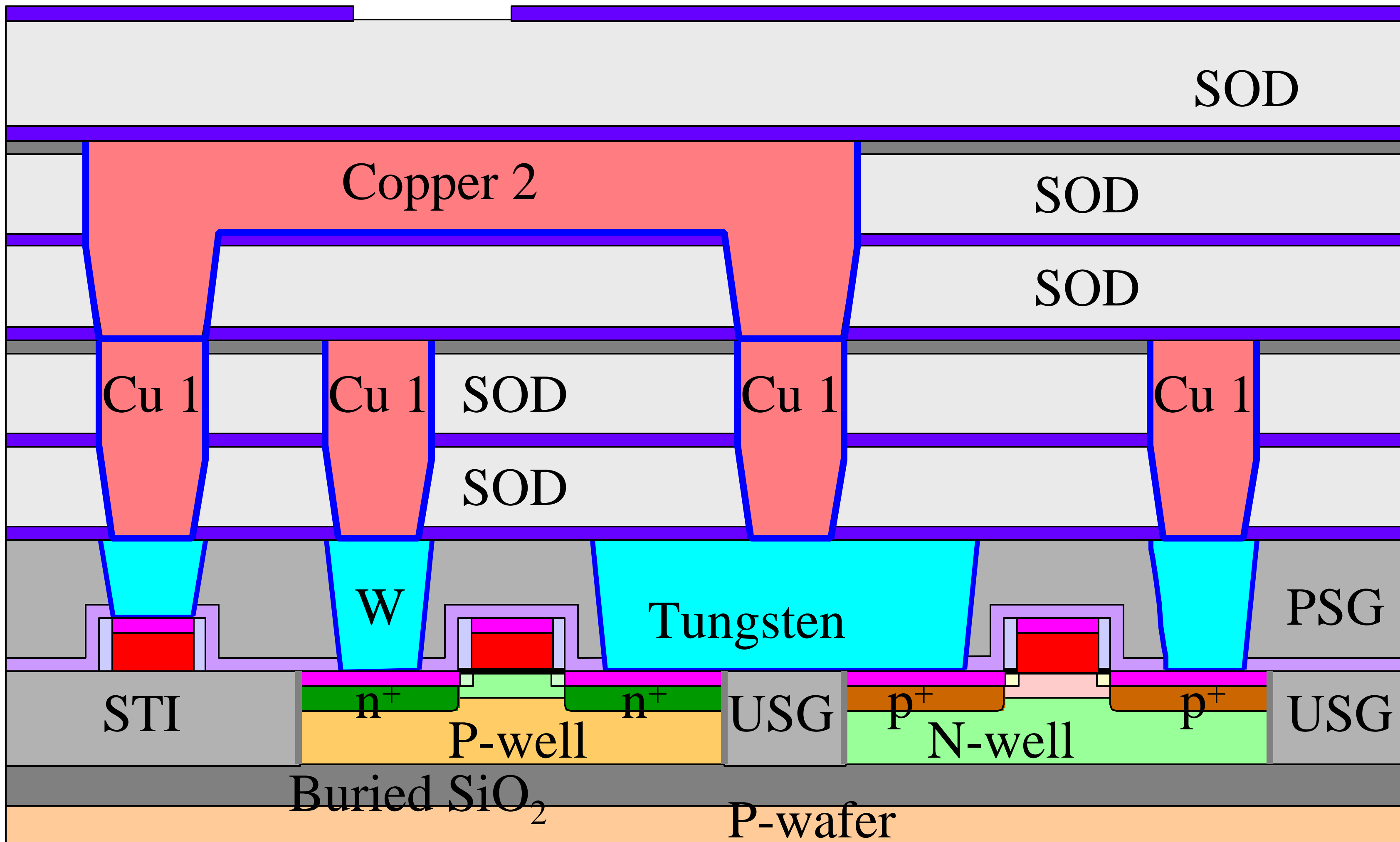
PEB, Development, and Inspection



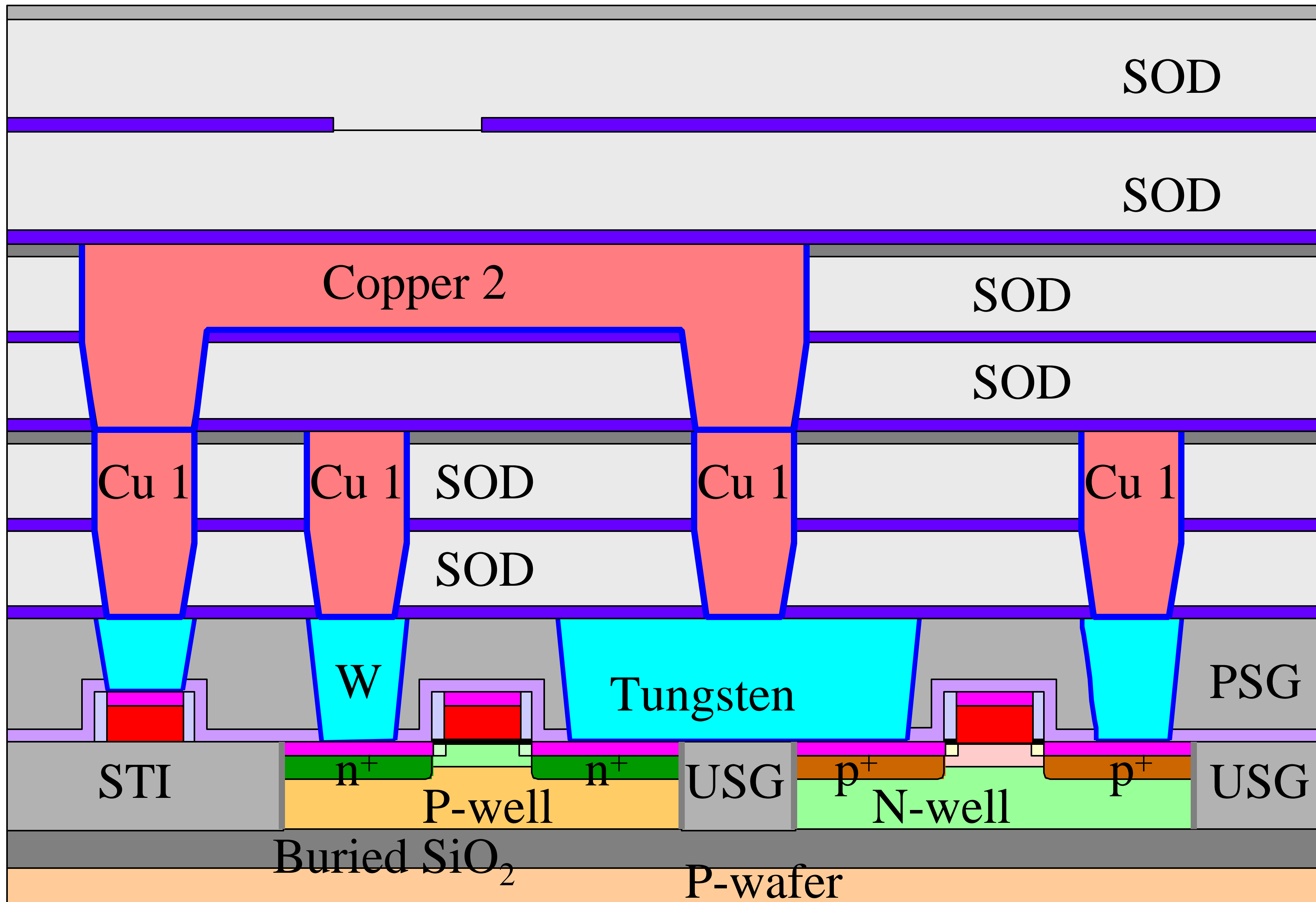
Etch SiC



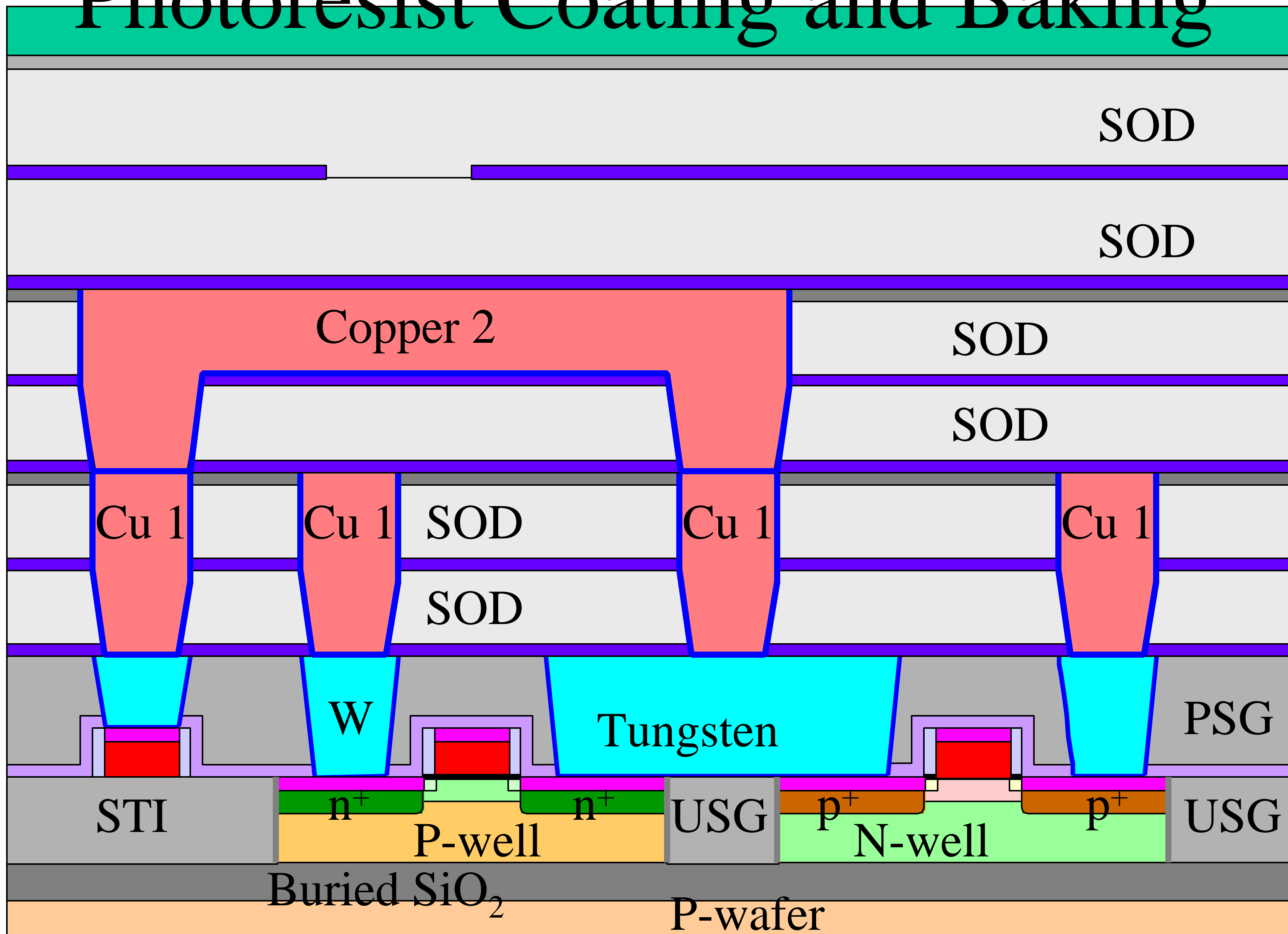
Strip Photoresist



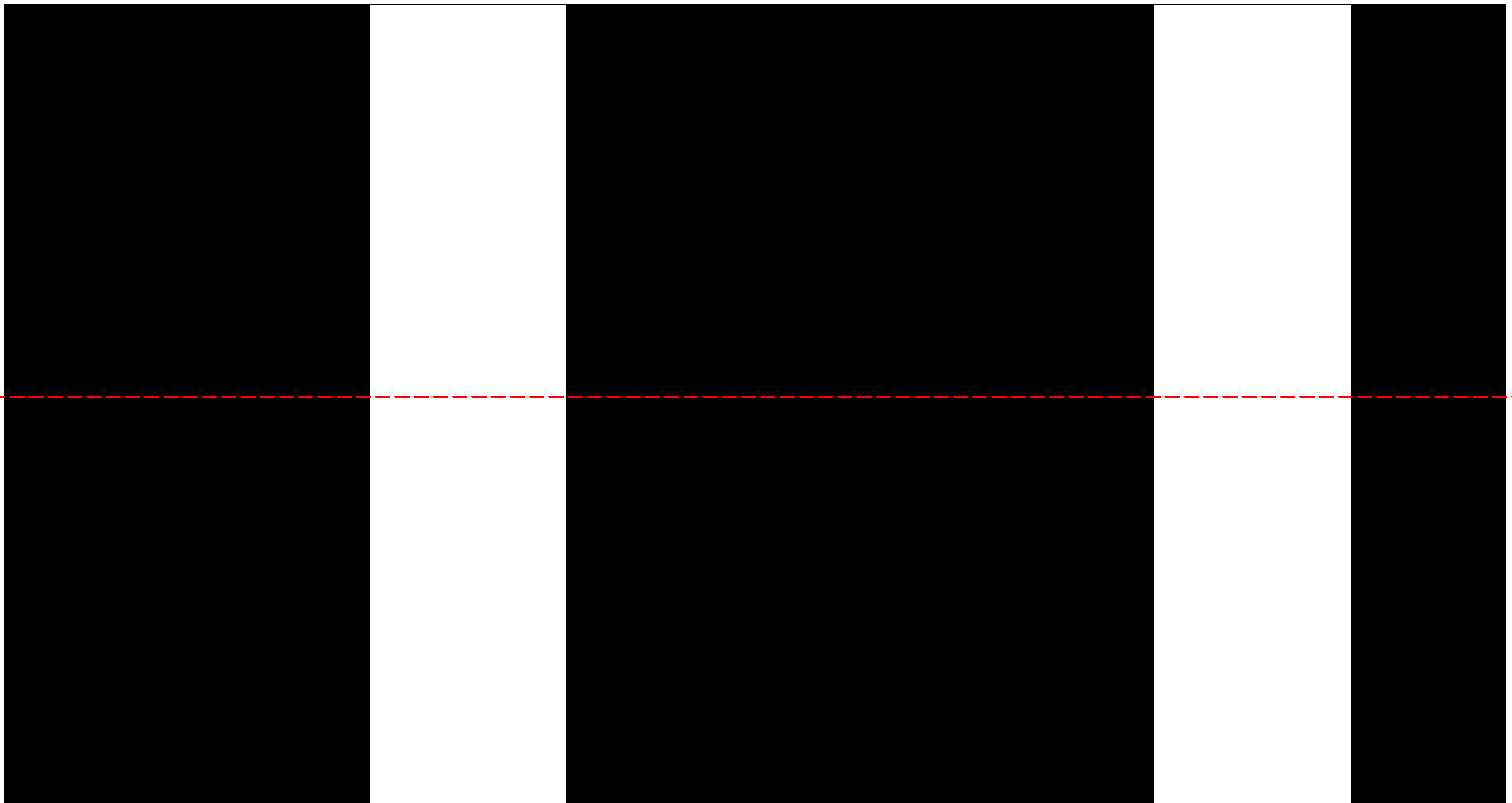
SOD Coating & Curing, PE-TEOS Cap



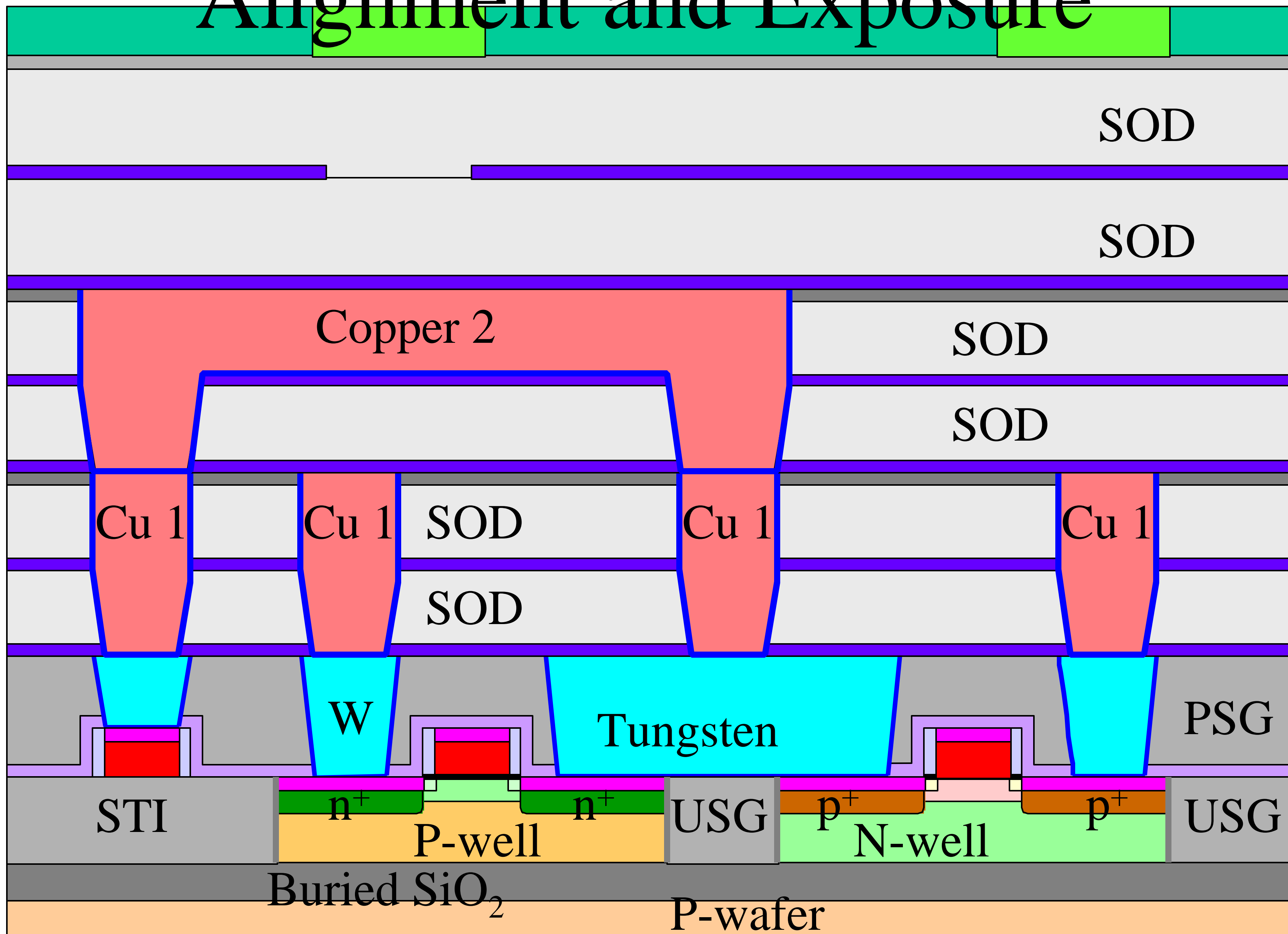
Photoresist Coating and Baking



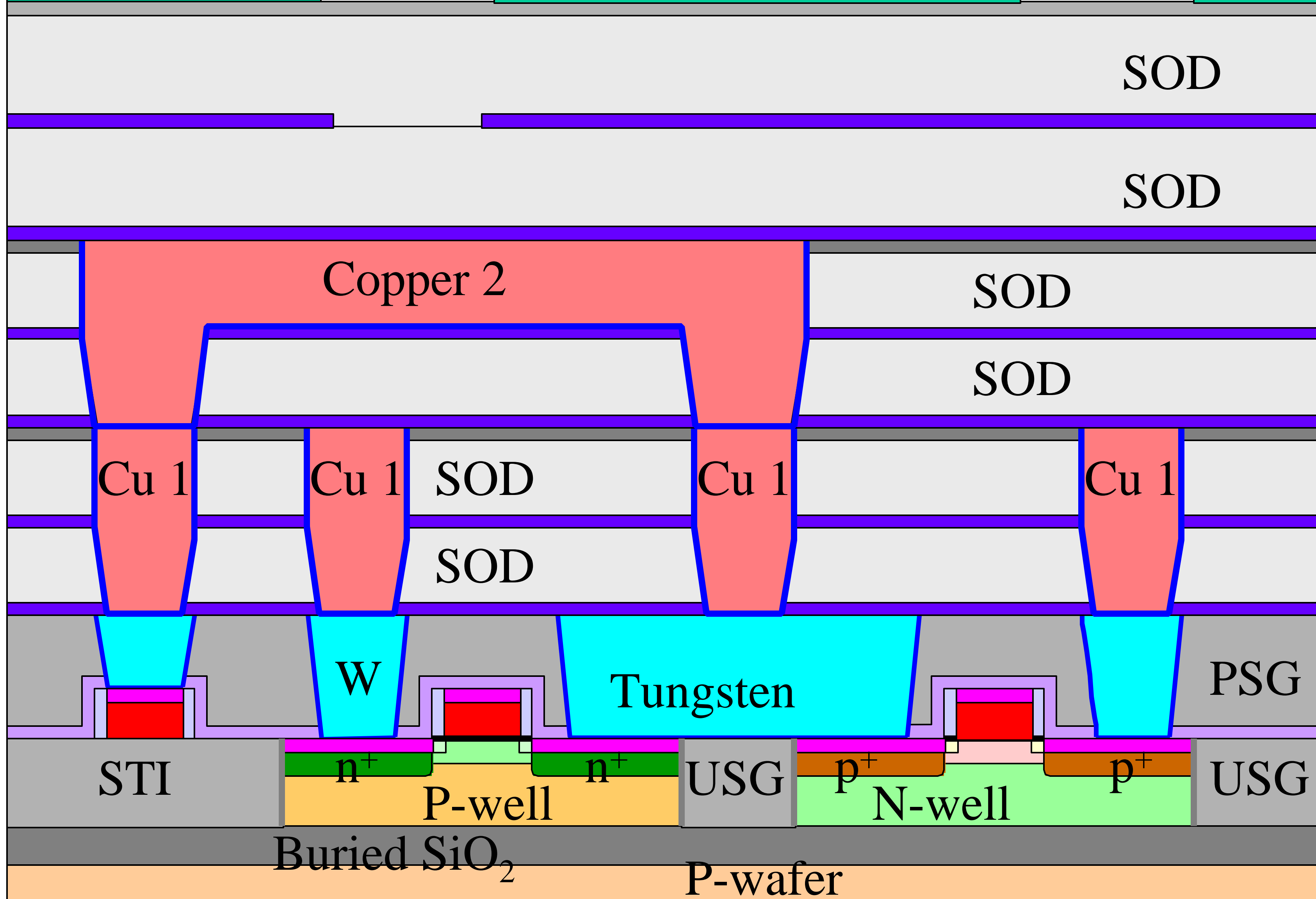
Mask 15, Metal Trench 3



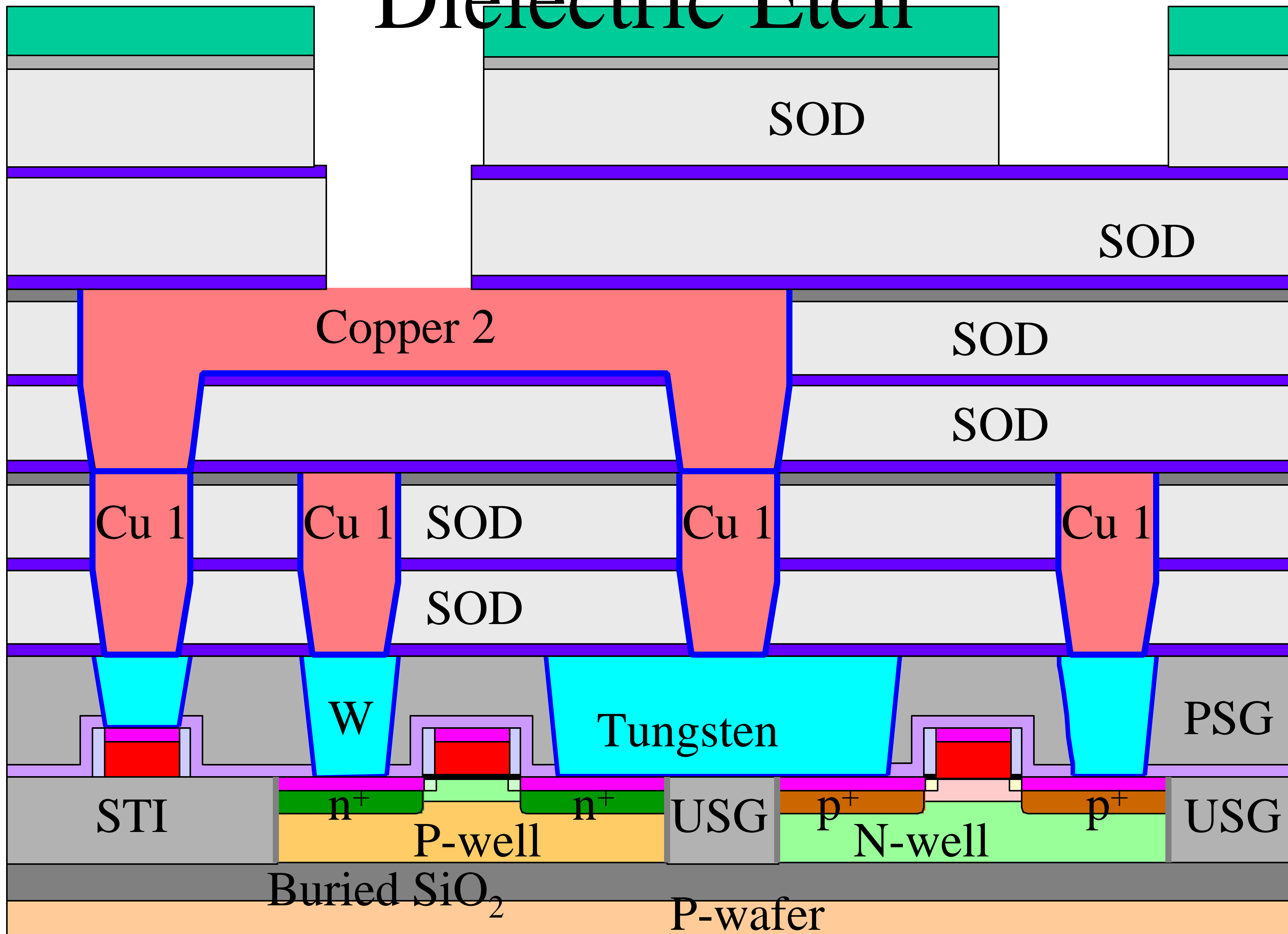
Alignment and Exposure



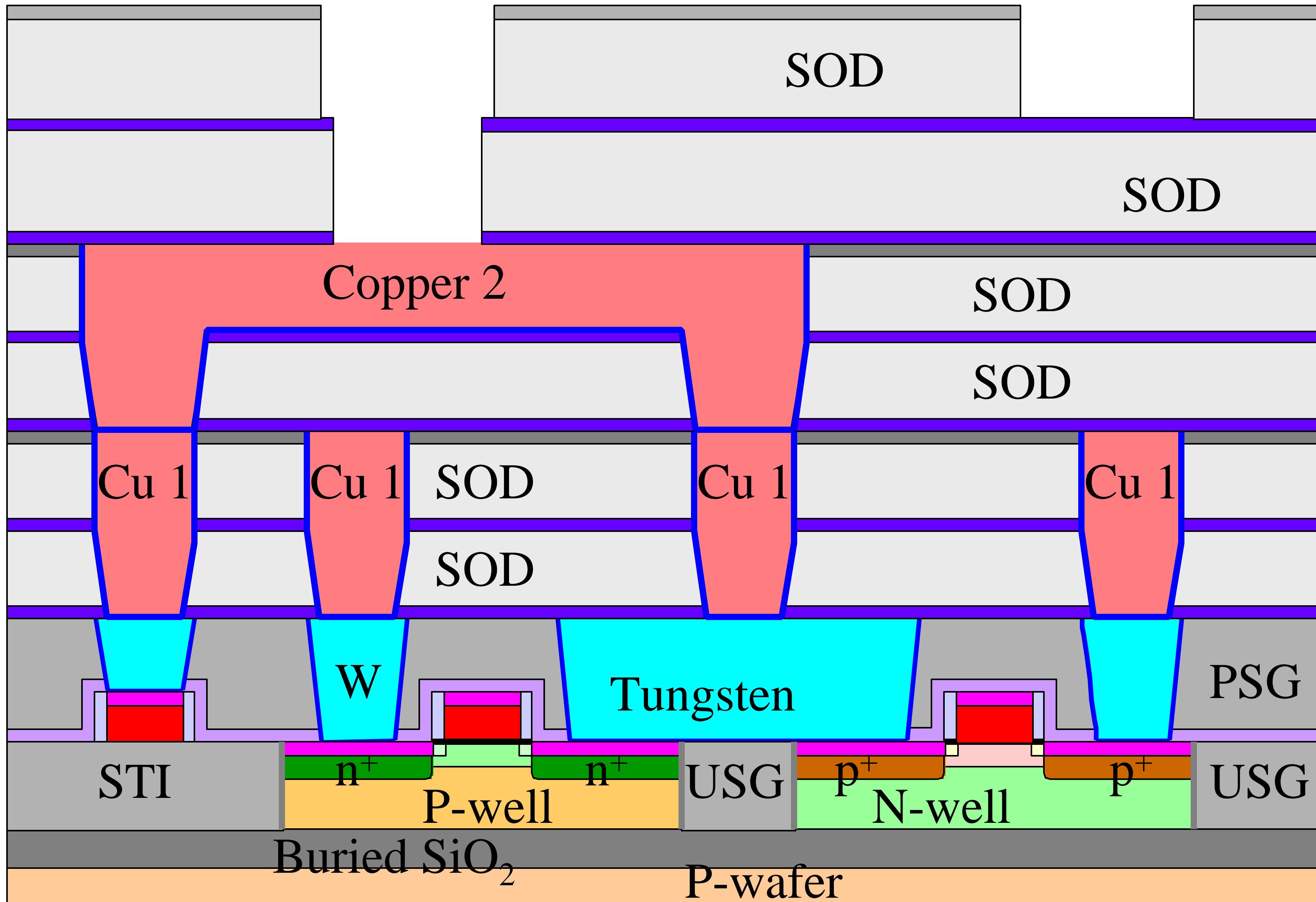
PEB, Development, and Inspection



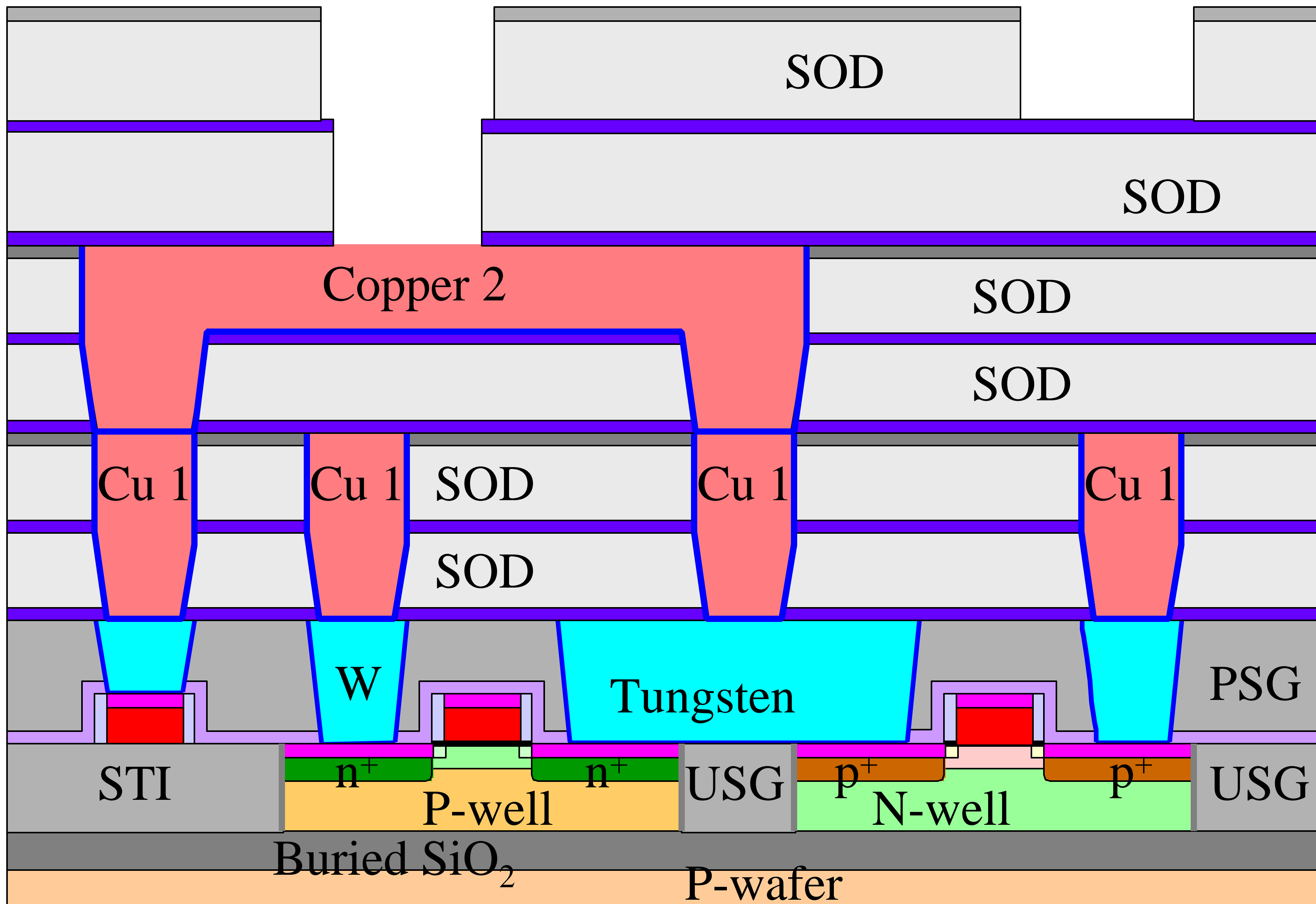
Dielectric Etch



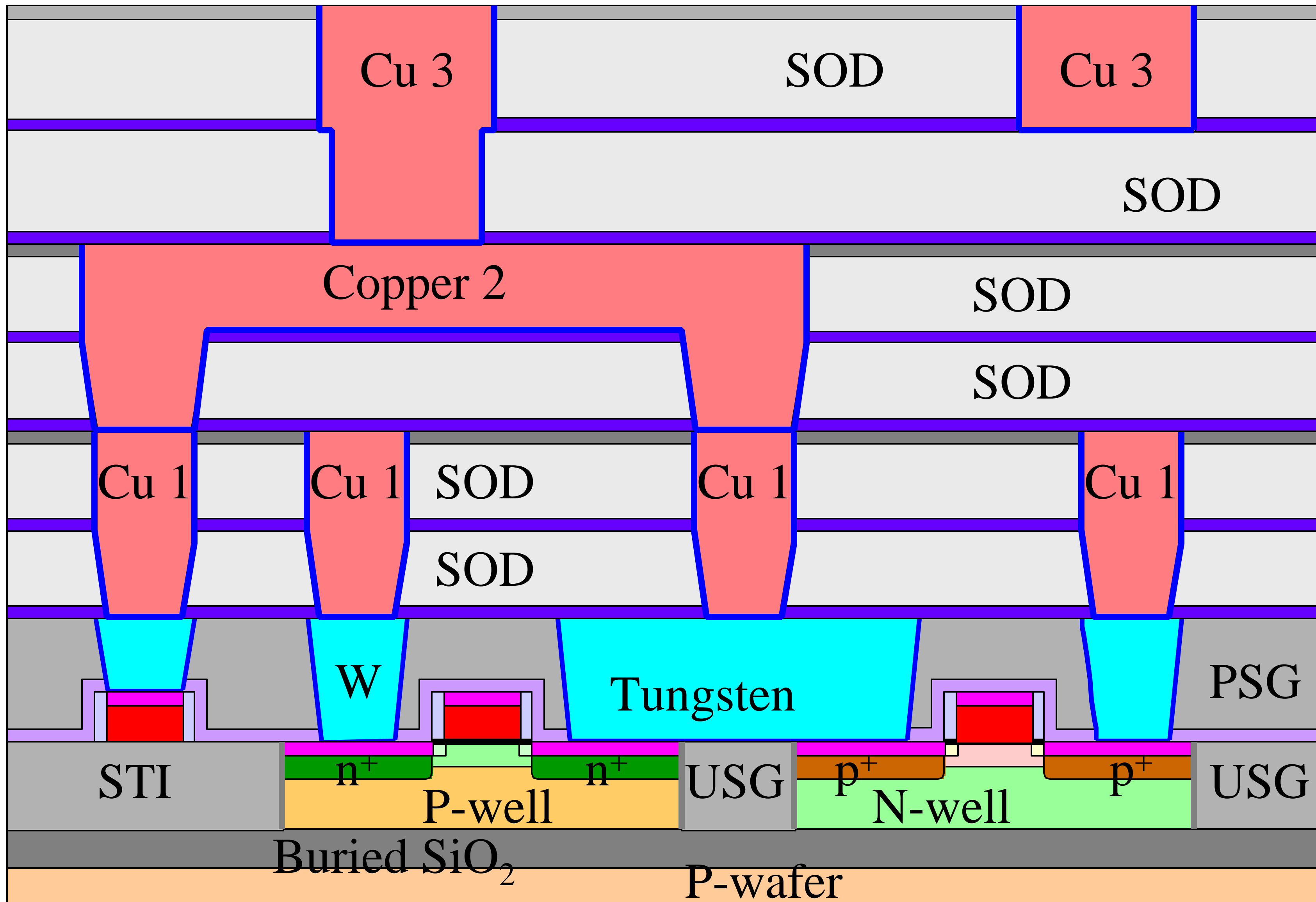
Strip Photoresist



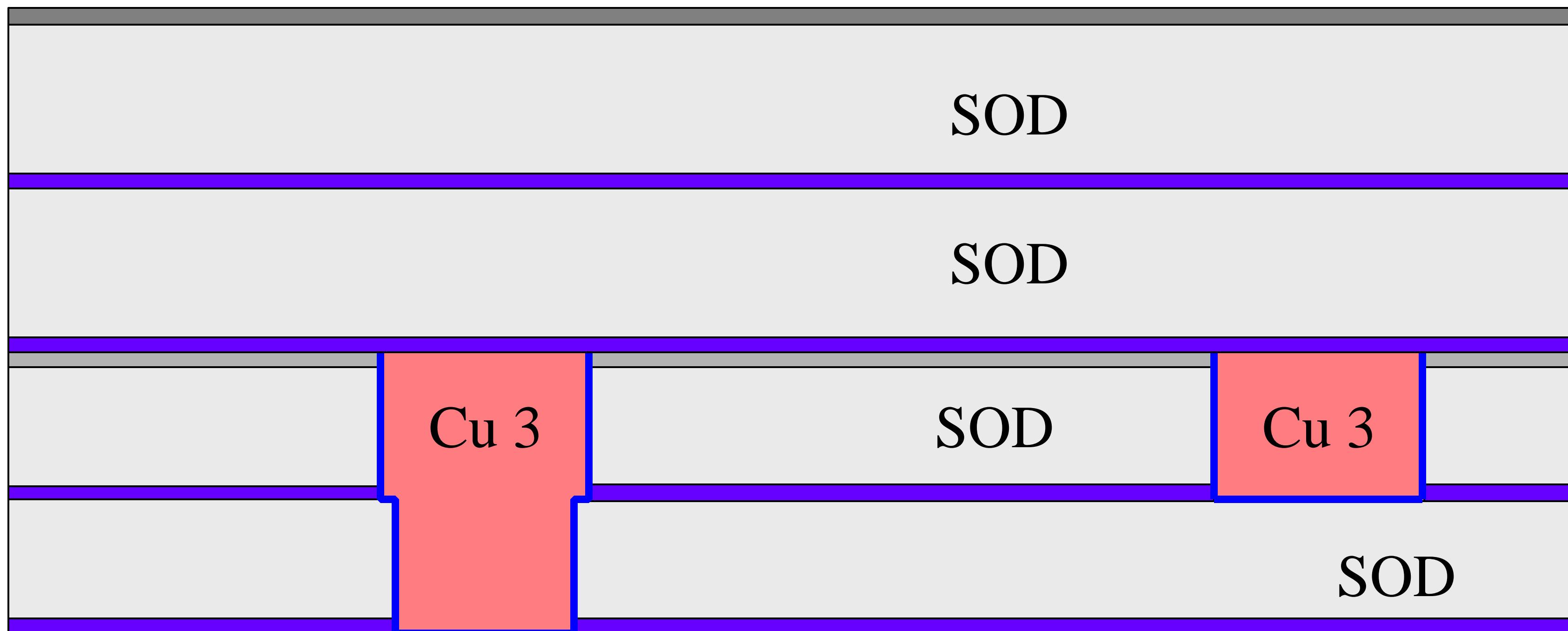
Hydrogen Plasma Clean



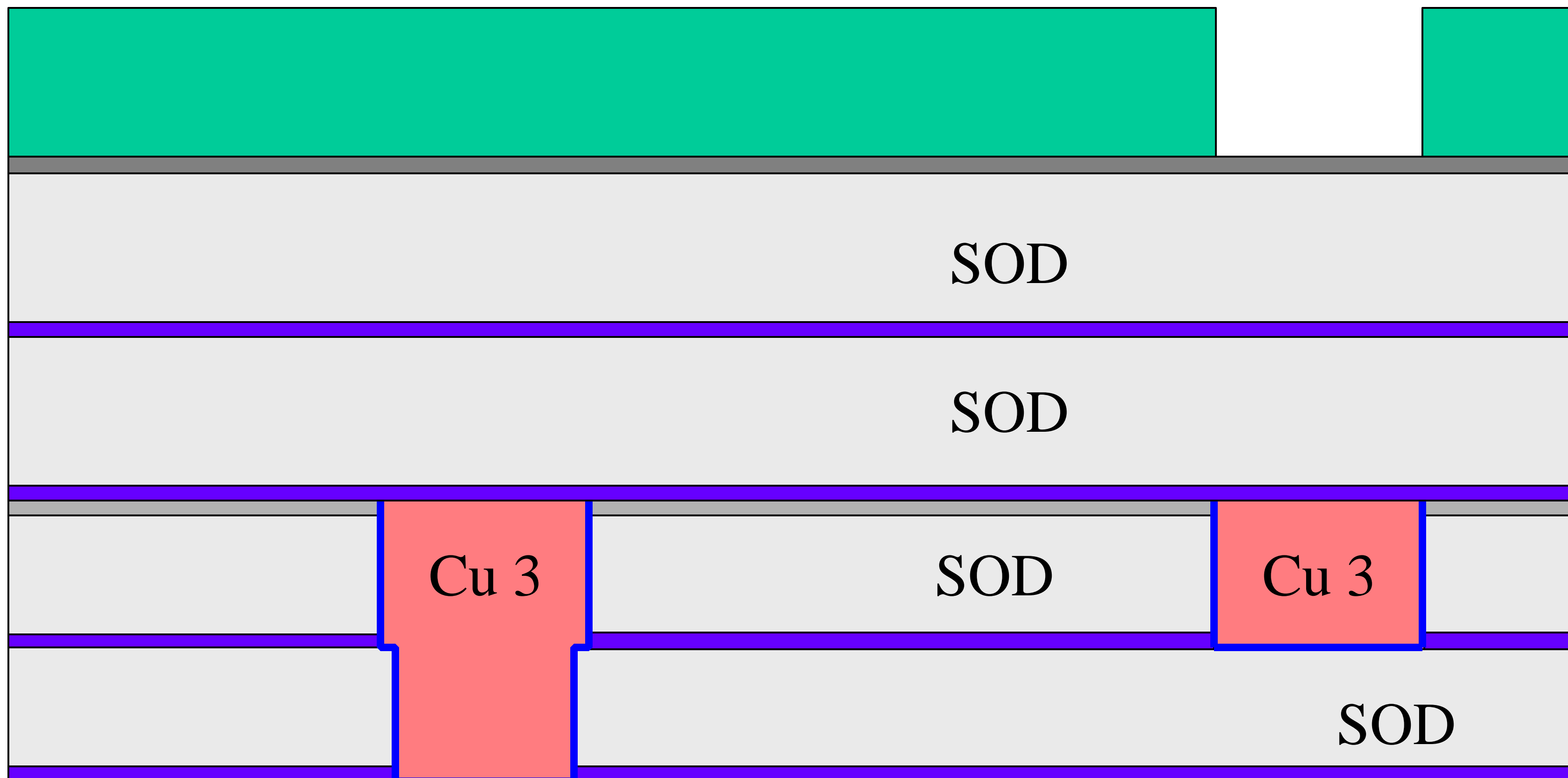
Cu, Ta, and TaN Deposition and CMP



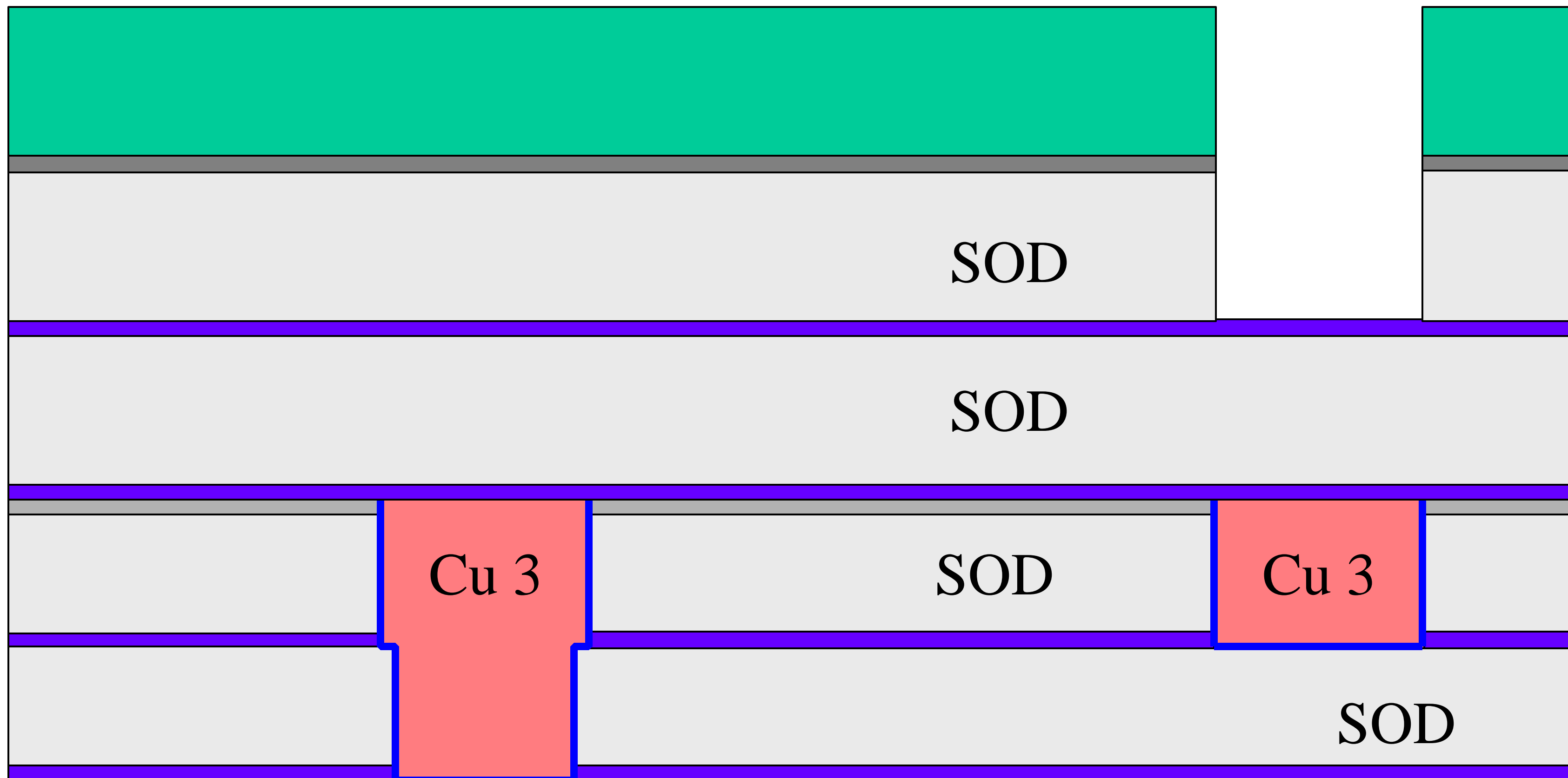
SiC, SOD, SiC, SOD, and PE-TEOS



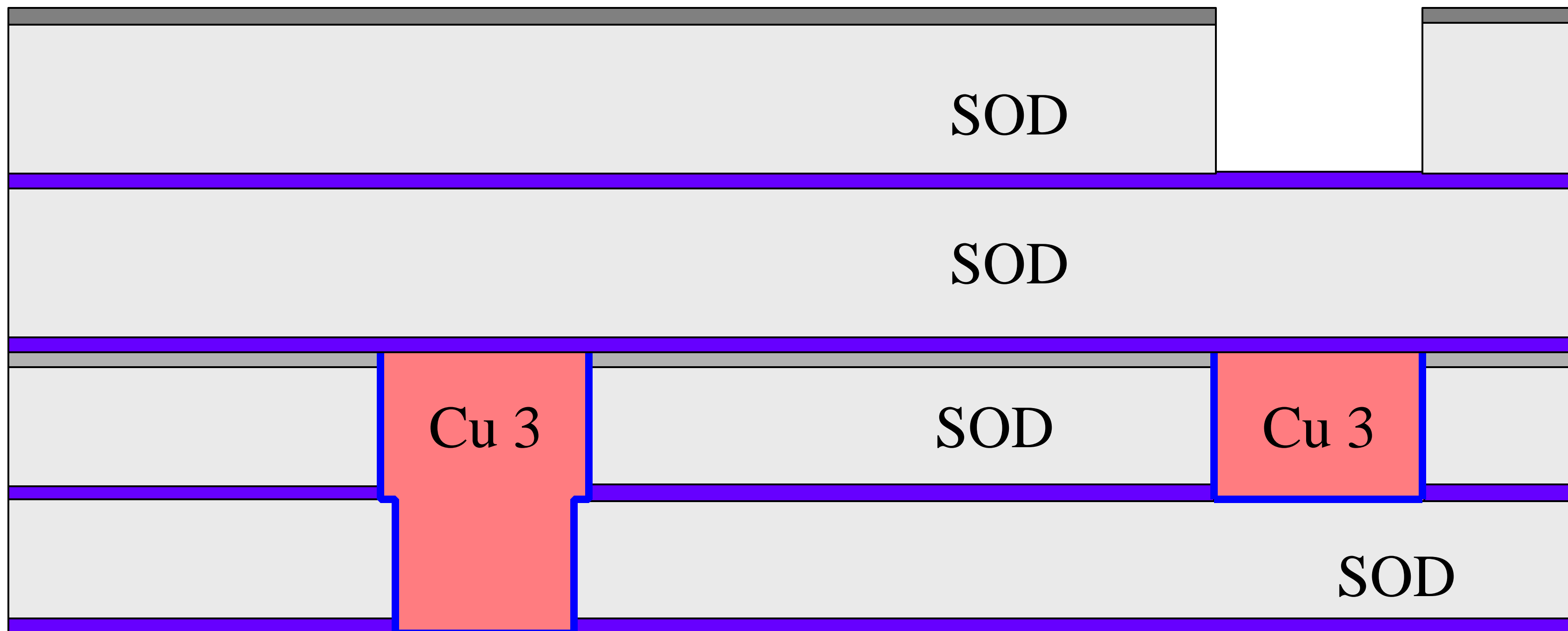
PR Coating, Alignment and Exposure, PEB, and Development



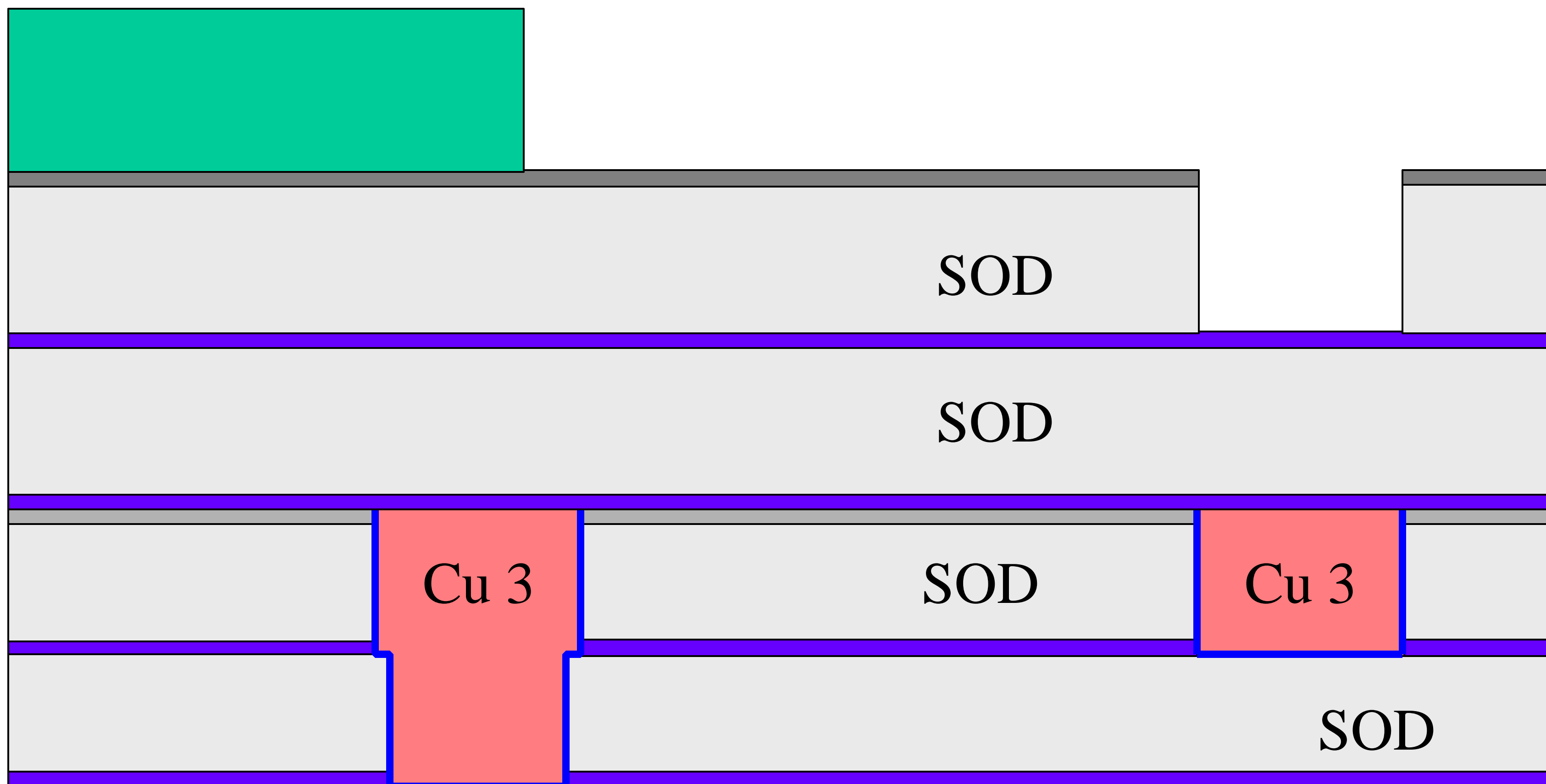
Via 4 Etch



Strip Photoresist



PR Coating, Alignment and Exposure, PEB, and Development



Etch Trench

SOD

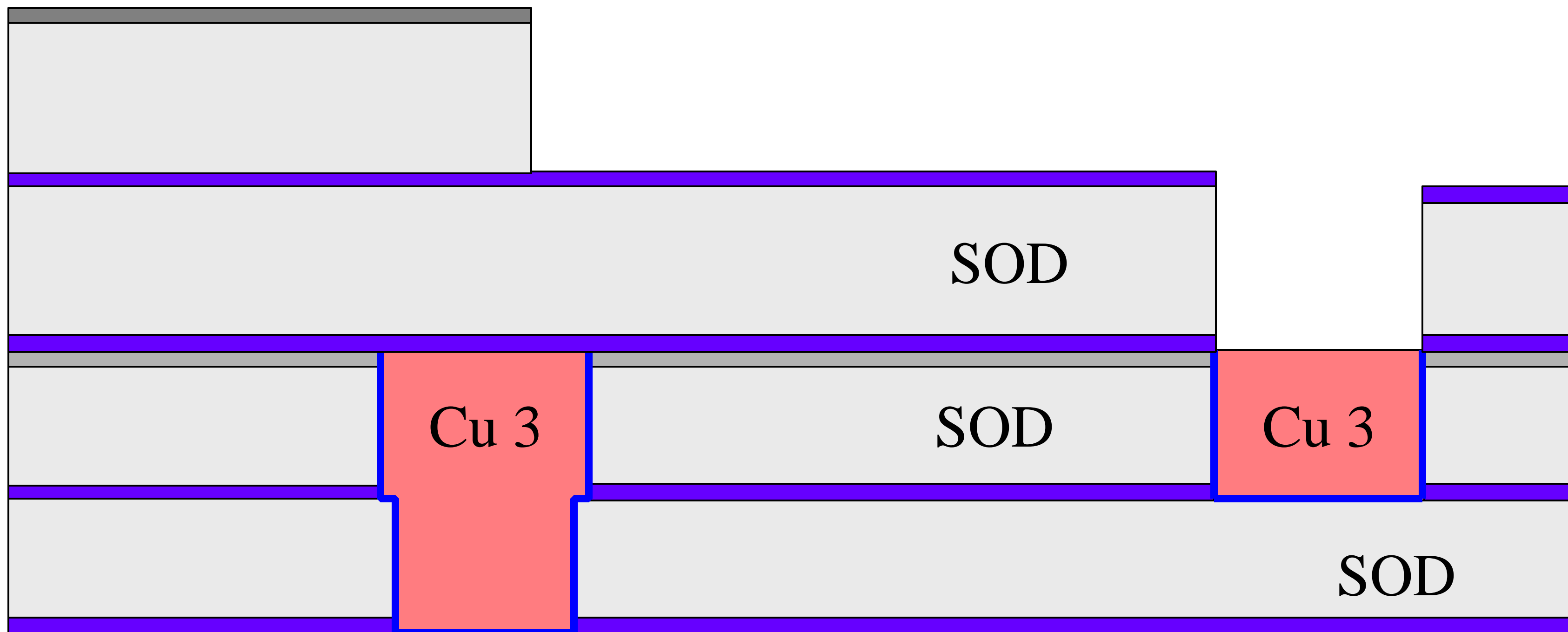
Cu 3

SOD

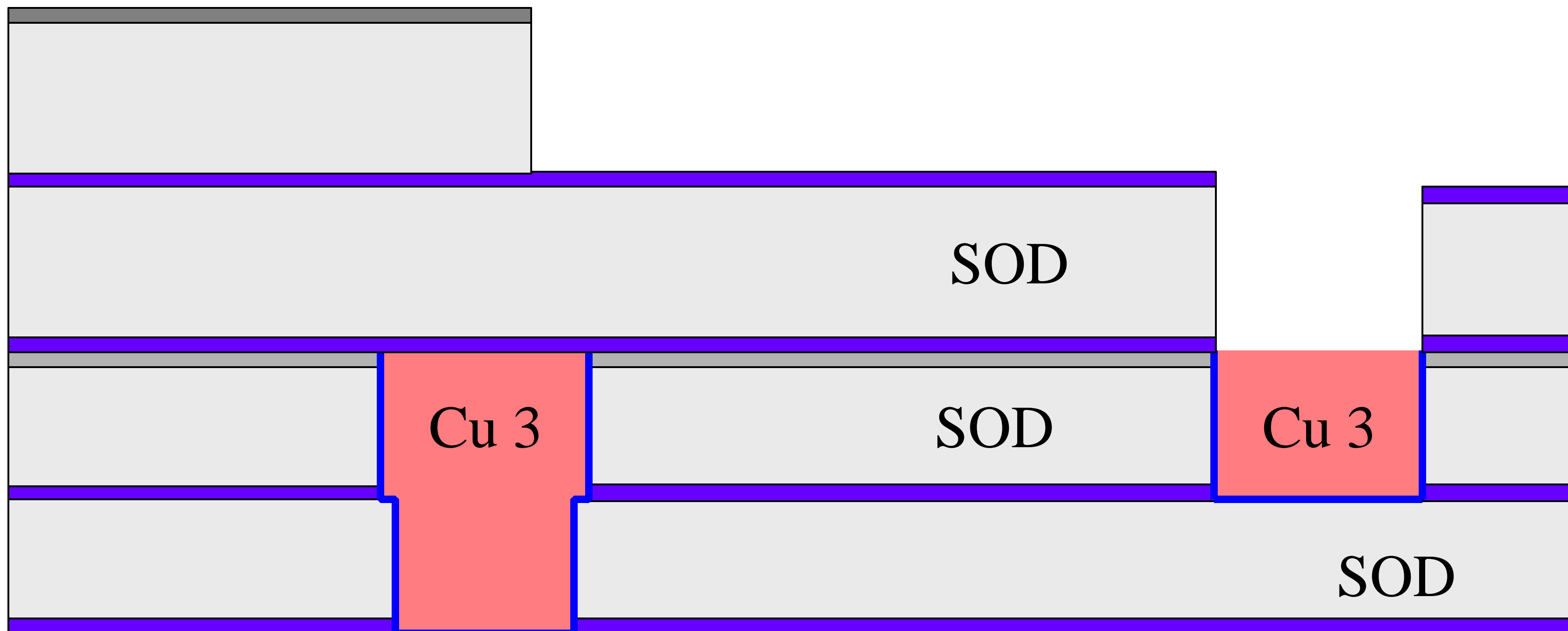
Cu 3

SOD

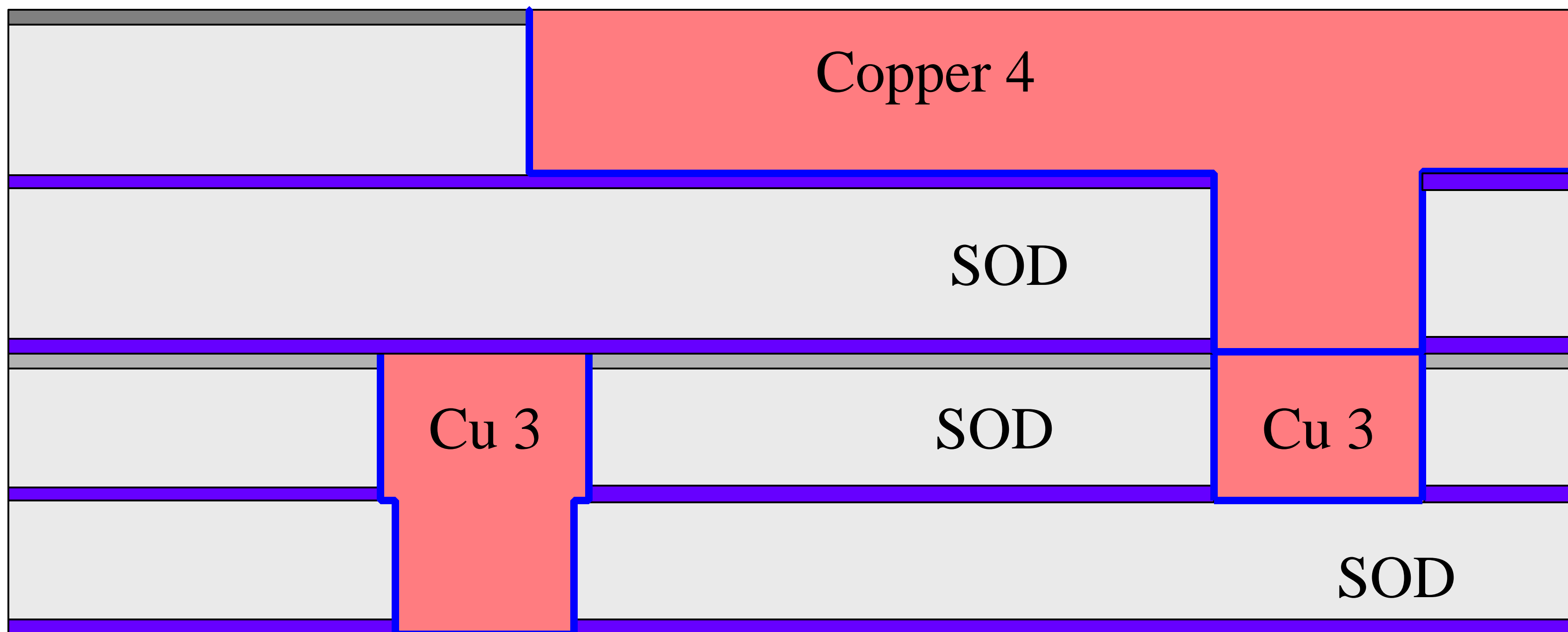
Strip Photoresist



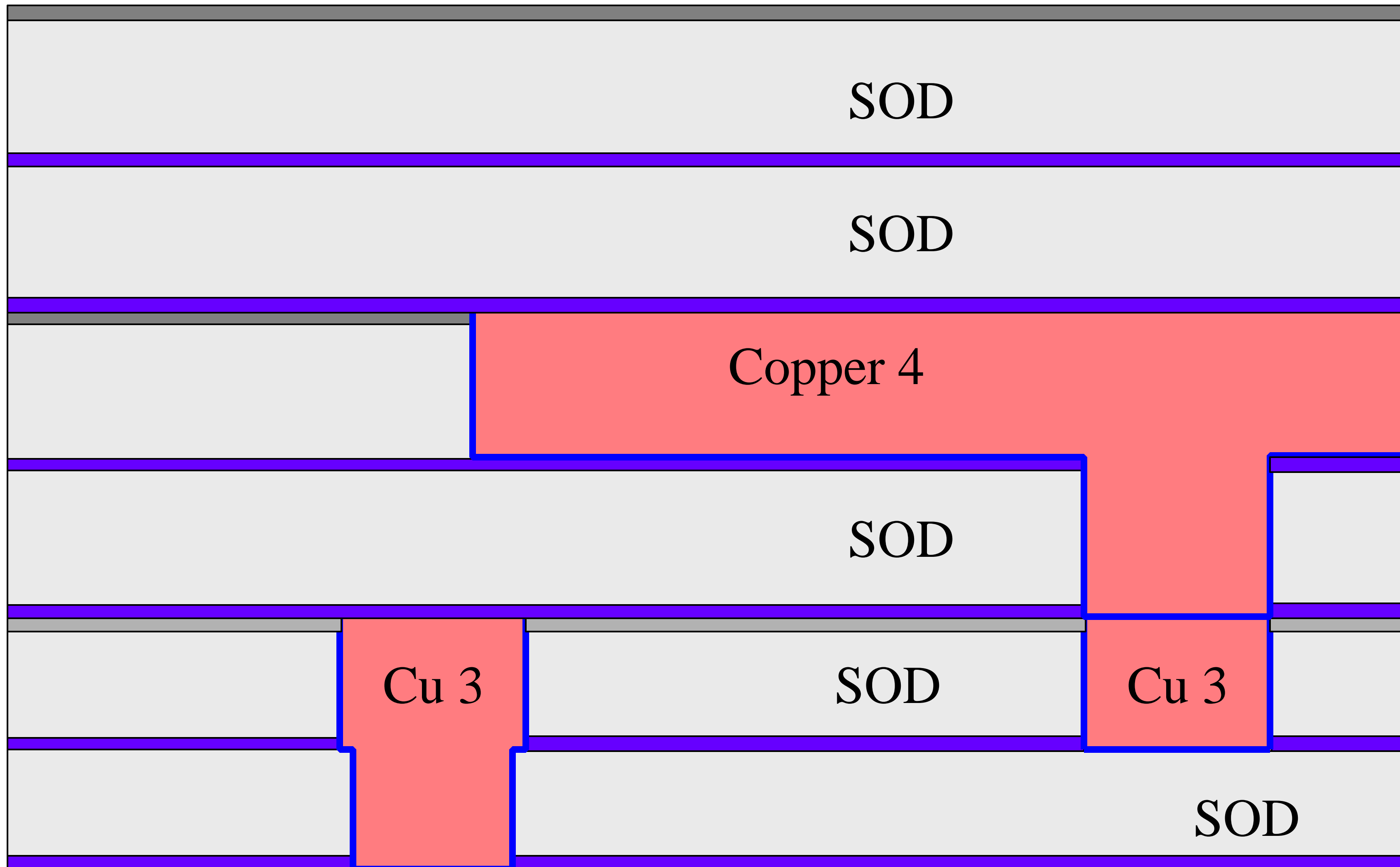
Hydrogen Plasma Clean



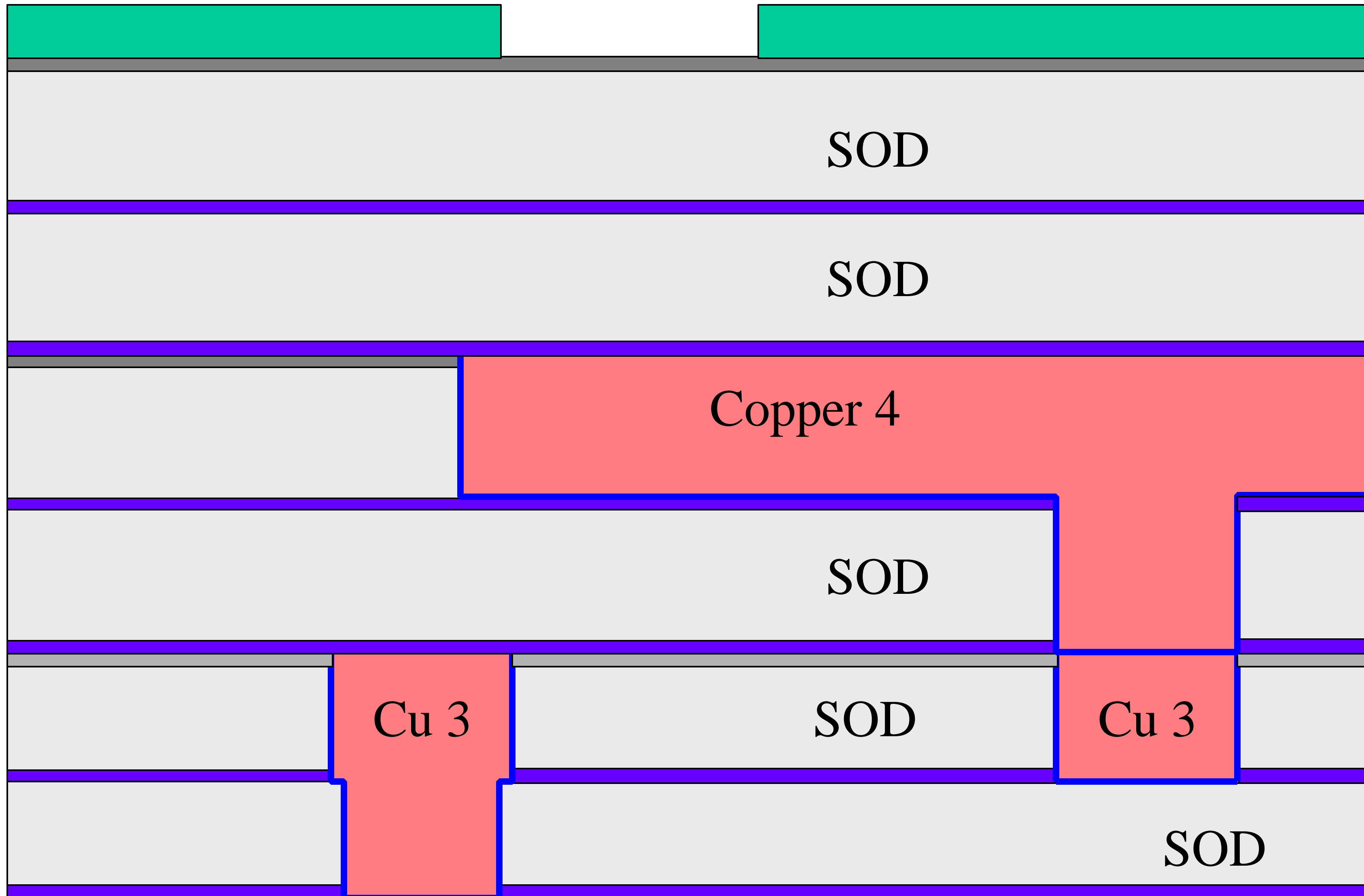
Cu, Ta, and TaN Deposition and CMP



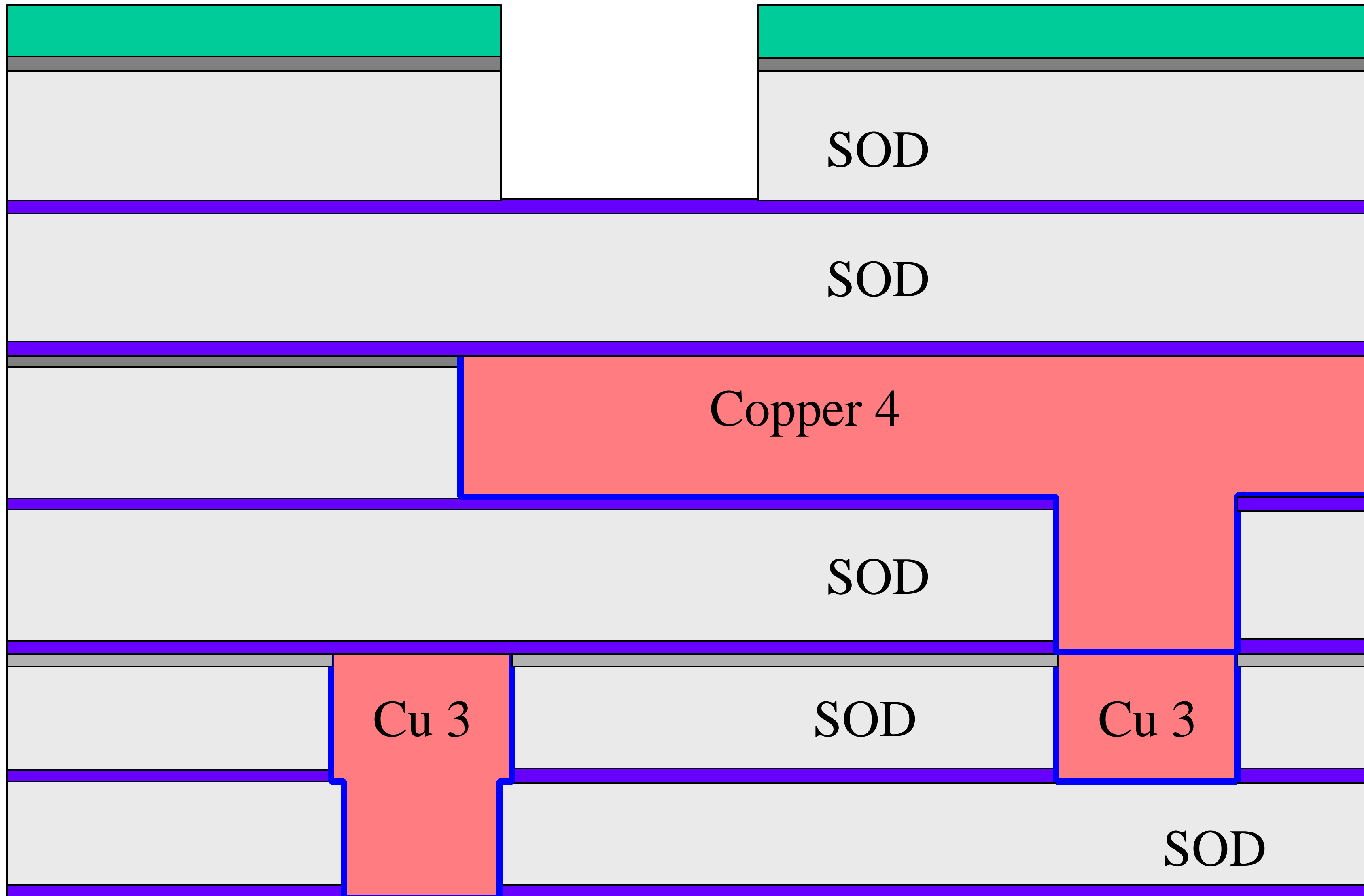
SiC, SOD, SiC, SOD, and PE-TEOS



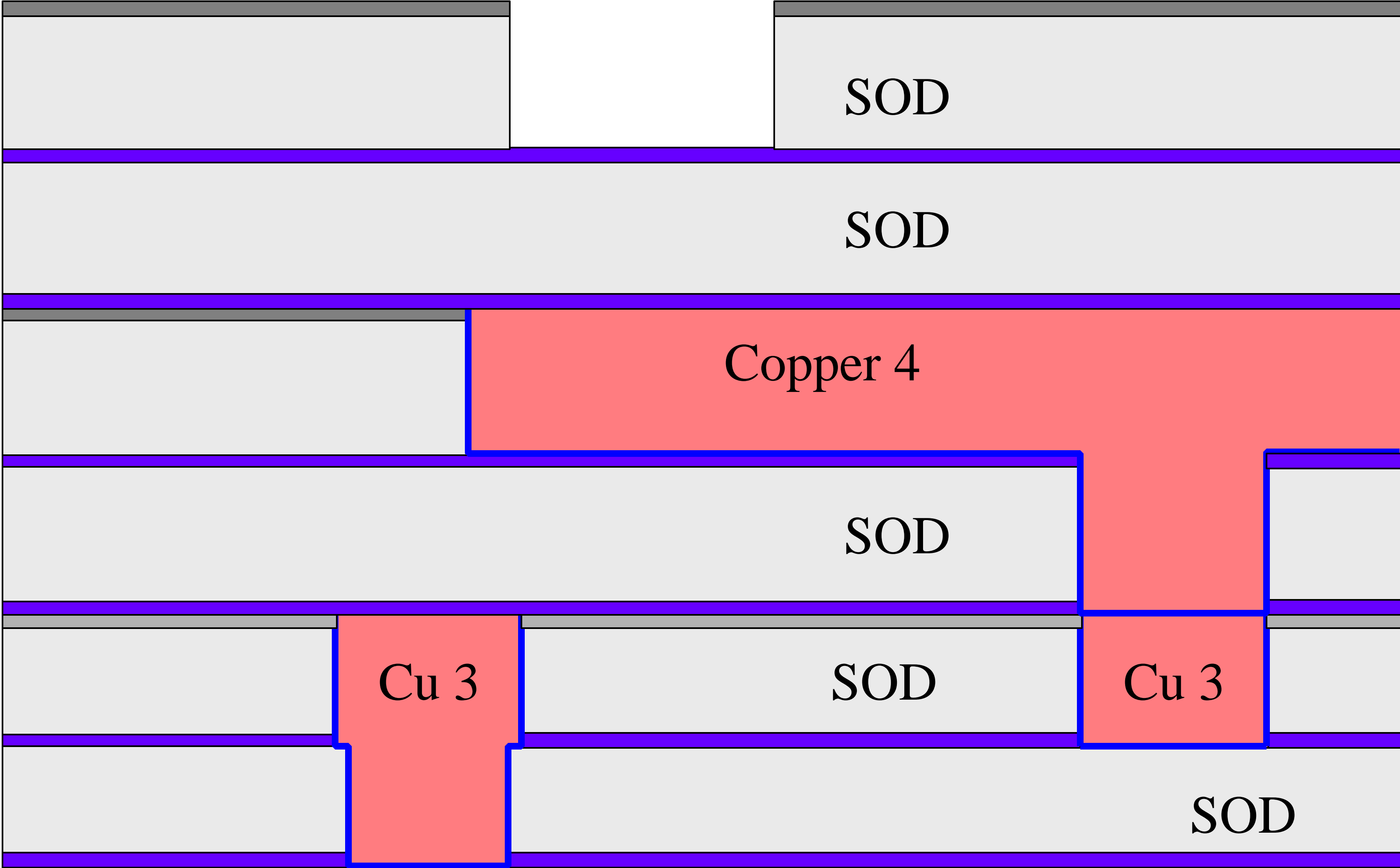
PR Coating, A&E, PEB, and Develop



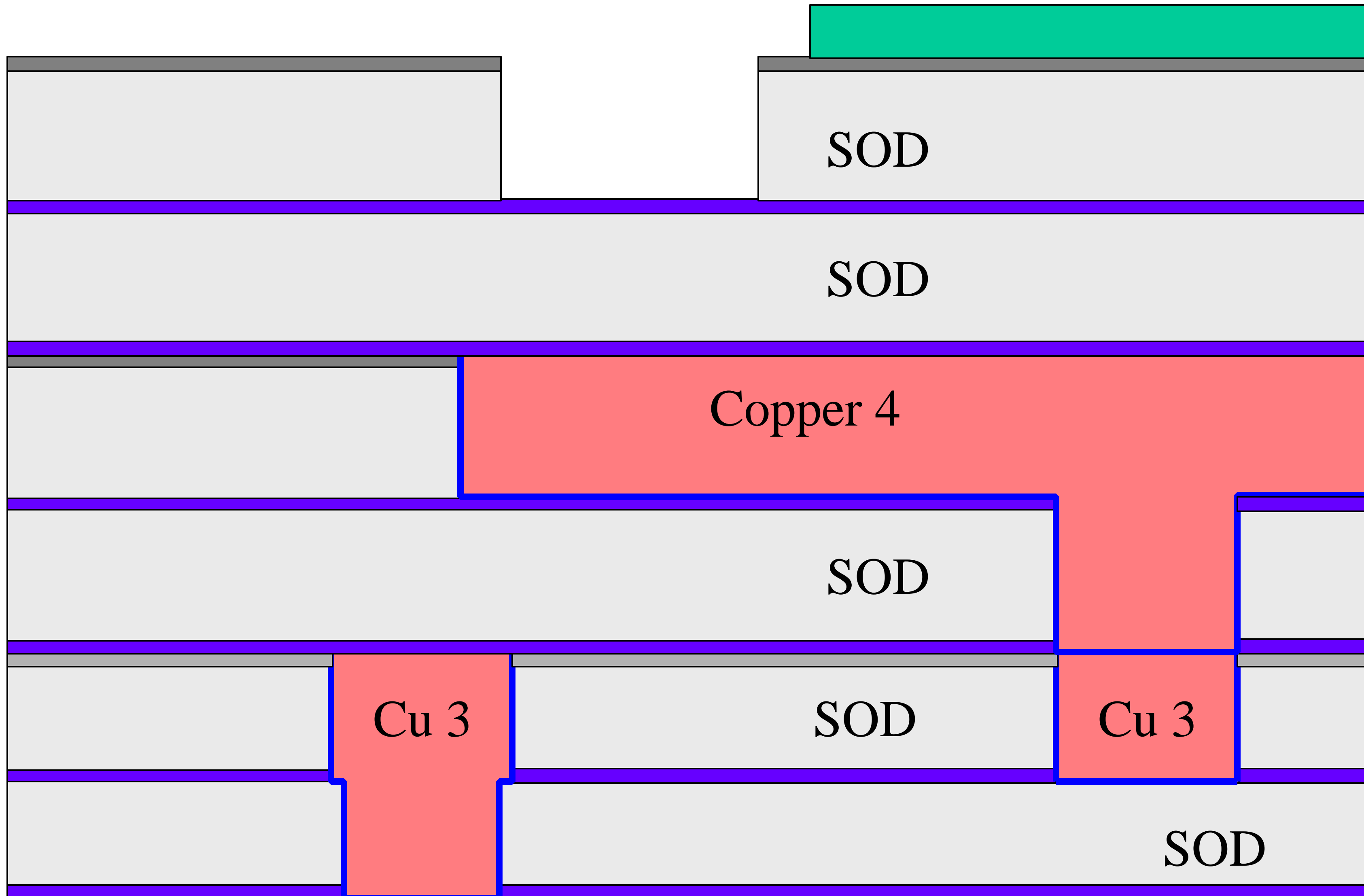
Etch Via5



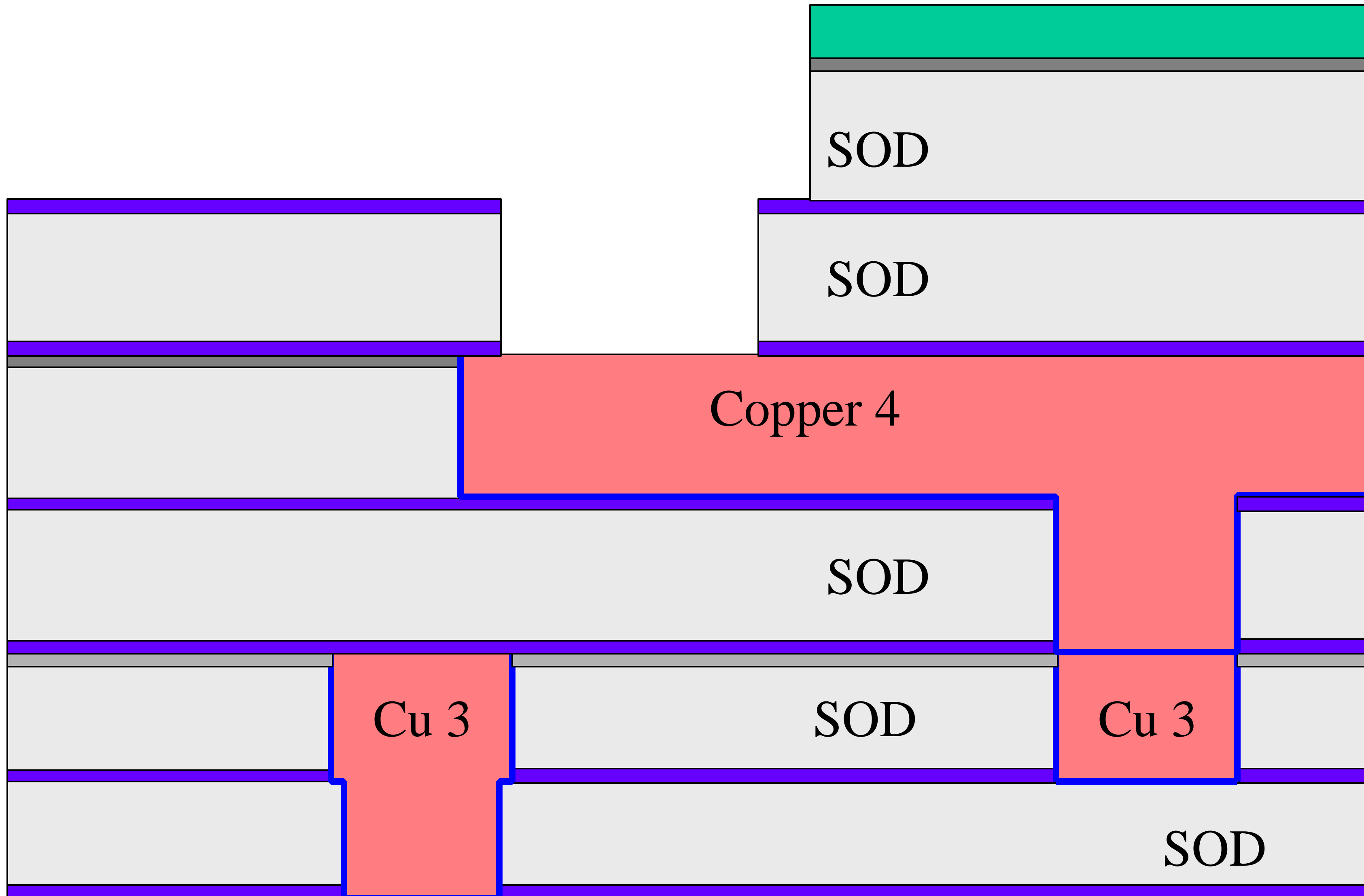
Strip Photoresist



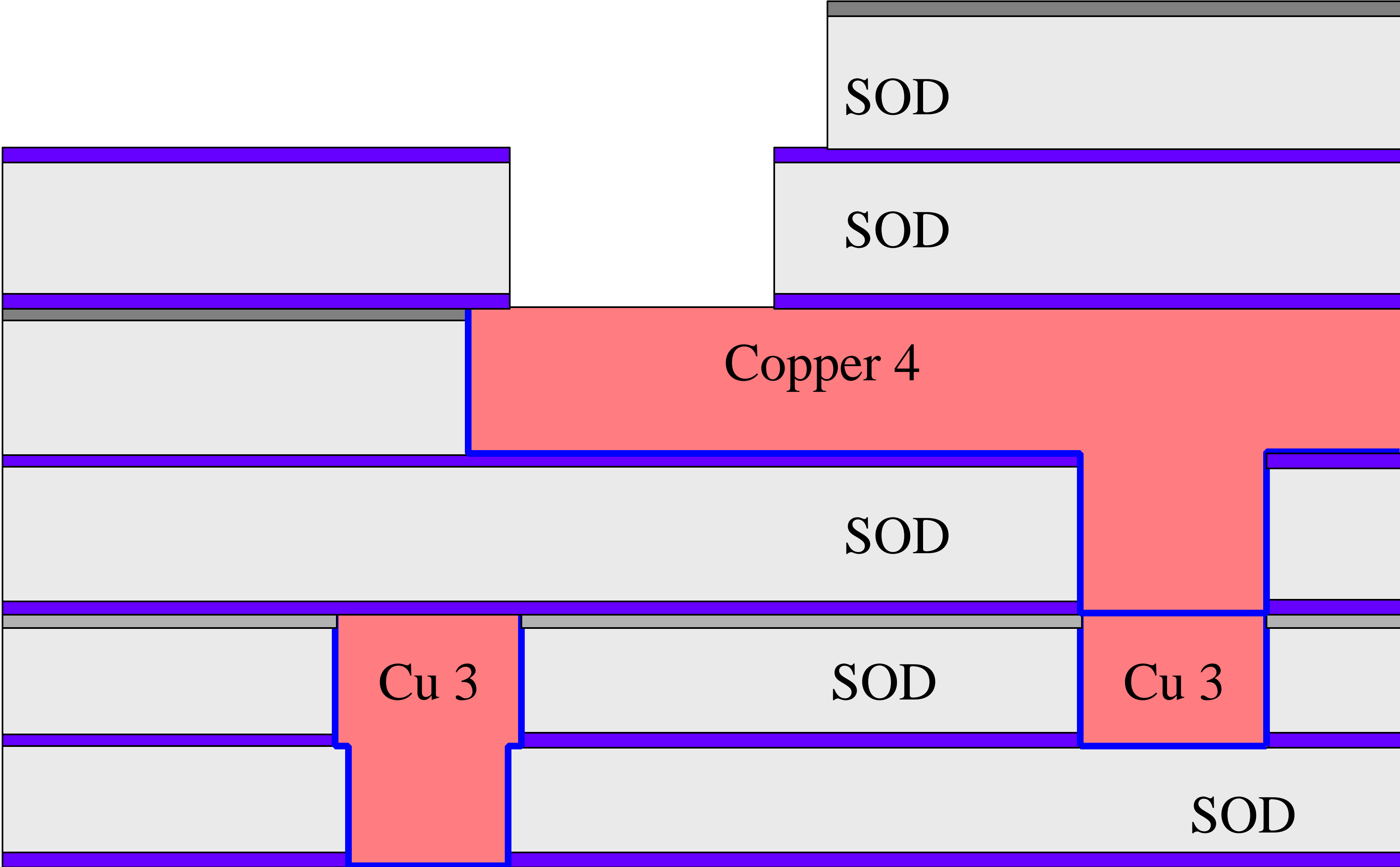
PR Coating, A&E, PEB, and Develop



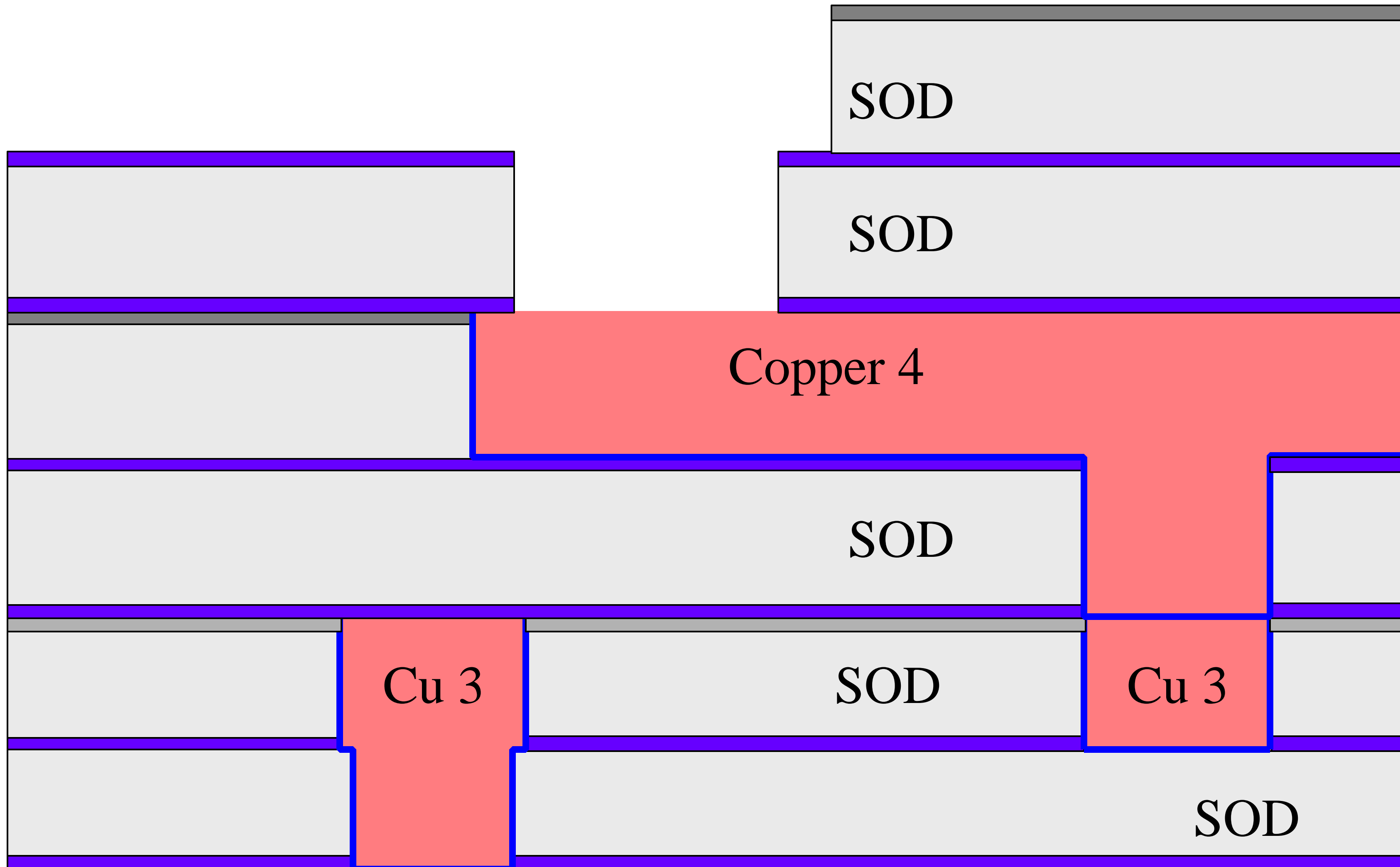
Dielectric Etch



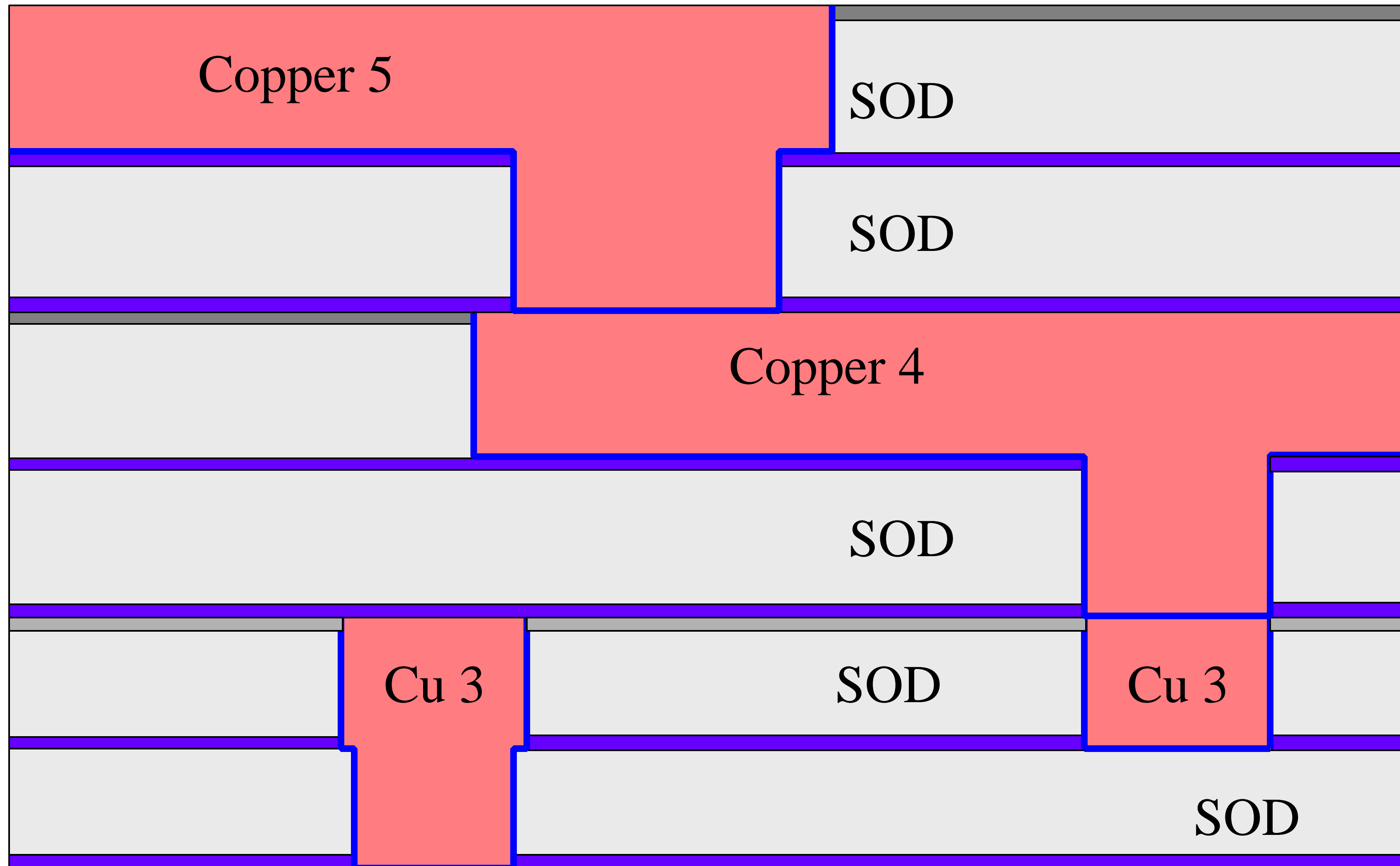
Strip Photoresist



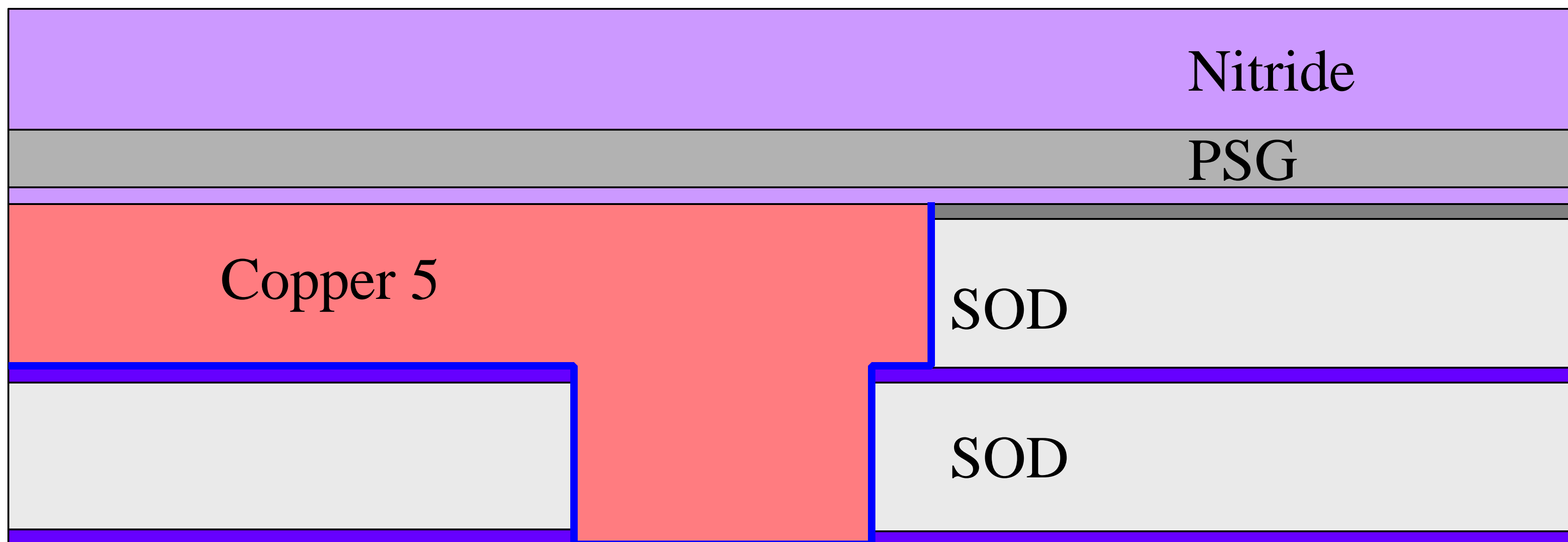
Hydrogen Plasma Clean



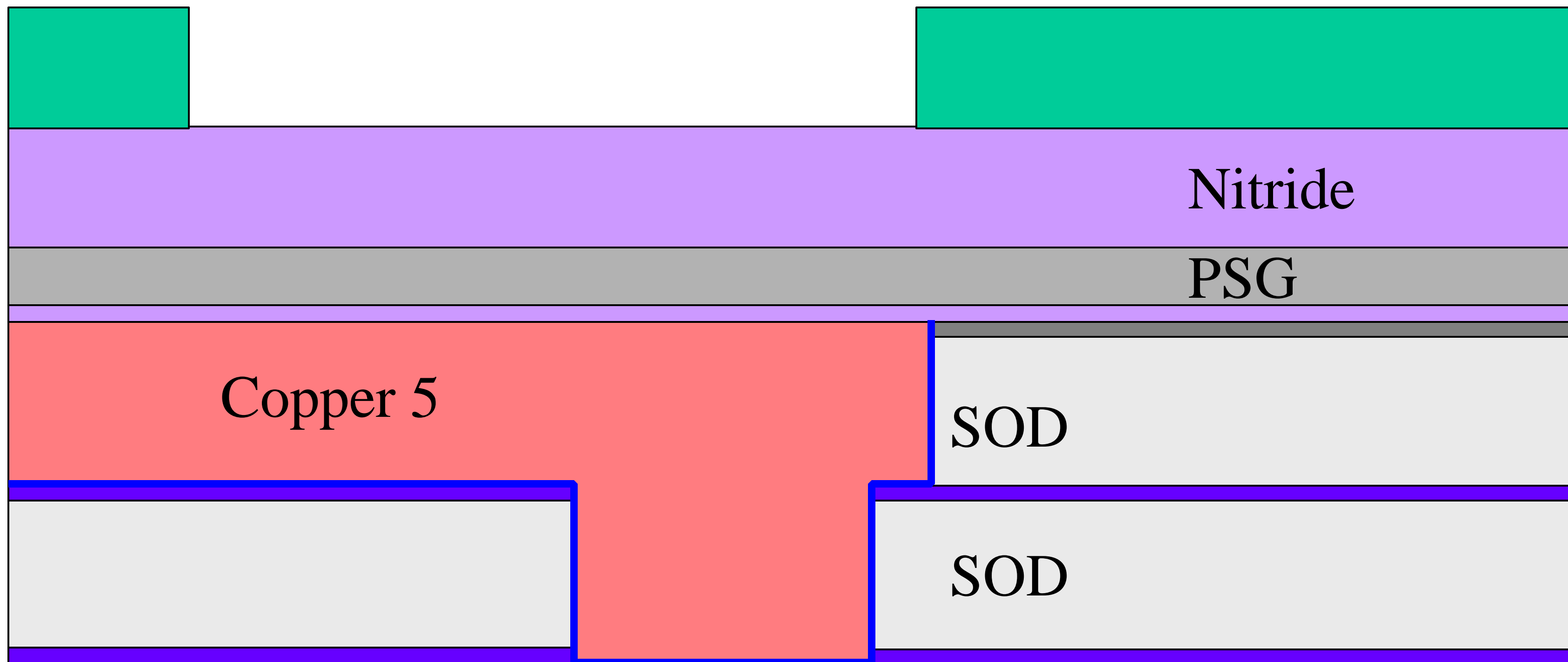
Cu, Ta, and TaN Deposition and CMP



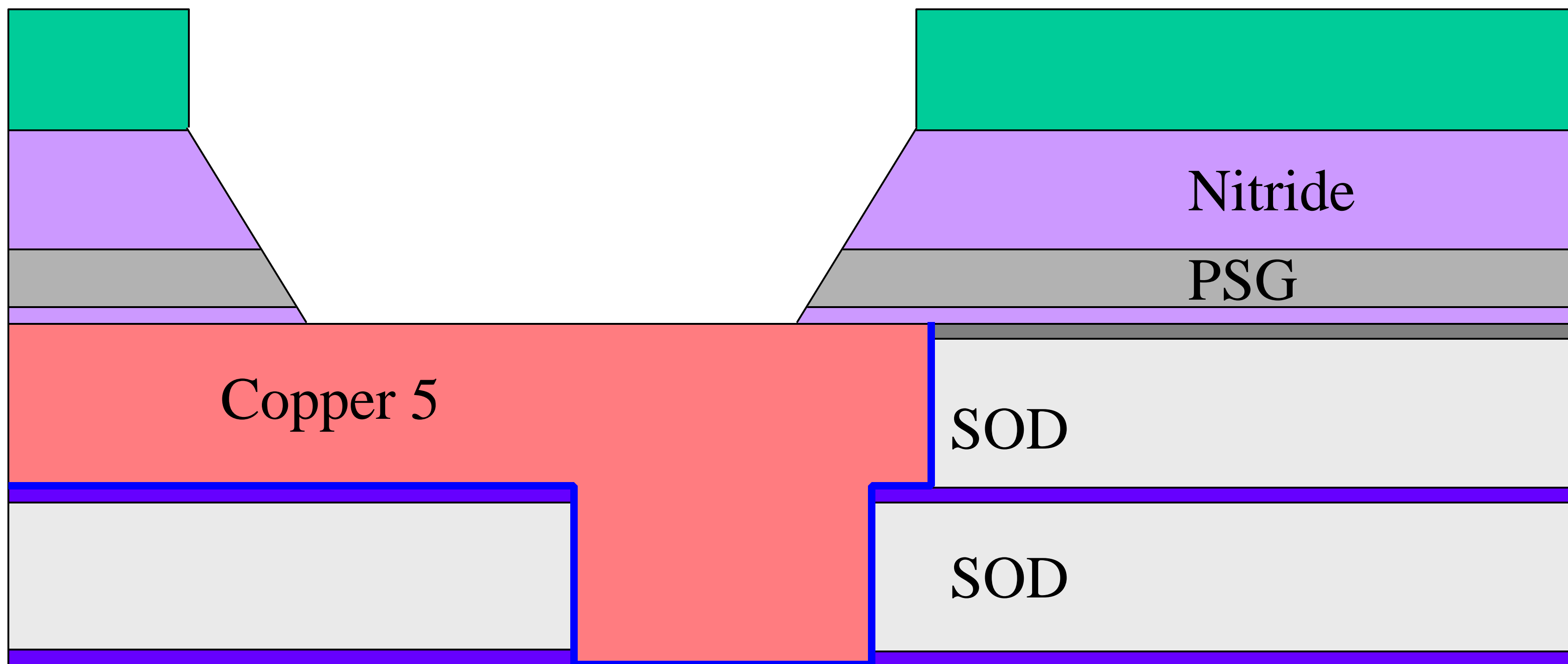
PECVD Passivation Layers: Nitride, PSG, and Nitride



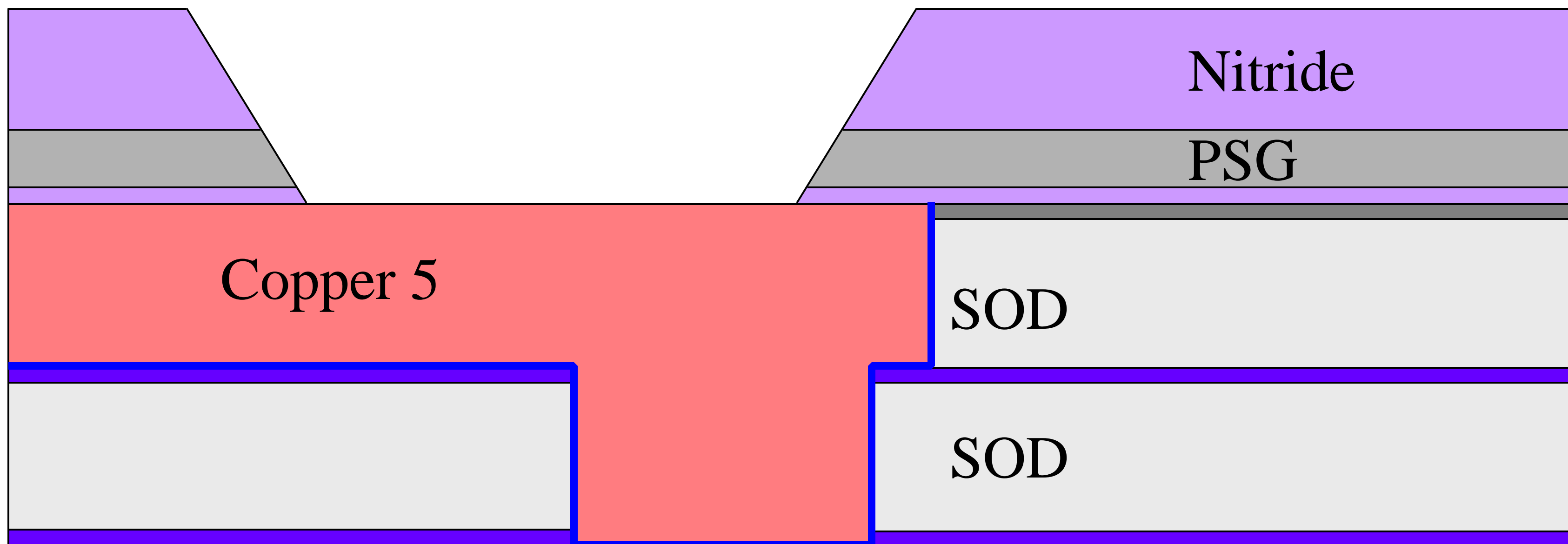
PR Coating, A&E, PEB, and Develop



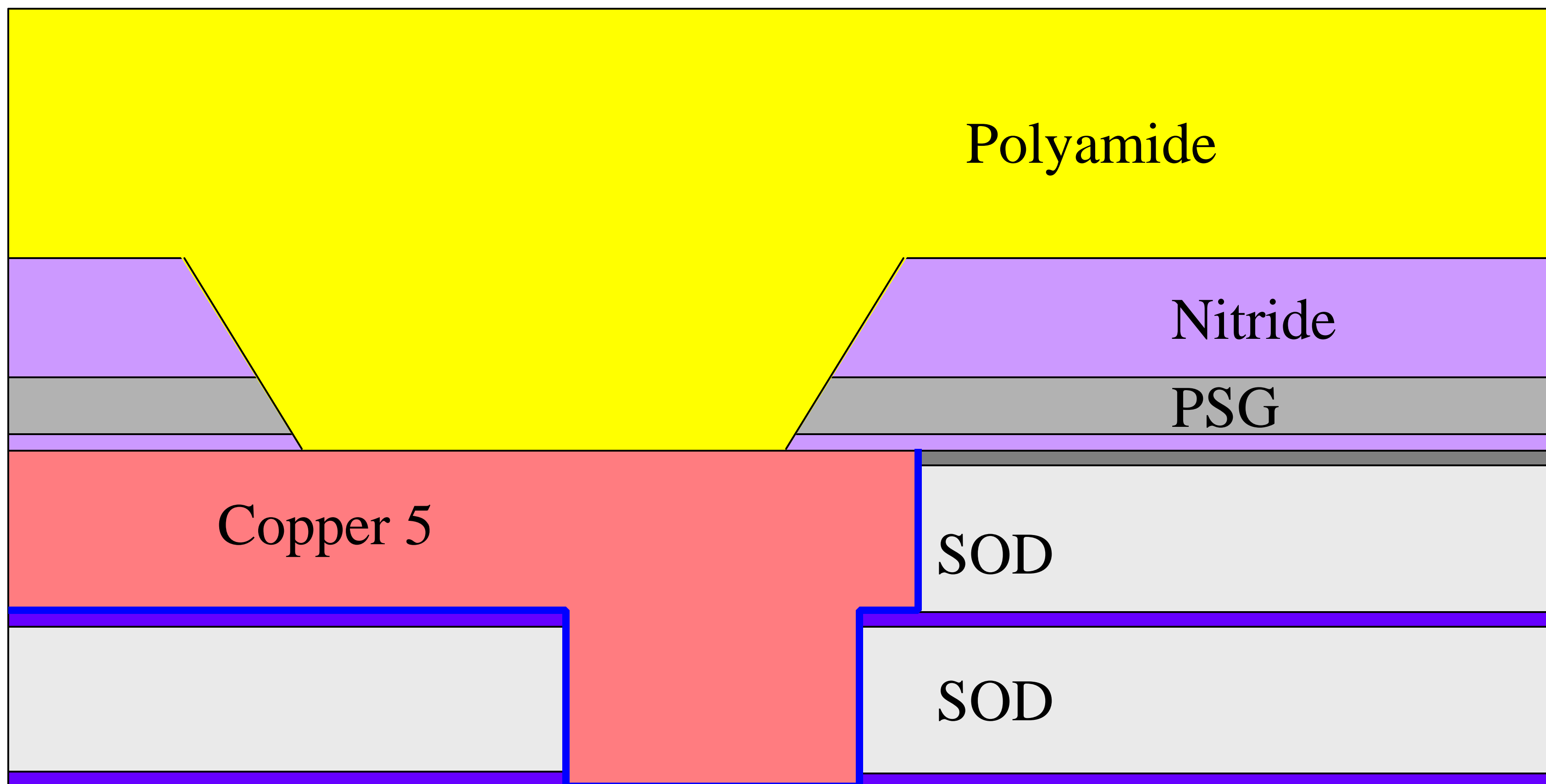
Etch Passivation Layers



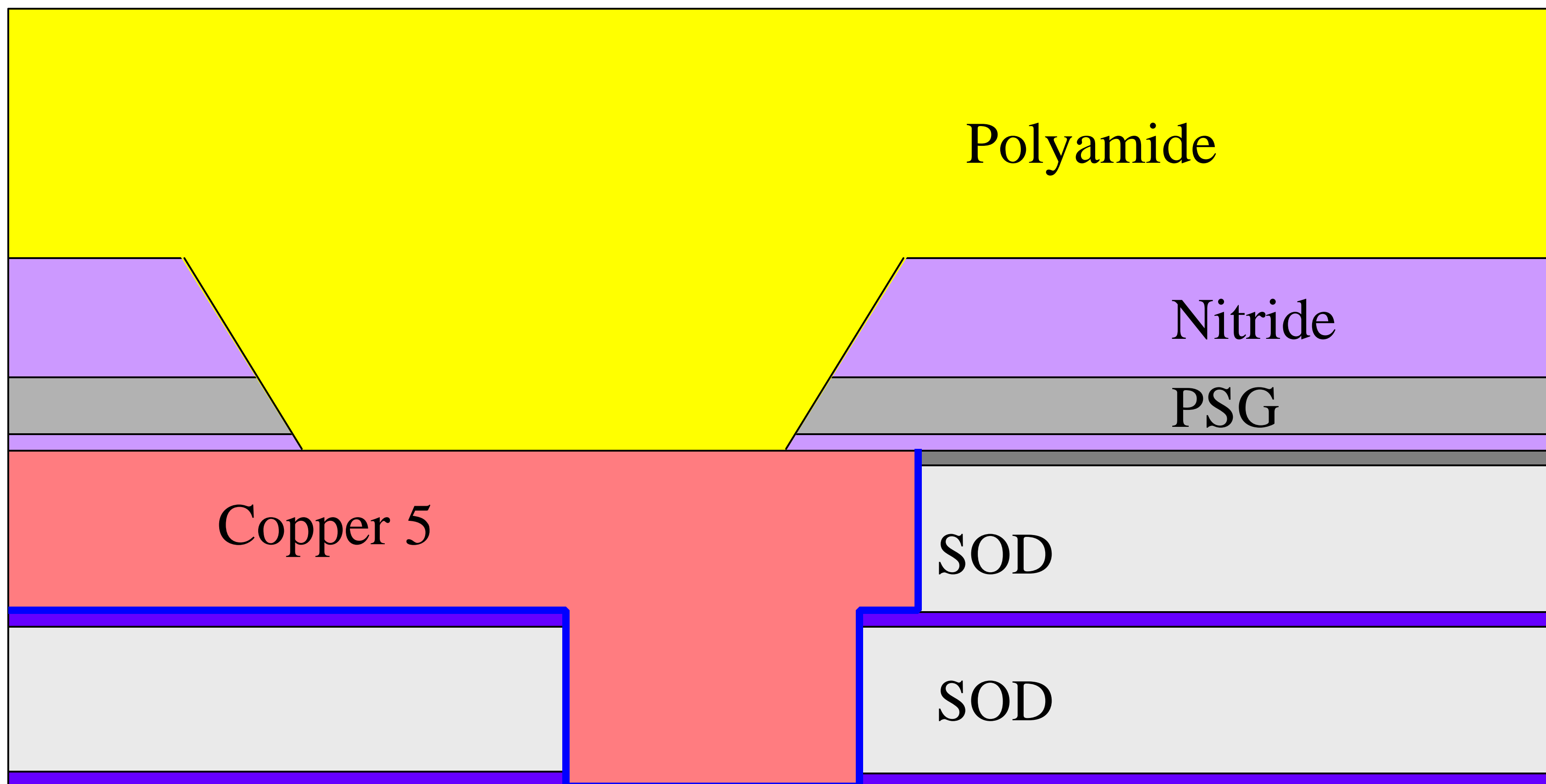
Strip Photoresist



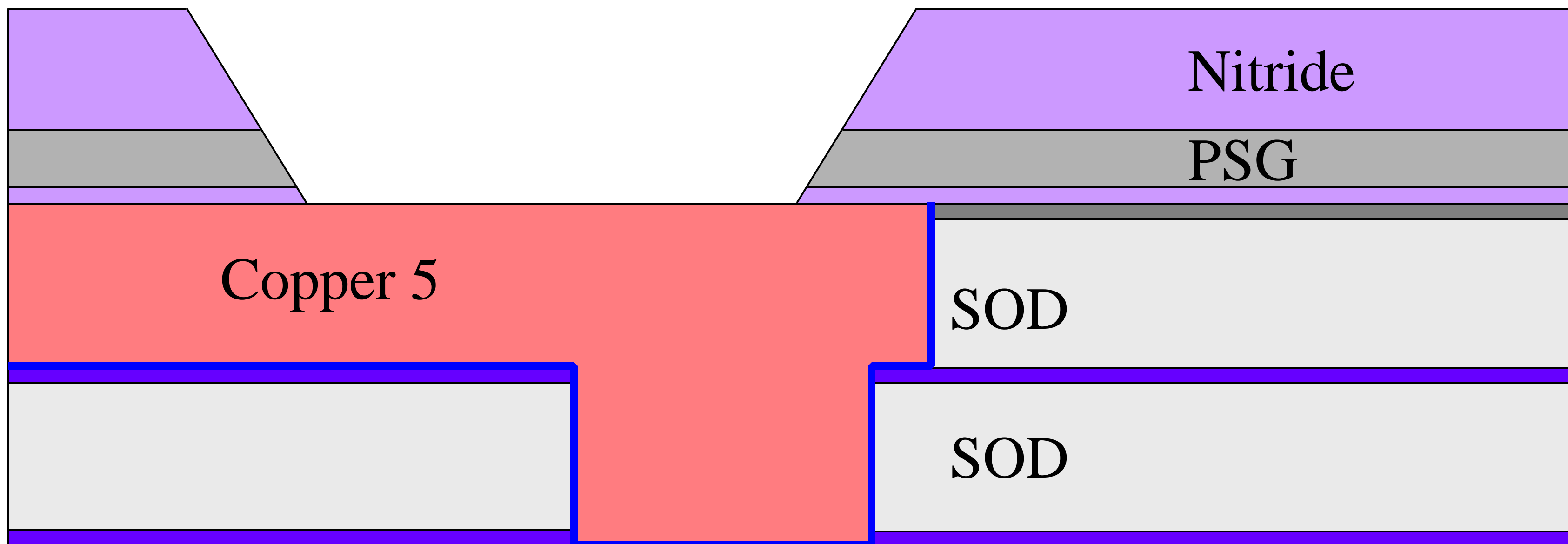
Polyamide Coating



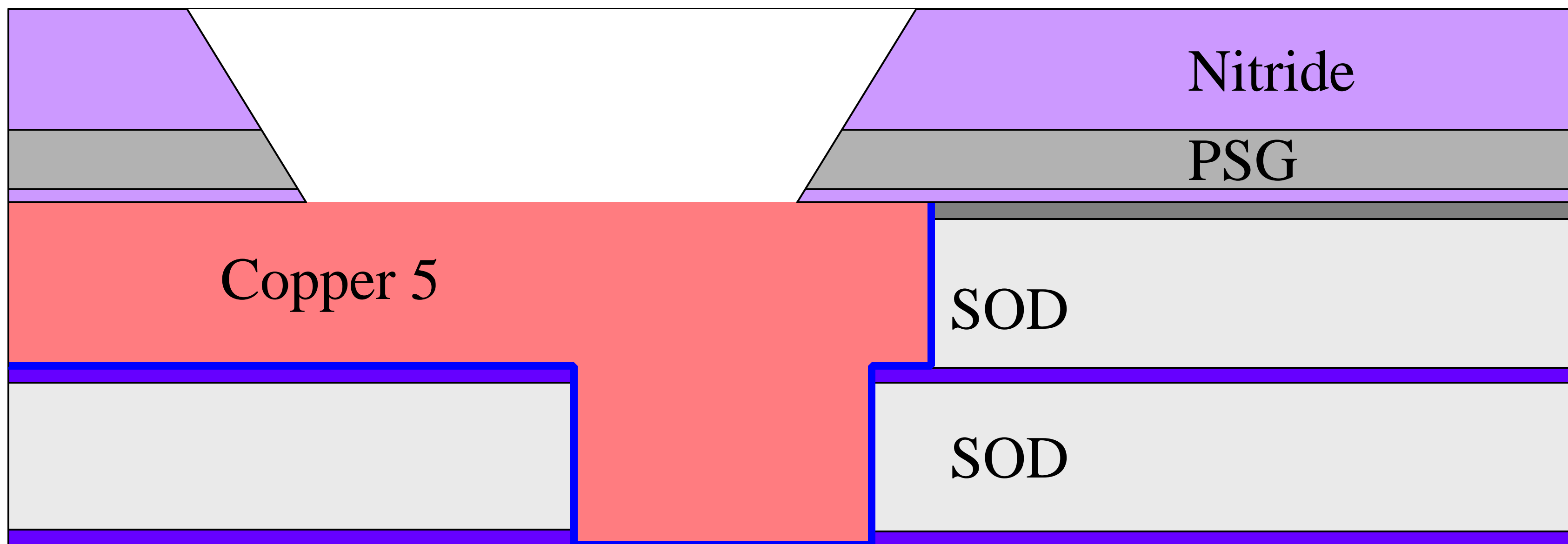
Ship to Test and Package



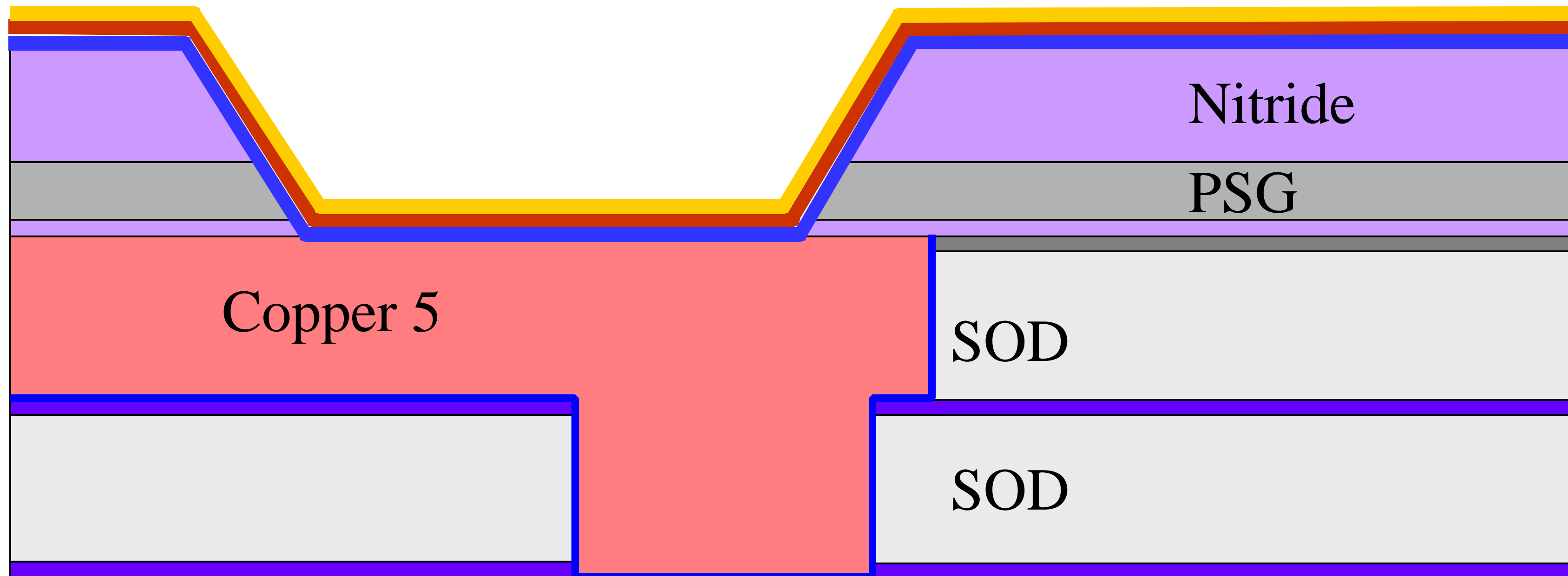
Strip Polyamide



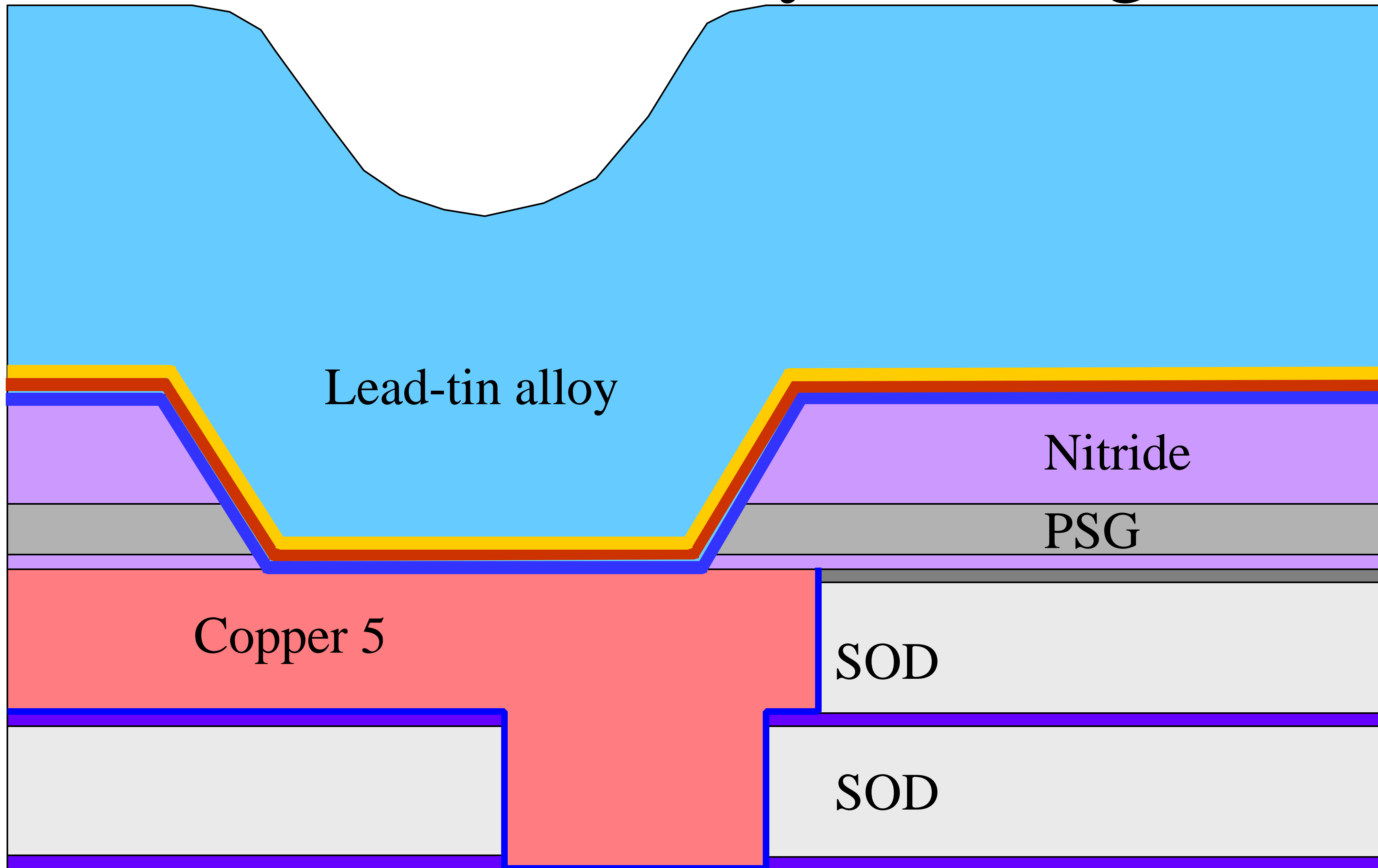
Argon Sputtering Etch



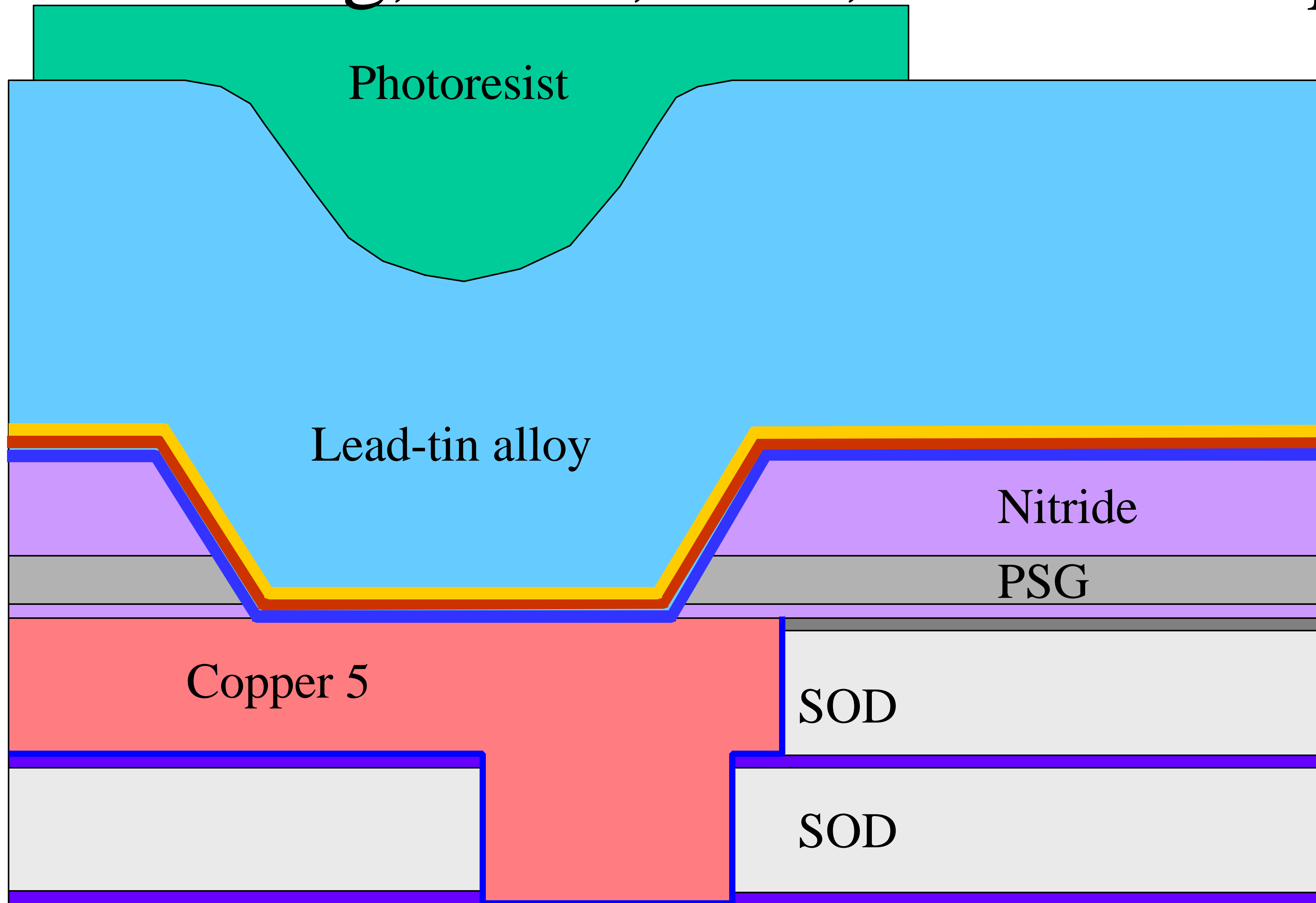
Cr, Cu, and Au Liner Coating



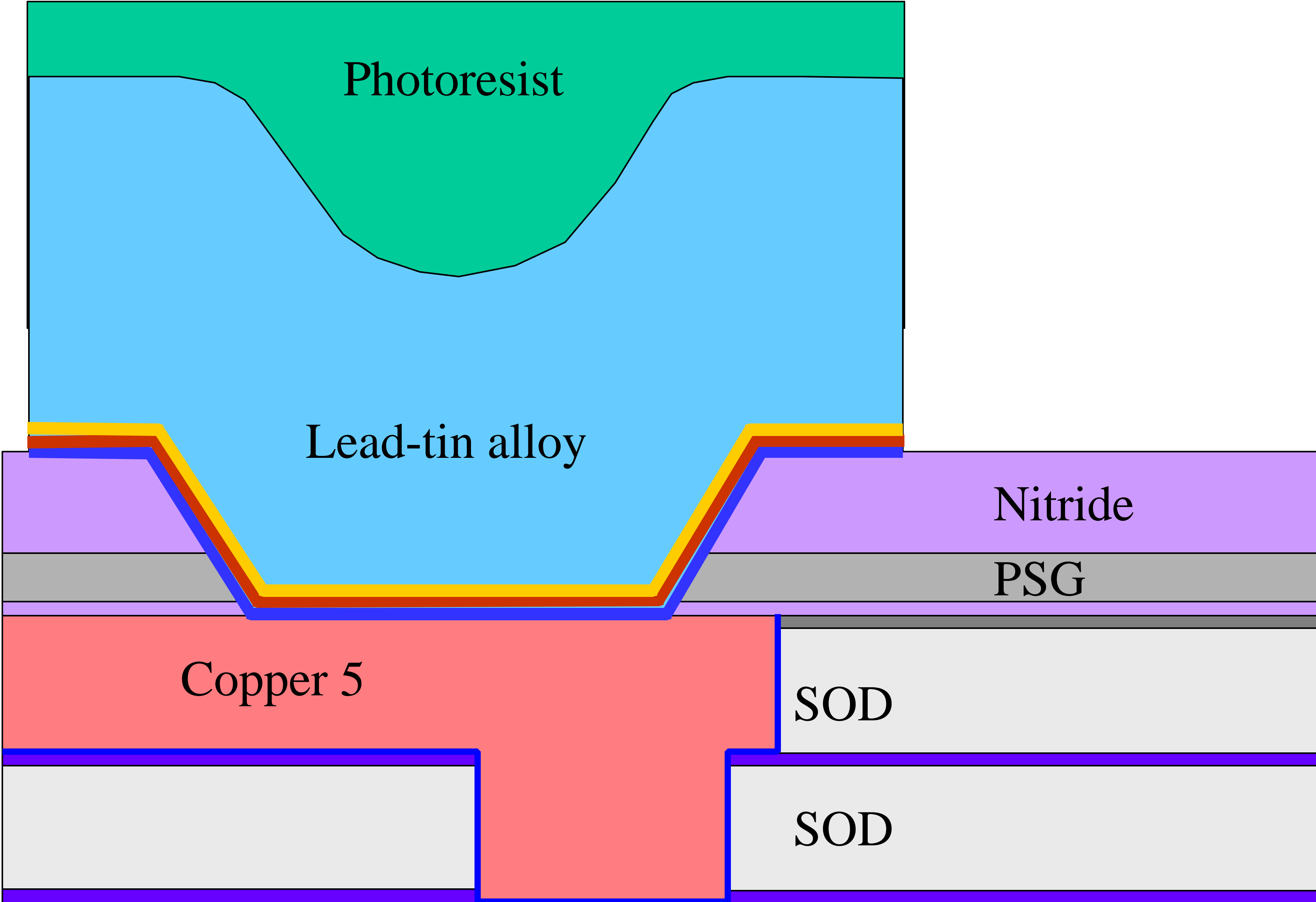
Lead-Tin Alloy Coating



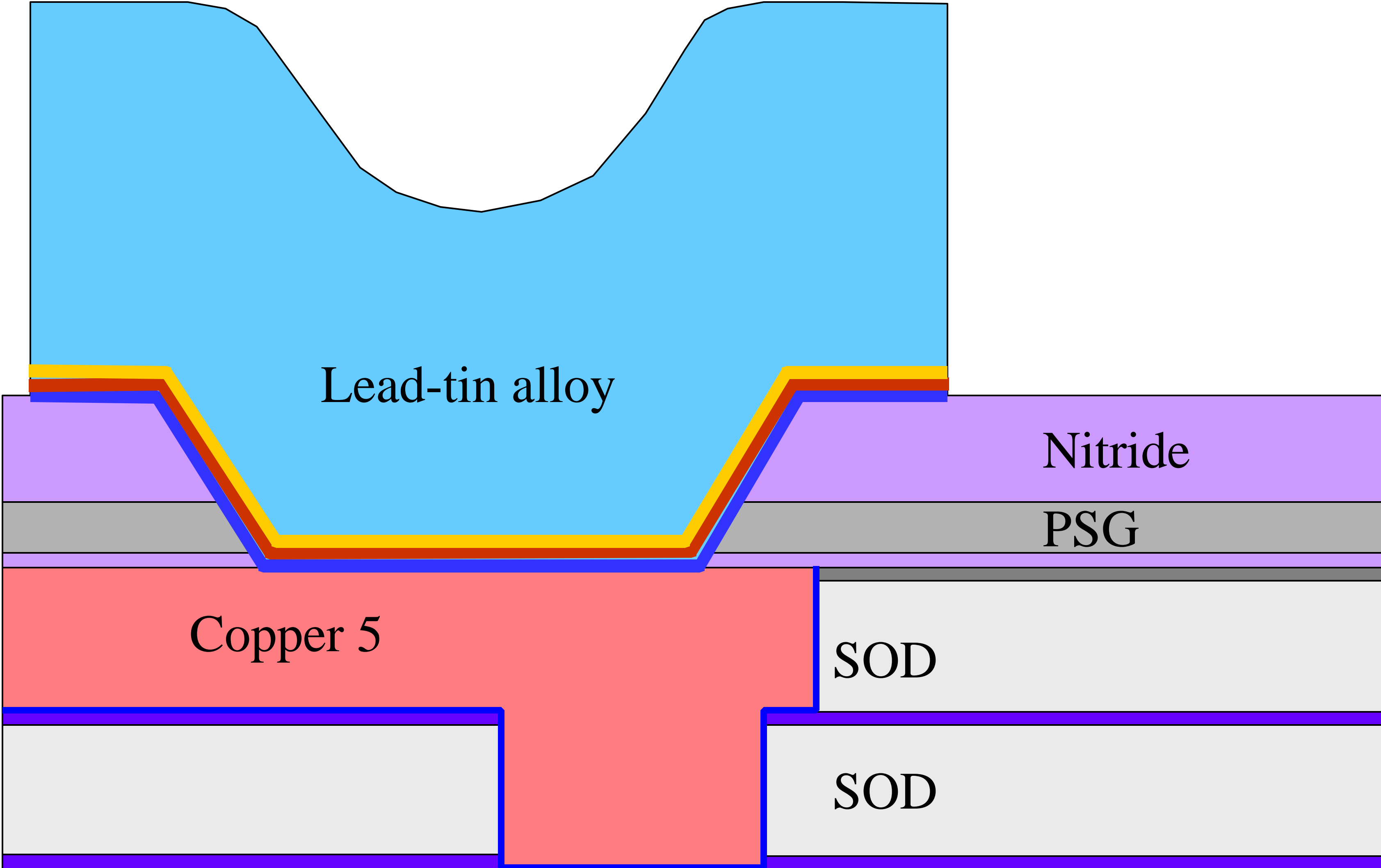
PR Coating, A&E, PEB, and Develop



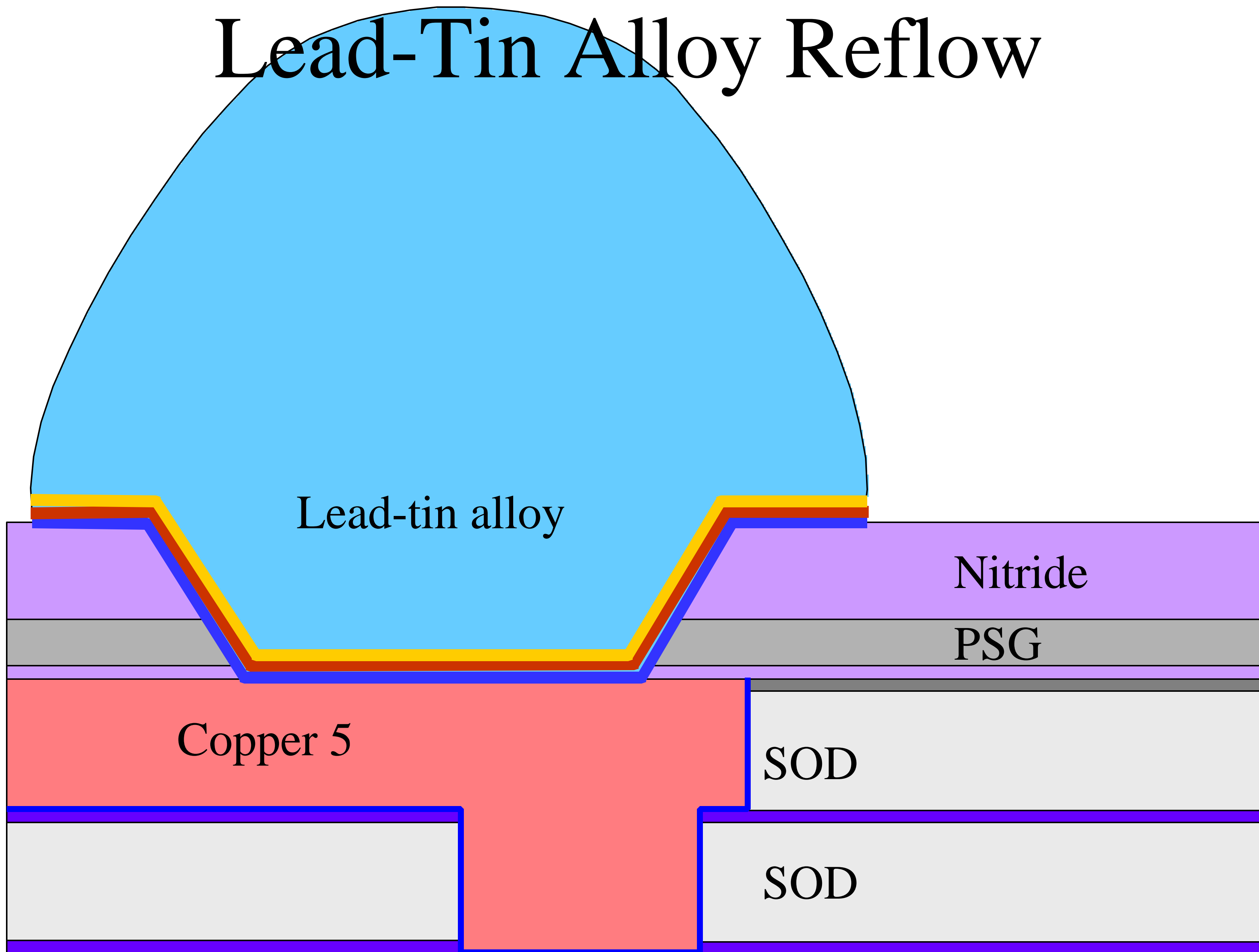
Metal Etch

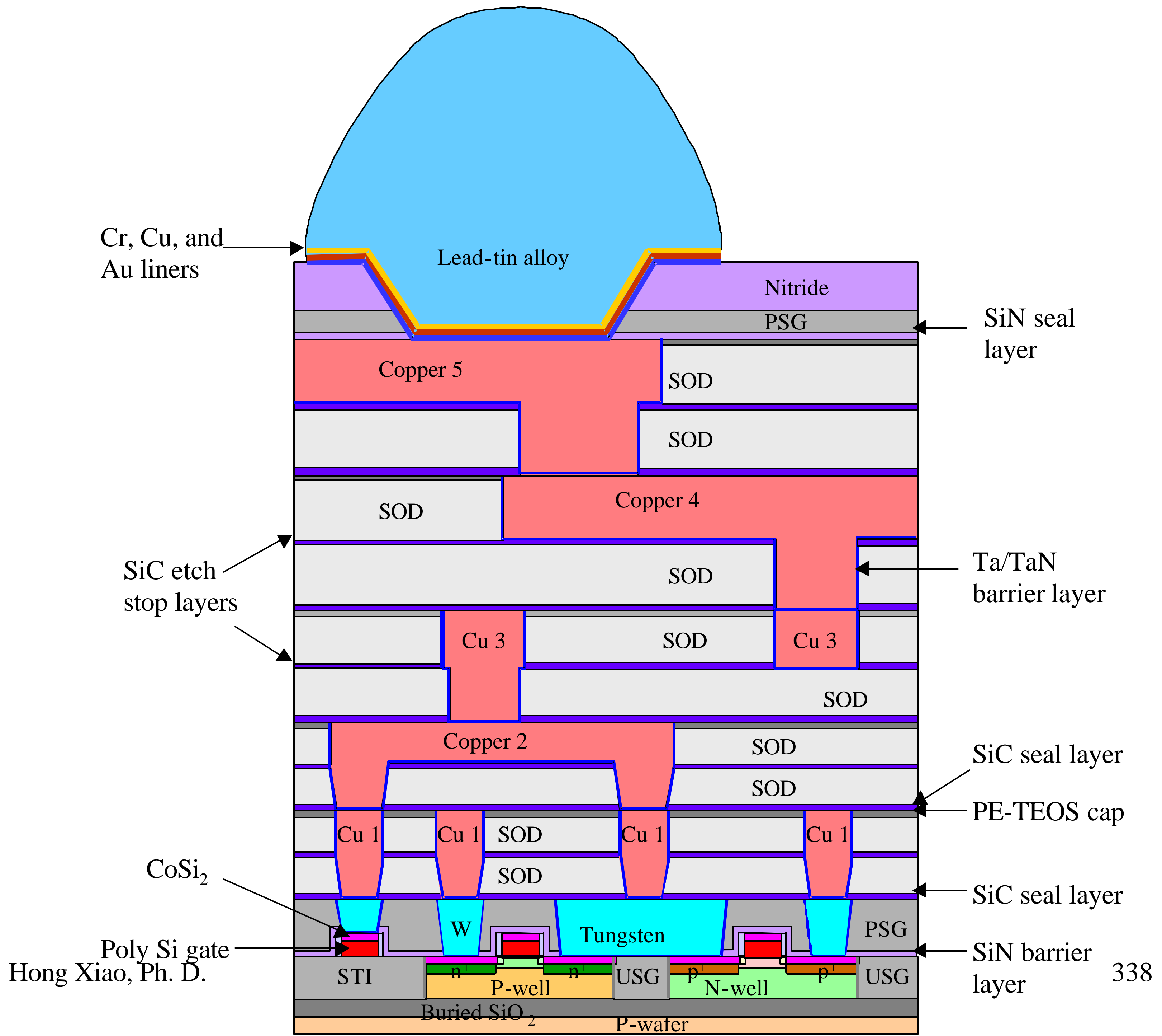


Strip Photoresist



Lead-Tin Alloy Reflow





Hong Xiao, Ph. D.

Summary

- CMOS IC chips dominate semiconductor industry
  - Demands for digital electronics, such as electronic watches, calculators, and personal computers

Summary

- In the 1980s
  - 3 micron to sub-micron
  - Multi-layer metallization
  - Tungsten CVD, dielectric CVD and metal sputtering
  - Sidewall spacer for LDD
  - Plasma etch gradually replaced wet etch in all patterning etch processes.
  - Steppers became popular for alignment and exposure while projection systems were widely used

Summary

- In the 1990s,
  - 0.8 micron to 0.18 micron
  - Silicides used for the gate and local interconnection
  - CMP widely used for tungsten polishing and dielectric planarization
  - RTP is widely used for anneal processes
  - HDP sources are used for etch, CVD, sputtering clean, and sputtering deposition
  - O_3-TEOS oxide CVD processes commonly used for STI, PMD and IMD depositions.
  - ECP is used for copper metallization process