Project: MOSFETs

Due : April 30, 2020

Design MOSFETs by TCAD device simulator Silvaco.

For atlas MOSFET case: (70%)

#Specifications:

1. **Channel length = 0.18 μm.**
2. **Gate oxide thickness = 3 nm.**
3. **Adequate threshold voltage = 0.5 ± 0.2 V.**

#Output: (in A4 format)

(1) Generate the device mesh for N-MOSFETs and P-MOSFETs. (as Figure 1) (10%)

(2) Plot I_d-V_g at V_{ds}= 1V for N-MOSFETs and P-MOSFETs. (as Figure 2) (20%)

(3) Plot I_d-V_d at V_{gs}= 0.6, 0.8, 1V for N-MOSFETs and P-MOSFETs. (as Figure 3) (20%)

(4) Shows the threshold voltage and subthreshold swing of your devices at V_{ds}= 1V (as Figure4) (10%)

(5) Upload all **.in** file. (10%)

For athena Inverter case: (30%)

#Specifications:

1. **Channel length = 0.18 μm.**
2. **STI isolation.**

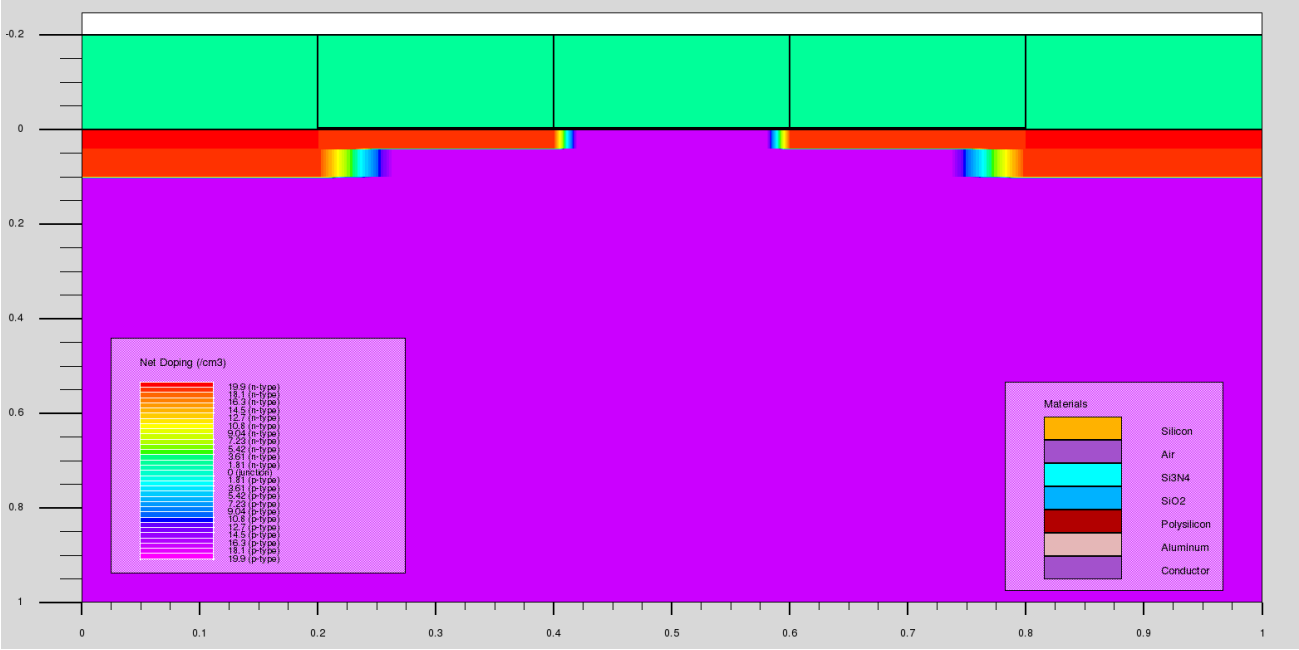
#Output: (in A4 format)

(1) Upload Inverter **.in** file. (10%)

(2) Generate the device for Inverter. (as Figure 5) (20%)

#Sample Plots:

N-MOSFET



P-MOSFET

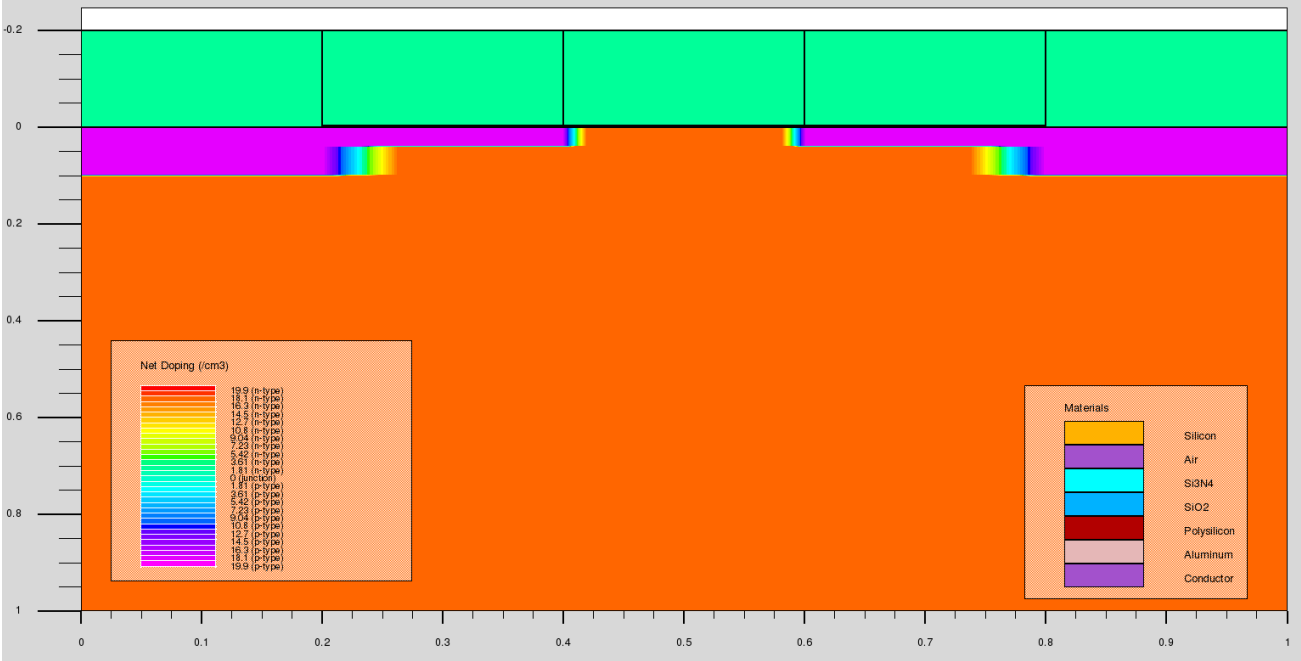
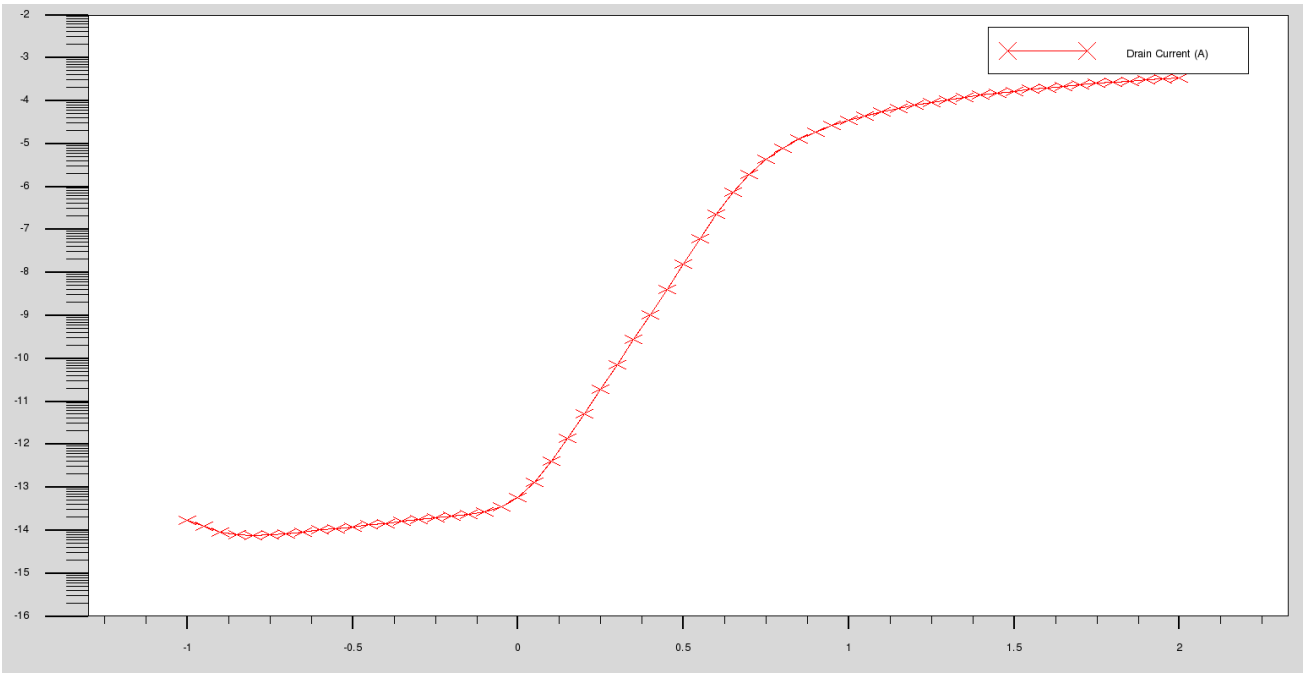


Figure 1

N-MOSFET



P-MOSFET

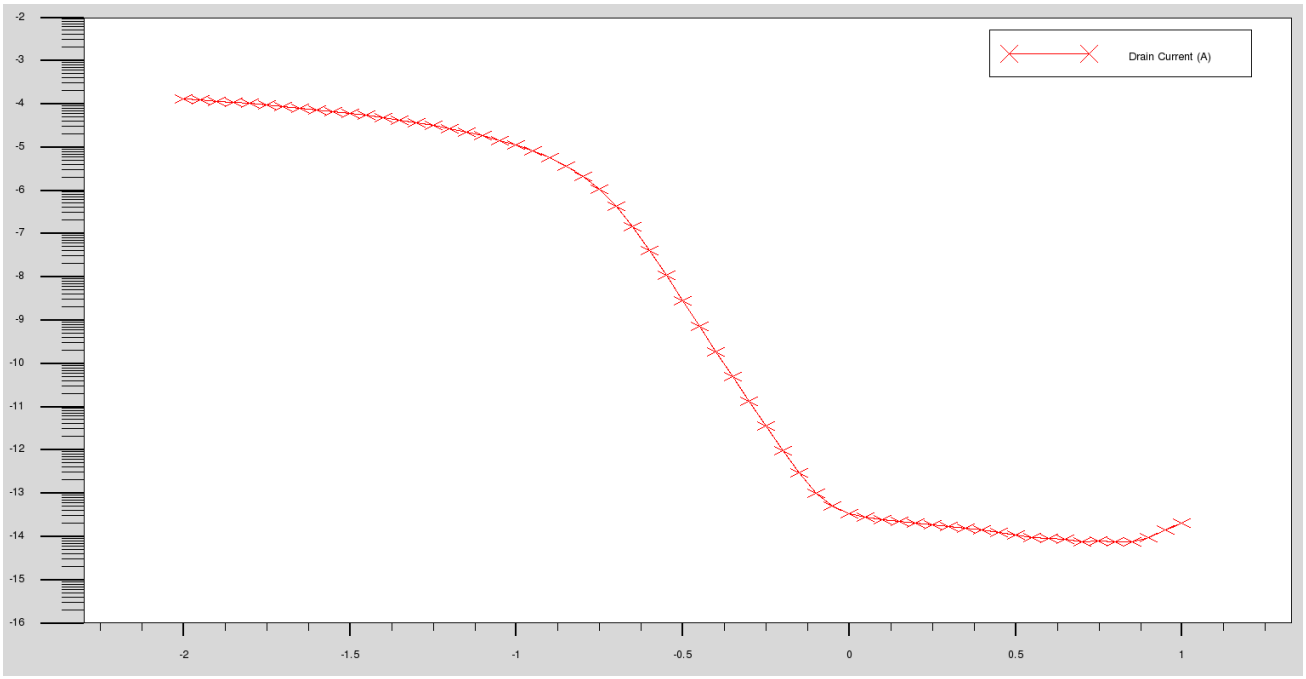
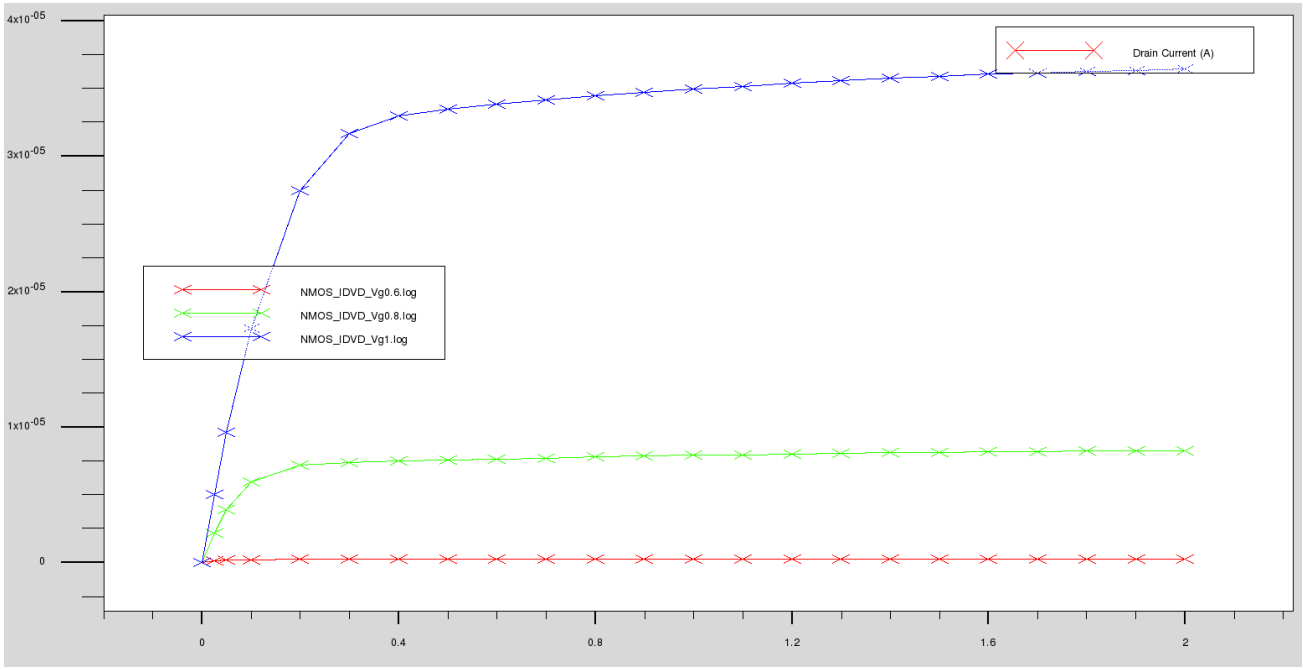


Figure 2

N-MOSFET



P-MOSFET

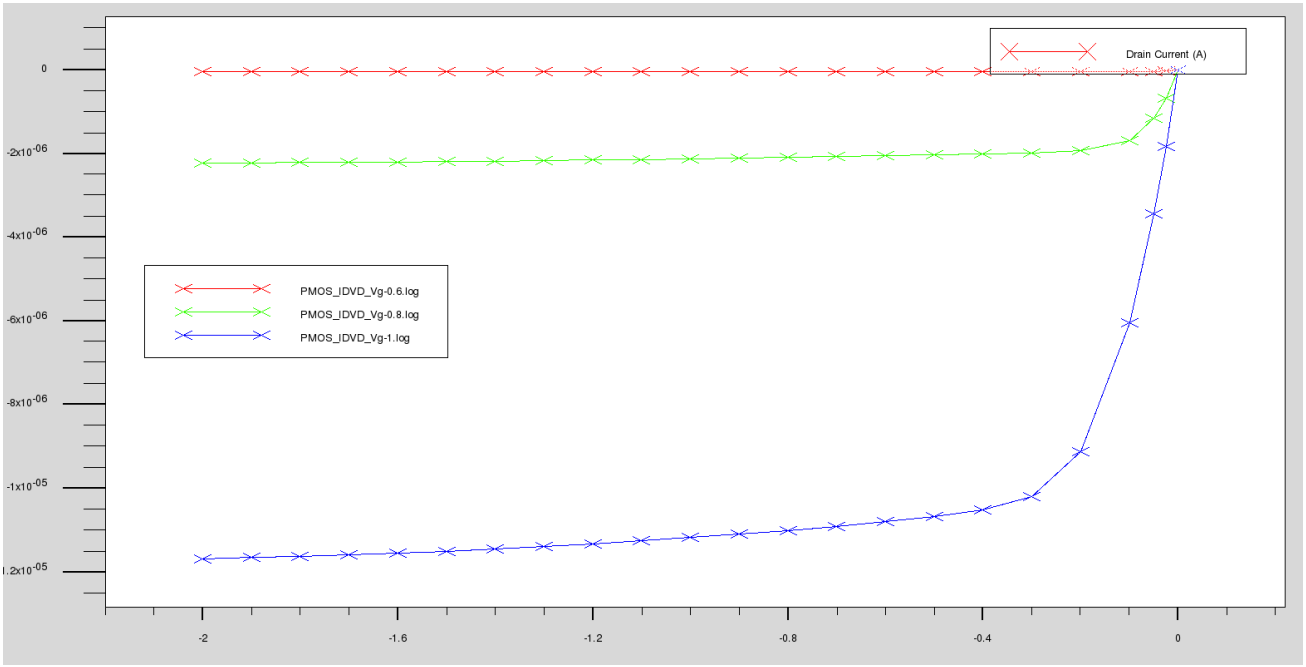


Figure 3

```
extract name="vt" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")))) - abs(ave(v."drain"))/2.0)
#
extract name="subvt" 1.0/slope(maxslope(curve(abs(v."gate"),log10(abs(i."drain")))))
```

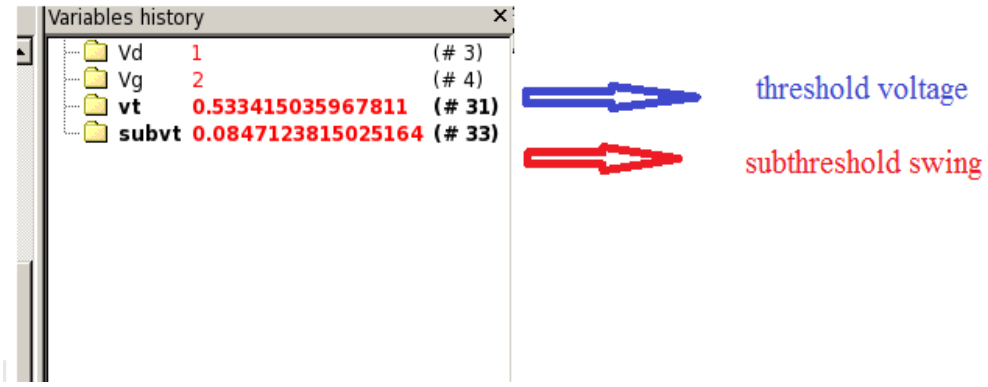


Figure 4

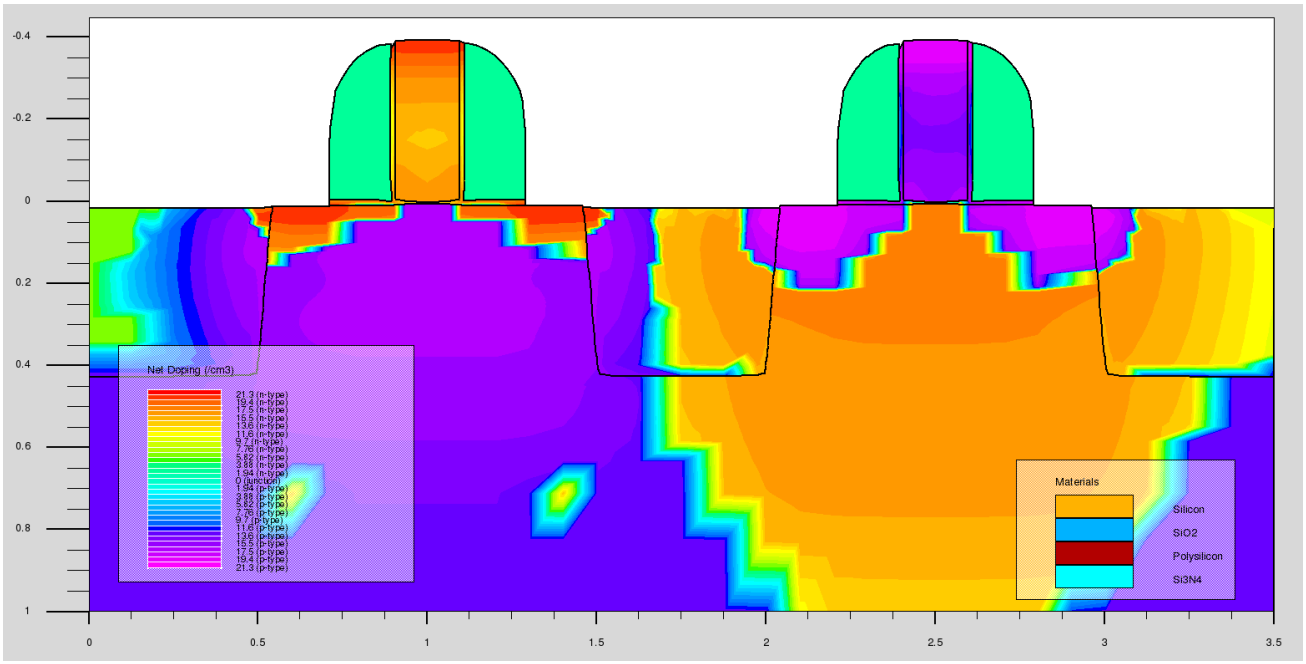


Figure 5